MT6797 LTE-A Smartphone Application Processor Register Table for Development Board (Part I)

Version: 1.0
Release date: 2016-07-19

Specifications are subject to change without notice.

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1.1 On-chip Memory Controller

Module name: sramrom_reg Base address: (+10202000h)

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10202010 SEC_VIO_STAT Security Violation Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sec_vio_rw						sec_vio_domain									
Type	RO						RO									
Reset	0						0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																sec_vio
Type																W1C
Reset																0

Bit(s)	Mnemonic	Name	Description
31		sec_vio_rw	**Direction of transaction which violates security setting** 0: Read 1: Write
25:24		sec_vio_domain	**Indicates which domain is the transaction which violates security setting** 00: Domain 0 01: Domain 1 10: Domain 2 11: Reserved
0		sec_vio	**Shows violation status of SRAMROM** 0: Normal 1: Security violation IRQ pending

10202014 SEC_VIO_ADDR **Security Violation Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sec_vio_addr															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sec_vio_addr															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		sec_vio_addr	Address of transaction which violates security setting

10202018 SEC_VIO_ACK **Security Violation Acknowledge Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																sec_vio_ack
Type																WO
Reset																0

Bit(s)	Mnemonic	Name	Description
0		sec_vio_ack	**Acknowledges security violation** Write any value to this register to clear SEC_VIO_STAT.sec_vio.

10202020 PWR_CTRL **80000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	rrb_en															
Type	RW															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																rom_swrst_b
Type																RW
Reset																1

Bit(s)	Mnemonic	Name	Description
31		rrb_en	
0		rom_swrst_b	

10202034 BOOT_META0 META Data Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_meta0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_meta0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_meta0	**Meta data register** General purpose register for boot-up process. Can be reset by WDT reset.

10202038 BOOT_META1 META Data Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_meta1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_meta1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_meta1	**Meta data register** General purpose register for boot-up process. Can be reset by WDT reset.

1020203C BOOT_META2 META Data Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_meta2															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_meta2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_meta2	**Meta data register** General purpose register for boot-up process. Can be reset by WDT reset.

10202040 BOOT_META3 META Data Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_meta3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_meta3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_meta3	**Meta data register** General purpose register for boot-up process. Can be reset by WDT reset.

10202050 BOOT_META_NR0 Non-resettable META Data Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_meta_nr0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_meta_nr0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_meta_nr0	**Meta data register** General purpose register for boot-up process. Can only be reset by HW reset; cannot be reset by WDT reset.

10202054 BOOT_META_NR1 Non-resettable META Data Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_meta_nr1															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_meta_nr1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_meta_nr1	**Meta data register** General purpose register for boot-up process. Can only be reset by HW reset; cannot be reset by WDT reset.

10202058 BOOT_META_NR2 **Non-resettable META Data Register 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_meta_nr2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_meta_nr2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_meta_nr2	**Meta data register** General purpose register for boot-up process. Can only be reset by HW reset; cannot be reset by WDT reset.

1020205C BOOT_META_NR3 **Non-resettable META Data Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_meta_nr3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_meta_nr3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_meta_nr3	**Meta data register** General purpose register for boot-up process. Can only be reset by HW reset; cannot be reset by WDT reset.

10202080 BOOT_MISC0 **Spare Register for Bootrom** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_misco	Spare register for bootrom

10202084 BOOT_MISC1 Spare Register for Bootrom 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_misco	Spare register for bootrom

10202088 BOOT_MISC2 Spare Register for Bootrom 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_misco	Spare register for bootrom

1020208C BOOT_MISC3 Spare Register for Bootrom 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_misco	Spare register for bootrom

10202090 BOOT_MISC4 Spare Register for Bootrom 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_misco	Spare register for bootrom

10202094 BOOT_MISC5 Spare Register for Bootrom 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_misco	Spare register for bootrom

10202098 BOOT_MISC6 Spare Register for Bootrom 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_misco	Spare register for bootrom

1020209C BOOT_MISC7 Spare Register for Bootrom 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_misco															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_misc0	Spare register for bootrom

102020A0 MISC_LOCK_KEY — Key for Write Misc Control Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	misc_lock_key															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		misc_lock_key	Key for write misc control register

102020A4 MISC_LOCK_CON — Lock for Write Misc Data Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									misc_lock_con							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		misc_lock_con	Lock for write misc data register

102020A8 MISC_RST_CON — Reset Control for Misc Data Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									misc_rst_con							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		misc_rst_con	**Reset control for misc data register**

102020AC MISC_SEC_CON **Security Control for Misc Data Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								misc_sec_con								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		misc_sec_con	Security control for misc data register

1.2 External Interrupt Controller

Module name: ap_cirq_eint Base address: (+1000b000h)

Address	Name	Width	Register Function
1000B000	EINT_STA0	32	External Interrupt Status Register
1000B004	EINT_STA1	32	External Interrupt Status Register
1000B008	EINT_STA2	32	External Interrupt Status Register
1000B00C	EINT_STA3	32	External Interrupt Status Register
1000B010	EINT_STA4	32	External Interrupt Status Register
1000B014	EINT_STA5	32	External Interrupt Status Register
1000B040	EINT_ACK0	32	External Interrupt Acknowledge Register
1000B044	EINT_ACK1	32	External Interrupt Acknowledge Register
1000B048	EINT_ACK2	32	External Interrupt Acknowledge Register
1000B04C	EINT_ACK3	32	External Interrupt Acknowledge Register
1000B050	EINT_ACK4	32	External Interrupt Acknowledge Register
1000B054	EINT_ACK5	32	External Interrupt Acknowledge Register
1000B080	EINT_MASK0	32	External Interrupt Mask Register
1000B084	EINT_MASK1	32	External Interrupt Mask Register
1000B088	EINT_MASK2	32	External Interrupt Mask Register
1000B08C	EINT_MASK3	32	External Interrupt Mask Register
1000B090	EINT_MASK4	32	External Interrupt Mask Register
1000B094	EINT_MASK5	32	External Interrupt Mask Register
1000B0C0	EINT_MASK_SET0	32	External Interrupt Mask Set Register
1000B0C4	EINT_MASK_SET1	32	External Interrupt Mask Set Register
1000B0C8	EINT_MASK_SET2	32	External Interrupt Mask Set Register
1000B0CC	EINT_MASK_SET3	32	External Interrupt Mask Set Register
1000B0D0	EINT_MASK_SET4	32	External Interrupt Mask Set Register
1000B0D4	EINT_MASK_SET5	32	External Interrupt Mask Set Register
1000B100	EINT_MASK_CLR0	32	External Interrupt Mask Set Register
1000B104	EINT_MASK_CLR1	32	External Interrupt Mask Set Register
1000B108	EINT_MASK_CLR2	32	External Interrupt Mask Set Register
1000B10C	EINT_MASK_CLR3	32	External Interrupt Mask Set Register
1000B110	EINT_MASK_CLR4	32	External Interrupt Mask Set Register
1000B114	EINT_MASK_CLR5	32	External Interrupt Mask Set Register
1000B140	EINT_SENS0	32	External Interrupt Sensitivity Register
1000B144	EINT_SENS1	32	External Interrupt Sensitivity Register
1000B148	EINT_SENS2	32	External Interrupt Sensitivity Register
1000B14C	EINT_SENS3	32	External Interrupt Sensitivity Register
1000B150	EINT_SENS4	32	External Interrupt Sensitivity Register
1000B154	EINT_SENS5	32	External Interrupt Sensitivity Register
1000B180	EINT_SENS_SET0	32	External Interrupt Sensitivity Set Register
1000B184	EINT_SENS_SET1	32	External Interrupt Sensitivity Set Register
1000B188	EINT_SENS_SET2	32	External Interrupt Sensitivity Set Register
1000B18C	EINT_SENS_SET3	32	External Interrupt Sensitivity Set Register
1000B190	EINT_SENS_SET4	32	External Interrupt Sensitivity Set Register
1000B194	EINT_SENS_SET5	32	External Interrupt Sensitivity Set Register
1000B1C0	EINT_SENS_CLR0	32	External Interrupt Sensitivity Clear Register

Address	Name	Width	Register Function
1000B1C4	EINT_SENS_CLR1	32	External Interrupt Sensitivity Clear Register
1000B1C8	EINT_SENS_CLR2	32	External Interrupt Sensitivity Clear Register
1000B1CC	EINT_SENS_CLR3	32	External Interrupt Sensitivity Clear Register
1000B1D0	EINT_SENS_CLR4	32	External Interrupt Sensitivity Clear Register
1000B1D4	EINT_SENS_CLR5	32	External Interrupt Sensitivity Clear Register
1000B200	EINT_SOFT0	32	Software Interrupt Register
1000B204	EINT_SOFT1	32	Software Interrupt Register
1000B208	EINT_SOFT2	32	Software Interrupt Register
1000B20C	EINT_SOFT3	32	Software Interrupt Register
1000B210	EINT_SOFT4	32	Software Interrupt Register
1000B214	EINT_SOFT5	32	Software Interrupt Register
1000B240	EINT_SOFT_SET0	32	Software Interrupt Set Register
1000B244	EINT_SOFT_SET1	32	Software Interrupt Set Register
1000B248	EINT_SOFT_SET2	32	Software Interrupt Set Register
1000B24C	EINT_SOFT_SET3	32	Software Interrupt Set Register
1000B250	EINT_SOFT_SET4	32	Software Interrupt Set Register
1000B254	EINT_SOFT_SET5	32	Software Interrupt Set Register
1000B280	EINT_SOFT_CLR0	32	Software Interrupt Clear Register
1000B284	EINT_SOFT_CLR1	32	Software Interrupt Clear Register
1000B288	EINT_SOFT_CLR2	32	Software Interrupt Clear Register
1000B28C	EINT_SOFT_CLR3	32	Software Interrupt Clear Register
1000B290	EINT_SOFT_CLR4	32	Software Interrupt Clear Register
1000B294	EINT_SOFT_CLR5	32	Software Interrupt Clear Register
1000B300	EINT_POL0	32	External Interrupt Polarity Register
1000B304	EINT_POL1	32	External Interrupt Polarity Register
1000B308	EINT_POL2	32	External Interrupt Polarity Register
1000B30C	EINT_POL3	32	External Interrupt Polarity Register
1000B310	EINT_POL4	32	External Interrupt Polarity Register
1000B314	EINT_POL5	32	External Interrupt Polarity Register
1000B340	EINT_POL_SET0	32	External Interrupt Polarity Set Register
1000B344	EINT_POL_SET1	32	External Interrupt Polarity Set Register
1000B348	EINT_POL_SET2	32	External Interrupt Polarity Set Register
1000B34C	EINT_POL_SET3	32	External Interrupt Polarity Set Register
1000B350	EINT_POL_SET4	32	External Interrupt Polarity Set Register
1000B354	EINT_POL_SET5	32	External Interrupt Polarity Set Register
1000B380	EINT_POL_CLR0	32	External Interrupt Polarity Clear Register
1000B384	EINT_POL_CLR1	32	External Interrupt Polarity Clear Register
1000B388	EINT_POL_CLR2	32	External Interrupt Polarity Clear Register
1000B38C	EINT_POL_CLR3	32	External Interrupt Polarity Clear Register
1000B390	EINT_POL_CLR4	32	External Interrupt Polarity Clear Register
1000B394	EINT_POL_CLR5	32	External Interrupt Polarity Clear Register
1000B400	EINT_D0EN0	32	Domain 0 External Interrupt Enable Control Register
1000B404	EINT_D0EN1	32	Domain 0 External Interrupt Enable Control Register
1000B408	EINT_D0EN2	32	Domain 0 External Interrupt Enable Control Register
1000B40C	EINT_D0EN3	32	Domain 0 External Interrupt Enable Control Register
1000B410	EINT_D0EN4	32	Domain 0 External Interrupt Enable Control Register

Address	Name	Width	Register Function
1000B414	EINT_D0EN5	32	Domain 0 External Interrupt Enable Control Register
1000B500	EINT_DBNC_3_0	32	External Interrupt Debounce Control Register
1000B600	EINT_DBNC_SET_3_0	32	External Interrupt Debounce Control Register
1000B700	EINT_DBNC_CLR_3_0	32	External Interrupt Debounce Control Register
1000B800	DEINT_CON	32	Direct Couple EINT Control Register
1000B840	DEINT_SEL_3_0	32	Direct Couple EINT Select Control Register
1000B880	DEINT_SEL_SET_3_0	32	Direct Couple EINT Select Control Set Register
1000B8C0	DEINT_SEL_CLR_3_0	32	Direct Couple EINT Select Control Clear Register
1000B900	EINT_EEVT	32	EINT Wakeup Event Status Register
1000BA00	EINT_RAW_STA0	32	External Interrupt Raw Status Register
1000BA04	EINT_RAW_STA1	32	External Interrupt Raw Status Register
1000BA08	EINT_RAW_STA2	32	External Interrupt Raw Status Register
1000BA0C	EINT_RAW_STA3	32	External Interrupt Raw Status Register
1000BA10	EINT_RAW_STA4	32	External Interrupt Raw Status Register
1000BA14	EINT_RAW_STA5	32	External Interrupt Raw Status Register
1000B504	EINT_DBNC_7_4	32	External Interrupt Debounce Control Register
1000B604	EINT_DBNC_SET_7_4	32	External Interrupt Debounce Control Register
1000B704	EINT_DBNC_CLR_7_4	32	External Interrupt Debounce Control Register
1000B508	EINT_DBNC_B_8	32	External Interrupt Debounce Control Register
1000B608	EINT_DBNC_SET_B_8	32	External Interrupt Debounce Control Register
1000B708	EINT_DBNC_CLR_B_8	32	External Interrupt Debounce Control Register
1000B50C	EINT_DBNC_F_C	32	External Interrupt Debounce Control Register
1000B60C	EINT_DBNC_SET_F_C	32	External Interrupt Debounce Control Register
1000B70C	EINT_DBNC_CLR_F_C	32	External Interrupt Debounce Control Register
1000B5B0	EINT_DBNC_B_3_0	32	External Interrupt Debounce Control Register
1000B6B0	EINT_DBNC_SET_B_3_0	32	External Interrupt Debounce Control Register
1000B7B0	EINT_DBNC_CLR_B_3_0	32	External Interrupt Debounce Control Register
1000B5B4	EINT_DBNC_B_7_4	32	External Interrupt Debounce Control Register
1000B6B4	EINT_DBNC_SET_B_7_4	32	External Interrupt Debounce Control Register
1000B7B4	EINT_DBNC_CLR_B_7_4	32	External Interrupt Debounce Control Register
1000BC00	EINT_SYNC_EN0	32	
1000BC04	EINT_SYNC_EN1	32	
1000BD00	EINT_SYNC_EN_SET_0	32	
1000BD04	EINT_SYNC_EN_SET_1	32	

Address	Name	Width	Register Function
1000BE00	EINT_SYNC_EN_CLR_0	32	
1000BE04	EINT_SYNC_EN_CLR_1	32	
1000BF00	FPGA_EMUL_0	32	FPGA EMUL Register 0
1000BF04	FPGA_EMUL_1	32	FPGA EMUL Register 1
1000BF08	FPGA_EMUL_2	32	FPGA EMUL Register 2
1000BF0C	FPGA_EMUL_3	32	FPGA EMUL Register 3
1000BF10	FPGA_EMUL_4	32	FPGA EMUL Register 4
1000BB00	SECURE_EINT_EN	32	SECURE_EINT_EN
1000BB10	SECURE_DIR_EINT_EN	32	SECURE_DIR_EINT_EN
1000BB20	DCM_ON	32	DCM_ON
1000BB30	SECURE_STATUS	32	SECURE_STATUS

1000B000 EINT_STA0 External Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_PEND0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_PEND0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_PEND0	**Each bit read as 1 indicates the corresponding external interrupt is pending.** 1: Compare AXI ID[9:0] (include gid[1:0])

1000B004 EINT_STA1 External Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_PEND1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_PEND1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_PEND1	**Each bit read as 1 indicates the corresponding external interrupt is pending.** 1: Compare AXI ID[9:0] (include gid[1:0])

1000B008 EINT_STA2 External Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_PEND2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_PEND2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_PEND2	**Each bit read as 1 indicates the corresponding external interrupt is pending.** 1: Compare AXI ID[9:0] (include gid[1:0])

1000B00C EINT_STA3 External Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_PEND3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_PEND3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_PEND3	**Each bit read as 1 indicates the corresponding external interrupt is pending.** 1: Compare AXI ID[9:0] (include gid[1:0])

1000B010 EINT_STA4 External Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_PEND4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_PEND4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_PEND4	**Each bit read as 1 indicates the corresponding external interrupt is pending.** 1: Compare AXI ID[9:0] (include gid[1:0])

1000B014 EINT_STA5 External Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_PEND5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_PEND5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_PEND5	**Each bit read as 1 indicates the corresponding external interrupt is pending.** 1: Compare AXI ID[9:0] (include gid[1:0])

1000B040 EINT_ACK0 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_ACK0	Write 1 to specific bit to acknowledge the corresponding external interrupt.

1000B044 EINT_ACK1 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_ACK1	Write 1 to specific bit to acknowledge the corresponding external interrupt.

1000B048 EINT_ACK2 External Interrupt Acknowledge 00000000

Register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_ACK2	Write 1 to specific bit to acknowledge the corresponding external interrupt.

1000B04C EINT_ACK3 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_ACK3	Write 1 to specific bit to acknowledge the corresponding external interrupt.

1000B050 EINT_ACK4 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_ACK4	Write 1 to specific bit to acknowledge the corresponding external interrupt.

1000B054 EINT_ACK5 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK5															

Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_ACK5	Write 1 to specific bit to acknowledge the corresponding external interrupt.

1000B080 EINT_MASK0 External Interrupt Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK0	External interrupt mask value

1000B084 EINT_MASK1 External Interrupt Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK1															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK1															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK1	External interrupt mask value

1000B088 EINT_MASK2 External Interrupt Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK2															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK2															
Type	RO															

Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK2	External interrupt mask value

1000B08C EINT_MASK3 External Interrupt Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK3															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK3															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK3	External interrupt mask value

1000B090 EINT_MASK4 External Interrupt Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK4															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK4															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK4	External interrupt mask value

1000B094 EINT_MASK5 External Interrupt Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK5															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK5															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK5	External interrupt mask value

1000B0C0 EINT_MASK_SET0 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET0	Write 1 to specific bit to set up the mask of corresponding external interrupt.

1000B0C4 EINT_MASK_SET1 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET1	Write 1 to specific bit to set up the mask of corresponding external interrupt.

1000B0C8 EINT_MASK_SET2 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET2	Write 1 to specific bit to set up the mask of corresponding external interrupt.

1000B0CC EINT_MASK_ External Interrupt Mask Set Register 00000000

SET3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET3	Write 1 to specific bit to set up the mask of corresponding external interrupt.

1000B0D0 EINT_MASK_SET4 **External Interrupt Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET4	Write 1 to specific bit to set up the mask of corresponding external interrupt.

1000B0D4 EINT_MASK_SET5 **External Interrupt Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET5	Write 1 to specific bit to set up the mask of corresponding external interrupt.

1000B100 EINT_MASK_CLR0 **External Interrupt Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR0															

Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR0	Write 1 to specific bit to set up the mask of corresponding external interrupt.

1000B104 EINT_MASK_CLR1 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR1	Write 1 to specific bit to set up the mask of corresponding external interrupt.

1000B108 EINT_MASK_CLR2 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR2	Write 1 to specific bit to set up the mask of corresponding external interrupt.

1000B10C EINT_MASK_CLR3 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	EINT_MASK_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR3	Write 1 to specific bit to set up the mask of corresponding external interrupt.

1000B110 EINT_MASK_CLR4 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR4	Write 1 to specific bit to set up the mask of corresponding external interrupt.

1000B114 EINT_MASK_CLR5 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR5	Write 1 to specific bit to set up the mask of corresponding external interrupt.

1000B140 EINT_SENS0 External Interrupt Sensitivity Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS0	External interrupt sensitivity value

1000B144 EINT_SENS1 External Interrupt Sensitivity Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS1															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS1															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS1	External interrupt sensitivity value

1000B148 EINT_SENS2 External Interrupt Sensitivity Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS2															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS2															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS2	External interrupt sensitivity value

1000B14C EINT_SENS3 External Interrupt Sensitivity Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS3															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS3															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS3	External interrupt sensitivity value

1000B150 EINT_SENS4 External Interrupt Sensitivity Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS4															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS4															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS4	External interrupt sensitivity value

1000B154 EINT_SENS5 External Interrupt Sensitivity Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS5															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS5															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS5	External interrupt sensitivity value

1000B180 EINT_SENS_SET0 External Interrupt Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET0	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

1000B184 EINT_SENS_SET1 External Interrupt Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_SET1															

Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET1	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

1000B188 EINT_SENS_SET2 External Interrupt Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET2	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

1000B18C EINT_SENS_SET3 External Interrupt Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET3	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

1000B190 EINT_SENS_SET4 External Interrupt Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	EINT_SENS_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET4	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

1000B194 EINT_SENS_SET5 — External Interrupt Sensitivity Set Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET5	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

1000B1C0 EINT_SENS_CLR0 — External Interrupt Sensitivity Clear Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR0	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

1000B1C4 EINT_SENS_CLR1 — External Interrupt Sensitivity Clear Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR1	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

1000B1C8 EINT_SENS_CLR2 External Interrupt Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR2	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

1000B1CC EINT_SENS_CLR3 External Interrupt Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR3	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

1000B1D0 EINT_SENS_CLR4 External Interrupt Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR4	Write 1 to specific bit to set up the sensitivity of

Bit(s)	Mnemonic	Name	Description
			corresponding external interrupt.

1000B1D4 EINT_SENS_CLR5 — **External Interrupt Sensitivity Clear Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR5	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

1000B200 EINT_SOFT0 — **Software Interrupt Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT0	Software interrupt value

1000B204 EINT_SOFT1 — **Software Interrupt Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT1	Software interrupt value

1000B208 EINT_SOFT2 — **Software Interrupt Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	EINT_SOFT2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT2	Software interrupt value

1000B20C EINT_SOFT3 Software Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT3	Software interrupt value

1000B210 EINT_SOFT4 Software Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT4	Software interrupt value

1000B214 EINT_SOFT5 Software Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT5	Software interrupt value

1000B240 EINT_SOFT_SET0 Software Interrupt Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET0	Write 1 to specific bit to set up the corresponding software interrupt.

1000B244 EINT_SOFT_SET1 Software Interrupt Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET1	Write 1 to specific bit to set up the corresponding software interrupt.

1000B248 EINT_SOFT_SET2 Software Interrupt Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET2	Write 1 to specific bit to set up the corresponding software interrupt.

1000B24C EINT_SOFT_SET3 **Software Interrupt Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET3	Write 1 to specific bit to set up the corresponding software interrupt.

1000B250 EINT_SOFT_SET4 **Software Interrupt Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET4	Write 1 to specific bit to set up the corresponding software interrupt.

1000B254 EINT_SOFT_SET5 **Software Interrupt Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET5	Write 1 to specific bit to set up the corresponding software interrupt.

1000B280 EINT_SOFT_ **Software Interrupt Clear Register** **00000000**

CLR0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CLR0	Write 1 to specific bit to set up the corresponding software interrupt.

1000B284 EINT_SOFT_CLR1 Software Interrupt Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CLR1	Write 1 to specific bit to set up the corresponding software interrupt.

1000B288 EINT_SOFT_CLR2 Software Interrupt Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CLR2	Write 1 to specific bit to set up the corresponding software interrupt.

1000B28C EINT_SOFT_CLR3 Software Interrupt Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR3															

Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CLR3	Write 1 to specific bit to set up the corresponding software interrupt.

1000B290 EINT_SOFT_CLR4 Software Interrupt Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CLR4	Write 1 to specific bit to set up the corresponding software interrupt.

1000B294 EINT_SOFT_CLR5 Software Interrupt Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CLR5	Write 1 to specific bit to set up the corresponding software interrupt.

1000B300 EINT_POL0 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	EINT_POL0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL0	External interrupt polarity value

1000B304 EINT_POL1 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL1	External interrupt polarity value

1000B308 EINT_POL2 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL2	External interrupt polarity value

1000B30C EINT_POL3 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL3	External interrupt polarity value

1000B310 EINT_POL4 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL4	External interrupt polarity value

1000B314 EINT_POL5 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL5	External interrupt polarity value

1000B340 EINT_POL_SET0 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET0	Write 1 to specific bit to set up the polarity of corresponding external interrupt.

1000B344 EINT_POL_SET1 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET1	Write 1 to specific bit to set up the polarity of corresponding external interrupt.

1000B348 EINT_POL_SET2 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET2	Write 1 to specific bit to set up the polarity of corresponding external interrupt.

1000B34C EINT_POL_SET3 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET3	Write 1 to specific bit to set up the polarity of corresponding external interrupt.

1000B350 EINT_POL_SET4 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	EINT_POL_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET4	Write 1 to specific bit to set up the polarity of corresponding external interrupt.

1000B354 EINT_POL_SET5 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET5	Write 1 to specific bit to set up the polarity of corresponding external interrupt.

1000B380 EINT_POL_CLR0 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR0	Write 1 to specific bit to clear the polarity of corresponding external interrupt.

1000B384 EINT_POL_CLR1 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR1	Write 1 to specific bit to clear the polarity of corresponding external interrupt.

1000B388 EINT_POL_CLR2 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR2	Write 1 to specific bit to clear the polarity of corresponding external interrupt.

1000B38C EINT_POL_CLR3 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR3	Write 1 to specific bit to clear the polarity of corresponding external interrupt.

1000B390 EINT_POL_CLR4 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR4															
Type	WO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR4	Write 1 to specific bit to clear the polarity of corresponding external interrupt.

1000B394 EINT_POL_CLR5 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR5	Write 1 to specific bit to clear the polarity of corresponding external interrupt.

1000B400 EINT_DOEN0 Domain 0 External Interrupt Enable Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_DOEN0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_DOEN0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_DOEN0	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

1000B404 EINT_DOEN1 Domain 0 External Interrupt Enable Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_DOEN1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_DOEN1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_D0EN1	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

1000B408 EINT_D0EN2 Domain 0 External Interrupt Enable Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_D0EN2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D0EN2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_D0EN2	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

1000B40C EINT_D0EN3 Domain 0 External Interrupt Enable Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_D0EN3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D0EN3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_D0EN3	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

1000B410 EINT_D0EN4 Domain 0 External Interrupt Enable Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_D0EN4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D0EN4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_D0EN4	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

Bit(s)	Mnemonic	Name	Description

1000B414 EINT_D0EN5 **Domain 0 External Interrupt Enable Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_D0EN5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D0EN5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_D0EN5	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

1000B500 EINT_DBNC_3_0 **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING3						DBNC_RST3	EN3	DBNC_SETTING2						DBNC_RST2	EN2
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING1						DBNC_RST1	EN1	DBNC_SETTING0						DBNC_RST0	EN0
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING3	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST3	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN3	**Enables de-bounce function** 0: Disable 1: Enable

Bit(s)	Mnemonic	Name	Description
23:20		DBNC_SETTING2	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST2	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN2	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING1	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST1	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN1	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING0	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST0	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN0	**Enables de-bounce function** 0: Disable 1: Enable

Bit(s)	Mnemonic	Name	Description

1000B600 EINT_DBNC_SET_3_0 **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET3						DBNC_RST_SET3	EN_SET3	DBNC_SETTING_SET2						DBNC_RST_SET2	EN_SET2
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_SET1						DBNC_RST_SET1	EN_SET1	DBNC_SETTING_SET0						DBNC_RST_SET0	EN_SET0
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_SET3	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST_SET3	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_SET3	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING_SET2	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST_SET2	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_SET2	**Enables de-bounce function** 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable
15:12		DBNC_SETTING_SET1	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST_SET1	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_SET1	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_SET0	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST_SET0	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_SET0	**Enables de-bounce function** 0: Disable 1: Enable

1000B700 EINT_DBNC_CLR_3_0 — **External Interrupt Debounce Control Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR3						DBNC_RST3	EN_CLR3		DBNC_SETTING_CLR_CLR2					DBNC_RST2	EN_CLR2
Type	WO						WO	WO		WO					WO	WO
Reset	0	0	0	0			0	0		0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_CLR1						DBNC_RST1	EN_CLR1	DBNC_SETTING_CLR_CLR0						DBNC_RST0	EN_CLR0
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_CLR_CLR3	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST3	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_CLR3	**Enables de-bounce function** 0: Disable 1: Enable
22:20		DBNC_SETTING_CLR_CLR2	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST2	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_CLR2	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_CLR_CLR1	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST1	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_CLR1	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_C	**De-bounce setting**

Bit(s)	Mnemonic	Name	Description
		LR_CLR0	0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST0	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_CLR0	**Enables de-bounce function** 0: Disable 1: Enable

1000B800 DEINT_CON **Direct Couple EINT Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DEINT_CON3	DEINT_CON2	DEINT_CON1	DEINT_CON0
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3		DEINT_CON3	**Controls direct couple EINT3** 0: Disable 1: Enable
2		DEINT_CON2	**Controls direct couple EINT2** 0: Disable 1: Enable
1		DEINT_CON1	**Controls direct couple EINT1** 0: Disable 1: Enable
0		DEINT_CON0	**Controls direct couple EINT0** 0: Disable 1: Enable

1000B840 DEINT_SEL_3_0 **Direct Couple EINT Select Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEINT_SEL3								DEINT_SEL2							
Type	RO								RO							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEINT_SEL1								DEINT_SEL0							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		DEINT_SEL3	**Selects direct couple EINT3** #: EINT number
23:16		DEINT_SEL2	**Selects direct couple EINT2** #: EINT number
15:8		DEINT_SEL1	**Selects direct couple EINT1** #: EINT number
7:0		DEINT_SEL0	**Selects direct couple EINT0** #: EINT number

1000B880 DEINT_SEL_SET_3_0 **Direct Couple EINT Select Control Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEINT_SEL3								DEINT_SEL2							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEINT_SEL1								DEINT_SEL0							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		DEINT_SEL3	**Sets up direct couple EINT3 selection** #: EINT number
23:16		DEINT_SEL2	**Sets up direct couple EINT2 selection** #: EINT number
15:8		DEINT_SEL1	**Sets up direct couple EINT1 selection** #: EINT number
7:0		DEINT_SEL0	**Sets up direct couple EINT0 selection** #: EINT number

1000B8C0 DEINT_SEL_CLR_3_0 **Direct Couple EINT Select Control Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEINT_SEL3								DEINT_SEL2							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEINT_SEL1								DEINT_SEL0							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
31:24		DEINT_SEL3	**Clears direct couple EINT3 selection** #: EINT number
23:16		DEINT_SEL2	**Clears direct couple EINT2 selection** #: EINT number
15:8		DEINT_SEL1	**Clears direct couple EINT1 selection** #: EINT number
7:0		DEINT_SEL0	**Clears direct couple EINT0 selection** #: EINT number

1000B900 EINT_EEVT **EINT Wakeup Event Status Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EINT_EEVT
Type																RO
Reset																1

Bit(s)	Mnemonic	Name	Description
0		EINT_EEVT	EINT wakeup event status

1000BA00 EINT_RAW_STA0 **External Interrupt Raw Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_RAW_PEND0	**Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it's mask or not).** 1: Compare AXI ID[9:0] (include gid[1:0])

1000BA04 EINT_RAW_STA1 **External Interrupt Raw Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND1															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_RAW_PEND1	**Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it is mask or not).** 1: Compare AXI ID[9:0] (include gid[1:0])

1000BA08 EINT_RAW_STA2 **External Interrupt Raw Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_RAW_PEND2	**Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it is mask or not).** 1: Compare AXI ID[9:0] (include gid[1:0])

1000BA0C EINT_RAW_STA3 **External Interrupt Raw Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_RAW_PEND3	**Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it is mask or not).** 1: Compare AXI ID[9:0] (include gid[1:0])

1000BA10 EINT_RAW_STA4 **External Interrupt Raw Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_RAW_PEND4	**Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it is mask or not).** 1: Compare AXI ID[9:0] (include gid[1:0])

1000BA14 EINT_RAW_STA5 **External Interrupt Raw Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_RAW_PEND5	**Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it is mask or not).** 1: Compare AXI ID[9:0] (include gid[1:0])

1000B504 EINT_DBNC_7_4 **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING7						DBNC_RST7	EN7	DBNC_SETTING6						DBNC_RST6	EN6
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING5						DBNC_RST5	EN5	DBNC_SETTING4						DBNC_RST4	EN4
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING7	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms

Bit(s)	Mnemonic	Name	Description
			0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST7	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN7	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING6	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST6	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN6	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING5	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST5	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN5	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING4	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms

Bit(s)	Mnemonic	Name	Description
			0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST4	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN4	**Enables de-bounce function** 0: Disable 1: Enable

1000B604 EINT_DBNC_SET_7_4 **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET7						DBNC_RST_SET7	EN_SET7	DBNC_SETTING_SET6						DBNC_RST_SET6	EN_SET6
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_SET5						DBNC_RST_SET5	EN_SET5	DBNC_SETTING_SET4						DBNC_RST_SET4	EN_SET4
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_SET7	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST_SET7	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_SET7	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING_SET6	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms

Bit(s)	Mnemonic	Name	Description
			0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST_SET6	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_SET6	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_SET5	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST_SET5	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_SET5	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_SET4	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST_SET4	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_SET4	**Enables de-bounce function** 0: Disable 1: Enable

1000B704 EINT_DBNC External Interrupt Debounce 00000000

CLR_7_4 **Control Register**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC _SET TING _CLR _CLR 7						DBNC _RST 7	EN_C LR7		DBNC_SETTING_ CLR_CLR6					DBNC _RST 6	EN_C LR6
Type	WO						WO	WO		WO					WO	WO
Reset	0	0	0	0			0	0		0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_ CLR5						DBNC _RST 5	EN_C LR5	DBNC_SETTING_CLR_ CLR4						DBNC _RST 4	EN_C LR4
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_CLR_CLR7	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST7	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_CLR7	**Enables de-bounce function** 0: Disable 1: Enable
22:20		DBNC_SETTING_CLR_CLR6	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST6	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_CLR6	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_CLR_CLR5	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms

Bit(s)	Mnemonic	Name	Description
			0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST5	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_CLR5	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_CLR_CLR4	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST4	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_CLR4	**Enables de-bounce function** 0: Disable 1: Enable

1000B508 EINT_DBNC_B_8 **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING11						DBNC_RST11	EN11	DBNC_SETTING10						DBNC_RST10	EN10
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING9						DBNC_RST9	EN9	DBNC_SETTING8						DBNC_RST8	EN8
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING11	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms

Bit(s)	Mnemonic	Name	Description
			0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST11	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN11	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING10	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST10	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN10	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING9	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST9	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN9	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING8	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms

Bit(s)	Mnemonic	Name	Description
			0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST8	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN8	**Enables de-bounce function** 0: Disable 1: Enable

1000B608 EINT_DBNC_SET_B_8 **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET11						DBNC_RST_SET11	EN_SET11	DBNC_SETTING_SET10						DBNC_RST_SET10	EN_SET10
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_SET9						DBNC_RST_SET9	EN_SET9	DBNC_SETTING_SET8						DBNC_RST_SET8	EN_SET8
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_SET11	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST_SET11	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_SET11	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING_SET10	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms

Bit(s)	Mnemonic	Name	Description
			0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST_SET10	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_SET10	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_SET9	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST_SET9	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_SET9	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_SET8	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST_SET8	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_SET8	**Enables de-bounce function** 0: Disable 1: Enable

1000B708 EINT_DBNC_CLR_B_8 **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	DBNC _SET TING _CLR _CLR 11						DBNC _RST 11	EN_C LR11		DBNC_SETTING_ CLR_CLR10					DBNC _RST 10	EN_C LR10
Type	WO						WO	WO		WO					WO	WO
Reset	0	0	0	0			0	0		0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_ CLR9						DBNC _RST 9	EN_C LR9	DBNC_SETTING_CLR_ CLR8						DBNC _RST 8	EN_C LR8
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_C LR_CLR11	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST11	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_CLR11	**Enables de-bounce function** 0: Disable 1: Enable
22:20		DBNC_SETTING_C LR_CLR10	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST10	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_CLR10	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_C LR_CLR9	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms

Bit(s)	Mnemonic	Name	Description
			0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST9	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_CLR9	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_CLR_CLR8	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST8	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_CLR8	**Enables de-bounce function** 0: Disable 1: Enable

1000B50C EINT_DBNC_F_C **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING15						DBNC_RST15	EN15	DBNC_SETTING14						DBNC_RST14	EN14
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING13						DBNC_RST13	EN13	DBNC_SETTING12						DBNC_RST12	EN12
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING15	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms

Bit(s)	Mnemonic	Name	Description
			0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST15	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN15	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING14	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST14	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN14	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING13	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST13	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN13	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING12	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms

Bit(s)	Mnemonic	Name	Description
			0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST12	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN12	**Enables de-bounce function** 0: Disable 1: Enable

1000B60C EINT_DBNC_SET_F_C **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET15						DBNC_RST_SET15	EN_SET15	DBNC_SETTING_SET14						DBNC_RST_SET14	EN_SET14
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_SET13						DBNC_RST_SET13	EN_SET13	DBNC_SETTING_SET12						DBNC_RST_SET12	EN_SET12
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_SET15	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST_SET15	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_SET15	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING_SET14	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms

Bit(s)	Mnemonic	Name	Description
			0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST_SET14	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_SET14	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_SET13	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST_SET13	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_SET13	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_SET12	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST_SET12	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_SET12	**Enables de-bounce function** 0: Disable 1: Enable

1000B70C EINT_DBNC_CLR_F_C — **External Interrupt Debounce Control Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR15						DBNC_RST	EN_CLR15		DBNC_SETTING_CLR_CLR14					DBNC_RST	EN_CLR14

							15								14	
Type	WO						WO	WO		WO					WO	WO
Reset	0	0	0	0			0	0		0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_CLR13						DBNC_RST13	EN_CLR13	DBNC_SETTING_CLR_CLR12						DBNC_RST12	EN_CLR12
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_CLR_CLR15	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST15	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_CLR15	**Enables de-bounce function** 0: Disable 1: Enable
22:20		DBNC_SETTING_CLR_CLR14	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST14	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_CLR14	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_CLR_CLR13	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms

Bit(s)	Mnemonic	Name	Description
			1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST13	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_CLR13	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_CLR_CLR12	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST12	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_CLR12	**Enables de-bounce function** 0: Disable 1: Enable

1000B5B0 EINT_DBNC_B_3_0 **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC _SET TING 148						DBNC_RST148	EN148	DBNC_SETTING147						DBNC_RST147	EN147
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING146						DBNC_RST146	EN146	DBNC_SETTING145						DBNC_RST145	EN145
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING14 8	
25		DBNC_RST148	
24		EN148	
23:20		DBNC_SETTING14 7	
17		DBNC_RST147	
16		EN147	
15:12		DBNC_SETTING14 6	
9		DBNC_RST146	
8		EN146	

Bit(s)	Mnemonic	Name	Description
7:4		DBNC_SETTING14 5	
1		DBNC_RST145	
0		EN145	

1000B6B0 EINT_DBNC_SET_B_3_0 **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET148						DBNC_RST_SET148	EN_SET148	DBNC_SETTING_SET147						DBNC_RST_SET147	EN_SET147
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_SET146						DBNC_RST_SET146	EN_SET146	DBNC_SETTING_SET145						DBNC_RST_SET145	EN_SET145
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_SET148	
25		DBNC_RST_SET14 8	
24		EN_SET148	
23:20		DBNC_SETTING_SET147	
17		DBNC_RST_SET14 7	
16		EN_SET147	
15:12		DBNC_SETTING_SET146	
9		DBNC_RST_SET14 6	
8		EN_SET146	
7:4		DBNC_SETTING_SET145	
1		DBNC_RST_SET14 5	
0		EN_SET145	

1000B7B0 EINT_DBNC_CLR_B_3_0 **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR148						DBNC_RST148	EN_CLR148		DBNC_SETTING_CLR_CLR147					DBNC_RST147	EN_CLR147
Type	WO						WO	WO		WO					WO	WO
Reset	0	0	0	0			0	0		0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_CLR146						DBNC_RST146	EN_CLR146	DBNC_SETTING_CLR_CLR145						DBNC_RST145	EN_CLR145
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_CLR_CLR148	
25		DBNC_RST148	
24		EN_CLR148	
22:20		DBNC_SETTING_CLR_CLR147	
17		DBNC_RST147	
16		EN_CLR147	
15:12		DBNC_SETTING_CLR_CLR146	
9		DBNC_RST146	
8		EN_CLR146	
7:4		DBNC_SETTING_CLR_CLR145	
1		DBNC_RST145	
0		EN_CLR145	

1000B5B4 EINT_DBNC_B_7_4 **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING152						DBNC_RST152	EN152	DBNC_SETTING151						DBNC_RST151	EN151
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING150						DBNC_RST150	EN150	DBNC_SETTING149						DBNC_RST149	EN149
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING152	
25		DBNC_RST152	
24		EN152	
23:20		DBNC_SETTING151	
17		DBNC_RST151	
16		EN151	
15:12		DBNC_SETTING150	
9		DBNC_RST150	
8		EN150	
7:4		DBNC_SETTING149	
1		DBNC_RST149	
0		EN149	

1000B6B4 EINT_DBNC_SET_B_7_4 **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET152						DBNC_RST	EN_SET15	DBNC_SETTING_SET151						DBNC_RST	EN_SET15

							_SET 152	2							_SET 151	1
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_SET150						DBNC_RST_SET150	EN_SET150	DBNC_SETTING_SET149						DBNC_RST_SET149	EN_SET149
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_SET152	
25		DBNC_RST_SET152	
24		EN_SET152	
23:20		DBNC_SETTING_SET151	
17		DBNC_RST_SET151	
16		EN_SET151	
15:12		DBNC_SETTING_SET150	
9		DBNC_RST_SET150	
8		EN_SET150	
7:4		DBNC_SETTING_SET149	
1		DBNC_RST_SET149	
0		EN_SET149	

1000B7B4 EINT_DBNC_CLR_B_7_4 **External Interrupt Debounce Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR152						DBNC_RST152	EN_CLR152		DBNC_SETTING_CLR_CLR151					DBNC_RST151	EN_CLR151
Type	WO						WO	WO		WO					WO	WO
Reset	0	0	0	0			0	0		0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_CLR150						DBNC_RST150	EN_CLR150	DBNC_SETTING_CLR_CLR149						DBNC_RST149	EN_CLR149
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_CLR_CLR152	
25		DBNC_RST152	
24		EN_CLR152	
22:20		DBNC_SETTING_CLR_CLR151	
17		DBNC_RST151	
16		EN_CLR151	
15:12		DBNC_SETTING_C	

Bit(s)	Mnemonic	Name	Description
		LR_CLR150	
9		DBNC_RST150	
8		EN_CLR150	
7:4		DBNC_SETTING_C	
		LR_CLR149	
1		DBNC_RST149	
0		EN_CLR149	

1000BC00 EINT_SYNC_EN0 **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYNC_EN0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYNC_EN0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		SYNC_EN0	**If the register is 0, it means the interrupt cannot be received.** Bit Y, control y*4+3: y*4 eint 0: Disable sync 1: Enable sync

1000BC04 EINT_SYNC_EN1 **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYNC_EN1															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
15:0		SYNC_EN1	**If the register is 0, it means the interrupt cannot be received.** Bit Y, control 128+y*4+3: 128+ y*4 eint 0: Disable sync 1: Enable sync

1000BD00 EINT_SYNC_EN_SET_0 **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYNC_EN_SET_0															

Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYNC_EN_SET_0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		SYNC_EN_SET_0	**Set EN0 to 1.** 0: Disable 1: Enable

1000BD04 EINT_SYNC_EN_SET_1 **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYNC_EN_SET_1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		SYNC_EN_SET_1	**Set EN1 to 1.** 0: Disable 1: Enable

1000BE00 EINT_SYNC_EN_CLR_0 **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYNC_EN_CLR_0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYNC_EN_CLR_0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		SYNC_EN_CLR_0	**Set EN0 to 1.** 0: Disable 1: Enable

1000BE04 EINT_SYNC_EN_CLR_1 **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYNC_EN_CLR_1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		SYNC_EN_CLR_1	**Set EN1 to 1.** 0: Disable 1: Enable

1000BF00 FPGA_EMUL_0 FPGA EMUL Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FPGA_EMUL_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FPGA_EMUL_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		FPGA_EMUL_0	Pretends IOPAD

1000BF04 FPGA_EMUL_1 FPGA EMUL Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FPGA_EMUL_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FPGA_EMUL_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		FPGA_EMUL_1	Pretends IOPAD

1000BF08 FPGA_EMUL_2 FPGA EMUL Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FPGA_EMUL_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	FPGA_EMUL_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		FPGA_EMUL_2	Pretends IOPAD

1000BF0C FPGA_EMUL_3 **FPGA EMUL Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FPGA_EMUL_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FPGA_EMUL_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		FPGA_EMUL_3	Pretends IOPAD

1000BF10 FPGA_EMUL_4 **FPGA EMUL Register 4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FPGA_EMUL_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FPGA_EMUL_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		FPGA_EMUL_4	Pretends IOPAD

1000BB00 SECURE_EINT_EN **SECURE_EINT_EN** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	secure_en															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		secure_en	Controls EINT15-0 is secure path or not

1000BB10 SECURE_DIR_EINT_EN **SECURE_DIR_EINT_EN** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													direct_secure_en			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0		direct_secure_ en	Controls direct IRQ 3~0 is secure path or not

1000BB20 DCM_ON **DCM_ON** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																dcm_on
Type																RW
Reset																1

Bit(s)	Mnemonic	Name	Description
0		dcm_on	Controls DCM enable

1000BB30 SECURE_STATUS **SECURE_STATUS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	secure_status															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		secure_status	**Same meaning as status** Will be 1 only when secure enable and interrupt occurs.

1.3 System Interrupt Controller

Module name: sys_cirq Base address: (+10204000h)

Address	Name	Width	Register Function
10204000	CIRQ_STA0	32	System CIRQ Status Register
10204004	CIRQ_STA1	32	System CIRQ Status Register
10204008	CIRQ_STA2	32	System CIRQ Status Register
1020400C	CIRQ_STA3	32	System CIRQ Status Register
10204010	CIRQ_STA4	32	System CIRQ Status Register
10204014	CIRQ_STA5	32	System CIRQ Status Register
10204018	CIRQ_STA6	32	System CIRQ Status Register
10204040	CIRQ_ACK0	32	System CIRQ Acknowledge Register
10204044	CIRQ_ACK1	32	System CIRQ Acknowledge Register
10204048	CIRQ_ACK2	32	System CIRQ Acknowledge Register
1020404C	CIRQ_ACK3	32	System CIRQ Acknowledge Register
10204050	CIRQ_ACK4	32	System CIRQ Acknowledge Register
10204054	CIRQ_ACK5	32	System CIRQ Acknowledge Register
10204058	CIRQ_ACK6	32	System CIRQ Acknowledge Register
10204080	CIRQ_MASK0	32	System CIRQ Mask Register
10204084	CIRQ_MASK1	32	System CIRQ Mask Register
10204088	CIRQ_MASK2	32	System CIRQ Mask Register
1020408C	CIRQ_MASK3	32	System CIRQ Mask Register
10204090	CIRQ_MASK4	32	System CIRQ Mask Register
10204094	CIRQ_MASK5	32	System CIRQ Mask Register
10204098	CIRQ_MASK6	32	System CIRQ Mask Register
102040C0	CIRQ_MASK_SET0	32	System CIRQ Mask Set Register
102040C4	CIRQ_MASK_SET1	32	System CIRQ Mask Set Register
102040C8	CIRQ_MASK_SET2	32	System CIRQ Mask Set Register
102040CC	CIRQ_MASK_SET3	32	System CIRQ Mask Set Register
102040D0	CIRQ_MASK_SET4	32	System CIRQ Mask Set Register
102040D4	CIRQ_MASK_SET5	32	System CIRQ Mask Set Register
102040D8	CIRQ_MASK_SET6	32	System CIRQ Mask Set Register
10204100	CIRQ_MASK_CLR0	32	System CIRQ Mask Set Register
10204104	CIRQ_MASK_CLR1	32	System CIRQ Mask Set Register
10204108	CIRQ_MASK_CLR2	32	System CIRQ Mask Set Register
1020410C	CIRQ_MASK_CLR3	32	System CIRQ Mask Set Register
10204110	CIRQ_MASK_CLR4	32	System CIRQ Mask Set Register
10204114	CIRQ_MASK_CLR5	32	System CIRQ Mask Set Register
10204118	CIRQ_MASK_CLR6	32	System CIRQ Mask Set Register
10204140	CIRQ_SENS0	32	System CIRQ Sensitivity Register
10204144	CIRQ_SENS1	32	System CIRQ Sensitivity Register
10204148	CIRQ_SENS2	32	System CIRQ Sensitivity Register
1020414C	CIRQ_SENS3	32	System CIRQ Sensitivity Register
10204150	CIRQ_SENS4	32	System CIRQ Sensitivity Register
10204154	CIRQ_SENS5	32	System CIRQ Sensitivity Register
10204158	CIRQ_SENS6	32	System CIRQ Sensitivity Register
10204180	CIRQ_SENS_SET0	32	System CIRQ Sensitivity Set Register

Address	Name	Width	Register Function
10204184	CIRQ_SENS_SET1	32	System CIRQ Sensitivity Set Register
10204188	CIRQ_SENS_SET2	32	System CIRQ Sensitivity Set Register
1020418C	CIRQ_SENS_SET3	32	System CIRQ Sensitivity Set Register
10204190	CIRQ_SENS_SET4	32	System CIRQ Sensitivity Set Register
10204194	CIRQ_SENS_SET5	32	System CIRQ Sensitivity Set Register
10204198	CIRQ_SENS_SET6	32	System CIRQ Sensitivity Set Register
102041C0	CIRQ_SENS_CLR0	32	System CIRQ Sensitivity Clear Register
102041C4	CIRQ_SENS_CLR1	32	System CIRQ Sensitivity Clear Register
102041C8	CIRQ_SENS_CLR2	32	System CIRQ Sensitivity Clear Register
102041CC	CIRQ_SENS_CLR3	32	System CIRQ Sensitivity Clear Register
102041D0	CIRQ_SENS_CLR4	32	System CIRQ Sensitivity Clear Register
102041D4	CIRQ_SENS_CLR5	32	System CIRQ Sensitivity Clear Register
102041D8	CIRQ_SENS_CLR6	32	System CIRQ Sensitivity Clear Register
10204200	CIRQ_POL0	32	External Interrupt Polarity Register
10204204	CIRQ_POL1	32	External Interrupt Polarity Register
10204208	CIRQ_POL2	32	External Interrupt Polarity Register
1020420C	CIRQ_POL3	32	External Interrupt Polarity Register
10204210	CIRQ_POL4	32	External Interrupt Polarity Register
10204214	CIRQ_POL5	32	External Interrupt Polarity Register
10204218	CIRQ_POL6	32	External Interrupt Polarity Register
10204240	CIRQ_POL_SET0	32	External Interrupt Polarity Set Register
10204244	CIRQ_POL_SET1	32	External Interrupt Polarity Set Register
10204248	CIRQ_POL_SET2	32	External Interrupt Polarity Set Register
1020424C	CIRQ_POL_SET3	32	External Interrupt Polarity Set Register
10204250	CIRQ_POL_SET4	32	External Interrupt Polarity Set Register
10204254	CIRQ_POL_SET5	32	External Interrupt Polarity Set Register
10204258	CIRQ_POL_SET6	32	External Interrupt Polarity Set Register
10204280	CIRQ_POL_CLR0	32	External Interrupt Polarity Clear Register
10204284	CIRQ_POL_CLR1	32	External Interrupt Polarity Clear Register
10204288	CIRQ_POL_CLR2	32	External Interrupt Polarity Clear Register
1020428C	CIRQ_POL_CLR3	32	External Interrupt Polarity Clear Register
10204290	CIRQ_POL_CLR4	32	External Interrupt Polarity Clear Register
10204294	CIRQ_POL_CLR5	32	External Interrupt Polarity Clear Register
10204298	CIRQ_POL_CLR6	32	External Interrupt Polarity Clear Register
10204300	CIRQ_CON	32	Sytem CIRQ Control Register

10204000 CIRQ_STA0 System CIRQ Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_PEND0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_PEND0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_PEND0	Each bit read as 1 indicates the corresponding system CIRQ is pending.

10204004 CIRQ_STA1 System CIRQ Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_PEND1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_PEND1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_PEND1	Each bit read as 1 indicates the corresponding system CIRQ is pending.

10204008 CIRQ_STA2 System CIRQ Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_PEND2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_PEND2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_PEND2	Each bit read as 1 indicates the corresponding system CIRQ is pending.

1020400C CIRQ_STA3 System CIRQ Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_PEND3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_PEND3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_PEND3	Each bit read as 1 indicates the corresponding system CIRQ is pending.

10204010 CIRQ_STA4 System CIRQ Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_PEND4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_PEND4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_PEND4	Each bit read as 1 indicates the corresponding system CIRQ is pending.

10204014 CIRQ_STA5 System CIRQ Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_PEND5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_PEND5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_PEND5	Each bit read as 1 indicates the corresponding system CIRQ is pending.

10204018 CIRQ_STA6 System CIRQ Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CIRQ_PEND5										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_PEND5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26:0		CIRQ_PEND5	Each bit read as 1 indicates the corresponding system CIRQ is pending.

10204040 CIRQ_ACK0 System CIRQ Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK0															
Type	WO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_ACK0	Write 1 to specific bit to acknowledge the corresponding system CIRQ.

10204044 CIRQ_ACK1 System CIRQ Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_ACK1	Write 1 to specific bit to acknowledge the corresponding system CIRQ.

10204048 CIRQ_ACK2 System CIRQ Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_ACK2	Write 1 to specific bit to acknowledge the corresponding system CIRQ.

1020404C CIRQ_ACK3 System CIRQ Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK3															

Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_ACK3	Write 1 to specific bit to acknowledge the corresponding system CIRQ.

10204050 CIRQ_ACK4 System CIRQ Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_ACK4	Write 1 to specific bit to acknowledge the corresponding system CIRQ.

10204054 CIRQ_ACK5 System CIRQ Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_ACK5	Write 1 to specific bit to acknowledge the corresponding system CIRQ.

10204058 CIRQ_ACK6 System CIRQ Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CIRQ_ACK6										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26:0		CIRQ_ACK6	Write 1 to specific bit to acknowledge the corresponding system CIRQ.

10204080 CIRQ_MASK0 System CIRQ Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK0	System CIRQ mask value

10204084 CIRQ_MASK1 System CIRQ Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK1															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK1															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK1	System CIRQ mask value

10204088 CIRQ_MASK2 System CIRQ Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK2															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK2															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK2	System CIRQ mask value

1020408C CIRQ_MASK3 System CIRQ Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK3															

Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK3															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK3	System CIRQ mask value

10204090 CIRQ_MASK4 System CIRQ Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK4															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK4															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK4	System CIRQ mask value

10204094 CIRQ_MASK5 System CIRQ Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK5															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK5															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK5	System CIRQ mask value

10204098 CIRQ_MASK6 System CIRQ Mask Register 07FFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CIRQ_MASK6										
Type						RO										
Reset						1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK6															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
26:0		CIRQ_MASK6	System CIRQ mask value

102040C0 CIRQ_MASK_SET0 System CIRQ Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_SET0	Write 1 to specific bit to set up the mask of the corresponding system CIRQ.

102040C4 CIRQ_MASK_SET1 System CIRQ Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_SET1	Write 1 to specific bit to set up the mask of the corresponding system CIRQ.

102040C8 CIRQ_MASK_SET2 System CIRQ Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_SET2	Write 1 to specific bit to set up the mask of the corresponding system CIRQ.

102040CC CIRQ_MASK_SET3 **System CIRQ Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_SET3	Write 1 to specific bit to set up the mask of the corresponding system CIRQ.

102040D0 CIRQ_MASK_SET4 **System CIRQ Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_SET4	Write 1 to specific bit to set up the mask of the corresponding system CIRQ.

102040D4 CIRQ_MASK_SET5 **System CIRQ Mask Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_SET5	Write 1 to specific bit to set up the mask of the corresponding system CIRQ.

102040D8 CIRQ_MASK **System CIRQ Mask Set Register** **00000000**

SET6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CIRQ_MASK_SET5										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26:0		CIRQ_MASK_SET5	Write 1 to specific bit to set up the mask of the corresponding system CIRQ.

10204100 CIRQ_MASK_CLR0 System CIRQ Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_CLR0	Write 1 to specific bit to clear the mask of the corresponding system CIRQ.

10204104 CIRQ_MASK_CLR1 System CIRQ Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_CLR1	Write 1 to specific bit to clear the mask of the corresponding system CIRQ.

10204108 CIRQ_MASK_CLR2 System CIRQ Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	CIRQ_MASK_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_CLR2	Write 1 to specific bit to clear the mask of the corresponding system CIRQ.

1020410C CIRQ_MASK_CLR3 System CIRQ Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_CLR3	Write 1 to specific bit to clear the mask of the corresponding system CIRQ.

10204110 CIRQ_MASK_CLR4 System CIRQ Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_CLR4	Write 1 to specific bit to clear the mask of the corresponding system CIRQ.

10204114 CIRQ_MASK_CLR5 System CIRQ Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_CLR5	Write 1 to specific bit to clear the mask of the corresponding system CIRQ.

10204118 CIRQ_MASK_CLR6 System CIRQ Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CIRQ_MASK_CLR6										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26:0		CIRQ_MASK_CLR6	Write 1 to specific bit to clear the mask of the corresponding system CIRQ.

10204140 CIRQ_SENS0 System CIRQ Sensitivity Register FFFFFFE3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS0	System CIRQ sensitivity value

10204144 CIRQ_SENS1 System CIRQ Sensitivity Register FEEC7FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS1															
Type	RO															
Reset	1	1	1	1	1	1	1	0	1	1	1	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS1															
Type	RO															

Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS1	System CIRQ sensitivity value

10204148 CIRQ_SENS2 System CIRQ Sensitivity Register FBFFDFF8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS2															
Type	RO															
Reset	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS2															
Type	RO															
Reset	1	1	0	1	1	1	1	1	1	1	1	1	1	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS2	System CIRQ sensitivity value

1020414C CIRQ_SENS3 System CIRQ Sensitivity Register FFFFFF5F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS3															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS3															
Type	RO															
Reset	1	1	1	1	1	1	1	1	0	1	0	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS3	System CIRQ sensitivity value

10204150 CIRQ_SENS4 System CIRQ Sensitivity Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS4															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS4															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS4	System CIRQ sensitivity value

10204154 CIRQ_SENS5 System CIRQ Sensitivity Register 000000EA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS5	System CIRQ sensitivity value

10204158 CIRQ_SENS6 System CIRQ Sensitivity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CIRQ_SENS6										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26:0		CIRQ_SENS6	System CIRQ sensitivity value

10204180 CIRQ_SENS_SET0 System CIRQ Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_SET0	Write 1 to specific bit to set up the sensitivity of the corresponding system CIRQ.

10204184 CIRQ_SENS_SET1 System CIRQ Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	CIRQ_SENS_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_SET1	Write 1 to specific bit to set up the sensitivity of the corresponding system CIRQ.

10204188 CIRQ_SENS_SET2 System CIRQ Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_SET2	Write 1 to specific bit to set up the sensitivity of the corresponding system CIRQ.

1020418C CIRQ_SENS_SET3 System CIRQ Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_SET3	Write 1 to specific bit to set up the sensitivity of the corresponding system CIRQ.

10204190 CIRQ_SENS_SET4 System CIRQ Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_SET4	Write 1 to specific bit to set up the sensitivity of the corresponding system CIRQ.

10204194 CIRQ_SENS_SET5 **System CIRQ Sensitivity Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_SET5	Write 1 to specific bit to set up the sensitivity of the corresponding system CIRQ.

10204198 CIRQ_SENS_SET6 **System CIRQ Sensitivity Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CIRQ_SENS_SET6										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26:0		CIRQ_SENS_SET6	Write 1 to specific bit to set up the sensitivity of the corresponding system CIRQ.

102041C0 CIRQ_SENS_CLR0 **System CIRQ Sensitivity Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR0															
Type	WO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_CLR0	Write 1 to specific bit to clear the sensitivity of the corresponding system CIRQ.

102041C4 CIRQ_SENS_CLR1 **System CIRQ Sensitivity Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_CLR1	Write 1 to specific bit to clear the sensitivity of the corresponding system CIRQ.

102041C8 CIRQ_SENS_CLR2 **System CIRQ Sensitivity Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_CLR2	Write 1 to specific bit to clear the sensitivity of the corresponding system CIRQ.

102041CC CIRQ_SENS_CLR3 **System CIRQ Sensitivity Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_CLR3	Write 1 to specific bit to clear the sensitivity of the corresponding system CIRQ.

102041D0 CIRQ_SENS_CLR4 System CIRQ Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_CLR4	Write 1 to specific bit to clear the sensitivity of the corresponding system CIRQ.

102041D4 CIRQ_SENS_CLR5 System CIRQ Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_CLR5	Write 1 to specific bit to clear the sensitivity of the corresponding system CIRQ.

102041D8 CIRQ_SENS_CLR6 System CIRQ Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CIRQ_SENS_CLR6										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26:0		CIRQ_SENS_CLR6	Write 1 to specific bit to clear the sensitivity of the corresponding system CIRQ.

Bit(s)	Mnemonic	Name	Description

10204200 CIRQ_POL0 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL0	System CIRQ polarity value

10204204 CIRQ_POL1 External Interrupt Polarity Register 00138000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL1															
Type	RO															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL1	System CIRQ polarity value

10204208 CIRQ_POL2 External Interrupt Polarity Register 03E60007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL2															
Type	RO															
Reset	0	0	0	0	0	0	1	1	1	1	1	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL2	System CIRQ polarity value

1020420C CIRQ_POL3 External Interrupt Polarity Register 00000060

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL3	System CIRQ polarity value

10204210 CIRQ_POL4 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL4	System CIRQ polarity value

10204214 CIRQ_POL5 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL5	System CIRQ polarity value

10204218 CIRQ_POL6 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CIRQ_POL6										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	CIRQ_POL6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26:0		CIRQ_POL6	System CIRQ polarity value

10204240 CIRQ_POL_SET0 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_SET0	Write 1 to specific bit to set up the polarity of the corresponding system CIRQ.

10204244 CIRQ_POL_SET1 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_SET1	Write 1 to specific bit to set up the polarity of the corresponding system CIRQ.

10204248 CIRQ_POL_SET2 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_SET2	Write 1 to specific bit to set up the polarity of the corresponding system CIRQ.

1020424C CIRQ_POL_SET3 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_SET3	Write 1 to specific bit to set up the polarity of the corresponding system CIRQ.

10204250 CIRQ_POL_SET4 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_SET4	Write 1 to specific bit to set up the polarity of the corresponding system CIRQ.

10204254 CIRQ_POL_SET5 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_SET5	Write 1 to specific bit to set up the polarity of the corresponding system CIRQ.

Bit(s)	Mnemonic	Name	Description

10204258 CIRQ_POL_SET6 — **External Interrupt Polarity Set Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CIRQ_POL_SET6										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26:0		CIRQ_POL_SET6	Write 1 to specific bit to set up the polarity of the corresponding system CIRQ.

10204280 CIRQ_POL_CLR0 — **External Interrupt Polarity Clear Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_CLR0	Write 1 to specific bit to clear the polarity of the corresponding system CIRQ.

10204284 CIRQ_POL_CLR1 — **External Interrupt Polarity Clear Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_CLR1	Write 1 to specific bit to clear the polarity of the corresponding system CIRQ.

10204288 CIRQ_POL_CLR2 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_CLR2	Write 1 to specific bit to clear the polarity of the corresponding system CIRQ.

1020428C CIRQ_POL_CLR3 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_CLR3	Write 1 to specific bit to clear the polarity of the corresponding system CIRQ.

10204290 CIRQ_POL_CLR4 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_CLR4	Write 1 to specific bit to clear the polarity of the corresponding system CIRQ.

10204294 CIRQ_POL_CLR5 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	CIRQ_POL_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_CLR5	Write 1 to specific bit to clear the polarity of the corresponding system CIRQ.

10204298 CIRQ_POL_CLR6 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CIRQ_POL_CLR6										
Type						WO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26:0		CIRQ_POL_CLR6	Write 1 to specific bit to clear the polarity of the corresponding system CIRQ.

10204300 CIRQ_CON Sytem CIRQ Control Register 80000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_EVENT_B															
Type	RO															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CIRQ_FLUSH	CIRQ_EDGE_ONLY	CIRQ_EN
Type														WO	RW	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
31		CIRQ_EVENT_B	**Indicates sys_cirq_irq_b is triggered**
2		CIRQ_FLUSH	**Flushes pending interrupts**
1		CIRQ_EDGE_ONLY	**Sets up edge-only mode** Only edge-triggered interrupt will be recorded.
0		CIRQ_EN	**Enable bit of system CIRQ controller**

1.4 Infrastructure System Configuration Module

Module name: infracfg_ao_reg Base address: (+10001000h)

Address	Name	Width	Register Function
10001000	MCU_MEMEQ	32	TOPCKGEN Clock Mux Control Register
10001008	TOP_CKDIV1	32	TOPCKGEN Clock Divider 1 Control Register
10001010	TOP_DCMCTL	32	TOPCKGEN Cortex-A7 DCM Control Register
10001014	TOP_DCMDBC	32	TOPCKGEN DCM Debounce Control Register
10001050	INFRA_GLOBALCON_DCMCTL	32	Infrasys DCM Control Register
10001070	INFRA_BUS_DCM_CTRL	32	Infrasys DCM Control Register
10001074	PERI_BUS_DCM_CTRL	32	Infrasys DCM Control Register
10001078	MEM_DCM_CTRL	32	Infrasys DCM Control Register
1000107C	DFS_MEM_DCM_CTRL	32	Infrasys DCM Control Register
10001080	MODULE_SW_CG_0_SET	32	Infrasys DCM Control Register
10001084	MODULE_SW_CG_0_CLR	32	Infrasys DCM Control Register
10001088	MODULE_SW_CG_1_SET	32	Infrasys DCM Control Register
1000108C	MODULE_SW_CG_1_CLR	32	Infrasys DCM Control Register
10001090	MODULE_SW_CG_0_STA	32	Infrasys DCM Control Register
10001094	MODULE_SW_CG_1_STA	32	Infrasys DCM Control Register
10001098	MODULE_CLK_SEL	32	Infrasys DCM Control Register
1000109C	MEM_CG_CTRL	32	Infrasys DCM Control Register
100010A0	PTP_RX_CLK_ON	32	rg_p2p_rx_clk_force_on
100010A4	DRAMC_WBR	32	rg_dramc_wbr
100010A8	MODULE_SW_CG_2_SET	32	Infrasys DCM Control Register
100010AC	MODULE_SW_CG_2_CLR	32	Infrasys DCM Control Register
100010B0	MODULE_SW_CG_2_STA	32	Infrasys DCM Control Register
10001100	I2C_DBTOOL_MISC	32	reg_dbg_i2c_rising_mode
10001104	MD_SLEEP_CTRL_MASK	32	md_sleep_ctrl_mask
10001108	PMICW_CLOCK_CTRL	32	
1000110C	SSUSB_INT_SEL	32	ssusb int sel
10001120	INFRA_GLOBALCON_RSTo_SET	32	Infrasys Always-on Reset Control Register
10001124	INFRA_GLOBALCON_RSTo_CLR	32	Infrasys Always-on Reset Control Register
10001128	INFRA_GLOBALCON_RSTo_STA	32	Infrasys Always-on Reset Control Register
10001130	INFRA_GLOBALCON_RST1_SET	32	Infrasys Always-on Reset Control Register

Address	Name	Width	Register Function
10001134	INFRA_GLOBALCON_RST1_CLR	32	Infrasys Always-on Reset Control Register
10001138	INFRA_GLOBALCON_RST1_STA	32	Infrasys Always-on Reset Control Register
10001140	INFRA_GLOBALCON_RST2_SET	32	Infrasys Always-on Reset Control Register
10001144	INFRA_GLOBALCON_RST2_CLR	32	Infrasys Always-on Reset Control Register
10001148	INFRA_GLOBALCON_RST2_STA	32	Infrasys Always-on Reset Control Register
10001160	LTE_OCCUPY_ANT	32	Set BPI 5~20 Controlled by LTE MODEM
10001164	C2K_OCCUPY_ANT	32	Set BPI 5~20 Controlled by C2K MODEM
10001168	LTE_C2K_BPI_CONFLICT	32	Record LTE C2K BPI Conflict Status
10001200	INFRA_TOPAXI_SI0_CTL	32	Top AXI Fabric SI0 Control Register
10001204	INFRA_TOPAXI_SI1_CTL	32	Top AXI Fabric SI1 Control Register
10001208	INFRA_TOPAXI_MDBUS_CTL	32	MDSYS AXI Fabric Control Register
1000120C	INFRA_MCI_SI0_CTL	32	MCI Infra Top Dispatcher 0 Control Register
10001210	INFRA_MCI_SI1_CTL	32	MCI Infra Top Dispatcher 1 Control Register
10001214	INFRA_MCI_SI2_CTL	32	MCI Infra Top Dispatcher 2 Control Register
10001218	INFRA_MCI_ASYNC_CTRL	32	MCI IOMMU Asynchronous Slice Configure
1000121C	INFRA_MCI_CG_MFG_SEC_STA	32	MCI CG Disable Configure and MFG Secure Control
10001220	INFRA_TOPAXI_PROTECTEN	32	Top AXI Protect Module Control Register
10001224	INFRA_TOPAXI_PROTECTSTA0	32	Top AXI Protect Module Status Register 0
10001228	INFRA_TOPAXI_PROTECTSTA1	32	Top AXI Protect Module Status Register 1
10001238	INFRA_TOPAXI_PROTECTSTA2	32	Top AXI Protect Module Status Register 2
1000123C	INFRA_TOPAXI_PROTECTSTA3	32	Top AXI Protect Module Status Register 3
1000122C	INFRA_AXI_ASLICE_CTRL	32	Top AXI Aslice Control Register
10001230	INFRA_APB_ASYNC_STA	32	INFRASYSI ASYNC APB Config Register
10001234	INFRA_TOPAXI_PROTECTEN1	32	Top AXI Protect Module Control Register 1
10001240	INFRA_MCI_TRANS_CON_READ	32	Infrasys MCI Transaction Read Configure
10001244	INFRA_MCI_TRANS_CON_WRITE	32	Infrasys MCI Transaction Write Configure
10001248	INFRA_MCI_ID_REMAP_CON	32	Infrasys MCI ID Remap Configure
1000124C	INFRA_MCI_EMI_TRANS_CON	32	Infrasys MCI EMI Threshold Sel Configure

Address	Name	Width	Register Function
10001260	MDSYS_INTF_CON0	32	MDSYS Interface Control 0
10001264	MDSYS_INTF_CON1	32	MDSYS Interface Control 1
1000126C	MDSYS_INTF_CON2	32	MDSYS Interface Control 2
10001300	MD1_BANK0_MAP0	32	MDSYS1 Bank 0 Remap Register 0
10001304	MD1_BANK0_MAP1	32	MDSYS1 Bank 0 Remap Register 1
10001308	MD1_BANK1_MAP0	32	MDSYS1 Bank 1 Remap Register 0
1000130C	MD1_BANK1_MAP1	32	MDSYS1 Bank 1 Remap Register 1
10001310	MD1_BANK4_MAP0	32	MDSYS1 Bank 4 Remap Register 0
10001314	MD1_BANK4_MAP1	32	MDSYS1 Bank 4 Remap Register 1
10001320	MD2_BANK0_MAP0	32	MDSYS2 Bank 0 Remap Register 0
10001324	MD2_BANK0_MAP1	32	MDSYS2 Bank 0 Remap Register 1
10001330	MD2_BANK4_MAP0	32	MDSYS2 Bank 4 Remap Register 0
10001334	MD2_BANK4_MAP1	32	MDSYS2 Bank 4 Remap Register 1
10001370	C2K_BANK0_MAP0	32	C2K Bank 0 Remap Register 0
10001374	C2K_BANK0_MAP1	32	C2K Bank 0 Remap Register 1
10001378	C2K_BANK1_MAP0	32	C2K Bank 1 Remap Register 0
1000137C	C2K_BANK1_MAP1	32	C2K Bank 1 Remap Register 1
10001380	C2K_BANK4_MAP0	32	C2K Bank 4 Remap Register 0
10001384	C2K_BANK4_MAP1	32	C2K Bank 4 Remap Register 1
10001340	CONN_MAP0	32	CONNSYS Bank Remap Register
10001344	CLDMA_MAP0	32	CLDMA AP Remap Register 0
10001348	MD_DUMMY	32	
10001350	CONN_BUS_CON	32	ConnSYS Interface Bus Control
10001368	C2K_HANDSHAKE	32	ap2c2k_ready
10001400	PERI_CCI_SIDEBAND_CON	32	PERISYS to CCI-400 ACE Sideband Config
10001404	MFG_CCI_SIDEBAND_CON	32	MFG to CCI-400 Sideband Configure
10001500	INFRA_AO_DBG_CON0	32	Infra_AO debug Control 0
10001504	INFRA_AO_DBG_CON1	32	Infra_AO debug Control 1
10001508	INFRA_AO_DBG_CON2	32	Infra_AO debug Control 2
1000150C	INFRA_AO_DBG_CON3	32	Infra_AO debug Control 3
10001680	BOOT_MISC0	32	Spare Register for Bootrom
10001684	BOOT_MISC1	32	Spare Register for Bootrom
10001688	BOOT_MISC2	32	Spare Register for Bootrom
1000168C	BOOT_MISC3	32	Spare Register for Bootrom
10001690	BOOT_MISC4	32	Spare Register for Bootrom
10001694	BOOT_MISC5	32	Spare Register for Bootrom
10001698	BOOT_MISC6	32	Spare Register for Bootrom
1000169C	BOOT_MISC7	32	Spare Register for Bootrom
100016A0	MISC_LOCK_KEY	32	KEY for Write Misc Control Register
100016A4	MISC_LOCK_CON	32	LOCK for Write Misc Data Register
100016A8	MISC_RST_CON	32	Reset Control for Misc Data Register
100016AC	MISC_SEC_CON	32	Security Control for Misc Data Register

Address	Name	Width	Register Function
10001700	INFRA_RSVD0	32	Infra Reserved 0
10001704	INFRA_RSVD1	32	Infra Reserved 1
10001708	INFRA_RSVD2	32	Infra Reserved 2
1000170C	INFRA_RSVD3	32	Infra Reserved 3
10001900	INFRA_BONDING	32	INFRA_BONDING
10001A00	INFRA_AO_SCPSYS_APB_ASYNC_STA	32	Infra AO SCPSYS Async APB Interface
10001A04	INFRA_AO_MD32_TX_APB_ASYNC_STA	32	Infra AO MD32 TX Async APB Interface
10001A08	INFRA_AO_MD32_RX_APB_ASYNC_STA	32	Infra AO MD32 RX Async APB Interface
10001A10	INFRA_AO_PMIC_TX_APB_ASYNC_STA	32	Infra AO PMIC TX Async APB Interface
10001A0C	INFRA_AO_CKSYS_APB_ASYNC_STA	32	Infra AO CKSYS Async APB Interface
10001600	MFG_MISC_CON	32	
10001F00	INFRA_MISC	32	Infrasys Miscellaneous Control Register
10001F04	INFRA_ACP	32	SW CCI Arcache Configure Register
10001F08	MISC_CONFIG	32	SW CCI Arcache Configure Register
10001F0C	SPM_WAKEUP_EVENT_EN	32	
10001F10	SPM_WAKEUP_EVENT_STA	32	
10001F14	GCPU_SEC_CON	32	
10001F18	INFRA_MISC2	32	
10001800	SRAMROM_BOOT_ADDR	32	SRAMROM Boot Address Register
10001804	SRAMROM_SEC_CTRL	32	SRAMROM Secure Control Register
10001808	SRAMROM_SEC_ADDR	32	SRAMROM Region Address Register
1000180C	SRAMROM_FPC_BOOT_ADDR	32	SRAMROM FPC Boot Address Register
10001810	SRAMROM_FPC_BOOT_CON	32	SRAMROM FPC Boot Control Register
10001880	MD1_SBC_KEY0	32	
10001884	MD1_SBC_KEY1	32	
10001888	MD1_SBC_KEY2	32	
1000188C	MD1_SBC_KEY3	32	
10001890	MD1_SBC_KEY4	32	
10001894	MD1_SBC_KEY5	32	
10001898	MD1_SBC_KEY6	32	
1000189C	MD1_SBC_KEY7	32	
100018A0	MD1_SBC_KEY_LOCK	32	
10001B00	PLL_ULPOSC_CON0	32	ULPOSC Register
10001B10	PLL_AUXADC_CON0	32	AUXADC Register

Address	Name	Width	Register Function
10001F80	INFRA_AO_SEC_CON	32	
10001F84	INFRA_AO_SEC_CG_CON0	32	
10001F88	INFRA_AO_SEC_CG_CON1	32	
10001FE8	INFRA_AO_SEC_CG_CON2	32	
10001F8C	INFRA_AO_SEC_RST_CON0	32	
10001F90	INFRA_AO_SEC_RST_CON1	32	
10001F94	INFRA_AO_SEC_RST_CON2	32	

10001000 MCU_MEMEQ **TOPCKGEN Clock Mux Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													mem_eq			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0		mem_eq	MEM EQ for MCU memory

10001008 TOP_CKDIV1 **TOPCKGEN Clock Divider 1 Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		clkdiv1_sel					ca15_clkdiv1_sel					ca7_clkdiv1_sel				
Type		RW					RW					RW				
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
14:10		clkdiv1_sel	
9:5		ca15_clkdiv1_s el	**CA15 ARMPLL clock divider 1 setting** 01000: 4/4 01001: 3/4 01010: 2/4 01011: 1/4 10000: 5/5

Bit(s)	Mnemonic	Name	Description
			10001: 4/5 10010: 3/5 10011: 2/5 101xx: 1/5 11000: 6/6 11001: 5/6 11010: 4/6 11011: 3/6 11100: 2/6 11101: 1/6 00xxx: 1/1
4:0		ca7_clkdiv1_se l	**CA7 ARMPLL clock divider 1 setting** 01000: 4/4 01001: 3/4 01010: 2/4 01011: 1/4 10000: 5/5 10001: 4/5 10010: 3/5 10011: 2/5 101xx: 1/5 11000: 6/6 11001: 5/6 11010: 4/6 11011: 3/6 11100: 2/6 11101: 1/6 00xxx: 1/1

10001010 TOP_DCMCTL **TOPCKGEN Cortex-A7 DCM Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						ca15_dcm_wfe_enable	ca15_dcm_wfi_enable	ca15_dcm_enable		ca7_dcm_wfe_enable	ca7_dcm_wfi_enable	ca7_dcm_enable				infra_dcm_enable
Type						RW	RW	RW		RW	RW	RW				RW
Reset						0	0	0		0	0	0				0

Bit(s)	Mnemonic	Name	Description
10		ca15_dcm_wfe_e nable	**Enables CortexA15 DCM in WFE mode** 0: Disable 1: Enable
9		ca15_dcm_wfi_e nable	**Enables CortexA15 DCM in WFI mode** 0: Disable 1: Enable
8		ca15_dcm_enabl e	**Enables CortexA15 DCM** 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable
6		ca7_dcm_wfe_en able	**Enables CortexA7 DCM in WFE mode** 0: Disable 1: Enable
5		ca7_dcm_wfi_en able	**Enables CortexA7 DCM in WFI mode** 0: Disable 1: Enable
4		ca7_dcm_enable	**Enables CortexA7 DCM** 0: Disable 1: Enable
0		infra_dcm_enab le	**Enables TOP bus DCM** 0: Disable 1: Enable

10001014 TOP_DCMDBC TOPCKGEN DCM Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										topckgen_dcm_dbc_cnt						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6:0		topckgen_dcm_d bc_cnt	DCM debouncing counter

10001050 INFRA_GLOBALCON_DCMCTL Infrasys DCM Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							l2c_sram_infra_dcm_en	axi_clock_gated_en								
Type							RW	RW								
Reset							0	0								

Bit(s)	Mnemonic	Name	Description
9		l2c_sram_infra _dcm_en	**Enables L2C SRAM DCM** 0: Disable 1: Enable

Bit(s)	Mnemonic	Name	Description
8		axi_clock_gate d_en	**Stops AXI clock in DCM mode** 0: Disable 1: Enable

10001070 INFRA_BUS_DCM_CTRL **Infrasys DCM Control Register** **00187FE0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_cbip_p2p_rxck_on_recog_dvfs_spm1	rg_modem_temp_share_dcm_en	rg_mempsrv_dis	rg_cbip_p2p_rxck_on_recog_dvfs_spm0	rg_cbip_p2p_rxck_on_recog_scp	rg_mcusys_dcm_en				rg_pllck_sel_no_spm	rg_axi_dcm_dis_en	infra_dcm_dbc_rg_dbc_en	infra_dcm_dbc_rg_dbc_num			
Type	RW	RW	RW	RW	RW	RW				RW	RW	RW	RW			
Reset	0	0	0	0	0	0				0	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	infra_dcm_dbc_rg_dbc_num	infra_dcm_rg_sfsel					infra_dcm_rg_fsel					infra_dcm_rg_force_on	infra_dcm_rg_force_clkslow	infra_dcm_rg_force_clkoff	infra_dcm_rg_clkslow_en	infra_dcm_rg_clkoff_en
Type	RW	RW					RW					RW	RW	RW	RW	RW
Reset	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		rg_cbip_p2p_rxck_on_recog_dvfs_spm1	**rx_clock of apb_async_bridge will be turned on if slave is being accessed. (DVFS_SPM1)** 0: Disable 1: Enable
30		rg_modem_temp_share_dcm_en	**Enables MODEM_TEMP_SHARE HWDCM** 0: Disable 1: Enable
29		rg_mempsrv_dis	**Disables memory preserved mode clock gating** 0: Disable 1: Enable
28		rg_cbip_p2p_rxck_on_recog_dvfs_spm0	**rx_clock of apb_async_bridge will be turned on if slave is being accessed. (DVFS_SPM0)** 0: Disable 1: Enable
27		rg_cbip_p2p_rxck_on_recog_scp	**rx_clock of apb_async_bridge will be turned on if slave is being accessed. (SCP)** 0: Disable 1: Enable
26		rg_mcusys_dcm_en	**Enables AXI bus WFI_L2 DCM** 0: Disable 1: Enable
22		rg_pllck_sel_no_spm	**Selects INFRA PLL clock** 0: Disable 1: Enable
21		rg_axi_dcm_dis_en	**Enables SPM DCM disable** 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable
20		infra_dcm_dbc_ rg_dbc_en	**Enables INFRA DCM debounce** 0: Disable 1: Enable
19:15		infra_dcm_dbc_ rg_dbc_num	**INFRA DCM debounce number**
14:10		infra_dcm_rg_s fsel	**Selects INFRA DCM idle divide** 10000: /1 01000: /2 00100: /4 00010: /8 00001: /16 00000: /32
9:5		infra_dcm_rg_f sel	**Selects INFRA DCM active divide** 10000: /1 01000: /2 00100: /4 00010: /8 00001: /16 00000: /32
4		infra_dcm_rg_f orce_on	**Forces on INFRA DCM clock** 0: Disable 1: Enable
3		infra_dcm_rg_f orce_clkslow	**INFRA DCM force clock slow** 0: Disable 1: Enable
2		infra_dcm_rg_f orce_clkoff	**INFRA DCM froce clock off** 0: Disable 1: Enable
1		infra_dcm_rg_c lkslow_en	**Enables INFRA DCM clock slow** 0: Disable 1: Enable
0		infra_dcm_rg_c lkoff_en	**Enables INFRA DCM clock off** 0: Disable 1: Enable

10001074 PERI_BUS_DCM_CTRL **Infrasys DCM Control Register** **04387FE0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_top_dcm_en	rg_ssusb_top_ref_ck_cg_sel	rg_audio_dcm_en	rg_icusb_dcm_en	pmic_cnt_mst_rg_sfsel					rg_pmic_dcm_en	rg_usb_dcm_en	peri_dcm_dbc_rg_dbc_en	peri_dcm_dbc_rg_dbc_num			
Type	RW	RW	RW	RW	RW					RW	RW	RW	RW			
Reset	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	peri_dcm_dbc_rg_dbc_num	peri_dcm_rg_sfsel					peri_dcm_rg_fsel					peri_dcm_rg_force_on	peri_dcm_rg_force_clkslow	peri_dcm_rg_force_clkoff	peri_dcm_rg_clkslow_en	peri_dcm_rg_clkoff_en
Type	RW	RW					RW					RW	RW	RW	RW	RW

Reset	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		rg_ssusb_top_d cm_en	**Enables SSUSB_TOP HWDCM** 0: Disable 1: Enable
30		rg_ssusb_top_r ef_ck_cg_sel	**Selects SSUSB_TOP CGCTRL** 0: sw_ctrl 1: hw_ctrl
29		rg_audio_dcm_e n	**Enables audio bus DCM** 0: Disable 1: Enable
28		rg_icusb_dcm_e n	**Enables ICUSB HWDCM** 0: Disable 1: Enable
27:23		pmic_cnt_mst_r g_sfsel	**Selects PMIC idle divide** 10000: /1 01000: /2 00100: /4 00010: /8 00001: /16 00000: /32
22		rg_pmic_dcm_en	**Enables PMIC HWDCM** 0: Disable 1: Enable
21		rg_usb_dcm_en	**Enables USB HWDCM** 0: Disable 1: Enable
20		peri_dcm_dbc_r g_dbc_en	**Enables PERI DCM debounce** 0: Disable 1: Enable
19:15		peri_dcm_dbc_r g_dbc_num	**PERI DCM debounce number**
14:10		peri_dcm_rg_sf sel	**Selects PERI DCM idle divide** 10000: /1 01000: /2 00100: /4 00010: /8 00001: /16 00000: /32
9:5		peri_dcm_rg_fs el	**Selects PERI DCM active divide** 10000: /1 01000: /2 00100: /4 00010: /8 00001: /16 00000: /32
4		peri_dcm_rg_fo rce_on	**Forces on PERI DCM clock** 0: Disable 1: Enable
3		peri_dcm_rg_fo rce_clkslow	**PERI DCM force clock slow** 0: Disable 1: Enable
2		peri_dcm_rg_fo rce_clkoff	**PERI DCM force clock off** 0: Disable 1: Enable
1		peri_dcm_rg_cl	**Enables PERI DCM clock slow**

Bit(s)	Mnemonic	Name	Description
		kslow_en	0: Disable 1: Enable
0		peri_dcm_rg_clkoff_en	**Enables PERI DCM clock off** 0: Disable 1: Enable

10001078 MEM_DCM_CTRL Infrasys DCM Control Register 03E05F00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	mem_dcm_hwcg_off_disable		mem_mdsys_gating_sel	mem_mcu_wfi_cg_off_enable		mem_dcm_force_off	mem_dcm_idle_fsel					mem_dcm_fsel				
Type	RW		RW	RW		RW	RW					RW				
Reset	0		0	0		0	1	1	1	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mem_dcm_dbc_cnt							mem_dcm_dbc_en	mem_dcm_dcm_en	mem_dcm_force_on	mem_dcm_apb_sel					mem_dcm_apb_toggle
Type	RW							RW	RW	RW	RW					RW
Reset	0	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		mem_dcm_hwcg_off_disable	**Disables hardware clock gating for MEM bus domain** 1: Disble DCM 0: Enable DCM
29		mem_mdsys_gating_sel	**MEM CLK to MDSYS gating condition** 0: MEM bus idle 1: srclkena
28		mem_mcu_wfi_cg_off_enable	**Disables MEM bus WFI_L2 DCM** 0: Enable DCM 1: Disable DCM
26		mem_dcm_force_off	**DCM output clk is 0.**
25:21		mem_dcm_idle_fsel	**Selects DCM idle divide**
20:16		mem_dcm_fsel	**Selects DCM active divide**
15:9		mem_dcm_dbc_cnt	**Debounce count**
8		mem_dcm_dbc_en	**Enables debounce** 0: Enable 1: Disable
7		mem_dcm_dcm_en	**clk is not slowed down. DCM state indication signal = 0.** 0: Enable 1: Disable
6		mem_dcm_force_on	**clk is not slowed down.**
5:1		mem_dcm_apb_sel	**Each bit corresponds to the selection of change to activate.** bit 0: dcm_force_on bit 1: dcm_en bit 2: dbc_en bit 3: dcm_fsel bit 4: dcm_idle_fsel

Bit(s)	Mnemonic	Name	Description
0		mem_dcm_apb_to ggle	**Toggle the bit to activate the change** 0: Disable 1: Enable

1000107C DFS_MEM_DCM_CTRL **Infrasys DCM Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							dramc_pipe_slowdown_enable	dramc_pipe_ck_cg	mfg_mo_clk_ready_on_dis	cci_m2_clk_ready_on_dis	cci_m1_clk_ready_on_dis	dramc1_hclk_ck_cg	dramco_hclk_ck_cg	dramc_free_clk_switch_rate_enable	dramc_free_clk_slow_ratio	
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
9		dramc_pipe_slowdown_enable	**Enables DRAMC pipeslowdown** 0: Disable 1: Enable
8		dramc_pipe_ck_ cg	**Enables DRAMC pipe gating** 0: Disable 1: Enable
7		mfg_mo_clk_ready_on_dis	**Diables mfg_mo clock ready on** 0: Enable clk_ready_on 1: Disable clk_ready_on
6		cci_m2_clk_ready_on_dis	**Diables cci_m2 clock ready on** 0: Enable clk_ready_on 1: Disable clk_ready_on
5		cci_m1_clk_ready_on_dis	**Diables cci_m1 clock ready on** 0: Enable clk_ready_on 1: Disable clk_ready_on
4		dramc1_hclk_ck _cg	**Enables DRAMC1 clock gating** 0: Disable DCM 1: Enable DCM
3		dramco_hclk_ck _cg	**Enables DRAMCo clock gating** 0: Disable DCM 1: Enable DCM
2		dramc_free_clk_switch_rate_e nable	
1:0		dramc_free_clk_slow_ratio	**After slow_ratio is configured, write switch_rate_enable to 1 then 0 to latch the setting.** 0: DIV1 1: DIV16 2: DIV32 3: DIV64

10001080 MODULE_SW_CG_0_SET **Infrasys DCM Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	btif_cg_set	fhctl_cg_set	md2md_ccif_2_cg_set	md2md_ccif_1_cg_set	md2md_ccif_0_cg_set		uart3_cg_set	uart2_cg_set	uart1_cg_set	uart0_cg_set	pwm_cg_set		pwm4_cg_set	pwm3_cg_set	pwm2_cg_set	pwm1_cg_set
Type	WO	WO	WO	WO	WO		WO	WO	WO	WO	WO		WO	WO	WO	WO
Reset	0	0	0	0	0		0	0	0	0	0		0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pwm_hclk_cg_set	i2c3_cg_set	i2c2_cg_set	i2c1_cg_set	i2c0_cg_set	therm_cg_set	gce_cg_set	icusb_cg_set	sej_13m_cg_set	apxgpt_cg_set	sej_cg_set	scp_cg_set	pmic_cg_conn_set	pmic_cg_md_set	pmic_cg_ap_set	pmic_cg_tmr_set
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		btif_cg_set	**Sets up BTIF SWCG** 0: Enable 1: Disable
30		fhctl_cg_set	**Sets up FHCTL SWCG** 0: Enable 1: Disable
29		md2md_ccif_2_cg_set	
28		md2md_ccif_1_cg_set	
27		md2md_ccif_0_cg_set	
25		uart3_cg_set	**Sets up UART3 SWCG** 0: Enable 1: Disable
24		uart2_cg_set	**Sets up UART2 SWCG** 0: Enable 1: Disable
23		uart1_cg_set	**Sets up UART1 SWCG** 0: Enable 1: Disable
22		uart0_cg_set	**Sets up UART0 SWCG** 0: Enable 1: Disable
21		pwm_cg_set	**Sets up PWM SWCG** 0: Enable 1: Disable
19		pwm4_cg_set	**Sets up PWM4 SWCG** 0: Enable 1: Disable
18		pwm3_cg_set	**Sets up PWM3 SWCG** 0: Enable 1: Disable
17		pwm2_cg_set	**Sets up PWM2 SWCG** 0: Enable 1: Disable
16		pwm1_cg_set	**Sets up PWM1 SWCG** 0: Enable 1: Disable

Bit(s)	Mnemonic	Name	Description
15		pwm_hclk_cg_se t	**Sets up PWM HCLK SWCG** 0: Enable 1: Disable
14		i2c3_cg_set	**Sets up I2C3 SWCG** 0: Enable 1: Disable
13		i2c2_cg_set	**Sets up I2C2 SWCG** 0: Enable 1: Disable
12		i2c1_cg_set	**Sets up I2C1 SWCG** 0: Enable 1: Disable
11		i2c0_cg_set	**Sets up I2C0 SWCG** 0: Enable 1: Disable
10		therm_cg_set	**Sets up THERM_CTRL SWCG** 0: Enable 1: Disable
9		gce_cg_set	**Sets up GCE SWCG** 0: Enable 1: Disable
8		icusb_cg_set	**Sets up ICUSB SWCG** 0: Enable 1: Disable
7		sej_13m_cg_set	**Sets up SEJ_13M SWCG** 0: Enable 1: Disable
6		apxgpt_cg_set	**Sets up GPT SWCG** 0: Enable 1: Disable
5		sej_cg_set	**Sets up SEJ SWCG** 0: Enable 1: Disable
4		scp_cg_set	**Sets up SCP SWCG** 0: Enable 1: Disable
3		pmic_cg_conn_s et	**Sets up PMIC CONN SWCG** 0: Enable 1: Disable
2		pmic_cg_md_set	**Sets up PMIC MD SWCG** 0: Enable 1: Disable
1		pmic_cg_ap_set	**Sets up PMIC AP SWCG** 0: Enable 1: Disable
0		pmic_cg_tmr_se t	**Sets up PMIC TMR SWCG** 0: Enable 1: Disable

10001084 MODULE_SW_CG_0_CLR **Infrasys DCM Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	btif_cg_clr	fhctl_cg_clr	md2md_ccif_2_cg_clr	md2md_ccif_1_cg_clr	md2md_ccif_0_cg_clr		uart3_cg_clr	uart2_cg_clr	uart1_cg_clr	uart0_cg_clr	pwm_cg_clr		pwm4_cg_clr	pwm3_cg_clr	pwm2_cg_clr	pwm1_cg_clr
Type	WO	WO	WO	WO	WO		WO	WO	WO	WO	WO		WO	WO	WO	WO
Reset	0	0	0	0	0		0	0	0	0	0		0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pwm_hclk_cg_clr	i2c3_cg_clr	i2c2_cg_clr	i2c1_cg_clr	i2c0_cg_clr	therm_cg_clr	gce_cg_clr	icusb_cg_clr	sej_13m_cg_clr	apxgpt_cg_clr	sej_cg_clr	scp_cg_clr	pmic_cg_conn_clr	pmic_cg_md_clr	pmic_cg_ap_clr	pmic_cg_tmr_clr
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		btif_cg_clr	**Clears BTIF SWCG** 0: Enable 1: Disable
30		fhctl_cg_clr	**Clears FHCTL SWCG** 0: Enable 1: Disable
29		md2md_ccif_2_c g_clr	
28		md2md_ccif_1_c g_clr	
27		md2md_ccif_0_c g_clr	
25		uart3_cg_clr	**Clears UART3 SWCG** 0: Enable 1: Disable
24		uart2_cg_clr	**Clears UART2 SWCG** 0: Enable 1: Disable
23		uart1_cg_clr	**Clears UART1 SWCG** 0: Enable 1: Disable
22		uart0_cg_clr	**Clears UART0 SWCG** 0: Enable 1: Disable
21		pwm_cg_clr	**Clears PWM SWCG** 0: Enable 1: Disable
19		pwm4_cg_clr	**Clears PWM4 SWCG** 0: Enable 1: Disable
18		pwm3_cg_clr	**Clears PWM3 SWCG** 0: Enable 1: Disable
17		pwm2_cg_clr	**Clears PWM2 SWCG** 0: Enable 1: Disable
16		pwm1_cg_clr	**Clears PWM1 SWCG** 0: Enable 1: Disable
15		pwm_hclk_cg_cl r	**Clears PWM HCLK SWCG** 0: Enable 1: Disable
14		i2c3_cg_clr	**Clears I2C3 SWCG** 0: Enable

Bit(s)	Mnemonic	Name	Description
			1: Disable
13		i2c2_cg_clr	**Clears I2C2 SWCG** 0: Enable 1: Disable
12		i2c1_cg_clr	**Clears I2C1 SWCG** 0: Enable 1: Disable
11		i2c0_cg_clr	**Clears I2C0 SWCG** 0: Enable 1: Disable
10		therm_cg_clr	**Clears THERM_CTRL SWCG** 0: Enable 1: Disable
9		gce_cg_clr	**Clears GCE SWCG** 0: Enable 1: Disable
8		icusb_cg_clr	**Clears ICUSB SWCG** 0: Enable 1: Disable
7		sej_13m_cg_clr	**Clears SEJ_13M SWCG** 0: Enable 1: Disable
6		apxgpt_cg_clr	**Clears GPT SWCG** 0: Enable 1: Disable
5		sej_cg_clr	**Clears SEJ SWCG** 0: Enable 1: Disable
4		scp_cg_clr	**Clears SCP SWCG** 0: Enable 1: Disable
3		pmic_cg_conn_c lr	**Clears PMIC CONN SWCG** 0: Enable 1: Disable
2		pmic_cg_md_clr	**Clears PMIC MD SWCG** 0: Enable 1: Disable
1		pmic_cg_ap_clr	**Clears PMIC AP SWCG** 0: Enable 1: Disable
0		pmic_cg_tmr_cl r	**Clears PMIC TMR SWCG** 0: Enable 1: Disable

10001088 MODULE_SW_CG_1_SET **Infrasys DCM Control Register** **00000400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dramc_f26m_cg_set	md1dbg_ap_bus_ck_cg_set	md1lte_ap_bus_ck_cg_set	md1bus_ap_bus_ck_cg_set	md1mcu_ap_bus_ck_cg_set	ccif_md_cg_set	audio_cg_set	debugsys_cg_set	ccif_ap_cg_set	l2c_sram_cg_set	md11sys_ap_bus_ck_cg_set	device_apc_cg_set	md11mcu_ap_bus_ck_cg_set	ap_dma_cg_set	disppwm_cg_set	cldma_cg_set
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ap_c2k_ccif_1_cg_set	ap_c2k_ccif_0_cg_set	cpum_cg_set	auxadc_cg_set	trng_cg_set	gcpu_cg_set	md2md_ccif_5_cg_set	msdc3_cg_set	msdc2_cg_set	msdc1_cg_set	md2md_ccif_4_cg_set	msdc0_cg_set	spi_cg_set	md2md_ccif_3_cg_set
Type			WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset			0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		dramc_f26m_cg_ set	**Sets up DRAMC_26M SWCG** 0: Enable 1: Disable
30		md1dbg_ap_bus_ ck_cg_set	**Sets up MD1DBG_AP_BUS_CK SWCG** 0: Enable 1: Disable
29		md1lte_ap_bus_ ck_cg_set	**Sets up MD1LTE_AP_BUS_CK SWCG** 0: Enable 1: Disable
28		md1bus_ap_bus_ ck_cg_set	**Sets up MD1BUS_AP_BUS_CK SWCG** 0: Enable 1: Disable
27		md1mcu_ap_bus_ ck_cg_set	**Sets up MD1MCU_AP_BUS_CK SWCG** 0: Enable 1: Disable
26		ccif_md_cg_set	**Sets up CCIF MD SWCG** 0: Enable 1: Disable
25		audio_cg_set	**Sets up AUDIO SWCG** 0: Enable 1: Disable
24		debugsys_cg_se t	**Sets up DEBUGSYS SWCG** 0: Enable 1: Disable
23		ccif_ap_cg_set	**Sets up CCIF AP SWCG** 0: Enable 1: Disable
22		l2c_sram_cg_se t	**Sets up L2C_SRAM SWCG** 0: Enable 1: Disable
21		md1l1sys_ap_bu s_ck_cg_set	**Sets up MD1L1SYS_AP_BUS_CK SWCG** 0: Enable 1: Disable
20		device_apc_cg_ set	**Sets up DEVICE_APC SWCG** 0: Enable 1: Disable
19		md1l1mcu_ap_bu s_ck_cg_set	**Sets up MD1L1MCU_AP_BUS_CK SWCG** 0: Enable 1: Disable
18		ap_dma_cg_set	**Sets up AP_DMA SWCG** 0: Enable 1: Disable
17		disp_pwm_cg_se t	**Sets up DISP_PWM SWCG** 0: Enable 1: Disable
16		cldma_cg_set	**Sets up CLDMA SWCG**

Bit(s)	Mnemonic	Name	Description
			0: Enable 1: Disable
13		ap_c2k_ccif_1_ cg_set	
12		ap_c2k_ccif_0_ cg_set	
11		cpum_cg_set	**Sets up CPUM SWCG** 0: Enable 1: Disable
10		auxadc_cg_set	**Sets up AUXADC SWCG** 0: Enable 1: Disable
9		trng_cg_set	**TRNG_SWCG_SET** 0: Enable 1: Disable
8		gcpu_cg_set	**Sets up GCPU SWCG** 0: Enable 1: Disable
7		md2md_ccif_5_c g_set	
6		msdc3_cg_set	**Sets up MSDC3 SWCG** 0: Enable 1: Disable
5		msdc2_cg_set	**Sets up MSDC2 SWCG** 0: Enable 1: Disable
4		msdc1_cg_set	**Sets up MSDC1 SWCG** 0: Enable 1: Disable
3		md2md_ccif_4_c g_set	
2		msdc0_cg_set	**Sets up MSDC0 SWCG** 0: Enable 1: Disable
1		spi_cg_set	**Sets up SPI SWCG** 0: Enable 1: Disable
0		md2md_ccif_3_c g_set	

1000108C MODULE_SW_CG_1_CLR **Infrasys DCM Control Register** **00000400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dramc_f26m_cg_clr	md1dbg_ap_bus_ck_cg_clr	md1lte_ap_bus_ck_cg_clr	md1bus_ap_bus_ck_cg_clr	md1mcu_ap_bus_ck_cg_clr	ccif_md_cg_clr	audio_cg_clr	debugsys_cg_clr	ccif_ap_cg_clr	l2c_sram_cg_clr	md11sys_ap_bus_ck_cg_clr	device_apc_cg_clr	md11mcu_ap_bus_ck_cg_clr	ap_dma_cg_clr	disppwm_cg_clr	cldma_cg_clr
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ap_c2k_ccif_1_cg_clr	ap_c2k_ccif_0_cg_clr	cpum_cg_clr	auxadc_cg_clr	trng_cg_clr	gcpu_cg_clr	md2md_ccif_5_cg_clr	msdc3_cg_clr	msdc2_cg_clr	msdc1_cg_clr	md2md_ccif_4_cg_clr	msdc0_cg_clr	spi_cg_clr	md2md_ccif_3_cg_clr
Type			WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset			0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		dramc_f26m_cg_ clr	**Clears DRAMC_26M SWCG** 0: Enable 1: Disable
30		md1dbg_ap_bus_ ck_cg_clr	**Clears MD1DBG_AP_BUS_CK SWCG** 0: Enable 1: Disable
29		md1lte_ap_bus_ ck_cg_clr	**Clears MD1LTE_AP_BUS_CK SWCG** 0: Enable 1: Disable
28		md1bus_ap_bus_ ck_cg_clr	**Clears MD1BUS_AP_BUS_CK SWCG** 0: Enable 1: Disable
27		md1mcu_ap_bus_ ck_cg_clr	**Clears MD1MCU_AP_BUS_CK SWCG** 0: Enable 1: Disable
26		ccif_md_cg_clr	**Clears CCIF MD SWCG** 0: Enable 1: Disable
25		audio_cg_clr	**Clears AUDIO SWCG** 0: Enable 1: Disable
24		debugsys_cg_cl r	**Clears DEBUGSYS SWCG** 0: Enable 1: Disable
23		ccif_ap_cg_clr	**Clears CCIF AP SWCG** 0: Enable 1: Disable
22		l2c_sram_cg_cl r	**Clears L2C_SRAM SWCG** 0: Enable 1: Disable
21		md1l1sys_ap_bu s_ck_cg_clr	**Clears MD1L1SYS_AP_BUS_CK SWCG** 0: Enable 1: Disable
20		device_apc_cg_ clr	**Clears DEVICE_APC SWCG** 0: Enable 1: Disable
19		md1l1mcu_ap_bu s_ck_cg_clr	**Clears MD1L1MCU_AP_BUS_CK SWCG** 0: Enable 1: Disable
18		ap_dma_cg_clr	**Clears AP_DMA SWCG** 0: Enable 1: Disable
17		disp_pwm_cg_cl r	**Clears DISP_PWM SWCG** 0: Enable 1: Disable
16		cldma_cg_clr	**Clears CLDMA SWCG** 0: Enable 1: Disable
13		ap_c2k_ccif_1_ cg_clr	
12		ap_c2k_ccif_0_ cg_clr	
11		cpum_cg_clr	**Clears CPUM SWCG** 0: Enable 1: Disable
10		auxadc_cg_clr	**Clears AUXADC SWCG** 0: Enable

Bit(s)	Mnemonic	Name	Description
			1: Disable
9		trng_cg_clr	**Clears TRNG SWCG** 0: Enable 1: Disable
8		gcpu_cg_clr	**Clears GCPU SWCG** 0: Enable 1: Disable
7		md2md_ccif_5_c g_clr	
6		msdc3_cg_clr	**Clears MSDC3 SWCG** 0: Enable 1: Disable
5		msdc2_cg_clr	**Clears MSDC2 SWCG** 0: Enable 1: Disable
4		msdc1_cg_clr	**Clears MSDC1 SWCG** 0: Enable 1: Disable
3		md2md_ccif_4_c g_clr	
2		msdc0_cg_clr	**Clears MSDC0 SWCG** 0: Enable 1: Disable
1		spi_cg_clr	**Clears SPI SWCG** 0: Enable 1: Disable
0		md2md_ccif_3_c g_clr	

10001090 MODULE_SW_CG_0_STA **Infrasys DCM Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	btif_cg_sta	fhctl_cg_sta	md2md_ccif_2_cg_sta	md2md_ccif_1_cg_sta	md2md_ccif_0_cg_sta		uart3_cg_sta	uart2_cg_sta	uart1_cg_sta	uart0_cg_sta	pwm_cg_sta		pwm4_cg_sta	pwm3_cg_sta	pwm2_cg_sta	pwm1_cg_sta
Type	RO	RO	RO	RO	RO		RO	RO	RO	RO	RO		RO	RO	RO	RO
Reset	0	0	0	0	0		0	0	0	0	0		0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pwm_hclk_cg_sta	i2c3_cg_sta	i2c2_cg_sta	i2c1_cg_sta	i2c0_cg_sta	therm_cg_sta	gce_cg_sta	icusb_cg_sta	sej_13m_cg_sta	apxgpt_cg_sta	sej_cg_sta	scp_cg_sta	pmic_cg_conn_sta	pmic_cg_md_sta	pmic_cg_ap_sta	pmic_cg_tmr_sta
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		btif_cg_sta	**BTIF SWCG status** 0: Enable 1: Disable
30		fhctl_cg_sta	**FHCTL SWCG status** 0: Enable 1: Disable
29		md2md_ccif_2_c g_sta	
28		md2md_ccif_1_c g_sta	
27		md2md_ccif_0_c	

Bit(s)	Mnemonic	Name	Description
		g_sta	
25		uart3_cg_sta	**UART3 SWCG status** 0: Enable 1: Disable
24		uart2_cg_sta	**UART2 SWCG status** 0: Enable 1: Disable
23		uart1_cg_sta	**UART1 SWCG status** 0: Enable 1: Disable
22		uart0_cg_sta	**UART0 SWCG status** 0: Enable 1: Disable
21		pwm_cg_sta	**PWM SWCG status** 0: Enable 1: Disable
19		pwm4_cg_sta	**PWM4 SWCG status** 0: Enable 1: Disable
18		pwm3_cg_sta	**PWM3 SWCG status** 0: Enable 1: Disable
17		pwm2_cg_sta	**PWM2 SWCG status** 0: Enable 1: Disable
16		pwm1_cg_sta	**PWM1 SWCG status** 0: Enable 1: Disable
15		pwm_hclk_cg_st a	**PWM HCLK SWCG status** 0: Enable 1: Disable
14		i2c3_cg_sta	**I2C3 SWCG status** 0: Enable 1: Disable
13		i2c2_cg_sta	**I2C2 SWCG status** 0: Enable 1: Disable
12		i2c1_cg_sta	**I2C1 SWCG status** 0: Enable 1: Disable
11		i2c0_cg_sta	**I2C0 SWCG status** 0: Enable 1: Disable
10		therm_cg_sta	**THERM_CTRL SWCG status** 0: Enable 1: Disable
9		gce_cg_sta	**GCE SWCG status** 0: Enable 1: Disable
8		icusb_cg_sta	**ICUSB SWCG status** 0: Enable 1: Disable
7		sej_13m_cg_sta	**SEJ_13M SWCG status** 0: Enable 1: Disable

Bit(s)	Mnemonic	Name	Description
6		apxgpt_cg_sta	**GPT SWCG status** 0: Enable 1: Disable
5		sej_cg_sta	**SEJ SWCG status** 0: Enable 1: Disable
4		scp_cg_sta	**SCP SWCG status** 0: Enable 1: Disable
3		pmic_cg_conn_s ta	**PMIC CONN SWCG status** 0: Enable 1: Disable
2		pmic_cg_md_sta	**PMIC MD SWCG status** 0: Enable 1: Disable
1		pmic_cg_ap_sta	**PMIC AP SWCG status** 0: Enable 1: Disable
0		pmic_cg_tmr_st a	**PMIC TMR SWCG status** 0: Enable 1: Disable

10001094 MODULE_SW_CG_1_STA **Infrasys DCM Control Register** **00000400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dramc_f26m_cg_st a	md1dbg_ap_bus_ck_cg_sta	md1lte_ap_bus_ck_cg_sta	md1bus_ap_bus_ck_cg_sta	md1mcu_ap_bus_ck_cg_sta	ccif_md_cg_sta	audio_cg_sta	debugsys_cg_sta	ccif_ap_cg_sta	l2c_sram_cg_sta	xiu2ahb_cg_sta	device_apc_cg_st a	md1l1mcu_ap_bus_ck_cg_st a	ap_dma_cg_st a	disp_pwm_cg_sta	cldma_cg_sta
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ap_c2k_ccif_1_cg_sta	ap_c2k_ccif_0_cg_sta	cpum_cg_sta	auxadc_cg_st a		gcpu_cg_sta	md2md_ccif_5_cg_sta	msdc3_cg_sta	msdc2_cg_sta	msdc1_cg_sta	md2md_ccif_4_cg_sta	msdc0_cg_sta	spi_cg_sta	md2md_ccif_3_cg_sta
Type			RO	RO	RO	RO		RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset			0	0	0	1		0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		dramc_f26m_cg_ sta	**DRAMC_26M SWCG status** 0: Enable 1: Disable
30		md1dbg_ap_bus_ ck_cg_sta	**MD1DBG_AP_BUS_CK SWCG status** 0: Enable 1: Disable
29		md1lte_ap_bus_ ck_cg_sta	**MD1LTE_AP_BUS_CK SWCG status** 0: Enable 1: Disable
28		md1bus_ap_bus_ ck_cg_sta	**MD1BUS_AP_BUS_CK SWCG status** 0: Enable 1: Disable

Bit(s)	Mnemonic	Name	Description
27		md1mcu_ap_bus_ck_cg_sta	**MD1MCU_AP_BUS_CK SWCG status** 0: Enable 1: Disable
26		ccif_md_cg_sta	**CCIF MD SWCG status** 0: Enable 1: Disable
25		audio_cg_sta	**AUDIO SWCG status** 0: Enable 1: Disable
24		debugsys_cg_st a	**DEBUGSYS SWCG status** 0: Enable 1: Disable
23		ccif_ap_cg_sta	**CCIF AP SWCG status** 0: Enable 1: Disable
22		l2c_sram_cg_st a	**L2C_SRAM SWCG status** 0: Enable 1: Disable
21		xiu2ahb_cg_sta	**XIU2AHB SWCG status** 0: Enable 1: Disable
20		device_apc_cg_ sta	**DEVICE_APC SWCG status** 0: Enable 1: Disable
19		md1l1mcu_ap_bus_ck_cg_sta	**MD1L1MCU_AP_BUS_CK SWCG status** 0: Enable 1: Disable
18		ap_dma_cg_sta	**AP_DMA SWCG status** 0: Enable 1: Disable
17		disp_pwm_cg_st a	**DISP_PWM SWCG status** 0: Enable 1: Disable
16		cldma_cg_sta	**CLDMA SWCG status** 0: Enable 1: Disable
13		ap_c2k_ccif_1_ cg_sta	
12		ap_c2k_ccif_0_ cg_sta	
11		cpum_cg_sta	**CPUM SWCG status** 0: Enable 1: Disable
10		auxadc_cg_sta	**AUXADC SWCG status** 0: Enable 1: Disable
8		gcpu_cg_sta	**GCPU SWCG status** 0: Enable 1: Disable
7		md2md_ccif_5_c g_sta	
6		msdc3_cg_sta	**MSDC3 SWCG status** 0: Enable 1: Disable
5		msdc2_cg_sta	**MSDC2 SWCG status** 0: Enable 1: Disable
4		msdc1_cg_sta	**MSDC1 SWCG status**

Bit(s)	Mnemonic	Name	Description
			0: Enable 1: Disable
3		md2md_ccif_4_c g_sta	
2		msdc0_cg_sta	**MSDC0 SWCG status** 0: Enable 1: Disable
1		spi_cg_sta	**SPI SWCG status** 0: Enable 1: Disable
0		md2md_ccif_3_c g_sta	

10001098 MODULE_CLK_SEL **Infrasys DCM Control Register** **00001C70**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sys_cirq_ck_sel	dbg_sel		spi5_ck_sel	spi4_ck_sel	spi3_ck_sel	dramc_b_ck_sel	ulposc_ck_sel	dramc_ck_sel	spi2_ck_sel	spi1_ck_sel	spi_ck_sel	uart3_ck_sel	uart2_ck_sel	uart1_ck_sel	uart0_ck_sel
Type	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15		sys_cirq_ck_se l	**Selects SYS_CIRQ clock** 0:66m 1:ulposc/4
14:13		dbg_sel	**Selects debug**
12		spi5_ck_sel	**Selects SPI5 clock** 0: 66m 1: 133m
11		spi4_ck_sel	**Selects SPI4 clock** 0: 66m 1: 133m
10		spi3_ck_sel	**Selects SPI3 clock** 0: 66m 1: 133m
9		dramc_b_ck_sel	**Selects DRAMC_B 26M** 0: 26m 1: 3.25m
8		ulposc_ck_sel	**Selects ULPOSC** 0: Div8 1: Div16
7		dramc_ck_sel	**Selects DRAMC 26M** 0: 26m 1: 3.25m
6		spi2_ck_sel	**Selects SPI clock** 0: 66m 1: 133m
5		spi1_ck_sel	**Selects SPI clock**

Bit(s)	Mnemonic	Name	Description
			0: 66m 1: 133m
4		spi_ck_sel	**Selects SPI clock** 0: 66m 1: 133m
3		uart3_ck_sel	**Selects UART3 clock** 0: 52m 1: 26m
2		uart2_ck_sel	**Selects UART2 clock** 0: 52m 1: 26m
1		uart1_ck_sel	**Selects UART1 clock** 0: 52m 1: 26m
0		uart0_ck_sel	**Selects UART0 clock** 0: 52m 1: 26m

1000109C MEM_CG_CTRL **Infrasys DCM Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													rg_fmem_cg_ctrl			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0		rg_fmem_cg_ctr l	

100010A0 PTP_RX_CLK_ON **rg_p2p_rx_clk_force_on** **0000000F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													rg_p2p_rx_clk_force_on			
Type													RW			
Reset													1	1	1	1

Bit(s)	Mnemonic	Name	Description
3:0		rg_p2p_rx_clk_ force_on	

100010A4 DRAMC_WBR **rg_dramc_wbr** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														rg_dramc_wbr		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0		rg_dramc_wbr	

100010A8 MODULE_SW_CG_2_SET **Infrasys DCM Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dramc_b_conf_cg_set	dramc_conf_cg_set	vad_wrap_soc_cg_set	modem_temp_share_cg_set	audio_26m_pad_top_cg_set	audio_26m_cg_set	ssusb_ref_cg_set	ssusb_sys_cg_set	irtx_cg_set	spi5_cg_set	spi4_cg_set	spi3_cg_set	spi2_cg_set	ssusb_bus_cg_set	aes_top1_cg_set	aes_topo_cg_set
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dvfs_spm1_cg_set	dvfs_spm0_cg_set	anc_md32_32k_cg_set	anc_md32_cg_set	dramc_b_f26m_cg_set	spi1_cg_set		sys_cirq_cg_set	i2c5_cg_set	i2c3_arb_cg_set	i2c3_imm_cg_set	i2c2_arb_cg_set	i2c2_imm_cg_set	i2c_gpupm_cg_set	i2c_appm_cg_set	i2c4_cg_set
Type	WO	WO	WO	WO	WO	WO		WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		dramc_b_conf_c g_set	**Sets up DRAMC_B_CONF SWCG** 0: Enable 1: Disable
30		dramc_conf_cg_ set	**Sets up DRAMC_CONF SWCG** 0: Enable 1: Disable
29		vad_wrap_soc_c g_set	**Sets up VAD_WRAP_SOC SWCG** 0: Enable 1: Disable
28		modem_temp_sha re_cg_set	**Sets up MODEM_TEMP_SHARE SWCG** 0: Enable 1: Disable
27		audio_26m_pad_ top_cg_set	**Sets up AUDIO_26M_PAD_TOP SWCG** 0: Enable 1: Disable
26		audio_26m_cg_s et	**Sets up AUDIO_26M SWCG**

Bit(s)	Mnemonic	Name	Description
			0: Enable 1: Disable
25		ssusb_ref_cg_s et	**Sets up SSUSB_REF SWCG** 0: Enable 1: Disable
24		ssusb_sys_cg_s et	**Sets up SSUSB_SYS SWCG** 0: Enable 1: Disable
23		irtx_cg_set	**IRTX_CG_SET** 0: Enable 1: Disable
22		spi5_cg_set	**Sets up SPI5 SWCG** 0: Enable 1: Disable
21		spi4_cg_set	**Sets up SPI4 SWCG** 0: Enable 1: Disable
20		spi3_cg_set	**Sets up SPI3 SWCG** 0: Enable 1: Disable
19		spi2_cg_set	**Sets up SPI2 SWCG** 0: Enable 1: Disable
18		ssusb_bus_cg_s et	**Sets up SSUSB_BUS SWCG** 0: Enable 1: Disable
17		aes_top1_cg_se t	**Sets up AES_TOP1 SWCG** 0: Enable 1: Disable
16		aes_top0_cg_se t	**Sets up AES_TOP0 SWCG** 0: Enable 1: Disable
15		dvfs_spm1_cg_s et	**Sets up DVFS_SPM1 SWCG** 0: Enable 1: Disable
14		dvfs_spm0_cg_s et	**Sets up DVFS_SPM0 SWCG** 0: Enable 1: Disable
13		anc_md32_32k_c g_set	**Sets up ANC_MD32_32K SWCG** 0: Enable 1: Disable
12		anc_md32_cg_se t	**Sets up ANC_MD32 SWCG** 0: Enable 1: Disable
11		dramc_b_f26m_c g_set	**Sets up DRAMC_B_26M SWCG** 0: Enable 1: Disable
10		spi1_cg_set	**Sets up SPI1 SWCG** 0: Enable 1: Disable
8		sys_cirq_cg_se t	**Sets up SYS_CIRQ SWCG** 0: Enable 1: Disable
7		i2c5_cg_set	**Sets up I2C5 SWCG** 0: Enable

Bit(s)	Mnemonic	Name	Description
			1: Disable
6		i2c3_arb_cg_se t	**Sets up I2C3_ARB SWCG**
			0: Enable
			1: Disable
5		i2c3_imm_cg_se t	**Sets up I2C3_IMM SWCG**
			0: Enable
			1: Disable
4		i2c2_arb_cg_se t	**Sets up I2C2_ARB SWCG**
			0: Enable
			1: Disable
3		i2c2_imm_cg_se t	**Sets up I2C2_IMM SWCG**
			0: Enable
			1: Disable
2		i2c_gpupm_cg_s et	**Sets up I2C_GPUPM SWCG**
			0: Enable
			1: Disable
1		i2c_appm_cg_se t	**Sets up I2C_APPM SWCG**
			0: Enable
			1: Disable
0		i2c4_cg_set	**Sets up I2C4 SWCG**
			0: Enable
			1: Disable

100010AC MODULE_SW_CG_2_CLR **Infrasys DCM Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dramc_b_conf_cg_clr	dramc_conf_cg_cl r	vad_wrap_soc_cg_clr	modem_temp_share_cg_clr	audio_26m_pad_top_cg_clr	audio_26m_cg_clr	ssusb_ref_cg_clr	ssusb_sys_cg_clr	irtx_cg_clr	spi5_cg_clr	spi4_cg_clr	spi3_cg_clr	spi2_cg_clr	ssusb_bus_cg_clr	aes_top1_cg_clr	aes_topo_cg_clr
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dvfs_spm1_cg_clr	dvfs_spm0_cg_clr	anc_md32_32k_cg_clr	anc_md32_cg_clr	dramc_b_f26m_cg_clr	spi1_cg_clr		sys_cirq_cg_clr	i2c5_cg_clr	i2c3_arb_cg_clr	i2c3_imm_cg_clr	i2c2_arb_cg_clr	i2c2_imm_cg_clr	i2c_gpupm_cg_clr	i2c_appm_cg_clr	i2c4_cg_clr
Type	WO	WO	WO	WO	WO	WO		WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		dramc_b_conf_c g_clr	**Clears DRAMC_B_CONF SWCG**
			0: Enable
			1: Disable
30		dramc_conf_cg_ clr	**Clears DRAMC_CONF SWCG**
			0: Enable
			1: Disable
29		vad_wrap_soc_c g_clr	**Clears VAD_WRAP_SOC SWCG**
			0: Enable
			1: Disable
28		modem_temp_sha	**Clears MODEM_TEMP_SHARE SWCG**

Bit(s)	Mnemonic	Name	Description
		re_cg_clr	0: Enable 1: Disable
27		audio_26m_pad_top_cg_clr	**Clears AUDIO_26M_PAD_TOP SWCG** 0: Enable 1: Disable
26		audio_26m_cg_c lr	**Clears AUDIO_26M SWCG** 0: Enable 1: Disable
25		ssusb_ref_cg_c lr	**Clears SSUSB_REF SWCG** 0: Enable 1: Disable
24		ssusb_sys_cg_c lr	**Clears SSUSB_SYS SWCG** 0: Enable 1: Disable
23		irtx_cg_clr	**IRTX_CG_CLR** 0: Enable 1: Disable
22		spi5_cg_clr	**Clears SPI5 SWCG** 0: Enable 1: Disable
21		spi4_cg_clr	**Clears SPI4 SWCG** 0: Enable 1: Disable
20		spi3_cg_clr	**Clears SPI3 SWCG** 0: Enable 1: Disable
19		spi2_cg_clr	**Clears SPI2 SWCG** 0: Enable 1: Disable
18		ssusb_bus_cg_c lr	**Clears SSUSB_BUS SWCG** 0: Enable 1: Disable
17		aes_top1_cg_cl r	**Clears AES_TOP1 SWCG** 0: Enable 1: Disable
16		aes_top0_cg_cl r	**Clears AES_TOP0 SWCG** 0: Enable 1: Disable
15		dvfs_spm1_cg_c lr	**Clears DVFS_SPM1 SWCG** 0: Enable 1: Disable
14		dvfs_spm0_cg_c lr	**Clears DVFS_SPM0 SWCG** 0: Enable 1: Disable
13		anc_md32_32k_cg_clr	**Clears ANC_MD32_32K SWCG** 0: Enable 1: Disable
12		anc_md32_cg_cl r	**Clears ANC_MD32 SWCG** 0: Enable 1: Disable
11		dramc_b_f26m_c g_clr	**Clears DRAMC_B_26M SWCG** 0: Enable 1: Disable
10		spi1_cg_clr	**Clears SPI1 SWCG** 0: Enable

Bit(s)	Mnemonic	Name	Description
			1: Disable
8		sys_cirq_cg_cl r	**SYS_CIRQ_CG_CLR** 0: Enable 1: Disable
7		i2c5_cg_clr	**Clears I2C5 SWCG** 0: Enable 1: Disable
6		i2c3_arb_cg_cl r	**Clears I2C3_ARB SWCG** 0: Enable 1: Disable
5		i2c3_imm_cg_cl r	**Clears I2C3_IMM SWCG** 0: Enable 1: Disable
4		i2c2_arb_cg_cl r	**Clears I2C2_ARB SWCG** 0: Enable 1: Disable
3		i2c2_imm_cg_cl r	**Clears I2C2_IMM SWCG** 0: Enable 1: Disable
2		i2c_gpupm_cg_c lr	**Clears I2C_GPUPM SWCG** 0: Enable 1: Disable
1		i2c_appm_cg_cl r	**Clears I2C_APPM SWCG** 0: Enable 1: Disable
0		i2c4_cg_clr	**Clears I2C4 SWCG** 0: Enable 1: Disable

100010B0 MODULE_SW_CG_2_STA **Infrasys DCM Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dramc_b_conf_cg_sta	dramc_conf_cg_st a	vad_wrap_soc_cg_sta	modem_temp_share_cg_sta	audio_26m_pad_top_cg_sta	audio_26m_cg_sta	ssusb_ref_cg_sta	ssusb_sys_cg_sta	irtx_cg_sta	spi5_cg_sta	spi4_cg_sta	spi3_cg_sta	spi2_cg_sta	ssusb_bus_cg_sta	aes_top1_cg_sta	aes_topo_cg_sta
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dvfs_spm1_cg_sta	dvfs_spm0_cg_sta	anc_md32_32k_cg_sta	anc_md32_cg_sta	dramc_b_f26m_cg_sta	spi1_cg_sta		sys_cirq_cg_sta	i2c5_cg_sta	i2c3_arb_cg_sta	i2c3_imm_cg_sta	i2c2_arb_cg_sta	i2c2_imm_cg_sta	i2c_gpupm_cg_sta	i2c_appm_cg_sta	i2c4_cg_sta
Type	RO	RO	RO	RO	RO	RO		RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		dramc_b_conf_c g_sta	**DRAMC_B_CONF SWCG status** 0: Enable 1: Disable
30		dramc_conf_cg_ sta	**DRAMC_CONF SWCG status**

Bit(s)	Mnemonic	Name	Description
			0: Enable 1: Disable
29		vad_wrap_soc_c g_sta	**VAD_WRAP_SOC SWCG status** 0: Enable 1: Disable
28		modem_temp_sha re_cg_sta	**MODEM_TEMP_SHARE SWCG status** 0: Enable 1: Disable
27		audio_26m_pad_ top_cg_sta	**AUDIO_26M_PAD_TOP SWCG status** 0: Enable 1: Disable
26		audio_26m_cg_s ta	**AUDIO_26M SWCG status** 0: Enable 1: Disable
25		ssusb_ref_cg_s ta	**SSUSB_REF SWCG status** 0: Enable 1: Disable
24		ssusb_sys_cg_s ta	**SSUSB_SYS SWCG status** 0: Enable 1: Disable
23		irtx_cg_sta	**IRTX_CG_STA** 0: Enable 1: Disable
22		spi5_cg_sta	**SPI5 SWCG status** 0: Enable 1: Disable
21		spi4_cg_sta	**SPI4 SWCG status** 0: Enable 1: Disable
20		spi3_cg_sta	**SPI3 SWCG status** 0: Enable 1: Disable
19		spi2_cg_sta	**SPI2 SWCG status** 0: Enable 1: Disable
18		ssusb_bus_cg_s ta	**SSUSB_BUS SWCG status** 0: Enable 1: Disable
17		aes_top1_cg_st a	**AES_TOP1 SWCG status** 0: Enable 1: Disable
16		aes_top0_cg_st a	**AES_TOP0 SWCG status** 0: Enable 1: Disable
15		dvfs_spm1_cg_s ta	**DVFS_SPM1 SWCG status** 0: Enable 1: Disable
14		dvfs_spm0_cg_s ta	**DVFS_SPM0 SWCG status** 0: Enable 1: Disable
13		anc_md32_32k_c g_sta	**ANC_MD32_32K SWCG status** 0: Enable 1: Disable
12		anc_md32_cg_st a	**ANC_MD32 SWCG status** 0: Enable

Bit(s)	Mnemonic	Name	Description
			1: Disable
11		dramc_b_f26m_cg_sta	**DRAMC_B_26M SWCG status** 0: Enable 1: Disable
10		spi1_cg_sta	**SPI1 SWCG status** 0: Enable 1: Disable
8		sys_cirq_cg_st a	**SYS_CIRQ_CG_STA** 0: Enable 1: Disable
7		i2c5_cg_sta	**I2C5 SWCG status** 0: Enable 1: Disable
6		i2c3_arb_cg_st a	**I2C3_ARB SWCG status** 0: Enable 1: Disable
5		i2c3_imm_cg_st a	**I2C3_IMM SWCG status** 0: Enable 1: Disable
4		i2c2_arb_cg_st a	**I2C2_ARB SWCG status** 0: Enable 1: Disable
3		i2c2_imm_cg_st a	**I2C2_IMM SWCG status** 0: Enable 1: Disable
2		i2c_gpupm_cg_s ta	**I2C_GPUPM SWCG status** 0: Enable 1: Disable
1		i2c_appm_cg_st a	**I2C_APPM SWCG status** 0: Enable 1: Disable
0		i2c4_cg_sta	**I2C4 SWCG status** 0: Enable 1: Disable

10001100 I2C_DBTOOL_MISC **reg_dbg_i2c_rising_mode** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																rg_dbg_i2c_rising_mode
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
0		rg_dbg_i2c_ris ing_mode	

10001104 MD_SLEEP_CTRL_MASK md_sleep_ctrl_mask 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													md_sleep_ctrl_mas k			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0		md_sleep_ctrl_ mask	

10001108 PMICW_CLOCK_CTRL 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															spm_pmicw_sw_en	pmicw_26m_sel
Type															RW	RW
Reset															1	1

Bit(s)	Mnemonic	Name	Description
1		spm_pmicw_sw_e n	
0		pmicw_26m_sel	

1000110C SSUSB_INT_SEL ssusb int sel 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															ssusb_dev_int_md_sel	
Type															RW	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0		ssusb_dev_int_ md_sel	

10001120 INFRA_GLOBALCON_RSTOSET **Infrasys Always-on Reset Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																l2c_infra_swrst_set
Type																WO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dvfs_proc_1_swrst_set	dvfs_proc_0_swrst_set	cldma_swrst_set	btif_swrst_set	mipi_c_swrst_set	mipi_d_swrst_set	ap_dma_swrst_set	dramc_swrst_set	msdc0_swrst_set	msdc1_swrst_set	msdc2_swrst_set	msdc3_swrst_set	mm_iommu_swrst_set	peri_iommu_swrst_set	usb_top_swrst_set	therm_ctrl_swrst_set
Type	WO	WO	RO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		l2c_infra_swrs t_set	
15		dvfs_proc_1_sw rst_set	
14		dvfs_proc_0_sw rst_set	
13		cldma_swrst_se t	**Enables CLDMA software reset** 0: Normal 1: Enable reset
12		btif_swrst_set	**Enables BTIF software reset** 0: Normal 1: Enable reset
11		mipi_c_swrst_s et	**Enables MIPI_C software reset** 0: Normal 1: Enable reset
10		mipi_d_swrst_s et	**Enables MIPI_D software reset** 0: Normal 1: Enable reset
9		ap_dma_swrst_s et	**Enables AP_DMA software reset** 0: Normal 1: Enable reset
8		dramc_swrst_se t	**Enables DRAMC software reset** 0: Normal 1: Enable reset
7		msdc0_swrst_se t	**Enables MSDC0 software reset** 0: Normal 1: Enable reset
6		msdc1_swrst_se t	**Enables MSDC1 software reset** 0: Normal 1: Enable reset
5		msdc2_swrst_se t	**Enables MSDC2 software reset** 0: Normal 1: Enable reset

Bit(s)	Mnemonic	Name	Description
4		msdc3_swrst_se t	**Enables MSDC3 software reset** 0: Normal 1: Enable reset
3		mm_iommu_swrst _set	**Enables MM_IOMMU software reset** 0: Normal 1: Enable reset
2		peri_iommu_swr st_set	**Enables PERI IOMMU software reset** 0: Normal 1: Enable reset
1		usb_top_swrst_ set	**Enables USB software reset** 0: Normal 1: Enable reset
0		therm_ctrl_swr st_set	**Enables thermal control software reset** 0: Normal 1: Enable reset

10001124 INFRA_GLOBALCON_RST0_CLR **Infrasys Always-on Reset Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																l2c_infra_swrst_clr
Type																WO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dvfs_proc_1_swrst_clr	dvfs_proc_0_swrst_clr	cldma_swrst_clr	btif_swrst_clr	mipi_c_swrst_clr	mipi_d_swrst_clr	ap_dma_swrst_clr	dramc_swrst_clr	msdc0_swrst_clr	msdc1_swrst_clr	msdc2_swrst_clr	msdc3_swrst_clr	mm_iommu_swrst_clr	peri_iommu_swrst_clr	usb_top_swrst_clr	therm_ctrl_swrst_clr
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		l2c_infra_swrs t_clr	
15		dvfs_proc_1_sw rst_clr	
14		dvfs_proc_0_sw rst_clr	
13		cldma_swrst_cl r	**Disables CLDMA software reset** 0: Normal 1: Disable reset
12		btif_swrst_clr	**Disables BTIF software reset** 0: Normal 1: Disable reset
11		mipi_c_swrst_c lr	**Disables MIPI_C software reset** 0: Normal 1: Disable reset
10		mipi_d_swrst_c lr	**Disables MIPI_D software reset** 0: Normal 1: Disable reset
9		ap_dma_swrst_c lr	**Disables AP_DMA software reset** 0: Normal

Bit(s)	Mnemonic	Name	Description
			1: Disable reset
8		dramc_swrst_cl r	**Disables DRAMC software reset** 0: Normal 1: Disable reset
7		msdc0_swrst_cl r	**Disables MSDC0 software reset** 0: Normal 1: Disable reset
6		msdc1_swrst_cl r	**Disables MSDC1 software reset** 0: Normal 1: Disable reset
5		msdc2_swrst_cl r	**Disables MSDC2 software reset** 0: Normal 1: Disable reset
4		msdc3_swrst_cl r	**Disables MSDC3 software reset** 0: Normal 1: Disable reset
3		mm_iommu_swrst _clr	**Disables MM_IOMMU software reset** 0: Normal 1: Disable reset
2		peri_iommu_swr st_clr	**Disables PERI IOMMU software reset** 0: Normal 1: Disable reset
1		usb_top_swrst_ clr	**Disables USB software reset** 0: Normal 1: Disable reset
0		therm_ctrl_swr st_clr	**Disables thermal control software reset** 0: Normal 1: Disable reset

10001128 INFRA_GLOBALCON_RSTOSTA **Infrasys Always-on Reset Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																l2c_infra_swrst_sta
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dvfs_proc_1_swrst_sta	dvfs_proc_0_swrst_sta	cldma_swrst_sta	btif_swrst_sta	mipi_c_swrst_sta	mipi_d_swrst_sta	ap_dma_swrst_sta	dramc_swrst_sta	msdc0_swrst_sta	msdc1_swrst_sta	msdc2_swrst_sta	msdc3_swrst_sta	mm_iommu_swrst_sta	peri_iommu_swrst_sta	usb_top_swrst_sta	therm_ctrl_swrst_sta
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		l2c_infra_swrs t_sta	
15		dvfs_proc_1_sw rst_sta	
14		dvfs_proc_0_sw rst_sta	

Bit(s)	Mnemonic	Name	Description
13		cldma_swrst_st a	**CLDMA software reset status** 0: Normal 1: Reset status
12		btif_swrst_sta	**BTIF software reset status** 0: Normal 1: Reset status
11		mipi_c_swrst_s ta	**MIPI_C software reset status** 0: Normal 1: Reset status
10		mipi_d_swrst_s ta	**MIPI_D software reset status** 0: Normal 1: Reset status
9		ap_dma_swrst_s ta	**AP_DMA software reset status** 0: Normal 1: Reset status
8		dramc_swrst_st a	**DRAMC software reset status** 0: Normal 1: Reset status
7		msdc0_swrst_st a	**MSDC0 software reset status** 0: Normal 1: Reset status
6		msdc1_swrst_st a	**MSDC1 software reset status** 0: Normal 1: Reset status
5		msdc2_swrst_st a	**MSDC2 software reset status** 0: Normal 1: Reset status
4		msdc3_swrst_st a	**MSDC3 software reset status** 0: Normal 1: Reset status
3		mm_iommu_swrst _sta	**MM_IOMMU software reset status** 0: Normal 1: Reset status
2		peri_iommu_swr st_sta	**PERI IOMMU software reset status** 0: Normal 1: Reset status
1		usb_top_swrst_ sta	**USB software reset status** 0: Normal 1: Reset status
0		therm_ctrl_swr st_sta	**Thermal control software reset status** 0: Normal 1: Reset status

10001130 INFRA_GLOBALCON_RST1_SET **Infrasys Always-on Reset Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																l2c_infra_swrst_set
Type																WO

Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rsv														ssusb_top_swrst	
Type	WO														WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Mnemonic	Name	Description
16		l2c_infra_swrst_set	
15:2		rsv	
1		ssusb_top_swrst	

10001134 INFRA_GLOBALCON_RST1_CLR **Infrasys Always-on Reset Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																l2c_infra_swrst_clr
Type																WO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rsv														ssusb_top_swrst	
Type	WO														WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Mnemonic	Name	Description
16		l2c_infra_swrst_clr	
15:2		rsv	
1		ssusb_top_swrst	

10001138 INFRA_GLOBALCON_RST1_STA **Infrasys Always-on Reset Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																l2c_infra_swrst_sta
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rsv														ssusb_top_swrst	

Type	RO														RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Mnemonic	Name	Description
16		l2c_infra_swrs t_sta	
15:2		rsv	
1		ssusb_top_swrs t	

10001140 INFRA_GLOBALCON_RST2_SET **Infrasys Always-on Reset Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										ssusb_dig_phy_prst_b	scp_secure_swrst_set	cldma_ao_swrst_set	scp_swrst_set	usbsif_swrst_set	spm_swrst_set	pmic_wrap_swrst_set
Type										WO	WO	RO	WO	WO	WO	WO
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6		ssusb_dig_phy_ prst_b	
5		scp_secure_swr st_set	
4		cldma_ao_swrst _set	**Enables CLDMA AO software reset** 0: Normal 1: Reset status
3		scp_swrst_set	**Enables SCP software reset** 0: Normal 1: Enable reset
2		usbsif_swrst_s et	**Enables USBSIF software reset** 0: Normal 1: Enable reset
1		spm_swrst_set	**Enables SPM software reset** 0: Normal 1: Enable reset
0		pmic_wrap_swrs t_set	**Enables pmic_wrap software reset** 0: Normal 1: Enable reset

10001144 INFRA_GLOBALCON_RST2_CLR **Infrasys Always-on Reset Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name										ssusb_dig_phy_prst_b	scp_secure_swrst_clr	cldma_ao_swrst_clr	scp_swrst_clr	usbsif_swrst_clr	spm_swrst_clr	pmic_wrap_swrst_clr
Type										WO	WO	RO	WO	WO	WO	WO
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6		ssusb_dig_phy_ prst_b	
5		scp_secure_swr st_clr	
4		cldma_ao_swrst _clr	**Disables CLDMA AO software reset** 0: Normal 1: Reset status
3		scp_swrst_clr	**Disables SCP software reset** 0: Normal 1: Disable reset
2		usbsif_swrst_c lr	**Disables USBSIF software reset** 0: Normal 1: Disable reset
1		spm_swrst_clr	**Disables SPM software reset** 0: Normal 1: Disable reset
0		pmic_wrap_swrs t_clr	**Disables pmic_wrap software reset** 0: Normal 1: Disable reset

10001148 INFRA_GLOBALCON_RST2_STA **Infrasys Always-on Reset Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										ssusb_dig_phy_prst_b	scp_secure_swrst_sta	cldma_ao_swrst_sta	scp_swrst_sta	usbsif_swrst_sta	spm_swrst_sta	pmic_wrap_swrst_sta
Type										WO	RO	RO	RO	RO	RO	RO
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6		ssusb_dig_phy_ prst_b	
5		scp_secure_swr st_sta	
4		cldma_ao_swrst _sta	**CLDMA AO software reset status** 0: Normal 1: Reset status
3		scp_swrst_sta	**SCP software reset status** 0: Normal 1: Reset status
2		usbsif_swrst_s ta	**USBSIF software reset status** 0: Normal

Bit(s)	Mnemonic	Name	Description
			1: Reset status
1		spm_swrst_sta	**SPM software reset status** 0: Normal 1: Reset status
0		pmic_wrap_swrs t_sta	**pmic_wrap software reset status** 0: Normal 1: Reset status

10001160 LTE_OCCUPY_ANT **Set BPI 5~20 Controlled by LTE MODEM** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_lte_occupy_ant															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		reg_lte_occupy _ant	**LTE modem controls chip BPI pad.** 0: LTE modem does not occupy BPI. 1: LTE occupies BPI.

10001164 C2K_OCCUPY_ANT **Set BPI 5~20 Controlled by C2K MODEM** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_c2k_occupy_ant															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		reg_c2k_occupy _ant	**C2K modem controls chip BPI pad.** 0: C2K modem does not occupy BPI. 1: C2K occupies BPI.

10001168 LTE_C2K_BPI_CONFLICT **Record LTE C2K BPI Conflict Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																bpi_

																sw_conflict
Type																W1C
Reset																0

Bit(s)	Mnemonic	Name	Description
0		bpi_sw_conflict	**C2K LTE BPI SW conflict** 0: Normal 1: SW conflict

10001200 INFRA_TOPAXI_SI0_CTL **Top AXI Fabric SI0 Control Register** **050000F0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	topaxi_cg_disable				topaxi_mst_sync_sel		topaxi_slv_sync_sel									
Type	RW				RW		RW									
Reset	0				0	1	0	1								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									topaxi_sio_way_en						topaxi_sio_ctrl_bypass	topaxi_sio_outstanding_disable
Type									RW						RW	RW
Reset									1	1	1	1			0	0

Bit(s)	Mnemonic	Name	Description
31		topaxi_cg_disable	**Disables auto clock gating of all AXI components**
27:26		topaxi_mst_sync_sel	**Selects TOPAXI async slice master side sync**
25:24		topaxi_slv_sync_sel	**Selects TOPAXI async slice slave side sync**
7:4		topaxi_sio_way_en	**Controls output path of TOPAXI SI0** [6]: mmapb_s (including mfgsys) [5]: peri_s [4]: sram_s
1		topaxi_sio_ctrl_bypass	**Bypasses idle check when updating SI setting**
0		topaxi_sio_outstanding_disable	**Disables outstanding capability of SI0**

10001204 INFRA_TOPAXI_SI1_CTL **Top AXI Fabric SI1 Control Register** **30000030**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	gce2mmapb_cg_disable		mmapb_slice_early_en	mmapb_wbuf_early_en												
Type	RW		RW	RW												

Reset	0		1	1												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											topaxi_si1_way_en				topaxi_si1_ctrl_bypass	topaxi_si1_outstanding_disable
Type											RW				RW	RW
Reset											1	1			0	0

Bit(s)	Mnemonic	Name	Description
31		gce2mmapb_cg_disable	
29		mmapb_slice_early_en	**Disables/Bypasses MMAPB apb_slice write buffer (inside Infrasys)** 0: Disable 1: Enable
28		mmapb_wbuf_early_en	**Disables/Bypasses MMAPB write buffer (inside MMSYS)** 0: Disable 1: Enable
5:4		topaxi_si1_way _en	**Controls output path of TOPAXI SI1** [5]: peri_m1 [4]: topaxi_m1
1		topaxi_si1_ctr l_bypass	**Bypasses idle check when updating SI setting**
0		topaxi_si1_out standing_disab le	**Disables outstanding capability of SI1**

10001208 INFRA_TOPAXI_MDBUS_CTL **MDSYS AXI Fabric Control Register** **00000E83**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		mdmst_axi_cg_disable	mdslv_axi_cg_disable	mdahb_axi_cg_disable	md1_ahb2axi_merge_en	md1_ahb2axi_eight_byte_bus	md1_ahb2axi_ahb_buffer_en	md1_ahb2axi_hbstrb_en	md1_ahb2axi_hsecur_en		ap2md2_postwrite_dis	md12ap_postwrite_dis	md_mio_outstanding_extend_en	md_mio_qos_on	mdbus_axi2ahb_buffer_en	mdbus_axi2ahb_burst_en
Type		RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW
Reset		0	0	0	1	1	1	0	1		0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
14		mdmst_axi_cg_disable	**(Obsolete)** 0: Disable 1: Enable
13		mdslv_axi_cg_disable	**(Obsolete)** 0: Disable 1: Enable
12		mdahb_axi_cg_disable	**(Obsolete)**

Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable
11		md1_ahb2axi_merge_en	**(Obsolete)** 0: Disable 1: Enable
10		md1_ahb2axi_eight_byte_bus	**(Obsolete)** 0: Disable 1: Enable
9		md1_ahb2axi_ahb_buffer_en	**(Obsolete)** 0: Disable 1: Enable
8		md1_ahb2axi_hbstrb_en	**(Obsolete)** 0: Disable 1: Enable
7		md1_ahb2axi_hsecur_en	**(Obsolete)** 0: Disable 1: Enable
5		ap2md2_postwrite_dis	
4		md12ap_postwrite_dis	
3		md_mi0_outstanding_extend_en	
2		md_mi0_qos_on	
1		mdbus_axi2ahb_buffer_en	**(Obsolete)** 0: Disable 1: Enable
0		mdbus_axi2ahb_burst_en	**(Obsolete)** 0: Disable 1: Enable

1000120C INFRA_MCI_SI0_CTL **MCI Infra Top Dispatcher 0 Control Register** **00000030**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	mci_sio_aw_snoop_en_ack	mci_sio_ar_snoop_en_ack														
Type	RO	RO														
Reset	0	0														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						mci_sio_reorder_en	mci_sio_aw_snoop_en_req	mci_sio_ar_snoop_en_req			mci_sio_way_en				mci_sio_ctrl_bypass	mci_sio_outstanding_disable
Type						RW	RW	RW			RW				RW	RW
Reset						0	0	0			1	1			0	0

Bit(s)	Mnemonic	Name	Description
31		mci_sio_aw_snoop_en_ack	**Acknowledges aw snoop enable request**
30		mci_sio_ar_snoop_en_ack	**Acknowledges ar snoop enable request**

Bit(s)	Mnemonic	Name	Description
10		mci_sio_reorde r_en	**Enables command queue to reorder transaction** 0: Disable 1: Enable
9		mci_sio_aw_sno op_en_req	**Enable aw snoop path, or all transactions will enter EMI.** 0: Disable 1: Enable
8		mci_sio_ar_sno op_en_req	**Enable ar snoop path, or all transactions will enter EMI.** 0: Disable 1: Enable
5:4		mci_sio_way_en	**Controls output path of dispatcher** [4]: EMI [5]: snoop 0: Disable 1: Enable
1		mci_sio_ctrl_b ypass	**Bypasses idle check when updating SI setting** 0: Disable 1: Enable
0		mci_sio_outsta nding_disable	**Disables outstanding capibility of dispatcher** 0: Disable 1: Enable

10001210 INFRA_MCI_SI1_CTL **MCI Infra Top Dispatcher 1 Control Register** **00000030**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	mci_si1_aw_snoop_en_ack	mci_si1_ar_snoop_en_ack														
Type	RO	RO														
Reset	0	0														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						mci_si1_reorder_en	mci_si1_aw_snoop_en_req	mci_si1_ar_snoop_en_req			mci_si1_way_en				mci_si1_ctrl_bypass	mci_si1_outstanding_disable
Type						RW	RW	RW			RW				RW	RW
Reset						0	0	0			1	1			0	0

Bit(s)	Mnemonic	Name	Description
31		mci_si1_aw_sno op_en_ack	**Acknowledges aw snoop enable request**
30		mci_si1_ar_sno op_en_ack	**Acknowledges ar snoop enable request**
10		mci_si1_reorde r_en	**Enables command queue to reorder transaction** 0: Disable 1: Enable
9		mci_si1_aw_sno op_en_req	**Enable aw snoop path, or all transactions will enter EMI.**

Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable
8		mci_si1_ar_snoop_en_req	**Enable ar snoop path, or all transactions will enter EMI.** 0: Disable 1: Enable
5:4		mci_si1_way_en	**Controls output path of dispatcher** [4]: EMI [5]: snoop
1		mci_si1_ctrl_bypass	**Bypasses idle check when updating SI setting**
0		mci_si1_outstanding_disable	**Disables outstanding capibility of dispatcher** 0: Disable 1: Enable

10001214 INFRA_MCI_SI2_CTL **MCI Infra Top Dispatcher 2 Control Register** **00000070**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	mci_si2_aw_snoop_en_ack	mci_si2_ar_snoop_en_ack														
Type	RO	RO														
Reset	0	0														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						mci_si2_reorder_en	mci_si2_aw_snoop_en_req	mci_si2_ar_snoop_en_req		mci_si2_way_en					mci_si2_ctrl_bypass	mci_si2_outstanding_disable
Type						RW	RW	RW		RW					RW	RW
Reset						0	0	0		1	1	1			0	0

Bit(s)	Mnemonic	Name	Description
31		mci_si2_aw_snoop_en_ack	**Acknowledges aw snoop enable request**
30		mci_si2_ar_snoop_en_ack	**Acknowledges ar snoop enable request**
10		mci_si2_reorder_en	**Enables command queue to reorder transaction** 0: Disable 1: Enable
9		mci_si2_aw_snoop_en_req	**Enable aw snoop path, or all transactions will enter EMI.** 0: Disable 1: Enable
8		mci_si2_ar_snoop_en_req	**Enable ar snoop path, or all transactions will enter EMI.** 0: Disable 1: Enable
6:4		mci_si2_way_en	**Controls output path of dispatcher** [4]: EMI [5]: snoop
1		mci_si2_ctrl_bypass	**Bypasses idle check when updating SI setting**

Bit(s)	Mnemonic	Name	Description
0		mci_si2_outstanding_disable	**Disables outstanding capibility of dispatcher** 0: Disable 1: Enable

10001218 INFRA_MCI_ASYNC_CTRL **MCI IOMMU Asynchronous Slice Configure** **00000011**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							mci_iommu_depth_val									mci_iommu_reg_ar_fctrl_en
Type							RW									RW
Reset							0	0	0	0	0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		mci_iommu_wthre						mci_iommu_reg_aw_fctrl_en			mci_iommu_aslo_mst_sync_sel				mci_iommu_aslo_slv_sync_sel	
Type		RW						RW			RW				RW	
Reset		0	0	0				0			0	1			0	1

Bit(s)	Mnemonic	Name	Description
25:20		mci_iommu_depth_val	
16		mci_iommu_reg_ar_fctrl_en	**Enables read data channel flow control** 0: Disable 1: Enable
14:12		mci_iommu_wthr e	
8		mci_iommu_reg_aw_fctrl_en	**Enables write data channel flow control** 0: Disable 1: Enable
5:4		mci_iommu_aslo_mst_sync_sel	
1:0		mci_iommu_aslo_slv_sync_sel	

1000121C INFRA_MCI_CG_MFG_SEC_STA **MCI CG Disable Configure and MFG Secure Control** **00000004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												mfg_secure_si_outstandin	mfg_secure_si_ctrl_bypass	mfg_secure_si_way_en	mci_iommu_cg_disable	mci_infra_cg_disable

												g_disable				
Type												RW	RW	RW	RW	RW
Reset												0	0	1	0	0

Bit(s)	Mnemonic	Name	Description
4		mfg_secure_si_outstanding_disable	
3		mfg_secure_si_ctrl_bypass	
2		mfg_secure_si_way_en	
1		mci_iommu_cg_disable	
0		mci_infra_cg_disable	**Disables auto clock gating of all AXI components** 1: Disable 0: Enable

10001220 INFRA_TOPAXI_PROTECTEN **Top AXI Protect Module Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	abbmix_prot_en	reserved_prot_en							mfg_snoop_out_prot_en		mfg_mo_prot_en	iommu_prot_en	ap2conn_prot_en	conn2ap_prot_en		md1_l1sys_prot_en
Type	RW	RW							RW		RW	RW	RW	RW		RW
Reset	0	0	0	0	0	0	0	0	0		0	0	0	0		0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c2k2ap_prot_en	ap2c2k_prot_en	c2k_axi_prot_en	l2ss_aff_prot_en	l2ss_smi_prot_en	md1_l1mcu_prot_en	cci_mo_prot_en	cci_m2_prot_en	ap2md_md1_prot_en	mmapb_s_prot_en	md1_md2ap_prot_en	md1_mddma_prot_en	md1_psmcu_prot_en	mm_m1_prot_en	mm_m0_prot_en	cci_m1_prot_en
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		abbmix_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
30:24		reserved_prot_ en	**Enables AXI protection unit** 0: Disable 1: Enable
23		mfg_snoop_out_ prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
21		mfg_mo_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
20		iommu_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable

Bit(s)	Mnemonic	Name	Description
19		ap2conn_prot_e n	**Enables AXI protection unit** 0: Disable 1: Enable
18		conn2ap_prot_e n	**Enables AXI protection unit** 0: Disable 1: Enable
16		md1_l1sys_prot _en	**Enables AXI protection unit** 0: Disable 1: Enable
15		c2k2ap_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
14		ap2c2k_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
13		c2k_axi_prot_e n	**Enables AXI protection unit** 0: Disable 1: Enable
12		l2ss_aff_prot_ en	**Enables AXI protection unit** 0: Disable 1: Enable
11		l2ss_smi_prot_ en	**Enables AXI protection unit** 0: Disable 1: Enable
10		md1_l1mcu_prot _en	**Enables AXI protection unit** 0: Disable 1: Enable
9		cci_m0_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
8		cci_m2_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
7		ap2md_md1_prot _en	**Enables AXI protection unit** 0: Disable 1: Enable
6		mmapb_s_prot_e n	**Enables AXI protection unit** 0: Disable 1: Enable
5		md1_md2ap_prot _en	**Enables AXI protection unit** 0: Disable 1: Enable
4		md1_mddma_prot _en	**Enables AXI protection unit** 0: Disable 1: Enable
3		md1_psmcu_prot _en	**Enables AXI protection unit** 0: Disable 1: Enable
2		mm_m1_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
1		mm_m0_prot_en	**Enables AXI protection unit** 0: Disable 1: Enable
0		cci_m1_prot_en	**Enables AXI protection unit**

Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable

10001224 INFRA_TOPAXI_PROTECTSTA0 **Top AXI Protect Module Status Register 0** **E0FDFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved_prot_idle								mfg_snoop_out_prot_idle	mfg_m1_prot_idle	mfg_mo_prot_idle	iommu_prot_idle	ap2conn_prot_idle	conn2ap_prot_idle		md1_l1sys_prot_idle
Type	RU								RU	RU	RU	RU	RU	RU		RU
Reset	1	1	1	0	0	0	0	0	1	1	1	1	1	1		1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c2k2ap_prot_idle	ap2c2k_prot_idle	c2k_axi_prot_idle	l2ss_aff_prot_idle	l2ss_smi_prot_idle	md1_l1mcu_prot_idle	cci_mo_prot_idle	cci_m2_prot_idle	ap2md_md1_prot_idle	mmapb_s_prot_idle	md1_md2ap_prot_idle	md1_mddma_prot_idle	md1_psmcu_prot_idle	mm_m1_prot_idle	mm_mo_prot_idle	cci_m1_prot_idle
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		reserved_prot_ idle	**Indicates protect is in idle state** 0: Busy 1: Idle
23		mfg_snoop_out_ prot_idle	**Indicates protect is in idle state** 0: Busy 1: Idle
22		mfg_m1_prot_id le	**Indicates protect is in idle state** 0: Busy 1: Idle
21		mfg_mo_prot_id le	**Indicates protect is in idle state** 0: Busy 1: Idle
20		iommu_prot_idl e	**Indicates protect is in idle state** 0: Busy 1: Idle
19		ap2conn_prot_i dle	**Indicates protect is in idle state** 0: Busy 1: Idle
18		conn2ap_prot_i dle	**Indicates protect is in idle state** 0: Busy 1: Idle
16		md1_l1sys_prot _idle	**Indicates protect is in idle state** 0: Busy 1: Idle
15		c2k2ap_prot_id le	**Indicates protect is in idle state** 0: Busy 1: Idle
14		ap2c2k_prot_id le	**Indicates protect is in idle state** 0: Busy

Bit(s)	Mnemonic	Name	Description
			1: Idle
13		c2k_axi_prot_i dle	**Indicates protect is in idle state** 0: Busy 1: Idle
12		l2ss_aff_prot_ idle	**Indicates protect is in idle state** 0: Busy 1: Idle
11		l2ss_smi_prot_ idle	**Indicates protect is in idle state** 0: Busy 1: Idle
10		md1_l1mcu_prot _idle	**Indicates protect is in idle state** 0: Busy 1: Idle
9		cci_m0_prot_id le	**Indicates protect is in idle state** 0: Busy 1: Idle
8		cci_m2_prot_id le	**Indicates protect is in idle state** 0: Busy 1: Idle
7		ap2md_md1_prot _idle	**Indicates protect is in idle state** 0: Busy 1: Idle
6		mmapb_s_prot_i dle	**Indicates protect is in idle state** 0: Busy 1: Idle
5		md1_md2ap_prot _idle	**Indicates protect is in idle state** 0: Busy 1: Idle
4		md1_mddma_prot _idle	**Indicates protect is in idle state** 0: Busy 1: Idle
3		md1_psmcu_prot _idle	**Indicates protect is in idle state** 0: Busy 1: Idle
2		mm_m1_prot_idl e	**Indicates protect is in idle state** 0: Busy 1: Idle
1		mm_m0_prot_idl e	**Indicates protect is in idle state** 0: Busy 1: Idle
0		cci_m1_prot_id le	**Indicates protect is in idle state** 0: Busy 1: Idle

10001228 INFRA_TOPAXI_PROTECTSTA1 **Top AXI Protect Module Status Register 1** **FF400000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved_prot_rdy								mfg_snoop_out_prot_rdy	mfg_m1_prot_rdy	mfg_m0_prot_rdy	iommu_prot_rdy	ap2conn_prot_rdy	conn2ap_prot_rdy		md1_l1sys_prot_rdy

Type	RU								RU	RU	RU	RU	RU	RU		RU
Reset	1	1	1	1	1	1	1	1	0	1	0	0	0	0		0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c2k2ap_prot_rdy	ap2c2k_prot_rdy	c2k_emi_prot_rdy	l2ss_aff_prot_rdy	l2ss_smi_prot_rdy	md1_l1mcu_prot_rdy	cci_mo_prot_rdy	cci_m2_prot_rdy	ap2md_md1_prot_rdy	mmapb_s_prot_rdy	md1_md2ap_prot_rdy	md1_mddma_prot_rdy	md1_psmcu_prot_rdy	mm_m1_prot_r dy	mm_mo_prot_r dy	cci_m1_prot_rdy
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		reserved_prot_ rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
23		mfg_snoop_out_ prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
22		mfg_m1_prot_rd y	**Indicates protect is in protect mode** 0: Not ready 1: Ready
21		mfg_mo_prot_rd y	**Indicates protect is in protect mode** 0: Not ready 1: Ready
20		iommu_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
19		ap2conn_prot_r dy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
18		conn2ap_prot_r dy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
16		md1_l1sys_prot _rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
15		c2k2ap_prot_rd y	**Indicates protect is in protect mode** 0: Not ready 1: Ready
14		ap2c2k_prot_rd y	**Indicates protect is in protect mode** 0: Not ready 1: Ready
13		c2k_emi_prot_r dy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
12		l2ss_aff_prot_ rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
11		l2ss_smi_prot_ rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
10		md1_l1mcu_prot _rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
9		cci_mo_prot_rd y	**Indicates protect is in protect mode** 0: Not ready

Bit(s)	Mnemonic	Name	Description
			1: Ready
8		cci_m2_prot_rd y	**Indicates protect is in protect mode** 0: Not ready 1: Ready
7		ap2md_md1_prot _rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
6		mmapb_s_prot_r dy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
5		md1_md2ap_prot _rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
4		md1_mddma_prot _rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
3		md1_psmcu_prot _rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
2		mm_m1_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
1		mm_m0_prot_rdy	**Indicates protect is in protect mode** 0: Not ready 1: Ready
0		cci_m1_prot_rd y	**Indicates protect is in protect mode** 0: Not ready 1: Ready

10001238 INFRA_TOPAXI_PROTECTSTA2 **Top AXI Protect Module Status Register 2** **0000F48C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	protect_idle_47_32															
Type	RU															
Reset	1	1	1	1	0	1	0	0	1	0	0	0	1	1	0	0

Bit(s)	Mnemonic	Name	Description
15:0		protect_idle_4 7_32	

1000123C INFRA_TOPAXI_PROTECTSTA3 **Top AXI Protect Module Status Register 3** **0000FF77**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	protect_ready_47_32															
Type	RU															
Reset	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1

Bit(s)	Mnemonic	Name	Description
15:0		protect_ready_ 47_32	

1000122C INFRA_AXI_ASLICE_CTRL **Top AXI Aslice Control Register** **55555555**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved2_aslice_slv_sync_sel		md2hwmix_m2_aslice_slv_sync_sel		md2arm9_m1_aslice_slv_sync_sel		md1hwmix_m2_aslice_slv_sync_sel		md1cr4_m1_aslice_slv_sync_sel		reserved1_aslice_slv_sync _sel					
Type	RW		RW		RW		RW		RW		RW					
Reset	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved2_aslice_mst_sync_sel		md2hwmix_m2_aslice_mst_sync_sel		md2arm9_m1_aslice_mst_sync_sel		md1hwmix_m2_aslice_mst_sync_sel		md1cr4_m1_aslice_mst_sync_sel		reserved1_aslice_mst_sync _sel					
Type	RW		RW		RW		RW		RW		RW					
Reset	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
31:30		reserved2_aslice_slv_sync_sel	**Selects AXI aslice slave sync** 00: Sync 1T 01: Sync 2T 10: Sync 3T 11: Sync 3T
29:28		md2hwmix_m2_aslice_slv_sync_ sel	**Selects AXI aslice slave sync** 00: Sync 1T 01: Sync 2T 10: Sync 3T 11: Sync 3T
27:26		md2arm9_m1_aslice_slv_sync_s el	**Selects AXI aslice slave sync** 00: Sync 1T 01: Sync 2T 10: Sync 3T 11: Sync 3T
25:24		md1hwmix_m2_aslice_slv_sync_ sel	**Selects AXI aslice slave sync** 00: Sync 1T 01: Sync 2T 10: Sync 3T 11: Sync 3T
23:22		md1cr4_m1_aslice_slv_sync_sel	**Selects AXI aslice slave sync** 00: Sync 1T 01: Sync 2T 10: Sync 3T 11: Sync 3T
21:16		reserved1_aslice_slv_sync_sel	**Selects AXI aslice slave sync** 00: Sync 1T 01: Sync 2T

Bit(s)	Mnemonic	Name	Description
			10: Sync 3T 11: Sync 3T
15:14		reserved2_aslice_mst_sync_sel	**Selects AXI aslice master sync** 00: Sync 1T 01: Sync 2T 10: Sync 3T 11: Sync 3T
13:12		md2hwmix_m2_aslice_mst_sync_sel	**Selects AXI aslice master sync** 00: Sync 1T 01: Sync 2T 10: Sync 3T 11: Sync 3T
11:10		md2arm9_m1_aslice_mst_sync_sel	**Selects AXI aslice master sync** 00: Sync 1T 01: Sync 2T 10: Sync 3T 11: Sync 3T
9:8		md1hwmix_m2_aslice_mst_sync_sel	**Selects AXI aslice master sync** 00: Sync 1T 01: Sync 2T 10: Sync 3T 11: Sync 3T
7:6		md1cr4_m1_aslice_mst_sync_sel	**Selects AXI aslice master sync** 00: Sync 1T 01: Sync 2T 10: Sync 3T 11: Sync 3T
5:0		reserved1_aslice_mst_sync_sel	**Selects AXI aslice master sync** 00: Sync 1T 01: Sync 2T 10: Sync 3T 11: Sync 3T

10001230 INFRA_APB_ASYNC_STA **INFRASYSI ASYNC APB Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																bsibpi_apb_timer_en
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			efusec_apb_rx_timer_en	efusec_apb_tx_timer_en				apmixedsys_tx_timer_en				mipi_csi_apb_timer_en				mipi_dsi_apb_timer_en
Type			RW	RW				RW				RW				RW
Reset			0	0				0				0				0

Bit(s)	Mnemonic	Name	Description
16		bsibpi_apb_timer_en	
13		efusec_apb_rx_	**Enables RX timer**

Bit(s)	Mnemonic	Name	Description
		timer_en	0: Disable 1: Enable
12		efusec_apb_tx_ timer_en	**Enables TX timer** 0: Disable 1: Enable
8		apmixedsys_tx_ timer_en	**Enables TX timer** 0: Disable 1: Enable
4		mipi_csi_apb_t imer_en	**Enables TX timer** 0: Disable 1: Enable
0		mipi_dsi_apb_t imer_en	**Enables TX timer** 0: Disable 1: Enable

10001234 INFRA_TOPAXI_PROTECTEN1 **Top AXI Protect Module Control Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	protect_en_47_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		protect_en_47_ 32	

10001240 INFRA_MCI_TRANS_CON_READ **Infrasys MCI Transaction Read Configure** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			mci_r_th resh old_ con2								mci_r_thresho ld_con1					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			mci_r_threshold_cono													mci_r_limiter_enable
Type			RW													RW
Reset			0	0	0	0	0	0								0

Bit(s)	Mnemonic	Name	Description
29:24		mci_r_threshol d_con2	
21:16		mci_r_threshol d_con1	
13:8		mci_r_threshol d_cono	

Bit(s)	Mnemonic	Name	Description
0		mci_r_limiter_ enable	**Enables blocking function** 0: Disable 1: Enable

10001244 INFRA_MCI_TRANS_CON_WRITE **Infrasys MCI Transaction Write Configure** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			mci_ w_th resh old_ con2								mci_w_thresho ld_con1					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			mci_w_threshold_cono													mci_ w_li mite r_en able
Type			RW													RW
Reset			0	0	0	0	0	0								0

Bit(s)	Mnemonic	Name	Description
29:24		mci_w_threshol d_con2	
21:16		mci_w_threshol d_con1	
13:8		mci_w_threshol d_cono	
0		mci_w_limiter_ enable	**Enables blocking function** 0: Disable 1: Enable

10001248 INFRA_MCI_ID_REMAP_CON **Infrasys MCI ID Remap Configure** **00001001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				mci_ acp_ sio_ way_ inte rlea ve_e n				mci_ acp_ sio_ outs tand ing_ disa ble				mci_ acp_ sio_ ctrl _byp ass				mci_ acp_ sio_ way_ en
Type				RW				RW				RW				RW
Reset				1				0				0				1

Bit(s)	Mnemonic	Name	Description
12		mci_acp_sio_wa y_interleave_e n	

Bit(s)	Mnemonic	Name	Description
8		mci_acp_sio_ou tstanding_disa ble	
4		mci_acp_sio_ct rl_bypass	
0		mci_acp_sio_wa y_en	

1000124C INFRA_MCI_EMI_TRANSCON **Infrasys MCI EMI Threshold Sel Configure** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															emi_threshold_sel	
Type															RW	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0		emi_threshold_ sel	

10001260 MDSYS_INTFCON0 **MDSYS Interface Control 0** **78007800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		md1_l1sys_emi_arflush_thre		md1_l1sys_emi_awflush_thre		md1_l1sys_emi_wthre			md1_l1sys_emi_reg_aw_fctrl_en	md1_l1sys_emi_reg_ar_fctrl_en	md1_l1sys_emi_depth_val					
Type		RW		RW		RW			RW	RW	RW					
Reset		1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		md1_l1mcu_emi_arflush_thre		md1_l1mcu_emi_awflush_thre		md1_l1mcu_emi_wthre			md1_l1mcu_emi_reg_aw_fctrl_en	md1_l1mcu_emi_reg_ar_fctrl_en	md1_l1mcu_emi_depth_val					
Type		RW		RW		RW			RW	RW	RW					
Reset		1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:29		md1_l1sys_emi_ arflush_thre	
28:27		md1_l1sys_emi_ awflush_thre	
26:24		md1_l1sys_emi_ wthre	
23		md1_l1sys_emi_ reg_aw_fctrl_e n	

Bit(s)	Mnemonic	Name	Description
22		md1_l1sys_emi_reg_ar_fctrl_e n	
21:16		md1_l1sys_emi_depth_val	
14:13		md1_l1mcu_emi_arflush_thre	
12:11		md1_l1mcu_emi_awflush_thre	
10:8		md1_l1mcu_emi_wthre	
7		md1_l1mcu_emi_reg_aw_fctrl_e n	
6		md1_l1mcu_emi_reg_ar_fctrl_e n	
5:0		md1_l1mcu_emi_depth_val	

10001264 MDSYS_INTF_CON1 MDSYS Interface Control 1 78007800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		md1_psmcu_emi_arflush_thre		md1_psmcu_emi_awflush_thre		md1_psmcu_emi_wthre			md1_psmcu_emi_reg_aw_fctrl_e n	md1_psmcu_emi_reg_ar_fctrl_e n	md1_psmcu_emi_depth_val					
Type		RW		RW		RW			RW	RW	RW					
Reset		1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		md1_mddma_emi_arflush_thre		md1_mddma_emi_awflush_thre		md1_mddma_emi_wthre			md1_mddma_emi_reg_aw_fctrl_e n	md1_mddma_emi_reg_ar_fctrl_e n	md1_mddma_emi_depth_val					
Type		RW		RW		RW			RW	RW	RW					
Reset		1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:29		md1_psmcu_emi_arflush_thre	
28:27		md1_psmcu_emi_awflush_thre	
26:24		md1_psmcu_emi_wthre	
23		md1_psmcu_emi_reg_aw_fctrl_e n	
22		md1_psmcu_emi_reg_ar_fctrl_e n	
21:16		md1_psmcu_emi_depth_val	
14:13		md1_mddma_emi_arflush_thre	
12:11		md1_mddma_emi_awflush_thre	

Bit(s)	Mnemonic	Name	Description
10:8		md1_mddma_emi_ wthre	
7		md1_mddma_emi_ reg_aw_fctrl_e n	
6		md1_mddma_emi_ reg_ar_fctrl_e n	
5:0		md1_mddma_emi_ depth_val	

1000126C MDSYS_INTF_CON2 MDSYS Interface Control 2 00007800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		c2k_mcu_emi_arflush_thre		c2k_mcu_emi_awflush_thre		c2k_mcu_emi_wthre			c2k_mcu_emi_reg_aw_fctrl_en	c2k_mcu_emi_reg_ar_fctrl_en	c2k_mcu_emi_depth_val					
Type		RW		RW		RW			RW	RW	RW					
Reset		1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
14:13		c2k_mcu_emi_ar flush_thre	
12:11		c2k_mcu_emi_aw flush_thre	
10:8		c2k_mcu_emi_wt hre	
7		c2k_mcu_emi_re g_aw_fctrl_en	
6		c2k_mcu_emi_re g_ar_fctrl_en	
5:0		c2k_mcu_emi_de pth_val	

10001300 MD1_BANK0_MAP0 MDSYS1 Bank 0 Remap Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md1_bo_map3_addr							md1_bo_map3_en	md1_bo_map2_addr							md1_bo_map2_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md1_bo_map1_addr							md1_bo_map1_en	md1_bo_mapo_addr							md1_bo_mapo_en
Type	RW							RW	RW							RW

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		md1_bo_map3_ad dr	**Sub-bank3 remap address register**
24		md1_bo_map3_en	**Sub-bank3 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_011 will be remapped to bo_map3_addr. 0: Disable 1: Enable
23:17		md1_bo_map2_ad dr	**Sub-bank2 remap address register**
16		md1_bo_map2_en	**Sub-bank2 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_010 will be remapped to bo_map2_addr. 0: Disable 1: Enable
15:9		md1_bo_map1_ad dr	**Sub-bank1 remap address register**
8		md1_bo_map1_en	**Sub-bank0 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_001 will be remapped to bo_map1_addr. 0: Disable 1: Enable
7:1		md1_bo_map0_ad dr	**Sub-bank0 remap address register**
0		md1_bo_map0_en	**Sub-bank0 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_000 will be remapped to bo_map0_addr. 0: Disable 1: Enable

10001304 MD1_BANK0_MAP1 MDSYS1 Bank 0 Remap Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md1_bo_map7_addr							md1_bo_map7_en	md1_bo_map6_addr							md1_bo_map6_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md1_bo_map5_addr							md1_bo_map5_en	md1_bo_map4_addr							md1_bo_map4_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		md1_bo_map7_ad dr	**Sub-bank7 remap address register**
24		md1_bo_map7_en	**Sub-bank7 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_111 will be remapped to bo_map7_addr. 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable
23:17		md1_b0_map6_ad dr	**Sub-bank6 remap address register**
16		md1_b0_map6_en	**Sub-bank6 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_110 will be remapped to b0_map6_addr. 0: Disable 1: Enable
15:9		md1_b0_map5_ad dr	**Sub-bank5 remap address register**
8		md1_b0_map5_en	**Sub-bank5 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_101 will be remapped to b0_map5_addr. 0: Disable 1: Enable
7:1		md1_b0_map4_ad dr	**Sub-bank4 remap address register**
0		md1_b0_map4_en	**Sub-bank4 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_100 will be remapped to b0_map4_addr. 0: Disable 1: Enable

10001308 MD1_BANK1_MAP0 MDSYS1 Bank 1 Remap Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md1_b1_map3_addr							md1_b1_map3_en	md1_b1_map2_addr							md1_b1_map2_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md1_b1_map1_addr							md1_b1_map1_en	md1_b1_map0_addr							md1_b1_map0_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		md1_b1_map3_ad dr	**Sub-bank3 remap address register**
24		md1_b1_map3_en	**Sub-bank3 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_011 will be remapped to b1_map3_addr. 0: Disable 1: Enable
23:17		md1_b1_map2_ad dr	**Sub-bank2 remap address register**
16		md1_b1_map2_en	**Sub-bank2 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_010 will be remapped to b1_map2_addr. 0: Disable 1: Enable

Bit(s)	Mnemonic	Name	Description
15:9		md1_b1_map1_ad dr	**Sub-bank1 remap address register**
8		md1_b1_map1_en	**Sub-bank0 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_001 will be remapped to b1_map1_addr. 0: Disable 1: Enable
7:1		md1_b1_map0_ad dr	**Sub-bank0 remap address register**
0		md1_b1_map0_en	**Sub-bank0 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_000 will be remapped to b1_map0_addr. 0: Disable 1: Enable

1000130C MD1_BANK1_MAP1 **MDSYS1 Bank 1 Remap Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md1_b1_map7_addr							md1_b1_map7_en	md1_b1_map6_addr							md1_b1_map6_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md1_b1_map5_addr							md1_b1_map5_en	md1_b1_map4_addr							md1_b1_map4_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		md1_b1_map7_ad dr	**Sub-bank7 remap address register**
24		md1_b1_map7_en	**Sub-bank7 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_111 will be remapped to b1_map7_addr. 0: Disable 1: Enable
23:17		md1_b1_map6_ad dr	**Sub-bank6 remap address register**
16		md1_b1_map6_en	**Sub-bank6 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_110 will be remapped to b1_map6_addr. 0: Disable 1: Enable
15:9		md1_b1_map5_ad dr	**Sub-bank5 remap address register**
8		md1_b1_map5_en	**Sub-bank5 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_101 will be remapped to b1_map5_addr. 0: Disable 1: Enable
7:1		md1_b1_map4_ad dr	**Sub-bank4 remap address register**

Bit(s)	Mnemonic	Name	Description
0		md1_b1_map4_en	**Sub-bank4 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_100 will be remapped to b1_map4_addr. 0: Disable 1: Enable

10001310 MD1_BANK4_MAP0 MDSYS1 Bank 4 Remap Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md1_b4_map3_addr							md1_b4_map3_en	md1_b4_map2_addr							md1_b4_map2_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md1_b4_map1_addr							md1_b4_map1_en	md1_b4_map0_addr							md1_b4_map0_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		md1_b4_map3_ad dr	**Sub-bank3 remap address register**
24		md1_b4_map3_en	**Sub-bank3 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_011 will be remapped to b0_map3_addr. 0: Disable 1: Enable
23:17		md1_b4_map2_ad dr	**Sub-bank2 remap address register**
16		md1_b4_map2_en	**Sub-bank2 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_010 will be remapped to b0_map2_addr. 0: Disable 1: Enable
15:9		md1_b4_map1_ad dr	**Sub-bank1 remap address register**
8		md1_b4_map1_en	**Sub-bank0 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_001 will be remapped to b0_map1_addr. 0: Disable 1: Enable
7:1		md1_b4_map0_ad dr	**Sub-bank0 remap address register**
0		md1_b4_map0_en	**Sub-bank0 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_000 will be remapped to b4_map0_addr. 0: Disable 1: Enable

10001314 MD1_BANK4_MAP1 MDSYS1 Bank 4 Remap Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md1_b4_map7_addr							md1_b4_map7_en	md1_b4_map6_addr							md1_b4_map6_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md1_b4_map5_addr							md1_b4_map5_en	md1_b4_map4_addr							md1_b4_map4_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		md1_b4_map7_ad dr	**Sub-bank7 remap address register**
24		md1_b4_map7_en	**Sub-bank7 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_111 will be remapped to b0_map7_addr. 0: Disable 1: Enable
23:17		md1_b4_map6_ad dr	**Sub-bank6 remap address register**
16		md1_b4_map6_en	**Sub-bank6 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_110 will be remapped to b0_map6_addr. 0: Disable 1: Enable
15:9		md1_b4_map5_ad dr	**Sub-bank5 remap address register**
8		md1_b4_map5_en	**Sub-bank5 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_101 will be remapped to b0_map5_addr . 0: Disable 1: Enable
7:1		md1_b4_map4_ad dr	**Sub-bank4 remap address register**
0		md1_b4_map4_en	**Sub-bank4 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_100 will be remapped to b0_map4_addr. 0: Disable 1: Enable

10001320 MD2_BANK0_MAP0 MDSYS2 Bank 0 Remap Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md2_bo_map3_addr							md2_bo_map3_en	md2_bo_map2_addr							md2_bo_map2_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md2_bo_map1_addr							md2_bo_map1_en	md2_bo_map0_addr							md2_bo_map0_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		md2_bo_map3_addr	**Sub-bank3 remap address register**
24		md2_bo_map3_en	**Sub-bank3 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_011 will be remapped to bo_map3_addr. 0: Disable 1: Enable
23:17		md2_bo_map2_addr	**Sub-bank2 remap address register**
16		md2_bo_map2_en	**Sub-bank2 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_010 will be remapped to bo_map2_addr. 0: Disable 1: Enable
15:9		md2_bo_map1_addr	**Sub-bank1 remap address register**
8		md2_bo_map1_en	**Sub-bank0 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_001 will be remapped to bo_map1_addr. 0: Disable 1: Enable
7:1		md2_bo_map0_addr	**Sub-bank0 remap address register**
0		md2_bo_map0_en	**Sub-bank0 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_000 will be remapped to bo_map0_addr. 0: Disable 1: Enable

10001324 MD2_BANK0_MAP1 MDSYS2 Bank 0 Remap Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md2_bo_map7_addr							md2_bo_map7_en	md2_bo_map6_addr							md2_bo_map6_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md2_bo_map5_addr							md2_bo_map5_en	md2_bo_map4_addr							md2_bo_map4_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
31:25		md2_b0_map7_addr	**Sub-bank7 remap address register**
24		md2_b0_map7_en	**Sub-bank7 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_111 will be remapped to b0_map7_addr. 0: Disable 1: Enable
23:17		md2_b0_map6_addr	**Sub-bank6 remap address register**
16		md2_b0_map6_en	**Sub-bank6 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_110 will be remapped to b0_map6_addr. 0: Disable 1: Enable
15:9		md2_b0_map5_addr	**Sub-bank5 remap address register**
8		md2_b0_map5_en	**Sub-bank5 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_101 will be remapped to b0_map5_addr. 0: Disable 1: Enable
7:1		md2_b0_map4_addr	**Sub-bank4 remap address register**
0		md2_b0_map4_en	**Sub-bank4 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_100 will be remapped to b0_map4_addr. 0: Disable 1: Enable

10001330 MD2_BANK4_MAP0 MDSYS2 Bank 4 Remap Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md2_b4_map3_addr							md2_b4_map3_en	md2_b4_map2_addr							md2_b4_map2_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md2_b4_map1_addr							md2_b4_map1_en	md2_b4_map0_addr							md2_b4_map0_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		md2_b4_map3_addr	**Sub-bank3 remap address register**
24		md2_b4_map3_en	**Sub-bank3 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_011 will be remapped to b0_map3_addr. 0: Disable 1: Enable
23:17		md2_b4_map2_addr	**Sub-bank2 remap address register**

Bit(s)	Mnemonic	Name	Description
16		md2_b4_map2_en	**Sub-bank2 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_010 will be remapped to b0_map2_addr. 0: Disable 1: Enable
15:9		md2_b4_map1_ad dr	**Sub-bank1 remap address register**
8		md2_b4_map1_en	**Sub-bank0 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_001 will be remapped to b0_map1_addr. 0: Disable 1: Enable
7:1		md2_b4_map0_ad dr	**Sub-bank0 remap address register**
0		md2_b4_map0_en	**Selects debug** 0: Disable 1: Enable

10001334 MD2_BANK4_MAP1 MDSYS2 Bank 4 Remap Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md2_b4_map7_addr							md2_b4_map7_en	md2_b4_map6_addr							md2_b4_map6_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md2_b4_map5_addr							md2_b4_map5_en	md2_b4_map4_addr							md2_b4_map4_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		md2_b4_map7_ad dr	**Sub-bank7 remap address register**
24		md2_b4_map7_en	**Sub-bank7 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_111 will be remapped to b0_map7_addr. 0: Disable 1: Enable
23:17		md2_b4_map6_ad dr	**Sub-bank6 remap address register**
16		md2_b4_map6_en	**Sub-bank6 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_110 will be remapped to b0_map6_addr. 0: Disable 1: Enable
15:9		md2_b4_map5_ad dr	**Sub-bank5 remap address register**
8		md2_b4_map5_en	**Sub-bank5 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_101 will be remapped to b0_map5_addr.

Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable
7:1		md2_b4_map4_ad dr	**Sub-bank4 remap address register**
0		md2_b4_map4_en	**Sub-bank4 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_100 will be remapped to b0_map4_addr. 0: Disable 1: Enable

10001370 C2K_BANK0_MAP0 C2K Bank 0 Remap Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	c2k_b0_map3_addr							c2k_b0_map3_en	c2k_b0_map2_addr							c2k_b0_map2_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c2k_b0_map1_addr							c2k_b0_map1_en	c2k_b0_map0_addr							c2k_b0_map0_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		c2k_b0_map3_ad dr	**Sub-bank3 remap address register**
24		c2k_b0_map3_en	**Sub-bank3 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_011 will be remapped to b0_map3_addr. 0: Disable 1: Enable
23:17		c2k_b0_map2_ad dr	**Sub-bank2 remap address register**
16		c2k_b0_map2_en	**Sub-bank2 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_010 will be remapped to b0_map2_addr. 0: Disable 1: Enable
15:9		c2k_b0_map1_ad dr	**Sub-bank1 remap address register**
8		c2k_b0_map1_en	**Sub-bank0 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_001 will be remapped to b0_map1_addr. 0: Disable 1: Enable
7:1		c2k_b0_map0_ad dr	**Sub-bank0 remap address register**
0		c2k_b0_map0_en	**Sub-bank0 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_000 will be remapped to b0_map0_addr. 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable

10001374 C2K_BANK0_MAP1 C2K Bank 0 Remap Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	c2k_b0_map7_addr							c2k_b0_map7_en	c2k_b0_map6_addr							c2k_b0_map6_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c2k_b0_map5_addr							c2k_b0_map5_en	c2k_b0_map4_addr							c2k_b0_map4_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		c2k_b0_map7_ad dr	**Sub-bank7 remap address register**
24		c2k_b0_map7_en	**Sub-bank7 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_111 will be remapped to b0_map7_addr. 0: Disable 1: Enable
23:17		c2k_b0_map6_ad dr	**Sub-bank6 remap address register**
16		c2k_b0_map6_en	**Sub-bank6 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_110 will be remapped to b0_map6_addr. 0: Disable 1: Enable
15:9		c2k_b0_map5_ad dr	**Sub-bank5 remap address register**
8		c2k_b0_map5_en	**Sub-bank5 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_101 will be remapped to b0_map5_addr. 0: Disable 1: Enable
7:1		c2k_b0_map4_ad dr	**Sub-bank4 remap address register**
0		c2k_b0_map4_en	**Sub-bank4 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_100 will be remapped to b0_map4_addr. 0: Disable 1: Enable

10001378 C2K_BANK1_MAP0 C2K Bank 1 Remap Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	c2k_b1_map3_addr							c2k_	c2k_b1_map2_addr							c2k_

								b1_map3_en								b1_map2_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c2k_b1_map1_addr							c2k_b1_map1_en	c2k_b1_map0_addr							c2k_b1_map0_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		c2k_b1_map3_ad dr	**Sub-bank3 remap address register**
24		c2k_b1_map3_en	**Sub-bank3 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_011 will be remapped to b1_map3_addr. 0: Disable 1: Enable
23:17		c2k_b1_map2_ad dr	**Sub-bank2 remap address register**
16		c2k_b1_map2_en	**Sub-bank2 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_010 will be remapped to b1_map2_addr. 0: Disable 1: Enable
15:9		c2k_b1_map1_ad dr	**Sub-bank1 remap address register**
8		c2k_b1_map1_en	**Sub-bank0 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_001 will be remapped to b1_map1_addr. 0: Disable 1: Enable
7:1		c2k_b1_map0_ad dr	**Sub-bank0 remap address register**
0		c2k_b1_map0_en	**Sub-bank0 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_000 will be remapped to b1_map0_addr. 0: Disable 1: Enable

1000137C C2K_BANK1_MAP1 **C2K Bank 1 Remap Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	c2k_b1_map7_addr							c2k_b1_map7_en	c2k_b1_map6_addr							c2k_b1_map6_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c2k_b1_map5_addr							c2k_b1_map5_en	c2k_b1_map4_addr							c2k_b1_map4_en

Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		c2k_b1_map7_ad dr	**Sub-bank7 remap address register**
24		c2k_b1_map7_en	**Sub-bank7 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_111 will be remapped to b1_map7_addr. 0: Disable 1: Enable
23:17		c2k_b1_map6_ad dr	**Sub-bank6 remap address register**
16		c2k_b1_map6_en	**Sub-bank6 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_110 will be remapped to b1_map6_addr. 0: Disable 1: Enable
15:9		c2k_b1_map5_ad dr	**Sub-bank5 remap address register**
8		c2k_b1_map5_en	**Sub-bank5 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_101 will be remapped to b1_map5_addr. 0: Disable 1: Enable
7:1		c2k_b1_map4_ad dr	**Sub-bank4 remap address register**
0		c2k_b1_map4_en	**Sub-bank4 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0000_100 will be remapped to b1_map4_addr. 0: Disable 1: Enable

10001380 C2K_BANK4_MAP0 C2K Bank 4 Remap Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	c2k_b4_map3_addr							c2k_b4_map3_en	c2k_b4_map2_addr							c2k_b4_map2_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c2k_b4_map1_addr							c2k_b4_map1_en	c2k_b4_map0_addr							c2k_b4_map0_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		c2k_b4_map3_ad dr	**Sub-bank3 remap address register**
24		c2k_b4_map3_en	**Sub-bank3 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_011 will be remapped to b0_map3_addr.

Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable
23:17		c2k_b4_map2_ad dr	**Sub-bank2 remap address register**
16		c2k_b4_map2_en	**Sub-bank2 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_010 will be remapped to b0_map2_addr. 0: Disable 1: Enable
15:9		c2k_b4_map1_ad dr	**Sub-bank1 remap address register**
8		c2k_b4_map1_en	**Sub-bank0 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_001 will be remapped to b0_map1_addr. 0: Disable 1: Enable
7:1		c2k_b4_map0_ad dr	**Sub-bank0 remap address register**
0		c2k_b4_map0_en	**Sub-bank0 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_000 will be remapped to b4_map0_addr. 0: Disable 1: Enable

10001384 C2K_BANK4_MAP1 **C2K Bank 4 Remap Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	c2k_b4_map7_addr							c2k_b4_map7_en	c2k_b4_map6_addr							c2k_b4_map6_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c2k_b4_map5_addr							c2k_b4_map5_en	c2k_b4_map4_addr							c2k_b4_map4_en
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		c2k_b4_map7_ad dr	**Sub-bank7 remap address register**
24		c2k_b4_map7_en	**Sub-bank7 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_111 will be remapped to b0_map7_addr. 0: Disable 1: Enable
23:17		c2k_b4_map6_ad dr	**Sub-bank6 remap address register**
16		c2k_b4_map6_en	**Sub-bank6 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_110 will be remapped to b0_map6_addr. 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable
15:9		c2k_b4_map5_ad dr	**Sub-bank5 remap address register**
8		c2k_b4_map5_en	**Sub-bank5 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_101 will be remapped to b0_map5_addr. 0: Disable 1: Enable
7:1		c2k_b4_map4_ad dr	**Sub-bank4 remap address register**
0		c2k_b4_map4_en	**Sub-bank4 remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:25] = 7'b0100_100 will be remapped to b0_map4_addr. 0: Disable 1: Enable

10001340 CONN_MAP0 CONNSYS Bank Remap Register 180E0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	peri2conn_prog_remap															
Type	RW															
Reset	0	0	0	1	1	0	0	0	0	0	0	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	conn2ap_busreq_ultra	conn2ap_busreq_hp	conn_iommu	conn2ap_addr_remap												conn_cache
Type	RW	RW	RW	RW												RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		peri2conn_prog _remap	
15		conn2ap_busreq _ultra	
14		conn2ap_busreq _hp	
13		conn_iommu	
12:1		conn2ap_addr_r emap	
0		conn_cache	

10001344 CLDMA_MAP0 CLDMA AP Remap Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																usb_moly_remap_en
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				cldma_ap_map_addr												cldma_ap_map_en

Type				RW												RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		usb_moly_remap _en	
12:1		cldma_ap_map_a ddr	**CLDMA remap address register**
0		cldma_ap_map_e n	**CLDMA remap enable register** When disabled, the address will be unchanged. When enabled, addr[31:20] will be remapped to cldma_map_addr 0: Disable 1: Enable

10001348 MD_DUMMY **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_ap2md_dummy															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		reg_ap2md_dumm y	

10001350 CONN_BUS_CON **ConnSYS Interface Bus Control** **0000001D**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								conn2ap_is_sleep_mask	conn_ahb2axi_read_ahead_bw	conn_ahb2axi_fifo_threshold			conn_ahb2axi_merge_en	conn_ahb2axi_ahb_buffer_en	conn_ahb2axi_hstrb_en	conn_ahb2axi_hsecur_en
Type								RW	RW	RW			RW	RW	RW	RW
Reset								0	0	0	0	1	1	1	0	1

Bit(s)	Mnemonic	Name	Description
8		conn2ap_is_sle ep_mask	
7		conn_ahb2axi_r ead_ahead_bw	
6:4		conn_ahb2axi_f ifo_threshold	
3		conn_ahb2axi_m erge_en	

Bit(s)	Mnemonic	Name	Description
2		conn_ahb2axi_ahb_buffer_en	
1		conn_ahb2axi_hstrb_en	
0		conn_ahb2axi_hsecur_en	

10001368 C2K_HANDSHAKE **ap2c2k_ready** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															ap2c2k_wake_up	ap2c2k_ready
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1		ap2c2k_wake_up	
0		ap2c2k_ready	

10001400 PERI_CCI_SIDEBAND_CON **PERISYS to CCI-400 ACE Sideband Config** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	iommu_cci_arregion_reg				iommu_cci_arqos_reg				iommu_cci_arsnoop_reg				iommu_cci_arbar_reg		iommu_cci_ar_ace_domain_reg	
Type	RW				RW				RW				RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	iommu_cci_awregion_reg				iommu_cci_awqos_reg					iommu_cci_awsnoop_reg			iommu_cci_awbar_reg		iommu_cci_aw_ace_domain_reg	
Type	RW				RW					RW			RW		RW	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		iommu_cci_arregion_reg	
27:24		iommu_cci_arqos_reg	
23:20		iommu_cci_arsnoop_reg	
19:18		iommu_cci_arbar_reg	
17:16		iommu_cci_ar_ace_domain_reg	
15:12		iommu_cci_awregion_reg	
11:8		iommu_cci_awqo	

Bit(s)	Mnemonic	Name	Description
		s_reg	
6:4		iommu_cci_awsn oop_reg	
3:2		iommu_cci_awba r_reg	
1:0		iommu_cci_aw_a ce_domain_reg	

10001404 MFG_CCI_SIDEBAND_CON **MFG to CCI-400 Sideband Configure** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																mfg_cci_qos_use_real
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mfg_cci_arregion_reg				mfg_cci_arqos_reg				mfg_cci_awregion_reg				mfg_cci_awqos_reg			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		mfg_cci_qos_us e_real	
15:12		mfg_cci_arregi on_reg	
11:8		mfg_cci_arqos_ reg	
7:4		mfg_cci_awregi on_reg	
3:0		mfg_cci_awqos_ reg	

10001500 INFRA_AO_DBG_CON0 **Infra_AO debug Control 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					infra_ao_debug_mon_selo											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0		infra_ao_debug _mon_selo	Debug monitor control register 0

10001504 INFRA_AO_DBG_CON1 **Infra_AO debug Control 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					infra_ao_debug_mon_sel1											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0		infra_ao_debug_mon_sel1	Debug monitor control register 1

10001508 INFRA_AO_DBG_CON2 Infra_AO debug Control 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					infra_ao_debug_mon_sel2											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0		infra_ao_debug_mon_sel2	Debug monitor control register 2

1000150C INFRA_AO_DBG_CON3 Infra_AO debug Control 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					infra_ao_debug_mon_sel3											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0		infra_ao_debug_mon_sel3	Debug monitor control register 3

10001680 BOOT_MISC0 Spare Register for Bootrom 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_misco															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_misc0	Spare register for bootrom

10001684 BOOT_MISC1 Spare Register for Bootrom 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_misc0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_misc0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_misc0	Spare register for bootrom

10001688 BOOT_MISC2 Spare Register for Bootrom 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_misc0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_misc0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_misc0	Spare register for bootrom

1000168C BOOT_MISC3 Spare Register for Bootrom 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_misc0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_misc0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_misc0	Spare register for bootrom

10001690 BOOT_MISC4 Spare Register for Bootrom 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_misc0															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_misco	Spare register for bootrom

10001694 BOOT_MISC5 Spare Register for Bootrom 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_misco	Spare register for bootrom

10001698 BOOT_MISC6 Spare Register for Bootrom 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_misco	Spare register for bootrom

1000169C BOOT_MISC7 Spare Register for Bootrom 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	boot_misco															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		boot_misco	Spare register for bootrom

100016A0 MISC_LOCK_KEY — **KEY for Write Misc Control Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	misc_lock_key															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		misc_lock_key	KEY for write misc control register

100016A4 MISC_LOCK_CON — **LOCK for Write Misc Data Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									misc_lock_con							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		misc_lock_con	LOCK for write misc data register

100016A8 MISC_RST_CON — **Reset Control for Misc Data Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									misc_rst_con							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		misc_rst_con	Reset control for misc data register

100016AC MISC_SEC_CON — **Security Control for Misc Data Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								misc_sec_con								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		misc_sec_con	Security control for misc data register

10001700 INFRA_RSVD0 Infra Reserved 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_rsvd0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_rsvd0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		reg_rsvd0	

10001704 INFRA_RSVD1 Infra Reserved 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_rsvd1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		reg_rsvd1	

10001708 INFRA_RSVD2 Infra Reserved 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sw_efuse_mp_disable	reg_rsvd2														
Type	RW	RW														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15		sw_efuse_mp_di sable	
14:0		reg_rsvd2	

1000170C INFRA_RSVD3 **Infra Reserved 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_rsvd3							i2c_dmareq								
Type	RW							RW								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:9		reg_rsvd3	
8:0		i2c_dmareq	

10001900 INFRA_BONDING **INFRA_BONDING** **01800007**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								usbdl		reg_bonding_option						
Type								RU		RO						
Reset								1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_bonding_option															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
24:23		usbdl	
22:0		reg_bonding_op tion	Bonding option

10001A00 INFRA_AO_SCPSYS_APB_ASYNC_STA **Infra AO SCPSYS Async APB Interface** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			apb_async _scpsys_f hctl_rx_e rr_addr_r eg													apb_asyn c_scpsys_fhc tl_rx_ti mer_en
Type			RO													RW
Reset			0	0	0	0	0	0	0	0	0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name			apb_async_scpsys_fhctl_tx_err_addr_reg													apb_async_scpsys_fhctl_tx_timer_en
Type			RO													RW
Reset			0	0	0	0	0	0	0	0	0	0				0

Bit(s)	Mnemonic	Name	Description
29:20		apb_async_scpsys_fhctl_rx_err_addr_reg	
16		apb_async_scpsys_fhctl_rx_timer_en	
13:4		apb_async_scpsys_fhctl_tx_err_addr_reg	
0		apb_async_scpsys_fhctl_tx_timer_en	

10001A04 INFRA_AO_MD32_TX_APB_ASYNC_STA — **Infra AO MD32 TX Async APB Interface** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									apb_async_md32_err_tx_addr_reg							
Type									RO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	apb_async_md32_err_tx_addr_reg															apb_async_md32_tx_timer_en
Type	RO															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0				0

Bit(s)	Mnemonic	Name	Description
23:4		apb_async_md32_err_tx_addr_reg	
0		apb_async_md32_tx_timer_en	

10001A08 INFRA_AO_MD32_RX_APB_ASYNC_STA — **Infra AO MD32 RX Async APB Interface** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									apb_async_md32_err_rx_addr_reg							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	apb_async_md32_err_rx_addr_reg															apb_async_md32_rx_timer_en
Type	RO															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0				0

Bit(s)	Mnemonic	Name	Description
23:4		apb_async_md32_err_rx_addr_reg	
0		apb_async_md32_rx_timer_en	

10001A10 INFRA_AO_PMIC_TX_APB_ASYNC_STA — **Infra AO PMIC TX Async APB Interface** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													apb_async_pmic_wrap_tx_err_addr_reg			
Type													RO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	apb_async_pmic_wrap_tx_err_addr_reg															apb_async_pmic_wrap_tx_timer_en
Type	RO															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0				0

Bit(s)	Mnemonic	Name	Description
19:4		apb_async_pmic_wrap_tx_err_addr_reg	
0		apb_async_pmic_wrap_tx_timer_en	

10001A0C INFRA_AO_CKSYS_APB_ASYNC_STA — **Infra AO CKSYS Async APB Interface** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							apb_async_cksys_err_addr_reg									
Type							RO									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																apb_async_ck

																sys_timer_en
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
25:16		apb_async_cksys_err_addr_reg	
0		apb_async_cksys_timer_en	

10001600 MFG_MISC_CON 00030011

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															mfg_misc_reg_1	
Type															RW	
Reset															1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			mfg_misc_reg_0					mfg_dfd_en				mfg_sw_reset_en				mfg_clock_gated_en
Type			RW					RW				RW				RW
Reset			0	0				0				1				1

Bit(s)	Mnemonic	Name	Description
17:16		mfg_misc_reg_1	
13:12		mfg_misc_reg_0	
8		mfg_dfd_en	
4		mfg_sw_reset_e n	
0		mfg_clock_gate d_en	

10001F00 INFRA_MISC Infrasys Miscellaneous Control Register 11401200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md_src_req_1_en				md_src_req_0_en					spk_sdata_in_en	ap_dbgiic2usb_en	ltel1_pd_reserve_req	ltel1_clk_off_req	ltel1_mem_pd_req	ltel1_mtcmos_pd_req	ltel1_extpwr_off
Type	RW				RW					RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	1	0	0	0	1		1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	emitype_change_en	ap_usb2jtag_en	ddr_4gb_support_en	fhctl_f26m_en	conn_bt_cvsd_mask	ap2conn_osc_en	ap2conn_mcusys_wakeup_b	ap2conn_jtag_2wire		smi_early_response_enable	md_dbgack_mask		md_legacy_jtag_sel			emi_gated_when_dramc_idle
Type	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW		RW			RW
Reset	0	0	0	1	0	0	1	0		0	0	0	0	0		0

Bit(s)	Mnemonic	Name	Description
31:28		md_src_req_1_e n	
27:24		md_src_req_0_e n	
22		spk_sdata_in_e n	**Enables spk_miso pad_macro** 0: Disable 1: Enable
21		ap_dbgiic2usb_ en	**Enables DBG I2C to USB** 0: Disable 1: Enable
20		ltel1_pd_reser ve_req	**ltel1_pd_reserve_req**
19		ltel1_clk_off_ req	**ltel1_clk_off_req**
18		ltel1_mem_pd_r eq	**ltel1_mem_pd_req**
17		ltel1_mtcmos_p d_req	**ltel1_mtcmos_pd_req**
16		ltel1_extpwr_o ff	**Enables LTEL1 external power off ISO** 0: Disable 1: Enable
15		emitype_change _en	**Enables EMI type change** 0: Disable 1: Enable
14		ap_usb2jtag_en	**Enables USB to JTAG** 0: Disable 1: Enable
13		ddr_4gb_suppor t_en	**DDR 4GB support** 0: Disable 4 GB DDR support 1: Enable 4 GB DDR support
12		fhctl_f26m_en	**FHCTL 26MHz clock gating register** 0: Disable 26M clock to FHCTL 1: Enable 26M clock to FHCTL
11		conn_bt_cvsd_m ask	
10		ap2conn_osc_en	
9		ap2conn_mcusys _wakeup_b	**AP SW triggered interrupt to CONSYS register** 0: AP enable interrupt request to CONNSYS 1: AP disable interrupt request to CONNSYS
8		ap2conn_jtag_2 wire	**CONNSYS JTAG 2-wire switching register** 0: Disable 2-wire switching 1: Enable 2-wire switching
6		smi_early_resp onse_enable	
5:4		md_dbgack_mask	**MD DBGACK option** 0: Enable MD1's ack 1: bypass MD1's ack
3:2		md_legacy_jtag _sel	**Selects MDSYS legacy JTAG** 0: cs_jtag_ap 1: LEGACY_JTAG 2: Reserved 3: Reserved
0		emi_gated_when _dramc_idle	**EMI clock is gated when DRAMC is ilde.**

10001F04 INFRA_ACP **SW CCI Arcache Configure Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sw_peri_mo_awcache				sw_peri_mo_arcache							sw_mfg_cache_en				sw_peri_cache_en
Type	RW				RW							RW				RW
Reset	0	0	0	0	0	0	0	0				0				0

Bit(s)	Mnemonic	Name	Description
15:12		sw_peri_mo_awcache	**sw_peri_cci_awcache**
11:8		sw_peri_mo_arcache	**sw_peri_cci_arcache**
4		sw_mfg_cache_en	**sw_mfg_cci_cache_force_on** 0: Disable 1: Enable
0		sw_peri_cache_en	**sw_peri_cci_cache_force_on** 0: Disable 1: Enable

10001F08 MISC_CONFIG SW CCI Arcache Configure Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	misc_config_ao											md2_mpll_autok_mux_sel	tdpll_mux_sel	ltepll_mux_sel	md2_416m_ck_mux_sel	md2_26m_ck_sel
Type	RW											RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	misc_config									apc2_mux_sel	apc1_mux_sel	lte_bbrx_mux_sel	td_bbrx_mux_sel	conn_top2_test_mem_pd	conn_top1_test_mem_pd	conn_top2_test_pwr_on
Type	RW									RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:21		misc_config_ao	**misc_config_ao**
20		md2_mpll_autok_mux_sel	**md2_mpll_autok_mux_sel** 0: MDLITE mpll autok from ltepll 1: MDLITE mpll autok from tdpll
19		tdpll_mux_sel	**tdpll_mux_sel** 0: tdpll controlled by MD 1: tdpll controlled by MDLITE
18		ltepll_mux_sel	**ltepll_mux_sel** 0: ltepll controlled by MD 1: ltepll controlled by MDLITE
17		md2_416m_ck_mux_sel	**md2_416m_ck_mux_sel** 0: MDLITE 416M from ltepll 1: MDLITE 416M from tdpll
16		md2_26m_ck_sel	**md2_26m_ck_sel** 0: MDLITE 26M from ltepll

Bit(s)	Mnemonic	Name	Description
			1: MDLITE 26M from tdpll
15:7		misc_config	**misc_config**
6		apc2_mux_sel	**apc2_mux_sel** 0: APC2 controlled by MD 1: APC2 controlled by MDLITE
5		apc1_mux_sel	**apc1_mux_sel** 0: APC1 controlled by MD 1: APC1 controlled by MDLITE
4		lte_bbrx_mux_s el	**lte_bbrx_mux_sel** 0: LTE_BBRX controlled by MD 1: LTE_BBRX controlled by MDLITE
3		td_bbrx_mux_se l	**td_bbrx_mux_sel** 0: LTE_BBRX controlled by MD 1: LTE_BBRX controlled by MDLITE
2		conn_top2_test _mem_pd	**conn_top2_test_mem_pd**
1		conn_top1_test _mem_pd	**conn_top1_test_mem_pd**
0		conn_top2_test _pwr_on	**conn_top2_test_pwr_on**

10001F0C SPM_WAKEUP_EVENT_EN **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_spm_wakeup_event_en															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
15:0		reg_spm_wakeup _event_en	spm_wakeup_event_en

10001F10 SPM_WAKEUP_EVENT_STA **0000001C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	spm_wakeup_event_sta															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
15:0		spm_wakeup_eve nt_sta	spm_wakeup_event_sta

Bit(s)	Mnemonic	Name	Description

10001F14 GCPU_SEC_CON **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													gcpu_lock_ao			gcpu_init_ao
Type													RW			RW
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:1		gcpu_lock_ao	
0		gcpu_init_ao	

10001F18 INFRA_MISC2 **00010063**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	mmsys_cg_gated_mask	mmsys_apb_idle_mask		emi_apb_rx_cg_mask	emi_mpu_apb_rx_cg_mask	spm_apb_rx_cg_mask	pmic_apb_rx_cg_mask	dvfs_proc1_apb_rx_cg_mask	dvfs_proc0_apb_rx_cg_mask	md32_apb_rx_cg_mask					reg_cldma_ap2ap_wakeup_event	cldma_ap_ip_busy_mask
Type	RW	RW		RW	RW	RW	RW	RW	RW	RW					RW	RW
Reset	0	0		0	0	0	0	0	0	0					0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									reg_srcclk_settle							
Type									RW							
Reset									0	1	1	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31		mmsys_cg_gated_mask	
30		mmsys_apb_idle_mask	
28		emi_apb_rx_cg_ mask	Enables emi_async_apb_cg
27		emi_mpu_apb_rx_cg_mask	Enables emi_mpu_async_apb_cg
26		spm_apb_rx_cg_ mask	Enables spm_async_apb_cg
25		pmic_apb_rx_cg_mask	Enables pmic_async_apb_cg
24		dvfs_proc1_apb_rx_cg_mask	
23		dvfs_proc0_apb_rx_cg_mask	
22		md32_apb_rx_cg_mask	
17		reg_cldma_ap2a	

Bit(s)	Mnemonic	Name	Description
16		p_wakeup_event cldma_ap_ip_bu sy_mask	
7:0		reg_srcclk_set tle	

10001800 SRAMROM_BOOT_ADDR SRAMROM Boot Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_b_addr															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_b_addr															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		sramrom_b_addr	SRAMROM power-down jump address register

10001804 SRAMROM_SEC_CTRL SRAMROM Secure Control Register 40000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_sw_rom_pd	sw_dfd_disable		sramrom_sec_addr_en	sramrom_sec1_set3			sramrom_sec1_set2			sramrom_sec1_set1			sramrom_sec1_set0		
Type	RW	RW		RW	RW			RW			RW			RW		
Reset	0	1		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					sramrom_seco_set3			sramrom_seco_set2			sramrom_seoc_set1			sramrom_seco_seto		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		sramrom_sw_rom _pd	**SRAMROM software power-down control register** 0: Does not power down 1: Power down
30		sw_dfd_disable	**Controls DFD disable by security SW** Only both efuse bit and this register are high will DFD feature be disabled. 0: Enable DFD 1: Disable DFD
28		sramrom_sec_ad dr_en	**SRAMROM Region 1 enable register** 0: Disable Region 1 protection 1: Enable Region 1 protection and based on Region 1's security setting
27:25		sramrom_sec1_s et3	**Region 1 security setting for transactions from Domain 3** 000: S R/W, NS R/W 001: S R/W, NS block

Bit(s)	Mnemonic	Name	Description
			010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block
24:22		sramrom_sec1_s et2	**Region 1 Security setting for transactions from domain 2** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block
21:19		sramrom_sec1_s et1	**Region 1 Security setting for transactions from domain 1** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block
18:16		sramrom_sec1_s et0	**Region 1 Security setting for transactions from domain 0** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block
11:9		sramrom_sec0_s et3	**Region 0 security setting for transactions from Domain 3** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block
8:6		sramrom_sec0_s et2	**Region 0 security setting for transactions from Domain 2** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block

Bit(s)	Mnemonic	Name	Description
5:3		sramrom_se0c_s et1	**Region 0 security setting for transactions from Domain 1** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block
2:0		sramrom_sec0_s et0	**Region 0 security setting for transactions from Domain 0** 000: S R/W, NS R/W 001: S R/W, NS block 010: S R/W, NS RO 011: S R/W, NS WO 100: S RO, NS RO 101: S block, NS block 110: S block, NS block 111: S block, NS block

10001808 SRAMROM_SEC_ADDR **SRAMROM Region Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															sram rom_ sec_ addr	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sram rom_ sec_ addr															
Type	RW															
Reset	0	0	0	0	0	0										

Bit(s)	Mnemonic	Name	Description
17:10		sramrom_sec_ad dr	**Partitions internal SRAM into two regions** Region 0 is from 0x0010_0000 to 0x001X_XX00. Region 1 is from 0x001X_XX00 to 0x0012_FFFF. SRAMROM_SEC_ADDR can specify address[17:10].

1000180C SRAMROM_FPC_BOOT_ADDR **SRAMROM FPC Boot Address Register** **00100000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_fpc_b_addr															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_fpc_b_addr															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		sramrom_fpc_b_ addr	**Specifies jump address of CPU when in FPC mode** Can only be written when unlocked.

10001810 SRAMROM_FPC_BOOT_CON SRAMROM FPC Boot Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_fpc_key															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_fpc_key															sramrom_fpc_b_addr_en
Type	WO															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Mnemonic	Name	Description
31:8		sramrom_fpc_ke y	**Stores magic key for enabling FPC bootstrap function** Enter 24'h34AE8C to unlock the function.
0		sramrom_fpc_b_ addr_en	**When this register is set to 1, the jump address specified in sramrom_fpc_boot_addr will take effect.** Can only be written when unlocked.

10001880 MD1_SBC_KEY0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md1_sbc_key															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md1_sbc_key															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		md1_sbc_key	

10001884 MD1_SBC_KEY1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md1_sbc_key1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	md1_sbc_key1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		md1_sbc_key1	

10001888 MD1_SBC_KEY2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md1_sbc_key2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md1_sbc_key2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		md1_sbc_key2	

1000188C MD1_SBC_KEY3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md1_sbc_key3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md1_sbc_key3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		md1_sbc_key3	

10001890 MD1_SBC_KEY4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md1_sbc_key4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md1_sbc_key4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		md1_sbc_key4	

10001894 MD1_SBC_KEY5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md1_sbc_key5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md1_sbc_key5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		md1_sbc_key5	

10001898 MD1_SBC_KEY6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md1_sbc_key6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md1_sbc_key6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		md1_sbc_key6	

1000189C MD1_SBC_KEY7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md1_sbc_key7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md1_sbc_key7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		md1_sbc_key7	

100018A0 MD1_SBC_KEY_LOCK 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																md1_sbc_key_lock
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		md1_sbc_key_lo ck	

10001B00 PLL_ULPOSC_CON0 ULPOSC Register 10000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_o sc_mod		rg_osc_cali							rg_isc_iband						
Type	RW		RW							RW						
Reset	0	0	0	1	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_osc_fband					rg_ftune_en	rg_cp_en	rg_osc_lpf_enb	rg_osc_rsv							
Type	RW					RW	RW	RW	RW							
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:30		rg_osc_mod	
29:24		rg_osc_cali	
22:16		rg_isc_iband	
15:12		rg_osc_fband	
10		rg_ftune_en	
9		rg_cp_en	
8		rg_osc_lpf_enb	
7:0		rg_osc_rsv	

10001B10 PLL_AUXADC_CON0 AUXADC Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	auxa dc_r sv								auxadc_cono_rsv1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									auxadc_cono_rsvo			auxadc_fs	auxadc_cali			
Type									RW			RW	RW			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		auxadc_rsv	
23:16		auxadc_cono_rs v1	
7:5		auxadc_cono_rs vo	
4		auxadc_fs	

Bit(s)	Mnemonic	Name	Description
3:0		auxadc_cali	

10001F80 INFRA_AO_SEC_CON **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												c2k_map_lock	cldma_map_lock	conn_map_lock	md2_map_lock	md1_map_lock
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												c2k_map_sen	cldma_map_sen	conn_map_sen	md2_map_sen	md1_map_sen
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20		c2k_map_lock	
19		cldma_map_lock	
18		conn_map_lock	
17		md2_map_lock	
16		md1_map_lock	
4		c2k_map_sen	
3		cldma_map_sen	
2		conn_map_sen	
1		md2_map_sen	
0		md1_map_sen	

10001F84 INFRA_AO_SEC_CG_CON0 **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sw_cgen_sen_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sw_cgen_sen_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		sw_cgen_sen_0	

10001F88 INFRA_AO_SEC_CG_CON1 **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sw_cgen_sen_1															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sw_cgen_sen_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		sw_cgen_sen_1	

10001FE8 INFRA_AO_SEC_CG_CON2 **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sw_cgen_sen_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sw_cgen_sen_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		sw_cgen_sen_2	

10001F8C INFRA_AO_SEC_RST_CON **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sw_rst_sen_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		sw_rst_sen_0	

10001F90 INFRA_AO_SEC_RST_CON1 **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sw_rst_sen_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		sw_rst_sen_1	

10001F94 INFRA_AO_SEC_RST_CON2 **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sw_rst_sen_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		sw_rst_sen_2	

Module name: INFRA_AO_MBIST Base address: (+10001000h)

Address	Name	Width	Register Function
10001190	INFRA_AO_MBIST_DELSEL_MD32	32	INFRA AO DELSEL MD32
10001194	INFRA_AO_MBIST_DELSEL_MD32_1	32	INFRA AO DELSEL MD32 1
10001198	INFRA_AO_MBIST_DELSEL_MD32_2	32	INFRA AO DELSEL MD32 2
1000119C	INFRA_AO_MBIST_DELSEL_MD32_3	32	INFRA AO DELSEL MD32 3
100011A0	INFRA_AO_MBIST_DELSEL	32	INFRA AO MBIST DELSEL
100011A4	INFRA_AO_MBIST_BSEL	32	INFRA AO MBIST BSEL
100011A8	INFRA_AO_MBIST_CFG	32	INFRA AO MBIST CFG
100011AC	INFRA_AO_MBIST_FUSE_SRAMROM	32	INFRA AO MBIST FUSE SRAMROM
100011F0	INFRA_AO_MBIST_FUSE_MON	32	INFRA AO MBIST FUSE MON
100011B4	INFRA_AO_MBIST_HOLDB	32	INFRA AO MBIST HOLDB
100011B8	INFRA_AO_MBIST_MODE	32	INFRA AO MBIST Mode
100011BC	INFRA_AO_MBIST_MON_SEL	32	INFRA AO MBIST MON SEL
100011C0	INFRA_AO_MBIST_RESULT	32	INFRA AO MBIST Result
10001250	INFRA_AO_MBIST_FUSE_SCP_1	32	INFRA AO MBIST FUSE SCP 1
10001254	INFRA_AO_MBIST_FUSE_SCP_2	32	INFRA AO MBIST FUSE SCP 2

10001190 INFRA_AO_MBIST_DELSEL_MD32 INFRA AO DELSEL MD32 AAAAAAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	scp_mad_mem_delsel				md32_mem_delsel_27_0											
Type	RW				RW											
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md32_mem_delsel_27_0															
Type	RW															
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Name	Description
31:28	scp_mad_mem_delsel	
27:0	md32_mem_delsel_27_0	

10001194 INFRA_AO_MBIST_DELSEL_MD32_1 INFRA AO DELSEL MD32 1 0AAAAAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					md32_mem_delsel_55_28											
Type					RW											
Reset					1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md32_mem_delsel_55_28															
Type	RW															
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Name	Description
27:0	md32_mem_delsel_55_28	

10001198 INFRA_AO_MBIST_DELSEL_MD32_2 INFRA AO DELSEL MD32 2 0AAAAAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					md32_mem_delsel_83_56											
Type					RW											
Reset					1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md32_mem_delsel_83_56															
Type	RW															
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Name	Description
27:0	md32_mem_delsel_83_56	

1000119C INFRA_AO_MBIST_DELSEL_MD32_3 INFRA AO DELSEL MD32 3 0AAAAAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					md32_mem_delsel_111_84											
Type					RW											
Reset					1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md32_mem_delsel_111_84															
Type	RW															
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Name	Description
27:0	md32_mem_delsel_111_84	

100011A0 INFRA_AO_MBIST_DELSEL INFRA AO MBIST DELSEL 00AA0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									scpsys_mem_delsel							
Type									RW							
Reset									1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
23:16	scpsys_mem_delsel	

100011A4 INFRA_AO_MBIST_BSEL INFRA AO MBIST BSEL 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													infra_ao_top_mbist_bsel			
Type													RW			
Reset													1	1	1	1

Bit(s)	Name	Description
3:0	infra_ao_top_mbist_bsel	

100011A8 INFRA_AO_M INFRA AO MBIST CFG 00000000

BIST_CFG

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												rg_scp_ram_mbisr_rprst_b	ram_fuse_load		rg_sramrom_ram_mbisr_rprst_b	rg_mbist_rst_b
Type												RW	RW		RW	RW
Reset												0	0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														infra_ao_top_mbist_background		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
20	rg_scp_ram_mbisr_rprst_b	
19	ram_fuse_load	
17	rg_sramrom_ram_mbisr_rprst_b	
16	rg_mbist_rst_b	
2:0	infra_ao_top_mbist_background	

100011AC INFRA_AO_MBIST_FUSE_SRAMROM — **INFRA AO MBIST FUSE SRAMROM** — **0000007F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_ram_mbisr_rp_ok												sramrom_ram_mbisr_rp_fail			
Type	RO												RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_ram_mbisr_rp_fail									sramrom_ram_pre_fuse						
Type	RO									RO						
Reset	0	0	0	0	0	0	0	0		1	1	1	1	1	1	1

Bit(s)	Name	Description
31:20	sramrom_ram_mbisr_rp_ok	
19:8	sramrom_ram_mbisr_rp_fail	
6:0	sramrom_ram_pre_fuse	

100011F0 INFRA_AO_MBIST_FUSE_MON — **INFRA AO MBIST FUSE MON** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			mbist_fuse_mon_sel								mbist_pre_fuse_mon_sel					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mbist_repair_fuse_mon								mbist_repair_pre_fuse_mon							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:24	mbist_fuse_mon_sel	
21:16	mbist_pre_fuse_mon_sel	
15:8	mbist_repair_fuse_mon	
7:0	mbist_repair_pre_fuse_mon	

100011B4 INFRA_AO_MBIST_HOLDB **INFRA AO MBIST HOLDB** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																scpsys_mbist_holdb
Type																RW
Reset																1

Bit(s)	Name	Description
0	scpsys_mbist_holdb	

100011B8 INFRA_AO_MBIST_MODE **INFRA AO MBIST Mode** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	scpsys_mbist_sleep_test	scpsys_mbist_sleep_w	scpsys_mbist_sleep_r	scpsys_mbist_sleep_inv												
Type	RW	RW	RW	RW												
Reset	0	0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														scp_mad_mbist_mode	scpsys_mbist_mode	md32_mbist_mode
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
31	scpsys_mbist_sleep_test	
30	scpsys_mbist_sleep_w	

Bit(s)	Name	Description
29	scpsys_mbist_sleep_r	
28	scpsys_mbist_sleep_inv	
2	scp_mad_mbist_mode	
1	scpsys_mbist_mode	
0	md32_mbist_mode	

100011BC INFRA_AO_MBIST_MON_SEL INFRA AO MBIST MON SEL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												infra_ao_top_mbist_fail_sel				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															infra_ao_top_mbist_done_sel	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
20:16	infra_ao_top_mbist_fail_sel	
1:0	infra_ao_top_mbist_done_sel	

100011C0 INFRA_AO_MBIST_RESULT INFRA AO MBIST Result 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	infra_ao_mbist_debug_mon															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	infra_ao_mbist_debug_mon															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	infra_ao_mbist_debug_mon	

10001250 INFRA_AO_MBIST_FUSE_SCP_1 INFRA AO MBIST FUSE SCP 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	scp_ram_mbisr_rp_ok															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	scp_ram_mbisr_rp_fail															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	scp_ram_mbisr_rp_ok	
15:0	scp_ram_mbisr_rp_fail	

10001254 INFRA_AO_MBIST_FUSE_SCP_2 INFRA AO MBIST FUSE SCP 2 0000007F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										scp_ram_pre_fuse						
Type										RO						
Reset										1	1	1	1	1	1	1

Bit(s)	Name	Description
6:0	scp_ram_pre_fuse	

Module name: infracfg_reg Base address: (+10201000h)

Address	Name	Width	Register Function
10201000	INFRA_TOPAXI_SI0_STA	32	Top AXI Fabric SI0 Control Register
10201008	INFRA_TOPAXI_SI1_STA	32	gce2mmapb
10201004	INFRA_TOPAXI_MI_STA	32	Top AXI Fabric MI Control Register
10201010	INFRA_MCI_SI0_STA	32	MCI Infra MFG SI0 Port Dispatcher SI Signals
10201018	INFRA_MCI_SI2_STA	32	MCI Infra MFG SI2 Port Dispatcher SI Signals
10201040	INFRA_MIPI_ASYNC_APB_STA	32	MIPI CSI and DSI APB Async Timeout Error Address
10201044	INFRA_APMIXEDSYS_ASYNC_APB_STA	32	APMIXEDSYS Async APB Timeout Error Address
10201048	INFRA_EFUSEC_ASYNC_APB_STA	32	Efusec Async APB Timeout Error Address
1020104C	INFRA_BSI_BPI_ASYNC_APB_STA	32	BSI BPI Async APB Timeout Error Address
10201100	INFRA_TOP_DBG_CON0	32	Infra TOP Debug Control 0
10201104	INFRA_TOP_DBG_CON1	32	Infra TOP Debug Control 1

Address	Name	Width	Register Function
10201108	INFRA_TOP_DBG_CON2	32	Infra TOP Debug Control 2
1020110C	INFRA_TOP_DBG_CON3	32	Infra TOP Debug Control 3
10201200	INFRA_SCPSYS_DBG_SEL	32	Infra TOP SCPSYS Debug Select
10201250	MDSYS_INTF_PERMON0	32	MDSYS INTF PREMON 0
10201254	MDSYS_INTF_PERMON1	32	MDSYS INTF PREMON 1
10201258	MDSYS_INTF_PERMON2	32	MDSYS INTF PREMON 2
1020125C	MDSYS_INTF_PERMON3	32	MDSYS INTF PREMON 3
10201260	MDSYS_INTF_PERMON4	32	MDSYS INTF PREMON 4
10201264	MDSYS_INTF_PERMON5	32	MDSYS INTF PREMON 5
10201268	MDSYS_INTF_PERMON6	32	MDSYS INTF PREMON 6
1020126C	MDSYS_INTF_PERMON7	32	MDSYS INTF PREMON 7
10201274	INFRA_TOPAXI_PERMON_0	32	Infra TOPAXI PERMON 0
10201278	INFRA_TOPAXI_PERMON_1	32	Infra TOPAXI PERMON 1
1020127C	INFRA_TOPAXI_PERMON_2	32	Infra TOPAXI PERMON 2
10201280	INFRA_TOPAXI_PERMON_3	32	Infra TOPAXI PERMON 3
10201284	INFRA_TOPAXI_PERMON_4	32	Infra TOPAXI PERMON 4
10201288	INFRA_TOPAXI_PERMON_5	32	Infra TOPAXI PERMON 5
1020128C	INFRA_TOPAXI_PERMON_6	32	Infra TOPAXI PERMON 6
10201290	INFRA_TOPAXI_PERMON_7	32	Infra TOPAXI PERMON 7
10201294	INFRA_TOPAXI_PERMON_8	32	Infra TOPAXI PERMON 8
10201180	INFRA_BUS_IDLE_STA1	32	Infrasys Bus Idle Status Set 0
10201184	INFRA_BUS_IDLE_STA2	32	Infrasys Bus Idle Status Set 1
10201188	INFRA_BUS_IDLE_STA3	32	Infrasys Bus Idle Status Set 2
1020118C	INFRA_BUS_IDLE_STA4	32	Infrasys Bus Idle Status Set 3
10201190	INFRA_BUS_IDLE_STA5	32	Infrasys Bus Idle Status Set 4
102011A0	INFRA_BUS_IDLE_LAT1	32	Infrasys Bus Idle Status LAT 1
102011A4	INFRA_BUS_IDLE_LAT2	32	Infrasys Bus Idle Status LAT 2

Address	Name	Width	Register Function
102011A8	INFRA_BUS_IDLE_LAT3	32	Infrasys Bus Idle Status LAT 3
102011AC	INFRA_BUS_IDLE_LAT4	32	Infrasys Bus Idle Status LAT 4
102011B0	INFRA_BUS_IDLE_LAT5	32	Infrasys Bus Idle Status LAT 5
10201300	INFRA_MD1_BOOT_STA0	32	md1_boot_status[31:0]
10201304	INFRA_MD1_BOOT_STA1	32	md1_boot_status[63:32]
10201310	MD2AP_DUMMY	32	reg_md2ap_dummy
10201314	L2C_INFRA_CTRL	32	l2c_Infra_ctrl

10201000 INFRA_TOPAXI_SI0_STA Top AXI Fabric SI0 Control Register 01000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								topaxi_sio_ctrl_updated								
Type								RU								
Reset								1								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			topaxi_sio_wr_ot_busy	topaxi_sio_rd_ot_busy	topaxi_sio_set_rid_miss	topaxi_sio_set_bid_miss	topaxi_sio_dfslv_set_wirq	topaxi_sio_dfslv_set_rirq	topaxi_sio_r_chnl_sel				topaxi_sio_b_chnl_sel			
Type			RU	RU	RU	RU	RU	RU	RU				RU			
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24		topaxi_sio_ctrl_updated	
13		topaxi_sio_wr_ot_busy	
12		topaxi_sio_rd_ot_busy	
11		topaxi_sio_set_rid_miss	
10		topaxi_sio_set_bid_miss	
9		topaxi_sio_dfslv_set_wirq	
8		topaxi_sio_dfslv_set_rirq	
7:4		topaxi_sio_r_chnl_sel	
3:0		topaxi_sio_b_chnl_sel	

10201008 INFRA_TOPAXI_SI1_STA **gce2mmapb** **01000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								gce2mmapb_ctrl_updated								
Type								RU								
Reset								1								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			gce2mmapb_wr_ot_busy	gce2mmapb_rd_ot_busy	gce2mmapb_set_rid_miss	gce2mmapb_set_bid_miss					gce2mmapb_r_chnl_sel				gce2mmapb_b_chnl_sel	
Type			RU	RU	RU	RU					RU				RU	
Reset			0	0	0	0					0	0			0	0

Bit(s)	Mnemonic	Name	Description
24		gce2mmapb_ctrl_updated	
13		gce2mmapb_wr_ot_busy	
12		gce2mmapb_rd_ot_busy	
11		gce2mmapb_set_rid_miss	
10		gce2mmapb_set_bid_miss	
5:4		gce2mmapb_r_chnl_sel	
1:0		gce2mmapb_b_chnl_sel	

10201004 INFRA_TOPAXI_MI_STA **Top AXI Fabric MI Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													topaxi_mi4_w_busy	topaxi_mi4_r_busy	topaxi_mi4_errmid_set_birq	topaxi_mi4_errmid_set_rirq
Type													RU	RU	RU	RU
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	topaxi_mi3_w_busy	topaxi_mi3_r_busy	topaxi_mi3_errmid_set_birq	topaxi_mi3_errmid_set_rirq	topaxi_mi2_w_busy	topaxi_mi2_r_busy	topaxi_mi2_errmid_set_birq	topaxi_mi2_errmid_set_rirq	topaxi_mi1_w_busy	topaxi_mi1_r_busy	topaxi_mi1_errmid_set_birq	topaxi_mi1_errmid_set_rirq	topaxi_mio_w_busy	topaxi_mio_r_busy	topaxi_mio_errmid_set_birq	topaxi_mio_errmid_set_rirq
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19		topaxi_mi4_w_b usy	
18		topaxi_mi4_r_b usy	
17		topaxi_mi4_err mid_set_birq	
16		topaxi_mi4_err mid_set_rirq	
15		topaxi_mi3_w_b usy	
14		topaxi_mi3_r_b usy	
13		topaxi_mi3_err mid_set_birq	
12		topaxi_mi3_err mid_set_rirq	
11		topaxi_mi2_w_b usy	
10		topaxi_mi2_r_b usy	
9		topaxi_mi2_err mid_set_birq	
8		topaxi_mi2_err mid_set_rirq	
7		topaxi_mi1_w_b usy	
6		topaxi_mi1_r_b usy	
5		topaxi_mi1_err mid_set_birq	
4		topaxi_mi1_err mid_set_rirq	
3		topaxi_mi0_w_b usy	
2		topaxi_mi0_r_b usy	
1		topaxi_mi0_err mid_set_birq	
0		topaxi_mi0_err mid_set_rirq	

10201010 INFRA_MCI_SI0_STA — **MCI Infra MFG SI0 Port Dispatcher SI Signals** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				mci_sio_ctrl_updated				mci_sio_wr_ot_busy				mci_sio_rd_ot_busy		mci_sio_r_chnl_sel		
Type				RU				RU				RU		RU		
Reset				0				0				0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		mci_sio_b_chnl_sel					mci_sio_set_rid_miss	mci_sio_set_bid_miss				mci_sio_dispatcher_idle				mci_sio_cmd_queue_full
Type		RU					RU	RU				RU				RU
Reset		0	0	0			0	0				0				0

Bit(s)	Mnemonic	Name	Description
28		mci_sio_ctrl_u pdated	
24		mci_sio_wr_ot_ busy	
20		mci_sio_rd_ot_ busy	
18:16		mci_sio_r_chnl _sel	
14:12		mci_sio_b_chnl _sel	
9		mci_sio_set_ri d_miss	
8		mci_sio_set_bi d_miss	
4		mci_sio_dispat cher_idle	
0		mci_sio_cmd_qu eue_full	

10201018 INFRA_MCI_SI2_STA — **MCI Infra MFG SI2 Port Dispatcher SI Signals** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				mci_si2_ctrl_updated				mci_si2_wr_ot_busy				mci_si2_rd_ot_busy		mci_si2_r_chnl_sel		
Type				RU				RU				RU		RU		
Reset				0				0				0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		mci_si2_b_chnl_sel					mci_si2_set_rid_miss	mci_si2_set_bid_miss				mci_si2_dispatcher_idle				mci_si2_cmd_queue_full
Type		RU					RU	RU				RU				RU
Reset		0	0	0			0	0				0				0

Bit(s)	Mnemonic	Name	Description
28		mci_si2_ctrl_u pdated	
24		mci_si2_wr_ot_ busy	
20		mci_si2_rd_ot_ busy	
18:16		mci_si2_r_chnl _sel	
14:12		mci_si2_b_chnl _sel	
9		mci_si2_set_ri d_miss	
8		mci_si2_set_bi d_miss	
4		mci_si2_dispat cher_idle	
0		mci_si2_cmd_qu eue_full	

10201040 INFRA_MIPI_ASYNC_APB_STA — **MIPI CSI and DSI APB Async Timeout Error Address** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							mipi_csi_tx_err_a ddr_reg									
Type							RU									
Reset							0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							mipi_dsi_tx_err_addr_reg									
Type							RU									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25:16		mipi_csi_tx_err_addr_reg	
9:0		mipi_dsi_tx_err_addr_reg	

10201044 INFRA_APMIXEDSYS_ASYNC_APB_STA — **APMIXEDSYS Async APB Timeout Error Address** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							apmixedsys_tx_err_addr_reg									
Type							RU									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
9:0		apmixedsys_tx_err_addr_reg	

10201048 INFRA_EFUSEC_ASYNC_APB_STA — **Efusec Async APB Timeout Error Address** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	efusec_tx_err_addr_reg															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		efusec_tx_err_addr_reg	

1020104C INFRA_BSI_BPI_ASYNC_APB_STA — **BSI BPI Async APB Timeout Error Address** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bsi_bpi_tx_err_addr_reg															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		bsi_bpi_tx_err_addr_reg	

10201100 INFRA_TOP_DBG_CON0 Infra TOP Debug Control 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_debug_mon0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		reg_debug_mon0	Debug monitor control register 0

10201104 INFRA_TOP_DBG_CON1 Infra TOP Debug Control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_debug_mon1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		reg_debug_mon1	Debug monitor control register 1

10201108 INFRA_TOP_DBG_CON2 Infra TOP Debug Control 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_debug_mon2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		reg_debug_mon2	Debug monitor control register 2

1020110C INFRA_TOP_DBG_CON3 Infra TOP Debug Control 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_debug_mon3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		reg_debug_mon3	Debug monitor control register 3

10201200 INFRA_SCPSYS_DBG_SEL Infra TOP SCPSYS Debug Select 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	scpsys_dbg_sel															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		scpsys_dbg_sel	

10201250 MDSYS_INTF_PERMON0 MDSYS INTF PREMON 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_mdbus_axi_prf_mon_en							rg_mdbus_mon_sel	rg_mdbus_out_sel					rg_mdbus_r_os_thr		
Type	RW							RW	RW					RW		
Reset	0							0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_mdbus_r_os_thr		rg_mdbus_w_os_thr					rg_mdbus_addr_set_ren	rg_mdbus_addr_set_wen	rg_mdbus_addr_match_dis	rg_mdbus_set2_ren	rg_mdbus_set1_ren	rg_mdbus_set2_wen	rg_mdbus_set1_wen	rg_mdbus_id_match_dis	rg_mdbus_mon_clr
Type	RW		RW					RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		rg_mdbus_axi_prf_mon_en	
24		rg_mdbus_mon_sel	
23:19		rg_mdbus_out_sel	
18:14		rg_mdbus_r_os_thr	
13:9		rg_mdbus_w_os_thr	
8		rg_mdbus_addr_set_ren	
7		rg_mdbus_addr_set_wen	
6		rg_mdbus_addr_match_dis	
5		rg_mdbus_set2_ren	
4		rg_mdbus_set1_ren	
3		rg_mdbus_set2_wen	
2		rg_mdbus_set1_wen	
1		rg_mdbus_id_match_dis	
0		rg_mdbus_mon_clr	

10201254 MDSYS_INTF_PERMON1 MDSYS INTF PREMON 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				rg_mdbus_id_set2												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				rg_mdbus_id_set1												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		rg_mdbus_id_set2	
12:0		rg_mdbus_id_set1	

10201258 MDSYS_INTF_PERMON2 MDSYS INTF PREMON 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				rg_mdbus_id_en2												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				rg_mdbus_id_en1												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		rg_mdbus_id_en 2	
12:0		rg_mdbus_id_en 1	

1020125C MDSYS_INTF_PERMON3 MDSYS INTF PREMON 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_mdbus_addr_start_wset															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_mdbus_addr_start_wset															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		rg_mdbus_addr_ start_wset	

10201260 MDSYS_INTF_PERMON4 MDSYS INTF PREMON 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_mdbus_addr_end_wset															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_mdbus_addr_end_wset															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		rg_mdbus_addr_ end_wset	

10201264 MDSYS_INTF_PERMON5 MDSYS INTF PREMON 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_mdbus_addr_start_rset															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_mdbus_addr_start_rset															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		rg_mdbus_addr_ start_rset	

10201268 MDSYS_INTF_PERMON6 MDSYS INTF PREMON 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_mdbus_addr_end_rset															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_mdbus_addr_end_rset															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		rg_mdbus_addr_ end_rset	

1020126C MDSYS_INTF_PERMON7 MDSYS INTF PREMON 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_mdbus_cyc_thr															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_mdbus_cyc_thr															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		rg_mdbus_cyc_t hr	

10201274 INFRA_TOPAXI_PERMON_ Infra TOPAXI PERMON 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_topaxi_mi_topaxi_si_axi_prf_mon_en								rg_topaxi_mi_topaxi_si_out_sel					rg_topaxi_mi_topaxi_si_r_os_thr		
Type	RW								RW					RW		

Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_topaxi_mi_topaxi_si_r_os_thr		rg_topaxi_mi_topaxi_si_w_os_thr					rg_topaxi_mi_topaxi_si_addr_set_ren	rg_topaxi_mi_topaxi_si_addr_set_wen	rg_topaxi_mi_topaxi_si_addr_match_dis	rg_topaxi_mi_topaxi_si_set2_ren	rg_topaxi_mi_topaxi_si_set1_ren	rg_topaxi_mi_topaxi_si_set2_wen	rg_topaxi_mi_topaxi_si_set1_wen	rg_topaxi_mi_topaxi_si_id_match_dis	rg_topaxi_mi_topaxi_si_mon_clr
Type	RW		RW					RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		rg_topaxi_mi_topaxi_si_axi_prf_mon_en	
23:19		rg_topaxi_mi_topaxi_si_out_s el	
18:14		rg_topaxi_mi_topaxi_si_r_os_ thr	
13:9		rg_topaxi_mi_topaxi_si_w_os_ thr	
8		rg_topaxi_mi_topaxi_si_addr_set_ren	
7		rg_topaxi_mi_topaxi_si_addr_set_wen	
6		rg_topaxi_mi_topaxi_si_addr_match_dis	
5		rg_topaxi_mi_topaxi_si_set2_ ren	
4		rg_topaxi_mi_topaxi_si_set1_ ren	
3		rg_topaxi_mi_topaxi_si_set2_ wen	
2		rg_topaxi_mi_topaxi_si_set1_ wen	
1		rg_topaxi_mi_topaxi_si_id_match_dis	
0		rg_topaxi_mi_topaxi_si_mon_c lr	

10201278 INFRA_TOPAXI_PERMON_1 Infra TOPAXI PERMON 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						rg_topaxi_mi_topaxi_si_id _set2										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						rg_topaxi_mi_topaxi_si_id_set1										

Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26:16		rg_topaxi_mi_topaxi_si_id_en2	
10:0		rg_topaxi_mi_topaxi_si_id_en1	

1020127C INFRA_TOPAXI_PERMON_2 Infra TOPAXI PERMON 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						rg_topaxi_mi_topaxi_si_id_en2										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						rg_topaxi_mi_topaxi_si_id_en1										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26:16		rg_topaxi_mi_topaxi_si_id_en 2	
10:0		rg_topaxi_mi_topaxi_si_id_en 1	

10201280 INFRA_TOPAXI_PERMON_3 Infra TOPAXI PERMON 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_topaxi_mi_topaxi_si_addr_start_wset															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_topaxi_mi_topaxi_si_addr_start_wset															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		rg_topaxi_mi_topaxi_si_addr_start_wset	

10201284 INFRA_TOPAXI_PERMON_4 Infra TOPAXI PERMON 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_topaxi_mi_topaxi_si_addr_end_wset															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_topaxi_mi_topaxi_si_addr_end_wset															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		rg_topaxi_mi_topaxi_si_addr_end_wset	

10201288 INFRA_TOPAXI_PERMON_5 Infra TOPAXI PERMON 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_topaxi_mi_topaxi_si_addr_start_rset															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_topaxi_mi_topaxi_si_addr_start_rset															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		rg_topaxi_mi_topaxi_si_addr_start_rset	

1020128C INFRA_TOPAXI_PERMON_6 Infra TOPAXI PERMON 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_topaxi_mi_topaxi_si_addr_end_rset															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_topaxi_mi_topaxi_si_addr_end_rset															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		rg_topaxi_mi_topaxi_si_addr_end_rset	

10201290 INFRA_TOPAXI_PERMON_7 Infra TOPAXI PERMON 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_topaxi_mi_topaxi_si_cyc_thr															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_topaxi_mi_topaxi_si_cyc_thr															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		rg_topaxi_mi_topaxi_si_cyc_thr	

10201294 INFRA_TOPAXI_PERMON_8 Infra TOPAXI PERMON 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_topaxi_mi_topaxi_si_mon_result															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_topaxi_mi_topaxi_si_mon_result															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		rg_topaxi_mi_topaxi_si_mon_result	

10201180 INFRA_BUS_IDLE_STA1 Infrasys Bus Idle Status Set 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	peri_bus_idle															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	peri_bus_idle															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		peri_bus_idle	

10201184 INFRA_BUS Infrasys Bus Idle Status Set 1 00000000

IDLE_STA2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	peri_bus_idle_async															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	peri_bus_idle_async															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		peri_bus_idle_ async	

10201188 INFRA_BUS_IDLE_STA3 Infrasys Bus Idle Status Set 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	infra_bus_idle															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	infra_bus_idle															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		infra_bus_idle	

1020118C INFRA_BUS_IDLE_STA4 Infrasys Bus Idle Status Set 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	infra_bus_idle_async															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	infra_bus_idle_async															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		infra_bus_idle _async	

10201190 INFRA_BUS_IDLE_STA5 Infrasys Bus Idle Status Set 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	mem_idle_async															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mem_idle_async															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		mem_idle_async	

102011A0 INFRA_BUS_IDLE_LAT1 **Infrasys Bus Idle Status LAT 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	peri_bus_idle_lat															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	peri_bus_idle_lat															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		peri_bus_idle_ lat	

102011A4 INFRA_BUS_IDLE_LAT2 **Infrasys Bus Idle Status LAT 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	peri_bus_idle_async_lat															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	peri_bus_idle_async_lat															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		peri_bus_idle_ async_lat	

102011A8 INFRA_BUS_IDLE_LAT3 **Infrasys Bus Idle Status LAT 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	infra_bus_idle_lat															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	infra_bus_idle_lat															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		infra_bus_idle _lat	

102011AC INFRA_BUS_IDLE_LAT4 Infrasys Bus Idle Status LAT 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	infra_bus_idle_async_lat															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	infra_bus_idle_async_lat															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		infra_bus_idle _async_lat	

102011B0 INFRA_BUS_IDLE_LAT5 Infrasys Bus Idle Status LAT 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	mem_idle_async_lat															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mem_idle_async_lat															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		mem_idle_async _lat	

10201300 INFRA_MD1_BOOT_STA0 md1_boot_status[31:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md1_boot_status															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md1_boot_status															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		md1_boot_statu s	

Bit(s)	Mnemonic	Name	Description

10201304 INFRA_MD1_BOOT_STA1 md1_boot_status[63:32] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md1_boot_status_1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md1_boot_status_1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		md1_boot_statu s_1	

10201310 MD2AP_DUMMY reg_md2ap_dummy 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_md2ap_dummy															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		reg_md2ap_dumm y	

10201314 L2C_INFRA_CTRL l2c_Infra_ctrl 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																re_l2c_infra_sw_reset
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		re_l2c_infra_s w_reset	

Module name: INFRA_MBIST Base address: (+1020d000h)

Address	Name	Width	Register Function
1020D000	INFRA_DELSEL0	32	INFRA DELSEL 0
1020D004	INFRA_DELSEL1	32	INFRA DELSEL 1
1020D008	INFRA_DELSEL2	32	INFRA DELSEL 2
1020D00C	INFRA_DELSEL3	32	INFRA DELSEL 3
1020D010	INFRA_DELSEL4	32	INFRA DELSEL 4
1020D014	INFRA_DELSEL5	32	INFRA DELSEL 5
1020D09C	INFRA_DELSEL6	32	INFRA DELSEL 6
1020D018	INFRA_MBIST_BSEL0	32	INFRA BSEL 0
1020D01C	INFRA_MBIST_BSEL1	32	INFRA BSEL 1
1020D020	INFRA_MBIST_BSEL2	32	INFRA BSEL 2
1020D024	INFRA_MBIST_BSEL3	32	INFRA BSEL 3
1020D028	INFRA_MBIST_GCPUROM_MISR_IN	32	Infra GCPUROM MISR
1020D030	INFRA_MBIST_SRAMROM_MISR_IN0	32	Infra SRAMROM MISR 0
1020D034	INFRA_MBIST_SRAMROM_MISR_IN1	32	Infra SRAMROM MISR 1
1020D038	INFRA_MBIST_SRAMROM_MISR_IN2	32	Infra SRAMROM MISR 2
1020D03C	INFRA_MBIST_SRAMROM_MISR_IN3	32	Infra SRAMROM MISR 3
1020D040	INFRA_MBIST_SRAMROM_MISR_IN4	32	Infra SRAMROM MISR 4
1020D044	INFRA_MBIST_SRAMROM_MISR_IN5	32	Infra SRAMROM MISR 5
1020D048	INFRA_MBIST_BACKGROUND	32	Infra Background
1020D04C	INFRA_MBIST_GCPU_DEBUG	32	Infra GCPU Debug
1020D050	INFRA_MBIST_DEBUG	32	Infra Debug
1020D054	INFRA_MBIST_HOLDB	32	Infra HOLDB
1020D060	INFRA_MBIST_MODE0	32	Infra MBIST Mode 0
1020D064	INFRA_MBIST_MODE1	32	Infra MBIST Mode 1
1020D068	INFRA_MBIST_DONE0	32	Infra MBIST Done 0
1020D06C	INFRA_MBIST_DONE1	32	Infra MBIST Done 1
1020D070	INFRA_MBIST_FAIL0	32	Infra MBIST Fail 0
1020D074	INFRA_MBIST_FAIL1	32	Infra MBIST Fail 1
1020D078	INFRA_MBIST_FAIL2	32	Infra MBIST Fail 2
1020D098	INFRA_MBIST_FA	32	Infra MBIST Fail 3

Address	Name	Width	Register Function
	IL3		
1020D07C	INFRA_MBIST_GCPUROM_CKSUM0	32	Infra GCPUROM Checksum
1020D080	INFRA_MBIST_SRAMROM_CKSUM0	32	Infra SRAMROM Checksum 0
1020D084	INFRA_MBIST_SRAMROM_CKSUM1	32	Infra SRAMROM Checksum 1
1020D088	INFRA_MBIST_SRAMROM_CKSUM2	32	Infra SRAMROM Checksum 2
1020D08C	INFRA_MBIST_SRAMROM_CKSUM3	32	Infra SRAMROM Checksum 3
1020D090	INFRA_MBIST_SRAMROM_CKSUM4	32	Infra SRAMROM Checksum 4
1020D094	INFRA_MBIST_SRAMROM_CKSUM5	32	Infra SRAMROM Checksum 5

1020D000 INFRA_DELSEL0 INFRA DELSEL 0 AAAAAAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	perisys_delsel_31_0															
Type	RW															
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	perisys_delsel_31_0															
Type	RW															
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Name	Description
31:0	perisys_delsel_31_0	

1020D004 INFRA_DELSEL1 INFRA DELSEL 1 2AAAAAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			perisys_delsel_61_32													
Type			RW													
Reset			1	0	1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	perisys_delsel_61_32															
Type	RW															
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Name	Description
29:0	perisys_delsel_61_32	

1020D008 INFRA_DELSEL2 INFRA DELSEL 2 AAAAAAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ccif_md2md_delsel				mm_iommu_delsel											
Type	RW				RW											
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mm_iommu_delsel															
Type	RW															
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Name	Description
31:28	ccif_md2md_delsel	
27:0	mm_iommu_delsel	

1020D00C INFRA_DELSEL3 **INFRA DELSEL 3** **AAAAAAAA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ccif_delsel				ccif1_delsel				peri_iommu_delsel							
Type	RW				RW				RW							
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	peri_iommu_delsel															
Type	RW															
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Name	Description
31:28	ccif_delsel	
27:24	ccif1_delsel	
23:0	peri_iommu_delsel	

1020D010 INFRA_DELSEL4 **INFRA DELSEL 4** **A5154AA5**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	audio_delsel											gce_delsel				gcpu_rom_delsel
Type	RW											RW				RW
Reset	1	0	1	0	0	1	0	1				1	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gcpu_rom_delsel				gcpu_ram_delsel											
Type	RW				RW											
Reset	0	1	0	0	1	0	1	0	1	0	1	0	0	1	0	1

Bit(s)	Name	Description
31:24	audio_delsel	
20:17	gce_delsel	
16:12	gcpu_rom_delsel	
11:0	gcpu_ram_delsel	

1020D014 INFRA_DELSEL **INFRA DELSEL 5** **AAAAA50A**

EL5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	debugtop_dels el				emi_delsel											
Type	RW				RW											
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_rom_delsel2				sramrom_rom_delsel							sramrom_ram_delsel				
Type	RW				RW							RW				
Reset	1	0	1	0	0	1	0	1	0	0		0	1	0	1	0

Bit(s)	Name	Description
31:28	debugtop_delsel	
27:16	emi_delsel	
15:11	sramrom_rom_delsel2	
10:6	sramrom_rom_delsel	
4:0	sramrom_ram_delsel	

1020D09C INFRA_DELSEL6 INFRA DELSEL 6 0AAAAAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					dvfs_proc1_delsel _1				dvfs_proc1_delsel				dvfs_proco_delsel _1			
Type					RW				RW				RW			
Reset					1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dvfs_proco_delsel				anc_md32_mbist_delsel								ssusb_dev_epo_sra m_delsel			
Type	RW				RW								RW			
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Name	Description
27:24	dvfs_proc1_delsel_1	
23:20	dvfs_proc1_delsel	
19:16	dvfs_proco_delsel_1	
15:12	dvfs_proco_delsel	
11:4	anc_md32_mbist_delsel	
3:0	ssusb_dev_epo_sram_delsel	

1020D018 INFRA_MBIST_BSEL0 INFRA BSEL 0 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	infra_bsel_31_0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	infra_bsel_31_0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	infra_bsel_31_0	

Bit(s)	Name	Description

1020D01C INFRA_MBIST_BSEL1 **INFRA BSEL 1** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	infra_bsel_63_32															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	infra_bsel_63_32															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	infra_bsel_63_32	

1020D020 INFRA_MBIST_BSEL2 **INFRA BSEL 2** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	infra_bsel_95_64															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	infra_bsel_95_64															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	infra_bsel_95_64	

1020D024 INFRA_MBIST_BSEL3 **INFRA BSEL 3** **000001FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								infra_bsel_104_96								
Type								RW								
Reset								1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
8:0	infra_bsel_104_96	

1020D028 INFRA_MBIST **Infra GCPUROM MISR** **00000000**

T_GCPUROM_MISR_IN

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	gcpurom_misr_in															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gcpurom_misr_in															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	gcpurom_misr_in	

1020D030 INFRA_MBIST_SRAMROM_MISR_IN0 — Infra SRAMROM MISR 0 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_rom_misr_in_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_rom_misr_in_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	sramrom_rom_misr_in_31_0	

1020D034 INFRA_MBIST_SRAMROM_MISR_IN1 — Infra SRAMROM MISR 1 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_rom_misr_in_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_rom_misr_in_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	sramrom_rom_misr_in_63_32	

1020D038 INFRA_MBIST_SRAMROM_MISR_IN2 — Infra SRAMROM MISR 2 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_rom_misr_in_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_rom_misr_in_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	sramrom_rom_misr_in_95_64	

1020D03C INFRA_MBIST_SRAMROM_MISR_IN3 **Infra SRAMROM MISR 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_rom_misr_in_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_rom_misr_in_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	sramrom_rom_misr_in_127_96	

1020D040 INFRA_MBIST_SRAMROM_MISR_IN4 **Infra SRAMROM MISR 4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_rom_misr_in_159_128															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_rom_misr_in_159_128															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	sramrom_rom_misr_in_159_128	

1020D044 INFRA_MBIST_SRAMROM_MISR_IN5 **Infra SRAMROM MISR 5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	sramrom_rom_misr_in_191_160															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_rom_misr_in_191_160															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	sramrom_rom_misr_in_191_160	

1020D048 INFRA_MBIST_BACKGROUND — Infra Background — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	infra_mbist_background															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														infra_mbist_background_comp		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
31:16	infra_mbist_background	
2:0	infra_mbist_background_comp	

1020D04C INFRA_MBIST_GCPU_DEBUG — Infra GCPU Debug — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gcpu_ram_mbist_sleep_w				gcpu_ram_mbist_sleep_r				gcpu_ram_mbist_sleep_inv				gcpu_ram_mbist_sleep_test			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	gcpu_ram_mbist_sleep_w	
11:8	gcpu_ram_mbist_sleep_r	
7:4	gcpu_ram_mbist_sleep_inv	
3:0	gcpu_ram_mbist_sleep_test	

1020D050 INFRA_MBIST_DEBUG **Infra Debug** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_ram_mbist_sleep_w	sramrom_ram_mbist_sleep_r	sramrom_ram_mbist_sleep_inv	sramrom_ram_mbist_sleep_test				dvfs_proc1_sleep_r	dvfs_proc1_sleep_w	dvfs_proc1_sleep_inv	dvfs_proc1_sleep_test	dvfs_proco_sleep_r	dvfs_proco_sleep_w	dvfs_proco_sleep_inv	dvfs_proco_sleep_test	rg_mbist_rst_b
Type	RW	RW	RW	RW				RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													anc_md32_sleep_r	anc_md32_sleep_w	anc_md32_sleep_inv	anc_md32_sleep_test
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
31	sramrom_ram_mbist_sleep_w	
30	sramrom_ram_mbist_sleep_r	
29	sramrom_ram_mbist_sleep_inv	
28	sramrom_ram_mbist_sleep_test	
24	dvfs_proc1_sleep_r	
23	dvfs_proc1_sleep_w	
22	dvfs_proc1_sleep_inv	
21	dvfs_proc1_sleep_test	
20	dvfs_proco_sleep_r	
19	dvfs_proco_sleep_w	
18	dvfs_proco_sleep_inv	
17	dvfs_proco_sleep_test	
16	rg_mbist_rst_b	
3	anc_md32_sleep_r	
2	anc_md32_sleep_w	
1	anc_md32_sleep_inv	
0	anc_md32_sleep_test	

1020D054 INFRA_MBIST_HOLDB **Infra HOLDB** **0FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					mcusys_dfd_sram_mbist_holdb	dvfs_proc1_mbist_holdb	dvfs_proco_mbist_holdb	anc_md32_mbist_holdb	ccif_md2md_holdb	ccif1_holdb	emi_holdb	audio_holdb	debugtop_holdb	ccif_holdb	gce_holdb	gcpu_rom_holdb
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gcpu_ram_holdb						peri_iommu_h	mm_iommu_hol	perisys_holdb						sramrom_rom_	sramrom_ram_

							oldb	db							holdb	holdb
Type	RW						RW	RW	RW						RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27	mcusys_dfd_sram_mbist_holdb	
26	dvfs_proc1_mbist_holdb	
25	dvfs_proc0_mbist_holdb	
24	anc_md32_mbist_holdb	
23	ccif_md2md_holdb	
22	ccif1_holdb	
21	emi_holdb	
20	audio_holdb	
19	debugtop_holdb	
18	ccif_holdb	
17	gce_holdb	
16	gcpu_rom_holdb	
15:10	gcpu_ram_holdb	
9	peri_iommu_holdb	
8	mm_iommu_holdb	
7:2	perisys_holdb	
1	sramrom_rom_holdb	
0	sramrom_ram_holdb	

1020D060 INFRA_MBIST_MODE0 **Infra MBIST Mode 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				peri_iommu_mbist_mode			audio_mbist_mode									
Type				RW			RW									
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mm_iommu_mbist_mode				perisys_mbist_mode										sramrom_rom_mbist_mode	sramrom_ram_mbist_mode
Type	RW				RW										RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:26	peri_iommu_mbist_mode	
25:16	audio_mbist_mode	
15:12	mm_iommu_mbist_mode	
11:2	perisys_mbist_mode	
1	sramrom_rom_mbist_mode	
0	sramrom_ram_mbist_mode	

1020D064 INFRA_MBIST_MODE1 **Infra MBIST Mode 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																mcusys_dfd_sram_mbist_mode
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dvfs_proc1_mbist_mode	dvfs_proc0_mbist_mode	anc_md32_mbist_mode	ccif_md2md_mbist_mode	ccif1_mbist_mode	gce_mbist_mode	ccif_mbist_mode	debugtop_mbist_mode	emi_mbist_mode	gcpu_rom_mbist_mode	gcpu_ram_mbist_mode					
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	mcusys_dfd_sram_mbist_mode	
15	dvfs_proc1_mbist_mode	
14	dvfs_proc0_mbist_mode	
13	anc_md32_mbist_mode	
12	ccif_md2md_mbist_mode	
11	ccif1_mbist_mode	
10	gce_mbist_mode	
9	ccif_mbist_mode	
8	debugtop_mbist_mode	
7	emi_mbist_mode	
6	gcpu_rom_mbist_mode	
5:0	gcpu_ram_mbist_mode	

1020D068 INFRA_MBIST_DONE0 **Infra MBIST Done 0** **1C000F84**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	debugtop_mbist_done	ccif_mbist_done	emi_mbist_done	peri_iommu_mbist_done			audio_mbist_done									
Type	RO	RO	RO	RO			RO									
Reset	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mm_iommu_mbist_done				perisys_mbist_done										sramrom_ram_mbist_done	sramrom_rom_mbist_done
Type	RO				RO										RO	RO
Reset	0	0	0	0	1	1	1	1	1	0	0	0	0	1	0	0

Bit(s)	Name	Description
31	debugtop_mbist_done	
30	ccif_mbist_done	
29	emi_mbist_done	

Bit(s)	Name	Description
28:26	peri_iommu_mbist_done	
25:16	audio_mbist_done	
15:12	mm_iommu_mbist_done	
11:2	perisys_mbist_done	
1	sramrom_ram_mbist_done	
0	sramrom_rom_mbist_done	

1020D06C INFRA_MBIST_DONE1 **Infra MBIST Done 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												mcusys_dfd_sram_mbist_done	dvfs_proc1_pcmim_mbist_done	dvfs_proco_pcmim_mbist_done	ssusb_mbist_done	
Type												RO	RO	RO	RO	
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ssusb_mbist_done				ccif1_mbist_done	anc_md32_mbist_done	ccif_md2md_mbist_done	infra_mbist_done	gce_mbist_done	gcpu_rom_mbist_done	gcpu_ram_mbist_done					
Type	RO				RO	RO	RO	RO	RO	RO	RO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20	mcusys_dfd_sram_mbist_done	
19	dvfs_proc1_pcmim_mbist_done	
18	dvfs_proco_pcmim_mbist_done	
17:12	ssusb_mbist_done	
11	ccif1_mbist_done	
10	anc_md32_mbist_done	
9	ccif_md2md_mbist_done	
8	infra_mbist_done	
7	gce_mbist_done	
6	gcpu_rom_mbist_done	
5:0	gcpu_ram_mbist_done	

1020D070 INFRA_MBIST_FAIL0 **Infra MBIST Fail 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		peri_iommu_mbist_fail						mm_iommu_mbist_fail							sramrom_rom_mbist_fail	
Type		RO						RO							RO	
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	sramrom_rom_mbist_fail				sramrom_ram_mbist_fail											
Type	RO				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:25	peri_iommu_mbist_fail	
24:18	mm_iommu_mbist_fail	
17:12	sramrom_rom_mbist_fail	
11:0	sramrom_ram_mbist_fail	

1020D074 INFRA_MBIST_FAIL1 Infra MBIST Fail 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	anc_md32_mbist_fail	emi_mbist_fail						gcpu_rom_mbist_fail	gcpu_ram_mbist_fail							perisys_mbist_fail
Type	RO	RO						RO	RO							RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	perisys_mbist_fail															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	anc_md32_mbist_fail	
30:25	emi_mbist_fail	
24	gcpu_rom_mbist_fail	
23:17	gcpu_ram_mbist_fail	
16:0	perisys_mbist_fail	

1020D078 INFRA_MBIST_FAIL2 Infra MBIST Fail 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						dvfs_proc1_pcmim_mbist_fail_1	dvfs_proc1_pcmim_mbist_fail_0	dvfs_proco_pcmim_mbist_fail_1	dvfs_proco_pcmim_mbist_fail_0	ccif_md2md_mbist_fail	ccif1_mbist_fail	infra_mbist_fail	debugtop_mbist_fail	ccif_mbist_fail	gce_mbist_fail	audio_mbist_fail
Type						RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	audio_mbist_fail															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26	dvfs_proc1_pcmim_mbist_fail_1	

Bit(s)	Name	Description
25	dvfs_proc1_pcmim_mbist_fail_0	
24	dvfs_proc0_pcmim_mbist_fail_1	
23	dvfs_proc0_pcmim_mbist_fail_0	
22	ccif_md2md_mbist_fail	
21	ccif1_mbist_fail	
20	infra_mbist_fail	
19	debugtop_mbist_fail	
18	ccif_mbist_fail	
17	gce_mbist_fail	
16:0	audio_mbist_fail	

1020D098 INFRA_MBIST_FAIL3 Infra MBIST Fail 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											mcusys_dfd_sram_mbist_fail					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mcusys_dfd_sram_mbist_fail			ssusb_mbist_fail												
Type	RO			RO												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:13	mcusys_dfd_sram_mbist_fail	
12:0	ssusb_mbist_fail	

1020D07C INFRA_MBIST_GCPUROM_CKSUM0 Infra GCPUROM Checksum 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	gcpurom_misr_cksum															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gcpurom_misr_cksum															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	gcpurom_misr_cksum	

1020D080 INFRA_MBIST_SRAMROM_CKSUM0 Infra SRAMROM Checksum 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_rom_misr_cksum_31_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_rom_misr_cksum_31_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	sramrom_rom_misr_cksum_31_0	

1020D084 INFRA_MBIST_SRAMROM_CKSUM1 **Infra SRAMROM Checksum 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_rom_misr_cksum_63_32															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_rom_misr_cksum_63_32															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	sramrom_rom_misr_cksum_63_32	

1020D088 INFRA_MBIST_SRAMROM_CKSUM2 **Infra SRAMROM Checksum 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_rom_misr_cksum_95_64															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_rom_misr_cksum_95_64															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	sramrom_rom_misr_cksum_95_64	

1020D08C INFRA_MBIST_SRAMROM_CKSUM3 **Infra SRAMROM Checksum 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_rom_misr_cksum_127_96															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_rom_misr_cksum_127_96															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	sramrom_rom_misr_cksum_127_96	

1020D090 INFRA_MBIST_SRAMROM_CKSUM4 **Infra SRAMROM Checksum 4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_rom_misr_cksum_159_128															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_rom_misr_cksum_159_128															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	sramrom_rom_misr_cksum_159_128	

1020D094 INFRA_MBIST_SRAMROM_CKSUM5 **Infra SRAMROM Checksum 5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sramrom_rom_misr_cksum_191_160															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sramrom_rom_misr_cksum_191_160															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	sramrom_rom_misr_cksum_191_160	

Module name: ldoctl Base address: (+10001000h)

Address	Name	Width	Register Function

Address	Name	Width	Register Function
10001F98	CPULDO_CTRL_0	32	CPULDO Control 0
10001F9C	CPULDO_CTRL_1	32	CPULDO Control 1
10001FA0	CPULDO_CTRL_2	32	CPULDO Control 2
10001FA4	CPULDO_CTRL_3	32	CPULDO Control 3
10001FA8	CPULDO_CTRL_4	32	CPULDO Control 4
10001FAC	CPULDO_CTRL_5	32	CPULDO Control 5
10001FB0	CPULDO_CTRL_6	32	CPULDO Control 6
10001FB4	CPULDO_CTRL_7	32	CPULDO Control 7
10001FB8	CPULDO_CTRL_8	32	CPULDO Control 8
10001FBC	GPULDO_CTRL_0	32	GPULDO Control 0
10001FC0	GPULDO_CTRL_1	32	GPULDO Control 1
10001FC4	GPULDO_CTRL_2	32	GPULDO Control 2
10001FC8	GPULDO_CTRL_3	32	GPULDO Control 3
10001FCC	GPULDO_CTRL_4	32	GPULDO Control 4
10001FD0	GPULDO_CTRL_5	32	GPULDO Control 5
10001FD4	GPULDO_CTRL_6	32	GPULDO Control 6
10001FD8	GPULDO_CTRL_7	32	GPULDO Control 7
10001FDC	GPULDO_CTRL_8	32	GPULDO Control 8
10001FE0	GPULDO_CTRL_9	32	GPULDO Control 9
10001FE4	GPULDO_CTRL_10	32	GPULDO Control 10

10001F98 CPULDO_CTRL_0 CPULDO Control 0 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CPULDO_EN_7	RG_CPULDO_EN_6	RG_CPULDO_EN_5	RG_CPULDO_EN_4	RG_CPULDO_EN_3	RG_CPULDO_EN_2	RG_CPULDO_EN_1	RG_CPULDO_EN_0
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
7		RG_CPULDO_EN_7	
6		RG_CPULDO_EN_6	
5		RG_CPULDO_EN_5	
4		RG_CPULDO_EN_4	
3		RG_CPULDO_EN_3	
2		RG_CPULDO_EN_2	
1		RG_CPULDO_EN_1	
0		RG_CPULDO_EN_0	

10001F9C CPULDO_CTRL_1 CPULDO Control 1 09090909

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CPULDO_LP_3	RG_CPULDO_VOSEL_3							RG_CPULDO_LP_2	RG_CPULDO_VOSEL_2			
Type				RW	RW							RW	RW			
Reset				0	1	0	0	1				0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_CPULDO_LP_1	RG_CPULDO_VOSEL_1							RG_CPULDO_LP_0	RG_CPULDO_VOSEL_0			
Type				RW	RW							RW	RW			
Reset				0	1	0	0	1				0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
28		RG_CPULDO_LP_3	
27:24		RG_CPULDO_VOSEL_3	
20		RG_CPULDO_LP_2	
19:16		RG_CPULDO_VOSEL_2	
12		RG_CPULDO_LP_1	
11:8		RG_CPULDO_VOSEL_1	
4		RG_CPULDO_LP_0	
3:0		RG_CPULDO_VOSEL_0	

10001FA0 CPULDO_CTRL_2 **CPULDO Control 2** **09090909**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CPULDO_LP_7	RG_CPULDO_VOSEL_7							RG_CPULDO_LP_6	RG_CPULDO_VOSEL_6			
Type				RW	RW							RW	RW			
Reset				0	1	0	0	1				0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_CPULDO_LP_5	RG_CPULDO_VOSEL_5							RG_CPULDO_LP_4	RG_CPULDO_VOSEL_4			
Type				RW	RW							RW	RW			
Reset				0	1	0	0	1				0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
28		RG_CPULDO_LP_7	
27:24		RG_CPULDO_VOSEL_7	
20		RG_CPULDO_LP_6	
19:16		RG_CPULDO_VOSEL_6	
12		RG_CPULDO_LP_5	
11:8		RG_CPULDO_VOSEL_5	
4		RG_CPULDO_LP_4	

Bit(s)	Mnemonic	Name	Description
3:0		RG_CPULDO_VOSEL_4	

10001FA4 CPULDO_CTRL_3 **CPULDO Control 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CPULDO_CAL_7				RG_CPULDO_CAL_6				RG_CPULDO_CAL_5				RG_CPULDO_CAL_4			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CPULDO_CAL_3				RG_CPULDO_CAL_2				RG_CPULDO_CAL_1				RG_CPULDO_CAL_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		RG_CPULDO_CAL_7	
27:24		RG_CPULDO_CAL_6	
23:20		RG_CPULDO_CAL_5	
19:16		RG_CPULDO_CAL_4	
15:12		RG_CPULDO_CAL_3	
11:8		RG_CPULDO_CAL_2	
7:4		RG_CPULDO_CAL_1	
3:0		RG_CPULDO_CAL_0	

10001FA8 CPULDO_CTRL_4 **CPULDO Control 4** **0000FF00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CPU_LDO_CAL_EN								RG_CPULDO_NDIS_7	RG_CPULDO_NDIS_6	RG_CPULDO_NDIS_5	RG_CPULDO_NDIS_4	RG_CPULDO_NDIS_3	RG_CPULDO_NDIS_2	RG_CPULDO_NDIS_1	RG_CPULDO_NDIS_0
Type	RW								RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CPULDO_STB_7	RG_CPULDO_STB_6	RG_CPULDO_STB_5	RG_CPULDO_STB_4	RG_CPULDO_STB_3	RG_CPULDO_STB_2	RG_CPULDO_STB_1	RG_CPULDO_STB_0	RG_CPULDO_BYPASS_7	RG_CPULDO_BYPASS_6	RG_CPULDO_BYPASS_5	RG_CPULDO_BYPASS_4	RG_CPULDO_BYPASS_3	RG_CPULDO_BYPASS_2	RG_CPULDO_BYPASS_1	RG_CPULDO_BYPASS_0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		CPU_LDO_CAL_EN	
23		RG_CPULDO_NDIS_7	
22		RG_CPULDO_NDIS_6	
21		RG_CPULDO_NDIS_5	
20		RG_CPULDO_NDIS_4	
19		RG_CPULDO_NDIS_3	
18		RG_CPULDO_NDIS_2	
17		RG_CPULDO_NDIS_1	
16		RG_CPULDO_NDIS_0	

Bit(s)	Mnemonic	Name	Description
15		RG_CPULDO_STB_7	
14		RG_CPULDO_STB_6	
13		RG_CPULDO_STB_5	
12		RG_CPULDO_STB_4	
11		RG_CPULDO_STB_3	
10		RG_CPULDO_STB_2	
9		RG_CPULDO_STB_1	
8		RG_CPULDO_STB_0	
7		RG_CPULDO_BYPASS_7	
6		RG_CPULDO_BYPASS_6	
5		RG_CPULDO_BYPASS_5	
4		RG_CPULDO_BYPASS_4	
3		RG_CPULDO_BYPASS_3	
2		RG_CPULDO_BYPASS_2	
1		RG_CPULDO_BYPASS_1	
0		RG_CPULDO_BYPASS_0	

10001FAC CPULDO_CTRL_5 **CPULDO Control 5** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									RG_CPULDO_PROBE_I_EN_7	RG_CPULDO_PROBE_I_EN_6	RG_CPULDO_PROBE_I_EN_5	RG_CPULDO_PROBE_I_EN_4	RG_CPULDO_PROBE_I_EN_3	RG_CPULDO_PROBE_I_EN_2	RG_CPULDO_PROBE_I_EN_1	RG_CPULDO_PROBE_I_EN_0
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CPULDO_PROBE_V_EN_7	RG_CPULDO_PROBE_V_EN_6	RG_CPULDO_PROBE_V_EN_5	RG_CPULDO_PROBE_V_EN_4	RG_CPULDO_PROBE_V_EN_3	RG_CPULDO_PROBE_V_EN_2	RG_CPULDO_PROBE_V_EN_1	RG_CPULDO_PROBE_V_EN_0	RG_CPULDO_PROBE_ENB_7	RG_CPULDO_PROBE_ENB_6	RG_CPULDO_PROBE_ENB_5	RG_CPULDO_PROBE_ENB_4	RG_CPULDO_PROBE_ENB_3	RG_CPULDO_PROBE_ENB_2	RG_CPULDO_PROBE_ENB_1	RG_CPULDO_PROBE_ENB_0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
23		RG_CPULDO_PROBE_I_EN_7	
22		RG_CPULDO_PROBE_I_EN_6	
21		RG_CPULDO_PROBE_I_EN_5	
20		RG_CPULDO_PROBE_I_EN_4	
19		RG_CPULDO_PROBE_I_EN_3	
18		RG_CPULDO_PROB	

Bit(s)	Mnemonic	Name	Description
		E_I_EN_2	
17		RG_CPULDO_PROB E_I_EN_1	
16		RG_CPULDO_PROB E_I_EN_0	
15		RG_CPULDO_PROB E_V_EN_7	
14		RG_CPULDO_PROB E_V_EN_6	
13		RG_CPULDO_PROB E_V_EN_5	
12		RG_CPULDO_PROB E_V_EN_4	
11		RG_CPULDO_PROB E_V_EN_3	
10		RG_CPULDO_PROB E_V_EN_2	
9		RG_CPULDO_PROB E_V_EN_1	
8		RG_CPULDO_PROB E_V_EN_0	
7		RG_CPULDO_PROB E_ENB_7	
6		RG_CPULDO_PROB E_ENB_6	
5		RG_CPULDO_PROB E_ENB_5	
4		RG_CPULDO_PROB E_ENB_4	
3		RG_CPULDO_PROB E_ENB_3	
2		RG_CPULDO_PROB E_ENB_2	
1		RG_CPULDO_PROB E_ENB_1	
0		RG_CPULDO_PROB E_ENB_0	

10001FB0 CPULDO_CTRL_6 **CPULDO Control 6** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CPULDO_RSV_H_7				RG_CPULDO_RSV_H_6				RG_CPULDO_RSV_H_5				RG_CPULDO_RSV_H_4			
Type	RW				RW				RW				RW			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CPULDO_RSV_H_3				RG_CPULDO_RSV_H_2				RG_CPULDO_RSV_H_1				RG_CPULDO_RSV_H_0			
Type	RW				RW				RW				RW			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:28		RG_CPULDO_RSV_H_7	
27:24		RG_CPULDO_RSV_H_6	
23:20		RG_CPULDO_RSV_H_5	
19:16		RG_CPULDO_RSV_H_4	

Bit(s)	Mnemonic	Name	Description
15:12		RG_CPULDO_RSV_H_3	
11:8		RG_CPULDO_RSV_H_2	
7:4		RG_CPULDO_RSV_H_1	
3:0		RG_CPULDO_RSV_H_0	

10001FB4 CPULDO_CTRL_7 **CPULDO Control 7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CPULDO_RSV_M_7				RG_CPULDO_RSV_M_6				RG_CPULDO_RSV_M_5				RG_CPULDO_RSV_M_4			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CPULDO_RSV_M_3				RG_CPULDO_RSV_M_2				RG_CPULDO_RSV_M_1				RG_CPULDO_RSV_M_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		RG_CPULDO_RSV_M_7	
27:24		RG_CPULDO_RSV_M_6	
23:20		RG_CPULDO_RSV_M_5	
19:16		RG_CPULDO_RSV_M_4	
15:12		RG_CPULDO_RSV_M_3	
11:8		RG_CPULDO_RSV_M_2	
7:4		RG_CPULDO_RSV_M_1	
3:0		RG_CPULDO_RSV_M_0	

10001FB8 CPULDO_CTRL_8 **CPULDO Control 8** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CPULDO_RSV_L_7				RG_CPULDO_RSV_L_6				RG_CPULDO_RSV_L_5				RG_CPULDO_RSV_L_4			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CPULDO_RSV_L_3				RG_CPULDO_RSV_L_2				RG_CPULDO_RSV_L_1				RG_CPULDO_RSV_L_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		RG_CPULDO_RSV_L_7	
27:24		RG_CPULDO_RSV_L_6	

Bit(s)	Mnemonic	Name	Description
23:20		RG_CPULDO_RSV_L_5	
19:16		RG_CPULDO_RSV_L_4	
15:12		RG_CPULDO_RSV_L_3	
11:8		RG_CPULDO_RSV_L_2	
7:4		RG_CPULDO_RSV_L_1	
3:0		RG_CPULDO_RSV_L_0	

10001FBC GPULDO_CTRL_0 **GPULDO Control 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_GPULDO_EN_8	RG_GPULDO_EN_7	RG_GPULDO_EN_6	RG_GPULDO_EN_5	RG_GPULDO_EN_4	RG_GPULDO_EN_3	RG_GPULDO_EN_2	RG_GPULDO_EN_1	RG_GPULDO_EN_0
Type								RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8		RG_GPULDO_EN_8	
7		RG_GPULDO_EN_7	
6		RG_GPULDO_EN_6	
5		RG_GPULDO_EN_5	
4		RG_GPULDO_EN_4	
3		RG_GPULDO_EN_3	
2		RG_GPULDO_EN_2	
1		RG_GPULDO_EN_1	
0		RG_GPULDO_EN_0	

10001FC0 GPULDO_CTRL_1 **GPULDO Control 1** **09090909**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_GPULDO_LP_3	RG_GPULDO_VOSEL_3							RG_GPULDO_LP_2	RG_GPULDO_VOSEL_2			
Type				RW	RW							RW	RW			
Reset				0	1	0	0	1				0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_GPULDO_LP_1	RG_GPULDO_VOSEL_1							RG_GPULDO_LP_0	RG_GPULDO_VOSEL_0			
Type				RW	RW							RW	RW			
Reset				0	1	0	0	1				0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
28		RG_GPULDO_LP_3	
27:24		RG_GPULDO_VOSEL_3	
20		RG_GPULDO_LP_2	
19:16		RG_GPULDO_VOSEL_2	
12		RG_GPULDO_LP_1	
11:8		RG_GPULDO_VOSEL_1	
4		RG_GPULDO_LP_0	
3:0		RG_GPULDO_VOSEL_0	

10001FC4 GPULDO_CTRL_2 **GPULDO Control 2** **09090909**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_GPULDO_LP_7	RG_GPULDO_VOSEL_7							RG_GPULDO_LP_6	RG_GPULDO_VOSEL_6			
Type				RW	RW							RW	RW			
Reset				0	1	0	0	1				0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_GPULDO_LP_5	RG_GPULDO_VOSEL_5							RG_GPULDO_LP_4	RG_GPULDO_VOSEL_4			
Type				RW	RW							RW	RW			
Reset				0	1	0	0	1				0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
28		RG_GPULDO_LP_7	
27:24		RG_GPULDO_VOSEL_7	
20		RG_GPULDO_LP_6	
19:16		RG_GPULDO_VOSEL_6	
12		RG_GPULDO_LP_5	
11:8		RG_GPULDO_VOSEL_5	
4		RG_GPULDO_LP_4	
3:0		RG_GPULDO_VOSEL_4	

10001FC8 GPULDO_CTRL_3 **GPULDO Control 3** **00000009**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_GPULD	RG_GPULDO_VOSEL_8			

												O_LP_8				
Type												RW	RW			
Reset												0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
4		RG_GPULDO_LP_8	
3:0		RG_GPULDO_VOSEL_8	

10001FCC GPULDO_CTRL_4 **GPULDO Control 4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_GPULDO_CAL_7				RG_GPULDO_CAL_6				RG_GPULDO_CAL_5				RG_GPULDO_CAL_4			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_GPULDO_CAL_3				RG_GPULDO_CAL_2				RG_GPULDO_CAL_1				RG_GPULDO_CAL_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		RG_GPULDO_CAL_7	
27:24		RG_GPULDO_CAL_6	
23:20		RG_GPULDO_CAL_5	
19:16		RG_GPULDO_CAL_4	
15:12		RG_GPULDO_CAL_3	
11:8		RG_GPULDO_CAL_2	
7:4		RG_GPULDO_CAL_1	
3:0		RG_GPULDO_CAL_0	

10001FD0 GPULDO_CTRL_5 **GPULDO Control 5** **0200FF00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						RG_GPULDO_NDIS_8	RG_GPULDO_STB_8	RG_GPULDO_BYPASS_8	RG_GPULDO_NDIS_7	RG_GPULDO_NDIS_6	RG_GPULDO_NDIS_5	RG_GPULDO_NDIS_4	RG_GPULDO_NDIS_3	RG_GPULDO_NDIS_2	RG_GPULDO_NDIS_1	RG_GPULDO_NDIS_0
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset						0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_GPULDO_STB_7	RG_GPULDO_STB_6	RG_GPULDO_STB_5	RG_GPULDO_STB_4	RG_GPULDO_STB_3	RG_GPULDO_STB_2	RG_GPULDO_STB_1	RG_GPULDO_STB_0	RG_GPULDO_BYPASS_7	RG_GPULDO_BYPASS_6	RG_GPULDO_BYPASS_5	RG_GPULDO_BYPASS_4	RG_GPULDO_BYPASS_3	RG_GPULDO_BYPASS_2	RG_GPULDO_BYPASS_1	RG_GPULDO_BYPASS_0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26		RG_GPULDO_NDIS_8	
25		RG_GPULDO_STB_8	
24		RG_GPULDO_BYPA	

Bit(s)	Mnemonic	Name	Description
		SS_8	
23		RG_GPULDO_NDIS _7	
22		RG_GPULDO_NDIS _6	
21		RG_GPULDO_NDIS _5	
20		RG_GPULDO_NDIS _4	
19		RG_GPULDO_NDIS _3	
18		RG_GPULDO_NDIS _2	
17		RG_GPULDO_NDIS _1	
16		RG_GPULDO_NDIS _0	
15		RG_GPULDO_STB_ 7	
14		RG_GPULDO_STB_ 6	
13		RG_GPULDO_STB_ 5	
12		RG_GPULDO_STB_ 4	
11		RG_GPULDO_STB_ 3	
10		RG_GPULDO_STB_ 2	
9		RG_GPULDO_STB_ 1	
8		RG_GPULDO_STB_ 0	
7		RG_GPULDO_BYPA SS_7	
6		RG_GPULDO_BYPA SS_6	
5		RG_GPULDO_BYPA SS_5	
4		RG_GPULDO_BYPA SS_4	
3		RG_GPULDO_BYPA SS_3	
2		RG_GPULDO_BYPA SS_2	
1		RG_GPULDO_BYPA SS_1	
0		RG_GPULDO_BYPA SS_0	

10001FD4 GPULDO_CTRL_6 **GPULDO Control 6** **010000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						RG_GPULDO_PROBE_IEN_8	RG_GPULDO_PROBE_VEN_8	RG_GPULDO_PROBENB_8	RG_GPULDO_PROBE_IEN_7	RG_GPULDO_PROBE_IEN_6	RG_GPULDO_PROBE_IEN_5	RG_GPULDO_PROBE_IEN_4	RG_GPULDO_PROBE_IEN_3	RG_GPULDO_PROBE_IEN_2	RG_GPULDO_PROBE_IEN_1	RG_GPULDO_PROBE_IEN_0
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset						0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_GPULDO_PROBE_VEN_7	RG_GPULDO_PROBE_VEN_6	RG_GPULDO_PROBE_VEN_5	RG_GPULDO_PROBE_VEN_4	RG_GPULDO_PROBE_VEN_3	RG_GPULDO_PROBE_VEN_2	RG_GPULDO_PROBE_VEN_1	RG_GPULDO_PROBE_VEN_0	RG_GPULDO_PROBENB_7	RG_GPULDO_PROBENB_6	RG_GPULDO_PROBENB_5	RG_GPULDO_PROBENB_4	RG_GPULDO_PROBENB_3	RG_GPULDO_PROBENB_2	RG_GPULDO_PROBENB_1	RG_GPULDO_PROBENB_0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
26		RG_GPULDO_PROB	

Bit(s)	Mnemonic	Name	Description
		E_I_EN_8	
25		RG_GPULDO_PROBE_V_EN_8	
24		RG_GPULDO_PROBE_ENB_8	
23		RG_GPULDO_PROBE_I_EN_7	
22		RG_GPULDO_PROBE_I_EN_6	
21		RG_GPULDO_PROBE_I_EN_5	
20		RG_GPULDO_PROBE_I_EN_4	
19		RG_GPULDO_PROBE_I_EN_3	
18		RG_GPULDO_PROBE_I_EN_2	
17		RG_GPULDO_PROBE_I_EN_1	
16		RG_GPULDO_PROBE_I_EN_0	
15		RG_GPULDO_PROBE_V_EN_7	
14		RG_GPULDO_PROBE_V_EN_6	
13		RG_GPULDO_PROBE_V_EN_5	
12		RG_GPULDO_PROBE_V_EN_4	
11		RG_GPULDO_PROBE_V_EN_3	
10		RG_GPULDO_PROBE_V_EN_2	
9		RG_GPULDO_PROBE_V_EN_1	
8		RG_GPULDO_PROBE_V_EN_0	
7		RG_GPULDO_PROBE_ENB_7	
6		RG_GPULDO_PROBE_ENB_6	
5		RG_GPULDO_PROBE_ENB_5	
4		RG_GPULDO_PROBE_ENB_4	
3		RG_GPULDO_PROBE_ENB_3	
2		RG_GPULDO_PROBE_ENB_2	
1		RG_GPULDO_PROBE_ENB_1	
0		RG_GPULDO_PROBE_ENB_0	

10001FD8 GPULDO_CTRL_7 **GPULDO Control 7** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_GPULDO_RSV_H_7				RG_GPULDO_RSV_H_6				RG_GPULDO_RSV_H_5				RG_GPULDO_RSV_H_4			
Type	RW				RW				RW				RW			

Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_GPULDO_RSV_H_3				RG_GPULDO_RSV_H_2				RG_GPULDO_RSV_H_1				RG_GPULDO_RSV_H_0			
Type	RW				RW				RW				RW			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:28		RG_GPULDO_RSV_H_7	
27:24		RG_GPULDO_RSV_H_6	
23:20		RG_GPULDO_RSV_H_5	
19:16		RG_GPULDO_RSV_H_4	
15:12		RG_GPULDO_RSV_H_3	
11:8		RG_GPULDO_RSV_H_2	
7:4		RG_GPULDO_RSV_H_1	
3:0		RG_GPULDO_RSV_H_0	

10001FDC GPULDO_CTRL_8 **GPULDO Control 8** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_GPULDO_RSV_M_7				RG_GPULDO_RSV_M_6				RG_GPULDO_RSV_M_5				RG_GPULDO_RSV_M_4			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_GPULDO_RSV_M_3				RG_GPULDO_RSV_M_2				RG_GPULDO_RSV_M_1				RG_GPULDO_RSV_M_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		RG_GPULDO_RSV_M_7	
27:24		RG_GPULDO_RSV_M_6	
23:20		RG_GPULDO_RSV_M_5	
19:16		RG_GPULDO_RSV_M_4	
15:12		RG_GPULDO_RSV_M_3	
11:8		RG_GPULDO_RSV_M_2	
7:4		RG_GPULDO_RSV_M_1	
3:0		RG_GPULDO_RSV_M_0	

10001FE0 GPULDO_CTRL_9 **GPULDO Control 9** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_GPULDO_RSV_L_7				RG_GPULDO_RSV_L_6				RG_GPULDO_RSV_L_5				RG_GPULDO_RSV_L_4			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_GPULDO_RSV_L_3				RG_GPULDO_RSV_L_2				RG_GPULDO_RSV_L_1				RG_GPULDO_RSV_L_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		RG_GPULDO_RSV_L_7	
27:24		RG_GPULDO_RSV_L_6	
23:20		RG_GPULDO_RSV_L_5	
19:16		RG_GPULDO_RSV_L_4	
15:12		RG_GPULDO_RSV_L_3	
11:8		RG_GPULDO_RSV_L_2	
7:4		RG_GPULDO_RSV_L_1	
3:0		RG_GPULDO_RSV_L_0	

10001FE4 GPULDO_CTRL_10 **GPULDO Control 10** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPU_LDO_CAL_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_GPULDO_CAL_8				RG_GPULDO_RSV_L_8				RG_GPULDO_RSV_M_8				RG_GPULDO_RSV_H_8			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		GPU_LDO_CAL_EN	
15:12		RG_GPULDO_CAL_8	
11:8		RG_GPULDO_RSV_L_8	
7:4		RG_GPULDO_RSV_M_8	
3:0		RG_GPULDO_RSV_H_8	

1.5 External Memory Interface

Module name: EMI_MPU_REG Base address: (+10200000h)

Address	Name	Width	Register Function
10200160	EMI_MPUA	32	Memory Protection Unit Control Registers A
10200168	EMI_MPUB	32	Memory Protection Unit Control Registers B
10200170	EMI_MPUC	32	Memory Protection Unit Control Registers C
10200178	EMI_MPUD	32	Memory Protection Unit Control Registers D
10200180	EMI_MPUE	32	Memory Protection Unit Control Registers E
10200188	EMI_MPUF	32	Memory Protection Unit Control Registers F
10200190	EMI_MPUG	32	Memory Protection Unit Control Registers G
10200198	EMI_MPUH	32	Memory Protection Unit Control Registers H
102001A0	EMI_MPUI	32	Memory Protection Unit Control Registers I
102001A4	EMI_MPUI_2ND	32	Memory Protection Unit Control Registers I
102001A8	EMI_MPUJ	32	Memory Protection Unit Control Registers I
102001AC	EMI_MPUJ_2ND	32	Memory Protection Unit Control Registers I
102001B0	EMI_MPUK	32	Memory Protection Unit Control Registers I
102001B4	EMI_MPUK_2ND	32	Memory Protection Unit Control Registers I
102001B8	EMI_MPUL	32	Memory Protection Unit Control Registers I
102001BC	EMI_MPUL_2ND	32	Memory Protection Unit Control Registers I
102001C0	EMI_MPUM	32	Memory Protection Unit Control Registers M
102001C8	EMI_MPUN	32	Memory Protection Unit Control Registers N
102001D0	EMI_MPUO	32	Memory Protection Unit Control Registers O
10200200	EMI_MPUU	32	Memory Protection Unit Control Registers U
10200208	EMI_MPUV	32	Memory Protection Unit Control Registers V
10200210	EMI_MPUW	32	Memory Protection Unit Control Registers W
10200218	EMI_MPUX	32	Memory Protection Unit Control Registers X
10200260	EMI_MPUA2	32	Memory Protection Unit Control Registers A
10200268	EMI_MPUB2	32	Memory Protection Unit Control Registers B
10200270	EMI_MPUC2	32	Memory Protection Unit Control Registers C
10200278	EMI_MPUD2	32	Memory Protection Unit Control Registers D
10200280	EMI_MPUE2	32	Memory Protection Unit Control Registers E
10200288	EMI_MPUF2	32	Memory Protection Unit Control Registers F
10200290	EMI_MPUG2	32	Memory Protection Unit Control Registers G
10200298	EMI_MPUH2	32	Memory Protection Unit Control Registers H
102002A0	EMI_MPUI2	32	Memory Protection Unit Control Registers I
102002A4	EMI_MPUI2_2ND	32	Memory Protection Unit Control Registers I
102002A8	EMI_MPUJ2	32	Memory Protection Unit Control Registers I
102002AC	EMI_MPUJ2_2ND	32	Memory Protection Unit Control Registers I
102002B0	EMI_MPUK2	32	Memory Protection Unit Control Registers I
102002B4	EMI_MPUK2_2ND	32	Memory Protection Unit Control Registers I
102002B8	EMI_MPUL2	32	Memory Protection Unit Control Registers I
102002BC	EMI_MPUL2_2ND	32	Memory Protection Unit Control Registers I
102002C0	EMI_MPUM2	32	Memory Protection Unit Control Registers M
102002C8	EMI_MPUN2	32	Memory Protection Unit Control Registers N
102002D0	EMI_MPUO2	32	Memory Protection Unit Control Registers O
10200300	EMI_MPUU2	32	Memory Protection Unit Control Registers U

Address	Name	Width	Register Function
10200360	EMI_MPUA3	32	Memory Protection Unit Control Registers A
10200368	EMI_MPUB3	32	Memory Protection Unit Control Registers B
10200370	EMI_MPUC3	32	Memory Protection Unit Control Registers C
10200378	EMI_MPUD3	32	Memory Protection Unit Control Registers D
10200380	EMI_MPUE3	32	Memory Protection Unit Control Registers E
10200388	EMI_MPUF3	32	Memory Protection Unit Control Registers F
10200390	EMI_MPUG3	32	Memory Protection Unit Control Registers G
10200398	EMI_MPUH3	32	Memory Protection Unit Control Registers H
102003A0	EMI_MPUI3	32	Memory Protection Unit Control Registers I
102003A4	EMI_MPUI3_2ND	32	Memory Protection Unit Control Registers I
102003A8	EMI_MPUJ3	32	Memory Protection Unit Control Registers I
102003AC	EMI_MPUJ3_2ND	32	Memory Protection Unit Control Registers J
102003B0	EMI_MPUK3	32	Memory Protection Unit Control Registers I
102003B4	EMI_MPUK3_2ND	32	Memory Protection Unit Control Registers K
102003B8	EMI_MPUL3	32	Memory Protection Unit Control Registers I
102003BC	EMI_MPUL3_2ND	32	Memory Protection Unit Control Registers L

10200160 EMI_MPUA — Memory Protection Unit Control Registers A — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_0	Memory protection Region 0 start address addr[31:16]
15:0	MPU_STOP_ADDR_0	Memory protection Region 0 stop address addr[31:16]

10200168 EMI_MPUB — Memory Protection Unit Control Registers B — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_1	Memory protection Region 1 start address addr[31:16]
15:0	MPU_STOP_ADDR_1	Memory protection Region 1 stop address addr[31:16]

Bit(s)	Name	Description

10200170 EMI_MPUC **Memory Protection Unit Control Registers C** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_2	Memory protection Region 2 start address addr[31:16]
15:0	MPU_STOP_ADDR_2	Memory protection Region 2 stop address addr[31:16]

10200178 EMI_MPUD **Memory Protection Unit Control Registers D** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_3	Memory protection Region 3 start address addr[31:16]
15:0	MPU_STOP_ADDR_3	Memory protection Region 3 stop address addr[31:16]

10200180 EMI_MPUE **Memory Protection Unit Control Registers E** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_4	Memory protection Region 4 start address addr[31:16]
15:0	MPU_STOP_ADDR_4	Memory protection Region 4 stop address addr[31:16]

10200188 EMI_MPUF **Memory Protection Unit Control Registers F** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_5	Memory protection Region 5 start address addr[31:16]
15:0	MPU_STOP_ADDR_5	Memory protection Region 5 stop address addr[31:16]

10200190 EMI_MPUG **Memory Protection Unit Control Registers G** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_6	Memory protection Region 6 start address addr[31:16]
15:0	MPU_STOP_ADDR_6	Memory protection Region 6 stop address addr[31:16]

10200198 EMI_MPUH **Memory Protection Unit Control Registers H** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_7	Memory protection Region 7 start address addr[31:16]
15:0	MPU_STOP_ADDR_7	Memory protection Region 7 stop address addr[31:16]

102001A0 EMI_MPUI **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	R0_LOCK								R0D7_APC			R0D6_APC			R0D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R0D5_APC	R0D4_APC			R0D3_APC			R0D2_APC			R0D1_APC			R0D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R0_LOCK	**Controls Region 1 Configuration lock** 0: No lock 1: Region 1 and Region 1 control register are unchangeable.
23:21	R0D7_APC	**Same as R0D0_APC**
20:18	R0D6_APC	**Same as R0D0_APC**
17:15	R0D5_APC	**Same as R0D0_APC**
14:12	R0D4_APC	**Same as R0D0_APC**
11:9	R0D3_APC	**Same as R0D0_APC**
8:6	R0D2_APC	**Same as R0D0_APC**
5:3	R0D1_APC	**Same as R0D0_APC**
2:0	R0D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102001A4 EMI_MPUI_2ND **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R4_LOCK								R4D7_APC			R4D6_APC			R4D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R4D5_APC	R4D4_APC			R4D3_APC			R4D2_APC			R4D1_APC			R4D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R4_LOCK	**Controls Region 1 Configuration lock** 0: No lock 1: Region 1 and Region 1 control register are unchangeable.
23:21	R4D7_APC	**Same as R4D0_APC**
20:18	R4D6_APC	**Same as R4D0_APC**
17:15	R4D5_APC	**Same as R4D0_APC**
14:12	R4D4_APC	**Same as R4D0_APC**
11:9	R4D3_APC	**Same as R4D0_APC**
8:6	R4D2_APC	**Same as R4D0_APC**
5:3	R4D1_APC	**Same as R4D0_APC**
2:0	R4D0_APC	000: No protection 001: Only RW for secure access

Bit(s)	Name	Description
		010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102001A8 EMI_MPUJ **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R1_LOCK								R1D7_APC			R1D6_APC			R1D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R1D5_APC	R1D4_APC			R1D3_APC			R1D2_APC			R1D1_APC			R1D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R1_LOCK	**Controls Region 1 Configuration lock** 0: No lock 1: Region 1 and Region 1 control register are unchangeable.
23:21	R1D7_APC	**Same as R1D0_APC**
20:18	R1D6_APC	**Same as R1D0_APC**
17:15	R1D5_APC	**Same as R1D0_APC**
14:12	R1D4_APC	**Same as R1D0_APC**
11:9	R1D3_APC	**Same as R1D0_APC**
8:6	R1D2_APC	**Same as R1D0_APC**
5:3	R1D1_APC	**Same as R1D0_APC**
2:0	R1D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102001AC EMI_MPUJ_2ND **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R5_LOCK								R5D7_APC			R5D6_APC			R5D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R5D5_APC	R5D4_APC			R5D3_APC			R5D2_APC			R5D1_APC			R5D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R5_LOCK	**Controls Region 1 Configuration lock** 0: No lock 1: Region 1 and Region 1 control register are unchangeable.
23:21	R5D7_APC	**Same as R5D0_APC**
20:18	R5D6_APC	**Same as R5D0_APC**
17:15	R5D5_APC	**Same as R5D0_APC**
14:12	R5D4_APC	**Same as R5D0_APC**
11:9	R5D3_APC	**Same as R5D0_APC**
8:6	R5D2_APC	**Same as R5D0_APC**
5:3	R5D1_APC	**Same as R5D0_APC**
2:0	R5D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102001B0 EMI_MPUK **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R2_LOCK								R2D7_APC			R2D6_APC			R2D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R2D5_APC	R2D4_APC			R2D3_APC			R2D2_APC			R2D1_APC			R2D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R2_LOCK	**Controls Region 1 Configuration lock** 0: No lock 1: Region 1 and Region 1 control register are unchangeable.
23:21	R2D7_APC	**Same as R2D0_APC**
20:18	R2D6_APC	**Same as R2D0_APC**
17:15	R2D5_APC	**Same as R2D0_APC**
14:12	R2D4_APC	**Same as R2D0_APC**
11:9	R2D3_APC	**Same as R2D0_APC**
8:6	R2D2_APC	**Same as R2D0_APC**
5:3	R2D1_APC	**Same as R2D0_APC**
2:0	R2D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102001B4 EMI_MPUK_2ND **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R6_LOCK								R6D7_APC			R6D6_APC			R6D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R6D5_APC	R6D4_APC			R6D3_APC			R6D2_APC			R6D1_APC			R6D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R6_LOCK	**Controls Region 1 Configuration lock** 0: No lock 1: Region 1 and Region 1 control register are unchangeable.
23:21	R6D7_APC	**Same as R6D0_APC**
20:18	R6D6_APC	**Same as R6D0_APC**
17:15	R6D5_APC	**Same as R6D0_APC**
14:12	R6D4_APC	**Same as R6D0_APC**
11:9	R6D3_APC	**Same as R6D0_APC**
8:6	R6D2_APC	**Same as R6D0_APC**
5:3	R6D1_APC	**Same as R6D0_APC**
2:0	R6D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102001B8 EMI_MPUL **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R3_LOCK								R3D7_APC			R3D6_APC			R3D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R3D5_APC	R3D4_APC			R3D3_APC			R3D2_APC			R3D1_APC			R3D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R3_LOCK	**Controls Region 1 Configuration lock** 0: No lock 1: Region 1 and Region 1 control register are unchangeable.
23:21	R3D7_APC	**Same as R3D0_APC**
20:18	R3D6_APC	**Same as R3D0_APC**
17:15	R3D5_APC	**Same as R3D0_APC**
14:12	R3D4_APC	**Same as R3D0_APC**
11:9	R3D3_APC	**Same as R3D0_APC**
8:6	R3D2_APC	**Same as R3D0_APC**
5:3	R3D1_APC	**Same as R3D0_APC**
2:0	R3D0_APC	000: No protection

Bit(s)	Name	Description
		001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102001BC EMI_MPUL_2ND **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R7_LOCK								R7D7_APC			R7D6_APC			R7D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R7D5_APC	R7D4_APC			R7D3_APC			R7D2_APC			R7D1_APC			R7D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R7_LOCK	**Controls Region 1 Configuration lock** 0: No lock 1: Region 1 and Region 1 control register are unchangeable.
23:21	R7D7_APC	**Same as R7D0_APC**
20:18	R7D6_APC	**Same as R7D0_APC**
17:15	R7D5_APC	**Same as R7D0_APC**
14:12	R7D4_APC	**Same as R7D0_APC**
11:9	R7D3_APC	**Same as R7D0_APC**
8:6	R7D2_APC	**Same as R7D0_APC**
5:3	R7D1_APC	**Same as R7D0_APC**
2:0	R7D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102001C0 EMI_MPUM **Memory Protection Unit Control Registers M** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D0_LOCK	D0_SEC		D0_REP					D0_MASK_HI							
Type	RW	RW		RW					RW							
Reset	0	0		0					0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D0_MASK_H20						D0_OOR_MASK	APB_VIO_MASK0	D0_MASK							
Type	RW						RW	RW	RW							

Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	D0_LOCK	**Controls Domain 0 violation control register lock access** 0: No lock 1: D0_mask[7:0], D0_SEC, D0_LOCK are not changeable.
30	D0_SEC	**Domain 4 region violation mask** 0001: Set to 1 to mask Region 16 violation to Domain 0 0010: Set to 1 to mask Region 17 violation to Domain 0 0100: Set to 1 to mask Region 18 violation to Domain 0 1000: Set to 1 to mask Region 19 violation to Domain 0
28	D0_REP	**Controls Domain 0 violation response** 0: AXI response OKAY when violation 1: AXI response SLVERR when violation
23:16	D0_MASK_HI	**Domain 0 region violation mask** 0000_0001: Set to 1 to mask Region 8 violation to Domain 0 0000_0010: Set to 1 to mask Region 9 violation to Domain 0 0000_0100: Set to 1 to mask Region 10 violation to Domain 0 0000_1000: Set to 1 to mask Region 11 violation to Domain 0 0001_0000: Set to 1 to mask Region 12 violation to Domain 0 0010_0000: Set to 1 to mask Region 13 violation to Domain 0 0100_0000: Set to 1 to mask Region 14 violation to Domain 0 1000_0000: Set to 1 to mask Region 15 violation to Domain 0
15:12	D0_MASK_H20	**Domain 0 region violation mask** 0001: Set to 1 to mask Region 16 violation to Domain 0 0010: Set to 1 to mask Region 17 violation to Domain 0 0100: Set to 1 to mask Region 18 violation to Domain 0 1000: Set to 1 to mask Region 19 violation to Domain 0
9	D0_OOR_MASK	**Domain 0 out of range mask** 0: Disable mask 1: Enable mask
8	APB_VIO_MASK0	**Domain 0 APB mask**
7:0	D0_MASK	**Domain 0 region violation mask** 0000_0001: Set to 1 to mask Region 0 violation to Domain 0 0000_0010: Set to 1 to mask Region 1 violation to Domain 0 0000_0100: Set to 1 to mask Region 2 violation to Domain 0 0000_1000: Set to 1 to mask Region 3 violation to Domain 0 0001_0000: Set to 1 to mask Region 4 violation to Domain 0 0010_0000: Set to 1 to mask Region 5 violation to Domain 0 0100_0000: Set to 1 to mask Region 6 violation to Domain 0 1000_0000: Set to 1 to mask Region 7 violation to Domain 0

102001C8 EMI_MPUN — Memory Protection Unit Control Registers N — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D1_LOCK	D1_SEC		D1_REP					D1_MASK_HI							
Type	RW	RW		RW					RW							
Reset	0	0		0					0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D1_MASK_H20						D1_OOR_MASK	APB_VIO_MASK1	D1_MASK							
Type	RW						RW	RW	RW							
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	D1_LOCK	**Controls Domain 1 violation control register lock access** 0: No lock 1: D1_mask[7:0], D1_SEC, D1_LOCK are not changeable.
30	D1_SEC	**2**
28	D1_REP	**Controls Domain 1 violation response** 0: AXI response OKAY when violation 1: AXI response SLVERR when violation
23:16	D1_MASK_HI	**Domain 1 region violation mask** 0000_0001: Set to 1 to mask Region 8 violation to Domain 0 0000_0010: Set to 1 to mask Region 9 violation to Domain 0 0000_0100: Set to 1 to mask Region 10 violation to Domain 0 0000_1000: Set to 1 to mask Region 11 violation to Domain 0 0001_0000: Set to 1 to mask Region 12 violation to Domain 0 0010_0000: Set to 1 to mask Region 13 violation to Domain 0 0100_0000: Set to 1 to mask Region 14 violation to Domain 0 1000_0000: Set to 1 to mask Region 15 violation to Domain 0
15:12	D1_MASK_H20	**Domain 1 region violation mask** 0001: Set to 1 to mask Region 16 violation to Domain 1 0010: Set to 1 to mask Region 17 violation to Domain 1 0100: Set to 1 to mask Region 18 violation to Domain 1 1000: Set to 1 to mask Region 19 violation to Domain 1
9	D1_OOR_MASK	**Domain 1 out of range mask** 0: Disable mask 1: Enable mask
8	APB_VIO_MASK1	**Domain 1 APB mask**
7:0	D1_MASK	**Domain 1 region violation mask** 0000_0001: Set to 1 to mask Region 0 violation to Domain 1 0000_0010: Set to 1 to mask Region 1 violation to Domain 1 0000_0100: Set to 1 to mask Region 2 violation to Domain 1 0000_1000: Set to 1 to mask Region 3 violation to Domain 1 0001_0000: Set to 1 to mask Region 4 violation to Domain 1 0010_0000: Set to 1 to mask Region 5 violation to Domain 1 0100_0000: Set to 1 to mask Region 6 violation to Domain 1 1000_0000: Set to 1 to mask Region 7 violation to Domain 1

102001D0 EMI_MPU0 Memory Protection Unit Control Registers 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D2_LOCK	D2_SEC		D2_REP					D2_MASK_HI							
Type	RW	RW		RW					RW							
Reset	0	0		0					0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D2_MASK_H20						D2_OOR_MASK	APB_VIO_MASK2	D2_MASK							
Type	RW						RW	RW	RW							
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	D2_LOCK	**Controls Domain 2 violation control register lock access** 0: No lock

Bit(s)	Name	Description
		1: D2_mask[7:0], D2_SEC, D2_LOCK are not changeable.
30	D2_SEC	**Controls Domain 2 violation control register secure access** Domain 2 violation control register includes EMI_MPUA~EMI_MPUL, EMI_MPUO. 0: Domain 2 violation control register can be accessed in both secure/non-secure mode. 1: Domain 2 violation control register can be accessed in secure mode only.
28	D2_REP	**Controls Domain 2 violation response** 0: AXI response OKAY when violation 1: AXI response SLVERR when violation
23:16	D2_MASK_HI	**Domain 2 region violation mask** 0000_0001: Set to 1 to mask Region 8 violation to Domain 0 0000_0010: Set to 1 to mask Region 9 violation to Domain 0 0000_0100: Set to 1 to mask Region 10 violation to Domain 0 0000_1000: Set to 1 to mask Region 11 violation to Domain 0 0001_0000: Set to 1 to mask Region 12 violation to Domain 0 0010_0000: Set to 1 to mask Region 13 violation to Domain 0 0100_0000: Set to 1 to mask Region 14 violation to Domain 0 1000_0000: Set to 1 to mask Region 15 violation to Domain 0
15:12	D2_MASK_H20	**Domain 2 region violation mask2** 0001: Set to 1 to mask Region 16 violation to Domain 2 0010: Set to 1 to mask Region 17 violation to Domain 2 0100: Set to 1 to mask Region 18 violation to Domain 2 1000: Set to 1 to mask Region 19 violation to Domain
9	D2_OOR_MASK	**Domain 2 out of range mask** 0: Disable mask 1: Enable mask
8	APB_VIO_MASK2	**Domain 2 APB mask**
7:0	D2_MASK	**Domain 2 region violation mask** 0000_0001: Set to 1 to mask Region 0 violation to Domain 2 0000_0010: Set to 1 to mask Region 1 violation to Domain 2 0000_0100: Set to 1 to mask Region 2 violation to Domain 2 0000_1000: Set to 1 to mask Region 3 violation to Domain 2 0001_0000: Set to 1 to mask Region 4 violation to Domain 2 0010_0000: Set to 1 to mask Region 5 violation to Domain 2 0100_0000: Set to 1 to mask Region 6 violation to Domain 2 1000_0000: Set to 1 to mask Region 7 violation to Domain 2

10200200 EMI_MPUU **Memory Protection Unit Control Registers U** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D3_LOCK	D3_SEC		D3_REP					D3_MASK_HI							
Type	RW	RW		RW					RW							
Reset	0	0		0					0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							D3_OOR_MASK	APB_VIO_MASK3	D3_MASK							
Type							RW	RW	RW							
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
31	D3_LOCK	**Controls Domain 3 violation control register lock access** 0: No lock 1: D3_mask[7:0], D3_SEC, D3_LOCK are not changeable.
30	D3_SEC	**Controls Domain 3 violation control register secure access** Domain 3 violation control register includes EMI_MPUA~EMI_MPUL, EMI_MPUU. 0: Domain 3 violation control register can be accessed in both secure/non-secure mode. 1: Domain 3 violation control register can be accessed in secure mode only.
28	D3_REP	**Controls Domain 3 violation response** 0: AXI response OKAY when violation 1: AXI response SLVERR when violation
23:16	D3_MASK_HI	**Domain 3 region violation mask** 0000_0001: Set to 1 to mask Region 8 violation to Domain 0 0000_0010: Set to 1 to mask Region 9 violation to Domain 0 0000_0100: Set to 1 to mask Region 10 violation to Domain 0 0000_1000: Set to 1 to mask Region 11 violation to Domain 0 0001_0000: Set to 1 to mask Region 12 violation to Domain 0 0010_0000: Set to 1 to mask Region 13 violation to Domain 0 0100_0000: Set to 1 to mask Region 14 violation to Domain 0 1000_0000: Set to 1 to mask Region 15 violation to Domain 0
9	D3_OOR_MASK	**Domain 3 out of range mask** 0: Disable mask 1: Enable mask
8	APB_VIO_MASK3	**Domain 3 APB mask**
7:0	D3_MASK	**Domain 3 region violation mask** 0000_0001: Set to 1 to mask Region 0 violation to Domain 3 0000_0010: Set to 1 to mask Region 1 violation to Domain 3 0000_0100: Set to 1 to mask Region 2 violation to Domain 3 0000_1000: Set to 1 to mask Region 3 violation to Domain 3 0001_0000: Set to 1 to mask Region 4 violation to Domain 3 0010_0000: Set to 1 to mask Region 5 violation to Domain 3 0100_0000: Set to 1 to mask Region 6 violation to Domain 3 1000_0000: Set to 1 to mask Region 7 violation to Domain 3

10200208 EMI_MPUV **Memory Protection Unit Control Registers V** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_DBG_CLR		MPU_APB_RD_ABORT	MPU_APB_WR_ABORT				MPU_APB_ABORT								
Type	W1C		RW	RW				RW								
Reset	0		0	0				0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31	MPU_DBG_CLR	**Clears debugging information** 0: No action 1: Clear debugging information
29	MPU_APB_RD_ABORT	**Read violation**

Bit(s)	Name	Description
		0: Abort is not caused by a READ violation. 1: Abort is caused by a READ violation.
28	MPU_APB_WR_ABORT	**Write violation** 0: Abort is not caused by a WRITE violation. 1: Abort is caused by a WRITE violation.
24	MPU_APB_ABORT	**Indicates if APB violation causes the abort** 0: Abort is not caused by a APB violation. 1: Abort is caused by a APB violation.

10200210 EMI_MPUW **Memory Protection Unit Control Registers W** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_ERROR_SECUR													MPU_ERROR_DOM		
Type	RW													RW		
Reset	0													0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_ERROR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MPU_ERROR_SECUR	Violation secure bit
18:16	MPU_ERROR_DOM	Violation domain
15:0	MPU_ERROR_ADDR	Violation address

10200218 EMI_MPUX **Memory Protection Unit Control Registers X** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	APB_VIO_CLR											MPU_VIO_MASK				ABP_VIO
Type	WO											RW				RO
Reset	0											0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MPU_APB_PROT_EN
Type																RW
Reset																1

Bit(s)	Name	Description
31	APB_VIO_CLR	**Clears APB violation**
20	MPU_VIO_MASK	**Masks APB violation**
16	ABP_VIO	0: No APB violation 11: APB violation happens.
0	MPU_APB_PROT_EN	0: No check 1: Check domain permission according to Region APC

Bit(s)	Name	Description

10200260 EMI_MPUA2 Memory Protection Unit Control Registers A 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_8															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_8															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_8	Memory protection Region 8 start address addr[31:16]
15:0	MPU_STOP_ADDR_8	Memory protection Region 8 stop address addr[31:16]

10200268 EMI_MPUB2 Memory Protection Unit Control Registers B 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_9															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_9															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_9	Memory protection Region 9 start address addr[31:16]
15:0	MPU_STOP_ADDR_9	Memory protection Region 9 stop address addr[31:16]

10200270 EMI_MPUC2 Memory Protection Unit Control Registers C 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_10	Memory protection Region 10 start address addr[31:16]
15:0	MPU_STOP_ADDR_10	Memory protection Region 10 stop address addr[31:16]

10200278 EMI_MPUD2 Memory Protection Unit Control Registers D 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_11	Memory protection Region 11 start address addr[31:16]
15:0	MPU_STOP_ADDR_11	Memory protection Region 11 stop address addr[31:16]

10200280 EMI_MPUE2 Memory Protection Unit Control Registers E 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_12	Memory protection Region 12 start address addr[31:16]
15:0	MPU_STOP_ADDR_12	Memory protection Region 12 stop address addr[31:16]

10200288 EMI_MPUF2 Memory Protection Unit Control Registers F 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_13	Memory protection Region 13 start address addr[31:16]
15:0	MPU_STOP_ADDR_13	Memory protection Region 13 stop address addr[31:16]

10200290 EMI_MPUG2 Memory Protection Unit Control Registers G 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	MPU_START_ADDR_14															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_14															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_14	Memory protection Region 14 start address addr[31:16]
15:0	MPU_STOP_ADDR_14	Memory protection Region 14 stop address addr[31:16]

10200298 EMI_MPUH2 Memory Protection Unit Control Registers H 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_15	Memory protection Region 15 start address addr[31:16]
15:0	MPU_STOP_ADDR_15	Memory protection Region 15 stop address addr[31:16]

102002A0 EMI_MPUI2 Memory Protection Unit Control Registers I 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R8_LOCK								R8D7_APC			R8D6_APC			R8D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R8D5_APC	R8D4_APC			R8D3_APC			R8D2_APC			R8D1_APC			R8D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R8_LOCK	**Controls Region 1 Configuration lock** 0: No lock 1: Region 1 and Region 1 control register are unchangeable.
23:21	R8D7_APC	**Same as R8D0_APC**
20:18	R8D6_APC	**Same as R8D0_APC**
17:15	R8D5_APC	**Same as R8D0_APC**
14:12	R8D4_APC	**Same as R8D0_APC**
11:9	R8D3_APC	**Same as R8D0_APC**
8:6	R8D2_APC	**Same as R8D0_APC**
5:3	R8D1_APC	**Same as R8D0_APC**

Bit(s)	Name	Description
2:0	R8D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102002A4 EMI_MPUI2_2ND **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R12_LOCK								R12D7_APC			R12D6_APC			R12D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R12D5_APC	R12D4_APC			R12D3_APC			R12D2_APC			R12D1_APC			R12D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R12_LOCK	**Controls Region 1 Configuration lock** 0: No lock 1: Region 1 and Region 1 control register are unchangeable.
23:21	R12D7_APC	**Same as R12D0_APC**
20:18	R12D6_APC	**Same as R12D0_APC**
17:15	R12D5_APC	**Same as R12D0_APC**
14:12	R12D4_APC	**Same as R12D0_APC**
11:9	R12D3_APC	**Same as R12D0_APC**
8:6	R12D2_APC	**Same as R12D0_APC**
5:3	R12D1_APC	**Same as R12D0_APC**
2:0	R12D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102002A8 EMI_MPUJ2 **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R9_LOCK								R9D7_APC			R9D6_APC			R9D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R9D5_APC	R9D4_APC			R9D3_APC			R9D2_APC			R9D1_APC			R9D0_APC		
Type	RW	RW			RW			RW			RW			RW		

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R9_LOCK	**Controls Region 1 Configuration lock** 0: No lock 1: Region 1 and Region 1 control register are unchangeable.
23:21	R9D7_APC	**Same as R9D0_APC**
20:18	R9D6_APC	**Same as R9D0_APC**
17:15	R9D5_APC	**Same as R9D0_APC**
14:12	R9D4_APC	**Same as R9D0_APC**
11:9	R9D3_APC	**Same as R9D0_APC**
8:6	R9D2_APC	**Same as R9D0_APC**
5:3	R9D1_APC	**Same as R9D0_APC**
2:0	R9D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102002AC EMI_MPUJ2_2ND **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R13_LOCK								R13D7_APC			R13D6_APC			R13D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R13D5_APC	R13D4_APC			R13D3_APC			R13D2_APC			R13D1_APC			R13D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R13_LOCK	**Controls Region 1 Configuration lock** 0: No lock 1: Region 1 and Region 1 control register are unchangeable.
23:21	R13D7_APC	**Same as R13D0_APC**
20:18	R13D6_APC	**Same as R13D0_APC**
17:15	R13D5_APC	**Same as R13D0_APC**
14:12	R13D4_APC	**Same as R13D0_APC**
11:9	R13D3_APC	**Same as R13D0_APC**
8:6	R13D2_APC	**Same as R13D0_APC**
5:3	R13D1_APC	**Same as R13D0_APC**
2:0	R13D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102002B0 EMI_MPUK2 **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R10_LOCK								R10D7_APC			R10D6_APC			R10D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R10D5_APC	R10D4_APC			R10D3_APC			R10D2_APC			R10D1_APC			R10D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R10_LOCK	**Controls Region 1 Configuration lock** 0: No lock 1: Region 1 and Region 1 control register are unchangeable.
23:21	R10D7_APC	**Same as R10D0_APC**
20:18	R10D6_APC	**Same as R10D0_APC**
17:15	R10D5_APC	**Same as R10D0_APC**
14:12	R10D4_APC	**Same as R10D0_APC**
11:9	R10D3_APC	**Same as R10D0_APC**
8:6	R10D2_APC	**Same as R10D0_APC**
5:3	R10D1_APC	**Same as R10D0_APC**
2:0	R10D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102002B4 EMI_MPUK2_2ND **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R14_LOCK								R14D7_APC			R14D6_APC			R14D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R14D5_APC	R14D4_APC			R14D3_APC			R14D2_APC			R14D1_APC			R14D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R14_LOCK	**Controls Region 1 Configuration lock** 0: No lock 1: Region 1 and Region 1 control register are unchangeable.
23:21	R14D7_APC	**Same as R14D0_APC**
20:18	R14D6_APC	**Same as R14D0_APC**
17:15	R14D5_APC	**Same as R14D0_APC**
14:12	R14D4_APC	**Same as R14D0_APC**
11:9	R14D3_APC	**Same as R14D0_APC**

Bit(s)	Name	Description
8:6	R14D2_APC	**Same as R14D0_APC**
5:3	R14D1_APC	**Same as R14D0_APC**
2:0	R14D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102002B8 EMI_MPUL2 **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R11_LOCK								R11D7_APC			R11D6_APC			R11D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R11D5_APC	R11D4_APC			R11D3_APC			R11D2_APC			R11D1_APC			R11D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R11_LOCK	**Controls Region 1 Configuration lock** 0: No lock 1: Region 1 and Region 1 control register are unchangeable.
23:21	R11D7_APC	**Same as R11D0_APC**
20:18	R11D6_APC	**Same as R11D0_APC**
17:15	R11D5_APC	**Same as R11D0_APC**
14:12	R11D4_APC	**Same as R11D0_APC**
11:9	R11D3_APC	**Same as R11D0_APC**
8:6	R11D2_APC	**Same as R11D0_APC**
5:3	R11D1_APC	**Same as R11D0_APC**
2:0	R11D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102002BC EMI_MPUL2_2ND **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R15_LOCK								R15D7_APC			R15D6_APC			R15D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R15D5_APC	R15D4_APC			R15D3_APC			R15D2_APC			R15D1_APC			R15D0_APC		

Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R15_LOCK	**Controls Region 1 Configuration lock** 0: No lock 1: Region 1 and Region 1 control register are unchangeable.
23:21	R15D7_APC	**Same as R15D0_APC**
20:18	R15D6_APC	**Same as R15D0_APC**
17:15	R15D5_APC	**Same as R15D0_APC**
14:12	R15D4_APC	**Same as R15D0_APC**
11:9	R15D3_APC	**Same as R15D0_APC**
8:6	R15D2_APC	**Same as R15D0_APC**
5:3	R15D1_APC	**Same as R15D0_APC**
2:0	R15D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102002C0 EMI_MPUM2 **Memory Protection Unit Control Registers M** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D4_LOCK	D4_SEC		D4_REP					D4_MASK_HI							
Type	RW	RW		RW					RW							
Reset	0	0		0					0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D4_MASK_H20						D4_OOR_MASK	APB_VIO_MASK0	D4_MASK							
Type	RW						RW	RW	RW							
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	D4_LOCK	**Controls Domain 4 violation control register lock access** 0: No lock 1: D4_mask[7:0], D4_SEC, D4_LOCK are not changeable.
30	D4_SEC	**Controls Domain 4 violation control register secure access** Domain 4 violation control register includes EMI_MPUA2~EMI_MPUL2, EMI_MPUM2. 0: Domain 4 violation control register can be accessed in secure/non-secure mode. 1: Domain 4 violation control register can be accessed in secure mode only.
28	D4_REP	**Controls Domain 4 violation response** 0: AXI response OKAY when violation 1: AXI response SLVERR when violation
23:16	D4_MASK_HI	**Domain 4 region violation mask** 0000_0001: Set to 1 to mask Region 8 violation to Domain 4 0000_0010: Set to 1 to mask Region 9 violation to Domain 4 0000_0100: Set to 1 to mask Region 10 violation to Domain 4

Bit(s)	Name	Description
		0000_1000: Set to 1 to mask Region 11 violation to Domain 4 0001_0000: Set to 1 to mask Region 12 violation to Domain 4 0010_0000: Set to 1 to mask Region 13 violation to Domain 4 0100_0000: Set to 1 to mask Region 14 violation to Domain 4 1000_0000: Set to 1 to mask Region 15 violation to Domain 4
15:12	D4_MASK_H20	**Domain 4 region violation mask** 0001: Set to 1 to mask Region 16 violation to Domain 0 0010: Set to 1 to mask Region 17 violation to Domain 0 0100: Set to 1 to mask Region 18 violation to Domain 0 1000: Set to 1 to mask Region 19 violation to Domain 0
9	D4_OOR_MASK	**Domain 4 out of range mask** 0: Disable mask 1: Enable mask
8	APB_VIO_MASK0	**Domain 4 APB mask**
7:0	D4_MASK	**Domain 4 region violation mask** 0000_0001: Set to 1 to mask Region 8 violation to Domain 4 0000_0010: Set to 1 to mask Region 9 violation to Domain 4 0000_0100: Set to 1 to mask Region 10 violation to Domain 4 0000_1000: Set to 1 to mask Region 11 violation to Domain 4 0001_0000: Set to 1 to mask Region 12 violation to Domain 4 0010_0000: Set to 1 to mask Region 13 violation to Domain 4 0100_0000: Set to 1 to mask Region 14 violation to Domain 4 1000_0000: Set to 1 to mask Region 15 violation to Domain 4

102002C8 EMI_MPUN2 **Memory Protection Unit Control Registers N** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D5_LOCK	D5_SEC		D5_REP					D5_MASK_HI							
Type	RW	RW		RW					RW							
Reset	0	0		0					0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D5_MASK_H20						D5_OOR_MASK	APB_VIO_MASK1	D5_MASK							
Type	RW						RW	RW	RW							
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	D5_LOCK	**Controls Domain 5 violation control register lock access** 0: No lock 1: D5_mask[7:0], D5_SEC, D5_LOCK are not changeable.
30	D5_SEC	**Controls Domain 5 violation control register secure access** Domain 5 violation control register includes EMI_MPUA2~EMI_MPUL2, EMI_MPUN2. 0: Domain 5 violation control register can be accessedin both secure/non-secure mode. 1: Domain 5 violation control register can be accessed in secure mode only.
28	D5_REP	**Controls Domain 5 violation response** 0: AXI response OKAY when violation 1: AXI response SLVERR when violation
23:16	D5_MASK_HI	**Domain 5 region violation mask** 0000_0001: Set to 1 to mask Region 8 violation to Domain 4

Bit(s)	Name	Description
		0000_0010: Set to 1 to mask Region 9 violation to Domain 4 0000_0100: Set to 1 to mask Region 90 violation to Domain 4 0000_1000: Set to 1 to mask Region 91 violation to Domain 4 0001_0000: Set to 1 to mask Region 92 violation to Domain 4 0010_0000: Set to 1 to mask Region 93 violation to Domain 4 0100_0000: Set to 1 to mask Region 94 violation to Domain 4 1000_0000: Set to 1 to mask Region 95 violation to Domain 4
15:12	D5_MASK_H20	**Domain 5 region violation mask** 0001: Set to 1 to mask Region 16 violation to Domain 1 0010: Set to 1 to mask Region 17 violation to Domain 1 0100: Set to 1 to mask Region 18 violation to Domain 1 1000: Set to 1 to mask Region 19 violation to Domain 1
9	D5_OOR_MASK	**Domain 5 out of range mask** 0: Disable mask 1: Enable mask
8	APB_VIO_MASK1	**Domain 5 APB mask**
7:0	D5_MASK	**Domain 5 region violation mask** 0000_0001: Set to 1 to mask Region 8 violation to Domain 5 0000_0010: Set to 1 to mask Region 9 violation to Domain 5 0000_0100: Set to 1 to mask Region 10 violation to Domain 5 0000_1000: Set to 1 to mask Region 11 violation to Domain 5 0001_0000: Set to 1 to mask Region 12 violation to Domain 5 0010_0000: Set to 1 to mask Region 13 violation to Domain 5 0100_0000: Set to 1 to mask Region 14 violation to Domain 5 1000_0000: Set to 1 to mask Region 15 violation to Domain 5

102002D0 EMI_MPUO2 **Memory Protection Unit Control Registers 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D6_LOCK	D6_SEC		D6_REP					D6_MASK_HI							
Type	RW	RW		RW					RW							
Reset	0	0		0					0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D6_MASK_H20						D6_OOR_MASK	APB_VIO_MASK2	D6_MASK							
Type	RW						RW	RW	RW							
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	D6_LOCK	**Controls Domain 6 violation control register lock access** 0: No lock 1: D6_mask[7:0], D6_SEC, D6_LOCK are not changeable.
30	D6_SEC	**Controls Domain 6 violation control register secure access** Domain 6 violation control register includes EMI_MPUA2~EMI_MPUL2, EMI_MPUO2. 0: Domain 6 violation control register can be accessed in both secure/non-secure mode. 1: Domain 6 violation control register can be accessed in secure mode only.
28	D6_REP	**Controls Domain 6 violation response** 0: AXI response OKAY when violation 1: AXI response SLVERR when violation

Bit(s)	Name	Description
23:16	D6_MASK_HI	**Domain 6 region violation mask** 0000_0001: Set to 1 to mask Region 8 violation to Domain 4 0000_0010: Set to 1 to mask Region 9 violation to Domain 4 0000_0100: Set to 1 to mask Region 90 violation to Domain 4 0000_1000: Set to 1 to mask Region 91 violation to Domain 4 0001_0000: Set to 1 to mask Region 92 violation to Domain 4 0010_0000: Set to 1 to mask Region 93 violation to Domain 4 0100_0000: Set to 1 to mask Region 94 violation to Domain 4 1000_0000: Set to 1 to mask Region 95 violation to Domain 4
15:12	D6_MASK_H20	**Domain 6 region violation mask** 0001: Set to 1 to mask Region 16 violation to Domain 1 0010: Set to 1 to mask Region 17 violation to Domain 1 0100: Set to 1 to mask Region 18 violation to Domain 1 1000: Set to 1 to mask Region 19 violation to Domain 1
9	D6_OOR_MASK	**Domain 6 out of range mask** 0: Disable mask 1: Enable mask
8	APB_VIO_MASK2	**Domain 6 APB mask**
7:0	D6_MASK	**Domain 6 region violation mask** 0000_0001: Set to 1 to mask Region 8 violation to Domain 6 0000_0010: Set to 1 to mask Region 9 violation to Domain 6 0000_0100: Set to 1 to mask Region 10 violation to Domain 6 0000_1000: Set to 1 to mask Region 11 violation to Domain 6 0001_0000: Set to 1 to mask Region 12 violation to Domain 6 0010_0000: Set to 1 to mask Region 13 violation to Domain 6 0100_0000: Set to 1 to mask Region 14 violation to Domain 6 1000_0000: Set to 1 to mask Region 15 violation to Domain 6

10200300 EMI_MPUU2 **Memory Protection Unit Control Registers U** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D7_LOCK	D7_SEC		D7_REP					D7_MASK_HI							
Type	RW	RW		RW					RW							
Reset	0	0		0					0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D7_MASK_H20						D7_OOR_MASK	APB_VIO_MASK3	D7_MASK							
Type	RW						RW	RW	RW							
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	D7_LOCK	**Controls Domain 7 violation control register lock access** 0: No lock 1: D7_mask[7:0], D7_SEC, D7_LOCK are not changeable.
30	D7_SEC	**Controls Domain 7 violation control register secure access** Domain 7 violation control register includes EMI_MPUA2~EMI_MPUL2, EMI_MPUU2. 0: Domain 7 violation control register can be accessed in both secure/non-secure mode. 1: Domain 7 violation control register can be accessed in secure mode only.
28	D7_REP	**Controls Domain 7 violation response**

Bit(s)	Name	Description
		0: AXI response OKAY when violation 1: AXI response SLVERR when violation
23:16	D7_MASK_HI	**Domain 7 region violation mask** 0000_0001: Set to 1 to mask Region 8 violation to Domain 4 0000_0010: Set to 1 to mask Region 9 violation to Domain 4 0000_0100: Set to 1 to mask Region 10 violation to Domain 4 0000_1000: Set to 1 to mask Region 11 violation to Domain 4 0001_0000: Set to 1 to mask Region 12 violation to Domain 4 0010_0000: Set to 1 to mask Region 13 violation to Domain 4 0100_0000: Set to 1 to mask Region 14 violation to Domain 4 1000_0000: Set to 1 to mask Region 15 violation to Domain 4
15:12	D7_MASK_H20	**Domain 7 region violation mask** 0001: Set to 1 to mask Region 16 violation to Domain 1 0010: Set to 1 to mask Region 17 violation to Domain 1 0100: Set to 1 to mask Region 18 violation to Domain 1 1000: Set to 1 to mask Region 19 violation to Domain 1
9	D7_OOR_MASK	**Domain 7 out of range mask** 0: Disable mask 1: Enable mask
8	APB_VIO_MASK3	**Domain 7 APB mask**
7:0	D7_MASK	**Domain 7 region violation mask** 0000_0001: Set to 1 to mask Region 8 violation to Domain 7 0000_0010: Set to 1 to mask Region 9 violation to Domain 7 0000_0100: Set to 1 to mask Region 10 violation to Domain 7 0000_1000: Set to 1 to mask Region 11 violation to Domain 7 0001_0000: Set to 1 to mask Region 12 violation to Domain 7 0010_0000: Set to 1 to mask Region 13 violation to Domain 7 0100_0000: Set to 1 to mask Region 14 violation to Domain 7 1000_0000: Set to 1 to mask Region 15 violation to Domain 7

10200360 EMI_MPUA3 **Memory Protection Unit Control Registers A** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_16															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_16															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_16	Memory protection Region 16 start address addr[31:16]
15:0	MPU_STOP_ADDR_16	Memory protection Region 16 stop address addr[31:16]

10200368 EMI_MPUB3 **Memory Protection Unit Control Registers B** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_17															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	MPU_STOP_ADDR_17															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_17	Memory protection Region 17 start address addr[31:16]
15:0	MPU_STOP_ADDR_17	Memory protection Region 17 stop address addr[31:16]

10200370 EMI_MPUC3 Memory Protection Unit Control Registers C 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_18															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_18															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_18	Memory protection Region 18 start address addr[31:16]
15:0	MPU_STOP_ADDR_18	Memory protection Region 18 stop address addr[31:16]

10200378 EMI_MPUD3 Memory Protection Unit Control Registers D 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_19															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_19															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_19	Memory protection Region 19 start address addr[31:16]
15:0	MPU_STOP_ADDR_19	Memory protection Region 19 stop address addr[31:16]

10200380 EMI_MPUE3 Memory Protection Unit Control Registers E 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_20															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_20															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_20	Memory protection Region 20 start address addr[31:16]
15:0	MPU_STOP_ADDR_20	Memory protection Region 20 stop address addr[31:16]

10200388 EMI_MPUF3 Memory Protection Unit Control Registers F 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_21															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_21															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_21	Memory protection Region 21 start address addr[31:16]
15:0	MPU_STOP_ADDR_21	Memory protection Region 21 stop address addr[31:16]

10200390 EMI_MPUG3 Memory Protection Unit Control Registers G 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_22															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_22															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_22	Memory protection Region 22 start address addr[31:16]
15:0	MPU_STOP_ADDR_22	Memory protection Region 22 stop address addr[31:16]

10200398 EMI_MPUH3 Memory Protection Unit Control Registers H 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_START_ADDR_23															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_STOP_ADDR_23															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MPU_START_ADDR_23	Memory protection Region 23 start address addr[31:16]

Bit(s)	Name	Description
15:0	MPU_STOP_ADDR_23	Memory protection Region 23 stop address addr[31:16]

102003A0 EMI_MPUI3 **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R16_LOCK								R16D7_APC			R16D6_APC			R16D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R16D5_APC	R16D4_APC			R16D3_APC			R16D2_APC			R16D1_APC			R16D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R16_LOCK	**Controls Region 1 Configuration lock** 0: No lock 1: Region 1 and Region 1 control register are unchangeable.
23:21	R16D7_APC	**Same as R16D0_APC**
20:18	R16D6_APC	**Same as R16D0_APC**
17:15	R16D5_APC	**Same as R16D0_APC**
14:12	R16D4_APC	**Same as R16D0_APC**
11:9	R16D3_APC	**Same as R16D0_APC**
8:6	R16D2_APC	**Same as R16D0_APC**
5:3	R16D1_APC	**Same as R16D0_APC**
2:0	R16D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102003A4 EMI_MPUI3_2ND **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R20_LOCK								R20D7_APC			R20D6_APC			R20D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R20D5_APC	R20D4_APC			R20D3_APC			R20D2_APC			R20D1_APC			R20D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R20_LOCK	**Controls Region 20 Configuration lock** 0: No lock 1: Region 1 and Region 20 control register are unchangeable.

Bit(s)	Name	Description
23:21	R20D7_APC	**Same as R20D0_APC**
20:18	R20D6_APC	**Same as R20D0_APC**
17:15	R20D5_APC	**Same as R20D0_APC**
14:12	R20D4_APC	**Same as R20D0_APC**
11:9	R20D3_APC	**Same as R20D0_APC**
8:6	R20D2_APC	**Same as R20D0_APC**
5:3	R20D1_APC	**Same as R20D0_APC**
2:0	R20D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102003A8 EMI_MPUJ3 **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R17_LOCK								R17D7_APC			R17D6_APC			R17D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R17D5_APC	R17D4_APC			R17D3_APC			R17D2_APC			R17D1_APC			R17D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R17_LOCK	**Controls Region 1 Configuration lock** 0: No lock 1: Region 1 and Region 1 control register are unchangeable.
23:21	R17D7_APC	**Same as R17D0_APC**
20:18	R17D6_APC	**Same as R17D0_APC**
17:15	R17D5_APC	**Same as R17D0_APC**
14:12	R17D4_APC	**Same as R17D0_APC**
11:9	R17D3_APC	**Same as R17D0_APC**
8:6	R17D2_APC	**Same as R17D0_APC**
5:3	R17D1_APC	**Same as R17D0_APC**
2:0	R17D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102003AC EMI_MPUJ3_2ND **Memory Protection Unit Control Registers J** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R21_LOCK								R21D7_APC			R21D6_APC			R21D5_APC	

Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R21D5_APC	R21D4_APC			R21D3_APC			R21D2_APC			R21D1_APC			R21D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R21_LOCK	**Controls Region 20 Configuration lock** 0: No lock 1: Region 1 and Region 20 control register are unchangeable.
23:21	R21D7_APC	**Same as R21D0_APC**
20:18	R21D6_APC	**Same as R21D0_APC**
17:15	R21D5_APC	**Same as R21D0_APC**
14:12	R21D4_APC	**Same as R21D0_APC**
11:9	R21D3_APC	**Same as R21D0_APC**
8:6	R21D2_APC	**Same as R21D0_APC**
5:3	R21D1_APC	**Same as R21D0_APC**
2:0	R21D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102003B0 EMI_MPUK3 **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R18_LOCK								R18D7_APC			R18D6_APC			R18D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R18D5_APC	R18D4_APC			R18D3_APC			R18D2_APC			R18D1_APC			R18D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R18_LOCK	**Controls Region 1 Configuration lock** 0: No lock 1: Region 1 and Region 1 control register are unchangeable.
23:21	R18D7_APC	**Same as R18D0_APC**
20:18	R18D6_APC	**Same as R18D0_APC**
17:15	R18D5_APC	**Same as R18D0_APC**
14:12	R18D4_APC	**Same as R18D0_APC**
11:9	R18D3_APC	**Same as R18D0_APC**
8:6	R18D2_APC	**Same as R18D0_APC**
5:3	R18D1_APC	**Same as R18D0_APC**
2:0	R18D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access

Bit(s)	Name	Description
		011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102003B4 EMI_MPUK3_2ND **Memory Protection Unit Control Registers K** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R22_LOCK								R22D7_APC			R22D6_APC			R22D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R22D5_APC	R22D4_APC			R22D3_APC			R22D2_APC			R22D1_APC			R22D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R22_LOCK	**Controls Region 20 Configuration lock** 0: No lock 1: Region 1 and Region 20 control register are unchangeable.
23:21	R22D7_APC	**Same as R22D0_APC**
20:18	R22D6_APC	**Same as R22D0_APC**
17:15	R22D5_APC	**Same as R22D0_APC**
14:12	R22D4_APC	**Same as R22D0_APC**
11:9	R22D3_APC	**Same as R22D0_APC**
8:6	R22D2_APC	**Same as R22D0_APC**
5:3	R22D1_APC	**Same as R22D0_APC**
2:0	R22D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102003B8 EMI_MPUL3 **Memory Protection Unit Control Registers I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R19_LOCK								R19D7_APC			R19D6_APC			R19D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R19D5_APC	R19D4_APC			R19D3_APC			R19D2_APC			R19D1_APC			R19D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
31	R19_LOCK	**Controls Region 1 Configuration lock** 0: No lock 1: Region 1 and Region 1 control register are unchangeable.
23:21	R19D7_APC	**Same as R19D0_APC**
20:18	R19D6_APC	**Same as R19D0_APC**
17:15	R19D5_APC	**Same as R19D0_APC**
14:12	R19D4_APC	**Same as R19D0_APC**
11:9	R19D3_APC	**Same as R19D0_APC**
8:6	R19D2_APC	**Same as R19D0_APC**
5:3	R19D1_APC	**Same as R19D0_APC**
2:0	R19D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

102003BC EMI_MPUL3_2ND **Memory Protection Unit Control Registers L** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R23_LOCK								R23D7_APC			R23D6_APC			R23D5_APC	
Type	RW								RW			RW			RW	
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R23D5_APC	R23D4_APC			R23D3_APC			R23D2_APC			R23D1_APC			R23D0_APC		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	R23_LOCK	**Controls Region 20 Configuration lock** 0: No lock 1: Region 1 and Region 20 control register are unchangeable.
23:21	R23D7_APC	**Same as R23D0_APC**
20:18	R23D6_APC	**Same as R23D0_APC**
17:15	R23D5_APC	**Same as R23D0_APC**
14:12	R23D4_APC	**Same as R23D0_APC**
11:9	R23D3_APC	**Same as R23D0_APC**
8:6	R23D2_APC	**Same as R23D0_APC**
5:3	R23D1_APC	**Same as R23D0_APC**
2:0	R23D0_APC	000: No protection 001: Only RW for secure access 010: Only RW for secure access and non-secure read access 011: Only RW for secure access and non-secure write access 100: Only read for secure/non-secure 101: Both RW are forbidden. 110: Only security write is forbidden.

Module name: EMI_REG Base address: (+10203000h)

Address	Name	Width	Register Function
10203000	EMI_CONA	32	Address Mapping
10203008	EMI_CONB	32	Data Transfer Overhead for Specific Data Size
10203010	EMI_CONC	32	Data Transfer Overhead for Specific Data Size
10203018	EMI_COND	32	FIFO Status
10203020	EMI_CONE	32	Feature Setting
10203028	EMI_CONF	32	Address Scramble Setting
10203030	EMI_CONG	32	Data Transfer Overhead for Specific Non-36 bytes Alignment Data Size
10203038	EMI_CONH	32	Address Mapping 2
1020303C	EMI_BWST	32	BW Status
10203040	EMI_CONI	32	ISP Configuration
10203048	EMI_CONJ	32	ISP Configuration 1
1020304C	EMI_CONO	32	Address Mapping 2
10203050	EMI_CONK	32	ISP Configuration 2
1020305C	EMI_BWST1	32	Selected Master BW Status
10203060	EMI_CONM	32	MISC
10203078	EMI_DRCT	32	EMI Modem Control Register
102030D0	EMI_TEST0	32	Test Mode 0
102030D8	EMI_TEST1	32	Test Mode 1
102030E0	EMI_TESTA	32	Test Mode A
102030E8	EMI_TESTB	32	Test Mode B
102030F0	EMI_TESTC	32	Test Mode B
102030F8	EMI_TESTD	32	Test Mode D
10203100	EMI_ARBA	32	EMI Bandwidth Filter Control M0/1
10203108	EMI_ARBB	32	EMI Bandwidth Filter Control M1
10203110	EMI_ARBC	32	EMI Bandwidth Filter Control M2
10203118	EMI_ARBD	32	EMI Bandwidth Filter Control M3
10203120	EMI_ARBE	32	EMI Bandwidth Filter Control M4
10203128	EMI_ARBF	32	EMI Bandwidth Filter Control M5
10203130	EMI_ARBG	32	EMI Bandwidth Filter Control M5
10203134	EMI_ARBG_2ND	32	EMI Bandwidth Filter Control GPU_2
10203138	EMI_ARBH	32	EMI Bandwidth Filter Control M5
10203140	EMI_ARBI	32	Filter Priority Encode
10203144	EMI_ARBI_2ND	32	Filter Priority Encode for MD Requirement
10203148	EMI_ARBJ	32	Turn Around Command Number
1020314C	EMI_ARBJ_2ND	32	Turn Around Command Number for MD Requirement
10203150	EMI_ARBK	32	Channel Arbiter Control
10203154	EMI_ARBK_2ND	32	Channel Arbiter Control
10203158	EMI_SLCT	32	EMI Slave Control Registers
102031D8	EMI_MPUP	32	Memory Protection Unit Control Registers P
102031E0	EMI_MPUQ	32	Memory Protection Unit Control Registers Q
102031E8	EMI_MPUR	32	Memory Protection Unit Control Registers R
102031F0	EMI_MPUS	32	Memory Protection Unit Control Registers S
102031F8	EMI_MPUT	32	Memory Protection Unit Control Registers T
10203220	EMI_MPUY	32	Memory Protection Unit Control Registers Y

Address	Name	Width	Register Function
102032D8	EMI_MPUP2	32	Memory Protection Unit Control Registers P
102032E0	EMI_MPUQ2	32	Memory Protection Unit Control Registers Q
102032E8	EMI_MPUR2	32	Memory Protection Unit Control Registers R
10203320	EMI_MPUY2	32	Memory Protection Unit Control Registers Y
10203400	EMI_BMEN	32	EMI Bus Monitor Control Registers
10203404	EMI_BSTP	32	EMI Bus Monitor Auto Stop Count
10203408	EMI_BCNT	32	EMI 3rd Double-word Counter of Selected Masters
10203410	EMI_TACT	32	EMI 4th Double-Word Counter of Selected Masters
10203418	EMI_TSCT	32	EMI 3rd Double-word Counter of Selected Masters
10203420	EMI_WACT	32	EMI 4th Double-Word Counter of Selected Masters
10203428	EMI_WSCT	32	EMI 3rd Double-word Counter of Selected Masters
10203430	EMI_BACT	32	EMI 4th Double-Word Counter of Selected Masters
10203438	EMI_BSCT	32	EMI 3rd Double-word Counter of Selected Masters
10203440	EMI_MSEL	32	EMI 4th Double-Word Counter of Selected Masters
10203448	EMI_TSCT2	32	EMI 4th Double-Word Counter of Selected Masters
10203450	EMI_TSCT3	32	EMI 3rd Double-word Counter of Selected Masters
10203458	EMI_WSCT2	32	EMI 4th Double-Word Counter of Selected Masters
10203460	EMI_WSCT3	32	EMI 3rd Double-word Counter of Selected Masters
10203464	EMI_WSCT4	32	EMI 4th Double-Word Counter of Selected Masters
10203468	EMI_MSEL2	32	EMI Master Selection for 4th and 5th Counters
10203470	EMI_MSEL3	32	EMI Master Selection for 6th and 7th Counters
10203478	EMI_MSEL4	32	EMI Master Selection for 8th and 9th Counters
10203480	EMI_MSEL5	32	EMI Master Selection for 10th and 11th Counters
10203488	EMI_MSEL6	32	EMI Master Selection for 12th and 13th Counters
10203490	EMI_MSEL7	32	EMI Master Selection for 14th and 15th Counters
10203498	EMI_MSEL8	32	EMI Master Selection for 16th and 17th Counters
102034A0	EMI_MSEL9	32	EMI Master Selection for 18th and 19th Counters
102034A8	EMI_MSEL10	32	EMI Master Selection for 20th and 21th Counters
102034B0	EMI_BMID0	32	EMI ID Selection for 1- 2 Transaction Type Counters
102034B4	EMI_BMID1	32	EMI ID Selection for 3- 4 Transaction Type Counters
102034B8	EMI_BMID2	32	EMI ID Selection for 5- 6 Transaction Type Counters
102034BC	EMI_BMID3	32	EMI ID Selection for 7- 8 Transaction Type Counters
102034C0	EMI_BMID4	32	EMI ID Selection for 9- 10 Transaction Type Counters
102034C4	EMI_BMID5	32	EMI ID Selection for 11- 12 Transaction Type Counters
102034C8	EMI_BMID6	32	EMI ID Selection for 13- 14 Transaction Type Counters
102034CC	EMI_BMID7	32	EMI ID Selection for 15- 16 Transaction Type Counters
102034D0	EMI_BMID8	32	EMI ID Selection for 17- 18 Transaction Type Counters
102034D4	EMI_BMID9	32	EMI ID Selection for 19- 20 Transaction Type Counters
102034D8	EMI_BMID10	32	EMI ID Selection for 21 Transaction Type Counters
102034E0	EMI_BMEN1	32	EMI ID Selection Enabling
102034E8	EMI_BMEN2	32	EMI ID Selection Enabling
102034F8	EMI_BMRW0	32	EMI ID Selection High Bit for 1-16 Transaction Type Counters
102034FC	EMI_BMRW1	32	EMI ID Selection High Bit for 1-16 Transaction Type Counters
10203500	EMI_TTYPE1	32	EMI 1st Transaction Type Counter of Selected Masters
10203508	EMI_TTYPE2	32	EMI 2nd Transaction Type Counter of Selected Masters
10203510	EMI_TTYPE3	32	EMI 3rd Transaction Type Counter of Selected Masters

Address	Name	Width	Register Function
10203518	EMI_TTYPE4	32	EMI 4th Transaction Type Counter of Selected Masters
10203520	EMI_TTYPE5	32	EMI 5th Transaction Type Counter of Selected Masters
10203528	EMI_TTYPE6	32	EMI 6th Transaction Type Counter of Selected Masters
10203530	EMI_TTYPE7	32	EMI 7th Transaction Type Counter of Selected Masters
10203538	EMI_TTYPE8	32	EMI 8th Transaction Type Counter of Selected Masters
10203540	EMI_TTYPE9	32	EMI 9th Transaction Type Counter of Selected Masters
10203548	EMI_TTYPE10	32	EMI 10th Transaction Type Counter of Selected Masters
10203550	EMI_TTYPE11	32	EMI 11th Transaction Type Counter of Selected Masters
10203558	EMI_TTYPE12	32	EMI 12th Transaction Type Counter of Selected Masters
10203560	EMI_TTYPE13	32	EMI 13th Transaction Type Counter of Selected Masters
10203568	EMI_TTYPE14	32	EMI 14th Transaction Type Counter of Selected Masters
10203570	EMI_TTYPE15	32	EMI 15th Transaction Type Counter of Selected Masters
10203578	EMI_TTYPE16	32	EMI 16th Transaction Type Counter of Selected Masters
10203580	EMI_TTYPE17	32	EMI 17th Transaction Type Counter of Selected Masters
10203588	EMI_TTYPE18	32	EMI 18th Transaction Type Counter of Selected Masters
10203590	EMI_TTYPE19	32	EMI 19th Transaction Type Counter of Selected Masters
10203598	EMI_TTYPE20	32	EMI 20th Transaction Type Counter of Selected Masters
102035A0	EMI_TTYPE21	32	EMI 21st Transaction Type Counter of Selected Masters
102035C0	EMI_EX_CON	32	Exclusive Monitor Status Control
102035C8	EMI_EX_ST0	32	Exclusive Monitor Status Register 0
102035D0	EMI_EX_ST1	32	Exclusive Monitor Status Register 1
102035D8	EMI_EX_ST2	32	Exclusive Monitor Status Register 2
102035E0	EMI_WP_ADR	32	Watch Point Address
102035E8	EMI_WP_CTRL	32	Watch Point Range
102035F0	EMI_CHKER	32	EMI AXI Checker
102035F4	EMI_CHKER_TYPE	32	EMI AXI Checker Type
102035F8	EMI_CHKER_ADR	32	EMI AXI Checker Address
10203700	EMI_EFF_MONA	32	EMI Efficiency Monitor Control Register A
10203704	EMI_EFF_MONB	32	EMI Efficiency Monitor Control Register B
10203708	EMI_EFF_MONC	32	EMI Efficiency Monitor Control Register C
1020370C	EMI_EFF_MOND	32	EMI Efficiency Monitor Control Register D
10203710	EMI_EFF_MONE	32	EMI Efficiency Monitor Control Register E
10203714	EMI_EFF_MONF	32	EMI Efficiency Monitor Control Register F
10203718	EMI_EFF_MONG	32	EMI Efficiency Monitor Control Register G
1020371C	EMI_EFF_MONH	32	EMI Efficiency Monitor Control Register H
10203720	EMI_EFF_MONI	32	EMI Efficiency Monitor Control Register I
10203724	EMI_EFF_MONJ	32	EMI Efficiency Monitor Control Register J
10203728	EMI_EFF_MONK	32	EMI Efficiency Monitor Control Register K
1020372C	EMI_EFF_MONL	32	EMI Efficiency Monitor Control Register L
10203730	EMI_EFF_MONM	32	EMI Efficiency Monitor Control Register M
10203734	EMI_EFF_MONN	32	EMI Efficiency Monitor Control Register N
10203738	EMI_EFF_MONO	32	EMI Efficiency Monitor Control Register O
1020373C	EMI_EFF_MONP	32	EMI Efficiency Monitor Control Register P

10203000 EMI_CONA **Address Mapping** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHN1_ROW2ND		CHN1_ROW		RANK_POS				CHN1_COL2ND		CHN1_COL			CHN_LOC	DUAL_RANK_EN	DUAL_RANK_EN_CHN1
Type	RW		RW		RW				RW		RW			RW	RW	RW
Reset	0	0	0	0	0				0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHN0_ROW2ND		CHN0_ROW		CAS_SIZE				CHN0_COL2ND		CHN0_COL		CHN_POS		DW32_EN	CHN_EN
Type	RW		RW		RW				RW		RW		RW		RW	RW
Reset	0	0	0	0	0	0			0	0	0	0	0	0	1	0

Bit(s)	Name	Description
31:30	CHN1_ROW2ND	**Rank 2 Row address bit number for channel 1** 0: 13-bit column address 1: 14-bit column address 2: 15-bit column address 3: 16-bit column address
29:28	CHN1_ROW	**Row address bit number for channel 1** 0: 13-bit column address 1: 14-bit column address 2: 15-bit column address 3: 16-bit column address
27	RANK_POS	**Selects emory mapping** 0: Address = {rank, row, bank,col} 1: Address = {row, rank, bank, col}. This mode is only supported when dual rank has the same bank and column bits.
23:22	CHN1_COL2ND	**Rank 2 Column address bit number for channel 1** 0: 9-bit column address (x32 only) 1: 10-bit column address 2: 11-bit column address 3: Reserved
21:20	CHN1_COL	**Column address bit number for channel 1** 0: 9-bit column address (x32 only) 1: 10-bit column address 2: 11-bit column address 3: Reserved
18	CHN_LOC	**Channel location** 0: Channel 0 1: Channel 1
17	DUAL_RANK_EN	**Enables two DRAM in one channel mode for channel 0** 0: Disable dual rank mode 1: Enable dual rank mode
16	DUAL_RANK_EN_CHN1	**Enables two DRAM in one channel mode for channel 1** 0: Disable dual rank mode 1: Enable dual rank mode
15:14	CHN0_ROW2ND	**Rank 2 Row address bit number for channel 0** 0: 13-bit column address 1: 14-bit column address 2: 15-bit column address 3: 16-bit column address
13:12	CHN0_ROW	**Row address bit number for channel 0** 0: 13-bit column address

Bit(s)	Name	Description
		1: 14-bit column address 2: 15-bit column address 3: 16-bit column address
11:10	CAS_SIZE	**Enables cascade mode** 2'b00: No cascase region 2'b01: 128MB 2'b10: 256MB 2'b11: 512MB
7:6	CHN0_COL2ND	**Rank 2 Column address bit number for channel 0** 0: 9-bit column address (x32 only) 1: 10-bit column address 2: 11-bit column address 3: Reserved
5:4	CHN0_COL	**Column address bit number for channel 0** 0: 9-bit column address (x32 only) 1: 10-bit column address 2: 11-bit column address 3: Reserved
3:2	CHN_POS	**Channel bit's position from AXI address view** The location of channel bit must be smaller than the bank address location. 0: AXI address bit 7 1: AXI address bit 8 2: AXI address bit 9 3: AXI address bit 12
1	DW32_EN	**32 bits data bus setting** 0: Reserved 1: Data bus supports 32 bits.
0	CHN_EN	**Enables two channel DRAM function** 0: One channel 1: Two channels

10203008 EMI_CONB **Data Transfer Overhead for Specific Data Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FOUR								THREE							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TWO								ONE							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	FOUR	**Overhead for 4 cycles of data transfer** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead ... 255: 15+ (15/16) overhead
23:16	THREE	**Overhead for 3 cycles of data transfer** 0: 0 overhead 1: 1/16 overhead

Bit(s)	Name	Description
		2: 1/8 overhead ... 255: 15+ (15/16) overhead
15:8	TWO	**Overhead for 2 cycles of data transfer** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead ... 255: 15+ (15/16) overhead
7:0	ONE	**Overhead for 1 cycle of data transfer** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead. ... 255: 15+ (15/16) overhead

10203010 EMI_CONC **Data Transfer Overhead for Specific Data Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EIGHT								SEVEN							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIX								FIVE							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	EIGHT	**Overhead for 8 cycles of data transfer** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead ... 255: 15+ (15/16) overhead
23:16	SEVEN	**Overhead for 7 cycles data transfer** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead ... 255: 15+ (15/16) overhead
15:8	SIX	**Overhead for 6 cycles of data transfer** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead ... 255: 15+ (15/16) overhead
7:0	FIVE	**Overhead for 5 cycles of data transfer** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead ... 255: 15+ (15/16) overhead

10203018 EMI_COND **FIFO Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WFF_BUSY_HIGH				WFF_BUSY_LOW				RFF_BUSY_HIGH				RFF_BUSY_LOW			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WFF_EMPTY_HIGH				WFF_EMPTY_LOW				RFF_EMPTY_HIGH				RFF_EMPTY_LOW			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	WFF_BUSY_HIGH	If the remaining write command FIFO is smaller than or equal to this field, rff_busy will be asserted.
27:24	WFF_BUSY_LOW	If the remaining write command FIFO is larger than this field, rff_busy will be de-asserted.
23:20	RFF_BUSY_HIGH	If the remaining read command FIFO is smaller than or equal to this field, rff_busy will be asserted.
19:16	RFF_BUSY_LOW	If the remaining read command FIFO is larger than this field, rff_busy will be de-asserted.
15:12	WFF_EMPTY_HIGH	If the remaining write command FIFO is smaller than this field, rff_empty will be de-asserted.
11:8	WFF_EMPTY_LOW	If the remaining write command FIFO is larger than or equal to this field, rff_empty will be asserted.
7:4	RFF_EMPTY_HIGH	If remain read command FIFO is smaller than this field, rff_empty will be de-asserted.
3:0	RFF_EMPTY_LOW	If the remaining read command FIFO is larger than or equal to this field, rff_empty will be asserted.

10203020 EMI_CONE **Feature Setting** **00000048**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AP_BUSY_WR_LAT								AP_BUSY_RD_LAT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AP_BUSY_THR				RCMD_OO_THR				DRAMC_CMD_CNT			
Type					RW				RW				RW			
Reset					0	0	0	0	0	1	0	0	1	0	0	0

Bit(s)	Name	Description
31:24	AP_BUSY_WR_LAT	**EMI APMCU busy threshold** If BW usage is over AP_BUSY_THR/16, EMI will change APMCU write startvation counter to AP_BUSY_WR_LAT.
23:16	AP_BUSY_RD_LAT	**EMI APMCU busy threshold** If BW usage is over AP_BUSY_THR/16, EMI will change APMCU read startvation counter to AP_BUSY_RD_LAT.
11:8	AP_BUSY_THR	**EMI APMCU busy threshold** If BW usage is over AP_BUSY_THR/16, EMI will change APMCU startvation counter to AP_BUSY_RD_LAT and AP_BUSY_WR_LAT. 0: Does not use AP_BUSY_RD_LAT and AP_BUSY_WR_LAT 1: 1/16 BW ... 14: 14/16 BW 15:15/16 BW
7:4	RCMD_OO_THR	**When RDQ is less than or equal to RCMD_OO_THR, EMI will stop reading out-of-order push.**

Bit(s)	Name	Description
3:0	DRAMC_CMD_CNT	This field cannot be 0. **DRAMC command FIFO count for test**

10203028 EMI_CONF **Address Scramble Setting** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BIT1 6_SC RAMB LE				BIT1 5_SC RAMB LE				BIT14_SCRAMBLE				BIT13_SCRAMBLE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIT12_SCRAMBLE				BIT11_SCRAMBLE											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Name	Description
31:28	BIT16_SCRAMBLE	**Enables scramble with address bit[19:16]** xxx1: XOR with address bit[16] xx1x: XOR with address bit[17] x1xx: XOR with address bit[18] 1xxx: XOR with address bit[19]
27:24	BIT15_SCRAMBLE	**Enables scramble with address bit[19:16]** xxx1: XOR with address bit[16] xx1x: XOR with address bit[17] x1xx: XOR with address bit[18] 1xxx: XOR with address bit[19]
23:20	BIT14_SCRAMBLE	**Enables scramble with address bit[19:16]** xxx1: XOR with address bit[16] xx1x: XOR with address bit[17] x1xx: XOR with address bit[18] 1xxx: XOR with address bit[19]
19:16	BIT13_SCRAMBLE	**Enables scramble with address bit[19:16]** xxx1: XOR with address bit[16] xx1x: XOR with address bit[17] x1xx: XOR with address bit[18] 1xxx: XOR with address bit[19]
15:12	BIT12_SCRAMBLE	**Enables scramble with address bit[19:16]** xxx1: XOR with address bit[16] xx1x: XOR with address bit[17] x1xx: XOR with address bit[18] 1xxx: XOR with address bit[19]
11:8	BIT11_SCRAMBLE	**Enables scramble with address bit[19:16]** SEDA does not support bit[11:9] scramble. xxx1: XOR with address bit[16] xx1x: XOR with address bit[17] x1xx: XOR with address bit[18]. 1xxx: XOR with address bit[19]

10203030 EMI_CONG **Data Transfer Overhead for Specific Non-36 bytes Alignment Data Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	EIGHT								SIX							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FOUR								TWO							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	EIGHT	**Overhead for 8 cycles of data transfer** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead ... 255: 15+ (15/16) overhead
23:16	SIX	**Overhead for 6 cycles of data transfer** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead ... 255: 15+ (15/16) overhead
15:8	FOUR	**Overhead for 4 cycles of data transfer** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead ... 255: 15+ (15/16) overhead
7:0	TWO	**Overhead for 2 cycles of data transfer** 0: 0 overhead 1: 1/16 overhead 2: 1/8 overhead ... 255: 15+ (15/16) overhead

10203038 EMI_CONH Address Mapping 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHN1_RANK 1_SIZE				CHN1_RANK0_SIZE				CHN0_RANK1_SIZE				CHN0_RANK0_SIZE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		BW_INT_BW_THR							BW_INT_EN	BW_INT_CLR	BW_INT_PER		BW_INT_MODE		DCM_RATIO	
Type		RW							RW	RW	RW		RW		RW	
Reset		0	0	0	0	0	0	0	0	0	0	0	0		0	0

Bit(s)	Name	Description
31:28	CHN1_RANK1_SIZE	**Channel 1 Rank 1 DRAM size** 0: Depend on CONA setting Others: Channel 1 Rank 1 DRAM size is CHN1_RANK1_SIZE*256MB
27:24	CHN1_RANK0_SIZE	**Channel 1 Rank 0 DRAM size** 0: Depend on CONA setting Others: Channel 1 Rank 0 DRAM size is CHN1_RANK0_SIZE*256MB
23:20	CHN0_RANK1_SIZE	**Channel 0 Rank 1 DRAM size**

Bit(s)	Name	Description
		0: Depend on CONA setting Others: Channel 0 Rank 1 DRAM size is CHN1_RANK1_SIZE*256MB
19:16	CHN0_RANK0_SIZE	**Channel 0 Rank 0 DRAM size** 0: Depend on CONA setting Others: Channel 0 Rank 0 DRAM size is CHN0_RANK0_SIZE*256MB
14:8	BW_INT_BW_THR	**BW interrupt threshold** 0: Reserved 1: BW larger than 1/64 issue interrupt 2: BW larger than 2/64 issue interrupt ... 127: BW larger than 127/64 issue interrupt
7	BW_INT_EN	**Enables BW interrupt** Interrupt will be cleared when EMI_BW status is read.
6	BW_INT_CLR	**BW_INT interrupt clear** Note: When read BW_INT_CLR ~= reg_conh[6]
5:4	BW_INT_PER	**BW interrupt period** 2'b00: 2^17 cycle 2'b01: 2^18 cycle 2'b10: 2^19 cycle 2'b11: 2^20 cycle
3	BW_INT_MODE	**BW interrupt mode** When BW_INT_MODE changes, all BW_INT related status/counter will be cleared. 0: BW larger than or equal to BW_THR issue interrupt 1: BW less than or equal to BW_THR issue interrupt
1:0	DCM_RATIO	**DCM slow-down ratio** 2'b00: no DCM 2'b01: 1/8 slow-down 2'b10: 1/16 slow-down 2'b11: 1/32 slow-down

1020303C EMI_BWST **BW Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EMI_BWST															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EMI_BWST															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EMI_BWST	**BW status** This register logs 32 period EMI BW information. When BW is larger than the threshold in one period, EMI_BW register will be set to 1.

10203040 EMI_CONI **ISP Configuration** **00000006**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ISP_WR_LATENCY								ISP_RD_LATENCY							

Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPU_WR_OS_THR_2				GPU_RD_OS_THR_2				ISP_ID2_EN		ISP_ID1_EN			MM_W_INFO_NUM		
Type	RW				RW				RW		RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0		1	1	

Bit(s)	Name	Description
31:24	ISP_WR_LATENCY	**Allowable write latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
23:16	ISP_RD_LATENCY	**Allowable read latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
15:12	GPU_WR_OS_THR_2	**Slave port write outstanding number** 0/1/2~14/15: 0/1/2/3/~/15
11:8	GPU_RD_OS_THR_2	**Slave port read outstanding number** 0/1/2~14/15: 0/4/6/~/30
7:6	ISP_ID2_EN	**Enables ISP ID match set 2** bit 0: Enable read bit 1: Enable write
5:4	ISP_ID1_EN	**Enables ISP ID match set 1** bit 0: Enable read bit 1: Enable write
2:1	MM_W_INFO_NUM	**MM port write information queue number**

10203048 EMI_CONJ **ISP Configuration 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ISP_ID_SET1_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISP_ID_SET1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ISP_ID_SET1_EN	Enables ISP ID match set 1 bit
15:0	ISP_ID_SET1	ISP ID match set 1

1020304C EMI_CONO **Address Mapping 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									SM_SEL_MASTER0							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		SM_BW_INT_BW_THR							SM_BW_INT_EN	SM_BW_INT_CLR	SM_BW_INT_PER		SM_BW_INT_MODE			
Type		RW							RW	RW	RW		RW			
Reset		0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
23:16	SM_SEL_MASTER0	**Monitors selected masters (master 0 ~ 7)** EMI_CONL[16]: ARM 0 EMI_CONL[17]: ARM 1 EMI_CONL[18]: MM 1 EMI_CONL[19]: MDMCU EMI_CONL[20]: Modem EMI_CONL[21]: Multimedia 0 EMI_CONL[22]: GPU 0 EMI_CONL[23]: GPU 1
14:8	SM_BW_INT_BW_THR	**BW interrupt threshold** 0: Reserved 1: BW larger than 1/64 issue interrupt 2: BW larger than 2/64 issue interrupt ... 127: BW larger than 127/64 issue interrupt
7	SM_BW_INT_EN	**BW interrupt enable. Interrupt will be clear when EMI_BW status will be read.**
6	SM_BW_INT_CLR	**Clears BW_INT interrupt** Note: Wwhen read SM_BW_INT_CLR ~= reg_cono[6]
5:4	SM_BW_INT_PER	**BW interrupt period** 2'b00: 2^20 cycle 2'b01: 2^21 cycle 2'b10: 2^22 cycle 2'b11: 2^23 cycle
3	SM_BW_INT_MODE	**BW interrupt mode** When BW_INT_MODE changes, all BW_INT related status/counter will be cleared. 0: BW larger than or equal to BW_THR issue interrupt 1: BW less than or equal to BW_THR issue interrupt

10203050 EMI_CONK ISP Configuration 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ISP_ID_SET2_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISP_ID_SET2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ISP_ID_SET2_EN	Enables ISP ID match set 2 bit
15:0	ISP_ID_SET2	ISP ID match set 2

1020305C EMI_BWST1 **Selected Master BW Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EMI_BWST1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EMI_BWST1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EMI_BWST1	**Selects master BW status** This registe logs 32 period EMI BW information. When BW is larger than the threshold in one period, EMI_BWST1 register will be set to 1.

10203060 EMI_CONM **MISC** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EMI_DCM_DIS								WR_RSV_NOR_NUM				RD_RSV_NOR_NUM			
Type	RW								RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						EMI_ENABLE	AGE_SPEED		PAGE_HIT_HIGH_PRIO_M7	PAGE_HIT_HIGH_PRIO_M6	PAGE_HIT_HIGH_PRIO_M5	PAGE_HIT_HIGH_PRIO_M4	PAGE_HIT_HIGH_PRIO_M3	PAGE_HIT_HIGH_PRIO_M2	PAGE_HIT_HIGH_PRIO_M1	ISP_ID_SET2_EN
Type						RW	RW		RW	RW	RW	RW	RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	EMI_DCM_DIS	**Disables EMI DCM** Bit 0: Disable write command and data DCM Bit 1: Disable read command DCM Bit 2: Disable read data DCM Bit 3: Reserved Bit 4: Disable emi_check module DCM Bit 5: Disable emi_command arbiter DCM Bit 6: Disable EMI top DCM Bit 7: Disable EMI APB DCM
23:20	WR_RSV_NOR_NUM	**Reserved write buffer for M0, ultra and under BW limiter request**
19:16	RD_RSV_NOR_NUM	**Reserved read buffer for M0, ultra and under BW limiter request**
10	EMI_ENABLE	**Enables EMI/DRAMC access** 0: No agent can access EMI or DRAMC. EMI will issue INT when someone accesses EMI. 1: Normal mode. EMI/DRAMC can be accessed.
9:8	AGE_SPEED	**Age decrement speed when bandwidth usage is larger than allocated one** 00: No decrement when bandwidth usage is larger than allocated one 01: 1/4 speed decrement when bandwidth usage is larger than allocated one

Bit(s)	Name	Description
		10: Normal speed decrement when bandwidth usage is larger than allocated one 11: 1/2 speed decrement when bandwidth usage is larger than allocated one
7	PAGE_HIT_HIGH_PRIO_M7	**Setting of page hit command is received first** 0: Does not receive page hit command when the master has issued allocated bandwidth 1: Receive page hit command first
6	PAGE_HIT_HIGH_PRIO_M6	**Setting of page hit command is received first** 0: Does not receive page hit command when the master has issued allocated bandwidth 1: Receive page hit command first
5	PAGE_HIT_HIGH_PRIO_M5	**Setting of page hit command is received first** 0: Does not receive page hit command when the master has issued allocated bandwidth 1: Receive page hit command first
4	PAGE_HIT_HIGH_PRIO_M4	**Setting of page hit command is received first** 0: Does not receive page hit command when the master has issued allocated bandwidth 1: Receive page hit command first
3	PAGE_HIT_HIGH_PRIO_M3	**Setting of page hit command is received first** 0: Does not receive page hit command when the master has issued allocated bandwidth 1: Receive page hit command first
2	PAGE_HIT_HIGH_PRIO_M2	**Setting of page hit command is received first** 0: Does not receive page hit command when the master has issued allocated bandwidth 1: Receive page hit command first
1	PAGE_HIT_HIGH_PRIO_M1	**Setting of page hit command is received first** 0: Does not receive page hit command when the master has issued allocated bandwidth 1: Receive page hit command first
0	ISP_ID_SET2_EN	**Setting of page hit command is received first** 0: Does not receive page hit command when the master has issued allocated bandwidth 1: Receive page hit command first

10203078 EMI_DRCT EMI Modem Control Register 12000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MDMCU_WR_MASK_EN	WR_AP_RSV_NUM			MDMCU_RD_MASK_EN	RD_AP_RSV_NUM			WR_HI_RSV_NUM		WR_ULTRA_RSV_NUM		RD_HI_RSV_NUM		RD_ULTRA_RSV_NUM	
Type	RW	RW			RW	RW			RW		RW		RW		RW	
Reset	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SBR_WRAP_MODE	MDMCU_SBR_EN	EXPIRE_SBR_EN	ULTRA_SBR_EN	W_ULTRA_WAIT_EN	R_ULTRA_WAIT_EN	W_ALL_WAIT_EN	R_ALL_WAIT_EN	R_ULTRA_STAR_WAIT_EN	W_ULTRA_STAR_WAIT_EN	W_S_AGE_EN	R_S_AGE_EN	W_S_ULT_EN	R_S_ULT_EN	W_A_ULT_EN	R_A_ULT_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MDMCU_WR_MASK_EN	**When MDMCU issues write request to DRAMC, the request of write command FIFO with same bank will be masked.**
30:28	WR_AP_RSV_NUM	**Reserved read buffer for APMCU** If the remaining buffer number is bigger than (WR_MDMCU_RSV_NUM+WR_ULTRA_RSV_NUM+WR_HI_RSV_NUM+WR_AP_RSV_NUM), APMCU command can be granted.
27	MDMCU_RD_MASK_EN	**When MDMCU issues read request to DRAMC, the request of read command FIFO with same bank will be masked.**
26:24	RD_AP_RSV_NUM	**Reserved read buffer for APMCU** If the remaining buffer number is bigger than (RD_MDMCU_RSV_NUM+RD_ULTRA_RSV_NUM+RD_HI_RSV_NUM+RD_AP_RSV_NUM), APMCU command can be granted.
23:22	WR_HI_RSV_NUM	**Reserved write buffer for high priority** If the remaining buffer number is bigger than (WR_MDMCU_RSV_NUM+WR_ULTRA_RSV_NUM+WR_HI_RSV_NUM), high priority command can be granted.
21:20	WR_ULTRA_RSV_NUM	**Reserved write buffer for ultra** If the remaining buffer number is bigger than (WR_MDMCU_RSV_NUM+WR_ULTRA_RSV_NUM), ultra priority command can be granted.
19:18	RD_HI_RSV_NUM	**Reserved read buffer for high priority** If the remaining buffer number is bigger than (RD_MDMCU_RSV_NUM+RD_ULTRA_RSV_NUM+RD_HI_RSV_NUM), high priority command can be granted.
17:16	RD_ULTRA_RSV_NUM	**Reserved read buffer for ultra** If the remaining buffer number is bigger than (RD_MDMCU_RSV_NUM+RD_ULTRA_RSV_NUM), ultra priority command can be granted.
15	SBR_WRAP_MODE	1: All 32B wrap accesses use 32 byte wrap mode.
14	MDMCU_SBR_EN	**Enables MDMCU command same bank reorder push**
13	EXPIRE_SBR_EN	**Enables starvation expired comman EMI to DRAMC same bank reorder push**
12	ULTRA_SBR_EN	**Enables ultra comman EMI to DRAMC same bank reorder push**
11	W_ULTRA_WAIT_EN	**Enables Write ultra command waiting when page miss for MD read requirement** MD write is not applied. 0: Does not wait 1: Wait until bank is not busy.
10	R_ULTRA_WAIT_EN	**Enables read ultra command waiting when page miss for MD read requirement** MD read is not applied. 0: Does not wait 1: Wait until bank is not busy.
9	W_ALL_WAIT_EN	**Enables write ultra command waiting when page miss** 0: Does not wait 1: Wait until bank is not busy.
8	R_ALL_WAIT_EN	**Enables read ultra command waiting when page miss** 0: Does not wait 1: Wait until bank is not busy.
7	R_ULTRA_STAR_WAIT_EN	**Enables read ultra and starvation command waiting when page miss for MD read requirement** MD read is not applied. 0: Does not wait 1: Wait until bank is not busy.
6	W_ULTRA_STAR_WAIT_EN	**Enables writed ultra and starvation command waiting when page miss for MD read requirement MD read is not applied.** 0: Does not wait 1: Wait until bank is not busy.

Bit(s)	Name	Description
5	W_S_AGE_EN	**Enables M3 write starvation higher than other feature** 0: Does not enable write starvation higher than other feature 1: Support write starvation higher than other feature
4	R_S_AGE_EN	**Enables M3 read starvation higher than other feature** 0: Does not enable read starvation higher than other feature 1: Support read starvation higher than other feature
3	W_S_ULT_EN	**Enables M3 write ultra high priority higher than other feature** 0: Does not enable read ultra high priority higher than other feature 1: Support read ultra high priority higher than other feature
2	R_S_ULT_EN	**Enables M3 read ultra high priority higher than other feature** 0: Does not enable read ultra high priority higher than other feature 1: Support read ultra high priority higher than other feature
1	W_A_ULT_EN	**Enables M3 write always ultra high priority feature** 0: Does not enable always ultra high priority feature 1: Support always ultra high priority feature
0	R_A_ULT_EN	**Enables M3 read always ultra high priority feature** 0: Does not enable always ultra high priority feature 1: Support always ultra high priority feature

102030D0 EMI_TEST0 **Test Mode 0** **88888888**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	M3_WR_OUTSTANDING				M3_RD_OUTSTANDING				M2_WR_OUTSTANDING				M2_RD_OUTSTANDING			
Type	RW				RW				RW				RW			
Reset	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	M1_WR_OUTSTANDING				M1_RD_OUTSTANDING				M0_WR_OUTSTANDING				M0_RD_OUTSTANDING			
Type	RW				RW				RW				RW			
Reset	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:28	M3_WR_OUTSTANDING	**Slave port write outstanding number** 0/1/2~14/15: 0/1/2/3/~/15
27:24	M3_RD_OUTSTANDING	**Slave port read outstanding number** 0/1/2~14/15: 0/4/6/~/30
23:20	M2_WR_OUTSTANDING	**Slave port write outstanding number** 0/1/2~14/15: 0/1/2/3/~/15
19:16	M2_RD_OUTSTANDING	**Slave port read outstanding number** 0/1/2~14/15: 0/4/6/~/30
15:12	M1_WR_OUTSTANDING	**Slave port write outstanding number** 0/1/2~14/15: 0/1/2/3/~/15
11:8	M1_RD_OUTSTANDING	**Slave port read outstanding number** 0/1/2~14/15: 0/4/6/~/30
7:4	M0_WR_OUTSTANDING	**Slave port write outstanding number** 0/1/2~14/15: 0/1/2/3/~/15
3:0	M0_RD_OUTSTANDING	**Slave port read outstanding number** 0/1/2~14/15: 0/2/4/~/30

102030D8 EMI_TEST1 **Test Mode 1** **88888888**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	M7_WR_OUTSTANDING				M7_RD_OUTSTANDING				M6_WR_OUTSTANDING				M6_RD_OUTSTANDING			

Type	RW				RW				RW				RW			
Reset	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	M5_WR_OUTSTANDING				M5_RD_OUTSTANDING				M4_WR_OUTSTANDING				M4_RD_OUTSTANDING			
Type	RW				RW				RW				RW			
Reset	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:28	M7_WR_OUTSTANDING	**Slave port write outstanding number** 0/1/2~14/15: 0/1/2/3/~/15.
27:24	M7_RD_OUTSTANDING	**Slave port read outstanding number** 0/1/2~14/15: 0/4/6/~/30
23:20	M6_WR_OUTSTANDING	**Slave port write outstanding number** 0/1/2~14/15: 0/1/2/3/~/15
19:16	M6_RD_OUTSTANDING	**Slave port read outstanding number** 0/1/2~14/15: 0/4/6/~/30
15:12	M5_WR_OUTSTANDING	**Slave port write outstanding number** 0/1/2~14/15: 0/1/2/3/~/15
11:8	M5_RD_OUTSTANDING	**Slave port read outstanding number** 0/1/2~14/15: 0/4/6/~/30
7:4	M4_WR_OUTSTANDING	**Slave port write outstanding number** 0/1/2~14/15: 0/1/2/3/~/15
3:0	M4_RD_OUTSTANDING	**Slave port read outstanding number** 0/1/2~14/15: 0/4/6/~/30

102030E0 EMI_TESTA **Test Mode A** **33433343**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RM_FG_CMD_THR2				RM_SERV_CNT_THR2				RM_FG_CMD_THR1				RM_SERV_CNT_THR1		
Type		RW				RW				RW				RW		
Reset		0	1	1		0	1	1		1	0	0		0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		WM_FG_CMD_THR2				WM_SERV_CNT_THR2				WM_FG_CMD_THR1				WM_SERV_CNT_THR1		
Type		RW				RW				RW				RW		
Reset		0	1	1		0	1	1		1	0	0		0	1	1

Bit(s)	Name	Description
30:28	RM_FG_CMD_THR2	**R_have_request_mask = serv_write & !r_have_urgent & ! more_than_max_write & [(serv_cnt <= RM_SERV_CNT_THR1 & FG_Pending_Cmd >= RM_FG_CMD_THR1) | (wcb_unmasked_diff_bk_cnt >= RM_SERV_CNT_THR2 & FG_Pending_Cmd >= WM_FG_CMD_THR2)]** This field can't be 0
26:24	RM_SERV_CNT_THR2	**R_have_request_mask = serv_write & !r_have_urgent & ! more_than_max_write & [(serv_cnt <= RM_SERV_CNT_THR1 & FG_Pending_Cmd >= RM_FG_CMD_THR1) | (wcb_unmasked_diff_bk_cnt >= RM_SERV_CNT_THR2 & FG_Pending_Cmd >= WM_FG_CMD_THR2)]**
22:20	RM_FG_CMD_THR1	**R_have_request_mask = serv_write & !r_have_urgent & ! more_than_max_write & [(serv_cnt <= RM_SERV_CNT_THR1 & FG_Pending_Cmd >= RM_FG_CMD_THR1) | (wcb_unmasked_diff_bk_cnt >=**

Bit(s)	Name	Description
		RM_SERV_CNT_THR2 & FG_Pending_Cmd >= WM_FG_CMD_THR2)] This field can't be 0
18:16	RM_SERV_CNT_THR1	R_have_request_mask = serv_write & !r_have_urgent & ! more_than_max_write & [(serv_cnt <= RM_SERV_CNT_THR1 & FG_Pending_Cmd >= RM_FG_CMD_THR1) | (wcb_unmasked_diff_bk_cnt >= RM_SERV_CNT_THR2 & FG_Pending_Cmd >= WM_FG_CMD_THR2)]
14:12	WM_FG_CMD_THR2	W_have_request_mask = !serv_write & !w_have_urgent & !more_than_max_read & [(serv_cnt <= WM_SERV_CNT_THR1 & FG_Pending_Cmd >= WM_FG_CMD_THR1) | (rcb_unmasked_diff_bk_cnt >= WM_SERV_CNT_THR2 & FG_Pending_Cmd >= WM_FG_CMD_THR2)] This field can't be 0
10:8	WM_SERV_CNT_THR2	W_have_request_mask = !serv_write & !w_have_urgent & !more_than_max_read & [(serv_cnt <= WM_SERV_CNT_THR1 & FG_Pending_Cmd >= WM_FG_CMD_THR1) | (rcb_unmasked_diff_bk_cnt >= WM_SERV_CNT_THR2 & FG_Pending_Cmd >= WM_FG_CMD_THR2)]
6:4	WM_FG_CMD_THR1	W_have_request_mask = !serv_write & !w_have_urgent & !more_than_max_read & [(serv_cnt <= WM_SERV_CNT_THR1 & FG_Pending_Cmd >= WM_FG_CMD_THR1) | (rcb_unmasked_diff_bk_cnt >= WM_SERV_CNT_THR2 & FG_Pending_Cmd >= WM_FG_CMD_THR2)] This field can't be 0
2:0	WM_SERV_CNT_THR1	W_have_request_mask = !serv_write & !w_have_urgent & !more_than_max_read & [(serv_cnt <= WM_SERV_CNT_THR1 & FG_Pending_Cmd >= WM_FG_CMD_THR1) | (rcb_unmasked_diff_bk_cnt >= WM_SERV_CNT_THR2 & FG_Pending_Cmd >= WM_FG_CMD_THR2)]

102030E8 EMI_TESTB **Test Mode B** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RD_INTERLEAVE_DIS								BW_THR				RD_DATA_MODE	WCMD_MDM CU_SUPER	RCMD_MDM CU_SUPER	WR_CHK_ORDER
Type	RW								RW				RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BW_THR_LE N		Mo_S HORT_DIS	RCMD_ISSUE_IN_ORDER	EARLY_RSP_DIS	EARLY_RESP_PRO_WR_DIS	SBR_MASK_CHK	DBG_OUT_EN	WR_ULTRA_WO_MASK	RSV_CHK_DQ	BYTE32_WRAP_EN	HALF_AGE_EN	COMMAND_SPLIT_EN	RFF_PBC_MASK_EN	RD_PBC_MASK_EN	PREULTRA_ENABLE
Type	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
31:24	RD_INTERLEAVE_DIS	**Disables read data interleave function by port**
23:20	BW_THR	**EMI BW threshold length** If BW usage is less than BW_THR/16, EMI will force M0 ultra. 0: Always non-ultra 1: 1/16 BW ... 14: 14/16 BW 15: Ultra always enabled
19	RD_DATA_MODE	0: Mask master of DRAMC input data before SRAM arbiter 1: Mask master of DRAMC input data after SRAM arbiter
18	WCMD_MDMCU_SUPER	**MDMCU write high priority command has higher priority than other write command.**
17	RCMD_MDMCU_SUPER	**MDMCU read high priority command has higher priority than other read command.**
16	WR_CHK_ORDER	**Writes command to DRAMC keep ID order**
15:14	BW_THR_LEN	**EMI BW threshold length** If BW usage is less than BW_THR/16, EMI will force M0 ultra. 2'b00: 256 cycles 2'b01: 512 cycles 2'b10: 1,024 cycles 2'b11: 2,048 cycles
13	M0_SHORT_DIS	**When all FIFOs are unused, APMCU read can bypss read command FIFO to reduce 1 cycle latency.** 0: Enable 1: Disable
12	RCMD_ISSUE_IN_ORDER	**Read command issue to DRAMC is in order** 0: Out- of- order 1: In order
11	EARLY_RSP_DIS	0: Enable early response function 1: Disable early response function
10	EARLY_RESP_PRO_WR_DIS	**When read early response occurs, EMI sets related write FIFO to be expired.**
9	SBR_MASK_CHK	0: Non-SBR command does not check reorder mask. 1: Non-SBR command checks reorder mask.
8	DBG_OUT_EN	**Enables debug output**
7	WR_ULTRA_WO_MASK	1: Ultra write command with starvation counter=0 does not need to defer read ultra with starvation counter=0.
6	RSV_CHK_DQ	**When EMI reserve buffer for AP, ultra, normal** 0: Check command FIFO only 1: Check command and data FIFO
5	BYTE32_WRAP_EN	**Processes wrap command in 32-byte alignment** 0: Process wrap command in 16-byte alignment 1: Process wrap command in 32-byte alignment
4	HALF_AGE_EN	**Shortens starvation value for high priority command** 0: Does not shorten starvation value 1: Shorten starvation value for high priority command
3	COMMAND_SPLIT_EN	**Splits long burst read command into two short commands** 0: Does not split read command 1: Split read command
2	RFF_PBC_MASK_EN	**Masks write command when row conflict with read command** 0: Write commands will not be masked. 1: Mask write commands
1	RD_PBC_MASK_EN	**Masks read command when row conflict with read command** 0: Read commands will not be masked. 1: Mask read commands

Bit(s)	Name	Description
0	PREULTRA_ENABLE	**When this feature is enabled, FIFO has the same ID as command arbiter granted ultra and preultra command.** 1. Starvation counter /2 or /4 by setting 2. Starvation counter does not check BW limiter.

102030F0 EMI_TESTC **Test Mode B** **38470000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CDWF_THR			DEFER_WR_WDATA_THR				DEFER_WR_RDATA_THR				DEFER_WR_WO_READ_PUSH	DEFER_WR_GROUP2	DEFER_WR_GROUP	URGENT_READ_FIRST
Type		RW			RW				RW				RW	RW	RW	RW
Reset		0	1	1	1	0	0	0	0	1	0	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RD_REORDER_DIS								M7_HIGH	M6_HIGH	M5_HIGH	M4_HIGH	M3_HIGH	M2_HIGH	M1_HIGH	M0_HIGH
Type	RW								RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:28	CDWF_THR	**Conditional DRAMC write flush issue threshold**
27:24	DEFER_WR_WDATA_THR	**Defer write group option 2: When DRAMC pending write data are larger than defer_wr_wdata_thr, EMI will stop pushing write command.** 0/1/2/~/15 means write data are 0/4/8/~/60. This field cannot be 0.
23:20	DEFER_WR_RDATA_THR	**Defer write group option 1: When DRAMC pending read data are larger than defer_wr_rdata_thr, EMI will stop pushing write command.** 0/1/2/~/15 means write data are 0/4/8/~/60. This field cannot be 0.
19	DEFER_WR_WO_READ_PUSH	**Channel arbiter will mask write when DRAMC queue counter is less than threhold. Enabling DEFER_WR_WO_READ_PUSH will remove read push in DRAMC queue count.**
18	DEFER_WR_GROUP2	**Defer write group option 2: When DRAMC pending write data are larger than defer_wr_wdata_thr, EMI will stop pushing write command.**
17	DEFER_WR_GROUP	**Defer write group: When DRAMC pending read data are larger than defer_wr_rdata_thr, EMI will stop pushing write command.**
16	URGENT_READ_FIRST	**Read first in channel artbiter**
15:8	RD_REORDER_DIS	**Disables read command re-order feature** 0: M0 1: M1 ...
7	M7_HIGH	**Enables bandwidth guarantee** 0: Does not enable 1: Enable bandwidth guarantee
6	M6_HIGH	**Enables bandwidth guarantee** 0: Does not enable 1: Enable bandwidth guarantee
5	M5_HIGH	**Enables bandwidth guarantee** 0: Does not enable

Bit(s)	Name	Description
		1: Enable bandwidth guarantee
4	M4_HIGH	**Enables bandwidth guarantee** 0: Does not enable 1: Enable bandwidth guarantee
3	M3_HIGH	**Enables bandwidth guarantee** 0: Does not enable 1: Enable bandwidth guarantee
2	M2_HIGH	**Enables bandwidth guarantee** 0: Does not enable 1: Enable bandwidth guarantee
1	M1_HIGH	**Enables bandwidth guarantee** 0: Does not enable 1: Enable bandwidth guarantee
0	M0_HIGH	**Enables bandwidth guarantee** 0: Does not enable 1: Enable bandwidth guarantee

102030F8 EMI_TESTD **Test Mode D** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EX_MODE	HARD_LIMIT	LOCK_DIS	WDF_DIS								WFF_DIS				
Type	RW	RW	RW	RW								RW				
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDF_FOR_SBR			RDF_DIS								RFF_DIS				
Type	RW			RW								RW				
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
31	EX_MODE	0: Overlapping write does not clear monitor. 1: Overlapping write clears monitor.
30	HARD_LIMIT	**Hard limit function** 0: Soft limit in channel arbiter 1: Hard limit in channel arbiter
29	LOCK_DIS	**Disables lock function** 0: Does not disable 1: Disable lock function
28:24	WDF_DIS	**Disables write data buffer number** Wait for 1ms to write 0 after 1 is written. If SW disables all buffer, EMI will be hanged. Due to LOCK EMI will need one FIFO to handle read/write at the same cycle case, EMI needs at least two (do not reserve the buffer) or three (reserve buffer) FIFO.
20:16	WFF_DIS	**Wait for 1ms to write 0 after 1 is written.** If SW disables all buffers, EMI will be hanged. Due to LOCK EMI will need one FIFO to handle read/write at the same cycle case, EMI needs at least two (do not reserve the buffer) or three (reserve the buffer) FIFOs.
15:13	RDF_FOR_SBR	**Disables read data buffer number for SBR command** (Read data FIO mnumber - RDF_DIS - RDF_FOR_SBR must > 4)
12:8	RDF_DIS	**Wait for 1ms to write 0 after 1 is written.** If SW disables all buffers, EMI will be hanged. EMI needs at least (reserved buffer+1) read FIFO.

Bit(s)	Name	Description
4:0	RFF_DIS	**Wait for 1ms to write 0 after 1 is written.** If SW disables all buffers, EMI will be hanged. Due to LOCK EMI will need one FIFO to handle read/write at the same cycle case. EMI needs at least two (do not reserve the buffer) or three (reserve the buffer) FIFO.

10203100 EMI_ARBA EMI Bandwidth Filter Control M0/1 00004000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Mo_WR_LATENCY								Mo_RD_LATENCY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Mo_BANDWIDTH_DISABLE	Mo_MODE	Mo_HI_PRIO_DOM_BW	Mo_BW_FILTER_EN	Mo_BW_FILTER_LEN		Mo_DOUBLE_HALF_BW			Mo_ULTRA_DOM_BW	Mo_BANDWIDTH					
Type	RW	RW	RW	RW	RW		RW			RW	RW					
Reset	0	1	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Mo_WR_LATENCY	**Allowable write latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
23:16	Mo_RD_LATENCY	**Allowable read latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
15	Mo_BANDWIDTH_DISABLE	**Stops counting consumed bandwidth** 0: Does not stop counting 1: Stop counting
14	Mo_MODE	**Bandwidth limit mode** 0: Hard mode 1: Soft mode
13	Mo_HI_PRIO_DOM_BW	**High priority requests dominate bandwidth limiter** 0: High priority requests from side-band signals should be controlled by bandwidth limiter. 1: High priority requests from side-band signals always dominate bandwidth limiter control.
12	Mo_BW_FILTER_EN	**Enables bandwidth filter** 0: Disable 1: Enable
11:10	Mo_BW_FILTER_LEN	**Enables bandwidth filter** 00: Filter length = 256 cycles 01: Filter length = 512 cycles 10: Filter length = 1,024 cycles 11: Filter length = 2,048 cycles
9:8	Mo_DOUBLE_HALF_BW	**Combined with allocated bandwidth** 00: Used for one channel LPDDR2-32, DDR3-32, LPDDR3-32

Bit(s)	Name	Description
		10: Used for two channel LPDDR2-32, DDR3-32, LPDDR3-32 01, 11: Reserved
6	M0_ULTRA_DOM_BW	**Ultra requests dominate bandwidth limiter** 0: Ultra priority requests from side-band signals should be controlled by bandwidth limiter. 1: Ultra priority requests from side-band signals always dominate bandwidth limiter control.
5:0	M0_BANDWIDTH	**Allocated bandwidth** Cannot be 0 in hard mode 0: Allocate 0 of the total bandwidth 1: Allocate 1/64 of the total bandwidth 2: Allocate 2/64 of the total bandwidth ... 63: Allocate 63/64 of the total bandwidth

10203108 EMI_ARBB **EMI Bandwidth Filter Control M1** **00004000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	M1_WR_LATENCY								M1_RD_LATENCY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	M1_BANDWIDTH_DISABLE	M1_MODE	M1_HI_PRIO_DOM_BW	M1_BW_FILTER_EN					M1_ULTRA_SLICE_EN	M1_ULTRA_DOM_BW	M1_BANDWIDTH					
Type	RW	RW	RW	RW					RW	RW	RW					
Reset	0	1	0	0					0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	M1_WR_LATENCY	**Allowable write latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
23:16	M1_RD_LATENCY	**Allowable read latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
15	M1_BANDWIDTH_DISABLE	**Stops counting consumed bandwidth** 0: Does not stop counting 1: Stop counting
14	M1_MODE	**Bandwidth limit mode** 0: Hard mode 1: Soft mode
13	M1_HI_PRIO_DOM_BW	**High priority requests dominate bandwidth limiter** 0: High priority requests from side-band signals should be controlled by bandwidth limiter. 1: High priority requests from side-band signals always dominate bandwidth limiter control.
12	M1_BW_FILTER_EN	**Enables bandwidth filter** 0: Disable

Bit(s)	Name	Description
		1: Enable
7	M1_ULTRA_SLICE_EN	**Enables M1 ultra slice**
6	M1_ULTRA_DOM_BW	**Ultra requests dominate bandwidth limiter** 0: Ultra priority requests from side-band signals should be controlled by bandwidth limiter. 1: Ultra priority requests from side-band signals always dominate bandwidth limiter control.
5:0	M1_BANDWIDTH	**Allocated bandwidth** Cannot be 0 in hard mode 0: Allocate 0 of the total bandwidth 1: Allocate 1/64 of the total bandwidth 2: Allocate 2/64 of the total bandwidth ... 63: Allocate 63/64 of the total bandwidth

10203110 EMI_ARBC EMI Bandwidth Filter Control M2 00004000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	M2_WR_LATENCY								M2_RD_LATENCY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	M2_BANDWIDTH_DISABLE	M2_MODE	M2_HI_PRIO_DOM_BW	M2_BW_FILTER_EN					M2_ULTRA_SLICE_EN	M2_ULTRA_DOM_BW	M2_BANDWIDTH					
Type	RW	RW	RW	RW					RW	RW	RW					
Reset	0	1	0	0					0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	M2_WR_LATENCY	**Allowable write latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
23:16	M2_RD_LATENCY	**Allowable read latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
15	M2_BANDWIDTH_DISABLE	**Stops counting consumed bandwidth** 0: Does not stop counting 1: Stop counting
14	M2_MODE	**Bandwidth limit mode** 0: Hard mode 1: Soft mode
13	M2_HI_PRIO_DOM_BW	**High priority requests dominate bandwidth limiter** 0: High priority requests from side-band signals should be controlled by bandwidth limiter. 1: High priority requests from side-band signals always dominate bandwidth limiter control.
12	M2_BW_FILTER_EN	**Enables bandwidth filter** 0: Disable

Bit(s)	Name	Description
		1: Enable
7	M2_ULTRA_SLICE_EN	**Enables M2 ultra slice**
6	M2_ULTRA_DOM_BW	**Ultra requests dominate bandwidth limiter** 0: Ultra priority requests from side-band signals should be controlled by bandwidth limiter. 1: Ultra priority requests from side-band signals always dominate bandwidth limiter control.
5:0	M2_BANDWIDTH	**Allocated bandwidth** Cannot be 0 in hard mode 0: Allocate 0 of the total bandwidth 1: Allocate 1/64 of the total bandwidth 2: Allocate 2/64 of the total bandwidth ... 63: Allocate 63/64 of the total bandwidth

10203118 EMI_ARBD EMI Bandwidth Filter Control M3 00004000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	M3_WR_LATENCY								M3_RD_LATENCY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	M3_BANDWIDTH_DISABLE	M3_MODE	M3_HI_PRIO_DOM_BW	M3_BW_FILTER_EN	WR_MDMCU_RSV_NUM		RD_MDMCU_RSV_NUM			M3_ULTRA_DOM_BW	M3_BANDWIDTH					
Type	RW	RW	RW	RW	RW		RW			RW	RW					
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	M3_WR_LATENCY	**Allowable read latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
23:16	M3_RD_LATENCY	**Allowable write latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
15	M3_BANDWIDTH_DISABLE	**Stops counting consumed bandwidth** 0: Does not stop counting 1: Stop counting
14	M3_MODE	**Bandwidth limit mode** 0: Hard mode 1: Soft mode
13	M3_HI_PRIO_DOM_BW	**High priority requests dominate bandwidth limiter** 0: High priority requests from side-band signals should be controlled by bandwidth limiter. 1: High priority requests from side-band signals always dominate bandwidth limiter control.
12	M3_BW_FILTER_EN	**Enables bandwidth filter** 0: Disable

Bit(s)	Name	Description
		1: Enable
11:10	WR_MDMCU_RSV_NUM	**Reserved write buffer for MDMCU** If the remaining buffer number is bigger than (WR_MDMCU_RSV_NUM), MDMCU command can be granted.
9:7	RD_MDMCU_RSV_NUM	**Reserved read buffer for MDMCU** If the remaining buffer number is bigger than (WR_MDMCU_RSV_NUM), MDMCU command can be granted.
6	M3_ULTRA_DOM_BW	**Ultra requests dominate bandwidth limiter** 0: Ultra priority requests from side-band signals should be controlled by bandwidth limiter. 1: Ultra priority requests from side-band signals always dominate bandwidth limiter control.
5:0	M3_BANDWIDTH	**Allocated bandwidth** Cannot be 0 in hard mode. 0: Allocate 0 of the total bandwidth 1: Allocate 1/64 of the total bandwidth 2: Allocate 2/64 of the total bandwidth ... 63: Allocate 63/64 of the total bandwidth

10203120 EMI_ARBE **EMI Bandwidth Filter Control M4** **00004000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	M4_WD_LATENCY								M4_RD_LATENCY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	M4_BANDWIDTH_DISABLE	M4_MODE	M4_HI_PRIO_DOM_BW	M4_BW_FILTER_EN						M4_ULTRA_DOM_BW	M4_BANDWIDTH					
Type	RW	RW	RW	RW						RW	RW					
Reset	0	1	0	0						0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	M4_WD_LATENCY	**Allowable latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles.
23:16	M4_RD_LATENCY	**Allowable latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
15	M4_BANDWIDTH_DISABLE	**Stops counting consumed bandwidth** 0: Does not stop counting 1: Stop counting
14	M4_MODE	**Bandwidth limit mode** 0: Hard mode 1: Soft mode

Bit(s)	Name	Description
13	M4_HI_PRIO_DOM_BW	**High priority requests dominate bandwidth limiter** 0: High priority requests from side-band signals should be controlled by bandwidth limiter. 1: High priority requests from side-band signals always dominate bandwidth limiter control.
12	M4_BW_FILTER_EN	**Enables bandwidth filter** 0: Disable 1: Enable
6	M4_ULTRA_DOM_BW	**Ultra requests dominate bandwidth limiter** 0: Ultra priority requests from side-band signals should be controlled by bandwidth limiter. 1: Ultra priority requests from side-band signals always dominate bandwidth limiter control.
5:0	M4_BANDWIDTH	**Allocated bandwidth** Cannot be 0 in hard mode. 0: Allocate 0 of the total bandwidth 1: Allocate 1/64 of the total bandwidth 2: Allocate 2/64 of the total bandwidth ... 63: Allocate 63/64 of the total bandwidth

10203128 EMI_ARBF EMI Bandwidth Filter Control M5 00004000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	M5_WR_LATENCY								M5_RD_LATENCY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	M5_BANDWIDTH_DISABLE	M5_MODE	M5_HI_PRIO_DOM_BW	M5_BW_FILTER_EN					M5_ULTRA_SLICE_EN	M5_ULTRA_DOM_BW	M5_BANDWIDTH					
Type	RW	RW	RW	RW					RW	RW	RW					
Reset	0	1	0	0					0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	M5_WR_LATENCY	**Allowable write latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
23:16	M5_RD_LATENCY	**Allowable read latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
15	M5_BANDWIDTH_DISABLE	**Stops counting consumed bandwidth** 0: Does not stop counting 1: Stop counting
14	M5_MODE	**Bandwidth limit mode** 0: Hard mode 1: Soft mode
13	M5_HI_PRIO_DOM_BW	**High priority requests dominate bandwidth limiter**

Bit(s)	Name	Description
		0: High priority requests from side-band signals should be controlled by bandwidth limiter. 1: High priority requests from side-band signals always dominate bandwidth limiter control.
12	M5_BW_FILTER_EN	**Enables bandwidth filter** 0: Disable 1: Enable
7	M5_ULTRA_SLICE_EN	**Enables M5 ultra slice**
6	M5_ULTRA_DOM_BW	**Ultra requests dominate bandwidth limiter** 0: Ultra priority requests from side-band signals should be controlled by bandwidth limiter. 1: Ultra priority requests from side-band signals always dominate bandwidth limiter control.
5:0	M5_BANDWIDTH	**Allocated bandwidth** Cannot be 0 in hard mode 0: Allocate 0 of the total bandwidth 1: Allocate 1/64 of the total bandwidth 2: Allocate 2/64 of the total bandwidth ... 63: Allocate 63/64 of the total bandwidth

10203130 EMI_ARBG **EMI Bandwidth Filter Control M5** **00004000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	M6_WR_LATENCY								M6_RD_LATENCY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	M6_BANDWIDTH_DISABLE	M6_MODE	M6_HI_PRIO_DOM_BW	M6_BW_FILTER_EN					M6_ULTRA_SLICE_EN	M6_ULTRA_DOM_BW	M6_BANDWIDTH					
Type	RW	RW	RW	RW					RW	RW	RW					
Reset	0	1	0	0					0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	M6_WR_LATENCY	**Allowable write latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
23:16	M6_RD_LATENCY	**Allowable read latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
15	M6_BANDWIDTH_DISABLE	**Stops counting consumed bandwidth** 0: Does not stop counting 1: Stop counting
14	M6_MODE	**Bandwidth limit mode** 0: Hard mode 1: Soft mode
13	M6_HI_PRIO_DOM_BW	**High priority requests dominate bandwidth limiter**

Bit(s)	Name	Description
		0: High priority requests from side-band signals should be controlled by bandwidth limiter. 1: High priority requests from side-band signals always dominate bandwidth limiter control.
12	M6_BW_FILTER_EN	**Enables bandwidth filter** 0: Disable 1: Enable
7	M6_ULTRA_SLICE_EN	**Enables M6 ultra slice**
6	M6_ULTRA_DOM_BW	**Ultra requests dominate bandwidth limiter** 0: Ultra priority requests from side-band signals should be controlled by bandwidth limiter. 1: Ultra priority requests from side-band signals always dominate bandwidth limiter control.
5:0	M6_BANDWIDTH	**Allocated bandwidth** Cannot be 0 in hard mode 0: Allocate 0 of the total bandwidth 1: Allocate 1/64 of the total bandwidth 2: Allocate 2/64 of the total bandwidth ... 63: Allocate 63/64 of the total bandwidth

10203134 EMI_ARBG_2ND **EMI Bandwidth Filter Control GPU_2** **00004000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPU_WR_LATENCY								GPU_RD_LATENCY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPU_BANDWIDTH_DISABLE	GPU_MODE	GPU_HI_PRIO_DOM_BW	GPU_BW_FILTER_EN						GPU_ULTRA_DOM_BW	GPU_BANDWIDTH					
Type	RW	RW	RW	RW						RW	RW					
Reset	0	1	0	0						0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	GPU_WR_LATENCY	**Allowable write latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
23:16	GPU_RD_LATENCY	**Allowable read latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
15	GPU_BANDWIDTH_DISABLE	**Stops counting consumed bandwidth** 0: Does not stop counting 1: Stop counting
14	GPU_MODE	**Bandwidth limit mode** 0: Hard mode 1: Soft mode

Bit(s)	Name	Description
13	GPU_HI_PRIO_DOM_BW	**High priority requests dominate bandwidth limiter** 0: High priority requests from side-band signals should be controlled by bandwidth limiter. 1: High priority requests from side-band signals always dominate bandwidth limiter control.
12	GPU_BW_FILTER_EN	**Enables bandwidth filter** 0: Disable 1: Enable
6	GPU_ULTRA_DOM_BW	**Ultra requests dominate bandwidth limiter** 0: Ultra priority requests from side-band signals should be controlled by bandwidth limiter. 1: Ultra priority requests from side-band signals always dominate bandwidth limiter control.
5:0	GPU_BANDWIDTH	**Allocated bandwidth** Cannot be 0 in hard mode 0: Allocate 0 of the total bandwidth 1: Allocate 1/64 of the total bandwidth 2: Allocate 2/64 of the total bandwidth ... 63: Allocate 63/64 of the total bandwidth

10203138 EMI_ARBH EMI Bandwidth Filter Control M5 00004000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	M7_WR_LATENCY								M7_RD_LATENCY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	M7_BANDWIDTH_DISABLE	M7_MODE	M7_HI_PRIO_DOM_BW	M7_BW_FILTER_EN					M7_ULTRA_SLICE_EN	M7_ULTRA_DOM_BW	M7_BANDWIDTH					
Type	RW	RW	RW	RW					RW	RW	RW					
Reset	0	1	0	0					0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	M7_WR_LATENCY	**Allowable write latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
23:16	M7_RD_LATENCY	**Allowable read latency in cycles** 0: 3 cycles 1: 7 cycles 2: 11 cycles ... 255: 1,023 cycles
15	M7_BANDWIDTH_DISABLE	**Stops counting consumed bandwidth** 0: Does not stop counting 1: Stop counting
14	M7_MODE	**Bandwidth limit mode** 0: Hard mode 1: Soft mode
13	M7_HI_PRIO_DOM_BW	**High priority requests dominate bandwidth limiter**

Bit(s)	Name	Description
		0: High priority requests from side-band signals should be controlled by bandwidth limiter. 1: High priority requests from side-band signals always dominate bandwidth limiter control.
12	M7_BW_FILTER_EN	**Enables bandwidth filter** 0: Disable 1: Enable
7	M7_ULTRA_SLICE_EN	**Enables M7 ultra slice**
6	M7_ULTRA_DOM_BW	**Ultra requests dominate bandwidth limiter** 0: Ultra priority requests from side-band signals should be controlled by bandwidth limiter. 1: Ultra priority requests from side-band signals always dominate bandwidth limiter control.
5:0	M7_BANDWIDTH	**Allocated bandwidth** Cannot be 0 in hard mode 0: Allocate 0 of the total bandwidth 1: Allocate 1/64 of the total bandwidth 2: Allocate 2/64 of the total bandwidth ... 63: Allocate 63/64 of the total bandwidth

10203140 EMI_ARBI **Filter Priority Encode** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	URGENT_2ND				LLAT				URGENT				MISS			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIT				LIMIT				AGE				ULTRA			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	URGENT_2ND	**2nd urgent priority code** The waiting time for the command is going to expire. Bigger number means higher priority. This number must be smaller than the older age code. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
27:24	LLAT	**Low latency request priority code** This means one command has the longest time delay with the previous page miss command among all command candidates. Bigger number means higher priority. This number must be smaller than the older age code. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
23:20	URGENT	**Urgent priority code** The waiting time for the command is going to expire. Bigger number means higher priority. This number must be smaller than the older age code. 0: The lowest priority 1: Priority higher than 0 ...

Bit(s)	Name	Description
		15: The highest priority
19:16	MISS	**No page miss with previous commands priority code** This means the page miss overhead can be hidden by the data cycles. Bigger number means higher priority. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
15:12	HIT	**Page hit priority code** Bigger number means higher priority. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
11:8	LIMIT	**No bandwidth limit priority code** The master does not consume its requested bandwidth. Bigger number means higher priority. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
7:4	AGE	**Order age priority code** The waiting time for the command is expired. Bigger number means higher priority. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
3:0	ULTRA	**Ultra high priority code** Bigger number means higher priority. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority

10203144 EMI_ARBI_2ND **Filter Priority Encode for MD Requirement** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	URGENT_2ND				LLAT				URGENT				MISS			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIT				LIMIT				AGE				ULTRA			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	URGENT_2ND	**2nd urgent priority code** The waiting time for the command is going to expire. Bigger number means higher priority. This number must besmaller than the older age code. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
27:24	LLAT	**Low latency request priority code**

Bit(s)	Name	Description
		This means one command has the longest time delay with the previous page miss command among all command candidates. Bigger number means higher priority. This number must be smaller than the older age code. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
23:20	URGENT	**Urgent priority code** The waiting time for the command is going to expire. Bigger number means higher priority. This number must besmaller than the older age code. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
19:16	MISS	**No page miss with previous commands priority code** This means the page miss overhead can be hidden by the data cycles. Bigger number means higher priority. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
15:12	HIT	**Page hit priority code** Bigger number means higher priority. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
11:8	LIMIT	**No bandwidth limit priority code** The master does not consume its requested bandwidth. Bigger number means higher priority. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
7:4	AGE	**Order age priority code** The waiting time for the command is expired. Bigger number means higher priority. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority
3:0	ULTRA	**Ultra high priority code** Bigger number means higher priority. 0: The lowest priority 1: Priority higher than 0 ... 15: The highest priority

10203148 EMI_ARBJ Turn Around Command Number 00684848

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RD_ULTRA_RDCNT_MIN				WR_ULTRA_WRCNT_MIN				POST_WR_CNT				WR_DLY_CYC			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RDCNT_MIN				RDCNT				WRCNT_MIN				WRCNT			
Type	RW				RW				RW				RW			
Reset	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0	0

Bit(s)	Name	Description
31:28	RD_ULTRA_RDCNT_MIN	**Issues read command numbers and changes to write commands when having urgent write command and urgent read command** 0: 4 read command 1: 8 read commands ... 15: Does not change to write command
27:24	WR_ULTRA_WRCNT_MIN	**Issues write command numbers and changes to read commands when having urgent read command and urgent write command** 0: 2 write command 1: 4 write commands ... 15: Does not change to read command
23:20	POST_WR_CNT	**Switches servicing read command to write command when there is n write commands and no read commands (combined with WR_DLY_CYC)** 0: 1 pending write command ... 15: 16 pending write commands
19:16	WR_DLY_CYC	**Delayed cycle number to issue write command when there is no pending read commands** 0: 1 cycle ... 15: 16 cycles
15:12	RDCNT_MIN	**Issues read command numbers and changes to write commands when having urgent write command** 0: 1 read command 1: 2 read commands ... 15: Does not change to write command
11:8	RDCNT	**Issues read command numbers and changes to write commands** 0: 4 read command 1: 8 read commands ... 15: Does not change to write command
7:4	WRCNT_MIN	**Issues write command numbers and changes to read commands when having urgent read command** 0: 1 write command 1: 2 write commands ... 15: Does not change to read command
3:0	WRCNT	**Issues write command numbers and changes to read commands** 0: 2 write command 1: 4 write commands ... 15: Does not change to read command

1020314C EMI_ARBJ_2ND **Turn Around Command Number for MD Requirement** **00684848**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RD_ULTRA_RDCNT_MIN				WR_ULTRA_WRCNT_MIN				POST_WR_CNT				WR_DLY_CYC			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDCNT_MIN				RDCNT				WRCNT_MIN				WRCNT			
Type	RW				RW				RW				RW			
Reset	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0	0

Bit(s)	Name	Description
31:28	RD_ULTRA_RDCNT_MIN	**Issues read command numbers and changes to write commands when having urgent write command and urgent read command** 0: 4 read command 1: 8 read commands ... 15: Does not change to write command
27:24	WR_ULTRA_WRCNT_MIN	**Issues write command numbers and changes to read commands when having urgent read command and urgent write command** 0: 2 write command 1: 4 write commands ... 15: Does not change to read command
23:20	POST_WR_CNT	**Switches servicing read command to write command when there is n write commands and no read commands (combined with WR_DLY_CYC)** 0: 1 pending write command ... 15: 16 pending write commands
19:16	WR_DLY_CYC	**Delayed cycle number to issue write command when there is no pending read commands** 0: 1 cycle ... 15: 16 cycles
15:12	RDCNT_MIN	**Issues read command numbers and changes to write commands when having urgent write command** 0: 1 read command 1: 2 read commands ... 15: Does not change to write command
11:8	RDCNT	**Issues read command numbers and changes to write commands** 0: 4 read command 1: 8 read commands ... 15: Does not change to write command
7:4	WRCNT_MIN	**Issues write command numbers and changes to read commands when having urgent read command** 0: 1 write command 1: 2 write commands ... 15: Does not change to read command
3:0	WRCNT	**Issues write command numbers and changes to read commands** 0: 2 write command 1: 4 write commands ... 15: Does not change to read command

10203150 EMI_ARBK Channel Arbiter Control 64003C7C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MULTI_CONF_BAN_PRO_NUM				RD_BAN_PRO_NUM				URGENT_CYC_2ND				URGENT_CYC_1St			
Type	RW				RW				RW				RW			
Reset	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MULTI_CONF_BAN_PRO	RD_BAN_PRO	PAGE_MISS_DLY_CYC				WR_SERV_CNT_MAX				RD_SERV_CNT_MAX			
Type			RW	RW	RW				RW				RW			
Reset			1	1	1	1	0	0	0	1	1	1	1	1	0	0

Bit(s)	Name	Description
31:28	MULTI_CONF_BAN_PRO_NUM	**When row confict command is larger than MULTI_CONF_BAN_PRO_NUM, EMI will inform DRAMC to promot this bank.**
27:24	RD_BAN_PRO_NUM	**When critical latenay bank command is larger than RD_BAN_PRO_NUM, EMI will inform DRAMC to promote this bank.**
23:20	URGENT_CYC_2ND	**Second level urgent active when the acceptable latency is less than specified cycles** 0: 31 cycles ... 15: 511 cycles
19:16	URGENT_CYC_1St	**First level urgent active when the acceptable latency is less than specified cycles** 0: 31 cycles ... 15: 511 cycles
13	MULTI_CONF_BAN_PRO	**When row confict command is larger than MULTI_CONF_BAN_PRO, EMI will inform DRAMC to promote this bank.** 0: Disable 1: Enable
12	RD_BAN_PRO	**When critical latenay bank command is larger than RD_BAN_PRO, EMI will inform DRAMC to promote this bank.** 0: Disable 1: Enable
11:8	PAGE_MISS_DLY_CYC	**Delays command request n cycles to channel arbiter when the command is page miss with previous grant command** 0: Delay 5 cycles ... 15: Delay 20 cycles
7:4	WR_SERV_CNT_MAX	**Read request will be masked in some conditions.** However, when write issue is over WR_SERV_CNT_MAXx2, read mask will be disabled.
3:0	RD_SERV_CNT_MAX	**Write request will be masked in some conditions.** However, when read issue is over RD_SERV_CNT_MAXx4, write mask will be disabled.

10203154 EMI_ARBK_2 Channel Arbiter Control 64003C7C

ND

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MULTI_CONF_BAN_PRO_NUM				RD_BAN_PRO_NUM				URGENT_CYC_2ND				URGENT_CYC_1St			
Type	RW				RW				RW				RW			
Reset	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MULTI_CONF_BAN_PRO	RD_BAN_PRO	PAGE_MISS_DLY_CYC				WR_SERV_CNT_MAX				RD_SERV_CNT_MAX			
Type			RW	RW	RW				RW				RW			
Reset			1	1	1	1	0	0	0	1	1	1	1	1	0	0

Bit(s)	Name	Description
31:28	MULTI_CONF_BAN_PRO_NUM	**When row confict command is larger than MULTI_CONF_BAN_PRO_NUM, EMI will inform DRAMC to promot this bank.**
27:24	RD_BAN_PRO_NUM	**When critical latenay bank command is larger than RD_BAN_PRO_NUM, EMI will inform DRAMC to promote this bank.**
23:20	URGENT_CYC_2ND	**Second level urgent active when the acceptable latency is less than specified cycles.** 0: 31 cycles ... 15: 511 cycles
19:16	URGENT_CYC_1St	**When critical latenay bank command is larger than RD_BAN_PRO, EMI will inform DRAMC to promote this bank.** 0: Disable 1: Enable
13	MULTI_CONF_BAN_PRO	**First level urgent active when the acceptable latency is less than specified cycles.** 0: 31 cycles ... 15: 511 cycles
12	RD_BAN_PRO	**When row confict command is larger than MULTI_CONF_BAN_PRO, EMI will inform DRAMC to promote this bank.** 0: Disable 1: Enable
11:8	PAGE_MISS_DLY_CYC	**Delays command request n cycles to channel arbiter when the command is page miss with previous grant command** 0: Delay 5 cycles ... 15: Delay 20 cycles
7:4	WR_SERV_CNT_MAX	**Read request will be masked in some conditions.** However, when write issue is over WR_SERV_CNT_MAXx2, read mask will be disabled.
3:0	RD_SERV_CNT_MAX	**Write request will be masked in some conditions.** However, when read issue is over RD_SERV_CNT_MAXx4, write mask will be disabled.

10203158 EMI_SLCT EMI Slave Control Registers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	M7_HI_PRIO_IND_EN	M6_HI_PRIO_IND_EN	M5_HI_PRIO_IND_EN	M4_HI_PRIO_IND_EN	M3_HI_PRIO_IND_EN	M2_HI_PRIO_IND_EN	M1_HI_PRIO_IND_EN	M0_HI_PRIO_IND_EN	M7_LLAT_EN	M6_LLAT_EN	M5_LLAT_EN	M4_LLAT_EN	M3_LLAT_EN	M2_LLAT_EN	M1_LLAT_EN	M0_LLAT_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HI_PRIO_EN_M7	HI_PRIO_EN_M6	HI_PRIO_EN_M5	HI_PRIO_EN_M4	HI_PRIO_EN_M3	HI_PRIO_EN_M2	HI_PRIO_EN_M1	HI_PRIO_EN_M0								
Type	RW	RW	RW	RW	RW	RW	RW	RW								
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Name	Description
31	M7_HI_PRIO_IND_EN	**Enables read high priority indication to DRAMC feature (for real-time GPU)** 0: Does not support high priority indication feature 1: Support high priority indication feature
30	M6_HI_PRIO_IND_EN	**Enables read high priority indication to DRAMC feature (for normal GPU)** 0: Does not support high priority indication feature 1: Support high priority indication feature
29	M5_HI_PRIO_IND_EN	**Enables read high priority indication to DRAMC feature** 0: Does not support high priority indication feature 1: Support high priority indication feature
28	M4_HI_PRIO_IND_EN	**Enables read high priority indication to DRAMC feature** 0: Does not support high priority indication feature 1: Support high priority indication feature
27	M3_HI_PRIO_IND_EN	**Enables read high priority indication to DRAMC feature** 0: Does not support high priority indication feature 1: Support high priority indication feature
26	M2_HI_PRIO_IND_EN	**Enables read high priority indication to DRAMC feature** 0: Does not support high priority indication feature 1: Support high priority indication feature
25	M1_HI_PRIO_IND_EN	**Enables read high priority indication to DRAMC feature (for PERISYS input from M0/1)** 0: Does not support high priority indication feature 1: Support high priority indication feature
24	M0_HI_PRIO_IND_EN	**Enables read high priority indication to DRAMC feature (for APMCU input from M0/1)** 0: Does not support high priority indication feature 1: Support high priority indication feature
23	M7_LLAT_EN	**Enables read low latency feature (for real-time GPU)** 0: Does not support low latency feature 1: Support low latency feature
22	M6_LLAT_EN	**Enables read low latency feature (for normal GPU)** 0: Does not support low latency feature 1: Support low latency feature
21	M5_LLAT_EN	**Enables read low latency feature** 0: Does not support low latency feature 1: Support low latency feature
20	M4_LLAT_EN	**Enables read low latency feature** 0: Does not support low latency feature 1: Support low latency feature
19	M3_LLAT_EN	**Enables read low latency feature** 0: Does not support low latency feature

Bit(s)	Name	Description
		1: Support low latency feature
18	M2_LLAT_EN	**Enables read low latency feature** 0: Does not support low latency feature 1: Support low latency feature
17	M1_LLAT_EN	**Enables read low latency feature (for PERISYS input from M0/1)** 0: Does not support low latency feature 1: Support low latency feature
16	M0_LLAT_EN	**Enables read low latency feature (for APMCU input from M0/1)** 0: Does not support low latency feature 1: Support low latency feature
15	HI_PRIO_EN_M7	**Enables high priority feature** 0: Does not support high priority feature 1: Support high priority feature
14	HI_PRIO_EN_M6	**Enables high priority feature** 0: Does not support high priority feature 1: Support high priority feature
13	HI_PRIO_EN_M5	**Enables high priority feature** 0: Does not support high priority feature 1: Support high priority feature
12	HI_PRIO_EN_M4	**Enables high priority feature** 0: Does not support high priority feature 1: Support high priority feature
11	HI_PRIO_EN_M3	**Enables high priority feature** 0: Does not support high priority feature 1: Support high priority feature
10	HI_PRIO_EN_M2	**Enables high priority feature** 0: Does not support high priority feature 1: Support high priority feature
9	HI_PRIO_EN_M1	**Enables high priority feature** 0: Does not support high priority feature 1: Support high priority feature
8	HI_PRIO_EN_M0	**Enables high priority feature** 0: Does not support high priority feature 1: Support high priority feature

102031D8 EMI_MPUP **Memory Protection Unit Control Registers P** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					R23_VIO	R22_VIO	R21_VIO	R20_VIO	R15_VIO	R14_VIO	R13_VIO	R12_VIO	R11_VIO	R10_VIO	R9_VIO	R8_VIO
Type					W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R19_VIO	R18_VIO	R17_VIO	R16_VIO			OOR_VIO	APB_VIO	R7_VIO	R6_VIO	R5_VIO	R4_VIO	R3_VIO	R2_VIO	R1_VIO	R0_VIO
Type	W1C	W1C	W1C	W1C			W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27	R23_VIO	**Region 23 abort violation status to domain 0** 0: No region 7 abort violation

Bit(s)	Name	Description
		1: Region 7 abort violation
26	R22_VIO	**Region 22 abort violation status to domain 0** 0: No region 6 abort violation 1: Region 6 abort violation
25	R21_VIO	**Region 21 abort violation status to domain 0** 0: No region 5 abort violation 1: Region 5 abort violation
24	R20_VIO	**Region 20 abort violation status to domain 0** 0: No region 4 abort violation 1: Region 4 abort violation
23	R15_VIO	**Region 15 abort violation status to domain 0** 0: No region 7 abort violation 1: Region 7 abort violation
22	R14_VIO	**Region 14 abort violation status to domain 0** 0: No region 6 abort violation 1: Region 6 abort violation
21	R13_VIO	**Region 13 abort violation status to domain 0** 0: No region 5 abort violation 1: Region 5 abort violation
20	R12_VIO	**Region 12 abort violation status to domain 0** 0: No region 4 abort violation 1: Region 4 abort violation
19	R11_VIO	**Region 11 abort violation status to domain 0** 0: No region 3 abort violation 1: Region 3 abort violation
18	R10_VIO	**Region 10 abort violation status to domain 0** 0: No region 2 abort violation 1: Region 2 abort violation
17	R9_VIO	**Region 9 abort violation status to domain 0** 0: No region 1 abort violation 1: Region 1 abort violation
16	R8_VIO	**Region 8 abort violation status to domain 0** EMI will first record the unmasked device abort information at EMI_MPUS and EMI_MPUT if unmasked and set up the corresponding R0_VIO status bit. Clear R0_VIO for EMI to record the next violation status. When multiple violations occur, the corresponding D0_VIO_STA status bit will be set. However, only the device abort information will be recorded at VIO_DBGx, and its content will not be changed until the software clears it. 0: No region 0 abort violation 1: Region 0 abort violation
15	R19_VIO	**Region 19 abort violation status to domain 0** 0: No region 19 abort violation 1: Region 19 abort violation
14	R18_VIO	**Region 18 abort violation status to domain 0** 0: No region 18 abort violation 1: Region 18 abort violation
13	R17_VIO	**Region 17 abort violation status to domain 0** 0: No region 17 abort violation 1: Region 17 abort violation
12	R16_VIO	**Region 16 abort violation status to domain 0** 0: No region 16 abort violation 1: Region 16 abort violation
9	OOR_VIO	**Out of range abort violation status to domain 0** 0: No out of range abort violation 1: Out of range abort violation

Bit(s)	Name	Description
8	APB_VIO	**APB abort violation status to domain 0** Note: Accessing EMI_MPUP is allowed in the secure mode only when D0_SEC = 1. 0: No APB abort violation 1: APB abort violation
7	R7_VIO	**Region 7 abort violation status to domain 0** 0: No region 7 abort violation 1: Region 7 abort violation
6	R6_VIO	**Region 6 abort violation status to domain 0** 0: No region 6 abort violation 1: Region 6 abort violation
5	R5_VIO	**Region 5 abort violation status to domain 0** 0: No region 5 abort violation 1: Region 5 abort violation
4	R4_VIO	**Region 4 abort violation status to domain 0** 0: No region 4 abort violation 1: Region 4 abort violation
3	R3_VIO	**Region 3 abort violation status to domain 0** 0: No region 3 abort violation 1: Region 3 abort violation
2	R2_VIO	**Region 2 abort violation status to domain 0** 0: No region 2 abort violation 1: Region 2 abort violation
1	R1_VIO	**Region 1 abort violation status to domain 0** 0: No region 1 abort violation 1: Region 1 abort violation
0	R0_VIO	**Region 0 abort violation status to domain 0** EMI will first record the unmasked device abort information at EMI_MPUS and EMI_MPUT if unmasked and set up the corresponding R0_VIO status bit. Clear R0_VIO for EMI to record the next violation status. When multiple violations occur, the corresponding D0_VIO_STA status bit will be set. However, only the device abort information will be recorded at VIO_DBGx, and its content will not be changed until the software clears it. 0: No region 0 abort violation 1: Region 0 abort violation

102031E0 EMI_MPUQ **Memory Protection Unit Control Registers Q** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					R23_VIO	R22_VIO	R21_VIO	R20_VIO	R15_VIO	R14_VIO	R13_VIO	R12_VIO	R11_VIO	R10_VIO	R9_VIO	R8_VIO
Type					W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R19_VIO	R18_VIO	R17_VIO	R16_VIO			OOR_VIO	APB_VIO	R7_VIO	R6_VIO	R5_VIO	R4_VIO	R3_VIO	R2_VIO	R1_VIO	R0_VIO
Type	W1C	W1C	W1C	W1C			W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27	R23_VIO	**Region 23 abort violation status to domain 1** 0: No region 7 abort violation

Bit(s)	Name	Description
		1: Region 7 abort violation
26	R22_VIO	**Region 22 abort violation status to domain 1** 0: No region 6 abort violation 1: Region 6 abort violation
25	R21_VIO	**Region 21 abort violation status to domain 1** 0: No region 5 abort violation 1: Region 5 abort violation
24	R20_VIO	**Region 20 abort violation status to domain 1** 0: No region 4 abort violation 1: Region 4 abort violation
23	R15_VIO	**Region 15 abort violation status to domain 1** 0: No region 7 abort violation 1: Region 7 abort violation
22	R14_VIO	**Region 14 abort violation status to domain 1** 0: No region 6 abort violation 1: Region 6 abort violation
21	R13_VIO	**Region 13 abort violation status to domain 1** 0: No region 5 abort violation 1: Region 5 abort violation
20	R12_VIO	**Region 12 abort violation status to domain 1** 0: No region 4 abort violation 1: Region 4 abort violation
19	R11_VIO	**Region 11 abort violation status to domain 1** 0: No region 3 abort violation 1: Region 3 abort violation
18	R10_VIO	**Region 10 abort violation status to domain 1** 0: No region 2 abort violation 1: Region 2 abort violation
17	R9_VIO	**Region 9 abort violation status to domain 1** 0: No region 1 abort violation 1: Region 1 abort violation
16	R8_VIO	**Region 8 abort violation status to domain 1** EMI will first record the unmasked device abort information at EMI_MPUS and EMI_MPUT if unmasked and set up the corresponding R0_VIO status bit. Clear R0_VIO for EMI to record the next violation status. When multiple violations occur, the corresponding D0_VIO_STA status bit will be set. However, only the device abort information will be recorded at VIO_DBGx, and its content will not be changed until the software clears it. 0: No region 0 abort violation 1: Region 0 abort violation
15	R19_VIO	**Region 19 abort violation status to domain 1** 0: No region 19 abort violation 1: Region 19 abort violation
14	R18_VIO	**Region 18 abort violation status to domain 1** 0: No region 18 abort violation 1: Region 18 abort violation
13	R17_VIO	**Region 17 abort violation status to domain 1** 0: No region 17 abort violation 1: Region 17 abort violation
12	R16_VIO	**Region 16 abort violation status to domain 1** 0: No region 16 abort violation 1: Region 16 abort violation
9	OOR_VIO	**Out of range abort violation status to domain 1** 0: No out of range abort violation 1: Out of range abort violation

Bit(s)	Name	Description
8	APB_VIO	**APB abort violation status to domain 1** Note: Accessing EMI_MPUQ is allowed in the secure mode only when D1_SEC = 1. 0: No APB abort violation 1: APB abort violation
7	R7_VIO	**Region 7 abort violation status to domain 1** 0: No region 7 abort violation 1: Region 7 abort violation
6	R6_VIO	**Region 6 abort violation status to domain 1** 0: No region 6 abort violation 1: Region 6 abort violation
5	R5_VIO	**Region 5 abort violation status to domain 1** 0: No region 5 abort violation 1: Region 5 abort violation
4	R4_VIO	**Region 4 abort violation status to domain 1** 0: No region 4 abort violation 1: Region 4 abort violation
3	R3_VIO	**Region 3 abort violation status to domain 1** 0: No region 3 abort violation 1: Region 3 abort violation
2	R2_VIO	**Region 2 abort violation status to domain 1** 0: No region 2 abort violation 1: Region 2 abort violation
1	R1_VIO	**Region 1 abort violation status to domain 1** 0: No region 1 abort violation 1: Region 1 abort violation
0	R0_VIO	**Region 0 abort violation status to domain 1** 0: No region 0 abort violation 1: Region 0 abort violation

102031E8 EMI_MPUR **Memory Protection Unit Control Registers R** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					R23_VIO	R22_VIO	R21_VIO	R20_VIO	R15_VIO	R14_VIO	R13_VIO	R12_VIO	R11_VIO	R10_VIO	R9_VIO	R8_VIO
Type					W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R19_VIO	R18_VIO	R17_VIO	R16_VIO			OOR_VIO	APB_VIO	R7_VIO	R6_VIO	R5_VIO	R4_VIO	R3_VIO	R2_VIO	R1_VIO	R0_VIO
Type	W1C	W1C	W1C	W1C			W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27	R23_VIO	**Region 23 abort violation status to domain 2** 0: No region 7 abort violation 1: Region 7 abort violation
26	R22_VIO	**Region 22 abort violation status to domain 2** 0: No region 6 abort violation 1: Region 6 abort violation
25	R21_VIO	**Region 21 abort violation status to domain 2** 0: No region 5 abort violation 1: Region 5 abort violation

Bit(s)	Name	Description
24	R20_VIO	**Region 20 abort violation status to domain 2** 0: No region 4 abort violation 1: Region 4 abort violation
23	R15_VIO	**Region 15 abort violation status to domain 2** 0: No region 7 abort violation 1: Region 7 abort violation
22	R14_VIO	**Region 14 abort violation status to domain 2** 0: No region 6 abort violation 1: Region 6 abort violation
21	R13_VIO	**Region 13 abort violation status to domain 2** 0: No region 5 abort violation 1: Region 5 abort violation
20	R12_VIO	**Region 12 abort violation status to domain 2** 0: No region 4 abort violation 1: Region 4 abort violation
19	R11_VIO	**Region 11 abort violation status to domain 2** 0: No region 3 abort violation 1: Region 3 abort violation
18	R10_VIO	**Region 10 abort violation status to domain 2** 0: No region 2 abort violation 1: Region 2 abort violation
17	R9_VIO	**Region 9 abort violation status to domain 2** 0: No region 1 abort violation 1: Region 1 abort violation
16	R8_VIO	**Region 8 abort violation status to domain 2** EMI will first record the unmasked device abort information at EMI_MPUS and EMI_MPUT if unmasked and set up the corresponding R0_VIO status bit. Clear R0_VIO for EMI to record the next violation status. When multiple violations occur, the corresponding D0_VIO_STA status bit will be set. However, only the device abort information will be recorded at VIO_DBGx, and its content will not be changed until the software clears it. 0: No region 0 abort violation 1: Region 0 abort violation
15	R19_VIO	**Region 19 abort violation status to domain 2** 0: No region 19 abort violation 1: Region 19 abort violation
14	R18_VIO	**Region 18 abort violation status to domain 2** 0: No region 18 abort violation 1: Region 18 abort violation
13	R17_VIO	**Region 17 abort violation status to domain 2** 0: No region 17 abort violation 1: Region 17 abort violation
12	R16_VIO	**Region 16 abort violation status to domain 2** 0: No region 16 abort violation 1: Region 16 abort violation
9	OOR_VIO	**Out of range abort violation status to domain 2** 0: No out of range abort violation 1: Out of range abort violation
8	APB_VIO	**APB abort violation status to domain 2** Note: Accessing EMI_MPUR is allowed in the secure mode only when D2_SEC = 1. 0: No APB abort violation 1: APB abort violation
7	R7_VIO	**Region 7 abort violation status to domain 2** 0: No region 7 abort violation

Bit(s)	Name	Description
		1: Region 7 abort violation
6	R6_VIO	**Region 6 abort violation status to domain 2** 0: No region 6 abort violation 1: Region 6 abort violation
5	R5_VIO	**Region 5 abort violation status to domain 2** 0: No region 5 abort violation 1: Region 5 abort violation
4	R4_VIO	**Region 4 abort violation status to domain 2** 0: No region 4 abort violation 1: Region 4 abort violation
3	R3_VIO	**Region 3 abort violation status to domain 2** 0: No region 3 abort violation 1: Region 3 abort violation
2	R2_VIO	**Region 2 abort violation status to domain 2** 0: No region 2 abort violation 1: Region 2 abort violation
1	R1_VIO	**Region 1 abort violation status to domain 2** 0: No region 1 abort violation 1: Region 1 abort violation
0	R0_VIO	**Region 0 abort violation status to domain 2** 0: No region 0 abort violation 1: Region 0 abort violation

102031F0 EMI_MPUS **Memory Protection Unit Control Registers S** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLR		R_VIO	W_VIO			FIX_ABORT	APB_ABORT	DOMAIN_ID			REGION_ABORT				
Type	WO		RO	RO			RO	RO	RO			RO				
Reset	0		0	0			0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MASTER_ID													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	CLR	**Clears debugging information** 0: No action 1: Clear debugging information
29	R_VIO	**Read violation** 0: Abort is not caused by a READ violation. 1: Abort is caused by a READ violation.
28	W_VIO	**Write violation** 0: Abort is not caused by a WRITE violation. 1: Abort is caused by a WRITE violation.
25	FIX_ABORT	**Indicates if fix transaction violation causes the abort** 0: Abort is not caused by a APB violation. 1: Abort is caused by a APB violation.
24	APB_ABORT	**Indicates if APB violation causes the abort** 0: Abort is not caused by a APB violation. 1: Abort is caused by a APB violation.
23:21	DOMAIN_ID	**Violation domain ID**

Bit(s)	Name	Description
		00: Domain 0 violation 01: Domain 1 violation 10: Domain 2 violation 11: Domain 3 violation 11: Reserved
20:16	REGION_ABORT	**Violated region** 0: Region 0 is violated. 1: Region 1 is violated. 2: Region 2 is violated. ... 19: Region 19 is violated.
13:0	MASTER_ID	**Records the violation master ID {AXI ID, Port ID}** AXI ID: 13 bits Port ID: 3 bits Bit 115 at 0x1f0[27:26]

102031F8 EMI_MPUT Memory Protection Unit Control Registers T 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPU_ERROR_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPU_ERROR_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MPU_ERROR_ADDR	**Violation address** If the violation comes from APB, the violation address will record the register offset value. Note: EMI_MPUS and EMI_MPUT are allowed to be cleared in the secure mode when D0_SEC = 1 or D1_SEC = 1 or D2_SEC = 1.

10203220 EMI_MPUY Memory Protection Unit Control Registers Y 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					R23_VIO	R22_VIO	R21_VIO	R20_VIO	R15_VIO	R14_VIO	R13_VIO	R12_VIO	R11_VIO	R10_VIO	R9_VIO	R8_VIO
Type					W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R19_VIO	R18_VIO	R17_VIO	R16_VIO			OOR_VIO	APB_VIO	R7_VIO	R6_VIO	R5_VIO	R4_VIO	R3_VIO	R2_VIO	R1_VIO	R0_VIO
Type	W1C	W1C	W1C	W1C			W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27	R23_VIO	**Region 23 abort violation status to domain 3** 0: No region 7 abort violation

Bit(s)	Name	Description
		1: Region 7 abort violation
26	R22_VIO	**Region 22 abort violation status to domain 3** 0: No region 6 abort violation 1: Region 6 abort violation
25	R21_VIO	**Region 21 abort violation status to domain 3** 0: No region 5 abort violation 1: Region 5 abort violation
24	R20_VIO	**Region 20 abort violation status to domain 3** 0: No region 4 abort violation 1: Region 4 abort violation
23	R15_VIO	**Region 15 abort violation status to domain 3** 0: No region 7 abort violation 1: Region 7 abort violation
22	R14_VIO	**Region 14 abort violation status to domain 3** 0: No region 6 abort violation 1: Region 6 abort violation
21	R13_VIO	**Region 13 abort violation status to domain 3** 0: No region 5 abort violation 1: Region 5 abort violation
20	R12_VIO	**Region 12 abort violation status to domain 3** 0: No region 4 abort violation 1: Region 4 abort violation
19	R11_VIO	**Region 11 abort violation status to domain 3** 0: No region 3 abort violation 1: Region 3 abort violation
18	R10_VIO	**Region 10 abort violation status to domain 3** 0: No region 2 abort violation 1: Region 2 abort violation
17	R9_VIO	**Region 9 abort violation status to domain 3** 0: No region 1 abort violation 1: Region 1 abort violation
16	R8_VIO	**Region 8 abort violation status to domain 3** EMI will first record the unmasked device abort information at EMI_MPUS and EMI_MPUT if unmasked and set up the corresponding R0_VIO status bit. Clear R0_VIO for EMI to record the next violation status. When multiple violations occur, the corresponding D0_VIO_STA status bit will be set. However, only the device abort information will be recorded at VIO_DBGx, and its content will not be changed until the software clears it. 0: No region 0 abort violation 1: Region 0 abort violation
15	R19_VIO	**Region 19 abort violation status to domain 3** 0: No region 19 abort violation 1: Region 19 abort violation
14	R18_VIO	**Region 18 abort violation status to domain 3** 0: No region 18 abort violation 1: Region 18 abort violation
13	R17_VIO	**Region 17 abort violation status to domain 3** 0: No region 17 abort violation 1: Region 17 abort violation
12	R16_VIO	**Region 16 abort violation status to domain 3** 0: No region 16 abort violation 1: Region 16 abort violation
9	OOR_VIO	**Out of range abort violation status to domain 3** 0: No out of range abort violation 1: Out of range abort violation

Bit(s)	Name	Description
8	APB_VIO	**APB abort violation status to domain 3** Note: EMI_MPUR is allowed to be accessed in the secure mode only when D2_SEC = 1. 0: No APB abort violation 1: APB abort violation
7	R7_VIO	**Region 7 abort violation status to domain 3** 0: No region 7 abort violation 1: Region 7 abort violation
6	R6_VIO	**Region 6 abort violation status to domain 3** 0: No region 6 abort violation 1: Region 6 abort violation
5	R5_VIO	**Region 5 abort violation status to domain 3** 0: No region 5 abort violation 1: Region 5 abort violation
4	R4_VIO	**Region 4 abort violation status to domain 3** 0: No region 4 abort violation 1: Region 4 abort violation
3	R3_VIO	**Region 3 abort violation status to domain 3** 0: No region 3 abort violation 1: Region 3 abort violation
2	R2_VIO	**Region 2 abort violation status to domain 3** 0: No region 2 abort violation 1: Region 2 abort violation
1	R1_VIO	**Region 1 abort violation status to domain 3** 0: No region 1 abort violation 1: Region 1 abort violation
0	R0_VIO	**Region 0 abort violation status to domain 3** 0: No region 0 abort violation 1: Region 0 abort violation

102032D8 EMI_MPUP2 **Memory Protection Unit Control Registers P** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					R23_VIO	R22_VIO	R21_VIO	R20_VIO	R15_VIO	R14_VIO	R13_VIO	R12_VIO	R11_VIO	R10_VIO	R9_VIO	R8_VIO
Type					W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R19_VIO	R18_VIO	R17_VIO	R16_VIO			OOR_VIO	APB_VIO	R7_VIO	R6_VIO	R5_VIO	R4_VIO	R3_VIO	R2_VIO	R1_VIO	R0_VIO
Type	W1C	W1C	W1C	W1C			W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27	R23_VIO	**Region 23 abort violation status to domain 4** 0: No region 7 abort violation 1: Region 7 abort violation
26	R22_VIO	**Region 22 abort violation status to domain 4** 0: No region 6 abort violation 1: Region 6 abort violation
25	R21_VIO	**Region 21 abort violation status to domain 4** 0: No region 5 abort violation 1: Region 5 abort violation

Bit(s)	Name	Description
24	R20_VIO	**Region 20 abort violation status to domain 4** 0: No region 4 abort violation 1: Region 4 abort violation
23	R15_VIO	**Region 15 abort violation status to domain 4** 0: No region 15 abort violation 1: Region 15 abort violation
22	R14_VIO	**Region 14 abort violation status to domain 4** 0: No region 14 abort violation 1: Region 14 abort violation
21	R13_VIO	**Region 13 abort violation status to domain 4** 0: No region 13 abort violation 1: Region 13 abort violation
20	R12_VIO	**Region 12 abort violation status to domain 4** 0: No region 12 abort violation 1: Region 12 abort violation
19	R11_VIO	**Region 11 abort violation status to domain 4** 0: No region 11 abort violation 1: Region 11 abort violation
18	R10_VIO	**Region 10 abort violation status to domain 4** 0: No region 10 abort violation 1: Region 10 abort violation
17	R9_VIO	**Region 9 abort violation status to domain 4** 0: No region 9 abort violation 1: Region 9 abort violation
16	R8_VIO	**Region 8 abort violation status to domain 4** EMI will first record the unmasked device abort information at EMI_MPUS and EMI_MPUT if unmasked and set up the corresponding R8_VIO status bit. Clear R8_VIO for EMI to record the next violation status. When multiple violations occur, the corresponding D0_VIO_STA status bit will be set. However, only the device abort information will be recorded at VIO_DBGx, and its content will not be changed until the software clears it. 0: No region 8 abort violation 1: Region 8 abort violation
15	R19_VIO	**Region 19 abort violation status to domain 0** 0: No region 19 abort violation 1: Region 19 abort violation
14	R18_VIO	**Region 18 abort violation status to domain 0** 0: No region 18 abort violation 1: Region 18 abort violation
13	R17_VIO	**Region 17 abort violation status to domain 0** 0: No region 17 abort violation 1: Region 17 abort violation
12	R16_VIO	**Region 16 abort violation status to domain 0** 0: No region 16 abort violation 1: Region 16 abort violation
9	OOR_VIO	**Out of range abort violation status to domain 4** 0: No out of range abort violation 1: Out of range abort violation
8	APB_VIO	**APB abort violation status to domain 4** Note: Accessing EMI_MPUP2 is allowed in the secure mode only when D4_SEC = 1. 0: No APB abort violation 1: APB abort violation
7	R7_VIO	**Region 7 abort violation status to domain 4** 0: No region 7 abort violation

Bit(s)	Name	Description
		1: Region 7 abort violation
6	R6_VIO	**Region 6 abort violation status to domain 4** 0: No region 6 abort violation 1: Region 6 abort violation
5	R5_VIO	**Region 5 abort violation status to domain 4** 0: No region 5 abort violation 1: Region 5 abort violation
4	R4_VIO	**Region 4 abort violation status to domain 4** 0: No region 4 abort violation 1: Region 4 abort violation
3	R3_VIO	**Region 3 abort violation status to domain 4** 0: No region 3 abort violation 1: Region 3 abort violation
2	R2_VIO	**Region 2 abort violation status to domain 4** 0: No region 2 abort violation 1: Region 2 abort violation
1	R1_VIO	**Region 1 abort violation status to domain 4** 0: No region 1 abort violation 1: Region 1 abort violation
0	R0_VIO	**region 0 abort violation status to domain 4** EMI will first record the unmasked device abort information at EMI_MPUS and EMI_MPUT if unmasked and set up the corresponding R0_VIO status bit. Clear R0_VIO for EMI to record the next violation status. When multiple violations occur, the corresponding D0_VIO_STA status bit will be set. However, only the device abort information will be recorded at VIO_DBGx, and its content will not be changed until the software clears it. 0: No region 0 abort violation 1: Region 0 abort violation

102032E0 EMI_MPUQ2 **Memory Protection Unit Control Registers Q** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					R23_VIO	R22_VIO	R21_VIO	R20_VIO	R15_VIO	R14_VIO	R13_VIO	R12_VIO	R11_VIO	R10_VIO	R9_VIO	R8_VIO
Type					W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R19_VIO	R18_VIO	R17_VIO	R16_VIO			OOR_VIO	APB_VIO	R7_VIO	R6_VIO	R5_VIO	R4_VIO	R3_VIO	R2_VIO	R1_VIO	R0_VIO
Type	W1C	W1C	W1C	W1C			W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27	R23_VIO	**Region 23 abort violation status to domain 5** 0: No region 7 abort violation 1: Region 7 abort violation
26	R22_VIO	**Region 22 abort violation status to domain 5** 0: No region 6 abort violation 1: Region 6 abort violation
25	R21_VIO	**Region 21 abort violation status to domain 5** 0: No region 5 abort violation 1: Region 5 abort violation

Bit(s)	Name	Description
24	R20_VIO	**Region 20 abort violation status to domain 5** 0: No region 4 abort violation 1: Region 4 abort violation
23	R15_VIO	**Region 15 abort violation status to domain 5** 0: No region 15 abort violation 1: Region 15 abort violation
22	R14_VIO	**Region 14 abort violation status to domain 5** 0: No region 14 abort violation 1: Region 14 abort violation
21	R13_VIO	**Region 13 abort violation status to domain 5** 0: No region 13 abort violation 1: Region 13 abort violation
20	R12_VIO	**Region 12 abort violation status to domain 5** 0: No region 12 abort violation 1: Region 12 abort violation
19	R11_VIO	**Region 11 abort violation status to domain 5** 0: No region 11 abort violation 1: Region 11 abort violation
18	R10_VIO	**Region 10 abort violation status to domain 5** 0: No region 10 abort violation 1: Region 10 abort violation
17	R9_VIO	**Region 9 abort violation status to domain 5** 0: No region 9 abort violation 1: Region 9 abort violation
16	R8_VIO	**Region 8 abort violation status to domain 5** EMI will first record the unmasked device abort information at EMI_MPUS and EMI_MPUT if unmasked and set up the corresponding R8_VIO status bit. Clear R8_VIO for EMI to record the next violation status. When multiple violations occur, the corresponding D0_VIO_STA status bit will be set. However, only the device abort information will be recorded at VIO_DBGx, and its content will not be changed until the software clears it. 0: No region 8 abort violation 1: Region 8 abort violation
15	R19_VIO	**Region 19 abort violation status to domain 0** 0: No region 19 abort violation 1: Region 19 abort violation
14	R18_VIO	**Region 18 abort violation status to domain 0** 0: No region 18 abort violation 1: Region 18 abort violation
13	R17_VIO	**Region 17 abort violation status to domain 0** 0: No region 17 abort violation 1: Region 17 abort violation
12	R16_VIO	**Region 16 abort violation status to domain 0** 0: No region 16 abort violation 1: Region 16 abort violation
9	OOR_VIO	**Out of range abort violation status to domain 5** 0: No out of range abort violation 1: Out of range abort violation
8	APB_VIO	**APB abort violation status to domain 5** Note: Accessing EMI_MPUP2 is allowed in the secure mode only when D4_SEC = 1. 0: No APB abort violation 1: APB abort violation
7	R7_VIO	**Region 7 abort violation status to domain 5** 0: No region 7 abort violation

Bit(s)	Name	Description
		1: Region 7 abort violation
6	R6_VIO	**Region 6 abort violation status to domain 5** 0: No region 6 abort violation 1: Region 6 abort violation
5	R5_VIO	**Region 5 abort violation status to domain 5** 0: No region 5 abort violation 1: Region 5 abort violation
4	R4_VIO	**Region 4 abort violation status to domain 5** 0: No region 4 abort violation 1: Region 4 abort violation
3	R3_VIO	**Region 3 abort violation status to domain 5** 0: No region 3 abort violation 1: Region 3 abort violation
2	R2_VIO	**Region 2 abort violation status to domain 5** 0: No region 2 abort violation 1: Region 2 abort violation
1	R1_VIO	**Region 1 abort violation status to domain 5** 0: No region 1 abort violation 1: Region 1 abort violation
0	R0_VIO	**Region 0 abort violation status to domain 5** 0: No region 0 abort violation 1: Region 0 abort violation

102032E8 EMI_MPUR2 **Memory Protection Unit Control Registers R** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					R23_VIO	R22_VIO	R21_VIO	R20_VIO	R15_VIO	R14_VIO	R13_VIO	R12_VIO	R11_VIO	R10_VIO	R9_VIO	R8_VIO
Type					W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R19_VIO	R18_VIO	R17_VIO	R16_VIO			OOR_VIO	APB_VIO	R7_VIO	R6_VIO	R5_VIO	R4_VIO	R3_VIO	R2_VIO	R1_VIO	R0_VIO
Type	W1C	W1C	W1C	W1C			W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27	R23_VIO	**Region 23 abort violation status to domain 6** 0: No region 7 abort violation 1: Region 7 abort violation
26	R22_VIO	**Region 22 abort violation status to domain 6** 0: No region 6 abort violation 1: Region 6 abort violation
25	R21_VIO	**Region 21 abort violation status to domain 6** 0: No region 5 abort violation 1: Region 5 abort violation
24	R20_VIO	**Region 20 abort violation status to domain 6** 0: No region 4 abort violation 1: Region 4 abort violation
23	R15_VIO	**Region 15 abort violation status to domain 6** 0: No region 15 abort violation 1: Region 15 abort violation
22	R14_VIO	**Region 14 abort violation status to domain 6**

Bit(s)	Name	Description
		0: No region 14 abort violation 1: Region 14 abort violation
21	R13_VIO	**Region 13 abort violation status to domain 6** 0: No region 13 abort violation 1: Region 13 abort violation
20	R12_VIO	**Region 12 abort violation status to domain 6** 0: No region 12 abort violation 1: Region 12 abort violation
19	R11_VIO	**Region 11 abort violation status to domain 6** 0: No region 11 abort violation 1: Region 11 abort violation
18	R10_VIO	**Region 10 abort violation status to domain 6** 0: No region 10 abort violation 1: Region 10 abort violation
17	R9_VIO	**Region 9 abort violation status to domain 6** 0: No region 9 abort violation 1: Region 9 abort violation
16	R8_VIO	**Region 8 abort violation status to domain 6** EMI will first record the unmasked device abort information at EMI_MPUS and EMI_MPUT if unmasked and set up the corresponding R8_VIO status bit. Clear R8_VIO for EMI to record the next violation status. When multiple violations occur, the corresponding D0_VIO_STA status bit will be set. However, only the device abort information will be recorded at VIO_DBGx, and its content will not be changed until the software clears it. 0: No region 8 abort violation 1: Region 8 abort violation
15	R19_VIO	**Region 19 abort violation status to domain 0** 0: No region 19 abort violation 1: Region 19 abort violation
14	R18_VIO	**Region 18 abort violation status to domain 0** 0: No region 18 abort violation 1: Region 18 abort violation
13	R17_VIO	**Region 17 abort violation status to domain 0** 0: No region 17 abort violation 1: Region 17 abort violation
12	R16_VIO	**Region 16 abort violation status to domain 0** 0: No region 16 abort violation 1: Region 16 abort violation
9	OOR_VIO	**Out of range abort violation status to domain 6** 0: No out of range abort violation 1: Out of range abort violation
8	APB_VIO	**APB abort violation status to domain 6** Note: Accessing EMI_MPUR2 is allowed in the secure mode only when D6_SEC = 1. 0: No APB abort violation 1: APB abort violation
7	R7_VIO	**Region 7 abort violation status to domain 6** 0: No region 7 abort violation 1: Region 7 abort violation
6	R6_VIO	**Region 6 abort violation status to domain 6** 0: No region 6 abort violation 1: Region 6 abort violation
5	R5_VIO	**Region 5 abort violation status to domain 6** 0: No region 5 abort violation 1: Region 5 abort violation

Bit(s)	Name	Description
4	R4_VIO	**Region 4 abort violation status to domain 6** 0: No region 4 abort violation 1: Region 4 abort violation
3	R3_VIO	**Region 3 abort violation status to domain 6** 0: No region 3 abort violation 1: Region 3 abort violation
2	R2_VIO	**Region 2 abort violation status to domain 6** 0: No region 2 abort violation 1: Region 2 abort violation
1	R1_VIO	**Region 1 abort violation status to domain 6** 0: No region 1 abort violation 1: Region 1 abort violation
0	R0_VIO	**Region 0 abort violation status to domain 6** 0: No region 0 abort violation 1: Region 0 abort violation

10203320 EMI_MPUY2 Memory Protection Unit Control Registers Y 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					R23_VIO	R22_VIO	R21_VIO	R20_VIO	R15_VIO	R14_VIO	R13_VIO	R12_VIO	R11_VIO	R10_VIO	R9_VIO	R8_VIO
Type					W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R19_VIO	R18_VIO	R17_VIO	R16_VIO			OOR_VIO	APB_VIO	R7_VIO	R6_VIO	R5_VIO	R4_VIO	R3_VIO	R2_VIO	R1_VIO	R0_VIO
Type	W1C	W1C	W1C	W1C			W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27	R23_VIO	**Region 23 abort violation status to domain 7** 0: No region 7 abort violation 1: Region 7 abort violation
26	R22_VIO	**Region 22 abort violation status to domain 7** 0: No region 6 abort violation 1: Region 6 abort violation
25	R21_VIO	**Region 21 abort violation status to domain 7** 0: No region 5 abort violation 1: Region 5 abort violation
24	R20_VIO	**Region 20 abort violation status to domain 7** 0: No region 4 abort violation 1: Region 4 abort violation
23	R15_VIO	**Region 15 abort violation status to domain 7** 0: No region 15 abort violation 1: Region 15 abort violation
22	R14_VIO	**Region 14 abort violation status to domain 7** 0: No region 14 abort violation 1: Region 14 abort violation
21	R13_VIO	**Region 13 abort violation status to domain 7** 0: No region 13 abort violation 1: Region 13 abort violation
20	R12_VIO	**Region 12 abort violation status to domain 7** 0: No region 12 abort violation

Bit(s)	Name	Description
		1: Region 12 abort violation
19	R11_VIO	**Region 11 abort violation status to domain 7** 0: No region 11 abort violation 1: Region 11 abort violation
18	R10_VIO	**Region 10 abort violation status to domain 7** 0: No region 10 abort violation 1: Region 10 abort violation
17	R9_VIO	**Region 9 abort violation status to domain 7** 0: No region 9 abort violation 1: Region 9 abort violation
16	R8_VIO	**Region 8 abort violation status to domain 7** EMI will first record the unmasked device abort information at EMI_MPUS and EMI_MPUT if unmasked and set up the corresponding R8_VIO status bit. Clear R8_VIO for EMI to record the next violation status. When multiple violations occur, the corresponding D0_VIO_STA status bit will be set. However, only the device abort information will be recorded at VIO_DBGx, and its content will not be changed until the software clears it. 0: No region 8 abort violation 1: Region 8 abort violation
15	R19_VIO	**Region 19 abort violation status to domain 0** 0: No region 19 abort violation 1: Region 19 abort violation
14	R18_VIO	**Region 18 abort violation status to domain 0** 0: No region 18 abort violation 1: Region 18 abort violation
13	R17_VIO	**Region 17 abort violation status to domain 0** 0: No region 17 abort violation 1: Region 17 abort violation
12	R16_VIO	**Region 16 abort violation status to domain 0** 0: No region 16 abort violation 1: Region 16 abort violation
9	OOR_VIO	**Out of range abort violation status to domain 7** 0: No out of range abort violation 1: Out of range abort violation
8	APB_VIO	**APB abort violation status to domain 7** Note: Accessing EMI_MPUR2 is allowed in the secure mode only when D6_SEC = 1. 0: No APB abort violation 1: APB abort violation
7	R7_VIO	**Region 7 abort violation status to domain 7** 0: No region 7 abort violation 1: Region 7 abort violation
6	R6_VIO	**Region 6 abort violation status to domain 7** 0: No region 6 abort violation 1: Region 6 abort violation
5	R5_VIO	**Region 5 abort violation status to domain 7** 0: No region 5 abort violation 1: Region 5 abort violation
4	R4_VIO	**Region 4 abort violation status to domain 7** 0: No region 4 abort violation 1: Region 4 abort violation
3	R3_VIO	**Region 3 abort violation status to domain 7** 0: No region 3 abort violation 1: Region 3 abort violation
2	R2_VIO	**Region 2 abort violation status to domain 7**

Bit(s)	Name	Description
		0: No region 2 abort violation 1: Region 2 abort violation
1	R1_VIO	**Region 1 abort violation status to domain 7** 0: No region 1 abort violation 1: Region 1 abort violation
0	R0_VIO	**Region 0 abort violation status to domain 7** 0: No region 0 abort violation 1: Region 0 abort violation

10203400 EMI_BMEN **EMI Bus Monitor Control Registers** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL_TRANS_TYPE								SEL_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								BC_OVERRUN			BUS_MON_RW		IDLE_DIS	BUS_MON_STP	BUS_MON_PAUSE	BUS_MON_EN
Type								RO			RW		RW	RO	RW	RW
Reset								0			0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SEL_TRANS_TYPE	**Uses SEL_MASTER (EMI_BMEN[30:16]) to select transaction type to be recorded** The result can be read from EMI_TTYPE1. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL_TRANS_TYPE[3:0]: 0000 ~ 1111 1-beat ~ 16-beat SEL_TRANS_TYPE[6:4]: 000 ~ 100 1/2/4/8/16-byte SEL_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL_MASTER	**Monitors selected masters (master 0 ~ 7)** EMI_BMEN[16]: ARM 0 EMI_BMEN[17]: ARM 1 EMI_BMEN[18]: MM 1 EMI_BMEN[19]: MDMCU EMI_BMEN[20]: MDHW EMI_BMEN[21]: MM 0 EMI_BMEN[22]: Peripheral EMI_BMEN[23]: GPU
8	BC_OVERRUN	**Bus counter (BUSCYC_CNT, WORD_ALL_CNT, BUSY_CNT)**
5:4	BUS_MON_RW	**Bus monitor for read/write** 00: Monitor read/write transactions 01: Monitor only read transactions 10: Monitor only write transactions 11: Monitor read/write transactions
3	IDLE_DIS	1: EMI idle force to 0. When SW wants to clear bus monitor, set IDLE_DIS=1, BUS_MON_EN=0 and set IDLE_DIS=0.
2	BUS_MON_STP	**Pauses monitor circuit is stop**
1	BUS_MON_PAUSE	**Pauses monitor circuit** When SW configure this bit, SW should: 1. Turn off EMI and infra DCM, or 2. Dummy read DDR

Bit(s)	Name	Description
		0: Does not pause 1: Pause
0	BUS_MON_EN	**Enables monitor circuit** When disabled, all monitor counters will be cleared. When SW configure this bit, SW should: 1. Turn off EMI and infra DCM, or 2. Dummy read DDR 0: Disable 1: Enable

10203404 EMI_BSTP **EMI Bus Monitor Auto Stop Count** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUSCYC_STOP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUSCYC_STOP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUSCYC_STOP	**When bus cycle count equal CUSCYC_STOP, all counters will stop automatically.** If BUSCYC_STOP set to 0, the counter cannot be stopped automatically.

10203408 EMI_BCNT **EMI 3rd Double-word Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUSCYC_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUSCYC_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUSCYC_CNT	**Bus cycle counter** Keeps to the maximum when reached. This counter is counted by a DCM clock. Thus the absolute time referred to this counter will be affected under the idle mode, during which the EMI clock is gated.

10203410 EMI_TACT **EMI 4th Double-Word Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TRANS_ALL_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANS_ALL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TRANS_ALL_CNT	**Counter for transactions of all masters (master 0 ~ 6)** Keeps to the maximum when reached.

10203418 EMI_TSCT — EMI 3rd Double-word Counter of Selected Masters — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TRANS_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANS_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TRANS_CNT	**Counter for transactions of all masters (master 0 ~ master 6)** The first counter for transactions of selected masters (master 0 ~ 6). Will keep to the maximum when reached. It is also counter for EMI cycles and will keep to the maximum when reached.

10203420 EMI_WACT — EMI 4th Double-Word Counter of Selected Masters — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD_ALL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_ALL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD_ALL_CNT	**Counter for access amount (unit: double words, 8-byte) to EMI of all masters (master 0 ~ 6)** Keeps to the maximum when reached

10203428 EMI_WSCT — EMI 3rd Double-word Counter of Selected Masters — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD_CNT	**First counter for access amount (unit: double words, 8-byte) to EMI of selected masters (master 0 ~ 6)** Keeps to the maximum when reached.

10203430 EMI_BACT — EMI 4th Double-Word Counter of Selected Masters — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BAND_WORD_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BAND_WORD_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BAND_WORD_CNT	**Bandwidth counter for access amount (unit: double words, 16-byte) to EMI of selected masters (master 0 ~ 6)** Will keep to the maximum when reached. If the EMI clock and DRAM clock is 1:1, one EMI cycle will represent 8 bytes. If the EMI clock and DRAM clock is 1:2, one EMI cycle will represent 16 bytes.

10203438 EMI_BSCT — EMI 3rd Double-word Counter of Selected Masters — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OVERHEAD_WORD_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OVERHEAD_WORD_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	OVERHEAD_WORD_CNT	**Overhead counter for access amount (unit: double words, 8-byte) to EMI of selected masters (master 0 ~ 6)** Will keep to the maximum when reached. When the EMI clock and DRAM clock is 1:1, one EMI cycle will represent 8 bytes. When the EMI clock and DRAM clock is 1:2, one EMI cycle will represent 16 bytes.

Bit(s)	Name	Description

10203440 EMI_MSEL **EMI 4th Double-Word Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL3_TRANS_TYPE								SEL3_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL2_TRANS_TYPE								SEL2_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SEL3_TRANS_TYPE	**Uses SEL3_TRANS_TYPE + SEL3_MASTER (EMI_MSEL[31:16]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE3. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL3_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL3_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL3_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL3_MASTER	**Monitors the selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT3, EMI_WSCT3, EMI_TTYPE3)**
15:8	SEL2_TRANS_TYPE	**Uses SEL2_TRANS_TYPE + SEL2_MASTER (EMI_MSEL[15:0]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE2. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL2_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL2_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL2_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
7:0	SEL2_MASTER	**Monitors the selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT2, EMI_WSCT2, EMI_TTYPE2)**

10203448 EMI_TSCT2 **EMI 4th Double-Word Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TRANS2_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANS2_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TRANS2_CNT	**2nd counter for transactions of selected masters (master 0 ~ 6)**

Bit(s)	Name	Description
		Will keep to the maximum when reached.

10203450 EMI_TSCT3 **EMI 3rd Double-word Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TRANS3_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANS3_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TRANS3_CNT	**3rd counter for transactions of selected masters (master 0 ~ 6)** Will keep to the maximum when reached.

10203458 EMI_WSCT2 **EMI 4th Double-Word Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD2_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD2_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD2_CNT	**2nd counter for access amount (unit: double words, 8-byte) to EMI of selected masters (master 0 ~ 6)** Will keep to the maximum when reached.

10203460 EMI_WSCT3 **EMI 3rd Double-word Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD3_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD3_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
31:0	WORD3_CNT	**3rd counter for access amount (unit: double words, 8-byte) to EMI of selected masters (master 0 ~ 6)** Will keep to the maximum when reached.

10203464 EMI_WSCT4 **EMI 4th Double-Word Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD4_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD4_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD4_CNT	**4th counter for access amount (unit: double words, 8-byte) to EMI of selected masters (master 0 ~ 6)** Will keep to the maximum when reached.

10203468 EMI_MSEL2 **EMI Master Selection for 4th and 5th Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL5_TRANS_TYPE								SEL5_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL4_TRANS_TYPE								SEL4_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SEL5_TRANS_TYPE	**Uses SEL5_TRANS_TYPE + SEL5_MASTER (EMI_MSEL2[31:16]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE5. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL5_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL5_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL5_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL5_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT5, EMI_WSCT5, EMI_TTYPE5)**
15:8	SEL4_TRANS_TYPE	**Uses SEL4_TRANS_TYPE + SEL4_MASTER (EMI_MSEL2[15:0]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE4. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL4_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL4_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte

Bit(s)	Name	Description
7:0	SEL4_MASTER	SEL4_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR **Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT4, EMI_WSCT4, EMI_TTYPE4)**

10203470 EMI_MSEL3 EMI Master Selection for 6th and 7th Counters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL7_TRANS_TYPE								SEL7_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL6_TRANS_TYPE								SEL6_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SEL7_TRANS_TYPE	**Uses SEL7_TRANS_TYPE + SEL7_MASTER (EMI_MSEL3[31:16]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE7. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL7_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL7_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL7_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL7_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT7, EMI_WSCT7, EMI_TTYPE7)**
15:8	SEL6_TRANS_TYPE	**Uses SEL6_TRANS_TYPE + SEL6_MASTER (EMI_MSEL3[15:0]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE6. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL6_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL6_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL6_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
7:0	SEL6_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT6, EMI_WSCT6, EMI_TTYPE6)**

10203478 EMI_MSEL4 EMI Master Selection for 8th and 9th Counters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL9_TRANS_TYPE								SEL9_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL8_TRANS_TYPE								SEL8_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SEL9_TRANS_TYPE	**Uses SEL9_TRANS_TYPE + SEL9_MASTER (EMI_MSEL4[31:16]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE9. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL9_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL9_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL9_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL9_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT9, EMI_WSCT9, EMI_TTYPE9)**
15:8	SEL8_TRANS_TYPE	**Uses SEL8_TRANS_TYPE + SEL8_MASTER (EMI_MSEL4[15:0]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE8. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL8_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL8_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL8_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
7:0	SEL8_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT8, EMI_WSCT8, EMI_TTYPE8)**

10203480 EMI_MSEL5 EMI Master Selection for 10th and 11th Counters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL11_TRANS_TYPE								SEL11_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL10_TRANS_TYPE								SEL10_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SEL11_TRANS_TYPE	**Uses SEL11_TRANS_TYPE + SEL11_MASTER (EMI_MSEL5[31:16]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE11. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL11_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL11_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL11_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL11_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT11, EMI_WSCT11, EMI_TTYPE11)**
15:8	SEL10_TRANS_TYPE	**Uses SEL10_TRANS_TYPE + SEL10_MASTER (EMI_MSEL5[15:0]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE10. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL10_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat

Bit(s)	Name	Description
7:0	SEL10_MASTER	SEL10_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL10_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR **Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT10, EMI_WSCT10, EMI_TTYPE10)**

10203488 EMI_MSEL6 **EMI Master Selection for 12th and 13th Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL13_TRANS_TYPE								SEL13_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL12_TRANS_TYPE								SEL12_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SEL13_TRANS_TYPE	**Uses SEL13_TRANS_TYPE + SEL13_MASTER (EMI_MSEL6[31:16]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE13. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL13_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL13_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL13_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL13_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT13, EMI_WSCT13, EMI_TTYPE13)**
15:8	SEL12_TRANS_TYPE	**Uses SEL12_TRANS_TYPE + SEL12_MASTER (EMI_MSEL6[15:0]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE12. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL12_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL12_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL12_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
7:0	SEL12_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT12, EMI_WSCT12, EMI_TTYPE12)**

10203490 EMI_MSEL7 **EMI Master Selection for 14th and 15th Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL15_TRANS_TYPE								SEL15_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL14_TRANS_TYPE								SEL14_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SEL15_TRANS_TYPE	**Uses SEL15_TRANS_TYPE + SEL15_MASTER (EMI_MSEL7[31:16]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE15. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL15_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL15_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL15_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL15_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT15, EMI_WSCT15, EMI_TTYPE15)**
15:8	SEL14_TRANS_TYPE	**Uses SEL14_TRANS_TYPE + SEL14_MASTER (EMI_MSEL7[15:0]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE14. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL14_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL14_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL14_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
7:0	SEL14_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT14, EMI_WSCT14, EMI_TTYPE14)**

10203498 EMI_MSEL8 EMI Master Selection for 16th and 17th Counters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL17_TRANS_TYPE								SEL17_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL16_TRANS_TYPE								SEL16_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SEL17_TRANS_TYPE	**Uses SEL17_TRANS_TYPE + SEL17_MASTER (EMI_MSEL8[31:16]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE17. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL17_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL17_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL17_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL17_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT17, EMI_WSCT17, EMI_TTYPE17)**
15:8	SEL16_TRANS_TYPE	**Uses SEL16_TRANS_TYPE + SEL16_MASTER (EMI_MSEL8[15:0]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE16. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]).

Bit(s)	Name	Description
7:0	SEL16_MASTER	SEL16_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL16_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL16_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR **Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT16, EMI_WSCT16, EMI_TTYPE16)**

102034A0 EMI_MSEL9 **EMI Master Selection for 18th and 19th Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL19_TRANS_TYPE								SEL19_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL18_TRANS_TYPE								SEL18_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SEL19_TRANS_TYPE	**Uses SEL19_TRANS_TYPE + SEL19_MASTER (EMI_MSEL9[31:16]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE19. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL19_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL19_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL19_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL19_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT19, EMI_WSCT19, EMI_TTYPE19)**
15:8	SEL18_TRANS_TYPE	**Uses SEL18_TRANS_TYPE + SEL18_MASTER (EMI_MSEL9[15:0]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE18. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL18_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL18_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL18_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
7:0	SEL18_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT18, EMI_WSCT18, EMI_TTYPE18)**

102034A8 EMI_MSEL10 **EMI Master Selection for 20th and 21th Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL21_TRANS_TYPE								SEL21_MASTER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL20_TRANS_TYPE								SEL20_MASTER							
Type	RW								RW							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SEL21_TRANS_TYPE	**Uses SEL21_TRANS_TYPE + SEL21_MASTER (EMI_MSEL10[31:16]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE21. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL21_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL21_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL21_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
23:16	SEL21_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT21, EMI_WSCT21, EMI_TTYPE21)**
15:8	SEL20_TRANS_TYPE	**Uses SEL20_TRANS_TYPE + SEL20_MASTER (EMI_MSEL10[15:0]) to select the transaction type to be recorded** The result can be read from EMI_TTYPE20. The read/write transaction to be recorded is determined by BUS_MON_RW (EMI_BMEN[5:4]). SEL20_TRANS_TYPE[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat SEL20_TRANS_TYPE[6:4]: 000 ~ 100: 1/2/4/8/16-byte SEL20_TRANS_TYPE[7]: 0/1 Burst type: WRAP/INCR
7:0	SEL20_MASTER	**Monitors selected masters (master 0 ~ 6) for the second transaction/word/type counters (EMI_TSCT20, EMI_WSCT20, EMI_TTYPE20)**

102034B0 EMI_BMID0 — EMI ID Selection for 1- 2 Transaction Type Counters — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEL2_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEL1_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	SEL2_ID	ID selection 2
9:0	SEL1_ID	ID selection 1

102034B4 EMI_BMID1 — EMI ID Selection for 3- 4 Transaction Type Counters — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEL4_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEL3_ID									
Type							RW									

Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	SEL4_ID	ID selection 4
9:0	SEL3_ID	ID selection 3

102034B8 EMI_BMID2 — EMI ID Selection for 5- 6 Transaction Type Counters — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEL6_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEL5_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	SEL6_ID	ID selection 6
9:0	SEL5_ID	ID selection 5

102034BC EMI_BMID3 — EMI ID Selection for 7- 8 Transaction Type Counters — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEL8_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEL7_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	SEL8_ID	ID selection 8
9:0	SEL7_ID	ID selection 7

102034C0 EMI_BMID4 — EMI ID Selection for 9- 10 Transaction Type Counters — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEL10_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEL9_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	SEL10_ID	ID selection 10
9:0	SEL9_ID	ID selection 9

102034C4 EMI_BMID5 **EMI ID Selection for 11- 12 Transaction Type Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEL12_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEL11_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	SEL12_ID	ID selection 12
9:0	SEL11_ID	ID selection 11

102034C8 EMI_BMID6 **EMI ID Selection for 13- 14 Transaction Type Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEL14_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEL13_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	SEL14_ID	ID selection 14
9:0	SEL13_ID	ID selection 13

102034CC EMI_BMID7 **EMI ID Selection for 15- 16 Transaction Type Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEL16_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEL15_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	SEL16_ID	ID selection 16
9:0	SEL15_ID	ID selection 15

102034D0 EMI_BMID8 — EMI ID Selection for 17- 18 Transaction Type Counters — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEL18_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEL17_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	SEL18_ID	ID selection 18
9:0	SEL17_ID	ID selection 17

102034D4 EMI_BMID9 — EMI ID Selection for 19- 20 Transaction Type Counters — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SEL20_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEL19_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	SEL20_ID	ID selection 20
9:0	SEL19_ID	ID selection 19

102034D8 EMI_BMID10 — EMI ID Selection for 21 Transaction Type Counters — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEL21_ID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
9:0	SEL21_ID	ID selection 21

102034E0 EMI_BMEN1 **EMI ID Selection Enabling** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												HPRI_EN				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HPRI_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	HPRI_EN	Enables high-priority filter for selected masters

102034E8 EMI_BMEN2 **EMI ID Selection Enabling** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL_ ID_E N1				NON_ALIGN _CNT_SEL		BAN_LAT_C NT_SEL					SEL_ID_EN				
Type	RW				RW		RW					RW				
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL_ID_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	SEL_ID_EN1	**bit 0: Enable ID selection for WSCT/TSCT counter (use 1st ID selection)** bit 1: Enable ID selection for WSCT2/TSCT2 counter (use 2nd ID selection) bit 2: Enable ID selection for WSCT3/TSCT3 counter (use 3rd ID selection) bit 3: Enable ID selection for WSCT4 counter (use 4th ID selection)
27:26	NON_ALIGN_CNT_SEL	**All counters for non-32B aligned or cross channel traffic except for bus cycle count and trans_all count** 00: Normal counter 01: Only count cross 32B transcation 10: Ony count cross channel
25:24	BAN_LAT_CNT_SEL	**Enables tType count used for bank usage count/Latency count enabling** 00: Type counter 01/11: ttType1-- ttype8 and ttype9 -- ttype16 changes as bank usage count 10: tTtype1 -- ttype7 changes as total latencies for m0 -- m6, and ttype9 -- ttype15 changes as total transaction counts for m0 -- m6
20:0	SEL_ID_EN	**21'h0: No ID selection for 21 type counters** 21'h1: Enable ID selection for type counter 1 21'h2: Enable ID selection for type counter 2 21'h4: Enable ID selection for type counter 3 ...

Bit(s)	Name	Description
		21'h100000: Enable ID selection for type counter 21.

102034F8 EMI_BMRW0 — **EMI ID Selection High Bit for 1-16 Transaction Type Counters** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEL16_RW		SEL15_RW		SEL14_RW		SEL13_RW		SEL12_RW		SEL11_RW		SEL10_RW		SEL9_RW	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEL8_RW		SEL7_RW		SEL6_RW		SEL5_RW		SEL4_RW		SEL3_RW		SEL2_RW		SEL1_RW	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	SEL16_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
29:28	SEL15_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
27:26	SEL14_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
25:24	SEL13_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
23:22	SEL12_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
21:20	SEL11_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
19:18	SEL10_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
17:16	SEL9_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
15:14	SEL8_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
13:12	SEL7_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only

Bit(s)	Name	Description
		11: Monitor read and write transaction
11:10	SEL6_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
9:8	SEL5_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
7:6	SEL4_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
5:4	SEL3_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
3:2	SEL2_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
1:0	SEL1_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Reserved 11: Monitor read and write transaction

102034FC EMI_BMRW1 **EMI ID Selection High Bit for 1-16 Transaction Type Counters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**SEL21_RW**		**SEL20_RW**		**SEL19_RW**		**SEL18_RW**		**SEL17_RW**	
Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:8	SEL21_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
7:6	SEL20_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
5:4	SEL19_RW	00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction
3:2	SEL18_RW	00: Follow EMI_BMEN[5:4] setting

Bit(s)	Name	Description
1:0	SEL17_RW	01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction 00: Follow EMI_BMEN[5:4] setting 01: Monitor read transaction only 10: Monitor write transaction only 11: Monitor read and write transaction

10203500 EMI_TTYPE1 **EMI 1st Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE1_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE1_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE1_CNT	**1st counter for number of a transaction type of selected masters (SEL_TRANS_TYPE + SEL_MASTER) (EMI_BMEN[31:16])** Will keep to the maximum when reached.

10203508 EMI_TTYPE2 **EMI 2nd Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE2_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE2_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE2_CNT	**2nd counter for number of a transaction type of selected masters (SEL2_TRANS_TYPE + SEL2_MASTER) (EMI_MSEL[15:0])** Will keep to the maximum when reached.

10203510 EMI_TTYPE3 **EMI 3rd Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE3_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE3_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE3_CNT	**3rd counter for number of a transaction type of selected masters (SEL3_TRANS_TYPE + SEL3_MASTER) (EMI_MSEL[31:16])** Will keep to the maximum when reached.

10203518 EMI_TTYPE4 **EMI 4th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE4_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE4_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE4_CNT	**4th counter for number of a transaction type of selected masters (SEL4_TRANS_TYPE + SEL4_MASTER) (EMI_MSEL2[15:0])** Will keep to the maximum when reached.

10203520 EMI_TTYPE5 **EMI 5th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE5_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE5_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE5_CNT	**5th counter for number of a transaction type of selected masters (SEL5_TRANS_TYPE + SEL5_MASTER) (EMI_MSEL2 [31:16])** Will keep to the maximum when reached.

10203528 EMI_TTYPE6 **EMI 6th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE6_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE6_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE6_CNT	**6th counter for number of a transaction type of selected masters (SEL6_TRANS_TYPE + SEL6_MASTER) (EMI_MSEL3[15:0])** Will keep to the maximum when reached.

10203530 EMI_TTYPE7 EMI 7th Transaction Type Counter of Selected Masters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE7_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE7_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE7_CNT	**7th counter for number of a transaction type of selected masters (SEL7_TRANS_TYPE + SEL7_MASTER) (EMI_MSEL3[31:16])** Will keep to the maximum when reached.

10203538 EMI_TTYPE8 EMI 8th Transaction Type Counter of Selected Masters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE8_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE8_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE8_CNT	**8th counter for number of a transaction type of selected masters (SEL8_TRANS_TYPE + SEL8_MASTER) (EMI_MSEL4[15:0])** Will keep to the maximum when reached.

10203540 EMI_TTYPE9 EMI 9th Transaction Type Counter of Selected Masters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE9_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE9_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE9_CNT	**9th counter for number of a transaction type of selected masters (SEL9_TRANS_TYPE + SEL9_MASTER) (EMI_MSEL4[31:16])** Will keep to the maximum when reached.

10203548 EMI_TTYPE1 **EMI 10th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE10_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE10_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE10_CNT	**10th counter for number of a transaction type of selected masters (SEL10_TRANS_TYPE + SEL10_MASTER) (EMI_MSEL5[15:0])** Will keep to the maximum when reached.

10203550 EMI_TTYPE11 **EMI 11th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE11_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE11_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE11_CNT	**11th counter for number of a transaction type of selected masters (SEL11_TRANS_TYPE + SEL11_MASTER) (EMI_MSEL5[31:16])** Will keep to the maximum when reached.

10203558 EMI_TTYPE12 **EMI 12th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE12_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE12_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE12_CNT	**12th counter for number of a transaction type of selected masters (SEL12_TRANS_TYPE + SEL12_MASTER) (EMI_MSEL6[15:0])** Will keep to the maximum when reached.

10203560 EMI_TTYPE13 **EMI 13th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE13_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE13_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE13_CNT	**13th counter for number of a transaction type of selected masters (SEL13_TRANS_TYPE + SEL13_MASTER) (EMI_MSEL6[31:16])** Will keep to the maximum when reached.

10203568 EMI_TTYPE14 **EMI 14th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE14_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE14_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE14_CNT	**14th counter for number of a transaction type of selected masters (SEL14_TRANS_TYPE + SEL14_MASTER) (EMI_MSEL7[15:0])** Will keep to the maximum when reached.

Bit(s)	Name	Description

10203570 EMI_TTYPE15 **EMI 15th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE15_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE15_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE15_CNT	**15th counter for number of a transaction type of selected masters (SEL15_TRANS_TYPE + SEL15_MASTER) (EMI_MSEL7[31:16])** Will keep to the maximum when reached.

10203578 EMI_TTYPE16 **EMI 16th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE16_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE16_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE16_CNT	**16th counter for number of a transaction type of selected masters (SEL16_TRANS_TYPE + SEL16_MASTER) (EMI_MSEL8[15:0])** Will keep to the maximum when reached.

10203580 EMI_TTYPE17 **EMI 17th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE17_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE17_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
31:0	TTYPE17_CNT	**17th counter for number of a transaction type of selected masters (SEL17_TRANS_TYPE + SEL17_MASTER) (EMI_MSEL8[31:16])** Will keep to the maximum when reached.

10203588 EMI_TTYPE18 **EMI 18th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE18_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE18_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE18_CNT	**18th counter for number of a transaction type of selected masters (SEL18_TRANS_TYPE + SEL18_MASTER) (EMI_MSEL9[15:0])** Will keep to the maximum when reached.

10203590 EMI_TTYPE19 **EMI 19th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE19_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE19_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE19_CNT	**19th counter for number of a transaction type of selected masters (SEL19_TRANS_TYPE + SEL19_MASTER) (EMI_MSEL9[31:16])** Will keep to the maximum when reached.

10203598 EMI_TTYPE20 **EMI 20th Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE20_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE20_CNT															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE20_CNT	**20th counter for number of a transaction type of selected masters (SEL20_TRANS_TYPE + SEL20_MASTER) (EMI_MSEL10[15:0])** Will keep to the maximum when reached.

102035A0 EMI_TTYPE21 **EMI 21st Transaction Type Counter of Selected Masters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TTYPE21_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TTYPE21_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TTYPE21_CNT	**21st counter for number of a transaction type of selected masters (SEL21_TRANS_TYPE + SEL21_MASTER) (EMI_MSEL10[31:16])** Will keep to the maximum when reached.

102035C0 EMI_EX_CON **Exclusive Monitor Status Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												EX_SEL				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	EX_SEL	Selects EX monitor number

102035C8 EMI_EX_ST0 **Exclusive Monitor Status Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EX_HIT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EX_USED															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	EX_HIT	Exclusive monitor fail
15:0	EX_USED	Exclusive monitor used

102035D0 EMI_EX_ST1 Exclusive Monitor Status Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EX_ADR_LAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EX_ADR_LAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EX_ADR_LAT	**Exclusive monitor address** When ser EX_SEL register, EMI latch selected monitor address

102035D8 EMI_EX_ST2 Exclusive Monitor Status Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															EX_FAIl_LAT	EX_USED_LAT
Type															RO	RO
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EX_ID_LAT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	EX_FAIl_LAT	**Exclusive monitor fail** When ser EX_SEL register, EMI latch selected monitor fail status
16	EX_USED_LAT	**Exclusive monitor used** When ser EX_SEL register, EMI latch selected monitor used status.
15:0	EX_ID_LAT	Exclusive monitor ID When ser EX_SEL register, EMI latch selected monitor ID

102035E0 EMI_WP_ADR Watch Point Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EMI_WP_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	EMI_WP_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EMI_WP_ADR	Watch point address

102035E8 EMI_WP_CTRL **Watch Point Range** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WP_INT_EN	NON_ALIGN_CHK_INT_EN	LOCK_CHK_INT_EN	ADR_CHK_INT_EN		EMI_WP_SLVERR	WP_WR_DIS	WP_RD_DIS	EMI_WP_TYPE		EMI_WP_RANGE					
Type	RW	RW	RW	RW		RW	RW	RW	RW		RW					
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	WP_INT_EN	**Enables watch point hit interrupt**
14	NON_ALIGN_CHK_INT_EN	**Enables AXI non-32B aligned check interrupt**
13	LOCK_CHK_INT_EN	**Enables AXI Lock command issue check interrupt**
12	ADR_CHK_INT_EN	**Enables AXI address violation (corss 4KB boundary) interrupt**
10	EMI_WP_SLVERR	**Watch point hit return slave error**
9	WP_WR_DIS	**Write hit watch point** EMI does not write data to DRAM.
8	WP_RD_DIS	**Read hit watch point** EMI does not read data from DRAMC and return 0 to master.
7:6	EMI_WP_TYPE	**Watch point read/write check** 11: Check read and write 01: Check read only 10: Check write only
5:0	EMI_WP_RANGE	**Watch point range** 4: 16 byte range (check EMP_WP_ADR[31:4]) 5: 32 bytes range (check EMP_WP_ADR[31:5]) 6: 64 bytes range (check EMP_WP_ADR[31:6]) ... 32: 4G byte range Others: Illegal

102035F0 EMI_CHKER **EMI AXI Checker** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WP_HIT	AXI_NON_ALIGN_ISSUE	AXI_Lock_issue	AXI_ADR_VIO	AXI_VIO_WR			VIO_CLR	NON_ALIGN_CHK_MST				WP_EN	NON_ALIGN_CHK_EN	LOCK_CHK_EN	ADR_CHK_EN
Type	RO	RO	RO	RO	RO			W1C	RW				RW	RW	RW	RW

Reset	0	0	0	0	0			0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AXI_VIO_ID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	WP_HIT	**AXI hit watch point range**
30	AXI_NON_ALIGN_ISSUE	**AXI non-aligned command issue**
29	AXI_Lock_issue	**AXI lock command issue**
28	AXI_ADR_VIO	**AXI address violation (corss 4KB boundary)**
27	AXI_VIO_WR	**AXI violation (lock or corss 4KB boundary) access type** 0: Read 1: Write
24	VIO_CLR	**Clears violation informatiion (bit 29..16 and EMI_CHKER_ADR) to 0**
23:20	NON_ALIGN_CHK_MST	**AXI non-32B align check master number** 0~7: Port 0~7 8: All ports
19	WP_EN	**Enables watch point**
18	NON_ALIGN_CHK_EN	**AXI non-32B aligned check**
17	LOCK_CHK_EN	**Enables AXI Lock command issue checker**
16	ADR_CHK_EN	**Enables AXI address violation (corss 4KB boundary) checker**
15:0	AXI_VIO_ID	**AXI violation (lock or corss 4KB boundary) ID**

102035F4 EMI_CHKER_TYPE — EMI AXI Checker Type — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AXI_CHECKER_TYP							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	AXI_CHECKER_TYP	**[3:0]: 0000 ~ 1111: 1-beat ~ 16-beat** [6:4]: 000 ~ 100: 1/2/4/8/16-byte [7]: 0/1 Burst type: WRAP/INCR

102035F8 EMI_CHKER_ADR — EMI AXI Checker Address — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AXI_VIO_ADR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AXI_VIO_ADR															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AXI_VIO_ADR	AXI Lock command issue

10203700 EMI_EFF_MONA EMI Efficiency Monitor Control Register A 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EFF_MON_EN															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CYC_THR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	EFF_MON_EN	**Efficiency monitor enable control**
15:0	CYC_THR	**Cycle threshold for efficiency monitor** Efficiency monitor calculates the efficiency per 2^CYC_THR+1 cycles.

10203704 EMI_EFF_MONB EMI Efficiency Monitor Control Register B 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						ALL_FF_THR_CHK	WFF_THR_CHK	RFF_THR_CHK				ALL_FF_TH R				
Type						RW	RW	RW				RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					WFF_THR						RFF_THR					
Type					RW						RW					
Reset					0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
26	ALL_FF_THR_CHK	Checks used number for sum of read command buffer + write command buffer
25	WFF_THR_CHK	Checks used number for write command buffer
24	RFF_THR_CHK	Checks used number for read command buffer
20:16	ALL_FF_THR	If ALL_FF_THR_CHK is set, the bandwidth will be taken into consideration only when used read command buffer + used write command buffer are always >= WFF_THR in each 2^CYC_THR+1 cycles.
11:8	WFF_THR	If WFF_THR_CHK is set, the bandwidth will be taken into consideration only when used write command buffer is always >= WFF_THR in each 2^CYC_THR+1 cycles.
5:0	RFF_THR	If RFF_THR_CHK is set, the bandwidth will be taken into consideration only when used read command buffer is always >=

Bit(s)	Name	Description
		RFF_THR in each 2^CYC_THR+1 cycles.

10203708 EMI_EFF_MONC **EMI Efficiency Monitor Control Register C** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EFF_THR_CHK															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					EFF_THR											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	EFF_THR_CHK	Checks efficiecny
11:0	EFF_THR	If EFF_THR_CHK is set, the calculated efficiency per 2^CYC_THR+1 cycles will be taken into consideration only when it >= EFF_THR.

1020370C EMI_EFF_MOND **EMI Efficiency Monitor Control Register D** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OVERHEAD_THR_CHK															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					OVERHEAD_THR											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	OVERHEAD_THR_CHK	Checks overhead efficiecny
11:0	OVERHEAD_THR	If OVERHEAD_THR_CHK is set, the calculated overhead efficiency per 2^CYC_THR+1 cycles will be taken into consideration only when it >= OVERHEAD_EFF_THR.

10203710 EMI_EFF_MONE **EMI Efficiency Monitor Control Register E** **00000FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LOW_EFF_WFF_1ST							LOW_EFF_RFF_1ST				
Type					RO							RO				
Reset					0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name					LOW_EFF_1ST											
Type					RO											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:24	LOW_EFF_WFF_1ST	Average used write command buffer number at lowest efficiency value duration
20:16	LOW_EFF_RFF_1ST	Average used read command buffer number at lowest efficiency value duration
11:0	LOW_EFF_1ST	Lowest efficiency value after efficiency monitor is enabled

10203714 EMI_EFF_MONF EMI Efficiency Monitor Control Register F 00000FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LOW_EFF_WFF_2ND							LOW_EFF_RFF_2ND				
Type					RO							RO				
Reset					0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					LOW_EFF_2ND											
Type					RO											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:24	LOW_EFF_WFF_2ND	Average used write command buffer number at second lowest efficiency value duration
20:16	LOW_EFF_RFF_2ND	Average used read command buffer number at second lowest efficiency value duration
11:0	LOW_EFF_2ND	Second lowest efficiency value after efficiency monitor is enabled

10203718 EMI_EFF_MONG EMI Efficiency Monitor Control Register G 00000FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LOW_USED_EFF_WFF_1ST							LOW_USED_EFF_RFF_1ST				
Type					RO							RO				
Reset					0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					LOW_USED_EFF_1ST											
Type					RO											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:24	LOW_USED_EFF_WFF_1ST	Average used write command buffer number at lowest used efficiency value duration
20:16	LOW_USED_EFF_RFF_1ST	Average used read command buffer number at lowest used efficiency value duration
11:0	LOW_USED_EFF_1ST	Lowest used efficiency value (total efficiency - overhead efficiency) after efficiency monitor is enabled

1020371C EMI_EFF_MONH **EMI Efficiency Monitor Control Register H** **00000FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LOW_USED_EFF_WFF_2ND							LOW_USED_EFF_RFF_2ND				
Type					RO							RO				
Reset					0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					LOW_USED_EFF_2ND											
Type					RO											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:24	LOW_USED_EFF_WFF_2ND	Average used write command buffer number at second lowest used efficiency value duration
20:16	LOW_USED_EFF_RFF_2ND	Average used read command buffer number at second lowest used efficiency value duration
11:0	LOW_USED_EFF_2ND	Second lowest used efficiency value (total efficiency - overhead efficiency) after efficiency monitor is enabled

10203720 EMI_EFF_MONI **EMI Efficiency Monitor Control Register I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LAST__OVERHEAD_EFF											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					LAST_EFF											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	LAST__OVERHEAD_EFF	Last overhead efficiency value
11:0	LAST_EFF	Last efficiency value

10203724 EMI_EFF_MONJ **EMI Efficiency Monitor Control Register J** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													LAST_WFF			
Type													RO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												LAST_RFF				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
19:16	LAST_WFF	Average used write command buffer number at last efficiency value

Bit(s)	Name	Description
		duration
4:0	LAST_RFF	Average used read command buffer number at lastt efficiency value duration

10203728 EMI_EFF_MONK **EMI Efficiency Monitor Control Register K** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LAST__OVERHEAD_EFF											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					LAST_EFF											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	LAST__OVERHEAD_EFF	Second last overhead efficiency value
11:0	LAST_EFF	Second last efficiency value

1020372C EMI_EFF_MONL **EMI Efficiency Monitor Control Register L** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													LAST _WFF			
Type													RO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												LAST_RFF				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
19:16	LAST_WFF	Average used write command buffer number at second last efficiency value duration
4:0	LAST_RFF	Average used read command buffer number at second lastt efficiency value duration

10203730 EMI_EFF_MONM **EMI Efficiency Monitor Control Register M** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LAST__OVERHEAD_EFF											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					LAST_EFF											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	LAST__OVERHEAD_EFF	Third last overhead efficiency value
11:0	LAST_EFF	Third last efficiency value

10203734 EMI_EFF_MONN EMI Efficiency Monitor Control Register N 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													LAST_WFF			
Type													RO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												LAST_RFF				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
19:16	LAST_WFF	Average used write command buffer number at third last efficiency value duration
4:0	LAST_RFF	Average used read command buffer number at third lastt efficiency value duration

10203738 EMI_EFF_MONO EMI Efficiency Monitor Control Register O 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LAST__OVERHEAD_EFF											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					LAST_EFF											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	LAST__OVERHEAD_EFF	Fourth last overhead efficiency value
11:0	LAST_EFF	Fourth last efficiency value

1020373C EMI_EFF_MONP EMI Efficiency Monitor Control Register P 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													LAST_WFF			
Type													RO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												LAST_RFF				
Type												RO				

Reset												0	0	0	0	0

Bit(s)	Name	Description
19:16	LAST_WFF	Average used write command buffer number at fourth last efficiency value duration
4:0	LAST_RFF	Average used read command buffer number at fourth lastt efficiency value duration

1.6 AP_DMA

Module name: AP_DMA Base address: (+11000000h)

Address	Name	Width	Register Function
11000000	AP_DMA_GLOBAL_INT_FLAG	32	AP DMA Global Interrupt Flag Register
11000004	AP_DMA_GLOBAL_RST	32	AP DMA Reset Register
11000008	AP_DMA_GLOBAL_RUNNING_STATUS	32	AP DMA Global Running Status Register
1100000C	AP_DMA_GLOBAL_SLOW_DOWN	32	AP DMA AXI Slow Down Register
11000010	AP_DMA_GLOBAL_SEC_EN	32	AP DMA Security Enable Register
11000014	AP_DMA_GLOBAL_GSEC_EN	32	AP DMA Global Security Enable Register
11000018	AP_DMA_GLOBAL_VIO_DBG1	32	AP DMA Security Latch Address Register
1100001C	AP_DMA_GLOBAL_VIO_DBG0	32	AP DMA Global Security Abort Register
11000020	AP_DMA_HIF0_SEC_EN	32	AP HIF0 Security Enable Register
11000024	AP_DMA_I2C0_SEC_EN	32	AP I2C0 Security Enable Register
11000028	AP_DMA_I2C1_SEC_EN	32	AP I2C1 Security Enable Register
1100002C	AP_DMA_I2C2_SEC_EN	32	AP I2C2 Security Enable Register
11000030	AP_DMA_I2C3_SEC_EN	32	AP I2C3 Security Enable Register
11000034	AP_DMA_I2C4_SEC_EN	32	AP I2C4 Security Enable Register
11000038	AP_DMA_I2C5_SEC_EN	32	AP I2C5 Security Enable Register
1100003C	AP_DMA_I2C6_SEC_EN	32	AP I2C6 Security Enable Register
11000040	AP_DMA_I2C7_SEC_EN	32	AP I2C7 Security Enable Register
11000044	AP_DMA_I2C8_SEC_EN	32	AP I2C8 Security Enable Register
11000048	AP_DMA_I2C9_SEC_EN	32	AP I2C9 Security Enable Register
1100004C	AP_DMA_UART0_TX_SEC_EN	32	AP UART0 TX Security Enable Register
11000050	AP_DMA_UART0_RX_SEC_EN	32	AP UART0 RX Security Enable Register
11000054	AP_DMA_UART1_TX_SEC_EN	32	AP UART1 TX Security Enable Register
11000058	AP_DMA_UART1_RX_SEC_EN	32	AP UART1 RX Security Enable Register
1100005C	AP_DMA_UART2_TX_SEC_EN	32	AP UART2 TX Security Enable Register
11000060	AP_DMA_UART2_RX_SEC_EN	32	AP UART2 RX Security Enable Register
11000064	AP_DMA_UART3_T	32	AP UART3 TX Security Enable Register

Address	Name	Width	Register Function
	X_SEC_EN		
11000068	AP_DMA_UART3_RX_SEC_EN	32	AP UART3 RX Security Enable Register
1100006C	AP_DMA_BTIF_0_TX_SEC_EN	32	AP BTIF TX Security Enable Register
11000070	AP_DMA_BTIF_0_RX_SEC_EN	32	AP BTIF0 RX Security Enable Register
11000074	AP_DMA_MD_INT_EN	32	AP DMA MD Interrupt Enable Register
11000080	AP_DMA_HIF_0_INT_FLAG	32	Peripheral DMA Interrupt Flag Register
11000084	AP_DMA_HIF_0_INT_EN	32	Peripheral DMA Interrupt Enable Register
11000088	AP_DMA_HIF_0_EN	32	Peripheral DMA Enable Register
1100008C	AP_DMA_HIF_0_RST	32	Peripheral DMA Reset Register
11000090	AP_DMA_HIF_0_STOP	32	Peripheral DMA Enable Register
11000094	AP_DMA_HIF_0_FLUSH	32	Peripheral DMA Flush Register
11000098	AP_DMA_HIF_0_CON	32	Peripheral DMA Control Register
1100009C	AP_DMA_HIF_0_SRC_ADDR	32	Peripheral DMA SRC Address Register
110000A0	AP_DMA_HIF_0_DST_ADDR	32	Peripheral DMA DST Address Register
110000A4	AP_DMA_HIF_0_LEN	32	Peripheral DMA Transfer Length Register
110000B8	AP_DMA_HIF_0_INT_BUF_SIZE	32	Peripheral DMA Internal Buffer Size Register
110000D0	AP_DMA_HIF_0_DEBUG_STATUS_00	32	Peripheral DMA Debug Status 00 Register
110000D4	AP_DMA_HIF_0_SRC_ADDR2	32	Peripheral DMA SRC Address Register
110000D8	AP_DMA_HIF_0_DST_ADDR2	32	Peripheral DMA DST Address Register
11000100	AP_DMA_I2C_0_INT_FLAG	32	Peripheral DMA Interrupt Flag Register
11000104	AP_DMA_I2C_0_INT_EN	32	Peripheral DMA Interrupt Enable Register
11000108	AP_DMA_I2C_0_EN	32	Peripheral DMA Enable Register
1100010C	AP_DMA_I2C_0_RST	32	Peripheral DMA Reset Register
11000110	AP_DMA_I2C_0_STOP	32	Peripheral DMA Enable Register
11000114	AP_DMA_I2C_0_FLUSH	32	Peripheral DMA Flush Register
11000118	AP_DMA_I2C_0_CON	32	Peripheral DMA Control Register
1100011C	AP_DMA_I2C_0_TX_MEM_ADDR	32	Peripheral DMA Memory Address Register
11000120	AP_DMA_I2C_0_RX_MEM_ADDR	32	Peripheral DMA Memory Address Register

Address	Name	Width	Register Function
11000124	AP_DMA_I2C_0_TX_LEN	32	Peripheral DMA Transfer Length Register
11000128	AP_DMA_I2C_0_RX_LEN	32	Peripheral DMA Transfer Length Register
11000138	AP_DMA_I2C_0_INT_BUF_SIZE	32	Peripheral DMA Internal Buffer Size Register
11000150	AP_DMA_I2C_0_DEBUG_STATUS_00	32	Peripheral DMA Debug Status 00 Register
11000154	AP_DMA_I2C_0_TX_MEM_ADDR2	32	Peripheral DMA Memory Address Register
11000158	AP_DMA_I2C_0_RX_MEM_ADDR2	32	Peripheral DMA Memory Address Register
11000180	AP_DMA_I2C_1_INT_FLAG	32	Peripheral DMA Interrupt Flag Register
11000184	AP_DMA_I2C_1_INT_EN	32	Peripheral DMA Interrupt Enable Register
11000188	AP_DMA_I2C_1_EN	32	Peripheral DMA Enable Register
1100018C	AP_DMA_I2C_1_RST	32	Peripheral DMA Reset Register
11000190	AP_DMA_I2C_1_STOP	32	Peripheral DMA Enable Register
11000194	AP_DMA_I2C_1_FLUSH	32	Peripheral DMA Flush Register
11000198	AP_DMA_I2C_1_CON	32	Peripheral DMA Control Register
1100019C	AP_DMA_I2C_1_TX_MEM_ADDR	32	Peripheral DMA Memory Address Register
110001A0	AP_DMA_I2C_1_RX_MEM_ADDR	32	Peripheral DMA Memory Address Register
110001A4	AP_DMA_I2C_1_TX_LEN	32	Peripheral DMA Transfer Length Register
110001A8	AP_DMA_I2C_1_RX_LEN	32	Peripheral DMA Transfer Length Register
110001B8	AP_DMA_I2C_1_INT_BUF_SIZE	32	Peripheral DMA Internal Buffer Size Register
110001D0	AP_DMA_I2C_1_DEBUG_STATUS_00	32	Peripheral DMA Debug Status 00 Register
110001D4	AP_DMA_I2C_1_TX_MEM_ADDR2	32	Peripheral DMA Memory Address Register
110001D8	AP_DMA_I2C_1_RX_MEM_ADDR2	32	Peripheral DMA Memory Address Register
11000200	AP_DMA_I2C_2_INT_FLAG	32	Peripheral DMA Interrupt Flag Register
11000204	AP_DMA_I2C_2_INT_EN	32	Peripheral DMA Interrupt Enable Register
11000208	AP_DMA_I2C_2_EN	32	Peripheral DMA Enable Register
1100020C	AP_DMA_I2C_2_RST	32	Peripheral DMA Reset Register
11000210	AP_DMA_I2C_2_STOP	32	Peripheral DMA Enable Register
11000214	AP_DMA_I2C_2_FLUSH	32	Peripheral DMA Flush Register
11000218	AP_DMA_I2C_2_CON	32	Peripheral DMA Control Register

Address	Name	Width	Register Function
1100021C	AP_DMA_I2C_2_TX_MEM_ADDR	32	Peripheral DMA Memory Address Register
11000220	AP_DMA_I2C_2_RX_MEM_ADDR	32	Peripheral DMA Memory Address Register
11000224	AP_DMA_I2C_2_TX_LEN	32	Peripheral DMA Transfer Length Register
11000228	AP_DMA_I2C_2_RX_LEN	32	Peripheral DMA Transfer Length Register
11000238	AP_DMA_I2C_2_INT_BUF_SIZE	32	Peripheral DMA Internal Buffer Size Register
11000250	AP_DMA_I2C_2_DEBUG_STATUS_00	32	Peripheral DMA Debug Status 00 Register
11000254	AP_DMA_I2C_2_TX_MEM_ADDR2	32	Peripheral DMA Memory Address Register
11000258	AP_DMA_I2C_2_RX_MEM_ADDR2	32	Peripheral DMA Memory Address Register
11000280	AP_DMA_I2C_3_INT_FLAG	32	Peripheral DMA Interrupt Flag Register
11000284	AP_DMA_I2C_3_INT_EN	32	Peripheral DMA Interrupt Enable Register
11000288	AP_DMA_I2C_3_EN	32	Peripheral DMA Enable Register
1100028C	AP_DMA_I2C_3_RST	32	Peripheral DMA Reset Register
11000290	AP_DMA_I2C_3_STOP	32	Peripheral DMA Enable Register
11000294	AP_DMA_I2C_3_FLUSH	32	Peripheral DMA Flush Register
11000298	AP_DMA_I2C_3_CON	32	Peripheral DMA Control Register
1100029C	AP_DMA_I2C_3_TX_MEM_ADDR	32	Peripheral DMA Memory Address Register
110002A0	AP_DMA_I2C_3_RX_MEM_ADDR	32	Peripheral DMA Memory Address Register
110002A4	AP_DMA_I2C_3_TX_LEN	32	Peripheral DMA Transfer Length Register
110002A8	AP_DMA_I2C_3_RX_LEN	32	Peripheral DMA Transfer Length Register
110002B8	AP_DMA_I2C_3_INT_BUF_SIZE	32	Peripheral DMA Internal Buffer Size Register
110002D0	AP_DMA_I2C_3_DEBUG_STATUS_00	32	Peripheral DMA Debug Status 00 Register
110002D4	AP_DMA_I2C_3_TX_MEM_ADDR2	32	Peripheral DMA Memory Address Register
110002D8	AP_DMA_I2C_3_RX_MEM_ADDR2	32	Peripheral DMA Memory Address Register
11000300	AP_DMA_I2C_4_INT_FLAG	32	Peripheral DMA Interrupt Flag Register
11000304	AP_DMA_I2C_4_INT_EN	32	Peripheral DMA Interrupt Enable Register
11000308	AP_DMA_I2C_4_EN	32	Peripheral DMA Enable Register
1100030C	AP_DMA_I2C_4_RST	32	Peripheral DMA Reset Register
11000310	AP_DMA_I2C_4_STOP	32	Peripheral DMA Enable Register

Address	Name	Width	Register Function
11000314	AP_DMA_I2C_4_FLUSH	32	Peripheral DMA Flush Register
11000318	AP_DMA_I2C_4_CON	32	Peripheral DMA Control Register
1100031C	AP_DMA_I2C_4_TX_MEM_ADDR	32	Peripheral DMA Memory Address Register
11000320	AP_DMA_I2C_4_RX_MEM_ADDR	32	Peripheral DMA Memory Address Register
11000324	AP_DMA_I2C_4_TX_LEN	32	Peripheral DMA Transfer Length Register
11000328	AP_DMA_I2C_4_RX_LEN	32	Peripheral DMA Transfer Length Register
11000338	AP_DMA_I2C_4_INT_BUF_SIZE	32	Peripheral DMA Internal Buffer Size Register
11000350	AP_DMA_I2C_4_DEBUG_STATUS_00	32	Peripheral DMA Debug Status 00 Register
11000354	AP_DMA_I2C_4_TX_MEM_ADDR2	32	Peripheral DMA Memory Address Register
11000358	AP_DMA_I2C_4_RX_MEM_ADDR2	32	Peripheral DMA Memory Address Register
11000380	AP_DMA_I2C_5_INT_FLAG	32	Peripheral DMA Interrupt Flag Register
11000384	AP_DMA_I2C_5_INT_EN	32	Peripheral DMA Interrupt Enable Register
11000388	AP_DMA_I2C_5_EN	32	Peripheral DMA Enable Register
1100038C	AP_DMA_I2C_5_RST	32	Peripheral DMA Reset Register
11000390	AP_DMA_I2C_5_STOP	32	Peripheral DMA Enable Register
11000394	AP_DMA_I2C_5_FLUSH	32	Peripheral DMA Flush Register
11000398	AP_DMA_I2C_5_CON	32	Peripheral DMA Control Register
1100039C	AP_DMA_I2C_5_TX_MEM_ADDR	32	Peripheral DMA Memory Address Register
110003A0	AP_DMA_I2C_5_RX_MEM_ADDR	32	Peripheral DMA Memory Address Register
110003A4	AP_DMA_I2C_5_TX_LEN	32	Peripheral DMA Transfer Length Register
110003A8	AP_DMA_I2C_5_RX_LEN	32	Peripheral DMA Transfer Length Register
110003B8	AP_DMA_I2C_5_INT_BUF_SIZE	32	Peripheral DMA Internal Buffer Size Register
110003D0	AP_DMA_I2C_5_DEBUG_STATUS_00	32	Peripheral DMA Debug Status 00 Register
110003D4	AP_DMA_I2C_5_TX_MEM_ADDR2	32	Peripheral DMA Memory Address Register
110003D8	AP_DMA_I2C_5_RX_MEM_ADDR2	32	Peripheral DMA Memory Address Register
11000400	AP_DMA_I2C_6_INT_FLAG	32	Peripheral DMA Interrupt Flag Register
11000404	AP_DMA_I2C_6_INT_EN	32	Peripheral DMA Interrupt Enable Register
11000408	AP_DMA_I2C_6_EN	32	Peripheral DMA Enable Register

Address	Name	Width	Register Function
1100040C	AP_DMA_I2C_6_RST	32	Peripheral DMA Reset Register
11000410	AP_DMA_I2C_6_STOP	32	Peripheral DMA Enable Register
11000414	AP_DMA_I2C_6_FLUSH	32	Peripheral DMA Flush Register
11000418	AP_DMA_I2C_6_CON	32	Peripheral DMA Control Register
1100041C	AP_DMA_I2C_6_TX_MEM_ADDR	32	Peripheral DMA Memory Address Register
11000420	AP_DMA_I2C_6_RX_MEM_ADDR	32	Peripheral DMA Memory Address Register
11000424	AP_DMA_I2C_6_TX_LEN	32	Peripheral DMA Transfer Length Register
11000428	AP_DMA_I2C_6_RX_LEN	32	Peripheral DMA Transfer Length Register
11000438	AP_DMA_I2C_6_INT_BUF_SIZE	32	Peripheral DMA Internal Buffer Size Register
11000450	AP_DMA_I2C_6_DEBUG_STATUS_00	32	Peripheral DMA Debug Status 00 Register
11000454	AP_DMA_I2C_6_TX_MEM_ADDR2	32	Peripheral DMA Memory Address Register
11000458	AP_DMA_I2C_6_RX_MEM_ADDR2	32	Peripheral DMA Memory Address Register
11000480	AP_DMA_I2C_7_INT_FLAG	32	Peripheral DMA Interrupt Flag Register
11000484	AP_DMA_I2C_7_INT_EN	32	Peripheral DMA Interrupt Enable Register
11000488	AP_DMA_I2C_7_EN	32	Peripheral DMA Enable Register
1100048C	AP_DMA_I2C_7_RST	32	Peripheral DMA Reset Register
11000490	AP_DMA_I2C_7_STOP	32	Peripheral DMA Enable Register
11000494	AP_DMA_I2C_7_FLUSH	32	Peripheral DMA Flush Register
11000498	AP_DMA_I2C_7_CON	32	Peripheral DMA Control Register
1100049C	AP_DMA_I2C_7_TX_MEM_ADDR	32	Peripheral DMA Memory Address Register
110004A0	AP_DMA_I2C_7_RX_MEM_ADDR	32	Peripheral DMA Memory Address Register
110004A4	AP_DMA_I2C_7_TX_LEN	32	Peripheral DMA Transfer Length Register
110004A8	AP_DMA_I2C_7_RX_LEN	32	Peripheral DMA Transfer Length Register
110004B8	AP_DMA_I2C_7_INT_BUF_SIZE	32	Peripheral DMA Internal Buffer Size Register
110004D0	AP_DMA_I2C_7_DEBUG_STATUS_00	32	Peripheral DMA Debug Status 00 Register
110004D4	AP_DMA_I2C_7_TX_MEM_ADDR2	32	Peripheral DMA Memory Address Register
110004D8	AP_DMA_I2C_7_RX_MEM_ADDR2	32	Peripheral DMA Memory Address Register
11000500	AP_DMA_I2C_8_I	32	Peripheral DMA Interrupt Flag Register

Address	Name	Width	Register Function
	NT_FLAG		
11000504	AP_DMA_I2C_8_INT_EN	32	Peripheral DMA Interrupt Enable Register
11000508	AP_DMA_I2C_8_EN	32	Peripheral DMA Enable Register
1100050C	AP_DMA_I2C_8_RST	32	Peripheral DMA Reset Register
11000510	AP_DMA_I2C_8_STOP	32	Peripheral DMA Enable Register
11000514	AP_DMA_I2C_8_FLUSH	32	Peripheral DMA Flush Register
11000518	AP_DMA_I2C_8_CON	32	Peripheral DMA Control Register
1100051C	AP_DMA_I2C_8_TX_MEM_ADDR	32	Peripheral DMA Memory Address Register
11000520	AP_DMA_I2C_8_RX_MEM_ADDR	32	Peripheral DMA Memory Address Register
11000524	AP_DMA_I2C_8_TX_LEN	32	Peripheral DMA Transfer Length Register
11000528	AP_DMA_I2C_8_RX_LEN	32	Peripheral DMA Transfer Length Register
11000538	AP_DMA_I2C_8_INT_BUF_SIZE	32	Peripheral DMA Internal Buffer Size Register
11000550	AP_DMA_I2C_8_DEBUG_STATUS_00	32	Peripheral DMA Debug Status 00 Register
11000554	AP_DMA_I2C_8_TX_MEM_ADDR2	32	Peripheral DMA Memory Address Register
11000558	AP_DMA_I2C_8_RX_MEM_ADDR2	32	Peripheral DMA Memory Address Register
11000580	AP_DMA_I2C_9_INT_FLAG	32	Peripheral DMA Interrupt Flag Register
11000584	AP_DMA_I2C_9_INT_EN	32	Peripheral DMA Interrupt Enable Register
11000588	AP_DMA_I2C_9_EN	32	Peripheral DMA Enable Register
1100058C	AP_DMA_I2C_9_RST	32	Peripheral DMA Reset Register
11000590	AP_DMA_I2C_9_STOP	32	Peripheral DMA Enable Register
11000594	AP_DMA_I2C_9_FLUSH	32	Peripheral DMA Flush Register
11000598	AP_DMA_I2C_9_CON	32	Peripheral DMA Control Register
1100059C	AP_DMA_I2C_9_TX_MEM_ADDR	32	Peripheral DMA Memory Address Register
110005A0	AP_DMA_I2C_9_RX_MEM_ADDR	32	Peripheral DMA Memory Address Register
110005A4	AP_DMA_I2C_9_TX_LEN	32	Peripheral DMA Transfer Length Register
110005A8	AP_DMA_I2C_9_RX_LEN	32	Peripheral DMA Transfer Length Register
110005B8	AP_DMA_I2C_9_INT_BUF_SIZE	32	Peripheral DMA Internal Buffer Size Register
110005D0	AP_DMA_I2C_9_DEBUG_STATUS_00	32	Peripheral DMA Debug Status 00 Register
110005D4	AP_DMA_I2C_9_T	32	Peripheral DMA Memory Address Register

Address	Name	Width	Register Function
	X_MEM_ADDR2		
110005D8	AP_DMA_I2C_9_RX_MEM_ADDR2	32	Peripheral DMA Memory Address Register
11000600	AP_DMA_UART_0_TX_INT_FLAG	32	UART TX Virtual FIFO Interrupt Flag Register
11000604	AP_DMA_UART_0_TX_INT_EN	32	UART TX Virtual FIFO Interrupt Enable Register
11000608	AP_DMA_UART_0_TX_EN	32	UART TX Virtual FIFO Enable Register
1100060C	AP_DMA_UART_0_TX_RST	32	UART TX Virtual FIFO Reset Register
11000610	AP_DMA_UART_0_TX_STOP	32	UART TX Virtual FIFO Enable Register
11000614	AP_DMA_UART_0_TX_FLUSH	32	UART TX Virtual FIFO Flush Register
1100061C	AP_DMA_UART_0_TX_VFF_ADDR	32	UART TX Virtual FIFO Base Address Register
11000624	AP_DMA_UART_0_TX_VFF_LEN	32	UART TX Virtual FIFO Length Register
11000628	AP_DMA_UART_0_TX_VFF_THRE	32	UART TX Virtual FIFO Threshold Register
1100062C	AP_DMA_UART_0_TX_VFF_WPT	32	UART TX Virtual FIFO Write Pointer Register
11000630	AP_DMA_UART_0_TX_VFF_RPT	32	UART TX Virtual FIFO Read Pointer Register
11000638	AP_DMA_UART_0_TX_INT_BUF_SIZE	32	UART Tx Internal Buffer Size Register
1100063C	AP_DMA_UART_0_TX_VFF_VALID_SIZE	32	UART Tx Virtual FIFO Valid Size Register
11000640	AP_DMA_UART_0_TX_VFF_LEFT_SIZE	32	UART Tx Virtual FIFO Left Size Register
11000650	AP_DMA_UART_0_TX_DEBUG_STATUS_00	32	UART Tx Debug Status 00
11000654	AP_DMA_UART_0_TX_VFF_ADDR2	32	UART TX Virtual FIFO Base Address Register
11000658	AP_DMA_UART_0_TX_VFF_WPT_VALID	32	UART TX Virtual FIFO Write Pointer Register by HW Control
1100065C	AP_DMA_UART_0_TX_VFF_WPT_VALID2	32	UART TX Virtual FIFO Write Pointer Register by HW Control
11000660	AP_DMA_UART_0_TX_FLUSH_ACT	32	UART TX Virtual FIFO Flush Status Register
11000664	AP_DMA_UART_0_TX_HW_FLUSH	32	UART TX Virtual FIFO HW Flush Register
11000668	AP_DMA_UART_0_TX_VFF_WPT_REAL	32	UART TX Virtual FIFO Write Pointer Register Value
11000700	AP_DMA_UART_1_TX_INT_FLAG	32	UART TX Virtual FIFO Interrupt Flag Register
11000704	AP_DMA_UART_1_TX_INT_EN	32	UART TX Virtual FIFO Interrupt Enable Register
11000708	AP_DMA_UART_1_	32	UART TX Virtual FIFO Enable Register

Address	Name	Width	Register Function
	TX_EN		
1100070C	AP_DMA_UART_1_TX_RST	32	UART TX Virtual FIFO Reset Register
11000710	AP_DMA_UART_1_TX_STOP	32	UART TX Virtual FIFO Enable Register
11000714	AP_DMA_UART_1_TX_FLUSH	32	UART TX Virtual FIFO Flush Register
1100071C	AP_DMA_UART_1_TX_VFF_ADDR	32	UART TX Virtual FIFO Base Address Register
11000724	AP_DMA_UART_1_TX_VFF_LEN	32	UART TX Virtual FIFO Length Register
11000728	AP_DMA_UART_1_TX_VFF_THRE	32	UART TX Virtual FIFO Threshold Register
1100072C	AP_DMA_UART_1_TX_VFF_WPT	32	UART TX Virtual FIFO Write Pointer Register
11000730	AP_DMA_UART_1_TX_VFF_RPT	32	UART TX Virtual FIFO Read Pointer Register
11000738	AP_DMA_UART_1_TX_INT_BUF_SIZE	32	UART Tx Internal Buffer Size Register
1100073C	AP_DMA_UART_1_TX_VFF_VALID_SIZE	32	UART Tx Virtual FIFO Valid Size Register
11000740	AP_DMA_UART_1_TX_VFF_LEFT_SIZE	32	UART Tx Virtual FIFO Left Size Register
11000750	AP_DMA_UART_1_TX_DEBUG_STATUS_00	32	UART Tx Debug Status 00
11000754	AP_DMA_UART_1_TX_VFF_ADDR2	32	UART TX Virtual FIFO Base Address Register
11000758	AP_DMA_UART_1_TX_VFF_WPT_VALID	32	UART TX Virtual FIFO Write Pointer Register by HW Control
1100075C	AP_DMA_UART_1_TX_VFF_WPT_VALID2	32	UART TX Virtual FIFO Write Pointer Register by HW Control
11000760	AP_DMA_UART_1_TX_FLUSH_ACT	32	UART TX Virtual FIFO Flush Status Register
11000764	AP_DMA_UART_1_TX_HW_FLUSH	32	UART TX Virtual FIFO HW Flush Register
11000768	AP_DMA_UART_1_TX_VFF_WPT_REAL	32	UART TX Virtual FIFO Write Pointer Register Value
11000800	AP_DMA_UART_2_TX_INT_FLAG	32	UART TX Virtual FIFO Interrupt Flag Register
11000804	AP_DMA_UART_2_TX_INT_EN	32	UART TX Virtual FIFO Interrupt Enable Register
11000808	AP_DMA_UART_2_TX_EN	32	UART TX Virtual FIFO Enable Register
1100080C	AP_DMA_UART_2_TX_RST	32	UART TX Virtual FIFO Reset Register
11000810	AP_DMA_UART_2_TX_STOP	32	UART TX Virtual FIFO Enable Register
11000814	AP_DMA_UART_2_TX_FLUSH	32	UART TX Virtual FIFO Flush Register
1100081C	AP_DMA_UART_2	32	UART TX Virtual FIFO Base Address Register

Address	Name	Width	Register Function
	TX_VFF_ADDR		
11000824	AP_DMA_UART_2_TX_VFF_LEN	32	UART TX Virtual FIFO Length Register
11000828	AP_DMA_UART_2_TX_VFF_THRE	32	UART TX Virtual FIFO Threshold Register
1100082C	AP_DMA_UART_2_TX_VFF_WPT	32	UART TX Virtual FIFO Write Pointer Register
11000830	AP_DMA_UART_2_TX_VFF_RPT	32	UART TX Virtual FIFO Read Pointer Register
11000838	AP_DMA_UART_2_TX_INT_BUF_SIZE	32	UART Tx Internal Buffer Size Register
1100083C	AP_DMA_UART_2_TX_VFF_VALID_SIZE	32	UART Tx Virtual FIFO Valid Size Register
11000840	AP_DMA_UART_2_TX_VFF_LEFT_SIZE	32	UART Tx Virtual FIFO Left Size Register
11000850	AP_DMA_UART_2_TX_DEBUG_STATUS_00	32	UART Tx Debug Status 00
11000854	AP_DMA_UART_2_TX_VFF_ADDR2	32	UART TX Virtual FIFO Base Address Register
11000858	AP_DMA_UART_2_TX_VFF_WPT_VALID	32	UART TX Virtual FIFO Write Pointer Register by HW Control
1100085C	AP_DMA_UART_2_TX_VFF_WPT_VALID2	32	UART TX Virtual FIFO Write Pointer Register by HW Control
11000860	AP_DMA_UART_2_TX_FLUSH_ACT	32	UART TX Virtual FIFO Flush Status Register
11000864	AP_DMA_UART_2_TX_HW_FLUSH	32	UART TX Virtual FIFO HW Flush Register
11000868	AP_DMA_UART_2_TX_VFF_WPT_REAL	32	UART TX Virtual FIFO Write Pointer Register Value
11000900	AP_DMA_UART_3_TX_INT_FLAG	32	UART TX Virtual FIFO Interrupt Flag Register
11000904	AP_DMA_UART_3_TX_INT_EN	32	UART TX Virtual FIFO Interrupt Enable Register
11000908	AP_DMA_UART_3_TX_EN	32	UART TX Virtual FIFO Enable Register
1100090C	AP_DMA_UART_3_TX_RST	32	UART TX Virtual FIFO Reset Register
11000910	AP_DMA_UART_3_TX_STOP	32	UART TX Virtual FIFO Enable Register
11000914	AP_DMA_UART_3_TX_FLUSH	32	UART TX Virtual FIFO Flush Register
1100091C	AP_DMA_UART_3_TX_VFF_ADDR	32	UART TX Virtual FIFO Base Address Register
11000924	AP_DMA_UART_3_TX_VFF_LEN	32	UART TX Virtual FIFO Length Register
11000928	AP_DMA_UART_3_TX_VFF_THRE	32	UART TX Virtual FIFO Threshold Register
1100092C	AP_DMA_UART_3_TX_VFF_WPT	32	UART TX Virtual FIFO Write Pointer Register
11000930	AP_DMA_UART_3_	32	UART TX Virtual FIFO Read Pointer Register

Address	Name	Width	Register Function
	TX_VFF_RPT		
11000938	AP_DMA_UART_3_TX_INT_BUF_SIZE	32	UART Tx Internal Buffer Size Register
1100093C	AP_DMA_UART_3_TX_VFF_VALID_SIZE	32	UART Tx Virtual FIFO Valid Size Register
11000940	AP_DMA_UART_3_TX_VFF_LEFT_SIZE	32	UART Tx Virtual FIFO Left Size Register
11000950	AP_DMA_UART_3_TX_DEBUG_STATUS_00	32	UART Tx Debug Status 00
11000954	AP_DMA_UART_3_TX_VFF_ADDR2	32	UART TX Virtual FIFO Base Address Register
11000958	AP_DMA_UART_3_TX_VFF_WPT_VALID	32	UART TX Virtual FIFO Write Pointer Register by HW Control
1100095C	AP_DMA_UART_3_TX_VFF_WPT_VALID2	32	UART TX Virtual FIFO Write Pointer Register by HW Control
11000960	AP_DMA_UART_3_TX_FLUSH_ACT	32	UART TX Virtual FIFO Flush Status Register
11000964	AP_DMA_UART_3_TX_HW_FLUSH	32	UART TX Virtual FIFO HW Flush Register
11000968	AP_DMA_UART_3_TX_VFF_WPT_REAL	32	UART TX Virtual FIFO Write Pointer Register Value
11000A00	AP_DMA_BTIF_0_TX_INT_FLAG	32	BTIF TX Virtual FIFO Interrupt Flag Register
11000A04	AP_DMA_BTIF_0_TX_INT_EN	32	BTIF TX Virtual FIFO Interrupt Enable Register
11000A08	AP_DMA_BTIF_0_TX_EN	32	BTIF TX Virtual FIFO Enable Register
11000A0C	AP_DMA_BTIF_0_TX_RST	32	BTIF TX Virtual FIFO Reset Register
11000A10	AP_DMA_BTIF_0_TX_STOP	32	BTIF TX Virtual FIFO Enable Register
11000A14	AP_DMA_BTIF_0_TX_FLUSH	32	BTIF TX Virtual FIFO Flush Register
11000A1C	AP_DMA_BTIF_0_TX_VFF_ADDR	32	BTIF TX Virtual FIFO Base Address Register
11000A24	AP_DMA_BTIF_0_TX_VFF_LEN	32	BTIF TX Virtual FIFO Length Register
11000A28	AP_DMA_BTIF_0_TX_VFF_THRE	32	BTIF TX Virtual FIFO Threshold Register
11000A2C	AP_DMA_BTIF_0_TX_VFF_WPT	32	BTIF TX Virtual FIFO Write Pointer Register
11000A30	AP_DMA_BTIF_0_TX_VFF_RPT	32	BTIF TX Virtual FIFO Read Pointer Register
11000A38	AP_DMA_BTIF_0_TX_INT_BUF_SIZE	32	BTIF Tx Internal Buffer Size Register
11000A3C	AP_DMA_BTIF_0_TX_VFF_VALID_SIZE	32	BTIF Tx Virtual FIFO Valid Size Register
11000A40	AP_DMA_BTIF_0_TX_VFF_LEFT_SIZE	32	BTIF Tx Virtual FIFO Left Size Register

Address	Name	Width	Register Function
11000A50	AP_DMA_BTIF_0_TX_DEBUG_STATUS_00	32	BTIF Tx Debug Status 00
11000A54	AP_DMA_BTIF_0_TX_VFF_ADDR2	32	BTIF TX Virtual FIFO Base Address Register
11000A58	AP_DMA_BTIF_0_TX_VFF_WPT_VALID	32	BTIF TX Virtual FIFO Write Pointer Register by HW Control
11000A5C	AP_DMA_BTIF_0_TX_VFF_WPT_VALID2	32	BTIF TX Virtual FIFO Write Pointer Register by HW Control
11000A60	AP_DMA_BTIF_0_TX_FLUSH_ACT	32	BTIF TX Virtual FIFO Flush Status Register
11000A64	AP_DMA_BTIF_0_TX_HW_FLUSH	32	BTIF TX Virtual FIFO HW Flush Register
11000A68	AP_DMA_BTIF_0_TX_VFF_WPT_REAL	32	BTIF TX Virtual FIFO Write Pointer Register Value
11000680	AP_DMA_UART_0_RX_INT_FLAG	32	UART RX Virtual FIFO Interrupt Flag Register
11000684	AP_DMA_UART_0_RX_INT_EN	32	UART RX Virtual FIFO Interrupt Enable Register
11000688	AP_DMA_UART_0_RX_EN	32	UART RX Virtual FIFO Enable Register
1100068C	AP_DMA_UART_0_RX_RST	32	UART RX Virtual FIFO Reset Register
11000690	AP_DMA_UART_0_RX_STOP	32	UART RX Virtual FIFO Enable Register
11000694	AP_DMA_UART_0_RX_FLUSH	32	UART RX Virtual FIFO Flush Register
1100069C	AP_DMA_UART_0_RX_VFF_ADDR	32	UART RX Virtual FIFO Base Address Register
110006A4	AP_DMA_UART_0_RX_VFF_LEN	32	UART RX Virtual FIFO Length Register
110006A8	AP_DMA_UART_0_RX_VFF_THRE	32	UART RX Virtual FIFO Threshold Register
110006AC	AP_DMA_UART_0_RX_VFF_WPT	32	UART RX Virtual FIFO Write Pointer Register
110006B0	AP_DMA_UART_0_RX_VFF_RPT	32	UART RX Virtual FIFO Read Pointer Register
110006B4	AP_DMA_UART_0_RX_FLOW_CTRL_THRE	32	UART RX Virtual FIFO Flow Control Threshold
110006B8	AP_DMA_UART_0_RX_INT_BUF_SIZE	32	UART Rx Internal Buffer Size Register
110006BC	AP_DMA_UART_0_RX_VFF_VALID_SIZE	32	UART Rx Virtual FIFO Valid Size Register
110006C0	AP_DMA_UART_0_RX_VFF_LEFT_SIZE	32	UART Rx Virtual FIFO Left Size Register
110006D0	AP_DMA_UART_0_RX_DEBUG_STATUS_00	32	UART Rx Debug Status 00
110006D4	AP_DMA_UART_0_RX_VFF_ADDR2	32	UART RX Virtual FIFO Base Address Register

Address	Name	Width	Register Function
11000780	AP_DMA_UART_1_RX_INT_FLAG	32	UART RX Virtual FIFO Interrupt Flag Register
11000784	AP_DMA_UART_1_RX_INT_EN	32	UART RX Virtual FIFO Interrupt Enable Register
11000788	AP_DMA_UART_1_RX_EN	32	UART RX Virtual FIFO Enable Register
1100078C	AP_DMA_UART_1_RX_RST	32	UART RX Virtual FIFO Reset Register
11000790	AP_DMA_UART_1_RX_STOP	32	UART RX Virtual FIFO Enable Register
11000794	AP_DMA_UART_1_RX_FLUSH	32	UART RX Virtual FIFO Flush Register
1100079C	AP_DMA_UART_1_RX_VFF_ADDR	32	UART RX Virtual FIFO Base Address Register
110007A4	AP_DMA_UART_1_RX_VFF_LEN	32	UART RX Virtual FIFO Length Register
110007A8	AP_DMA_UART_1_RX_VFF_THRE	32	UART RX Virtual FIFO Threshold Register
110007AC	AP_DMA_UART_1_RX_VFF_WPT	32	UART RX Virtual FIFO Write Pointer Register
110007B0	AP_DMA_UART_1_RX_VFF_RPT	32	UART RX Virtual FIFO Read Pointer Register
110007B4	AP_DMA_UART_1_RX_FLOW_CTRL_THRE	32	UART RX Virtual FIFO Flow Control Threshold
110007B8	AP_DMA_UART_1_RX_INT_BUF_SIZE	32	UART Rx Internal Buffer Size Register
110007BC	AP_DMA_UART_1_RX_VFF_VALID_SIZE	32	UART Rx Virtual FIFO Valid Size Register
110007C0	AP_DMA_UART_1_RX_VFF_LEFT_SIZE	32	UART Rx Virtual FIFO Left Size Register
110007D0	AP_DMA_UART_1_RX_DEBUG_STATUS_00	32	UART Rx Debug Status 00
110007D4	AP_DMA_UART_1_RX_VFF_ADDR2	32	UART RX Virtual FIFO Base Address Register
11000880	AP_DMA_UART_2_RX_INT_FLAG	32	UART RX Virtual FIFO Interrupt Flag Register
11000884	AP_DMA_UART_2_RX_INT_EN	32	UART RX Virtual FIFO Interrupt Enable Register
11000888	AP_DMA_UART_2_RX_EN	32	UART RX Virtual FIFO Enable Register
1100088C	AP_DMA_UART_2_RX_RST	32	UART RX Virtual FIFO Reset Register
11000890	AP_DMA_UART_2_RX_STOP	32	UART RX Virtual FIFO Enable Register
11000894	AP_DMA_UART_2_RX_FLUSH	32	UART RX Virtual FIFO Flush Register
1100089C	AP_DMA_UART_2_RX_VFF_ADDR	32	UART RX Virtual FIFO Base Address Register
110008A4	AP_DMA_UART_2_RX_VFF_LEN	32	UART RX Virtual FIFO Length Register
110008A8	AP_DMA_UART_2_RX_VFF_THRE	32	UART RX Virtual FIFO Threshold Register

Address	Name	Width	Register Function
110008AC	AP_DMA_UART_2_RX_VFF_WPT	32	UART RX Virtual FIFO Write Pointer Register
110008B0	AP_DMA_UART_2_RX_VFF_RPT	32	UART RX Virtual FIFO Read Pointer Register
110008B4	AP_DMA_UART_2_RX_FLOW_CTRL_THRE	32	UART RX Virtual FIFO Flow Control Threshold
110008B8	AP_DMA_UART_2_RX_INT_BUF_SIZE	32	UART Rx Internal Buffer Size Register
110008BC	AP_DMA_UART_2_RX_VFF_VALID_SIZE	32	UART Rx Virtual FIFO Valid Size Register
110008C0	AP_DMA_UART_2_RX_VFF_LEFT_SIZE	32	UART Rx Virtual FIFO Left Size Register
110008D0	AP_DMA_UART_2_RX_DEBUG_STATUS_00	32	UART Rx Debug Status 00
110008D4	AP_DMA_UART_2_RX_VFF_ADDR2	32	UART RX Virtual FIFO Base Address Register
11000980	AP_DMA_UART_3_RX_INT_FLAG	32	UART RX Virtual FIFO Interrupt Flag Register
11000984	AP_DMA_UART_3_RX_INT_EN	32	UART RX Virtual FIFO Interrupt Enable Register
11000988	AP_DMA_UART_3_RX_EN	32	UART RX Virtual FIFO Enable Register
1100098C	AP_DMA_UART_3_RX_RST	32	UART RX Virtual FIFO Reset Register
11000990	AP_DMA_UART_3_RX_STOP	32	UART RX Virtual FIFO Enable Register
11000994	AP_DMA_UART_3_RX_FLUSH	32	UART RX Virtual FIFO Flush Register
1100099C	AP_DMA_UART_3_RX_VFF_ADDR	32	UART RX Virtual FIFO Base Address Register
110009A4	AP_DMA_UART_3_RX_VFF_LEN	32	UART RX Virtual FIFO Length Register
110009A8	AP_DMA_UART_3_RX_VFF_THRE	32	UART RX Virtual FIFO Threshold Register
110009AC	AP_DMA_UART_3_RX_VFF_WPT	32	UART RX Virtual FIFO Write Pointer Register
110009B0	AP_DMA_UART_3_RX_VFF_RPT	32	UART RX Virtual FIFO Read Pointer Register
110009B4	AP_DMA_UART_3_RX_FLOW_CTRL_THRE	32	UART RX Virtual FIFO Flow Control Threshold
110009B8	AP_DMA_UART_3_RX_INT_BUF_SIZE	32	UART Rx Internal Buffer Size Register
110009BC	AP_DMA_UART_3_RX_VFF_VALID_SIZE	32	UART Rx Virtual FIFO Valid Size Register
110009C0	AP_DMA_UART_3_RX_VFF_LEFT_SIZE	32	UART Rx Virtual FIFO Left Size Register
110009D0	AP_DMA_UART_3_RX_DEBUG_STATUS_00	32	UART Rx Debug Status 00
110009D4	AP_DMA_UART_3_	32	UART RX Virtual FIFO Base Address Register

Address	Name	Width	Register Function
	RX_VFF_ADDR2		
11000A80	AP_DMA_BTIF_0_RX_INT_FLAG	32	BTIF RX Virtual FIFO Interrupt Flag Register
11000A84	AP_DMA_BTIF_0_RX_INT_EN	32	BTIF RX Virtual FIFO Interrupt Enable Register
11000A88	AP_DMA_BTIF_0_RX_EN	32	BTIF RX Virtual FIFO Enable Register
11000A8C	AP_DMA_BTIF_0_RX_RST	32	BTIF RX Virtual FIFO Reset Register
11000A90	AP_DMA_BTIF_0_RX_STOP	32	BTIF RX Virtual FIFO Enable Register
11000A94	AP_DMA_BTIF_0_RX_FLUSH	32	BTIF RX Virtual FIFO Flush Register
11000A9C	AP_DMA_BTIF_0_RX_VFF_ADDR	32	BTIF RX Virtual FIFO Base Address Register
11000AA4	AP_DMA_BTIF_0_RX_VFF_LEN	32	BTIF RX Virtual FIFO Length Register
11000AA8	AP_DMA_BTIF_0_RX_VFF_THRE	32	BTIF RX Virtual FIFO Threshold Register
11000AAC	AP_DMA_BTIF_0_RX_VFF_WPT	32	BTIF RX Virtual FIFO Write Pointer Register
11000AB0	AP_DMA_BTIF_0_RX_VFF_RPT	32	BTIF RX Virtual FIFO Read Pointer Register
11000AB4	AP_DMA_BTIF_0_RX_FLOW_CTRL_THRE	32	BTIF RX Virtual FIFO Flow Control Threshold
11000AB8	AP_DMA_BTIF_0_RX_INT_BUF_SIZE	32	BTIF Rx Internal Buffer Size Register
11000ABC	AP_DMA_BTIF_0_RX_VFF_VALID_SIZE	32	BTIF Rx Virtual FIFO Valid Size Register
11000AC0	AP_DMA_BTIF_0_RX_VFF_LEFT_SIZE	32	BTIF Rx Virtual FIFO Left Size Register
11000AD0	AP_DMA_BTIF_0_RX_DEBUG_STATUS_00	32	BTIF Rx Debug Status 00
11000AD4	AP_DMA_BTIF_0_RX_VFF_ADDR2	32	BTIF RX Virtual FIFO Base Address Register

11000000 AP_DMA_GLOBAL_INT_FLAG AP DMA Global Interrupt Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												BTIF0_RX	BTIF0_TX	UART3_RX	UART3_TX	UART2_RX
Type												RO	RO	RO	RO	RO
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UART2_TX	UART1_RX	UART1_TX	UART0_RX	UART0_TX	I2C9	I2C8	I2C7	I2C6	I2C5	I2C4	I2C3	I2C2	I2C1	I2C0	HIF0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20	BTIF0_RX	
19	BTIF0_TX	
18	UART3_RX	
17	UART3_TX	
16	UART2_RX	
15	UART2_TX	
14	UART1_RX	
13	UART1_TX	
12	UART0_RX	
11	UART0_TX	
10	I2C9	
9	I2C8	
8	I2C7	
7	I2C6	
6	I2C5	
5	I2C4	
4	I2C3	
3	I2C2	
2	I2C1	
1	I2C0	
0	HIF0	

11000004 AP_DMA_GLOBAL_RST **AP DMA Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**General DMA hard reset (reset regardless of the current transaction)** SW sets hard_rst to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**General DMA warm reset (after the current transaction)** SW sets warm_rst to 1 and waits for all running statuses to become 0. SW then sets warm_rst back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000008 AP_DMA_GLOBAL_RUNNING_STATUS **AP DMA Global Running Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												BTIF0_RX	BTIF0_TX	UART3_RX	UART3_TX	UART2_RX

Type												RO	RO	RO	RO	RO
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UART2_TX	UART1_RX	UART1_TX	UART0_RX	UART0_TX	I2C9	I2C8	I2C7	I2C6	I2C5	I2C4	I2C3	I2C2	I2C1	I2C0	HIF0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20	BTIF0_RX	0: Idle 1: Running
19	BTIF0_TX	0: Idle 1: Running
18	UART3_RX	0: Idle 1: Running
17	UART3_TX	0: Idle 1: Running
16	UART2_RX	0: Idle 1: Running
15	UART2_TX	0: Idle 1: Running
14	UART1_RX	0: Idle 1: Running
13	UART1_TX	0: Idle 1: Running
12	UART0_RX	0: Idle 1: Running
11	UART0_TX	0: Idle 1: Running
10	I2C9	0: Idle 1: Running
9	I2C8	0: Idle 1: Running
8	I2C7	0: Idle 1: Running
7	I2C6	0: Idle 1: Running
6	I2C5	0: Idle 1: Running
5	I2C4	0: Idle 1: Running
4	I2C3	0: Idle 1: Running
3	I2C2	0: Idle 1: Running
2	I2C1	0: Idle 1: Running
1	I2C0	0: Idle 1: Running
0	HIF0	0: Idle 1: Running

1100000C AP_DMA_GLOBAL_SLOW_DOWN **AP DMA AXI Slow Down Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	W_SLOW_CNT															W_SLOW_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0						0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R_SLOW_CNT															R_SLOW_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0						0

Bit(s)	Name	Description
31:22	W_SLOW_CNT	**AXI write to external AXI slow-down counter (0~1023)** The number means cycle. 0: Wait for 0 cycle then issue request 1: Wait for 1 cycle then issue request
16	W_SLOW_EN	**Enables AXI write to external AXI slow-down** 0: Does not slow down 1: Slow down
15:6	R_SLOW_CNT	**AXI read from external AXI slow-down counter (0~1023)** The number means cycle. 0: Wait for 0 cycle then issue request 1: Wait for 1 cycle then issue request
0	R_SLOW_EN	**Enables ARM side AXI read from external AXI slow-down** 0: Does not slow down 1: Slow down

11000010 AP_DMA_GLOBAL_SEC_EN **AP DMA Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LOCK	DLOCK										BTIF0_RX	BTIF0_TX	UART3_RX	UART3_TX	UART2_RX
Type	RW	RW										RO	RO	RO	RO	RO
Reset	0	0										0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UART2_TX	UART1_RX	UART1_TX	UART0_RX	UART0_TX	I2C9	I2C8	I2C7	I2C6	I2C5	I2C4	I2C3	I2C2	I2C1	I2C0	HIF0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	LOCK	**Locks the secure bit** 0: Unlock channel secure bit write 1: Lock channel secure bit
30	DLOCK	**Locks the domain registers** 0: Unlock channel domain register write 1: Lock channel domain register write
20	BTIF0_RX	0: This channel is non-secure. 1: This channel is secure.
19	BTIF0_TX	0: This channel is non-secure. 1: This channel is secure.
18	UART3_RX	0: This channel is non-secure.

Bit(s)	Name	Description
		1: This channel is secure.
17	UART3_TX	0: This channel is non-secure. 1: This channel is secure.
16	UART2_RX	0: This channel is non-secure. 1: This channel is secure.
15	UART2_TX	0: This channel is non-secure. 1: This channel is secure.
14	UART1_RX	0: This channel is non-secure. 1: This channel is secure.
13	UART1_TX	0: This channel is non-secure. 1: This channel is secure.
12	UART0_RX	0: This channel is non-secure. 1: This channel is secure.
11	UART0_TX	0: This channel is non-secure. 1: This channel is secure.
10	I2C9	0: This channel is non-secure. 1: This channel is secure.
9	I2C8	0: This channel is non-secure. 1: This channel is secure.
8	I2C7	0: This channel is non-secure. 1: This channel is secure.
7	I2C6	0: This channel is non-secure. 1: This channel is secure.
6	I2C5	0: This channel is non-secure. 1: This channel is secure.
5	I2C4	0: This channel is non-secure. 1: This channel is secure.
4	I2C3	0: This channel is non-secure. 1: This channel is secure.
3	I2C2	0: This channel is non-secure. 1: This channel is secure.
2	I2C1	0: This channel is non-secure. 1: This channel is secure.
1	I2C0	0: This channel is non-secure. 1: This channel is secure.
0	HIF0	0: This channel is non-secure. 1: This channel is secure.

11000014 AP_DMA_GLOBAL_GSEC_EN AP DMA Global Security Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GLOCK															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																GSEC_EN
Type																RW
Reset																0

Bit(s)	Name	Description
31	GLOCK	**This base address is locked.**

Bit(s)	Name	Description
		0: Unlock 1: Lock
0	GSEC_EN	**Controls global security enabling** When this bit is set to 0, the overall channel will be treated as non-security channel. When the this bit is set to 1, the security property will depend on each channel's sec_en. 0: Disable 1: Enable

11000018 AP_DMA_GLOBAL_VIO_DBG1 **AP DMA Security Latch Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LAT_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LAT_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LAT_ADDR	When any non-secure transaction accesses DMA security zone and when R_VID or W_VID is not 1, DMA will latch this transaction's address.

1100001C AP_DMA_GLOBAL_VIO_DBG0 **AP DMA Global Security Abort Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLR															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31	CLR	**SW writes 1 to CLR to clear R_VID, W_VID and APB_ABORT to 0.** 0: Keep status 1: Clear status

11000020 AP_DMA_HIF0_SEC_EN **AP HIF0 Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name															ARCACHE_CFG	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWCACHE_CFG		ARUSER_CFG				AWUSER_CFG				DOMAIN_CFG			SEC_EN
Type			RW		RW				RW				RW			WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	ARCACHE_CFG	**Sets up arcache value**
13:12	AWCACHE_CFG	**Sets up awcache value**
11:8	ARUSER_CFG	**Sets up aruser value**
7:4	AWUSER_CFG	**Sets up awuser value**
3:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enabling** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000024 AP_DMA_I2C0_SEC_EN **AP I2C0 Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															ARCACHE_CFG	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWCACHE_CFG		ARUSER_CFG				AWUSER_CFG				DOMAIN_CFG			SEC_EN
Type			RW		RW				RW				RW			WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	ARCACHE_CFG	**Sets up arcache value**
13:12	AWCACHE_CFG	**Sets up awcache value**
11:8	ARUSER_CFG	**Sets up aruser value**
7:4	AWUSER_CFG	**Sets up awuser value**
3:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enabling** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000028 AP_DMA_I2C1_SEC_EN **AP I2C1 Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															ARCACHE_CFG	

Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWCACHE_CFG		ARUSER_CFG				AWUSER_CFG				DOMAIN_CFG			SEC_EN
Type			RW		RW				RW				RW			WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	ARCACHE_CFG	**Sets up arcache value**
13:12	AWCACHE_CFG	**Sets up awcache value**
11:8	ARUSER_CFG	**Sets up aruser value**
7:4	AWUSER_CFG	**Sets up awuser value**
3:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enabling** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

1100002C AP_DMA_I2C2_SEC_EN **AP I2C2 Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															ARCACHE_CFG	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWCACHE_CFG		ARUSER_CFG				AWUSER_CFG				DOMAIN_CFG			SEC_EN
Type			RW		RW				RW				RW			WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	ARCACHE_CFG	**Sets up arcache value**
13:12	AWCACHE_CFG	**Sets up awcache value**
11:8	ARUSER_CFG	**Sets up aruser value**
7:4	AWUSER_CFG	**Sets up awuser value**
3:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enabling** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000030 AP_DMA_I2C3_SEC_EN **AP I2C3 Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															ARCACHE_CFG	
Type															RW	
Reset															0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWCACHE_CFG		ARUSER_CFG				AWUSER_CFG				DOMAIN_CFG			SEC_EN
Type			RW		RW				RW				RW			WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	ARCACHE_CFG	**Sets up arcache value**
13:12	AWCACHE_CFG	**Sets up awcache value**
11:8	ARUSER_CFG	**Sets up aruser value**
7:4	AWUSER_CFG	**Sets up awuser value**
3:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enabling** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000034 AP_DMA_I2C4_SEC_EN **AP I2C4 Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															ARCACHE_CFG	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWCACHE_CFG		ARUSER_CFG				AWUSER_CFG				DOMAIN_CFG			SEC_EN
Type			RW		RW				RW				RW			WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	ARCACHE_CFG	**Sets up arcache value**
13:12	AWCACHE_CFG	**Sets up awcache value**
11:8	ARUSER_CFG	**Sets up aruser value**
7:4	AWUSER_CFG	**Sets up awuser value**
3:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enabling** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000038 AP_DMA_I2C5_SEC_EN **AP I2C5 Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															ARCACHE_CFG	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWCACHE_C		ARUSER_CFG				AWUSER_CFG				DOMAIN_CFG			SEC_

			FG													EN
Type			RW		RW				RW				RW			WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	ARCACHE_CFG	**Sets up arcache value**
13:12	AWCACHE_CFG	**Sets up awcache value**
11:8	ARUSER_CFG	**Sets up aruser value**
7:4	AWUSER_CFG	**Sets up awuser value**
3:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enabling** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

1100003C AP_DMA_I2C6_SEC_EN **AP I2C6 Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															ARCACHE_CFG	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWCACHE_CFG		ARUSER_CFG				AWUSER_CFG				DOMAIN_CFG			SEC_EN
Type			RW		RW				RW				RW			WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	ARCACHE_CFG	**Sets up arcache value**
13:12	AWCACHE_CFG	**Sets up awcache value**
11:8	ARUSER_CFG	**Sets up aruser value**
7:4	AWUSER_CFG	**Sets up awuser value**
3:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enabling** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000040 AP_DMA_I2C7_SEC_EN **AP I2C7 Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															ARCACHE_CFG	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWCACHE_CFG		ARUSER_CFG				AWUSER_CFG				DOMAIN_CFG			SEC_EN
Type			RW		RW				RW				RW			WO

Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	ARCACHE_CFG	**Sets up arcache value**
13:12	AWCACHE_CFG	**Sets up awcache value**
11:8	ARUSER_CFG	**Sets up aruser value**
7:4	AWUSER_CFG	**Sets up awuser value**
3:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enabling** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000044 AP_DMA_I2C8_SEC_EN **AP I2C8 Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															ARCACHE_CFG	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWCACHE_CFG		ARUSER_CFG				AWUSER_CFG				DOMAIN_CFG			SEC_EN
Type			RW		RW				RW				RW			WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	ARCACHE_CFG	**Sets up arcache value**
13:12	AWCACHE_CFG	**Sets up awcache value**
11:8	ARUSER_CFG	**Sets up aruser value**
7:4	AWUSER_CFG	**Sets up awuser value**
3:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enabling** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000048 AP_DMA_I2C9_SEC_EN **AP I2C9 Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															ARCACHE_CFG	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWCACHE_CFG		ARUSER_CFG				AWUSER_CFG				DOMAIN_CFG			SEC_EN
Type			RW		RW				RW				RW			WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	ARCACHE_CFG	**Sets up arcache value**
13:12	AWCACHE_CFG	**Sets up awcache value**
11:8	ARUSER_CFG	**Sets up aruser value**
7:4	AWUSER_CFG	**Sets up awuser value**
3:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enabling** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

1100004C AP_DMA_UART0_TX_SEC_EN **AP UART0 TX Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															ARCACHE_CFG	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWCACHE_CFG		ARUSER_CFG				AWUSER_CFG				DOMAIN_CFG			SEC_EN
Type			RW		RW				RW				RW			WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	ARCACHE_CFG	**Sets up arcache value**
13:12	AWCACHE_CFG	**Sets up awcache value**
11:8	ARUSER_CFG	**Sets up aruser value**
7:4	AWUSER_CFG	**Sets up awuser value**
3:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enabling** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000050 AP_DMA_UART0_RX_SEC_EN **AP UART0 RX Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															ARCACHE_CFG	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWCACHE_CFG		ARUSER_CFG				AWUSER_CFG				DOMAIN_CFG			SEC_EN
Type			RW		RW				RW				RW			WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	ARCACHE_CFG	**Sets up arcache value**
13:12	AWCACHE_CFG	**Sets up awcache value**
11:8	ARUSER_CFG	**Sets up aruser value**
7:4	AWUSER_CFG	**Sets up awuser value**
3:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enabling** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000054 AP_DMA_UART1_TX_SEC_EN AP UART1 TX Security Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															ARCACHE_CFG	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWCACHE_CFG		ARUSER_CFG				AWUSER_CFG				DOMAIN_CFG			SEC_EN
Type			RW		RW				RW				RW			WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	ARCACHE_CFG	**Sets up arcache value**
13:12	AWCACHE_CFG	**Sets up awcache value**
11:8	ARUSER_CFG	**Sets up aruser value**
7:4	AWUSER_CFG	**Sets up awuser value**
3:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enabling** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000058 AP_DMA_UART1_RX_SEC_EN AP UART1 RX Security Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															ARCACHE_CFG	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWCACHE_CFG		ARUSER_CFG				AWUSER_CFG				DOMAIN_CFG			SEC_EN
Type			RW		RW				RW				RW			WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	ARCACHE_CFG	**Sets up arcache value**
13:12	AWCACHE_CFG	**Sets up awcache value**
11:8	ARUSER_CFG	**Sets up aruser value**
7:4	AWUSER_CFG	**Sets up awuser value**
3:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enabling** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

1100005C AP_DMA_UART2_TX_SEC_EN AP UART2 TX Security Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															ARCACHE_CFG	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWCACHE_CFG		ARUSER_CFG				AWUSER_CFG				DOMAIN_CFG			SEC_EN
Type			RW		RW				RW				RW			WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	ARCACHE_CFG	**Sets up arcache value**
13:12	AWCACHE_CFG	**Sets up awcache value**
11:8	ARUSER_CFG	**Sets up aruser value**
7:4	AWUSER_CFG	**Sets up awuser value**
3:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enabling** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000060 AP_DMA_UART2_RX_SEC_EN AP UART2 RX Security Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															ARCACHE_CFG	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWCACHE_CFG		ARUSER_CFG				AWUSER_CFG				DOMAIN_CFG			SEC_EN
Type			RW		RW				RW				RW			WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	ARCACHE_CFG	**Sets up arcache value**
13:12	AWCACHE_CFG	**Sets up awcache value**
11:8	ARUSER_CFG	**Sets up aruser value**
7:4	AWUSER_CFG	**Sets up awuser value**
3:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enabling** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000064 AP_DMA_UART3_TX_SEC_EN **AP UART3 TX Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															ARCACHE_CFG	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWCACHE_CFG		ARUSER_CFG				AWUSER_CFG				DOMAIN_CFG			SEC_EN
Type			RW		RW				RW				RW			WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	ARCACHE_CFG	**Sets up arcache value**
13:12	AWCACHE_CFG	**Sets up awcache value**
11:8	ARUSER_CFG	**Sets up aruser value**
7:4	AWUSER_CFG	**Sets up awuser value**
3:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enabling** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000068 AP_DMA_UART3_RX_SEC_EN **AP UART3 RX Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															ARCACHE_CFG	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWCACHE_CFG		ARUSER_CFG				AWUSER_CFG				DOMAIN_CFG			SEC_EN
Type			RW		RW				RW				RW			WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	ARCACHE_CFG	**Sets up arcache value**
13:12	AWCACHE_CFG	**Sets up awcache value**
11:8	ARUSER_CFG	**Sets up aruser value**
7:4	AWUSER_CFG	**Sets up awuser value**
3:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enabling** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

1100006C AP_DMA_BTIF_0_TX_SEC_EN **AP BTIF TX Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															ARCACHE_CFG	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWCACHE_CFG		ARUSER_CFG				AWUSER_CFG				DOMAIN_CFG			SEC_EN
Type			RW		RW				RW				RW			WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	ARCACHE_CFG	**Sets up arcache value**
13:12	AWCACHE_CFG	**Sets up awcache value**
11:8	ARUSER_CFG	**Sets up aruser value**
7:4	AWUSER_CFG	**Sets up awuser value**
3:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enabling** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000070 AP_DMA_BTIF_0_RX_SEC_EN **AP BTIF0 RX Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															ARCACHE_CFG	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AWCACHE_CFG		ARUSER_CFG				AWUSER_CFG				DOMAIN_CFG			SEC_EN
Type			RW		RW				RW				RW			WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	ARCACHE_CFG	**Sets up arcache value**
13:12	AWCACHE_CFG	**Sets up awcache value**
11:8	ARUSER_CFG	**Sets up aruser value**
7:4	AWUSER_CFG	**Sets up awuser value**
3:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enabling** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000074 AP_DMA_MD_INT_EN AP DMA MD Interrupt Enable Register 801FFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MD_INT_EN											dcm_en_btifo_rx	dcm_en_btifo_tx	dcm_en_uart3_rx	dcm_en_uart3_tx	dcm_en_uart2_rx
Type	RW											RW	RW	RW	RW	RW
Reset	1											1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcm_en_uart2_tx	dcm_en_uart1_rx	dcm_en_uart1_tx	dcm_en_uart0_rx	dcm_en_uart0_tx	dcm_en_i2c9	dcm_en_i2c8	dcm_en_i2c7	dcm_en_i2c6	dcm_en_i2c5	dcm_en_i2c4	dcm_en_i2c3	dcm_en_i2c2	dcm_en_i2c1	dcm_en_i2c0	dcm_en_hifo
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	MD_INT_EN	0: Disable 1: Enable
20	dcm_en_btifo_rx	**BTIF0 RX** 0: Disable DCM 1: Enable DCM
19	dcm_en_btifo_tx	**BTIF0 TX** 0: Disable DCM 1: Enable DCM
18	dcm_en_uart3_rx	**UART3 RX** 0: Disable DCM 1: Enable DCM
17	dcm_en_uart3_tx	**UART3 TX** 0: Disable DCM 1: Enable DCM
16	dcm_en_uart2_rx	**UART2 RX** 0: Disable DCM 1: Enable DCM
15	dcm_en_uart2_tx	**UART2 TX** 0: Disable DCM 1: Enable DCM
14	dcm_en_uart1_rx	**UART1 RX** 0: Disable DCM 1: Enable DCM
13	dcm_en_uart1_tx	**UART1 TX** 0: Disable DCM 1: Enable DCM

Bit(s)	Name	Description
12	dcm_en_uart0_rx	**UART0 RX** 0: Disable DCM 1: Enable DCM
11	dcm_en_uart0_tx	**UART0 TX** 0: Disable DCM 1: Enable DCM
10	dcm_en_i2c9	**I2C9** 0: Disable DCM 1: Enable DCM
9	dcm_en_i2c8	**I2C8** 0: Disable DCM 1: Enable DCM
8	dcm_en_i2c7	**I2C7** 0: Disable DCM 1: Enable DCM
7	dcm_en_i2c6	**I2C6** 0: Disable DCM 1: Enable DCM
6	dcm_en_i2c5	**I2C5** 0: Disable DCM 1: Enable DCM
5	dcm_en_i2c4	**I2C4** 0: Disable DCM 1: Enable DCM
4	dcm_en_i2c3	**I2C3** 0: Disable DCM 1: Enable DCM
3	dcm_en_i2c2	**I2C2** 0: Disable DCM 1: Enable DCM
2	dcm_en_i2c1	**I2C1** 0: Disable DCM 1: Enable DCM
1	dcm_en_i2c0	**I2C0** 0: Disable DCM 1: Enable DCM
0	dcm_en_hif0	**HIF0** 0: Disable DCM 1: Enable DCM

11000080 AP_DMA_HIF_0_INT_FLAG **Peripheral DMA Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG_0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG_0	**This flag is raised when DMA is finished. Write 0 to clear it.** 1. After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 2. If STOP =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 3. If FLUSH =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

11000084 AP_DMA_HIF_0_INT_EN **Peripheral DMA Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN_FLAG_0
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN_FLAG_0	**Enables interrupt for FLAG_0** 0: Disable 1: Enable

11000088 AP_DMA_HIF_0_EN **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA when other control registers are set. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest

Bit(s)	Name	Description
		transaction is finished. 0: Disable 1: Enable

1100008C AP_DMA_HIF_0_RST **Peripheral DMA Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (reset regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000090 AP_DMA_HIF_0_STOP **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA** Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP back to 0 to finish the stop mechanism.

Bit(s)	Name	Description
		When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

11000094 AP_DMA_HIF_0_FLUSH **Peripheral DMA Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

11000098 AP_DMA_HIF_0_CON **Peripheral DMA Control Register** **80000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_INCR														BURST_LEN	
Type	RW														RW	
Reset	1														0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		SLOW_CNT												SLOW_EN	FIX_EN	DIR
Type		RW												RW	RW	RW
Reset		0	0	0	0	0	0	0	0	0	0			0	0	0

Bit(s)	Name	Description
31	INT_INCR	**DMA issues incremental burst or fixed burst bus command to peripheral side.** 0: fixed burst command 1: incremental burst command
17:16	BURST_LEN	**Peripheral DMA burst length** Valid value: 0~3

Bit(s)	Name	Description
		0: 1-4 1: 2-4 2: 3-4 3: 4-4
14:5	SLOW_CNT	**Peripheral DMA slow-down counter** Only the read side is slowed down; the overall throughput will also decrease. Supports up to 1,023 cycles. 0: 0 cycle 1: 1 cycle
2	SLOW_EN	**Enables general DMA slow-down** 0: Disable 1: Enable
1	FIX_EN	**Peripheral DMA fixed pattern** When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as TX. 0: Does not use fixed pattern 1: Use fixed pattern
0	DIR	0: TX 1: RX

1100009C AP_DMA_HIF_0_SRC_ADDR **Peripheral DMA SRC Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_ADDR	**Peripheral DMA destination address** It can be any byte alignment. When DIR=1 (Rx mode), src_addr equals the HIF FIFO address and must be 4-byte aligned. When FIX_EN = 1, SRC_ADDR will be treated as FIX_PATTERN. dir=1: HIF FIFO address dir=0: Memory address

110000A0 AP_DMA_HIF_0_DST_ADDR **Peripheral DMA DST Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DST_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DST_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DST_ADDR	**Peripheral DMA destination address** This address is the HIF FIFO address when in Tx (dir=0) mode or the memory address when in Rx (dir=1) mode. Do not set MEM_ADDR to be within the last 8 bytes before the 4KB boundary when you use SYSRAM as a Tx/Rx memory, e.g. 0xff9 ~ 0xfff is not allowed to be MEM_ADDR when you use SYSRAM as a Tx/Rx memory. dir=1: Memory address dir=0: HIF FIFO address

110000A4 AP_DMA_HIF_0_LEN **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													LEN			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

110000B8 AP_DMA_HIF_0_INT_BUF_SIZE **Peripheral DMA Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	Byte size in internal buffer

110000D0 AP_DMA_HIF_0_DEBUG_S **Peripheral DMA Debug Status 00 Register** **00000013**

TATUS_00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RADDR_D								WADDR_D_LH						
Type		RO								RO						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		WADDR_D							RAADDR_FIX_EN	WADDR_FIX_EN		R_CLR	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type		RO							RO	RO		RO	RO	RO	RO	RO
Reset		0	0	0	0	0	0	0	0	0		1	0	0	1	1

Bit(s)	Name	Description
30:24	RADDR_D	Read point in internal buffer
22:16	WADDR_D_LH	Write point latch in internal buffer
14:8	WADDR_D	Write point in internal buffer
7	RAADDR_FIX_EN	
6	WADDR_FIX_EN	
4	R_CLR	
3	WREQ	Write command request
2	RREQ	Read command request
1	W_Q_CLR	Write side command queue empty
0	R_Q_CLR	Read side command queue empty

110000D4 AP_DMA_HIF_0_SRC_ADDR2 **Peripheral DMA SRC Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SRC_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	SRC_ADDR2	**Peripheral DMA source address bit[32]** dir=1: HIF FIFO address bit[32] dir=0 : memory address bit[32]

110000D8 AP_DMA_HIF_0_DST_ADDR2 **Peripheral DMA DST Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DST_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	DST_ADDR2	**Peripheral DMA destination address bit[32]** dir=1: memory address bit[32] dir=0 : HIF FIFO address bit[32]

11000100 AP_DMA_I2C_0_INT_FLAG Peripheral DMA Interrupt Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FLAG_0	RX_FLAG	TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FLAG_0	**Raised when TX-to-RX is asserted when DMA engine is running.**
1	RX_FLAG	**Raised when RX DMA is finished. Write 0 to clear it.**
0	TX_FLAG	**This flag is raised when TX DMA is finished. Write 0 to clear it.** 1. After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 2. If STOP =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 3. If FLUSH =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

11000104 AP_DMA_I2C_0_INT_EN Peripheral DMA Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INTEN_FLAG_0	INTEN_RX_FLA	INTEN_TX_FLA

															G	G
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	INTEN_FLAG_0	**Enables interrupt for FLAG_0** 0: Disable 1: Enable
1	INTEN_RX_FLAG	**Enables interrupt for RX_FLAG** 0: Disable 1: Enable
0	INTEN_TX_FLAG	**Enables interrupt for TX_FLAG** 0: Disable 1: Enable

11000108 AP_DMA_I2C_0_EN Peripheral DMA Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1100010C AP_DMA_I2C_0_RST Peripheral DMA Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (reset regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000110 AP_DMA_I2C_0_STOP **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA** Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

11000114 AP_DMA_I2C_0_FLUSH **Peripheral DMA Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW

Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

11000118 AP_DMA_I2C_0_CON **Peripheral DMA Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FIX_EN	DIR
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	FIX_EN	**Peripheral DMA fixed pattern** When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as TX. 0: Does not use fixed pattern 1: Use fixed pattern
0	DIR	**Half duplex peripheral DMA direction** 0: TX 1: RX

1100011C AP_DMA_I2C_0_TX_MEM_ADDR **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MEM_ADDR	**Peripheral DMA memory address**

Bit(s)	Name	Description
		It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN = 1, TX_MEM_ADDR will be treated as FIX_PATTERN. Do not set TX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be TX_MEM_ADDR when you use SYSRAM as a source memory.

11000120 AP_DMA_I2C_0_RX_MEM_ADDR **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be RX_MEM_ADDR when you use SYSRAM as a destination memory.

11000124 AP_DMA_I2C_0_TX_LEN **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

11000128 AP_DMA_I2C **Peripheral DMA Transfer** **00000000**

_0_RX_LEN Length Register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

11000138 AP_DMA_I2C_0_INT_BUF_SIZE Peripheral DMA Internal Buffer Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	Byte size in internal buffer

11000150 AP_DMA_I2C_0_DEBUG_STATUS_00 Peripheral DMA Debug Status 00 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D										WD_ACT	RD_ACT	WREQ	RREQ		
Type	RO										RO	RO	RO	RO		
Reset	0	0	0	0	0	0	0	0			0	0	0	0		

Bit(s)	Name	Description
31:24	RADDR_D	Read point in internal buffer
23:16	WADDR_D_LH	Write point latch in internal buffer

Bit(s)	Name	Description
15:8	WADDR_D	Write point in internal buffer
5	WD_ACT	
4	RD_ACT	
3	WREQ	Write command request
2	RREQ	Read command request

11000154 AP_DMA_I2C_0_TX_MEM_ADDR2 Peripheral DMA Memory Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TX_MEM_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	TX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

11000158 AP_DMA_I2C_0_RX_MEM_ADDR2 Peripheral DMA Memory Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RX_MEM_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	RX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

11000180 AP_DMA_I2C_1_INT_FLAG Peripheral DMA Interrupt Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FLAG_0	RX_FLAG	TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FLAG_0	**Raised when TX-to-RX is asserted when DMA engine is running.**
1	RX_FLAG	**Raised when RX DMA is finished. Write 0 to clear it.**
0	TX_FLAG	**This flag is raised when TX DMA is finished. Write 0 to clear it.** 1. After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 2. If STOP =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 3. If FLUSH =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

11000184 AP_DMA_I2C_1_INT_EN **Peripheral DMA Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INTEN_FLAG_0	INTEN_RX_FLAG	INTEN_TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	INTEN_FLAG_0	**Enables interrupt for FLAG_0** 0: Disable 1: Enable
1	INTEN_RX_FLAG	**Enables interrupt for RX_FLAG** 0: Disable 1: Enable
0	INTEN_TX_FLAG	**Enables interrupt for TX_FLAG** 0: Disable 1: Enable

11000188 AP_DMA_I2C_1_EN **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1100018C AP_DMA_I2C_1_RST Peripheral DMA Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (reset regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000190 AP_DMA_I2C_1_STOP Peripheral DMA Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA** Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

11000194 AP_DMA_I2C_1_FLUSH **Peripheral DMA Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

11000198 AP_DMA_I2C_1_CON **Peripheral DMA Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FIX_EN	DIR
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	FIX_EN	**Peripheral DMA fixed pattern** When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as TX. 0: Does not use fixed pattern 1: Use fixed pattern
0	DIR	**Half duplex peripheral DMA direction** 0: TX 1: RX

1100019C AP_DMA_I2C_1_TX_MEM_ADDR **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN = 1, TX_MEM_ADDR will be treated as FIX_PATTERN. Do not set TX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be TX_MEM_ADDR when you use SYSRAM as a source memory.

110001A0 AP_DMA_I2C_1_RX_MEM_ADDR **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
31:0	RX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be RX_MEM_ADDR when you use SYSRAM as a destination memory.

110001A4 AP_DMA_I2C_1_TX_LEN **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

110001A8 AP_DMA_I2C_1_RX_LEN **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

110001B8 AP_DMA_I2C_1_INT_BUF **Peripheral DMA Internal Buffer Size Register** **00000000**

_SIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	Byte size in internal buffer

110001D0 AP_DMA_I2C_1_DEBUG_STATUS_00 **Peripheral DMA Debug Status 00 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D										WD_ACT	RD_ACT	WREQ	RREQ		
Type	RO										RO	RO	RO	RO		
Reset	0	0	0	0	0	0	0	0			0	0	0	0		

Bit(s)	Name	Description
31:24	RADDR_D	Read point in internal buffer
23:16	WADDR_D_LH	Write point latch in internal buffer
15:8	WADDR_D	Write point in internal buffer
5	WD_ACT	
4	RD_ACT	
3	WREQ	Write command request
2	RREQ	Read command request

110001D4 AP_DMA_I2C_1_TX_MEM_ADDR2 **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TX_MEM_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	TX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

110001D8 AP_DMA_I2C_1_RX_MEM_ADDR2 **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RX_MEM_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	RX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

11000200 AP_DMA_I2C_2_INT_FLAG **Peripheral DMA Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FLAG_0	RX_FLAG	TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FLAG_0	**Raised when TX-to-RX is asserted when DMA engine is running.**
1	RX_FLAG	**Raised when RX DMA is finished. Write 0 to clear it.**
0	TX_FLAG	**This flag is raised when TX DMA is finished. Write 0 to clear it.** 1. After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 2. If STOP =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 3. If FLUSH =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

11000204 AP_DMA_I2C_2_INT_EN **Peripheral DMA Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INTEN_FLAG_0	INTEN_RX_FLAG	INTEN_TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	INTEN_FLAG_0	**Enables interrupt for FLAG_0** 0: Disable 1: Enable
1	INTEN_RX_FLAG	**Enables interrupt for RX_FLAG** 0: Disable 1: Enable
0	INTEN_TX_FLAG	**Enables interrupt for TX_FLAG** 0: Disable 1: Enable

11000208 AP_DMA_I2C_2_EN **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1100020C AP_DMA_I2C_2_RST **Peripheral DMA Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (reset regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000210 AP_DMA_I2C_2_STOP Peripheral DMA Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA** Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000214 AP_DMA_I2C Peripheral DMA Flush Register 00000000

_2_FLUSH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000218 AP_DMA_I2C_2_CON **Peripheral DMA Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FIX_EN	DIR
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	FIX_EN	**Peripheral DMA fixed pattern** When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as TX. 0: Does not use fixed pattern 1: Use fixed pattern
0	DIR	**Half duplex peripheral DMA direction** 0: TX 1: RX

1100021C AP_DMA_I2C_2_TX_MEM_ADDR **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MEM_ADDR															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN = 1, TX_MEM_ADDR will be treated as FIX_PATTERN. Do not set TX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be TX_MEM_ADDR when you use SYSRAM as a source memory.

11000220 AP_DMA_I2C_2_RX_MEM_ADDR **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be RX_MEM_ADDR when you use SYSRAM as a destination memory.

11000224 AP_DMA_I2C_2_TX_LEN **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_LEN	**Peripheral DMA transfer length**

Bit(s)	Name	Description
		It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

11000228 AP_DMA_I2C_2_RX_LEN **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

11000238 AP_DMA_I2C_2_INT_BUF_SIZE **Peripheral DMA Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	Byte size in internal buffer

11000250 AP_DMA_I2C_2_DEBUG_STATUS_00 **Peripheral DMA Debug Status 00 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D										WD_ACT	RD_ACT	WREQ	RREQ		
Type	RO										RO	RO	RO	RO		
Reset	0	0	0	0	0	0	0	0			0	0	0	0		

Bit(s)	Name	Description
31:24	RADDR_D	Read point in internal buffer
23:16	WADDR_D_LH	Write point latch in internal buffer
15:8	WADDR_D	Write point in internal buffer
5	WD_ACT	
4	RD_ACT	
3	WREQ	Write command request
2	RREQ	Read command request

11000254 AP_DMA_I2C_2_TX_MEM_ADDR2 **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TX_MEM_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	TX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

11000258 AP_DMA_I2C_2_RX_MEM_ADDR2 **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RX_MEM_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	RX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

11000280 AP_DMA_I2C_3_INT_FLAG **Peripheral DMA Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FLAG_0	RX_FLAG	TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FLAG_0	**Raised when TX-to-RX is asserted when DMA engine is running.**
1	RX_FLAG	**Raised when RX DMA is finished. Write 0 to clear it.**
0	TX_FLAG	**This flag is raised when TX DMA is finished. Write 0 to clear it.** 1. After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 2. If STOP =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 3. If FLUSH =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

11000284 AP_DMA_I2C_3_INT_EN **Peripheral DMA Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INTEN_FLAG_0	INTEN_RX_FLAG	INTEN_TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	INTEN_FLAG_0	**Enables interrupt for FLAG_0** 0: Disable 1: Enable
1	INTEN_RX_FLAG	**Enables interrupt for RX_FLAG** 0: Disable 1: Enable
0	INTEN_TX_FLAG	**Enables interrupt for TX_FLAG** 0: Disable 1: Enable

Bit(s)	Name	Description

11000288 AP_DMA_I2C_3_EN Peripheral DMA Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1100028C AP_DMA_I2C_3_RST Peripheral DMA Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (reset regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

Bit(s)	Name	Description

11000290 AP_DMA_I2C_3_STOP **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA** Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000294 AP_DMA_I2C_3_FLUSH **Peripheral DMA Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

Bit(s)	Name	Description

11000298 AP_DMA_I2C_3_CON **Peripheral DMA Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FIX_EN	DIR
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	FIX_EN	**Peripheral DMA fixed pattern** When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as TX. 0: Does not use fixed pattern 1: Use fixed pattern
0	DIR	**Half duplex peripheral DMA direction** 0: TX 1: RX

1100029C AP_DMA_I2C_3_TX_MEM_ADDR **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN = 1, TX_MEM_ADDR will be treated as FIX_PATTERN. Do not set TX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be TX_MEM_ADDR when you use SYSRAM as a source memory.

110002A0 AP_DMA_I2C_3_RX_MEM_ADDR **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be RX_MEM_ADDR when you use SYSRAM as a destination memory.

110002A4 AP_DMA_I2C_3_TX_LEN **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

110002A8 AP_DMA_I2C_3_RX_LEN **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_LEN	**Peripheral DMA transfer length**

Bit(s)	Name	Description
		It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

110002B8 AP_DMA_I2C_3_INT_BUF_SIZE — Peripheral DMA Internal Buffer Size Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	Byte size in internal buffer

110002D0 AP_DMA_I2C_3_DEBUG_STATUS_00 — Peripheral DMA Debug Status 00 Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D										WD_ACT	RD_ACT	WREQ	RREQ		
Type	RO										RO	RO	RO	RO		
Reset	0	0	0	0	0	0	0	0			0	0	0	0		

Bit(s)	Name	Description
31:24	RADDR_D	Read point in internal buffer
23:16	WADDR_D_LH	Write point latch in internal buffer
15:8	WADDR_D	Write point in internal buffer
5	WD_ACT	
4	RD_ACT	
3	WREQ	Write command request
2	RREQ	Read command request

110002D4 AP_DMA_I2C_3_TX_MEM_ADDR2 — Peripheral DMA Memory Address Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TX_MEM_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	TX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

110002D8 AP_DMA_I2C_3_RX_MEM_ADDR2 **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RX_MEM_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	RX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

11000300 AP_DMA_I2C_4_INT_FLAG **Peripheral DMA Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FLAG_0	RX_FLAG	TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FLAG_0	**Raised when TX-to-RX is asserted when DMA engine is running.**
1	RX_FLAG	**Raised when RX DMA is finished. Write 0 to clear it.**
0	TX_FLAG	**This flag is raised when TX DMA is finished. Write 0 to clear it.** 1. After normal operation is done, EN will be set from 1 to 0, and

Bit(s)	Name	Description
		interrupt flag will be set to 1. 2. If STOP =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 3. If FLUSH =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

11000304 AP_DMA_I2C_4_INT_EN **Peripheral DMA Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INTEN_FLAG_0	INTEN_RX_FLAG	INTEN_TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	INTEN_FLAG_0	**Enables interrupt for FLAG_0** 0: Disable 1: Enable
1	INTEN_RX_FLAG	**Enables interrupt for RX_FLAG** 0: Disable 1: Enable
0	INTEN_TX_FLAG	**Enables interrupt for TX_FLAG** 0: Disable 1: Enable

11000308 AP_DMA_I2C_4_EN **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will

Bit(s)	Name	Description
		be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1100030C AP_DMA_I2C_4_RST **Peripheral DMA Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (reset regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000310 AP_DMA_I2C_4_STOP **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA** Set to 1 to pause DMA and back to 0 to resume DMA.

Bit(s)	Name	Description
		0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000314 AP_DMA_I2C_4_FLUSH **Peripheral DMA Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000318 AP_DMA_I2C_4_CON **Peripheral DMA Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FIX_EN	DIR
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	FIX_EN	**Peripheral DMA fixed pattern** When FIX_EN is turned on, DIR will be ignored, and DMA will

Bit(s)	Name	Description
		always treat this transfer as TX. 0: Does not use fixed pattern 1: Use fixed pattern
0	DIR	**Half duplex peripheral DMA direction** 0: TX 1: RX

1100031C AP_DMA_I2C_4_TX_MEM_ADDR **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN = 1, TX_MEM_ADDR will be treated as FIX_PATTERN. Do not set TX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be TX_MEM_ADDR when you use SYSRAM as a source memory.

11000320 AP_DMA_I2C_4_RX_MEM_ADDR **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be RX_MEM_ADDR when you use SYSRAM as a destination memory.

11000324 AP_DMA_I2C_4_TX_LEN **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

11000328 AP_DMA_I2C_4_RX_LEN **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

11000338 AP_DMA_I2C_4_INT_BUF_SIZE **Peripheral DMA Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							

Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	Byte size in internal buffer

11000350 AP_DMA_I2C_4_DEBUG_STATUS_00 Peripheral DMA Debug Status 00 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D										WD_ACT	RD_ACT	WREQ	RREQ		
Type	RO										RO	RO	RO	RO		
Reset	0	0	0	0	0	0	0	0			0	0	0	0		

Bit(s)	Name	Description
31:24	RADDR_D	Read point in internal buffer
23:16	WADDR_D_LH	Write point latch in internal buffer
15:8	WADDR_D	Write point in internal buffer
5	WD_ACT	
4	RD_ACT	
3	WREQ	Write command request
2	RREQ	Read command request

11000354 AP_DMA_I2C_4_TX_MEM_ADDR2 Peripheral DMA Memory Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TX_MEM_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	TX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

11000358 AP_DMA_I2C_4_RX_MEM_ADDR2 Peripheral DMA Memory Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RX_MEM_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	RX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

11000380 AP_DMA_I2C_5_INT_FLAG **Peripheral DMA Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FLAG_0	RX_FLAG	TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FLAG_0	**Raised when TX-to-RX is asserted when DMA engine is running.**
1	RX_FLAG	**Raised when RX DMA is finished. Write 0 to clear it.**
0	TX_FLAG	**This flag is raised when TX DMA is finished. Write 0 to clear it.** 1. After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 2. If STOP =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 3. If FLUSH =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

11000384 AP_DMA_I2C_5_INT_EN **Peripheral DMA Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INTE	INTE	INTE

														N_FLAG_0	N_RX_FLAG	N_TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	INTEN_FLAG_0	**Enables interrupt for FLAG_0** 0: Disable 1: Enable
1	INTEN_RX_FLAG	**Enables interrupt for RX_FLAG** 0: Disable 1: Enable
0	INTEN_TX_FLAG	**Enables interrupt for TX_FLAG** 0: Disable 1: Enable

11000388 AP_DMA_I2C_5_EN **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1100038C AP_DMA_I2C_5_RST **Peripheral DMA Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW

Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (reset regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000390 AP_DMA_I2C_5_STOP **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA** Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000394 AP_DMA_I2C_5_FLUSH **Peripheral DMA Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH

Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000398 AP_DMA_I2C_5_CON **Peripheral DMA Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**FIX_EN**	**DIR**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	FIX_EN	**Peripheral DMA fixed pattern** When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as TX. 0: Does not use fixed pattern 1: Use fixed pattern
0	DIR	**Half duplex peripheral DMA direction** 0: TX 1: RX

1100039C AP_DMA_I2C_5_TX_MEM_ADDR **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TX_MEM_ADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TX_MEM_ADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
31:0	TX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN = 1, TX_MEM_ADDR will be treated as FIX_PATTERN. Do not set TX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be TX_MEM_ADDR when you use SYSRAM as a source memory.

110003A0 AP_DMA_I2C_5_RX_MEM_ADDR **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be RX_MEM_ADDR when you use SYSRAM as a destination memory.

110003A4 AP_DMA_I2C_5_TX_LEN **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

110003A8 AP_DMA_I2C_5_RX_LEN — Peripheral DMA Transfer Length Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

110003B8 AP_DMA_I2C_5_INT_BUF_SIZE — Peripheral DMA Internal Buffer Size Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	Byte size in internal buffer

110003D0 AP_DMA_I2C_5_DEBUG_STATUS_00 — Peripheral DMA Debug Status 00 Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D										WD_ACT	RD_ACT	WREQ	RREQ		
Type	RO										RO	RO	RO	RO		
Reset	0	0	0	0	0	0	0	0			0	0	0	0		

Bit(s)	Name	Description
31:24	RADDR_D	Read point in internal buffer

Bit(s)	Name	Description
23:16	WADDR_D_LH	Write point latch in internal buffer
15:8	WADDR_D	Write point in internal buffer
5	WD_ACT	
4	RD_ACT	
3	WREQ	Write command request
2	RREQ	Read command request

110003D4 AP_DMA_I2C_5_TX_MEM_ADDR2 — Peripheral DMA Memory Address Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TX_MEM_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	TX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

110003D8 AP_DMA_I2C_5_RX_MEM_ADDR2 — Peripheral DMA Memory Address Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RX_MEM_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	RX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

11000400 AP_DMA_I2C_6_INT_FLAG — Peripheral DMA Interrupt Flag Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FLAG_0	RX_FLAG	TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FLAG_0	**Raised when TX-to-RX is asserted when DMA engine is running.**
1	RX_FLAG	**Raised when RX DMA is finished. Write 0 to clear it.**
0	TX_FLAG	**This flag is raised when TX DMA is finished. Write 0 to clear it.** 1. After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 2. If STOP =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 3. If FLUSH =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

11000404 AP_DMA_I2C_6_INT_EN **Peripheral DMA Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INTEN_FLAG_0	INTEN_RX_FLAG	INTEN_TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	INTEN_FLAG_0	**Enables interrupt for FLAG_0** 0: Disable 1: Enable
1	INTEN_RX_FLAG	**Enables interrupt for RX_FLAG** 0: Disable 1: Enable
0	INTEN_TX_FLAG	**Enables interrupt for TX_FLAG** 0: Disable 1: Enable

11000408 AP_DMA_I2C_6_EN **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1100040C AP_DMA_I2C_6_RST **Peripheral DMA Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (reset regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000410 AP_DMA_I2C_6_STOP **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA** Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000414 AP_DMA_I2C_6_FLUSH **Peripheral DMA Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000418 AP_DMA_I2C_6_CON **Peripheral DMA Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FIX_EN	DIR
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	FIX_EN	**Peripheral DMA fixed pattern** When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as TX. 0: Does not use fixed pattern 1: Use fixed pattern
0	DIR	**Half duplex peripheral DMA direction** 0: TX 1: RX

1100041C AP_DMA_I2C_6_TX_MEM_ADDR — **Peripheral DMA Memory Address Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN = 1, TX_MEM_ADDR will be treated as FIX_PATTERN. Do not set TX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be TX_MEM_ADDR when you use SYSRAM as a source memory.

11000420 AP_DMA_I2C_6_RX_MEM_ADDR — **Peripheral DMA Memory Address Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be RX_MEM_ADDR when you use SYSRAM as a destination memory.

11000424 AP_DMA_I2C_6_TX_LEN **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

11000428 AP_DMA_I2C_6_RX_LEN **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

11000438 AP_DMA_I2C_6_INT_BUF **Peripheral DMA Internal Buffer Size Register** **00000000**

_SIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	Byte size in internal buffer

11000450 AP_DMA_I2C_6_DEBUG_STATUS_00 Peripheral DMA Debug Status 00 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D										WD_ACT	RD_ACT	WREQ	RREQ		
Type	RO										RO	RO	RO	RO		
Reset	0	0	0	0	0	0	0	0			0	0	0	0		

Bit(s)	Name	Description
31:24	RADDR_D	Read point in internal buffer
23:16	WADDR_D_LH	Write point latch in internal buffer
15:8	WADDR_D	Write point in internal buffer
5	WD_ACT	
4	RD_ACT	
3	WREQ	Write command request
2	RREQ	Read command request

11000454 AP_DMA_I2C_6_TX_MEM_ADDR2 Peripheral DMA Memory Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TX_MEM_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	TX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

11000458 AP_DMA_I2C_6_RX_MEM_ADDR2 **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RX_MEM_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	RX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

11000480 AP_DMA_I2C_7_INT_FLAG **Peripheral DMA Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FLAG_0	RX_FLAG	TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FLAG_0	**Raised when TX-to-RX is asserted when DMA engine is running.**
1	RX_FLAG	**Raised when RX DMA is finished. Write 0 to clear it.**
0	TX_FLAG	**This flag is raised when TX DMA is finished. Write 0 to clear it.** 1. After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 2. If STOP =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 3. If FLUSH =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

11000484 AP_DMA_I2C_7_INT_EN **Peripheral DMA Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INTEN_FLAG_0	INTEN_RX_FLAG	INTEN_TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	INTEN_FLAG_0	**Enables interrupt for FLAG_0** 0: Disable 1: Enable
1	INTEN_RX_FLAG	**Enables interrupt for RX_FLAG** 0: Disable 1: Enable
0	INTEN_TX_FLAG	**Enables interrupt for TX_FLAG** 0: Disable 1: Enable

11000488 AP_DMA_I2C_7_EN **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1100048C AP_DMA_I2C_7_RST **Peripheral DMA Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (reset regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000490 AP_DMA_I2C_7_STOP Peripheral DMA Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA** Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000494 AP_DMA_I2C Peripheral DMA Flush Register 00000000

_7_FLUSH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000498 AP_DMA_I2C_7_CON **Peripheral DMA Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FIX_EN	DIR
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	FIX_EN	**Peripheral DMA fixed pattern** When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as TX. 0: Does not use fixed pattern 1: Use fixed pattern
0	DIR	**Half duplex peripheral DMA direction** 0: TX 1: RX

1100049C AP_DMA_I2C_7_TX_MEM_ADDR **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MEM_ADDR															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN = 1, TX_MEM_ADDR will be treated as FIX_PATTERN. Do not set TX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be TX_MEM_ADDR when you use SYSRAM as a source memory.

110004A0 AP_DMA_I2C_7_RX_MEM_ADDR — Peripheral DMA Memory Address Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be RX_MEM_ADDR when you use SYSRAM as a destination memory.

110004A4 AP_DMA_I2C_7_TX_LEN — Peripheral DMA Transfer Length Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_LEN	**Peripheral DMA transfer length**

Bit(s)	Name	Description
		It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

110004A8 AP_DMA_I2C_7_RX_LEN — **Peripheral DMA Transfer Length Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

110004B8 AP_DMA_I2C_7_INT_BUF_SIZE — **Peripheral DMA Internal Buffer Size Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	Byte size in internal buffer

110004D0 AP_DMA_I2C_7_DEBUG_STATUS_00 — **Peripheral DMA Debug Status 00 Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D										WD_ACT	RD_ACT	WREQ	RREQ		
Type	RO										RO	RO	RO	RO		
Reset	0	0	0	0	0	0	0	0			0	0	0	0		

Bit(s)	Name	Description
31:24	RADDR_D	Read point in internal buffer
23:16	WADDR_D_LH	Write point latch in internal buffer
15:8	WADDR_D	Write point in internal buffer
5	WD_ACT	
4	RD_ACT	
3	WREQ	Write command request
2	RREQ	Read command request

110004D4 AP_DMA_I2C_7_TX_MEM_ADDR2 **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TX_MEM_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	TX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

110004D8 AP_DMA_I2C_7_RX_MEM_ADDR2 **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RX_MEM_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	RX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

11000500 AP_DMA_I2C_8_INT_FLAG **Peripheral DMA Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FLAG_0	RX_FLAG	TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FLAG_0	**Raised when TX-to-RX is asserted when DMA engine is running.**
1	RX_FLAG	**Raised when RX DMA is finished. Write 0 to clear it.**
0	TX_FLAG	**This flag is raised when TX DMA is finished. Write 0 to clear it.** 1. After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 2. If STOP =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 3. If FLUSH =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

11000504 AP_DMA_I2C_8_INT_EN **Peripheral DMA Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INTEN_FLAG_0	INTEN_RX_FLAG	INTEN_TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	INTEN_FLAG_0	**Enables interrupt for FLAG_0** 0: Disable 1: Enable
1	INTEN_RX_FLAG	**Enables interrupt for RX_FLAG** 0: Disable 1: Enable
0	INTEN_TX_FLAG	**Enables interrupt for TX_FLAG** 0: Disable

Bit(s)	Name	Description
		1: Enable

11000508 AP_DMA_I2C_8_EN **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1100050C AP_DMA_I2C_8_RST **Peripheral DMA Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (reset regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable

Bit(s)	Name	Description
		1: Enable

11000510 AP_DMA_I2C_8_STOP **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA** Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000514 AP_DMA_I2C_8_FLUSH **Peripheral DMA Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable

Bit(s)	Name	Description
		1: Enable

11000518 AP_DMA_I2C_8_CON **Peripheral DMA Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FIX_EN	DIR
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	FIX_EN	**Peripheral DMA fixed pattern** When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as TX. 0: Does not use fixed pattern 1: Use fixed pattern
0	DIR	**Half duplex peripheral DMA direction** 0: TX 1: RX

1100051C AP_DMA_I2C_8_TX_MEM_ADDR **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN = 1, TX_MEM_ADDR will be treated as FIX_PATTERN. Do not set TX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be TX_MEM_ADDR when you use SYSRAM as a source memory.

11000520 AP_DMA_I2C_8_RX_MEM **Peripheral DMA Memory Address Register** **00000000**

ADDR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be RX_MEM_ADDR when you use SYSRAM as a destination memory.

11000524 AP_DMA_I2C_8_TX_LEN — **Peripheral DMA Transfer Length Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

11000528 AP_DMA_I2C_8_RX_LEN — **Peripheral DMA Transfer Length Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
15:0	RX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

11000538 AP_DMA_I2C_8_INT_BUF_SIZE **Peripheral DMA Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	Byte size in internal buffer

11000550 AP_DMA_I2C_8_DEBUG_STATUS_00 **Peripheral DMA Debug Status 00 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D										WD_ACT	RD_ACT	WREQ	RREQ		
Type	RO										RO	RO	RO	RO		
Reset	0	0	0	0	0	0	0	0			0	0	0	0		

Bit(s)	Name	Description
31:24	RADDR_D	Read point in internal buffer
23:16	WADDR_D_LH	Write point latch in internal buffer
15:8	WADDR_D	Write point in internal buffer
5	WD_ACT	
4	RD_ACT	
3	WREQ	Write command request
2	RREQ	Read command request

11000554 AP_DMA_I2C_8_TX_MEM_ADDR2 **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TX_MEM_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	TX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

11000558 AP_DMA_I2C_8_RX_MEM_ADDR2 **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RX_MEM_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	RX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

11000580 AP_DMA_I2C_9_INT_FLAG **Peripheral DMA Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FLAG_0	RX_FLAG	TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FLAG_0	**Raised when TX-to-RX is asserted when DMA engine is running.**
1	RX_FLAG	**Raised when RX DMA is finished. Write 0 to clear it.**
0	TX_FLAG	**This flag is raised when TX DMA is finished. Write 0 to clear it.**

Bit(s)	Name	Description
		1. After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 2. If STOP =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 3. If FLUSH =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

11000584 AP_DMA_I2C_9_INT_EN **Peripheral DMA Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INTEN_FLAG_0	INTEN_RX_FLAG	INTEN_TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	INTEN_FLAG_0	**Enables interrupt for FLAG_0** 0: Disable 1: Enable
1	INTEN_RX_FLAG	**Enables interrupt for RX_FLAG** 0: Disable 1: Enable
0	INTEN_TX_FLAG	**Enables interrupt for TX_FLAG** 0: Disable 1: Enable

11000588 AP_DMA_I2C_9_EN **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA. When DMA is busy, EN will always be 1. When

Bit(s)	Name	Description
		DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1100058C AP_DMA_I2C_9_RST Peripheral DMA Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (reset regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000590 AP_DMA_I2C_9_STOP Peripheral DMA Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA**

Bit(s)	Name	Description
		Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000594 AP_DMA_I2C_9_FLUSH **Peripheral DMA Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000598 AP_DMA_I2C_9_CON **Peripheral DMA Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FIX_EN	DIR
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	FIX_EN	**Peripheral DMA fixed pattern**

Bit(s)	Name	Description
		When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as TX. 0: Does not use fixed pattern 1: Use fixed pattern
0	DIR	**Half duplex peripheral DMA direction** 0: TX 1: RX

1100059C AP_DMA_I2C_9_TX_MEM_ADDR **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN = 1, TX_MEM_ADDR will be treated as FIX_PATTERN. Do not set TX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be TX_MEM_ADDR when you use SYSRAM as a source memory.

110005A0 AP_DMA_I2C_9_RX_MEM_ADDR **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be RX_MEM_ADDR when you use SYSRAM as a destination memory.

110005A4 AP_DMA_I2C_9_TX_LEN — **Peripheral DMA Transfer Length Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

110005A8 AP_DMA_I2C_9_RX_LEN — **Peripheral DMA Transfer Length Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

110005B8 AP_DMA_I2C_9_INT_BUF_SIZE — **Peripheral DMA Internal Buffer Size Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							

Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	Byte size in internal buffer

110005D0 AP_DMA_I2C_9_DEBUG_STATUS_00 Peripheral DMA Debug Status 00 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D										WD_ACT	RD_ACT	WREQ	RREQ		
Type	RO										RO	RO	RO	RO		
Reset	0	0	0	0	0	0	0	0			0	0	0	0		

Bit(s)	Name	Description
31:24	RADDR_D	Read point in internal buffer
23:16	WADDR_D_LH	Write point latch in internal buffer
15:8	WADDR_D	Write point in internal buffer
5	WD_ACT	
4	RD_ACT	
3	WREQ	Write command request
2	RREQ	Read command request

110005D4 AP_DMA_I2C_9_TX_MEM_ADDR2 Peripheral DMA Memory Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TX_MEM_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	TX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

110005D8 AP_DMA_I2C_9_RX_MEM_ADDR2 Peripheral DMA Memory Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RX_MEM_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	RX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

11000600 AP_DMA_UART_0_TX_INT_FLAG — **UART TX Virtual FIFO Interrupt Flag Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	**Write 0 to clear it.** Interrupt will be issued to HW when FLAG=1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN=1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

11000604 AP_DMA_UART_0_TX_INT_EN — **UART TX Virtual FIFO Interrupt Enable Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enabling** This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Does not set flag to 1, even tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto set inten back to 0 when tx_vff_left_size >= tx_vff_thrs

11000608 AP_DMA_UART_0_TX_EN **UART TX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART TX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When EN = 0 and MCU writes data to the VFF_W port (a AHB slave port), VFF_W will ignore this command, and the data will not be writte to virtual FIFO. 0: Disable 1: Enable

1100060C AP_DMA_UART_0_TX_RST **UART TX Virtual FIFO Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable

Bit(s)	Name	Description
		1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RSTt to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000610 AP_DMA_UART_0_TX_STOP **UART TX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART TX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000614 AP_DMA_UART_0_TX_FLUSH **UART TX Virtual FIFO Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART TX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again.

Bit(s)	Name	Description
		Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1100061C AP_DMA_UART_0_TX_VFF_ADDR **UART TX Virtual FIFO Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	**UART memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

11000624 AP_DMA_UART_0_TX_VFF_LEN **UART TX Virtual FIFO Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

11000628 AP_DMA_UART_0_TX_VFF_THRE **UART TX Virtual FIFO Threshold Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	**VFF threshold in byte alignment** In TX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

1100062C AP_DMA_UART_0_TX_VFF_WPT — UART TX Virtual FIFO Write Pointer Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	**TX VFF write pointer wrap bit** It is initialized to 0. When wrapped to the ring head again, invert this bit. For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.
15:0	TX_VFF_WPT	**Byte alignment FIFO write pointer** For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.

11000630 AP_DMA_UART_0_TX_VFF_RPT — UART TX Virtual FIFO Read Pointer Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_RPT															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	**TX VFF read pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	TX_VFF_RPT	**TX VFF read pointer maintained by hardware** In byte alignment.

11000638 AP_DMA_UART_0_TX_INT_BUF_SIZE **UART Tx Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	**Virtual FIFO DMA TX internal buffer size** 0: 0 byte 1: 1 byte

1100063C AP_DMA_UART_0_TX_VFF_VALID_SIZE **UART Tx Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	**TX virtual FIFO valid size** 0: 0 byte 1: 1 byte

11000640 AP_DMA_UART_0_TX_VFF_LEFT_SIZE **UART Tx Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	**TX virtual FIFO left size** 0: 0 byte 1: 1 byte

11000650 AP_DMA_UART_0_TX_DEBUG_STATUS_00 **UART Tx Debug Status 00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D							WD_ACT	RD_ACT	WREQ	RREQ		
Type				RO							RO	RO	RO	RO		
Reset				0	0	0	0	0			0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	

11000654 AP_DMA_UART_0_TX_VFF_ADDR2 **UART TX Virtual FIFO Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TX_VFF_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	TX_VFF_ADDR2	UART memory address bit[32]

11000658 AP_DMA_UART_0_TX_VFF_WPT_VALID — **UART TX Virtual FIFO Write Pointer Register by HW Control** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	**TX VFF write pointer wrap bit** If FLUSH= 0, sync to TX_VFF_WPT_WRAP. If flush, it will not update the value untill the flush is finished.
15:0	TX_VFF_WPT_VALID	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

1100065C AP_DMA_UART_0_TX_VFF_WPT_VALID2 — **UART TX Virtual FIFO Write Pointer Register by HW Control** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_WPT_VALID2	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

11000660 AP_DMA_UART_0_TX_FLU — **UART TX Virtual FIFO Flush Status Register** — **00000000**

SH_ACT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLUSH_NEXT	FLUSH_ACT
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	There is a flush command when the UART TX channel is flushing.
0	FLUSH_ACT	UART TX channel flush status

11000664 AP_DMA_UART_0_TX_HW_FLUSH — **UART TX Virtual FIFO HW Flush Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HW_FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	**Flush control bit** Controls the UART TX write pointer if the SW setting value at flushing is updated. 0: Update wpt with SW setting 1: Update wpt when flush =0

11000668 AP_DMA_UART_0_TX_VFF_WPT_REAL — **UART TX Virtual FIFO Write Pointer Register Value** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_REAL
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_REAL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_REAL	**TX VFF write pointer wrap bit** If HW_FLUSH = 1, sync to TX_VFF_WPT_WRAP_VALID. If HW_FLUSH = 0, sync to TX_VFF_WPT_WRAP.
15:0	TX_VFF_WPT_REAL	**TX VFF write pointer** If HW_FLUSH = 1, sync to TX_VFF_WPT_VALID. If HW_FLUSH = 0, sync to TX_VFF_WPT.

11000700 AP_DMA_UART_1_TX_INT_FLAG **UART TX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	**Write 0 to clear it.** Interrupt will be issued to HW when FLAG=1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN=1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

11000704 AP_DMA_UART_1_TX_INT_EN **UART TX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enabling** This bit is used to control if the flag will be set to 1 when

Bit(s)	Name	Description
		TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Does not set flag to 1, even tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto set inten back to 0 when tx_vff_left_size >= tx_vff_thrs

11000708 AP_DMA_UART_1_TX_EN **UART TX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART TX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When EN = 0 and MCU writes data to the VFF_W port (a AHB slave port), VFF_W will ignore this command, and the data will not be writte to virtual FIFO. 0: Disable 1: Enable

1100070C AP_DMA_UART_1_TX_RST **UART TX Virtual FIFO Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RSTt to 1 and waits for EN to become 0. HW auto

Bit(s)	Name	Description
		sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000710 AP_DMA_UART_1_TX_STOP **UART TX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART TX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000714 AP_DMA_UART_1_TX_FLUSH **UART TX Virtual FIFO Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART TX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Flush finished 1: Enable

Bit(s)	Name	Description

1100071C AP_DMA_UART_1_TX_VFF_ADDR — **UART TX Virtual FIFO Base Address Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	**UART memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

11000724 AP_DMA_UART_1_TX_VFF_LEN — **UART TX Virtual FIFO Length Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

11000728 AP_DMA_UART_1_TX_VFF_THRE — **UART TX Virtual FIFO Threshold Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	**VFF threshold in byte alignment** In TX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

1100072C AP_DMA_UART_1_TX_VFF_WPT **UART TX Virtual FIFO Write Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	**TX VFF write pointer wrap bit** It is initialized to 0. When wrapped to the ring head again, invert this bit. For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.
15:0	TX_VFF_WPT	**Byte alignment FIFO write pointer** For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.

11000730 AP_DMA_UART_1_TX_VFF_RPT **UART TX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_RPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	**TX VFF read pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	TX_VFF_RPT	**TX VFF read pointer maintained by hardware** In byte alignment.

11000738 AP_DMA_UART_1_TX_INT_BUF_SIZE **UART Tx Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	**Virtual FIFO DMA TX internal buffer size** 0: 0 byte 1: 1 byte

1100073C AP_DMA_UART_1_TX_VFF_VALID_SIZE **UART Tx Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	**TX virtual FIFO valid size** 0: 0 byte 1: 1 byte

11000740 AP_DMA_UART_1_TX_VFF_LEFT_SIZE **UART Tx Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	**TX virtual FIFO left size** 0: 0 byte 1: 1 byte

11000750 **AP_DMA_UART_1_TX_DEBUG_STATUS_00** **UART Tx Debug Status 00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADD R_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D							WD_ACT	RD_ACT	WREQ	RREQ		
Type				RO							RO	RO	RO	RO		
Reset				0	0	0	0	0			0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	

11000754 **AP_DMA_UART_1_TX_VFF_ADDR2** **UART TX Virtual FIFO Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TX_VFF_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	TX_VFF_ADDR2	**UART memory address bit[32]**

Bit(s)	Name	Description

11000758 AP_DMA_UART_1_TX_VFF_WPT_VALID — **UART TX Virtual FIFO Write Pointer Register by HW Control** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	**TX VFF write pointer wrap bit** If FLUSH= 0, sync to TX_VFF_WPT_WRAP. If flush, it will not update the value untill the flush is finished.
15:0	TX_VFF_WPT_VALID	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

1100075C AP_DMA_UART_1_TX_VFF_WPT_VALID2 — **UART TX Virtual FIFO Write Pointer Register by HW Control** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_WPT_VALID2	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

11000760 AP_DMA_UART_1_TX_FLUSH_ACT — **UART TX Virtual FIFO Flush Status Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLUSH_NEXT	FLUSH_ACT
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	There is a flush command when the UART TX channel is flushing.
0	FLUSH_ACT	UART TX channel flush status

11000764 AP_DMA_UART_1_TX_HW_FLUSH — **UART TX Virtual FIFO HW Flush Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HW_FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	**Flush control bit** Controls the UART TX write pointer if the SW setting value at flushing is updated. 0: Update wpt with SW setting 1: Update wpt when flush =0

11000768 AP_DMA_UART_1_TX_VFF_WPT_REAL — **UART TX Virtual FIFO Write Pointer Register Value** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_REAL
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_REAL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_REAL	**TX VFF write pointer wrap bit** If HW_FLUSH = 1, sync to TX_VFF_WPT_WRAP_VALID. If HW_FLUSH = 0, sync to TX_VFF_WPT_WRAP.
15:0	TX_VFF_WPT_REAL	**TX VFF write pointer** If HW_FLUSH = 1, sync to TX_VFF_WPT_VALID. If HW_FLUSH = 0, sync to TX_VFF_WPT.

11000800 AP_DMA_UART_2_TX_INT_FLAG **UART TX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	**Write 0 to clear it.** Interrupt will be issued to HW when FLAG=1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN=1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

11000804 AP_DMA_UART_2_TX_INT_EN **UART TX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enabling** This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS.

Bit(s)	Name	Description
		0: Does not set flag to 1, even tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto set inten back to 0 when tx_vff_left_size >= tx_vff_thrs

11000808 AP_DMA_UART_2_TX_EN **UART TX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART TX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When EN = 0 and MCU writes data to the VFF_W port (a AHB slave port), VFF_W will ignore this command, and the data will not be writte to virtual FIFO. 0: Disable 1: Enable

1100080C AP_DMA_UART_2_TX_RST **UART TX Virtual FIFO Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RSTt to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism.

Bit(s)	Name	Description
		0: Disable 1: Enable

11000810 AP_DMA_UART_2_TX_STOP **UART TX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART TX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000814 AP_DMA_UART_2_TX_FLUSH **UART TX Virtual FIFO Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART TX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Flush finished 1: Enable

1100081C AP_DMA_UART_2_TX_VFF_ADDR — UART TX Virtual FIFO Base Address Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	**UART memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

11000824 AP_DMA_UART_2_TX_VFF_LEN — UART TX Virtual FIFO Length Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

11000828 AP_DMA_UART_2_TX_VFF_THRE — UART TX Virtual FIFO Threshold Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	**VFF threshold in byte alignment** In TX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

1100082C AP_DMA_UART_2_TX_VFF_WPT **UART TX Virtual FIFO Write Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	**TX VFF write pointer wrap bit** It is initialized to 0. When wrapped to the ring head again, invert this bit. For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.
15:0	TX_VFF_WPT	**Byte alignment FIFO write pointer** For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.

11000830 AP_DMA_UART_2_TX_VFF_RPT **UART TX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_RPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	**TX VFF read pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	TX_VFF_RPT	**TX VFF read pointer maintained by hardware**

Bit(s)	Name	Description
		In byte alignment.

11000838 AP_DMA_UART_2_TX_INT_BUF_SIZE **UART Tx Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	**Virtual FIFO DMA TX internal buffer size** 0: 0 byte 1: 1 byte

1100083C AP_DMA_UART_2_TX_VFF_VALID_SIZE **UART Tx Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	**TX virtual FIFO valid size** 0: 0 byte 1: 1 byte

11000840 AP_DMA_UART_2_TX_VFF_LEFT_SIZE **UART Tx Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	**TX virtual FIFO left size** 0: 0 byte 1: 1 byte

11000850 AP_DMA_UART_2_TX_DEBUG_STATUS_00 — UART Tx Debug Status 00 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D							WD_ACT	RD_ACT	WREQ	RREQ		
Type				RO							RO	RO	RO	RO		
Reset				0	0	0	0	0			0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	

11000854 AP_DMA_UART_2_TX_VFF_ADDR2 — UART TX Virtual FIFO Base Address Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TX_VFF_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	TX_VFF_ADDR2	UART memory address bit[32]

11000858 AP_DMA_UART_2_TX_VFF_WPT_VALID — **UART TX Virtual FIFO Write Pointer Register by HW Control** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	**TX VFF write pointer wrap bit** If FLUSH= 0, sync to TX_VFF_WPT_WRAP. If flush, it will not update the value untill the flush is finished.
15:0	TX_VFF_WPT_VALID	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

1100085C AP_DMA_UART_2_TX_VFF_WPT_VALID2 — **UART TX Virtual FIFO Write Pointer Register by HW Control** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_WPT_VALID2	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

11000860 AP_DMA_UART_2_TX_FLUSH_ACT — **UART TX Virtual FIFO Flush Status Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name															FLUSH_NEXT	FLUSH_ACT
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	There is a flush command when the UART TX channel is flushing.
0	FLUSH_ACT	UART TX channel flush status

11000864 AP_DMA_UART_2_TX_HW_FLUSH — **UART TX Virtual FIFO HW Flush Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HW_FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	**Flush control bit** Controls the UART TX write pointer if the SW setting value at flushing is updated. 0: Update wpt with SW setting 1: Update wpt when flush =0

11000868 AP_DMA_UART_2_TX_VFF_WPT_REAL — **UART TX Virtual FIFO Write Pointer Register Value** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_REAL
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_REAL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_REAL	**TX VFF write pointer wrap bit** If HW_FLUSH = 1, sync to TX_VFF_WPT_WRAP_VALID. If HW_FLUSH = 0, sync to TX_VFF_WPT_WRAP.
15:0	TX_VFF_WPT_REAL	**TX VFF write pointer**

Bit(s)	Name	Description
		If HW_FLUSH = 1, sync to TX_VFF_WPT_VALID. If HW_FLUSH = 0, sync to TX_VFF_WPT.

11000900 AP_DMA_UART_3_TX_INT_FLAG **UART TX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	**Write 0 to clear it.** Interrupt will be issued to HW when FLAG=1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN=1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

11000904 AP_DMA_UART_3_TX_INT_EN **UART TX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enabling** This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Does not set flag to 1, even tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto set inten back to 0 when tx_vff_left_size >= tx_vff_thrs

11000908 AP_DMA_UART_3_TX_EN **UART TX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART TX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When EN = 0 and MCU writes data to the VFF_W port (a AHB slave port), VFF_W will ignore this command, and the data will not be writte to virtual FIFO. 0: Disable 1: Enable

1100090C AP_DMA_UART_3_TX_RST **UART TX Virtual FIFO Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RSTt to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000910 AP_DMA_UART_3_TX_STOP — **UART TX Virtual FIFO Enable Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART TX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000914 AP_DMA_UART_3_TX_FLUSH — **UART TX Virtual FIFO Flush Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART TX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Flush finished 1: Enable

1100091C AP_DMA_UART_3_TX_VFF_ADDR — **UART TX Virtual FIFO Base Address Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	**UART memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

11000924 AP_DMA_UART_3_TX_VFF_LEN **UART TX Virtual FIFO Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

11000928 AP_DMA_UART_3_TX_VFF_THRE **UART TX Virtual FIFO Threshold Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	**VFF threshold in byte alignment** In TX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

Bit(s)	Name	Description

1100092C AP_DMA_UART_3_TX_VFF_WPT — **UART TX Virtual FIFO Write Pointer Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	**TX VFF write pointer wrap bit** It is initialized to 0. When wrapped to the ring head again, invert this bit. For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.
15:0	TX_VFF_WPT	**Byte alignment FIFO write pointer** For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.

11000930 AP_DMA_UART_3_TX_VFF_RPT — **UART TX Virtual FIFO Read Pointer Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_RPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	**TX VFF read pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	TX_VFF_RPT	**TX VFF read pointer maintained by hardware** In byte alignment.

11000938 AP_DMA_UART_3_TX_INT_BUF_SIZE **UART Tx Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	**Virtual FIFO DMA TX internal buffer size** 0: 0 byte 1: 1 byte

1100093C AP_DMA_UART_3_TX_VFF_VALID_SIZE **UART Tx Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	**TX virtual FIFO valid size** 0: 0 byte 1: 1 byte

11000940 AP_DMA_UART_3_TX_VFF_LEFT_SIZE **UART Tx Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	**TX virtual FIFO left size** 0: 0 byte 1: 1 byte

11000950 AP_DMA_UART_3_TX_DEBUG_STATUS_00 **UART Tx Debug Status 00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D							WD_ACT	RD_ACT	WREQ	RREQ		
Type				RO							RO	RO	RO	RO		
Reset				0	0	0	0	0			0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	

11000954 AP_DMA_UART_3_TX_VFF_ADDR2 **UART TX Virtual FIFO Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TX_VFF_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	TX_VFF_ADDR2	UART memory address bit[32]

11000958 AP_DMA_UART_3_TX_VFF_WPT_VALID **UART TX Virtual FIFO Write Pointer Register by HW Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	**TX VFF write pointer wrap bit** If FLUSH= 0, sync to TX_VFF_WPT_WRAP. If flush, it will not update the value untill the flush is finished.
15:0	TX_VFF_WPT_VALID	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

1100095C **AP_DMA_UART_3_TX_VFF_WPT_VALID2** **UART TX Virtual FIFO Write Pointer Register by HW Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_WPT_VALID2	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

11000960 **AP_DMA_UART_3_TX_FLUSH_ACT** **UART TX Virtual FIFO Flush Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLUSH_NEXT	FLUSH_ACT

Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	There is a flush command when the UART TX channel is flushing.
0	FLUSH_ACT	UART TX channel flush status

11000964 AP_DMA_UART_3_TX_HW_FLUSH **UART TX Virtual FIFO HW Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HW_FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	**Flush control bit** Controls the UART TX write pointer if the SW setting value at flushing is updated. 0: Update wpt with SW setting 1: Update wpt when flush =0

11000968 AP_DMA_UART_3_TX_VFF_WPT_REAL **UART TX Virtual FIFO Write Pointer Register Value** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_REAL
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_REAL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_REAL	**TX VFF write pointer wrap bit** If HW_FLUSH = 1, sync to TX_VFF_WPT_WRAP_VALID. If HW_FLUSH = 0, sync to TX_VFF_WPT_WRAP.
15:0	TX_VFF_WPT_REAL	**TX VFF write pointer** If HW_FLUSH = 1, sync to TX_VFF_WPT_VALID. If HW_FLUSH = 0, sync to TX_VFF_WPT.

11000A00 AP_DMA_BTIF_0_TX_INT_FLAG **BTIF TX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	**Write 0 to clear it.** Interrupt will be issued to HW when FLAG=1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN=1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to BTIF and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

11000A04 AP_DMA_BTIF_0_TX_INT_EN **BTIF TX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enabling** This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Does not set flag to 1, even tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto set inten back to 0 when tx_vff_left_size >= tx_vff_thrs

11000A08 AP_DMA_BTIF_0_TX_EN **BTIF TX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables BTIF TX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When EN = 0 and MCU writes data to the VFF_W port (a AHB slave port), VFF_W will ignore this command, and the data will not be writte to virtual FIFO. 0: Disable 1: Enable

11000A0C AP_DMA_BTIF_0_TX_RST **BTIF TX Virtual FIFO Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RSTt to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000A10 AP_DMA_BTIF_0_TX_STOP **BTIF TX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops BTIF TX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Disable 1: Enable

11000A14 AP_DMA_BTIF_0_TX_FLUSH **BTIF TX Virtual FIFO Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes BTIF TX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Flush finished 1: Enable

11000A1C AP_DMA_BTIF_0_TX_VFF_ADDR **BTIF TX Virtual FIFO Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	**BTIF memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

11000A24 AP_DMA_BTIF_0_TX_VFF_LEN — BTIF TX Virtual FIFO Length Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

11000A28 AP_DMA_BTIF_0_TX_VFF_THRE — BTIF TX Virtual FIFO Threshold Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	**VFF threshold in byte alignment** In TX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

11000A2C AP_DMA_BTI — BTIF TX Virtual FIFO Write — 00000000

F_0_TX_VFF_WPT Pointer Register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	**TX VFF write pointer wrap bit** It is initialized to 0. When wrapped to the ring head again, invert this bit. For BTIF TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.
15:0	TX_VFF_WPT	**Byte alignment FIFO write pointer** For BTIF TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.

11000A30 AP_DMA_BTIF_0_TX_VFF_RPT BTIF TX Virtual FIFO Read Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_RPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	**TX VFF read pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	TX_VFF_RPT	**TX VFF read pointer maintained by hardware** In byte alignment.

11000A38 AP_DMA_BTIF_0_TX_INT_BUF_SIZE BTIF Tx Internal Buffer Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	**Virtual FIFO DMA TX internal buffer size** 0: 0 byte 1: 1 byte

11000A3C AP_DMA_BTIF_0_TX_VFF_VALID_SIZE **BTIF Tx Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	**TX virtual FIFO valid size** 0: 0 byte 1: 1 byte

11000A40 AP_DMA_BTIF_0_TX_VFF_LEFT_SIZE **BTIF Tx Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	**TX virtual FIFO left size** 0: 0 byte 1: 1 byte

11000A50 AP_DMA_BTIF_0_TX_DEBUG_STATUS_00 — **BTIF Tx Debug Status 00** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D							WD_ACT	RD_ACT	WREQ	RREQ		
Type				RO							RO	RO	RO	RO		
Reset				0	0	0	0	0			0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	

11000A54 AP_DMA_BTIF_0_TX_VFF_ADDR2 — **BTIF TX Virtual FIFO Base Address Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TX_VFF_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	TX_VFF_ADDR2	BTIF memory address bit[32]

11000A58 AP_DMA_BTIF_0_TX_VFF_WPT_VALID — **BTIF TX Virtual FIFO Write Pointer Register by HW Control** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO

Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	**TX VFF write pointer wrap bit** If FLUSH= 0, sync to TX_VFF_WPT_WRAP. If flush, it will not update the value untill the flush is finished.
15:0	TX_VFF_WPT_VALID	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

11000A5C **AP_DMA_BTIF_0_TX_VFF_WPT_VALID2** **BTIF TX Virtual FIFO Write Pointer Register by HW Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_WPT_VALID2	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

11000A60 **AP_DMA_BTIF_0_TX_FLUSH_ACT** **BTIF TX Virtual FIFO Flush Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLUSH_NEXT	FLUSH_ACT
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	**There is a flush command when the BTIF TX channel is flushing.**
0	FLUSH_ACT	**BTIF TX channel flush status**

Bit(s)	Name	Description

11000A64 AP_DMA_BTIF_0_TX_HW_FLUSH **BTIF TX Virtual FIFO HW Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HW_FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	**Flush control bit** Controls the BTIF TX write pointer if the SW setting value at flushing is updated. 0: Update wpt with SW setting 1: Update wpt when flush =0

11000A68 AP_DMA_BTIF_0_TX_VFF_WPT_REAL **BTIF TX Virtual FIFO Write Pointer Register Value** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_REAL
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_REAL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_REAL	**TX VFF write pointer wrap bit** If HW_FLUSH = 1, sync to TX_VFF_WPT_WRAP_VALID. If HW_FLUSH = 0, sync to TX_VFF_WPT_WRAP.
15:0	TX_VFF_WPT_REAL	**TX VFF write pointer** If HW_FLUSH = 1, sync to TX_VFF_WPT_VALID. If HW_FLUSH = 0, sync to TX_VFF_WPT.

11000680 AP_DMA_UART_0_RX_INT_FLAG **UART RX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLAG1	FLAG0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	**Write 1 to clear it.** This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF.
0	FLAG0	**Write 1 to clear it.** This flag is raised when rx_vff_valid_size >= rx_vff_thre. (VFF is almost full and MCU needs to consume those data.)

11000684 AP_DMA_UART_0_RX_INT_EN — **UART RX Virtual FIFO Interrupt Enable Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN1	INTEN0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	**Controls interrupt enabling** Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	**Controls interrupt enabling** Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable 1: Enable

11000688 AP_DMA_UART_0_RX_EN — **UART RX Virtual FIFO Enable Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART1 RX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1100068C AP_DMA_UART_0_RX_RST **UART RX Virtual FIFO Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000690 AP_DMA_UART_0_RX_STOP **UART RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																RW

Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART RX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

11000694 AP_DMA_UART_0_RX_FLUSH **UART RX Virtual FIFO Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART RX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Flush finished 1: Enable

1100069C AP_DMA_UART_0_RX_VFF_ADDR **UART RX Virtual FIFO Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	**UART memory address** Must be 8-byte aligned.

Bit(s)	Name	Description
		Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

110006A4 AP_DMA_UART_0_RX_VFF_LEN **UART RX Virtual FIFO Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

110006A8 AP_DMA_UART_0_RX_VFF_THRE **UART RX Virtual FIFO Threshold Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	**VFF threshold in byte alignment** In RX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In TX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

110006AC AP_DMA_UART_0_RX_VFF_WPT **UART RX Virtual FIFO Write Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP

Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	**RX VFF write pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_WPT	**RX VFF write pointer maintained by hardware** In byte alignment.

110006B0 AP_DMA_UART_0_RX_VFF_RPT — UART RX Virtual FIFO Read Pointer Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	**RX VFF read pointer wrap bit maintained by software** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_RPT	**RX VFF read pointer maintained by software** In byte alignment.

110006B4 AP_DMA_UART_0_RX_FLOW_CTRL_THRE — UART RX Virtual FIFO Flow Control Threshold — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	**VFF flow control threshold in byte alignment** In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

110006B8 AP_DMA_UART_0_RX_INT_BUF_SIZE **UART Rx Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**RX_INT_BUF_SIZE**				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	**Virtual FIFO DMA RX internal buffer size** 0: 0 byte 1: 1 byte

110006BC AP_DMA_UART_0_RX_VFF_VALID_SIZE **UART Rx Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RX_VFF_VALID_SIZE**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	**RX virtual FIFO valid size** 0: 0 byte 1: 1 byte

110006C0 AP_DMA_UART_0_RX_VFF_LEFT_SIZE **UART Rx Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	**RX virtual FIFO left size** 0: 0 byte 1: 1 byte

110006D0 AP_DMA_UART_0_RX_DEBUG_STATUS_00 **UART Rx Debug Status 00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADD R_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT		WD_ACT	RD_ACT	WREQ	RREQ		
Type				RO					RO		RO	RO	RO	RO		
Reset				0	0	0	0	0	0		0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	

110006D4 AP_DMA_UART_0_RX_VFF_ADDR2 **UART RX Virtual FIFO Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RX_VFF_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description

Bit(s)	Name	Description
0	RX_VFF_ADDR2	UART memory address bit[32]

11000780 AP_DMA_UART_1_RX_INT_FLAG **UART RX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLAG1	FLAG0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	**Write 1 to clear it.** This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF.
0	FLAG0	**Write 1 to clear it.** This flag is raised when rx_vff_valid_size >= rx_vff_thre. (VFF is almost full and MCU needs to consume those data.)

11000784 AP_DMA_UART_1_RX_INT_EN **UART RX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN1	INTEN0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	**Controls interrupt enabling** Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	**Controls interrupt enabling** Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable 1: Enable

11000788 AP_DMA_UART_1_RX_EN **UART RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART1 RX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1100078C AP_DMA_UART_1_RX_RST **UART RX Virtual FIFO Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000790 AP_DMA_UART_1_RX_STOP **UART RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART RX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

11000794 AP_DMA_UART_1_RX_FLUSH — **UART RX Virtual FIFO Flush Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART RX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Flush finished 1: Enable

1100079C AP_DMA_UART_1_RX_VFF_ADDR — **UART RX Virtual FIFO Base Address Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	**UART memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

110007A4 AP_DMA_UART_1_RX_VFF_LEN **UART RX Virtual FIFO Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

110007A8 AP_DMA_UART_1_RX_VFF_THRE **UART RX Virtual FIFO Threshold Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	**VFF threshold in byte alignment** In RX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In TX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

110007AC AP_DMA_UAR **UART RX Virtual FIFO Write** **00000000**

T_1_RX_VFF_WPT **Pointer Register**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	**RX VFF write pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_WPT	**RX VFF write pointer maintained by hardware** In byte alignment.

110007B0 **AP_DMA_UART_1_RX_VFF_RPT** **UART RX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	**RX VFF read pointer wrap bit maintained by software** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_RPT	**RX VFF read pointer maintained by software** In byte alignment.

110007B4 **AP_DMA_UART_1_RX_FLOW_CTRL_THRE** **UART RX Virtual FIFO Flow Control Threshold** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	**VFF flow control threshold in byte alignment** In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

110007B8 AP_DMA_UART_1_RX_INT_BUF_SIZE **UART Rx Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	**Virtual FIFO DMA RX internal buffer size** 0: 0 byte 1: 1 byte

110007BC AP_DMA_UART_1_RX_VFF_VALID_SIZE **UART Rx Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	**RX virtual FIFO valid size** 0: 0 byte 1: 1 byte

110007C0 AP_DMA_UART_1_RX_VFF **UART Rx Virtual FIFO Left Size Register** **00000000**

_LEFT_SIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	**RX virtual FIFO left size** 0: 0 byte 1: 1 byte

110007D0 AP_DMA_UART_1_RX_DEBUG_STATUS_00 **UART Rx Debug Status 00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT		WD_ACT	RD_ACT	WREQ	RREQ		
Type				RO					RO		RO	RO	RO	RO		
Reset				0	0	0	0	0	0		0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	

110007D4 AP_DMA_UART_1_RX_VFF_ADDR2 **UART RX Virtual FIFO Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RX_VFF_ADDR2

Type																RW
Reset																0

Bit(s)	Name	Description
0	RX_VFF_ADDR2	UART memory address bit[32]

11000880 AP_DMA_UART_2_RX_INT_FLAG **UART RX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLAG1	FLAG0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	**Write 1 to clear it.** This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF.
0	FLAG0	**Write 1 to clear it.** This flag is raised when rx_vff_valid_size >= rx_vff_thre. (VFF is almost full and MCU needs to consume those data.)

11000884 AP_DMA_UART_2_RX_INT_EN **UART RX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN1	INTEN0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	**Controls interrupt enabling** Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	**Controls interrupt enabling** Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag0

Bit(s)	Name	Description
		will still be set to 1 regardless of this bit. 0: Disable 1: Enable

11000888 AP_DMA_UART_2_RX_EN UART RX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART1 RX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1100088C AP_DMA_UART_2_RX_RST UART RX Virtual FIFO Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

Bit(s)	Name	Description

11000890 AP_DMA_UART_2_RX_STOP **UART RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART RX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

11000894 AP_DMA_UART_2_RX_FLUSH **UART RX Virtual FIFO Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART RX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Flush finished 1: Enable

1100089C AP_DMA_UAR **UART RX Virtual FIFO Base** **00000000**

AP_DMA_UART_2_RX_VFF_ADDR **Address Register**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	**UART memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

110008A4 **AP_DMA_UART_2_RX_VFF_LEN** **UART RX Virtual FIFO Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

110008A8 **AP_DMA_UART_2_RX_VFF_THRE** **UART RX Virtual FIFO Threshold Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	**VFF threshold in byte alignment**

Bit(s)	Name	Description
		In RX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In TX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

110008AC AP_DMA_UART_2_RX_VFF_WPT — **UART RX Virtual FIFO Write Pointer Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	**RX VFF write pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_WPT	**RX VFF write pointer maintained by hardware** In byte alignment.

110008B0 AP_DMA_UART_2_RX_VFF_RPT — **UART RX Virtual FIFO Read Pointer Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	**RX VFF read pointer wrap bit maintained by software** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_RPT	**RX VFF read pointer maintained by software** In byte alignment.

110008B4 AP_DMA_UART — **UART RX Virtual FIFO Flow** — **00000000**

T_2_RX_FLOW_CTRL_THRE **Control Threshold**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	**VFF flow control threshold in byte alignment** In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

110008B8 **AP_DMA_UART_T_2_RX_INT_BUF_SIZE** **UART Rx Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	**Virtual FIFO DMA RX internal buffer size** 0: 0 byte 1: 1 byte

110008BC **AP_DMA_UART_T_2_RX_VFF_VALID_SIZE** **UART Rx Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	**RX virtual FIFO valid size** 0: 0 byte 1: 1 byte

110008C0 AP_DMA_UART_2_RX_VFF_LEFT_SIZE **UART Rx Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	**RX virtual FIFO left size** 0: 0 byte 1: 1 byte

110008D0 AP_DMA_UART_2_RX_DEBUG_STATUS_00 **UART Rx Debug Status 00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADD R_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT		WD_ACT	RD_ACT	WREQ	RREQ		
Type				RO					RO		RO	RO	RO	RO		
Reset				0	0	0	0	0	0		0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	

110008D4 AP_DMA_UART_2_RX_VFF **UART RX Virtual FIFO Base Address Register** **00000000**

_ADDR2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RX_VFF_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	RX_VFF_ADDR2	UART memory address bit[32]

11000980 AP_DMA_UART_3_RX_INT_FLAG **UART RX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLAG1	FLAG0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	**Write 1 to clear it.** This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF.
0	FLAG0	**Write 1 to clear it.** This flag is raised when rx_vff_valid_size >= rx_vff_thre. (VFF is almost full and MCU needs to consume those data.)

11000984 AP_DMA_UART_3_RX_INT_EN **UART RX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN1	INTEN0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	**Controls interrupt enabling** Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	**Controls interrupt enabling** Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable 1: Enable

11000988 AP_DMA_UART_3_RX_EN **UART RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART1 RX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1100098C AP_DMA_UART_3_RX_RST **UART RX Virtual FIFO Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism.

Bit(s)	Name	Description
		0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000990 AP_DMA_UART_3_RX_STOP UART RX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART RX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

11000994 AP_DMA_UART_3_RX_FLUSH UART RX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART RX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again.

Bit(s)	Name	Description
		Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1100099C AP_DMA_UART_3_RX_VFF_ADDR **UART RX Virtual FIFO Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	**UART memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

110009A4 AP_DMA_UART_3_RX_VFF_LEN **UART RX Virtual FIFO Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

110009A8 AP_DMA_UART_3_RX_VFF_THRE **UART RX Virtual FIFO Threshold Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	**VFF threshold in byte alignment** In RX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In TX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

110009AC AP_DMA_UART_3_RX_VFF_WPT **UART RX Virtual FIFO Write Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	**RX VFF write pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_WPT	**RX VFF write pointer maintained by hardware** In byte alignment.

110009B0 AP_DMA_UART_3_RX_VFF_RPT **UART RX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	**RX VFF read pointer wrap bit maintained by software** It is initialized to 0. When wrapped to the ring head again, invert

Bit(s)	Name	Description
		this bit.
15:0	RX_VFF_RPT	**RX VFF read pointer maintained by software** In byte alignment.

110009B4 AP_DMA_UART_3_RX_FLOW_CTRL_THRE **UART RX Virtual FIFO Flow Control Threshold** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	**VFF flow control threshold in byte alignment** In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

110009B8 AP_DMA_UART_3_RX_INT_BUF_SIZE **UART Rx Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	**Virtual FIFO DMA RX internal buffer size** 0: 0 byte 1: 1 byte

110009BC AP_DMA_UART_3_RX_VFF_VALID_SIZE **UART Rx Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	**RX virtual FIFO valid size** 0: 0 byte 1: 1 byte

110009C0 AP_DMA_UART_3_RX_VFF_LEFT_SIZE **UART Rx Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	**RX virtual FIFO left size** 0: 0 byte 1: 1 byte

110009D0 AP_DMA_UART_3_RX_DEBUG_STATUS_00 **UART Rx Debug Status 00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADD R_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT		WD_ACT	RD_ACT	WREQ	RREQ		
Type				RO					RO		RO	RO	RO	RO		
Reset				0	0	0	0	0	0		0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
5	WD_ACT	
4	RD_ACT	

Bit(s)	Name	Description
3	WREQ	
2	RREQ	

110009D4 AP_DMA_UART_3_RX_VFF_ADDR2 — UART RX Virtual FIFO Base Address Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RX_VFF_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	RX_VFF_ADDR2	UART memory address bit[32]

11000A80 AP_DMA_BTIF_0_RX_INT_FLAG — BTIF RX Virtual FIFO Interrupt Flag Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLAG1	FLAG0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	**Write 1 to clear it.** This flag is raised when BTIF issues flush to DMA and all data in BTIF FIFO are transferred to VFF.
0	FLAG0	**Write 1 to clear it.** This flag is raised when rx_vff_valid_size >= rx_vff_thre. (VFF is almost full and MCU needs to consume those data.)

11000A84 AP_DMA_BTIF_0_RX_INT_EN — BTIF RX Virtual FIFO Interrupt Enable Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN1	INTEN0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	**Controls interrupt enabling** Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	**Controls interrupt enabling** Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable 1: Enable

11000A88 AP_DMA_BTIF_0_RX_EN **BTIF RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables BTIF1 RX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

11000A8C AP_DMA_BTIF_0_RX_RST **BTIF RX Virtual FIFO Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW

Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000A90 AP_DMA_BTIF_0_RX_STOP **BTIF RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**STOP**
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops BTIF RX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

11000A94 AP_DMA_BTIF_0_RX_FLUSH **BTIF RX Virtual FIFO Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**FLUSH**
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes BTIF RX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. *Note: STOP and FLUSH cannot be set to 1 in the same operation.* 0: Flush finished 1: Enable

11000A9C AP_DMA_BTIF_0_RX_VFF_ADDR **BTIF RX Virtual FIFO Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	**BTIF memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

11000AA4 AP_DMA_BTIF_0_RX_VFF_LEN **BTIF RX Virtual FIFO Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

11000AA8 AP_DMA_BTIF_0_RX_VFF **BTIF RX Virtual FIFO Threshold Register** **00000000**

_THRE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	**VFF threshold in byte alignment** In RX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In TX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

11000AAC AP_DMA_BTIF_0_RX_VFF_WPT **BTIF RX Virtual FIFO Write Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	**RX VFF write pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_WPT	**RX VFF write pointer maintained by hardware** In byte alignment.

11000AB0 AP_DMA_BTIF_0_RX_VFF_RPT **BTIF RX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	**RX VFF read pointer wrap bit maintained by software** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_RPT	**RX VFF read pointer maintained by software** In byte alignment.

11000AB4 AP_DMA_BTIF_0_RX_FLOW_CTRL_THRE — BTIF RX Virtual FIFO Flow Control Threshold — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	**VFF flow control threshold in byte alignment** In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

11000AB8 AP_DMA_BTIF_0_RX_INT_BUF_SIZE — BTIF Rx Internal Buffer Size Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	**Virtual FIFO DMA RX internal buffer size** 0: 0 byte 1: 1 byte

11000ABC AP_DMA_BTIF_0_RX_VFF_VALID_SIZ — BTIF Rx Virtual FIFO Valid Size Register — 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	**RX virtual FIFO valid size** 0: 0 byte 1: 1 byte

11000AC0 AP_DMA_BTIF_0_RX_VFF_LEFT_SIZE **BTIF Rx Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	**RX virtual FIFO left size** 0: 0 byte 1: 1 byte

11000AD0 AP_DMA_BTIF_0_RX_DEBUG_STATUS_00 **BTIF Rx Debug Status 00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT		WD_ACT	RD_ACT	WREQ	RREQ		
Type				RO					RO		RO	RO	RO	RO		
Reset				0	0	0	0	0	0		0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	

Bit(s)	Name	Description
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	

11000AD4 AP_DMA_BTIF_0_RX_VFF_ADDR2 **BTIF RX Virtual FIFO Base Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RX_VFF_ADDR2
Type																RW
Reset																0

Bit(s)	Name	Description
0	RX_VFF_ADDR2	BTIF memory address bit[32]

2 Clock and Power Control

2.1 Top Clock Generator

Module name: TOPCKGEN Base address: (+10000000h)

Address	Name	Width	Register Function
10000000	CLK_MODE	32	Clock 26M, 32K PDN Control Register
10000004	CLK_CFG_UPDATE	32	Clock Configuration Update Register
10000040	CLK_CFG_0	32	Function Clock Selection Register 0
10000044	CLK_CFG_0_SET	32	SET Control of CLK_CFG_0
10000048	CLK_CFG_0_CLR	32	CLR Control of CLK_CFG_0
10000050	CLK_CFG_1	32	Function Clock Selection Register 1
10000054	CLK_CFG_1_SET	32	SET Control of CLK_CFG_1
10000058	CLK_CFG_1_CLR	32	CLR Control of CLK_CFG_1
10000060	CLK_CFG_2	32	Function Clock Selection Register 2
10000064	CLK_CFG_2_SET	32	SET Control of CLK_CFG_2
10000068	CLK_CFG_2_CLR	32	CLR Control of CLK_CFG_2
10000070	CLK_CFG_3	32	Function Clock Selection Register 3
10000074	CLK_CFG_3_SET	32	SET Control of CLK_CFG_3
10000078	CLK_CFG_3_CLR	32	CLR Control of CLK_CFG_3
10000080	CLK_CFG_4	32	Function Clock Selection Register 4
10000084	CLK_CFG_4_SET	32	SET Control of CLK_CFG_4
10000088	CLK_CFG_4_CLR	32	CLR Control of CLK_CFG_4
10000090	CLK_CFG_5	32	Function Clock Selection Register 5
10000094	CLK_CFG_5_SET	32	SET Control of CLK_CFG_5
10000098	CLK_CFG_5_CLR	32	CLR Control of CLK_CFG_5
100000A0	CLK_CFG_6	32	Function Clock Selection Register 6
100000A4	CLK_CFG_6_SET	32	SET Control of CLK_CFG_6
100000A8	CLK_CFG_6_CLR	32	CLR Control of CLK_CFG_6
100000B0	CLK_CFG_7	32	Function Clock Selection Register 7
100000B4	CLK_CFG_7_SET	32	SET Control of CLK_CFG_7
100000B8	CLK_CFG_7_CLR	32	CLR Control of CLK_CFG_7
100000C0	CLK_CFG_8	32	Function Clock Selection Register 8
100000C4	CLK_CFG_8_SET	32	SET Control of CLK_CFG_8
100000C8	CLK_CFG_8_CLR	32	CLR Control of CLK_CFG_8
10000100	CLK_MEM_DFS_CFG	32	APHY feedback clock divider Control
10000104	CLK_MISC_CFG_0	32	Miscellaneous Control
10000108	CLK_MISC_CFG_1	32	Miscellaneous Control 1
1000010C	CLK_DBG_CFG	32	Clock Debug
10000110	CLKM_CFG_0	32	CLKM Control 0
10000114	CLKM_CFG_1	32	CLKM Control 1
10000118	CLKM_CFG_2	32	CLKM Control 2
10000200	CLK_SCP_CFG_0	32	SCP Control Register 0
10000204	CLK_SCP_CFG_1	32	SCP Control Register 1
10000220	CLK26CALI_0	32	Frequency Meter Control Register 0

Address	Name	Width	Register Function
10000224	CLK26CALI_1	32	Frequency Meter Control Register 1
1000022C	CKSTA_REG	32	Function Clock Selection Status Register
10000300	CLK_DDRPHY_REG	32	DDRPHY RREF Control

10000000 CLK_MODE — Clock 26M, 32K PDN Control Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					pdn_conn_26m	pdn_conn_32k	pdn_md_26m	pdn_md_32k								topckgen_en
Type					RW	RW	RW	RW								RW
Reset					0	0	0	0								0

Bit(s)	Name	Description
11	pdn_conn_26m	
10	pdn_conn_32k	
9	pdn_md_26m	**Reserved** Turns off 26M clock source to MD. Turn off this clock in flight mode. 1: Enable turn-off
8	pdn_md_32k	**Turns off 32K clock source to MD** Turn off this clock in flight mode. 1: Enable turn-off
0	topckgen_en	**Enables TOPCKGEN** 0: Enable 1: Disable

10000004 CLK_CFG_UPDATE — Clock Configuration Update Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	bsi_spi_ck_update	spm_ck_update	anc_md32_ck_update	ssusb_top_sys_ck_update	audio_h_ck_update	aud_2_ck_update	aud_1_ck_update	scam_ck_update	dpio_ck_update	mjc_ck_update	atb_ck_update	scp_ck_update	pmicspi_ck_update	aud_intbus_ck_update	audio_ck_update	msdc30_3_ck_update
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	msdc30_2_ck_update	msdc30_1_ck_update	msdc50_0_ck_update	msdc50_0_hclk_ck_update	usb20_ck_update	spi_ck_update	uart_ck_update	camtg_ck_update	mfg_ck_update	venc_ck_update	vdec_ck_update	pwm_ck_update	mm_ck_update	ddrphycfg_ck_update	mem_ck_update	axi_ck_update
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	bsi_spi_ck_update	Write 1 to update the change for clk_sel and clk_inv
30	spm_ck_update	Write 1 to update the change for clk_sel and clk_inv
29	anc_md32_ck_update	Write 1 to update the change for clk_sel and clk_inv
28	ssusb_top_sys_ck_update	Write 1 to update the change for clk_sel and clk_inv
27	audio_h_ck_update	Write 1 to update the change for clk_sel and clk_inv
26	aud_2_ck_update	Write 1 to update the change for clk_sel and clk_inv
25	aud_1_ck_update	Write 1 to update the change for clk_sel and clk_inv
24	scam_ck_update	Write 1 to update the change for clk_sel and clk_inv
23	dpi0_ck_update	Write 1 to update the change for clk_sel and clk_inv
22	mjc_ck_update	Write 1 to update the change for clk_sel and clk_inv
21	atb_ck_update	Write 1 to update the change for clk_sel and clk_inv
20	scp_ck_update	Write 1 to update the change for clk_sel and clk_inv
19	pmicspi_ck_update	Write 1 to update the change for clk_sel and clk_inv
18	aud_intbus_ck_update	Write 1 to update the change for clk_sel and clk_inv
17	audio_ck_update	Write 1 to update the change for clk_sel and clk_inv
16	msdc30_3_ck_update	Write 1 to update the change for clk_sel and clk_inv
15	msdc30_2_ck_update	Write 1 to update the change for clk_sel and clk_inv
14	msdc30_1_ck_update	Write 1 to update the change for clk_sel and clk_inv
13	msdc50_0_ck_update	Write 1 to update the change for clk_sel and clk_inv
12	msdc50_0_hclk_ck_update	Write 1 to update the change for clk_sel and clk_inv
11	usb20_ck_update	Write 1 to update the change for clk_sel and clk_inv
10	spi_ck_update	Write 1 to update the change for clk_sel and clk_inv
9	uart_ck_update	Write 1 to update the change for clk_sel and clk_inv
8	camtg_ck_update	Write 1 to update the change for clk_sel and clk_inv
7	mfg_ck_update	Write 1 to update the change for clk_sel and clk_inv
6	venc_ck_update	Write 1 to update the change for clk_sel and clk_inv
5	vdec_ck_update	Write 1 to update the change for clk_sel and clk_inv
4	pwm_ck_update	Write 1 to update the change for clk_sel and clk_inv
3	mm_ck_update	Write 1 to update the change for clk_sel and clk_inv
2	ddrphycfg_ck_update	Write 1 to update the change for clk_sel and clk_inv
1	mem_ck_update	Write 1 to update the change for clk_sel and clk_inv
0	axi_ck_update	Write 1 to update the change for clk_sel and clk_inv

10000040 CLK_CFG_0 **Function Clock Selection Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_mm			clk_mm_inv			clk_mm_sel		pdn_ddrphycfg			clk_ddrphycfg_inv			clk_ddrphycfg_sel	
Type	RW			RW			RW		RW			RW			RW	
Reset	0			0			0	0	0			0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_mem			clk_mem_inv				clk_mem_sel				clk_axi_inv	ulposc_axi_ck_mux_pre	ulposc_axi_ck_mux	clk_axi_sel	
Type	RW			RW				RW				RW	RW	RW	RW	
Reset	0			0				0				0	0	0	0	0

Bit(s)	Name	Description
31	pdn_mm	**Turns off hf_fmm_ck** 1: Enable clock off
28	clk_mm_inv	**Inverts hf_fmm_ck clock phase** 1: Enable phase inversion

Bit(s)	Name	Description
25:24	clk_mm_sel	**Selects hf_fmm_ck clock mux** 0: clk26m 1: imgpll_ck 2: univpll1_d2 3: syspll1_d2
23	pdn_ddrphycfg	**Turns off hf_fddrphycfg_ck** 1: Enable clock off
20	clk_ddrphycfg_inv	**Inverts hf_fddrphycfg_ck clock phase** 1: Enable phase inversion
17:16	clk_ddrphycfg_sel	**Selects hf_fddrphycfg_ck clock mux** 0: clk26m 1: syspll3_d2 2: syspll2_d4 3: syspll1_d8
15	pdn_mem	1: Enable clock off
12	clk_mem_inv	**Inverts hf_fmem_ck clock phase** 1: Enable phase inversion
8	clk_mem_sel	**Selects hf_fmem_ck clock mux** 0: clk26m 1: dmpll_ck
4	clk_axi_inv	**Inverts hf_faxi_ck clock phase** 1: Enable phase inversion
3	ulposc_axi_ck_mux_pre	**Selects ulposc_axi_ck_mux_pre** 0: LPOSC/2 1: LPOSC/3
2	ulposc_axi_ck_mux	**Selects ulposc_axi_ck_mux** 0: syspll1_d4 1: LPOSC_axi_ck_mux_pre
1:0	clk_axi_sel	**Selects hf_faxi_ck clock mux** 0: clk26m 1: syspll_d7 2: LPOSC_axi_ck_mux

10000044 CLK_CFG_0_SET **SET Control of CLK_CFG_0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_0_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_0_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_0_set	**Sets up the correspondent bit of CLG_CFG_SEL_0** 0: Unchange 1: Set 1'b1 to the correspondent bit

10000048 CLK_CFG_0_CLR **CLR Control of CLK_CFG_0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_0_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_0_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_0_clr	**Clears the correspondent bit of CLG_CFG_SEL_0** 0: Unchange 1: Set 1'b0 to the correspondent bit

10000050 CLK_CFG_1 **Function Clock Selection Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_mfg			clk_mfg_inv			clk_mfg_sel		pdn_venc			clk_venc_inv			clk_venc_sel	
Type	RW			RW			RW		RW			RW			RW	
Reset	0			0			0	0	0			0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_vdec			clk_vdec_inv		clk_vdec_sel			pdn_pwm			clk_pwm_inv		clk_pwm_sel		
Type	RW			RW		RW			RW			RW		RW		
Reset	0			0		0	0	0	0			0		0	0	0

Bit(s)	Name	Description
31	pdn_mfg	**Turns off hf_fmfg_ck** 1: Enable clock off
28	clk_mfg_inv	**Inverts hf_fmfg_ck clock phase** 1: Enable phase inversion
25:24	clk_mfg_sel	**Selects hf_fmfg_ck clock mux** 0: clk26m 1: mfgpll_ck 2: syspll_d3 3: univpll_d3
23	pdn_venc	**Turns off hf_fvenc_ck** 1: Enable clock off
20	clk_venc_inv	**Inverts hf_fvenc_ck clock phase** 1: Enable phase inversion
17:16	clk_venc_sel	**Selects hf_fvenc_ck clock mux** 0: clk26m 1: codecpll_ck 2: syspll_d3
15	pdn_vdec	**Turns off hf_fvdec_ck** 1: Enable clock off
12	clk_vdec_inv	**Inverts hf_fvdec_ck clock phase** 1: Enable phase inversion
10:8	clk_vdec_sel	**Selects hf_fvdec_ck clock mux** 0: clk26m 1: vdecpll_ck

Bit(s)	Name	Description
		2: imgpll_ck 3: syspll_d3 4: univpll_d5 5: clk26m 6: clk26m
7	pdn_pwm	**Turns off f_fpwm_ck** 1: Enable clock off
4	clk_pwm_inv	**Inverts f_fpwm_ck clock phase** 1: Enable phase inversion
2:0	clk_pwm_sel	**Selects f_fpwm_ck clock mux** 0: clk26m 1: univpll2_d4 2: LPOSC/2 3: LPOSC/3 4: LPOSC/8 5: LPOSC/10 6: LPOSC/4

10000054 CLK_CFG_1_SET **SET Control of CLK_CFG_1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_1_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_1_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_1_set	**Sets up the correspondent bit of CLG_CFG_SEL_1** 0: Unchange 1: Set 1'b1 to the correspondent bit

10000058 CLK_CFG_1_CLR **CLR Control of CLK_CFG_1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_1_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_1_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_1_clr	**Clears the correspondent bit of CLG_CFG_SEL_1** 0: Unchange 1: Set 1'b0 to the correspondent bit

Bit(s)	Name	Description

10000060 CLK_CFG_2 **Function Clock Selection Register 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_usb20			clk_usb20_inv			clk_usb20_sel		pdn_spi			clk_spi_inv		ulposc_spi_ck_mux	clk_spi_sel	
Type	RW			RW			RW		RW			RW		RW	RW	
Reset	0			0			0	0	0			0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_uart			clk_uart_inv				clk_uart_sel	pdn_camtg			clk_camtg_inv			clk_camtg_sel	
Type	RW			RW				RW	RW			RW			RW	
Reset	0			0				0	0			0			0	0

Bit(s)	Name	Description
31	pdn_usb20	**Turns off h_usb20_ck** 1: Enable clock off
28	clk_usb20_inv	**Inverts h_usb20_ck clock phase** 1: Enable phase inversion
25:24	clk_usb20_sel	**Selects h_usb20_ck clock mux** 0: clk26m 1: univpll1_d8 2: syspll4_d2
23	pdn_spi	**Turns off hf_fspi_ck** 1: Enable clock off
20	clk_spi_inv	**Inverts h f_fspi_ck clock phase** 1: Enable phase inversion
18	ulposc_spi_ck_mux	**Selects ulposc_spi_ck_mux** 0: LPOSC/2 1: LPOSC/3
17:16	clk_spi_sel	**Selects hf_fspi_ck clock mux** 0: clk26m 1: syspll3_d2 2: syspll2_d4 3: LPOSC_spi_ck_mx
15	pdn_uart	**Turns off f_fuart_ck** 1: Enable clock off
12	clk_uart_inv	**Inverts f_fuart_ck clock phase** 1: Enable phase inversion
8	clk_uart_sel	**Selects f_fuart_ck clock mux** 0: clk26m 1: univpll2_d8
7	pdn_camtg	**Turns off hf_fcamtg_ck** 1: Enable clock off
4	clk_camtg_inv	**Inverts hf_fcamtg_ck clock phase** 1: Enable phase inversion
1:0	clk_camtg_sel	**Selects hf_fcamtg_ck clock mux** 0: clk26m 1: univpll_d26 2: univpll2_d2

Bit(s)	Name	Description

10000064 CLK_CFG_2_SET **SET Control of CLK_CFG_2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_2_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_2_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_2_set	**Sets up the correspondent bit of CLG_CFG_SEL_2** 0: Unchange 1: Set 1'b1 to the correspondent bit

10000068 CLK_CFG_2_CLR **CLR Control of CLK_CFG_2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_2_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_2_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_2_clr	**Clears the correspondent bit of CLG_CFG_SEL_2** 0: Unchange 1: Set 1'b0 to the correspondent bit

10000070 CLK_CFG_3 **Function Clock Selection Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_msdc30_1			clk_msdc30_1_inv		clk_msdc30_1_sel			pdn_msdc50_0			clk_msdc50_0_inv	clk_msdc50_0_sel			
Type	RW			RW		RW			RW			RW	RW			
Reset	0			0		0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_msdc50_0_hclk			clk_msdc50_0_hclk_inv			clk_msdc50_0_hclk_sel									

Type	RW			RW			RW									
Reset	0			0			0	0								

Bit(s)	Name	Description
31	pdn_msdc30_1	**Turns off hf_fmsdc30_1_ck** 1: Enable clock off
28	clk_msdc30_1_inv	**Inverts hf_fmsdc30_1_ck clock phase** 1: Enable phase inversion
26:24	clk_msdc30_1_sel	**Selects hf_fmsdc30_1_ck clock mux** 0: clk26m 1: univpll2_d2 2: msdcpll_d2 3: univpll1_d4 4: syspll2_d2 5: syspll_d7 6: univpll_d7
23	pdn_msdc50_0	**Turns off hf_fmsdc50_0_ck** 1: Enable clock off
20	clk_msdc50_0_inv	**Inverts hf_fmsdc50_0_ck clock phase** 1: Enable phase inversion
19:16	clk_msdc50_0_sel	**Selects hf_fmsdc50_0_ck clock mux** 0: clk26m 1: msdcpll 2: syspll_d3 3: univpll1_d4 4: syspll2_d2 5: syspll_d7 6: msdcpll_d2 7: univpll1_d2 8: univpll_d3
15	pdn_msdc50_0_hclk	**Turns off hf_fmsdc50_0_hclk_ck** 1: Enable clock off
12	clk_msdc50_0_hclk_inv	**Inverts hf_fmsdc50_0_hclk_ck clock phase** 1: Enable phase inversion
9:8	clk_msdc50_0_hclk_sel	**Selects hf_fmsdc50_0_hclk_ck clock mux** 0: clk26m 1: syspll1_d2 2: syspll2_d2 3: syspll4_d2

10000074 CLK_CFG_3_SET SET Control of CLK_CFG_3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_3_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_3_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_3_set	**Sets up the correspondent bit of CLG_CFG_SEL_3**

Bit(s)	Name	Description
		0: Unchange 1: Set 1'b1 to the correspondent bit

10000078 CLK_CFG_3_CLR **CLR Control of CLK_CFG_3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_3_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_3_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_3_clr	**Clears the correspondent bit of CLG_CFG_SEL_3** 0: Unchange 1: Set 1'b0 to the correspondent bit

10000080 CLK_CFG_4 **Function Clock Selection Register 4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_aud_intbus			clk_aud_intbus_inv			clk_aud_intbus_sel		pdn_audio			clk_audio_inv			clk_audio_sel	
Type	RW			RW			RW		RW			RW			RW	
Reset	0			0			0	0	0			0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									pdn_msdc30_2			clk_msdc30_2_inv		clk_msdc30_2_sel		
Type									RW			RW		RW		
Reset									0			0		0	0	0

Bit(s)	Name	Description
31	pdn_aud_intbus	**Turns off hf_faud_intbus_ck** 1: Enable clock off
28	clk_aud_intbus_inv	**Inverts hf_faud_intbus_ck clock phase** 1: Enable phase inversion
25:24	clk_aud_intbus_sel	**Selects hf_faud_intbus_ck clock mux** 0: clk26m 1: syspll1_d4 2: syspll4_d2
23	pdn_audio	**Turns off hf_faudio_ck** 1: Enable clock off
20	clk_audio_inv	**Inverts hf_faudio_ck clock phase** 1: Enable phase inversion
17:16	clk_audio_sel	**Selects hf_faudio_ck clock mux**

Bit(s)	Name	Description
		0: clk26m 1: syspll3_d4 2: syspll4_d4 3: syspll1_d16
7	pdn_msdc30_2	**Turns off hf_fmsdc30_2_ck** 1: Enable clock off
4	clk_msdc30_2_inv	**Inverts hf_fmsdc30_2_ck clock phas** 1: Enable phase inversion
2:0	clk_msdc30_2_sel	**Selects hf_fmsdc30_2_ck clock mux** 0: clk26m 1: univpll2_d8 2: syspll2_d8 3: syspll1_d8 4: mscpll_d8 5: syspll3_d4 6: univpll_d26

10000084 CLK_CFG_4_SET **SET Control of CLK_CFG_4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_4_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_4_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_4_set	**Sets up the correspondent bit of CLG_CFG_SEL_4** 0: Unchange 1: Set 1'b1 to the correspondent bit

10000088 CLK_CFG_4_CLR **CLR Control of CLK_CFG_4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_4_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_4_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_4_clr	**Clears the correspondent bit of CLG_CFG_SEL_4** 0: Unchange 1: Set 1'b0 to the correspondent bit

10000090 CLK_CFG_5 **Function Clock Selection Register 5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_mjc			clk_mjc_inv			clk_mjc_sel		pdn_atb			clk_atb_inv			clk_atb_sel	
Type	RW			RW			RW		RW			RW			RW	
Reset	0			0			0	0	0			0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_scp			clk_scp_inv			clk_scp_sel		pdn_pmicspi			clk_pmicspi_inv		clk_pmicspi_sel		
Type	RW			RW			RW		RW			RW		RW		
Reset	0			0			0	0	0			0		0	0	0

Bit(s)	Name	Description
31	pdn_mjc	**Turns off hf_fmjc_ck** 1: Enable clock off
28	clk_mjc_inv	**Inverts clock phase** 1: Enable phase inversion
25:24	clk_mjc_sel	**Selects hf_fmjc_ck clock mux** 0: clk26m 1: imgpll_ck 2: univpll_d5 3: syspll1_d2
23	pdn_atb	**Turns off hf_atb_ck** 1: Enable clock off
20	clk_atb_inv	**Inverts hf_atb_ck clock phase** 1: Enable phase inversion
17:16	clk_atb_sel	**Selects hf_atb_ck clock mux** 0: clk26m 1: syspll1_d2 2: syspll_d5
15	pdn_scp	**Turns off hf_fscp_ck** 1: Enable clock off
12	clk_scp_inv	**Inverts hf_fscp_ck clock phase** 1: Enable phase inversion
9:8	clk_scp_sel	**Selects hf_fscp_ck clock mux** 0: clk26m 1: syspll_d3 2: LPOSC 3: univpll_d5
7	pdn_pmicspi	**Turns off hf_fpmicspi_ck** 1: Enable clock off
4	clk_pmicspi_inv	**Inverts hf_fpmicspi_ck clock phase** 1: Enable phase inversion
2:0	clk_pmicspi_sel	**Selects hf_fpmicspi_ck clock mu** 0: clk26m 1: univpll_d26 2: syspll3_d4 3: syspll1_d8 4: LPOSC/4 5: LPOSC/8 6: syspll2_d8

10000094 CLK_CFG_5_SET — SET Control of CLK_CFG_5 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_5_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_5_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_5_set	**Sets up the correspondent bit of CLG_CFG_SEL_5** 0: Unchange 1: Set 1'b1 to the correspondent bit

10000098 CLK_CFG_5_CLR — CLR Control of CLK_CFG_5 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_5_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_5_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_5_clr	**Clears the correspondent bit of CLG_CFG_SEL_5** 0: Unchange 1: Set 1'b0 to the correspondent bit

100000A0 CLK_CFG_6 — Function Clock Selection Register 6 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_aud_2			clk_aud_2_inv				clk_aud_2_sel	pdn_aud_1			clk_aud_1_inv				clk_aud_1_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									pdn_dpio			clk_dpio_inv		clk_dpio_sel		
Type									RW			RW		RW		
Reset									0			0		0	0	0

Bit(s)	Name	Description
31	pdn_aud_2	**Turns off hf_faud_2_ck** 1: Enable clock off

Bit(s)	Name	Description
28	clk_aud_2_inv	**Inverts hf_faud_2_ck clock phase** 1: Enable phase inversion
24	clk_aud_2_sel	**Selects hf_faud_2_ck clock mux** 0: clk26m 1: apll2_ck
23	pdn_aud_1	**Turns off hf_faud_1_ck** 1: Enable clock off
20	clk_aud_1_inv	**Inverts hf_faud_1_ck clock phase** 1: Enable phase inversion
16	clk_aud_1_sel	**Selects hf_faud_1_ck clock mux** 0: clk26m 1: apll1_ck
7	pdn_dpio	**Turns off hf_fdpio_ck** 1: Enable clock off
4	clk_dpio_inv	**Inverts hf_fdpio_ck clock phase** 1: Enable phase inversion
2:0	clk_dpio_sel	**Selects hf_fdpio_ck clock mux** 0: clk26m 1: tvdpll_d2 2: tvdpll_d4 3: tvdpll_d8 4: tvdpll_d16 5: clk26m 6: clk26m

100000A4 CLK_CFG_6_SET **SET Control of CLK_CFG_6** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_6_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_6_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_6_set	**Sets up the correspondent bit of CLG_CFG_SEL_6** 0: Unchange 1: Set 1'b1 to the correspondent bit

100000A8 CLK_CFG_6_CLR **CLR Control of CLK_CFG_6** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_6_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_6_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_6_clr	**Clears the correspondent bit of CLG_CFG_SEL_6** 0: Unchange 1: Set 1'b0 to the correspondent bit

100000B0 CLK_CFG_7 **Function Clock Selection Register 7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_ssusb_top_sys			clk_ssusb_top_sys_inv				clk_ssusb_top_sys_sel								
Type	RW			RW				RW								
Reset	0			0				0								

Bit(s)	Name	Description
15	pdn_ssusb_top_sys	**Turns off f_fssusb_top_sys_ck** 1: Enable clock off
12	clk_ssusb_top_sys_inv	**Inverts f_fssusb_top_sys_ck clock phase** 1: Enable phase inversion
8	clk_ssusb_top_sys_sel	**Selects f_fssusb_top_sys_ck clock mux** 0: clk26m 1: univpll3_d2

100000B4 CLK_CFG_7_SET **SET Control of CLK_CFG_7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_7_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_7_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_7_set	**Sets up the correspondent bit of CLG_CFG_SEL_7** 0: Unchange 1: Set 1'b1 to the correspondent bit

100000B8 CLK_CFG_7_CLR **CLR Control of CLK_CFG_7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	clk_cfg_7_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_7_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_7_clr	**Clears the correspondent bit of CLG_CFG_SEL_7** 0: Unchange 1: Set 1'b0 to the correspondent bit

100000C0 CLK_CFG_8 **Function Clock Selection Register 8** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_anc_md32			clk_anc_md32_inv			clk_anc_md32_sel		pdn_audio_h			clk_audio_h_inv			clk_audio_h_sel	
Type	RW			RW			RW		RW			RW			RW	
Reset	0			0			0	0	0			0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_bsi_spi			clk_bsi_spi_inv			clk_bsi_spi_sel		pdn_spm			clk_spm_inv				clk_spm_sel
Type	RW			RW			RW		RW			RW				RW
Reset	0			0			0	0	0			0				0

Bit(s)	Name	Description
31	pdn_anc_md32	**Turns off hf_fanc_md32_ck** 1: Enable clock off
28	clk_anc_md32_inv	**Inverts hf_fanc_md32_ck clock phase** 1: Enable phase inversion
25:24	clk_anc_md32_sel	**Selects hf_fanc_md32_ck clock mux** 0: clk26m 1: syspll1_d2 2: univpll_d5
23	pdn_audio_h	**Turns off hf_faudio_h_ck** 1: Enable clock off
20	clk_audio_h_inv	**Inverts hf_faudio_h_ck clock phase** 1: Enable phase inversion
17:16	clk_audio_h_sel	**Selects hf_faudio_h_ck clock mux** 0: clk26m 1: apll2_ck 2: apll1_ck 3: univpll_d7
15	pdn_bsi_spi	**Turns off hf_fbsi_spi_ck** 1: Enable clock off
12	clk_bsi_spi_inv	**Inverts hf_fbsi_spi_ck clock phase** 1: Enable phase inversion
9:8	clk_bsi_spi_sel	**Selects hf_fbsi_spi_ck clock mux** 0: clk26m 1: syspll_d3_d3

Bit(s)	Name	Description
		2: syspll1_d4 3: syspll_d7
7	pdn_spm	**Turns off hg_fspm_ck** 1: Enable clock off
4	clk_spm_inv	**Inverts hg_fspm_ck clock phase** 1: Enable phase inversion
0	clk_spm_sel	**Selects hg_fspm_ck clock mux** 0: clk26m 1: syspll1_d8

100000C4 CLK_CFG_8_SET **SET Control of CLK_CFG_8** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_8_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_8_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_8_set	**Sets up the correspondent bit of CLG_CFG_SEL_8** 0: Unchange 1: Set 1'b1 to the correspondent bit

100000C8 CLK_CFG_8_CLR **CLR Control of CLK_CFG_8** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_8_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_8_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_8_clr	**Clears the correspondent bit of CLG_CFG_SEL_8** 0: Unchange 1: Set 1'b0 to the correspondent bit

10000100 CLK_MEM_DFS_CFG **APHY feedback clock divider Control** **00000100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				sc_emi_clk_cho_off_enable				ddrphy_fb_ck_force_on				ddrphy_fb_en	ddrphy_fb_cnt			
Type				RW				RW				RW	RW			
Reset				0				1				0	0	0	0	0

Bit(s)	Name	Description
12	sc_emi_clk_cho_off_enable	**Enables control from SPM** 0: Disable control from SPM 1: Enable control from SPM
8	ddrphy_fb_ck_force_on	**Forces on feedback clock divider clock** 0: Disalbe force-on 1: Force on feedback clock (not divide)
4	ddrphy_fb_en	**Enables feedback clock divider** 0: Disable clock divider 1: Enable clock divider
3:0	ddrphy_fb_cnt	**Feedback clock divider** 0000: Divide by 1 0001: Divide by 2 0011: Divide by 4 0111: Divide by 8 1111: Divide by 16

10000104 CLK_MISC_CFG_0 **Miscellaneous Control** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ckgen_k1								arm_k1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								abist_osc_ck_mon_en						mfg_52m_sel		pdn_mfg_52m_ck
Type								RW						RW		RW
Reset								0						0	0	0

Bit(s)	Name	Description
31:24	ckgen_k1	**Configures frequency meter divider (top_fqmtr)**
23:16	arm_k1	**For ARMPLL1**
8	abist_osc_ck_mon_en	**Enables AD_OSC_CK for abist monitor** 0: Disable AD_OSC_CK to abist 1: Enable AD_OSC_CK to abist
2:1	mfg_52m_sel	**Selects MFG 26M/52M/104M** 00: 26M 01: 52M 10: 104M 11: 104M
0	pdn_mfg_52m_ck	**Turns off mfg_52m_ck** 0: Enable clock

Bit(s)	Name	Description
		1: Disable clock

10000108 CLK_MISC_CFG_1 **Miscellaneous Control 1** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	arm_k3								arm_k2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31:24	arm_k3	For ARMPLL3
23:16	arm_k2	For ARMPLL2

1000010C CLK_DBG_CFG **Clock Debug** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	mipi_clk_dbg_sel			clkm_clk_out							abist_ck_sel					
Type	RW			RW							RW					
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				k2_topckgen_ck_dbg_sel											fqmtr_ck_sel	
Type				RW											RW	
Reset				0	0	0	0	0							0	0

Bit(s)	Name	Description
31:29	mipi_clk_dbg_sel	For mipi dbg sel
28:24	clkm_clk_out	
21:16	abist_ck_sel	
12:8	k2_topckgen_ck_dbg_sel	
1:0	fqmtr_ck_sel	

10000110 CLKM_CFG_0 **CLKM Control 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clkmgen_k1_1											clkm_ck_en_1	clkm_mux_sel_1			
Type	RW											RW	RW			
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clkmgen_k1_0											clkm_ck_en_0	clkm_mux_sel_0			

Type	RW											RW	RW			
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
31:24	clkmgen_k1_1	**CLKM_1 divider**
20	clkm_ck_en_1	**Enables CLKM_1** 0: Disable clock output 1: Enable clock outout
19:16	clkm_mux_sel_1	**Selects CLKM_1 mux** 0000: No clock 0001: No clock 0010: 32K 0011: 26M 0100: 48M 0101: 156M 0110: 180.6M 0111: 196.6M 1000: 208M 1001: 249.6M
15:8	clkmgen_k1_0	**CLKM_0 divider**
4	clkm_ck_en_0	**Enables CLKM_0** 0: Disable clock output 1: Enable clock outout
3:0	clkm_mux_sel_0	**Selects CLKM_0 mux** 0000: No clock 0001: No clock 0010: 32K 0011: 26M 0100: 48M 0101: 156M 0110: 180.6M 0111: 196.6M 1000: 208M 1001: 249.6M

10000114 CLKM_CFG_1 CLKM Control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clkmgen_k 1_3											clkm_ck_en_3	clkm_mux_sel_3			
Type	RW											RW	RW			
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clkmgen_k1_2											clkm_ck_en_2	clkm_mux_sel_2			
Type	RW											RW	RW			
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
31:24	clkmgen_k1_3	**CLKM_3 divider**
20	clkm_ck_en_3	**Enables CLKM_3** 0: Disable clock output 1: Enable clock outout

Bit(s)	Name	Description
19:16	clkm_mux_sel_3	**Selects CLKM_3 mux** 0000: No clock 0001: No clock 0010: 32K 0011: 26M 0100: 48M 0101: 156M 0110: 180.6M 0111: 196.6M 1000: 208M 1001: 249.6M
15:8	clkmgen_k1_2	**CLKM_2 divider**
4	clkm_ck_en_2	**Enables CLKM_2** 0: Disable clock output 1: Enable clock outout
3:0	clkm_mux_sel_2	**Selects CLKM_2 mux** 0000: No clock 0001: No clock 0010: 32K 0011: 26M 0100: 48M 0101: 156M 0110: 180.6M 0111: 196.6M 1000: 208M 1001: 249.6M

10000118 CLKM_CFG_2 CLKM Control 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clkmgen_k 1_5											clkm_ck_en_5	clkm_mux_sel_5			
Type	RW											RW	RW			
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clkmgen_k1_4											clkm_ck_en_4	clkm_mux_sel_4			
Type	RW											RW	RW			
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
31:24	clkmgen_k1_5	**CLKM_5 divider**
20	clkm_ck_en_5	**Enables CLKM_5** 0: Disable clock output 1: Enable clock outout
19:16	clkm_mux_sel_5	**Selects CLKM_5 mux** 0000: No clock 0001: No clock 0010: 32K 0011: 26M 0100: 48M 0101: 156M 0110: 180.6M

Bit(s)	Name	Description
		0111: 196.6M 1000: 208M 1001: 249.6M
15:8	clkmgen_k1_4	**CLKM_4 divider**
4	clkm_ck_en_4	**Enables CLKM_4** 0: Disable clock output 1: Enable clock outout
3:0	clkm_mux_sel_4	**Selects CLKM_4 mux** 0000: No clock 0001: No clock 0010: 32K 0011: 26M 0100: 48M 0101: 156M 0110: 180.6M 0111: 196.6M 1000: 208M 1001: 249.6M

10000200 CLK_SCP_CFG_0 **SCP Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					sc_armck_3_off_en	sc_armck_2_off_en	sc_mac_26m_off_en	sc_md2_26m_off_en	sc_md2_32k_off_en	sc_md_26m_off_en	sc_md_32k_off_en	sc_armck_1_off_en	sc_smick_off_en	sc_axick_off_en	sc_memck_off_en	sc_26ck_off_en
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	sc_armck_3_off_en	**No this control** 0: Disable scpsys clock off control 1: Enable scpsys clock off control
10	sc_armck_2_off_en	**No this control** 0: Disable scpsys clock off control 1: Enable scpsys clock off control
9	sc_mac_26m_off_en	**MIPI CSI 26M** 0: Disable scpsys clock off control 1: Enable scpsys clock off control
8	sc_md2_26m_off_en	**No this control** 0: Disable scpsys clock off control 1: Enable scpsys clock off control
7	sc_md2_32k_off_en	**connsys 32K** 0: Disable scpsys clock off control 1: Enable scpsys clock off control
6	sc_md_26m_off_en	**mdsys 32K** 0: Disable scpsys clock off control 1: Enable scpsys clock off control
5	sc_md_32k_off_en	**mdsys 26M**

Bit(s)	Name	Description
		0: Disable scpsys clock off control 1: Enable scpsys clock off control
4	sc_armck_1_off_en	**No this control** 0: Disable scpsys clock off control 1: Enable scpsys clock off control
3	sc_smick_off_en	**No this control** 0: Disable scpsys clock off control 1: Enable scpsys clock off control
2	sc_axick_off_en	**AXI bus clock OFF** 0: Disable scpsys clock off control 1: Enable scpsys clock off control
1	sc_memck_off_en	**mem bus clock off** 0: Disable scpsys clock off control 1: Enable scpsys clock off control
0	sc_26ck_off_en	**All 26M clock off** 0: Disable scpsys clock off control 1: Enable scpsys clock off control

10000204 CLK_SCP_CFG_1 **SCP Control Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														sc_scpck_26m_sel_en		sc_axick_26m_sel_en
Type														RW		RW
Reset														0		0

Bit(s)	Name	Description
2	sc_scpck_26m_sel_en	0: Disable scpsys clock off control 1: Enable scpsys clock off control
0	sc_axick_26m_sel_en	0: Disable scpsys clock off control 1: Enable scpsys clock off control

10000220 CLK26CALI **Frequency Meter Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				fmeter_en				ckgen_clk_exec				ckgen_tri_cal				pll_test
Type				RW				RW				RW				RW

Reset				0				0				0				0

Bit(s)	Name	Description
12	fmeter_en	0: Disable fmeter 1: Enable fmeter
8	ckgen_clk_exc	**Selects measuring clock** 0: f_fckgen_ck 1: CLK26M
4	ckgen_tri_cal	**Triggers frequency meter on f_fckgen_ck** Auto-cleared when calibration is done. 0: Disable 1: Enable
0	pll_test	**Selects clock divider test clock** 0: PLL 1: Test clock (26MHz)

10000224 CLK26CALI_1 **Frequency Meter Control Register 1** **03FF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ckgen_load_cnt									
Type							RW									
Reset							1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cal_cnt															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	ckgen_load_cnt	
15:0	cal_cnt	**Frequency meter result of f_ckgen_ck** Frequency = (26MHz*cal_cnt)/(ckgen_load_cnt + 1)

1000022C CKSTA_REG **Function Clock Selection Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	chg_bsi_spi	chg_spm	chg_anc_md32	chg_ssusb_top_sys	chg_audio_h	chg_aud_2	chg_aud_1	chg_scam	chg_dpio	chg_mjc	chg_atb	chg_scp	chg_pmicspi	chg_aud_intbus	chg_audio	chg_msdc30_3
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chg_msdc30_2	chg_msdc30_1	chg_msdc50_0	chg_msdc50_0_hclk	chg_usb20	chg_spi	chg_uart	chg_camtg	chg_mfg	chg_venc	chg_vdec	chg_pwm	chg_mm	chg_ddrphycfg	chg_mem	chg_axi
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	chg_bsi_spi	Clock switches changing in progress

Bit(s)	Name	Description
30	chg_spm	Clock switches changing in progress
29	chg_anc_md32	Clock switches changing in progress
28	chg_ssusb_top_sys	Clock switches changing in progress
27	chg_audio_h	Clock switches changing in progress
26	chg_aud_2	Clock switches changing in progress
25	chg_aud_1	Clock switches changing in progress
24	chg_scam	Clock switches changing in progress
23	chg_dpi0	Clock switches changing in progress
22	chg_mjc	Clock switches changing in progress
21	chg_atb	Clock switches changing in progress
20	chg_scp	Clock switches changing in progress
19	chg_pmicspi	Clock switches changing in progress
18	chg_aud_intbus	Clock switches changing in progress
17	chg_audio	Clock switches changing in progress
16	chg_msdc30_3	Clock switches changing in progress
15	chg_msdc30_2	Clock switches changing in progress
14	chg_msdc30_1	Clock switches changing in progress
13	chg_msdc50_0	Clock switches changing in progress
12	chg_msdc50_0_hclk	Clock switches changing in progress
11	chg_usb20	Clock switches changing in progress
10	chg_spi	Clock switches changing in progress
9	chg_uart	Clock switches changing in progress
8	chg_camtg	Clock switches changing in progress
7	chg_mfg	Clock switches changing in progress
6	chg_venc	Clock switches changing in progress
5	chg_vdec	Clock switches changing in progress
4	chg_pwm	Clock switches changing in progress
3	chg_mm	Clock switches changing in progress
2	chg_ddrphycfg	Clock switches changing in progress
1	chg_mem	Clock switches changing in progress
0	chg_axi	Clock switches changing in progress

10000300 CLK_DDRPHY_REG **DDRPHY RREF Control** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														ddrphy_rref_mux_sel		
Type														RW		
Reset														0	1	0

Bit(s)	Name	Description
2:0	ddrphy_rref_mux_sel	**DDRPHY RREF for MEMPLL** Must be configured before MEMPLL is enabled. 001: 104M (MPLL/1) 010: 52M (MPLL/2) 100: 26M (MPLL/4)

2.2 Top Reset Generator Unit

Module name: TOPRGU Base address: (+10007000h)

Address	Name	Width	Register Function
10007000	TOPRGUWDT_MODE	32	Watchdog Mode Register (Will Not be Reset)
10007004	TOPRGUWDT_LENGTH	32	Watchdog Counter Setting Register
10007008	TOPRGUWDT_RESTART	32	Watchdog Counter Restart Register
1000700C	TOPRGUWDT_STA	32	Watchdog Status Register (Will Not be Reset)
10007010	TOPRGUWDT_INTERVAL	32	Watchdog Reset Pulse Width Register
10007014	TOPRGUWDT_SWRST	32	Software Watchdog Reset Register
10007018	TOPRGUWDT_SWSYSRST	32	System Software Reset Register
10007020	TOPRGUWDT_NONRST_REG	32	Watchdog Non-reset Register (Will Not be Reset)
10007024	TOPRGUWDT_NONRST_REG2	32	Watchdog Non-reset Register (Will Not be Reset)
10007030	TOPRGUWDT_REQ_MODE	32	Reset Request Mode Register (Will Not be Reset)
10007034	TOPRGUWDT_REQ_IRQ_EN	32	Reset Request IRQ Enable Register (Will Not be Reset)
10007038	TOPRGUWDT_EXT_REQ_CON	32	External Reset Request IRQ Enable Register (Will Not be Reset)
10007040	TOPRGUWDT_DRAMC_CTL	32	Debug Control Register (Will Not be Reset)
10007044	TOPRGUWDT_LATCH_CTL	32	Latch Control Register
10007050	TOPRGUWDT_INTERCORE_SYNC	32	Register for Intercore Sync
10007054	TOPRGUWDT_INTERCORE_SYNC_SET	32	Set Control of Register for Intercore Sync
10007058	TOPRGUWDT_INTERCORE_SYNC_CLR	32	Clear Control of Register for Intercore Sync
10007080	TOPRGUWDT_RSTDEG_EN1	32	Reset Deglitch Enable Register 1
10007084	TOPRGUWDT_RSTDEG_EN2	32	Reset Deglitch Enable Register 2
10007500	TOPRGUDEBUG_0_REG	32	Shadow Register of WDT_MODE
10007504	TOPRGUDEBUG_1_REG	32	Shadow Register of WDT_STA
10007508	TOPRGUDEBUG_2_REG	32	Shadow Register of WDT_DEBUG_CTL
1000750C	TOPRGUDEBUG_3_REG	32	Shadow Register of WDT_REQ_MODE
10007510	TOPRGUDEBUG_4_REG	32	Shadow Register of WDT_REG_IRQ_EN

10007000 TOPRGUWDT_MODE Watchdog Mode Register (Will Not be Reset) 2200004D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key															
Type	WO															
Reset	0	0	1	0	0	0	1	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								wdt_cnt_reset_sel	ddr_reserve_mode	dual_mode	irq_lvl_en	wdt_restart_dummy_en	wdt_irq	exten	extpol	wdt_en
Type								RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset								0	0	1	0	0	1	1	0	1

Bit(s)	Name	Description
31:24	unlock_key	**Write 0x22 to unlock the write protection of this register.**
8	wdt_cnt_reset_sel	**Selects reset source of watchdog timer** 0: Reset only by external reset 1: Reset by TOPRGU
7	ddr_reserve_mode	**Enables ddr_reserve_mode mainly** 0: Disable 1: Enable
6	dual_mode	**Enables dual_mode** Turn on watchdog timer and enable the correspondent irq_en and wdt_en if dual_mode is used. 0: Disable 1: Enable
5	irq_lvl_en	**Selects IRQ type** 0: irq_b is pulse (32K) 1: irq_b is level
4	wdt_restart_dummy_en	**Enables extra watchdog timeout counter restart control** 0: Disable 1: Enable
3	wdt_irq	**Enables watchdog timer IRQ** 0: Trigger reset 1: Trigger IRQ
2	exten	**Enables watchdog output reset signal** 0: Disable 1: Enable
1	extpol	**Watchdog output reset signal polarity** 0: Active low 1: Active high
0	wdt_en	**Enables watchdog timer** 0: Disable 1: Enable

10007004 TOPRGUWDT_LENGTH Watchdog Counter Setting Register 0000FFE8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdt_length											unlock_key				

Type	RW											WO				
Reset	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0

Bit(s)	Name	Description
15:5	wdt_length	**Watchdog time-out counter setting** The counter is restarted with {wdt_length [10:0], 1_1111_1111b}; the watchdog timer time-out period is multiple of 512*T32k=15.6ms.
4:0	unlock_key	**Write 0x8 to unlock the write protection of this register.**

10007008 TOPRGUWDT_RESTART Watchdog Counter Restart Register 00001971

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdt_restart															
Type	WO															
Reset	0	0	0	1	1	0	0	1	0	1	1	1	0	0	0	1

Bit(s)	Name	Description
15:0	wdt_restart	Write 0x1971 to reset watchdog timeout counter.

1000700C TOPRGUWDT_STA Watchdog Status Register (Will Not be Reset) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	hw_wdt_rst	sw_wdt_rst	irq_assert	security_rst							ca9_wdt_rst		debug_rst	thermal_rst		
Type	RU	RU	RU	RU							RU		RU	RU		
Reset	0	0	0	0							0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														eint_key_rst	pcmsys_wdt_rst	spmsys_rst
Type														RU	RU	RU
Reset														0	0	0

Bit(s)	Name	Description
31	hw_wdt_rst	**Indicates hardware watchdog generated reset is asserted**
30	sw_wdt_rst	**Indicates software watchdog generated reset is asserted**
29	irq_assert	**Indicates IRQ is asserted instead of reset**
28	security_rst	**Indidates scecurity reset is asserted**
21:20	ca9_wdt_rst	**Indicates ca9 generated reset is asserted (reserved)**
19	debug_rst	**Indicates debug generated reset is asserted**
18	thermal_rst	**Indicates thermal controller reset is asserted** 0: Disable 1: Enable
2	eint_key_rst	**Indidates EINT key generated reset is asserted**
1	pcmsys_wdt_rst	**Indicates PCMSYS timeout generated reset is asserted**
0	spmsys_rst	**Indicates SPMSYS timeout generated reset is asserted**

Bit(s)	Name	Description

10007010 TOPRGUWDT_INTERVAL Watchdog Reset Pulse Width Register 00000FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					wdt_reset_interval											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
11:0	wdt_reset_interval	**Reset pulse width generated by watchdog** 2T 32K for TD modem is required. Unit: 1T=1*32kHz

10007014 TOPRGUWDT_SWRST Software Watchdog Reset Register 00001209

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unlock_key															
Type	WO															
Reset	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0	1

Bit(s)	Name	Description
15:0	unlock_key	Write 0x1209 to generate a software watchdog reset.

10007018 TOPRGUWDT_SWSYSRST System Software Reset Register 88010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key														c2k_wdt_grst_b	c2ksys_grst_b
Type	WO														RW	RW
Reset	1	0	0	0	1	0	0	0							0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	audio_grst_b		mjc_grst_b	conn_mcu_grst_b	pwrap_spictl_grst_b	apmixed_grst_b	conn_grst_b	grst_b_8	md_grst_b	ddrphy_grst_b	img_grst_b	vdec_grst_b	venc_grst_b	mfg_grst_b	mmsys_grst_b	infra_grst_b
Type	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	unlock_key	**Write 0x88 to unlock the write protection of this register.**
17	c2k_wdt_grst_b	**Write 1 to reset the MODEM C2K system.** 2T 32K duration is required for TD modem.
16	c2ksys_grst_b	**Write 0 to release the reset of the MODEM C2K system**
15	audio_grst_b	**Write 1 to reset AUDIOSYS**
13	mjc_grst_b	**Write 1 to reset MJC.**
12	conn_mcu_grst_b	**Write 1 to reset CONNSYS.**
11	pwrap_spictl_grst_b	**Write 1 to reset pwrap_spictl (reserved) AND with mcu_grst_b.**
10	apmixed_grst_b	**Write 1 to reset APMIXEDSYS.**
9	conn_grst_b	**Write 1 to reset CONNSYS.**
8	grst_b_8	**Write 1 to reset INFRA_AO.**
7	md_grst_b	**Write 1 to reset the MODEM system.** 2T 32K duration is required for TD modem.
6	ddrphy_grst_b	**Write 1 to reset DDRPHY and MEMPLL.**
5	img_grst_b	**Write 1 to reset VENC, IMG and its related pad macro (cam, mipi_rx).**
4	vdec_grst_b	**Write 1 to reset VENC.**
3	venc_grst_b	**Write 1 to reset VENC.**
2	mfg_grst_b	**Write 1 to reset MFG.**
1	mmsys_grst_b	**Write 1 to reset MM and its related pad macro (SPI, DPI, MIPI_CFG, MIPI_TX).**
0	infra_grst_b	**Write 1 to reset INFRASYS and its related pad macro (NLI, EFUSE).**

10007020 TOPRGUWDT_NONRST_REG **Watchdog Non-reset Register (Will Not be Reset)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	non_reset_register															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	non_reset_register															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	non_reset_register	**This register will not be reset by WDT; will only be reset by external system reset.** Used for SW to record the status of the pervious boot.

10007024 TOPRGUWDT_NONRST_REG 2 **Watchdog Non-reset Register (Will Not be Reset)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	non_reset_register2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	non_reset_register2															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	non_reset_register2	**This register will not be reset by WDT; will only be reset by external system reset.** Used for SW to record the status of the pervious boot.

10007030 TOPRGUWDT_REQ_MODE **Reset Request Mode Register (Will Not be Reset)** **333C0003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key										ca9_en		debug_en	thermal_ctl_en		
Type	WO										RW		RW	RW		
Reset	0	0	1	1	0	0	1	1			1	1	1	1		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														eint_en	pcmsys_en	spmsys_en
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
31:24	unlock_key	**Write 0x33 to unlock the write protection of this register.**
21:20	ca9_en	**Enables ca9 reset** 0: Disable 1: Enable
19	debug_en	**Enables debugsys reset** 0: Disable 1: Enable
18	thermal_ctl_en	**Enables thermal controller reset** 0: Disable 1: Enable
2	eint_en	**Enable eint reset** 0: Disable 1: Enable
1	pcmsys_en	**Enables pcmsys reset** 0: Disable 1: Enable
0	spmsys_en	**Enables spmsys reset** 0: Disable 1: Enable

10007034 TOPRGUWDT_REQ_IRQ_EN **Reset Request IRQ Enable Register (Will Not be Reset)** **443C0007**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key										ca9_irq		debug_irq	thermal_ctl_irq		
Type	WO										RW		RW	RW		
Reset	0	1	0	0	0	1	0	0			1	1	1	1		

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														eint_irq	pcmsys_irq	spmsys_irq
Type														RW	RW	RW
Reset														1	1	1

Bit(s)	Name	Description
31:24	unlock_key	**Write 0x44 to unlock the write protection of this register.**
21:20	ca9_irq	**Triggers IRQ instead of reset when ca9 reset is enabled** 0: Trigger reset 1: Trigger IRQ
19	debug_irq	**Triggers IRQ instead of reset when debugsys reset is enabled** 0: Trigger reset 1: Trigger IRQ
18	thermal_ctl_irq	**Triggers IRQ instead of reset when thermal controller reset is enabled** 0: Trigger reset 1: Trigger IRQ
2	eint_irq	**Triggers IRQ instead of reset when EINT reset is enabled** 0: Trigger reset 1: Trigger IRQ
1	pcmsys_irq	**Triggers IRQ instead of reset when PCMSYS reset is enabled** 0: Trigger reset 1: Trigger IRQ
0	spmsys_irq	**Triggers IRQ instead of reset when SPMSYS reset is enabled** 0: Trigger reset 1: Trigger IRQ

10007038 TOPRGUWDT_EXT_REQ_CON **External Reset Request IRQ Enable Register (Will Not be Reset)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									eint_sel							eint_dg_en
Type									RW							RW
Reset									0	0	0	0				0

Bit(s)	Name	Description
7:4	eint_sel	**Selects EINT key**
0	eint_dg_en	**Enables EINT signal deglitch** 0: Disable 1: Enable

10007040 TOPRGUWDT_DRAMC_CTL **Debug Control Register (Will Not be Reset)** **590000F1**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key														ddr_sref_sta	ddr_reserve_sta
Type	WO														RU	RO
Reset	0	1	0	1	1	0	0	1							0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		rg_mcu_pwr_iso_dis	rg_mcu_pwr_on_s	rg_mcu_pwr_on		rg_dramc_conf_iso_en_pre	rg_dramc_iso_en_pre	rg_dramc_sref_en_pre	rg_dramc_timeout					rg_mcu_cache_preserve_en	rg_dfd_count_en	rg_ddr_protect_en
Type		RW	RW	RW		RW	RW	RW	RW					RW	RW	RW
Reset		0	0	0		0	0	0	1	1	1	1		0	0	1

Bit(s)	Name	Description
31:24	unlock_key	**Write 0x59 to unlock the write protection of this register.**
17	ddr_sref_sta	**Indicates the current DDR status** 0: Currently not in self-refresh mode 1: Currently in self-refresh mode
16	ddr_reserve_sta	**Indicates ddr_reserve_mode is successful** 0: Fail 1: Succeed
14	rg_mcu_pwr_iso_dis	0: Disable 1: Enable
13	rg_mcu_pwr_on_s	0: Disable 1: Enable
12	rg_mcu_pwr_on	0: Disable 1: Enable
10	rg_dramc_conf_iso_en_pre	**ddr_reserve_mode related write register**
9	rg_dramc_iso_en_pre	**ddr_reserve_mode related write register**
8	rg_dramc_sref_en_pre	**ddr_reserve_mode related write register**
7:4	rg_dramc_timeout	**ddr_reserve_mode related write register**
2	rg_mcu_cache_preserve_en	**MCU cache preserve enable register** 0: Disable 1: Enable
1	rg_dfd_count_en	**Enables counting for prorammable DFD counter** 0: Disable 1: Enable
0	rg_ddr_protect_en	**Enables ddr_protect_mode** When ddr_reserve_mode is enabled, ddr_protect_en will be overidden automatically. For debugging. 0: Disable 1: Enable

10007044 TOPRGUWDT_LATCH_CTL **Latch Control Register** **95000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key												dramc_wt_tes	dramc_wt_tes	dramc_rd_tes	dramc_rd_tes

													t_en 1	t_en 0	t_en 1	t_en 0
Type	WO												RW	RW	RW	RW
Reset	1	0	0	1	0	1	0	1					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_dfd_timeout											dramc_latch_en		rg_spm_latch_en	rg_mcu_latch_en	latch_ctl_en
Type	RW											RW		RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
31:24	unlock_key	**Write 0x95 to unlock the write protection of this register.**
19	dramc_wt_test_en1	**Enables DRAMC ch1 write latch** 0: Disable 1: Enable
18	dramc_wt_test_en0	**Enables DRAMC ch0 write latch** 0: Disable 1: Enable
17	dramc_rd_test_en1	**Enables DRAMC ch1 read latch** 0: Disable 1: Enable
16	dramc_rd_test_en0	**Enables DRAMC ch0 read latch** 0: Disable 1: Enable
15:5	rg_dfd_timeout	**Sets up DFD counting number**
4	dramc_latch_en	**Enables DRAMC latch** 0: Disable 1: Enable
2	rg_spm_latch_en	**Enables SPM latch** 0: Disable 1: Enable
1	rg_mcu_latch_en	**Enables MCU latch** 0: Disable 1: Enable
0	latch_ctl_en	**Triggers MCU latch, SPM latch and DRAMC latch** 0: Disable 1: Enable

10007050 TOPRGUWDT_INTERCORE_SYNC Register for Intercore Sync 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_intercore_sync															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_intercore_sync															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	rg_intercore_sync	Register for using intercore sync

Bit(s)	Name	Description

10007054 TOPRGUWDT_INTERCORE_SYNC_SET **Set Control of Register for Intercore Sync** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_intercore_sync_set															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_intercore_sync_set															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	rg_intercore_sync_set	Set the correspondent bit of rg_intercore_sync to 1'b1.

10007058 TOPRGUWDT_INTERCORE_SYNC_CLR **Clear Control of Register for Intercore Sync** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_intercore_sync_clr															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_intercore_sync_clr															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	rg_intercore_sync_clr	Set the correspondent bit of rg_intercore_sync to 1'b0.

10007080 TOPRGUWDT_RSTDEG_EN1 **Reset Deglitch Enable Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	en															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	en_key															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	en	**Indicates reset deglitch is enabled or not** 0: Disable 1: Enable
15:0	en_key	**Write 0xa357 to enable the reset deglitch function** Both WDT_RSTDEG_EN1 and WDT_RSTDEG_EN2 need to write correct key to enable this function.

Bit(s)	Name	Description

10007084 TOPRGUWDT_RSTDEG_EN2 Reset Deglitch Enable Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	en															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	en_key															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	en	**Indicates reset deglitch is enabled or not** 0: Disable 1: Enable
15:0	en_key	**Write 0x67d2 to enable the reset deglitch function** Both WDT_RSTDEG_EN1 and WDT_RSTDEG_EN2 need to write correct key to enable this function.

10007500 TOPRGUDEBUG_0_REG Shadow Register of WDT_MODE 0000004D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								shadow_wdt_cnt_reset_sel	shadow_ddr_reserve_mode	shadow_dual_mode	shadow_irq_lvl_en	shadow_wdt_restart_dummy_en	shadow_wdt_irq	shadow_exten	shadow_extpol	shadow_wdt_en
Type								RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset								0	0	1	0	0	1	1	0	1

Bit(s)	Name	Description
8	shadow_wdt_cnt_reset_sel	
7	shadow_ddr_reserve_mode	
6	shadow_dual_mode	
5	shadow_irq_lvl_en	0: Disable 1: Enable
4	shadow_wdt_restart_dummy_en	
3	shadow_wdt_irq	
2	shadow_exten	0: Disable 1: Enable
1	shadow_extpol	
0	shadow_wdt_en	0: Disable 1: Enable

10007504 TOPRGUDEBUG_1_REG Shadow Register of WDT_STA 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	shadow_hw_wdt_rst	shadow_sw_wdt_rst	shadow_irq_assert	shadow_security_rst					rsvd		shadow_ca9_wdt_rst		shadow_debug_rst	shadow_thermal_rst		
Type	RU	RU	RU	RU					RO		RU		RU	RU		
Reset	0	0	0	0					0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														shadow_eint_key_rst	shadow_pcmsys_wdt_rst	shadow_spmsys_rst
Type														RU	RU	RU
Reset														0	0	0

Bit(s)	Name	Description
31	shadow_hw_wdt_rst	
30	shadow_sw_wdt_rst	
29	shadow_irq_assert	
28	shadow_security_rst	
23:22	rsvd	
21:20	shadow_ca9_wdt_rst	
19	shadow_debug_rst	
18	shadow_thermal_rst	
2	shadow_eint_key_rst	
1	shadow_pcmsys_wdt_rst	
0	shadow_spmsys_rst	

10007508 TOPRGUDEBUG_2_REG Shadow Register of WDT_DEBUG_CTL 000000F1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															ddr_sref_sta	ddr_reserve_sta
Type															RU	RO
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		rg_mcu_pwr_iso_dis	rg_mcu_pwr_on_s	rg_mcu_pwr_on		rg_dramc_conf_iso_en	rg_dramc_iso_en	rg_dramc_sref_en	rg_dramc_timeout					rg_mcu_cache_preserve_en	rg_dfd_count_en	rg_ddr_protect_en
Type		RO	RO	RO		RO	RO	RO	RO					RO	RO	RO
Reset		0	0	0		0	0	0	1	1	1	1		0	0	1

Bit(s)	Name	Description
17	ddr_sref_sta	**Indicates the current DDR status** 0: Currently not in self-refresh mode 1: Currently in self-refresh mode
16	ddr_reserve_sta	**Indicates ddr_reserve_mode is successful**

Bit(s)	Name	Description
		0: Fail 1: Succeed
14	rg_mcu_pwr_iso_dis	0: Disable 1: Enable
13	rg_mcu_pwr_on_s	0: Disable 1: Enable
12	rg_mcu_pwr_on	0: Disable 1: Enable
10	rg_dramc_conf_iso_en	**ddr_reserve_mode related register (current value)** 0: Disable 1: Enable
9	rg_dramc_iso_en	**ddr_reserve_mode related register (current value)** 0: Disable 1: Enable
8	rg_dramc_sref_en	**ddr_reserve_mode related register (current value)** 0: Disable 1: Enable
7:4	rg_dramc_timeout	**ddr_reserve_mode related register (current value)**
2	rg_mcu_cache_preserve_en	**MCU cache preserve enable register** 0: Disable 1: Enable
1	rg_dfd_count_en	**Enables counting for prorammable DFD counter** 0: Disable 1: Enable
0	rg_ddr_protect_en	**Enables ddr_protect_mode** When ddr_reserve_mode is enabled, ddr_protect_en will be overidden automatically. For debugging. 0: Disable 1: Enable

1000750C TOPRGUDEBUG_3_REG Shadow Register of WDT_REQ_MODE **003C0003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									rsvd		shadow_ca9_en		shadow_debug_en	shadow_thermal_ctl_en		
Type									RO		RO		RO	RO		
Reset									0	0	1	1	1	1		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															shadow_scpsys_en	shadow_thermal_en
Type															RO	RO
Reset															1	1

Bit(s)	Name	Description
23:22	rsvd	
21:20	shadow_ca9_en	0: Disable 1: Enable
19	shadow_debug_en	0: Disable

Bit(s)	Name	Description
		1: Enable
18	shadow_thermal_ctl_en	0: Disable 1: Enable
1	shadow_scpsys_en	0: Disable 1: Enable
0	shadow_thermal_en	0: Disable 1: Enable

10007510 TOPRGUDEBUG_4_REG Shadow Register of WDT_REG_IRQ_EN 003C0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									rsvd		shadow_ca9_irq		shadow_debug_irq	shadow_thermal_ctl_irq		
Type									RO		RO		RO	RO		
Reset									0	0	1	1	1	1		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														shadow_eint_irq	shadow_pcmsys_irq	shadow_spmsys_irq
Type														RO	RO	RO
Reset														1	1	1

Bit(s)	Name	Description
23:22	rsvd	
21:20	shadow_ca9_irq	
19	shadow_debug_irq	0: Trigger reset 1: Trigger IRQ
18	shadow_thermal_ctl_irq	0: Trigger reset 1: Trigger IRQ
2	shadow_eint_irq	**Triggers IRQ instead of reset when EINT reset is enabled** 0: Trigger reset 1: Trigger IRQ
1	shadow_pcmsys_irq	0: Trigger reset 1: Trigger IRQ
0	shadow_spmsys_irq	**Triggers IRQ instead of reset when SPMSYS reset is enabled** 0: Trigger reset 1: Trigger IRQ

2.3 PMIC Wrapper

Module name: PMIC_WRAP Base address: (+1000D000h)

Address	Name	Width	Register Function
1000D000	MUX_SEL	8	SPI MUX Selection
1000D004	WRAP_EN	8	SPI Wrapper Enable
1000D008	DIO_EN	8	Dual I/O Mode Enable of MT63xx
1000D00C	SIDLY	8	Serial Input Delay
1000D010	RDDMY	8	Read Dummy Cycle Number of MT63xx
1000D014	SI_CK_CON	8	SI Enable Delay
1000D018	CSHEXT_WRITE	8	CS High Extension - Write
1000D01C	CSHEXT_READ	8	CS High Extension - Read
1000D020	CSLEXT_START	8	CS Low Extension - Start
1000D024	CSLEXT_END	8	CS Low Extension - End
1000D028	STAUPD_PRD	8	Status Update Contro Register
1000D02C	STAUPD_GRPEN	8	Status Update Group Enable
1000D030	EINT_STA0_ADR	16	Address of External Interrupt status register 0
1000D034	EINT_STA1_ADR	16	Address of External Interrupt status register 1
1000D038	EINT_STA	8	External Interrupt status register
1000D03C	EINT_CLR	8	EINT status Clear
1000D040	STAUPD_MAN_TRIG	8	Status Update Manual Trigger
1000D044	STAUPD_STA	16	Status Update Status
1000D048	WRAP_STA	16	Wrapper Status
1000D04C	HARB_INIT	8	Arbiter Initialization
1000D050	HARB_HPRIO	32	Arbiter Priority Setting
1000D054	HIPRIO_ARB_EN	32	Arbiter Source Enables
1000D058	HARB_STA0	32	High Priority Arbiter Status 0
1000D05C	HARB_STA1	32	High Priority Arbiter Status 1
1000D060	MAN_EN	8	SPI Manual Mode Enable
1000D064	MAN_CMD	16	Manual Command
1000D068	MAN_RDATA	16	Manual Read Data
1000D06C	MAN_VLDCLR	8	Manual Valid Clear
1000D070	WACS0_EN	8	Wrapper Access (#0) Enable
1000D074	INIT_DONE0	8	Initialization Done
1000D078	WACS0_CMD	32	Wrapper Access (#0) Command
1000D07C	WACS0_RDATA	32	Wrapper Access (#0) Read Data
1000D080	WACS0_VLDCLR	8	Wapper Access (#0) Valid Clear
1000D084	WACS1_EN	8	Wapper Access (#1) Enable
1000D088	INIT_DONE1	8	Initialization Done
1000D08C	WACS1_CMD	32	Wapper Access (#1) Command
1000D090	WACS1_RDATA	32	Wapper Access (#1) Read Data

Address	Name	Width	Register Function
1000D094	WACS1_VLDCLR	8	Wapper Access (#1) Valid Clear
1000D098	WACS2_EN	8	Wapper Access (#2) Enable
1000D09C	INIT_DONE2	8	Initialization Done
1000D0A0	WACS2_CMD	32	Wapper Access (#2) Command
1000D0A4	WACS2_RDATA	32	Wapper Access (#2) Read Data
1000D0A8	WACS2_VLDCLR	8	Wapper Access (#2) Valid Clear
1000D0AC	WACS3_EN	8	Wapper Access (#3) Enable
1000D0B0	INIT_DONE3	8	Initialization Done
1000D0B4	WACS3_CMD	32	Wapper Access (#3) Command
1000D0B8	WACS3_RDATA	32	Wapper Access (#3) Read Data
1000D0BC	WACS3_VLDCLR	8	Wapper Access (#3) Valid Clear
1000D0C0	INT0_EN	32	Interrupt Enable
1000D0C4	INT0_FLG_RAW	32	Interrupt Flags - Raw
1000D0C8	INT0_FLG	32	Interrupt Flags
1000D0CC	INT0_CLR	32	Interrupt Clear
1000D0D0	INT1_EN	32	Interrupt Enable
1000D0D4	INT1_FLG_RAW	32	Interrupt Flags - Raw
1000D0D8	INT1_FLG	32	Interrupt Flags
1000D0DC	INT1_CLR	32	Interrupt Clear
1000D0E0	SIG_ADR	32	Signature Address in MT63xx
1000D0E4	SIG_MODE	8	Signature Checking Mode in MT63xx
1000D0E8	SIG_VALUE	32	Signature Value in MT63xx
1000D0EC	SIG_ERRVAL	32	Error Signature Value in MT63xx
1000D0F0	CRC_EN	8	CRC enable
1000D0F4	TIMER_EN	16	Timer Enable
1000D0F8	TIMER_STA	32	Timer Status
1000D0FC	WDT_UNIT	8	Watch Dog Timer Unit
1000D100	WDT_SRC_EN	32	Watch Dog Timer Source Enable
1000D104	WDT_FLG	32	Watch Dog Flag
1000D108	DEBUG_INT_SEL	8	Debug Interrupt Selection
1000D10C	DVFS_ADR0	16	DVFS Command #0 - Address
1000D110	DVFS_WDATA0	16	DVFS Command #0 - Write Data
1000D114	DVFS_ADR1	16	DVFS Command #1 - Address
1000D118	DVFS_WDATA1	16	DVFS Command #1 - Write Data
1000D11C	DVFS_ADR2	16	DVFS Command #2 - Address
1000D120	DVFS_WDATA2	16	DVFS Command #2 - Write Data
1000D124	DVFS_ADR3	16	DVFS Command #3 - Address
1000D128	DVFS_WDATA3	16	DVFS Command #3 - Write Data
1000D12C	DVFS_ADR4	16	DVFS Command #4 - Address

Address	Name	Width	Register Function
1000D130	DVFS_WDATA4	16	DVFS Command #4 - Write Data
1000D134	DVFS_ADR5	16	DVFS Command #5 - Address
1000D138	DVFS_WDATA5	16	DVFS Command #5 - Write Data
1000D13C	DVFS_ADR6	16	DVFS Command #6 - Address
1000D140	DVFS_WDATA6	16	DVFS Command #6 - Write Data
1000D144	DVFS_ADR7	16	DVFS Command #7 - Address
1000D148	DVFS_WDATA7	16	DVFS Command #7 - Write Data
1000D14C	DVFS_ADR8	16	DVFS Command #8 - Address
1000D150	DVFS_WDATA8	16	DVFS Command #8 - Write Data
1000D154	DVFS_ADR9	16	DVFS Command #9 - Address
1000D158	DVFS_WDATA9	16	DVFS Command #9 - Write Data
1000D15C	DVFS_ADR10	16	DVFS Command #10 - Address
1000D160	DVFS_WDATA10	16	DVFS Command #10 - Write Data
1000D164	DVFS_ADR11	16	DVFS Command #11 - Address
1000D168	DVFS_WDATA11	16	DVFS Command #11 - Write Data
1000D16C	DVFS_ADR12	16	DVFS Command #12 - Address
1000D170	DVFS_WDATA12	16	DVFS Command #12 - Write Data
1000D174	DVFS_ADR13	16	DVFS Command #13 - Address
1000D178	DVFS_WDATA13	16	DVFS Command #13 - Write Data
1000D17C	DVFS_ADR14	16	DVFS Command #14 - Address
1000D180	DVFS_WDATA14	16	DVFS Command #14 - Write Data
1000D184	DVFS_ADR15	16	DVFS Command #15 - Address
1000D188	DVFS_WDATA15	16	DVFS Command #15 - Write Data
1000D18C	DCXO_ENABLE	8	DCXO_ENABLE
1000D190	DCXO_CONN_ADR0	16	DCXO_CONN Command #0 - Address
1000D194	DCXO_CONN_WDATA0	16	DCXO_CONN Command #0 - Write Data
1000D198	DCXO_CONN_ADR1	16	DCXO_CONN Command #1 - Address
1000D19C	DCXO_CONN_WDATA1	16	DCXO_CONN Command #1- Write Data
1000D1A0	DCXO_NFC_ADR0	16	DCXO_NFC Command #0 - Address
1000D1A4	DCXO_NFC_WDATA0	16	DCXO_NFC Command #0 - Write Data
1000D1A8	DCXO_NFC_ADR1	16	DCXO_NFC Command #1 - Address
1000D1AC	DCXO_NFC_WDATA1	16	DCXO_NFC Command #1- Write Data
1000D1B0	SPMINF_STA	16	SPM interface status register

Address	Name	Width	Register Function
1000D1B4	CIPHER_KEY_SEL	8	CIPHER Key Selection
1000D1B8	CIPHER_IV_SEL	8	CIPHER Initial Vector Selection
1000D1BC	CIPHER_EN	8	CIPHER Engine Enable
1000D1C0	CIPHER_RDY	8	CIPHER Data Ready
1000D1C4	CIPHER_MODE	8	CIPHER Mode Enable
1000D1C8	CIPHER_SWRST	8	CIPHER Soft Reset
1000D1CC	DCM_EN	16	Internal DCM Enable
1000D1D0	DCM_SPI_DBC_PRD	8	Debounce Period at Entering DCM Mode for SPI_CK
1000D1D4	DCM_DBC_PRD	8	Debounce Period at Entering DCM Mode for SYS_CK
1000D1D8	EXT_CK	8	Extra Clock number
1000D1DC	ADC_CMD_ADDR	16	AuxADC command register address
1000D1E0	PWRAP_ADC_CMD	16	Command to AuxADC
1000D1E4	ADC_RDATA_ADDR	16	Address of thermal data [15:0] register in AuxADC
1000D1E8	GPS_STA	32	GPS Interface Status (Debug)
1000D1EC	SWRST	8	Software reset
1000D1F0	HARB_SLEEP_GATED_CTRL	8	Enable the sleep gated harb function
1000D1F4	MD_ADC_RDATA_ADDR_LATEST	16	Address of the latest thermal data [15:0] register in AuxADC
1000D1F8	MD_ADC_RDATA_ADDR_WP	16	Address of the latest bufter thermal data pointer
1000D1FC	MD_ADC_RDATA_ADDR0	16	Address of the buffer thermal data0
1000D200	MD_ADC_RDATA_ADDR1	16	Address of the buffer thermal data1
1000D204	MD_ADC_RDATA_ADDR2	16	Address of the buffer thermal data2
1000D208	MD_ADC_RDATA_ADDR3	16	Address of the buffer thermal data3
1000D20C	MD_ADC_RDATA_ADDR4	16	Address of the buffer thermal data4
1000D210	MD_ADC_RDATA_ADDR5	16	Address of the buffer thermal data5
1000D214	MD_ADC_RDATA_ADDR6	16	Address of the buffer thermal data6
1000D218	MD_ADC_RDATA_ADDR7	16	Address of the buffer thermal data7
1000D21C	MD_ADC_RDATA_ADDR8	16	Address of the buffer thermal data8
1000D220	MD_ADC_RDATA_ADDR9	16	Address of the buffer thermal data9
1000D224	MD_ADC_RDATA_ADDR10	16	Address of the buffer thermal data10
1000D228	MD_ADC_RDATA_ADDR11	16	Address of the buffer thermal data11

Address	Name	Width	Register Function
1000D22C	MD_ADC_RDATA_ADDR12	16	Address of the buffer thermal data12
1000D230	MD_ADC_RDATA_ADDR13	16	Address of the buffer thermal data13
1000D234	MD_ADC_RDATA_ADDR14	16	Address of the buffer thermal data14
1000D238	MD_ADC_RDATA_ADDR15	16	Address of the buffer thermal data15
1000D23C	MD_ADC_RDATA_ADDR16	16	Address of the buffer thermal data16
1000D240	MD_ADC_RDATA_ADDR17	16	Address of the buffer thermal data17
1000D244	MD_ADC_RDATA_ADDR18	16	Address of the buffer thermal data18
1000D248	MD_ADC_RDATA_ADDR19	16	Address of the buffer thermal data19
1000D24C	MD_ADC_RDATA_ADDR20	16	Address of the buffer thermal data20
1000D250	MD_ADC_RDATA_ADDR21	16	Address of the buffer thermal data21
1000D254	MD_ADC_RDATA_ADDR22	16	Address of the buffer thermal data22
1000D258	MD_ADC_RDATA_ADDR23	16	Address of the buffer thermal data23
1000D25C	MD_ADC_RDATA_ADDR24	16	Address of the buffer thermal data24
1000D260	MD_ADC_RDATA_ADDR25	16	Address of the buffer thermal data25
1000D264	MD_ADC_RDATA_ADDR26	16	Address of the buffer thermal data26
1000D268	MD_ADC_RDATA_ADDR27	16	Address of the buffer thermal data27
1000D26C	MD_ADC_RDATA_ADDR28	16	Address of the buffer thermal data28
1000D270	MD_ADC_RDATA_ADDR29	16	Address of the buffer thermal data29
1000D274	MD_ADC_RDATA_ADDR30	16	Address of the buffer thermal data30
1000D278	MD_ADC_RDATA_ADDR31	16	Address of the buffer thermal data31
1000D27C	MD_ADC_MODE_SEL	8	MD_AUXADC_MODE_LATCH_SEL
1000D280	MD_ADC_STA0	32	MD_AUXADC Interface Status0 (Debug)
1000D284	MD_ADC_STA1	32	MD_AUXADC Interface Status1 (Debug)
1000D288	PRIORITY_USER_SEL_0	32	ARBITER_PRIORITY_USER_SEL_0
1000D28C	PRIORITY_USER_SEL_1	32	ARBITER_PRIORITY_USER_SEL_1
1000D290	ARBITER_OUT_SEL_0	32	ARBITER_OUT_SEL_0
1000D294	ARBITER_OUT_SEL_1	32	ARBITER_OUT_SEL_1
1000D298	STARV_COUNTER_0	16	STARV_COUNTER_0
1000D29C	STARV_COUNT	16	STARV_COUNTER_1

Address	Name	Width	Register Function
	ER_1		
1000D2A0	STARV_COUNTER_2	16	STARV_COUNTER_2
1000D2A4	STARV_COUNTER_3	16	STARV_COUNTER_3
1000D2A8	STARV_COUNTER_4	16	STARV_COUNTER_4
1000D2AC	STARV_COUNTER_5	16	STARV_COUNTER_5
1000D2B0	STARV_COUNTER_6	16	STARV_COUNTER_6
1000D2B4	STARV_COUNTER_7	16	STARV_COUNTER_7
1000D2B8	STARV_COUNTER_8	16	STARV_COUNTER_8
1000D2BC	STARV_COUNTER_9	16	STARV_COUNTER_9
1000D2C0	STARV_COUNTER_10	16	STARV_COUNTER_10
1000D2C4	STARV_COUNTER_11	16	STARV_COUNTER_11
1000D2C8	STARV_COUNTER_12	16	STARV_COUNTER_12
1000D2CC	STARV_COUNTER_13	16	STARV_COUNTER_13
1000D2D0	STARV_COUNTER_14	16	STARV_COUNTER_14
1000D2D4	STARV_COUNTER_15	16	STARV_COUNTER_15
1000D2D8	STARV_COUNTER_0_STATUS	32	STARV_COUNTER_0_STATUS
1000D2DC	STARV_COUNTER_1_STATUS	32	STARV_COUNTER_1_STATUS
1000D2E0	STARV_COUNTER_2_STATUS	32	STARV_COUNTER_2_STATUS
1000D2E4	STARV_COUNTER_3_STATUS	32	STARV_COUNTER_3_STATUS
1000D2E8	STARV_COUNTER_4_STATUS	32	STARV_COUNTER_4_STATUS
1000D2EC	STARV_COUNTER_5_STATUS	32	STARV_COUNTER_5_STATUS
1000D2F0	STARV_COUNTER_6_STATUS	32	STARV_COUNTER_6_STATUS
1000D2F4	STARV_COUNTER_7_STATUS	32	STARV_COUNTER_7_STATUS
1000D2F8	STARV_COUNTER_8_STATUS	32	STARV_COUNTER_8_STATUS
1000D2FC	STARV_COUNTER_9_STATUS	32	STARV_COUNTER_9_STATUS
1000D300	STARV_COUNTER_10_STATUS	32	STARV_COUNTER_10_STATUS
1000D304	STARV_COUNTER_11_STATUS	32	STARV_COUNTER_11_STATUS
1000D308	STARV_COUNTER_12_STATUS	32	STARV_COUNTER_12_STATUS

Address	Name	Width	Register Function
1000D30C	STARV_COUNTER_13_STATUS	32	STARV_COUNTER_13_STATUS
1000D310	STARV_COUNTER_14_STATUS	32	STARV_COUNTER_14_STATUS
1000D314	STARV_COUNTER_15_STATUS	32	STARV_COUNTER_15_STATUS
1000D318	STARV_COUNTER_CLR	16	STARV_COUNTER_CLR
1000D31C	STARV_PRIO_STATUS	16	STARV_PRIO_STATUS
1000D320	DEBUG_STATUS	8	DEBUG_STATUS
1000D324	DEBUG_SQUENCE_0	32	DEBUG_SQUENCE_0
1000D328	DEBUG_SQUENCE_1	32	DEBUG_SQUENCE_1
1000D32C	DEBUG_SQUENCE_2	32	DEBUG_SQUENCE_2
1000D330	DEBUG_SQUENCE_3	32	DEBUG_SQUENCE_3
1000D334	DEBUG_SQUENCE_4	32	DEBUG_SQUENCE_4
1000D338	DEBUG_SQUENCE_5	32	DEBUG_SQUENCE_5
1000D33C	DEBUG_SQUENCE_6	32	DEBUG_SQUENCE_6

1000D000 MUX_SEL SPI MUX Selection 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MUX_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	MUX_SEL	**Select SPI controller source** 0: SPI is controlled by automatic wrapper 1: SPI is controlled in manual mode.

1000D004 WRAP_EN SPI Wrapper Enable 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WRAP_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	WRAP_EN	**Automatic wrapper circuit enabling switch.** 0: Wrapper circuit is disabled, but the current transaction will be finished. 1: Wrapper circuit is enabled, and new request can be accepted once wrapper

Bit(s)	Name	Description
		is available

1000D008 DIO_EN Dual I/O Mode Enable of MT63xx 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															DIO_EN1	DIO_EN0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	DIO_EN1	**SPI dual I/O mode feature enabling switch for PMIC1.** 0: Disable SPI dual I/O mode 1: Enable SPI dual I/O mode
0	DIO_EN0	**SPI dual I/O mode feature enabling switch for PMIC0.** 0: Disable SPI dual I/O mode 1: Enable SPI dual I/O mode

1000D00C SIDLY Serial Input Delay 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SIDLY	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	SIDLY	**Control SPI input data strobe timing.** The default setting (0ns) corresponds to strobing at rising edge of SPI CLK. 0: Delay 0ns 1: Delay 2ns 2: Delay 4ns 3: Delay 6ns

1000D010 RDDMY Read Dummy Cycle Number of MT63xx FF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RDDMY1				RDDMY0			
Type									RW				RW			
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:4	RDDMY1	**Applies (1+RDDMY1[3:0])T of dummy read cycles before read data phase** This setting should be in accordance with the one in slave. The max dummy cycle is 16T.
3:0	RDDMY0	**Applies (1+RDDMY0[3:0])T of dummy read cycles before read data phase.** This setting should be in accordance with the one in slave. The max dummy cycle is 16T.

1000D014 SI_CK_CON SI Enable Delay 01

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														SI_EN_SEL		SI_CK_SEL
Type														RW		RW
Reset														0	0	1

Bit(s)	Name	Description
2:1	SI_EN_SEL	**Control SI enabling timing.** T is the period of SPI CLK. 0: Delay 0T 1: Delay 1T 2: Delay 2T 3: Dealy 3T
0	SI_CK_SEL	0: Choose inverted SPI CLK 1: Choose SPI CLK

1000D018 CSHEXT_WRITE CS High Extension - Write 0F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CSHEXT_WRITE							
Type									RW							
Reset									0	0	0	0	1	1	1	1

Bit(s)	Name	Description
7:0	CSHEXT_WRITE	**After finishing a write transaction, extends CS high time to be at least (1+CSHEXT_WRITE[3:0])T of SPI CLK.** Applies to the CS high time between ADR and DATA of a write transaction.

1000D01C CSHEXT_READ CS High Extension - Read 0F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CSHEXT_READ							
Type									RW							
Reset									0	0	0	0	1	1	1	1

Bit(s)	Name	Description
7:0	CSHEXT_READ	**After finishing a read transaction, extends CS high time to be at least (1+CSHEXT_READ[3:0])T of SPI CLK.** Applies to the CS high time between ADR and DATA of a read transaction.

1000D020 CSLEXT_START CS Low Extension - Start 0F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CSLEXT_START			
Type													RW			
Reset													1	1	1	1

Bit(s)	Name	Description
3:0	CSLEXT_START	Extends CS low time after CSL command to be at least (1.5+CSLEXT_START[3:0])T of SPI CLK

1000D024 CSLEXT_END CS Low Extension - End 0F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CSLEXT_END			
Type													RW			
Reset													1	1	1	1

Bit(s)	Name	Description
3:0	CSLEXT_END	Extends CS low time before CSH command to be at least (1.5+CSLEXT_END[3:0])T of SPI CLK

1000D028 STAUPD_PRD Status Update Contro Register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													STAUPD_PRD			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	STAUPD_PRD	**Selects periodic status update timing (period).** This status will be updated every selected time period. Unit: 19.7us 0: Disable 1: 19.7us 2: 39.4us 5: 98.5us 15: 295.5us

1000D02C STAUPD_GRPEN Status Update Group Enable 0C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									STAUPD_GRPEN							
Type									RW							
Reset									0	0	0	0	1	1	0	0

Bit(s)	Name	Description
7:0	STAUPD_GRPEN	**Enables switch for each status update group.** [0]: Signature from MT6328 [1]: Signature from MT63xx [2]: Interrupt Status from MT6328 [3]: Interrupt Status from MT63xx

Bit(s)	Name	Description
		[4]: read data from MT6328 for MD [5]: read data from MT6328 for GPS

1000D030 EINT_STA0_ADR Address of External Interrupt status register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_STA0_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	EINT_STA0_ADR	Specifies addtess of interrupt statis in MT6328

1000D034 EINT_STA1_ADR Address of External Interrupt status register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_STA1_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	EINT_STA1_ADR	Specifies addtess of interrupt statis in MT63xx

1000D038 EINT_STA External Interrupt status register 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													EINT_STA			
Type													RO			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	EINT_STA	**Records external interrupt status** [0]: CPU IRQ status in MT6328 [1]: MD32 IRQ status in MT6328 [2]: CPU IRQ status in MT63xx [3]: RESERVED

1000D03C EINT_CLR EINT status Clear 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													EINT_CLR			
Type													WO			
Reset													0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
3:0	EINT_CLR	**Write 1 to corresponding bit to clear EINT status flag.** Ex: Write 4'b0100 will clear bit 2 (CPU IRQ status in MT63xx)

1000D040 STAUPD_MAN_TRIG Status Update Manual Trigger 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STAUPD_MAN_TRIG
Type																WO
Reset																0

Bit(s)	Name	Description
0	STAUPD_MAN_TRIG	Set to 1 to manually trigger the status update circuit.

1000D044 STAUPD_STA Status Update Status 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								STAUPD_FSM			STAUPD_ALE_CNT			STAUPD_DLE_CNT		
Type								RU			RU			RU		
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:6	STAUPD_FSM	**Current STAUPD FSM state** 0: IDLE 2: REQ 4: WFDLE
5:3	STAUPD_ALE_CNT	**Request count every time STAUPD is triggered.** For every period of STAUPD_PRD, 4 status update request will be triggered.
2:0	STAUPD_DLE_CNT	**Read data count every time STAUPD is triggered.** For every period of STAUPD_PRD, 4 status will be received after requests have been sent.

1000D048 WRAP_STA Wrapper Status 0280

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		WRAP_FSM				AG_WRAP_REQ	AG_WRAP_W	WRAP_CH_REQ	WRAP_CH_W	WRAP_AG_DLE_RESTCNT		WRAP_CH_ALE_RESTCNT		WRAP_CH_DLE_RESTCNT		
Type		RU				RU	RU	RU	RU	RU		RU		RU		
Reset		0	0	0	0	0	1	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:11	WRAP_FSM	**Current wrapper FSM states** 0x0: IDLE

Bit(s)	Name	Description
		0x2: CSL_ADR_START 0x4: ADR 0x6: CSL_ADR_END 0x8: CSH_ADR 0xA: CSL_DATA_START 0xC: DATA 0xE: CSL_DATA_END 0xF: CSH_DATA Others: Reserved
10	AG_WRAP_REQ	**Current WRAP request indicator**
9	AG_WRAP_W	**Current WRAP read/write direction**
8	WRAP_CH_REQ	**Current SPI request indicator**
7	WRAP_CH_W	**Current SPI read/write direction** 0: Read 1: Write
6:5	WRAP_AG_DLE_RESTCNT	**Remaining WRAP request counter for wrapper**
4:3	WRAP_CH_ALE_RESTCNT	**Remaining SPI request counter for wrapper**
2:0	WRAP_CH_DLE_RESTCNT	**Remaining SPI read data counter for wrapper**

1000D04C HARB_INIT Arbiter Initialization 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HARB_INIT
Type																RW
Reset																0

Bit(s)	Name	Description
0	HARB_INIT	**Clears high-priority arbiter internal registers to initial value.** 0: Normal state. 1: Set up arbiter in initialized state.

1000D050 HARB_HPRIO Arbiter Priority Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			HARB_HPRIO													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	HARB_HPRIO	**Sets high priority to the corresponding request.** The pre-defined priority is 0 > 1 > 2 ...etc; ie. request from agent 0 has the highest priority. However, by setting up the corresponding bit of HARB_HPRIO[5:0] to 1, the priority can be raised higher. Request whose

Bit(s)	Name	Description
		corresponding HARB_HPRIO bit is 1 has higher priority than other requests whose corresponding HARB_HPRIO is 0. For requests whose HARB_HPRIO bits are set to 1, their priorities still follow the order: 0 > 1 > 2 > ... etc [13]: WACSP2P (SCP SW) [12]: WACS1 (MD SW1) [11]: WACS2 (AP SW) [10]: GPSINF [9]: STAUPD [8]: MD_ADCINF [7]: DCXO_NFCINF [6]: DCXO_CONNINF [5]: WACS3(C2K SW) [4]: DVFSINF (SPMINF) [3]: WACS0 (MD SW0) [2]: MD_DVFSINF [1]: C2kINF [0]: MDINF

1000D054 HIPRIO_ARB_EN Arbiter Source Enables 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			HIPRIO_ARB_EN													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	HIPRIO_ARB_EN	[13]: WACSP2P (SCP SW) [12]: WACS1 (MD SW1) [11]: WACS2 (AP SW) [10]: GPSINF [9]: STAUPD [8]: MD_ADCINF [7]: DCXO_NFCINF [6]: DCXO_CONNINF [5]: WACS3(C2K SW) [4]: DVFSINF (SPMINF) [3]: WACS0 (MD SW0) [2]: MD_DVFSINF [1]: C2kINF [0]: MDINF 0: Disable 1: Enable

1000D058 HARB_STA0 High Priority Arbiter Status 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HARB_WRAP_REQ	HARB_WRAP_ADR														
Type	RU	RU														

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HARB_WRAP_WDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	HARB_WRAP_REQ	
30:16	HARB_WRAP_ADR	
15:0	HARB_WRAP_WDATA	

1000D05C HARB_STA1 High Priority Arbiter Status 1 20000005

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		HARB_WRAP_REQo	HARB_WRAP_W	AG_HARB_REQ[13:1]												
Type		RU	RU	RU												
Reset		0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AG_HARB_REQ[0:0]	HARB_DLE_RESTCNT				HARB_OWN				HARB_DLE_OWN				HARB_VLD	HARB_DLE_FULL	HARB_DLE_EMPTY
Type	RU	RU				RU				RU				RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit(s)	Name	Description
30	HARB_WRAP_REQo	
29	HARB_WRAP_W	0: Read 1: Write
28:15	AG_HARB_REQ	
14:11	HARB_DLE_RESTCNT	
10:7	HARB_OWN	
6:3	HARB_DLE_OWN	
2	HARB_VLD	
1	HARB_DLE_FULL	
0	HARB_DLE_EMPTY	

1000D060 MAN_EN SPI Manual Mode Enable 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MAN_EN
Type																RW
Reset																0

Bit(s)	Name	Description

Bit(s)	Name	Description
0	MAN_EN	**Manual mode circuit enabling switch.** 0: Disable Mannual mode circuit 1: Enable Mannual mode circuit

1000D064 MAN_CMD Manual Command 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			SPI_W	SPI_OP					SPI_WDATA							
Type			RW	RW					RW							
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13	SPI_W	**SPI command: Read/write direction** 0: Read 1: Write
12:8	SPI_OP	**SPI command: Operation code** 0x0: OP_CSH 0x1: OP_CSL 0x8: OP_OUTS 0x9: OP_OUTD 0xC: OP_INS 0xD: OP_IND
7:0	SPI_WDATA	**SPI command: Write data**

1000D068 MAN_RDATA Manual Read Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					MAN_REQ	MAN_FSM			MAN_RDATA							
Type					RU	RU			RU							
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	MAN_REQ	**Manual request indicator** 0: No MAN request is awaiting grant. 1: One MAN Request is still awaiting grant.
10:8	MAN_FSM	**Current MAN FSM states** 0x0: IDLE 0x2: REQ. Request in process 0x4: WFDLE. Wait for read data 0x6: WFVLDCLR. Wait for valid flag clearing Others: Reserved
7:0	MAN_RDATA	**Received read data in buffer.** SW must check if MAN_FSM equals to WFVLDCLR before reads MAN_RDATA.

1000D06C MAN_VLDCLR Manual Valid Clear 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name																MAN_VLDCLR
Type																WO
Reset																0

Bit(s)	Name	Description
0	MAN_VLDCLR	**Write 1 to clear valid flag.** 0: Disable 1: Enable

1000D070 WACS0_EN Wrapper Access (#0) Enable 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WACS0_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	WACS0_EN	**Enables wrapper access.** Set to disable will reset the FSM. 0: Disable 1: Enable

1000D074 INIT_DONE0 Initialization Done 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INIT_DONE0
Type																RW
Reset																0

Bit(s)	Name	Description
0	INIT_DONE0	**Indicates initialization is finished** During SPI transactions, if this bit is detected low, then current transaction may fail, which requires re-do or debugging. 0: Initialization is not yet finished. 1: Initialization is finished.

1000D078 WACS0_CMD Wrapper Access (#0) Command 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WACS0_WRITE	WACS0_ADR														
Type	RW	RW														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WACS0_WDATA															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	WACS0_WRITE	**Wrapper access: Read/write direction** 0: Read 1: Write
30:16	WACS0_ADR	**Wrapper access: Address[15:1]**
15:0	WACS0_WDATA	**Wrapper access: Write data[15:0]**

1000D07C WACS0_RDATA Wrapper Access (#0) Read Data 80500000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WACS0_FIFO_FREECNT				WACS0_FIFO_FILLCNT					SYS_IDLE0	INIT_DONE0	SYNC_IDLE0	WACS0_REQ	WACS0_FSM		
Type	RU				RU					RU	RU	RU	RU	RU		
Reset	1	0	0	0	0	0	0	0		1	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WACS0_RDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	WACS0_FIFO_FREECNT	**Records the number of data can be filled into FIFO**
27:24	WACS0_FIFO_FILLCNT	**Records the number of data filled into FIFO**
22	SYS_IDLE0	**PMIC_WRAP busy status indicator:** 1. WACS 0/1/2 idle 2. no arbitor request 3, no spi_wrap to mux request 4. no waiting read data 5. spi_man is idle 6. spI_sync is idle 0: PMIC_WRAP is busy 1: PMIC_WRAP is IDLE
21	INIT_DONE0	**Indicates initialization is finished.** During SPI transactions, if this bit is detected low, then current transaction may fail, which requires re-do or debugging. (This is equivalent to INIT_DONE) 0: Initialization is not yet finished 1: Initialization is finished.
20	SYNC_IDLE0	**SYNC module busy status.** It is used to judge if the request has reached SYNC module. 0: SYNC module is busy 1: SYNC module is IDLE
19	WACS0_REQ	**Wrapper access request indicator.** 0: No WACS request is awaiting grant. 1: One WACS Request is still awaiting grant.
18:16	WACS0_FSM	**Current WACS FSM states.** 0x0: IDLE 0x2: REQ. Request in process 0x4: WFDLE. Wait for read data

Bit(s)	Name	Description
		0x6: WFVLDCLR. Wait for valid flag clearing Others: Reserved
15:0	WACS0_RDATA	**Wrapper Access: read data.** SW must check if valid flag equals to 1 before using this read data.

1000D080 WACS0_VLDCLR Wapper Access (#0) Valid Clear 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WACS0_VLDCLR
Type																WO
Reset																0

Bit(s)	Name	Description
0	WACS0_VLDCLR	Write 1 to clear valid flag.

1000D084 WACS1_EN Wapper Access (#1) Enable 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WACS1_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	WACS1_EN	**Enables wrapper access** Set to disable will reset the FSM. 0: Disable 1: Enable

1000D088 INIT_DONE1 Initialization Done 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INIT_DONE1
Type																RW
Reset																0

Bit(s)	Name	Description
0	INIT_DONE1	**Indicates initialization is finished.** During SPI transactions, if this bit is detected low, then current transaction may fail, which requires re-do or debugging. 0: Initialization is not yet finished. 1: Initialization is finished.

1000D08C WACS1_CMD Wapper Access (#1) Command 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WACS1_WRITE	WACS1_ADR														
Type	RW	RW														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WACS1_WDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	WACS1_WRITE	**Wrapper access: Read/write direction** 0: Read 1: Write
30:16	WACS1_ADR	**Wrapper access: Address[15:1]**
15:0	WACS1_WDATA	**Wrapper access: Write data[15:0]**

1000D090 WACS1_RDATA Wapper Access (#1) Read Data 80500000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WACS1_FIFO_FREECNT				WACS1_FIFO_FILLCNT					SYS_IDLE1	INIT_DONE1	SYNC_IDLE1	WACS1_REQ	WACS1_FSM		
Type	RU				RU					RU	RU	RU	RU	RU		
Reset	1	0	0	0	0	0	0	0		1	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WACS1_RDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	WACS1_FIFO_FREECNT	**Records the number of data can be filled into FIFO**
27:24	WACS1_FIFO_FILLCNT	**Records the number of data filled into FIFO**
22	SYS_IDLE1	**PMIC_WRAP busy status indicator:** 1. WACS 0/1/2 idle 2. no arbitor request 3, no spi_wrap to mux request 4. no waiting read data 5. spi_man is idle 6. spI_sync is idle 0: PMIC_WRAP is busy 1: PMIC_WRAP is IDLE
21	INIT_DONE1	**Indicates initialization is finished.** During SPI transactions, if this bit is detected low, then current transaction may fail, which requires re-do or debugging. (This is equivalent to INIT_DONE) 0: Initialization is not yet finished 1: Initialization is finished.
20	SYNC_IDLE1	**SYNC module busy status.**

Bit(s)	Name	Description
		It is used to judge if the request has reached SYNC module. 0: SYNC module is busy 1: SYNC module is IDLE
19	WACS1_REQ	**Wrapper access request indicator.** 0: No WACS request is awaiting grant. 1: One WACS Request is still awaiting grant.
18:16	WACS1_FSM	**Current WACS FSM states.** 0x0: IDLE 0x2: REQ. Request in process 0x4: WFDLE. Wait for read data 0x6: WFVLDCLR. Wait for valid flag clearing Others: Reserved
15:0	WACS1_RDATA	**Wrapper Access: read data.** SW must check if valid flag equals to 1 before using this read data.

1000D094 WACS1_VLDCLR Wapper Access (#1) Valid Clear 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WACS1_VLDCLR
Type																WO
Reset																0

Bit(s)	Name	Description
0	WACS1_VLDCLR	Write 1 to clear valid flag.

1000D098 WACS2_EN Wapper Access (#2) Enable 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WACS2_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	WACS2_EN	**Enables wrapper access** Set to disable will reset the FSM. 0: Disable 1: Enable

1000D09C INIT_DONE2 Initialization Done 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INIT_DONE2
Type																RW

Reset																0

Bit(s)	Name	Description
0	INIT_DONE2	**Indicates initialization is finished.** During SPI transactions, if this bit is detected low, then current transaction may fail, which requires re-do or debugging. 0: Initialization is not yet finished. 1: Initialization is finished.

1000D0A0 WACS2_CMD Wapper Access (#2) Command 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WACS2_WRITE	WACS2_ADR														
Type	RW	RW														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WACS2_WDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	WACS2_WRITE	**Wrapper access: Read/write direction** 0: Read 1: Write
30:16	WACS2_ADR	**Wrapper access: Address[15:1]**
15:0	WACS2_WDATA	**Wrapper access: Write data[15:0]**

1000D0A4 WACS2_RDATA Wapper Access (#2) Read Data 80500000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WACS2_FIFO_FREECNT				WACS2_FIFO_FILLCNT					SYS_IDLE2	INIT_DONE2	SYNC_IDLE2	WACS2_REQ	WACS2_FSM		
Type	RU				RU					RU	RU	RU	RU	RU		
Reset	1	0	0	0	0	0	0	0		1	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WACS2_RDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	WACS2_FIFO_FREECNT	**Records the number of data can be filled into FIFO**
27:24	WACS2_FIFO_FILLCNT	**Records the number of data filled into FIFO**
22	SYS_IDLE2	**PMIC_WRAP busy status indicator:** 1. WACS 0/1/2 idle 2. no arbitor request 3, no spi_wrap to mux request 4. no waiting read data

Bit(s)	Name	Description
		5. spi_man is idle 6. spI_sync is idle 0: PMIC_WRAP is busy 1: PMIC_WRAP is IDLE
21	INIT_DONE2	**Indicates initialization is finished.** During SPI transactions, if this bit is detected low, then current transaction may fail, which requires re-do or debugging. (This is equivalent to INIT_DONE) 0: Initialization is not yet finished 1: Initialization is finished.
20	SYNC_IDLE2	**SYNC module busy status.** It is used to judge if the request has reached SYNC module. 0: SYNC module is busy 1: SYNC module is IDLE
19	WACS2_REQ	**Wrapper access request indicator.** 0: No WACS request is awaiting grant. 1: One WACS Request is still awaiting grant.
18:16	WACS2_FSM	**Current WACS FSM states.** 0x0: IDLE 0x2: REQ. Request in process 0x4: WFDLE. Wait for read data 0x6: WFVLDCLR. Wait for valid flag clearing Others: Reserved
15:0	WACS2_RDATA	**Wrapper Access: read data.** SW must check if valid flag equals to 1 before using this read data.

1000D0A8 WACS2_VLDCLR Wapper Access (#2) Valid Clear 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WACS2_VLDCLR
Type																WO
Reset																0

Bit(s)	Name	Description
0	WACS2_VLDCLR	Write 1 to clear valid flag.

1000D0AC WACS3_EN Wapper Access (#3) Enable 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WACS3_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	WACS3_EN	**Enables wrapper access** Set to disable will reset the FSM.

Bit(s)	Name	Description
		0: Disable 1: Enable

1000D0B0 INIT_DONE3 Initialization Done 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INIT_DONE3
Type																RW
Reset																0

Bit(s)	Name	Description
0	INIT_DONE3	**Indicates initialization is finished.** During SPI transactions, if this bit is detected low, then current transaction may fail, which requires re-do or debugging. 0: Initialization is not yet finished. 1: Initialization is finished.

1000D0B4 WACS3_CMD Wapper Access (#3) Command 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WACS3_WRITE	WACS3_ADR														
Type	RW	RW														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WACS3_WDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	WACS3_WRITE	**Wrapper access: Read/write direction** 0: Read 1: Write
30:16	WACS3_ADR	**Wrapper access: Address[15:1]**
15:0	WACS3_WDATA	**Wrapper access: Write data[15:0]**

1000D0B8 WACS3_RDATA Wapper Access (#3) Read Data 80500000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WACS3_FIFO_FREECNT				WACS3_FIFO_FILLCNT					SYS_IDLE3	INIT_DONE3	SYNC_IDLE3	WACS3_REQ	WACS3_FSM		
Type	RU				RU					RU	RU	RU	RU	RU		
Reset	1	0	0	0	0	0	0	0		1	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WACS3_RDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	WACS3_FIFO_FREECNT	**Records the number of data can be filled into FIFO**
27:24	WACS3_FIFO_FILLCNT	**Records the number of data filled into FIFO**
22	SYS_IDLE3	**PMIC_WRAP busy status indicator:** 1. WACS 0/1/2 idle 2. no arbitor request 3, no spi_wrap to mux request 4. no waiting read data 5. spi_man is idle 6. spI_sync is idle 0: PMIC_WRAP is busy 1: PMIC_WRAP is IDLE
21	INIT_DONE3	**Indicates initialization is finished.** During SPI transactions, if this bit is detected low, then current transaction may fail, which requires re-do or debugging. (This is equivalent to INIT_DONE) 0: Initialization is not yet finished 1: Initialization is finished.
20	SYNC_IDLE3	**SYNC module busy status.** It is used to judge if the request has reached SYNC module. 0: SYNC module is busy 1: SYNC module is IDLE
19	WACS3_REQ	**Wrapper access request indicator.** 0: No WACS request is awaiting grant. 1: One WACS Request is still awaiting grant.
18:16	WACS3_FSM	**Current WACS FSM states.** 0x0: IDLE 0x2: REQ. Request in process 0x4: WFDLE. Wait for read data 0x6: WFVLDCLR. Wait for valid flag clearing Others: Reserved
15:0	WACS3_RDATA	**Wrapper Access: read data.** SW must check if valid flag equals to 1 before using this read data.

1000D0BC WACS3_VLDCLR Wapper Access (#3) Valid Clear 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WACS3_VLDCLR
Type																WO
Reset																0

Bit(s)	Name	Description
0	WACS3_VLDCLR	Write 1 to clear valid flag.

1000D0C0 INT0_EN Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT0_EN[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT0_EN[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT0_EN	**Interrupt enable for each source.** [31]: Reserved [30]: INIT_FLOW_REQ_ERR: LTE CO_CLOCK initial flow request error [29]: WACS3_CMD_MISS: A WACS3 CMD is written while WACS3 is disabled [28]: WACS3_UNEXP_DLE: WACS3 unexpected DLE [27]: WACS3_UNEXP_VLDCLR: WACS3 unexpected VLDCLR [26]: C2K_REQ_ERR:C2K request errors occurs [25]: MD_ADC_DLE_CNT_OVF: MD_ADC DLE counter is overflowd [24]: MD_ADC_ALE_CNT_OVF: MD_ADC ALE counter is overflowd [23]: STAUPD_DLE_CNT_OVF: STAUPD DLE counter is overflowed. [22]: STAUPD_ALE_CNT_OVF: STAUPD ALE counter is overflowed. [21]: MDINF_REQ_ERR: Modem request error occurs [20]: WACS2_CMD_MISS: A WACS2 CMD is written while WACS2 is disabled. [19]: WACS2_UNEXP_DLE: WACS2 unexpected DLE [18]: WACS2_UNEXP_VLDCLR: WACS2 unexpected VLDCLR [17]: WACS1_CMD_MISS: A WACS1 CMD is written while WACS1 is disabled. [16]: WACS1_UNEXP_DLE: WACS1 unexpected DLE [15]: WACS1_UNEXP_VLDCLR: WACS1 unexpected VLDCLR [14]: WACS0_CMD_MISS: A WACS0 CMD is written while WACS0 is disabled. [13]: WACS0_UNEXP_DLE: WACS0 unexpected DLE [12]: WACS0_UNEXP_VLDCLR: WACS0 unexpected VLDCLR [11]: HARB_DLE_OVF: High priority aribiter DLE is overflowed. [10]: HARB_DLE_UNF: High priority aribiter DLE is underflowed. [9]: WRAP_AGDLE_OVF: WRAP agent DLE counter is overflowed. [8]: WRAP_AGDLE_UNF: WRAP agent DLE counter is underflowed. [7]: WRAP_CHDLE_OVF: WRAP channel DLE counter is overflowed. [6]: WRAP_CHDLE_UNF: WRAP channel DLE counter is underflowed. [5]: MAN_CMD_MISS: A MAN CMD is written while MAN is disabled. [4]: MAN_UNEXP_DLE: MAN unexpected DLE [3]: MAN_UNEXP_VLDCLR: MAN unexpected VLDCLR [2]: SIG_ERR1: Signature 1 Checking failed. [1]: SIG_ERR: Signature Checking failed. [0]: WDT_INT: WatchDog Timeout

1000D0C4 INT0_FLG_RAW Interrupt Flags - Raw 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT0_FLG_RAW[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT0_FLG_RAW[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT0_FLG_RAW	Interrupt flags (not gated with INT_EN)

1000D0C8 INT0_FLG Interrupt Flags 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT0_FLG[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT0_FLG[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT0_FLG	[31]: Reserved [30]: INIT_FLOW_REQ_ERR: LTE CO_CLOCK initial flow request error [29]: WACS3_CMD_MISS: A WACS3 CMD is written while WACS3 is disabled [28]: WACS3_UNEXP_DLE: WACS3 unexpected DLE [27]: WACS3_UNEXP_VLDCLR: WACS3 unexpected VLDCLR [26]: C2K_REQ_ERR:C2K request errors occurs [25]: MD_ADC_DLE_CNT_OVF: MD_ADC DLE counter is overflowd [24]: MD_ADC_ALE_CNT_OVF: MD_ADC ALE counter is overflowd [23]: STAUPD_DLE_CNT_OVF: STAUPD DLE counter is overflowed. [22]: STAUPD_ALE_CNT_OVF: STAUPD ALE counter is overflowed. [21]: MDINF_REQ_ERR: Modem request error occurs [20]: WACS2_CMD_MISS: A WACS2 CMD is written while WACS2 is disabled. [19]: WACS2_UNEXP_DLE: WACS2 unexpected DLE [18]: WACS2_UNEXP_VLDCLR: WACS2 unexpected VLDCLR [17]: WACS1_CMD_MISS: A WACS1 CMD is written while WACS1 is disabled. [16]: WACS1_UNEXP_DLE: WACS1 unexpected DLE [15]: WACS1_UNEXP_VLDCLR: WACS1 unexpected VLDCLR [14]: WACS0_CMD_MISS: A WACS0 CMD is written while WACS0 is disabled. [13]: WACS0_UNEXP_DLE: WACS0 unexpected DLE [12]: WACS0_UNEXP_VLDCLR: WACS0 unexpected VLDCLR [11]: HARB_DLE_OVF: High priority aribiter DLE is overflowed. [10]: HARB_DLE_UNF: High priority aribiter DLE is underflowed. [9]: WRAP_AGDLE_OVF: WRAP agent DLE counter is overflowed. [8]: WRAP_AGDLE_UNF: WRAP agent DLE counter is underflowed. [7]: WRAP_CHDLE_OVF: WRAP channel DLE counter is overflowed. [6]: WRAP_CHDLE_UNF: WRAP channel DLE counter is underflowed. [5]: MAN_CMD_MISS: A MAN CMD is written while MAN is disabled. [4]: MAN_UNEXP_DLE: MAN unexpected DLE [3]: MAN_UNEXP_VLDCLR: MAN unexpected VLDCLR [2]: SIG_ERR1: Signature 1 Checking failed. [1]: SIG_ERR: Signature Checking failed. [0]: WDT_INT: WatchDog Timeout

1000D0CC INT0_CLR Interrupt Clear 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT0_CLR[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT0_CLR[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT0_CLR	Clear interrupt flags by writing 1 to the corresponding bit.

1000D0D0 INT1_EN Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT1_EN[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT1_EN[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT1_EN	**Interrupt enable for each source** [31: 17]: RESERVED [16]: priroty_13 reach the starvation threshold [15]: priroty_12 reach the starvation threshold [14]: priroty_11 reach the starvation threshold [13]: priroty_10 reach the starvation threshold [12]: priroty_9 reach the starvation threshold [11]: priroty_8 reach the starvation threshold [10]: priroty_7 reach the starvation threshold [9]: priroty_6 reach the starvation threshold [8]: priroty_5 reach the starvation threshold [7]: priroty_4 reach the starvation threshold [6]: priroty_3 reach the starvation threshold [5]: priroty_2 reach the starvation threshold [4]: priroty_1 reach the starvation threshold [3]: priroty_0 reach the starvation threshold [2]: WACS_P2P_CMD_MISS: A WACS2 CMD is written while WACS2 is disabled. [1]: WACS_P2P_UNEXP_DLE: WACS2 unexpected DLE [0]: WACS_P2P_UNEXP_VLDCLR: WACS2 unexpected VLDCLR

1000D0D4 INT1_FLG_RAW Interrupt Flags - Raw 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT1_FLG_RAW[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT1_FLG_RAW[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT1_FLG_RAW	Interrupt flags (not gated with INT_EN)

1000D0D8 INT1_FLG Interrupt Flags 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT1_FLG[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT1_FLG[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT1_FLG	[31]: DEBUG_INT: Selected DEBUG source is asserted. [30:24]: RESERVED [23]: STAUPD_DLE_CNT_OVF: STAUPD DLE counter is overflowed. [22]: STAUPD_ALE_CNT_OVF: STAUPD ALE counter is overflowed. [21]: Modem request error occurs [20]: WACS2_CMD_MISS: A WACS2 CMD is written while WACS2 is disabled. [19]: WACS2_UNEXP_DLE: WACS2 unexpected DLE [18]: WACS2_UNEXP_VLDCLR: WACS2 unexpected VLDCLR [17]: WACS1_CMD_MISS: A WACS1 CMD is written while WACS1 is disabled. [16]: WACS1_UNEXP_DLE: WACS1 unexpected DLE [15]: WACS1_UNEXP_VLDCLR: WACS1 unexpected VLDCLR [14]: WACS0_CMD_MISS: A WACS0 CMD is written while WACS0 is disabled. [13]: WACS0_UNEXP_DLE: WACS0 unexpected DLE [12]: WACS0_UNEXP_VLDCLR: WACS0 unexpected VLDCLR [11]: HARB_DLE_OVF: High priority aribiter DLE is overflowed. [10]: HARB_DLE_UNF: High priority aribiter DLE is underflowed. [9]: WRAP_AGDLE_OVF: WRAP agent DLE counter is overflowed. [8]: WRAP_AGDLE_UNF: WRAP agent DLE counter is underflowed. [7]: WRAP_CHDLE_OVF: WRAP channel DLE counter is overflowed. [6]: WRAP_CHDLE_UNF: WRAP channel DLE counter is underflowed. [5]: MAN_CMD_MISS: A MAN CMD is written while MAN is disabled. [4]: MAN_UNEXP_DLE: MAN unexpected DLE [3]: MAN_UNEXP_VLDCLR: MAN unexpected VLDCLR [2]: SIG_ERR1: Signature 1 Checking failed. [1]: SIG_ERR: Signature Checking failed. [0]: WDT_INT: WatchDog Timeout

1000D0DC INT1_CLR Interrupt Clear 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT1_CLR[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT1_CLR[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT1_CLR	Clear interrupt flags by writing 1 to the corresponding bit.

1000D0E0 SIG_ADR Signature Address in MT63xx 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SIG_ADR1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIG_ADR0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SIG_ADR1	The signature address @PMIC side to be automatically checked. STAUPD circuit will fetch from address every STAUPD_PRD time.
15:0	SIG_ADR0	The signature address @PMIC side to be automatically checked. STAUPD circuit will fetch from address every STAUPD_PRD time.

1000D0E4 SIG_MODE Signature Checking Mode in MT63xx 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SIG_MODE1	SIG_MODE0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	SIG_MODE1	**Signature checking mode selection** 0: Check CRC value 1: Check SIG_VALUE
0	SIG_MODE0	**Signature checking mode selection** 0: Check CRC value 1: Check SIG_VALUE

1000D0E8 SIG_VALUE Signature Value in MT63xx 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SIG_VALUE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIG_VALUE0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SIG_VALUE1	**The signature value @PMIC side to be automatically checked.** If fetched data by STAUPD circuit does not match SIG_VALUE, an error interrupt (SIG_ERR) will be assert.
15:0	SIG_VALUE0	**The signature value @PMIC side to be automatically checked.** If fetched data by STAUPD circuit does not match SIG_VALUE, an error interrupt (SIG_ERR) will be assert.

1000D0EC SIG_ERRVAL Error Signature Value in MT63xx 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SIG_ERRVAL1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIG_ERRVAL0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SIG_ERRVAL1	When SIG_ERR occurs, the erronous signature will be latched and can be read out from this.
15:0	SIG_ERRVAL0	When SIG_ERR occurs, the erronous signature will be latched and can be read out from this.

1000D0F0 CRC_EN CRC enable 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CRC_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	CRC_EN	**Set 1 to enable CRC calculation of ADR[15:0], RDATA[15:0] and WDATA[15:0]** 0: Disable 1: Enable

1000D0F4 TIMER_EN Timer Enable 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TIMER_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	TIMER_EN	**Timer clock enable. Disable timer clock before modifying timer-related setting to avoid asynchronous issues.** 0: Disable 1: Enable

1000D0F8 TIMER_STA Timer Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				STAUPD_TIMER												

Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDT_TIMER															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	STAUPD_TIMER	**STAUPD timer status** Unit: 38ns
15:0	WDT_TIMER	**Watch Dog timer status** Unit: 38ns

1000D0FC WDT_UNIT Watch Dog Timer Unit 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													WDT_UNIT			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	WDT_UNIT	**Watch Dog timer unit selection** Watch Dog time-out will occur in 2~3 units. Unit is selected as WDT_TIMER[WDT_UNIT] which is a counter by 26MHz. Ex. if WDT_UNIT = 0x8, then watch dog time-out will occur in (2~3)*(2^9)*38ns = 38.9us ~ 58.4us 0: Disable 8: 38.9us ~ 58.4us 15: 5ms ~ 7.5ms

1000D100 WDT_SRC_EN Watch Dog Timer Source Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDT_SRC_EN[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDT_SRC_EN[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDT_SRC_EN	**Watch dog timer source enable** [31]: RESERVED [30]: RESERVED [29]: RESERVED [28]: RESERVED [27]: HARB_WACS3_DLE: HARB to WACS3 DLE timeout monitor [26]: PREADY: APB PREADY timeout monitor [25]: STAUPD_TRIG: STAUPD trigger signal timeout monitor [24]: MSTCTL_SYNC_DLE: MSTCTL to SYNC DLE timeout monitor [23]: MUX_MAN_DLE: MUX to MAN DLE timeout monitor [22]: MUX_WRAP_DLE: MUX to WRAP DLE timeout monitor [21]: HARB_WACSP2P_DLE: HARB to WACSP2P DLE timeout monitor

Bit(s)	Name	Description
		[20]: HARB_STAUPD_DLE: HARB to STAUPD DLE timeout monitor [19]: HARB_SPMINF_DLE: HARB to SPMINF DLE timeout monitor [18]: HARB_WACS2_DLE: HARB to WACS2 DLE timeout monitor [17]: HARB_WACS1_DLE: HARB to WACS1 DLE timeout monitor [16]: HARB_WACS0_DLE: HARB to WACS0 DLE timeout monitor [15]: SYNC_MUX_ALE: SYNC to MUX ALE timeout monitor [14]: MUX_MAN_ALE: MUX to MAN ALE timeout monitor [13]: MUX_WRAP_ALE: MUX to WRAP ALE timeout monitor [12]: WRAP_HARB_ALE: WRAP to HARB ALE timeout monitor [11]: HARB_WACSP2P_ALE: HARB to WACSP2P ALE timeout monitor [10]: HARB_MA_ADC_DLE: HARB to MD_ADC DLE timeout monitor [9]: HARB_WACS3_ALE: HARB to WACS3 ALE timeout monitor [8]: HARB_STAUPD_ALE: HARB to STAUPD ALE timeour monitor [7]: HARB_GPSINF_ALE: HARB to GPSINF ALE timeour monitor [6]: HARB_WACS1_ALE: HARB to WACS1 ALE timeout monitor [5]: HARB_MD_ADC_ALE: HARB to MD_ADC ALE timeour monitor [4]: HARB_WACS2_ALE: HARB to WACS2 ALE timeout monitor [3]: HARB_SPMINF_ALE: HARB to SPMINF ALE timeour monitor [2]: HARB_WACS0_ALE: HARB to WACS0 ALE timeout monitor [1]: HARB_C2KINF_ALE: HARB to C2KINF ALE timeour monitor [0]: HARB_MDINF_ALE: HARB to MDINF ALE timeout monitor

1000D104 WDT_FLG Watch Dog Flag 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDT_FLG[31:16]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDT_FLG[15:0]															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDT_FLG	[31]: RESERVED [30]: RESERVED [29]: RESERVED [28]: RESERVED [27]: HARB_WACS3_DLE: HARB to WACS3 DLE timeout monitor [26]: PREADY: APB PREADY timeout monitor [25]: STAUPD_TRIG: STAUPD trigger signal timeout monitor [24]: MSTCTL_SYNC_DLE: MSTCTL to SYNC DLE timeout monitor [23]: MUX_MAN_DLE: MUX to MAN DLE timeout monitor [22]: MUX_WRAP_DLE: MUX to WRAP DLE timeout monitor [21]: HARB_WACSP2P_DLE: HARB to WACSP2P DLE timeout monitor [20]: HARB_STAUPD_DLE: HARB to STAUPD DLE timeout monitor [19]: HARB_SPMINF_DLE: HARB to SPMINF DLE timeout monitor [18]: HARB_WACS2_DLE: HARB to WACS2 DLE timeout monitor [17]: HARB_WACS1_DLE: HARB to WACS1 DLE timeout monitor [16]: HARB_WACS0_DLE: HARB to WACS0 DLE timeout monitor [15]: SYNC_MUX_ALE: SYNC to MUX ALE timeout monitor [14]: MUX_MAN_ALE: MUX to MAN ALE timeout monitor [13]: MUX_WRAP_ALE: MUX to WRAP ALE timeout monitor [12]: WRAP_HARB_ALE: WRAP to HARB ALE timeout monitor [11]: HARB_WACSP2P_ALE: HARB to WACSP2P ALE timeout monitor [10]: HARB_MA_ADC_DLE: HARB to MD_ADC DLE timeout monitor [9]: HARB_WACS3_ALE: HARB to WACS3 ALE timeout monitor [8]: HARB_STAUPD_ALE: HARB to STAUPD ALE timeour monitor [7]: HARB_GPSINF_ALE: HARB to GPSINF ALE timeour monitor

Bit(s)	Name	Description
		[6]: HARB_WACS1_ALE: HARB to WACS1 ALE timeout monitor [5]: HARB_MD_ADC_ALE: HARB to MD_ADC ALE timeour monitor [4]: HARB_WACS2_ALE: HARB to WACS2 ALE timeout monitor [3]: HARB_SPMINF_ALE: HARB to SPMINF ALE timeour monitor [2]: HARB_WACS0_ALE: HARB to WACS0 ALE timeout monitor [1]: HARB_C2KINF_ALE: HARB to C2KINF ALE timeour monitor [0]: HARB_MDINF_ALE: HARB to MDINF ALE timeout monitor

1000D108 DEBUG_INT_SEL Debug Interrupt Selection 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DEBUG_INT_SEL		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	DEBUG_INT_SEL	**Debug flag as interrupt source selection** Select which bit of debug_out3[7:0] is used as interrupt source.

1000D10C DVFS_ADR0 DVFS Command #0 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR0	DVFS Command #0 - Address

1000D110 DVFS_WDATA0 DVFS Command #0 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA0	DVFS Command #0 - Write Data

1000D114 DVFS_ADR1 DVFS Command #1 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR1	DVFS Command #1 - Address

1000D118 DVFS_WDATA1 DVFS Command #1 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA1	DVFS Command #1 - Write Data

1000D11C DVFS_ADR2 DVFS Command #2 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR2	DVFS Command #2 - Address

1000D120 DVFS_WDATA2 DVFS Command #2 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA2	DVFS Command #2 - Write Data

1000D124 DVFS_ADR3 DVFS Command #3 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR3	DVFS Command #3 - Address

1000D128 DVFS_WDATA3 DVFS Command #3 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA3	DVFS Command #3 - Write Data

1000D12C DVFS_ADR4 DVFS Command #4 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR4	DVFS Command #4 - Address

1000D130 DVFS_WDATA4 DVFS Command #4 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA4	DVFS Command #4 - Write Data

1000D134 DVFS_ADR5 DVFS Command #5 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR5	DVFS Command #5 - Address

1000D138 DVFS_WDATA5 DVFS Command #5 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA5															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA5	DVFS Command #5 - Write Data

1000D13C DVFS_ADR6 DVFS Command #6 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR6	DVFS Command #6 - Address

1000D140 DVFS_WDATA6 DVFS Command #6 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA6	DVFS Command #6 - Write Data

1000D144 DVFS_ADR7 DVFS Command #7 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR7	DVFS Command #7 - Address

1000D148 DVFS_WDATA7 DVFS Command #7 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA7	DVFS Command #7 - Write Data

1000D14C DVFS_ADR8 DVFS Command #8 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR8															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR8	DVFS Command #8 - Address

1000D150 DVFS_WDATA8 DVFS Command #8 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA8															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA8	DVFS Command #8 - Write Data

1000D154 DVFS_ADR9 DVFS Command #9 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR9															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR9	DVFS Command #9 - Address

1000D158 DVFS_WDATA9 DVFS Command #9 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA9															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA9	DVFS Command #9 - Write Data

1000D15C DVFS_ADR10 DVFS Command #10 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR10															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR10	DVFS Command #10 - Address

1000D160 DVFS_WDATA10 DVFS Command #10 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA10	DVFS Command #10 - Write Data

1000D164 DVFS_ADR11 DVFS Command #11 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR11	DVFS Command #11 - Address

1000D168 DVFS_WDATA11 DVFS Command #11 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA11	DVFS Command #11 - Write Data

1000D16C DVFS_ADR12 DVFS Command #12 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR12	DVFS Command #12 - Address

1000D170 DVFS_WDATA12 DVFS Command #12 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA12	DVFS Command #12 - Write Data

1000D174 DVFS_ADR13 DVFS Command #13 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR13	DVFS Command #13 - Address

1000D178 DVFS_WDATA13 DVFS Command #13 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA13	DVFS Command #13 - Write Data

1000D17C DVFS_ADR14 DVFS Command #14 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR14															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR14	DVFS Command #14 - Address

1000D180 DVFS_WDATA14 DVFS Command #14 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA14															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA14	DVFS Command #14 - Write Data

1000D184 DVFS_ADR15 DVFS Command #15 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_ADR15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_ADR15	DVFS Command #15 - Address

1000D188 DVFS_WDATA15 DVFS Command #15 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DVFS_WDATA15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DVFS_WDATA15	DVFS Command #15 - Write Data

1000D18C DCXO_ENABLE DCXO_ENABLE 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															DCXO_CONN_ENABLE	DCXO_NFC_ENABLE
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	DCXO_CONN_ENABLE	**DCXO conn interfce enable** 0: Disable 1: Enable
0	DCXO_NFC_ENABLE	**DCXO nfc interfce enable** 0: Disable 1: Enable

1000D190 DCXO_CONN DCXO_CONN Command #0 - Address 0000

ADR0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCXO_CONN_ADR0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DCXO_CONN_ADR0	DCXO_CONN Command #0 - Address

1000D194 DCXO_CONN_WDATA0 DCXO_CONN Command #0 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCXO_CONN_WDATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DCXO_CONN_WDATA0	DCXO_CONN Command #0 - Write Data

1000D198 DCXO_CONN_ADR1 DCXO_CONN Command #1 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCXO_CONN_ADR1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DCXO_CONN_ADR1	DCXO_CONN Command #1 - Address

1000D19C DCXO_CONN_WDATA1 DCXO_CONN Command #1- Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCXO_CONN_WDATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DCXO_CONN_WDATA1	DCXO_CONN Command #1- Write Data

1000D1A0 DCXO_NFC_ADR0 DCXO_NFC Command #0 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	DCXO_NFC_ADR0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DCXO_NFC_ADR0	DCXO_NFC Command #0 - Address

1000D1A4 DCXO_NFC_WDATA0 DCXO_NFC Command #0 - Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCXO_NFC_WDATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DCXO_NFC_WDATA0	DCXO_NFC Command #0 - Write Data

1000D1A8 DCXO_NFC_ADR1 DCXO_NFC Command #1 - Address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCXO_NFC_ADR1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DCXO_NFC_ADR1	DCXO_NFC Command #1 - Address

1000D1AC DCXO_NFC_WDATA1 DCXO_NFC Command #1- Write Data 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCXO_NFC_WDATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DCXO_NFC_WDATA1	DCXO_NFC Command #1- Write Data

1000D1B0 SPMINF_STA SPM interface status register 003C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SPMINF_STA											
Type					RU											
Reset					0	0	0	0	0	0	1	1	1	1	0	0

Bit(s)	Name	Description
11:0	SPMINF_STA	**SPM interface status, involing status of DVFS control, sleep handshake interface and PMIC_IRQ interface** [11]: SYS_IDLE [10]: SLEEP_ACK [9]: SLEEP_REQ [8]: PMIC_SCP_IRQ [7]: PMIC_IRQ_ACK [6]: PMIC_IRQ_REQ [5: 2] DVFS_CTRL [1]: DVFS_CTRL_ACK [0]: DVFS_CTRL_RDY

1000D1B4 CIPHER_KEY_SEL CIPHER Key Selection 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CIPHER_KEY_SEL	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	CIPHER_KEY_SEL	**CIPHER key selection** All keys are hard-wired.

1000D1B8 CIPHER_IV_SEL CIPHER Initial Vector Selection 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CIPHER_IV_SEL	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	CIPHER_IV_SEL	**CIPHER initial vector selection** Set 0 to choose manual initial vector, otherwise, choose other Hard-wired initial vectors.

1000D1BC CIPHER_EN CIPHER Engine Enable 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CIPHER_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	CIPHER_EN	CIPHER engine start

1000D1C0 CIPHER_RDY CIPHER Data Ready 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CIPHER_RDY	
Type															RU	
Reset															0	0

Bit(s)	Name	Description
1:0	CIPHER_RDY	**CIPHER data ready** Bit 0 is for cipher 0, Bit 1 is for cipher 1 Data should be ready before enable CIPHER_MODE 0: Not ready 1: Ready

1000D1C4 CIPHER_MODE CIPHER Mode Enable 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CIPHER_MODE
Type																RW
Reset																0

Bit(s)	Name	Description
0	CIPHER_MODE	**CIPHER mode enable** 0: Disable 1: Enable

1000D1C8 CIPHER_SWRST CIPHER Soft Reset 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CIPHER_SWRST
Type																RW
Reset																0

Bit(s)	Name	Description
0	CIPHER_SWRST	CIPHER soft reset

1000D1CC DCM_EN Internal DCM Enable 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DCM_SPI	DCXO_CK_	MD_DVFS	STAUPD_C	GPS_CK_S	CO_CK_SE	SPM_CK_S	C2K_CK_S	MD_CK_S	CRC_CK_S	DCM_EN

						_EN	SEL	_CK_SEL	K_SEL	EL	L	EL	EL	EL	EL	
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	DCM_SPI_EN	**Enable internal SPI_CK DCM** 0: Disable internal SPI_CK DCM 1: Enable internal SPI_CK DCM. When PMIC_WRAP is in idle state, the clock will be gated.
9	DCXO_CK_SEL	**DCXO HW clock selection** 0: choose non-DCM clock 1: choose DCM clock
8	MD_DVFS_CK_SEL	**MD_DVFS HW clock selection** 0: choose non-DCM clock 1: choose DCM clock
7	STAUPD_CK_SEL	**STAUPD HW clock selection** 0: choose non-DCM clock 1: choose DCM clock
6	GPS_CK_SEL	**GPS HW clock selection** 0: choose non-DCM clock 1: choose DCM clock
5	CO_CK_SEL	**Co-clock HW clock selection** 0: choose non-DCM clock 1: choose DCM clock
4	SPM_CK_SEL	**SPM HW clock selection** 0: choose non-DCM clock 1: choose DCM clock
3	C2K_CK_SEL	**C2K HW clock selection** 0: choose non-DCM clock 1: choose DCM clock
2	MD_CK_SEL	**MD HW clock selection** 0: choose non-DCM clock 1: choose DCM clock
1	CRC_CK_SEL	**CRC clock selection** 0: choose non-DCM clock 1: choose DCM clock
0	DCM_EN	**Enable internal SYS_CK DCM** 0: Disable internal SYS_CK DCM 1: Enable internal SYS_CK DCM. When PMIC_WRAP is in idle state, the clock will be gated.

1000D1D0 DCM_SPI_DBC_PRD Debounce Period at Entering DCM Mode for SPI_CK 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DCM_SPI_DBC_PRD							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DCM_SPI_DBC_PRD	**Debounce period before entering DCM mode for SPI_CK** 0: Disable debounce.

1000D1D4 DCM_DBC_PRD Debounce Period at Entering DCM Mode for SYS_CK 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DCM_DBC_PRD							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DCM_DBC_PRD	**Debounce period before entering DCM mode for SYS_CK** 0: Disable debounce.

1000D1D8 EXT_CK Extra Clock number 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EXT_CK
Type																RW
Reset																0

Bit(s)	Name	Description
0	EXT_CK	Extra Clock number = (1 + EXT_CK)

1000D1DC ADC_CMD_ADDR AuxADC command register address 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_CMD_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ADC_CMD_ADDR	AuxADC command register address

1000D1E0 PWRAP_ADC_CMD Command to AuxADC 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PWRAP_ADC_CMD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PWRAP_ADC_CMD	Command to AuxADC

1000D1E4 ADC_RDATA_ADDR Address of thermal data [15:0] register in AuxADC 0004

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_RDATA_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
15:0	ADC_RDATA_ADDR	Address of thermal data [15:0] register in AuxADC

1000D1E8 GPS_STA GPS Interface Status (Debug) 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PWRAP_GPS_WDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						GPS_INF_FSM			GPSINF_ALE_CNT		GPSINF_DLE_CNT				GPS_PWRAP_REQ	PWRAP_GPS_ACK
Type						RU			RU		RU				RU	RU
Reset						0	0	1	0	0	0	0			0	0

Bit(s)	Name	Description
31:17	PWRAP_GPS_WDATA	**AUXADC thermal data for GPS**
10:8	GPS_INF_FSM	**Current GPSINF FSM State** 1: IDLE 2: REQ 4: WFRDY
7:6	GPSINF_ALE_CNT	**GPS interface ale count**
5:4	GPSINF_DLE_CNT	**GPS interface dle count**
1	GPS_PWRAP_REQ	**GPS request**
0	PWRAP_GPS_ACK	**AUXADC data ready bit for GPS**

1000D1EC SWRST Software reset 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SWRST
Type																RW
Reset																0

Bit(s)	Name	Description
0	SWRST	0: Idle 1: Reset

1000D1F0 HARB_SLEEP Enable the sleep gated harb function 00

_GATED_CTRL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HARB_SLEEP_GATED_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	HARB_SLEEP_GATED_EN	0: Disable 1: Enable

1000D1F4 MD_ADC_RDATA_ADDR_LATEST Address of the latest thermal data [15:0] register in AuxADC 0008

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR_LATEST															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR_LATEST	Address of the latest thermal data [15:0] register in AuxADC

1000D1F8 MD_ADC_RDATA_ADDR_WP Address of the latest bufter thermal data pointer 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR_WP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR_WP	Address of the latest bufter thermal data pointer

1000D1FC MD_ADC_RDATA_ADDRo Address of the buffer thermal datao 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDRo															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR0	Address of the buffer thermal data0

1000D200 MD_ADC_RDATA_ADDR1 Address of the buffer thermal data1 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR1	Address of the buffer thermal data1

1000D204 MD_ADC_RDATA_ADDR2 Address of the buffer thermal data2 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR2	Address of the buffer thermal data2

1000D208 MD_ADC_RDATA_ADDR3 Address of the buffer thermal data3 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR3	Address of the buffer thermal data3

1000D20C MD_ADC_RDATA_ADDR4 Address of the buffer thermal data4 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR4	Address of the buffer thermal data4

1000D210 MD_ADC_RDATA_ADDR5 Address of the buffer thermal data5 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR5	Address of the buffer thermal data5

1000D214 MD_ADC_RDATA_ADDR6 Address of the buffer thermal data6 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR6	Address of the buffer thermal data6

1000D218 MD_ADC_RDATA_ADDR7 Address of the buffer thermal data7 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR7	Address of the buffer thermal data7

1000D21C MD_ADC_RDATA_ADDR8 Address of the buffer thermal data8 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR8															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR8	Address of the buffer thermal data8

1000D220 MD_ADC_RDATA_ADDR9 Address of the buffer thermal data9 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR9															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR9	Address of the buffer thermal data9

1000D224 MD_ADC_RDATA_ADDR10 Address of the buffer thermal data10 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR10	Address of the buffer thermal data10

1000D228 MD_ADC_RDATA_ADDR11 Address of the buffer thermal data11 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR11	Address of the buffer thermal data11

1000D22C MD_ADC_RDATA_ADDR12 Address of the buffer thermal data12 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR12	Address of the buffer thermal data12

1000D230 MD_ADC_RDATA_ADDR13 Address of the buffer thermal data13 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR13	Address of the buffer thermal data13

1000D234 MD_ADC_RDATA_ADDR14 Address of the buffer thermal data14 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR14															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR14	Address of the buffer thermal data14

1000D238 MD_ADC_RDATA_ADDR15 Address of the buffer thermal data15 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR15	Address of the buffer thermal data15

1000D23C MD_ADC_RDATA_ADDR16 Address of the buffer thermal data16 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR16															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR16	Address of the buffer thermal data16

1000D240 MD_ADC_RDATA_ADDR17 Address of the buffer thermal data17 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR17															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR17	Address of the buffer thermal data17

1000D244 MD_ADC_RDATA_ADDR18 Address of the buffer thermal data18 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR18															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR18	Address of the buffer thermal data18

1000D248 MD_ADC_RDATA_ADDR19 Address of the buffer thermal data19 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR19															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR19	Address of the buffer thermal data19

1000D24C MD_ADC_RDATA_ADDR20 Address of the buffer thermal data20 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR20															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR20	Address of the buffer thermal data20

1000D250 MD_ADC_RDATA_ADDR21 Address of the buffer thermal data21 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR21															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR21	Address of the buffer thermal data21

1000D254 MD_ADC_RDATA_ADDR22 Address of the buffer thermal data22 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR22															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR22	Address of the buffer thermal data22

1000D258 MD_ADC_RDATA_ADDR23 Address of the buffer thermal data23 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR23															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR23	Address of the buffer thermal data23

1000D25C MD_ADC_RDATA_ADDR24 Address of the buffer thermal data24 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR24															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR24	Address of the buffer thermal data24

1000D260 MD_ADC_RDATA_ADDR25 Address of the buffer thermal data25 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR25															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR25	Address of the buffer thermal data25

1000D264 MD_ADC_RDATA_ADDR26 Address of the buffer thermal data26 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR26															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR26	Address of the buffer thermal data26

1000D268 MD_ADC_RDATA_ADDR27 Address of the buffer thermal data27 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR27															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR27	Address of the buffer thermal data27

1000D26C MD_ADC_RDATA_ADDR28 Address of the buffer thermal data28 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR28															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR28	Address of the buffer thermal data28

1000D270 MD_ADC_RDATA_ADDR29 Address of the buffer thermal data29 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR29															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR29	Address of the buffer thermal data29

1000D274 MD_ADC_RDATA_ADDR30 Address of the buffer thermal data30 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR30															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR30	Address of the buffer thermal data30

1000D278 MD_ADC_RDATA_ADDR31 Address of the buffer thermal data31 000A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_RDATA_ADDR31															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:0	MD_ADC_RDATA_ADDR31	Address of the buffer thermal data31

1000D27C MD_ADC_MODE_SEL MD_AUXADC_MODE_LATCH_SEL 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MD_ADC_MODE_LATCH_

																SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	MD_ADC_MODE_LATCH_SEL	1'b1: Normal mode first 1'b0: Initial mode first

1000D280 MD_ADC_STA0 MD_AUXADC Interface Status0 (Debug) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PWRAP_MD_ADC_TEMP_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31:16	PWRAP_MD_ADC_TEMP_DATA	

1000D284 MD_ADC_STA1 MD_AUXADC Interface Status1 (Debug) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						MD_ADC_DLE_CNT_REAL						MD_ADC_ALE_CNT[5:1]				
Type						RU						RU				
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MD_ADC_ALE_CNT[0:0]													MD_ADC_FSM		
Type	RU													RU		
Reset	0													0	0	0

Bit(s)	Name	Description
26:21	MD_ADC_DLE_CNT_REAL	
20:15	MD_ADC_ALE_CNT	
2:0	MD_ADC_FSM	

1000D288 PRIORITY_USER_SEL_0 ARBITER_PRIORITY_USER_SEL_0 76543210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARBITER_SEL_CH7				ARBITER_SEL_CH6				ARBITER_SEL_CH5				ARBITER_SEL_CH4			
Type	RW				RW				RW				RW			

Reset	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARBITER_SEL_CH3				ARBITER_SEL_CH2				ARBITER_SEL_CH1				ARBITER_SEL_CH0			
Type	RW				RW				RW				RW			
Reset	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:28	ARBITER_SEL_CH7	**Selects the user of the priority_7** [15]: RESERVE [14]: RESERVE [13]: WACS_P2P [12]: WACS1 (MD SW1) [11]: WACS2 (AP SW) [10]: GPSINF [9]: STAUPD [8]: MD_ADCINF [7]: DCXO_NFCINF [6]: DCXO_CONNINF [5]: WACS3(C2K SW) [4]: DVFSINF (SPMINF) [3]: WACS0 (MD SW0) [2]: MD_DVFSINF [1]: C2kINF [0]: MDINF
27:24	ARBITER_SEL_CH6	**Selects the user of the priority_6** [15]: RESERVE [14]: RESERVE [13]: WACS_P2P [12]: WACS1 (MD SW1) [11]: WACS2 (AP SW) [10]: GPSINF [9]: STAUPD [8]: MD_ADCINF [7]: DCXO_NFCINF [6]: DCXO_CONNINF [5]: WACS3(C2K SW) [4]: DVFSINF (SPMINF) [3]: WACS0 (MD SW0) [2]: MD_DVFSINF [1]: C2kINF [0]: MDINF
23:20	ARBITER_SEL_CH5	**Selects the user of the priority_5** [15]: RESERVE [14]: RESERVE [13]: WACS_P2P [12]: WACS1 (MD SW1) [11]: WACS2 (AP SW) [10]: GPSINF [9]: STAUPD [8]: MD_ADCINF [7]: DCXO_NFCINF [6]: DCXO_CONNINF [5]: WACS3(C2K SW) [4]: DVFSINF (SPMINF) [3]: WACS0 (MD SW0) [2]: MD_DVFSINF [1]: C2kINF [0]: MDINF
19:16	ARBITER_SEL_CH4	**Selects the user of the priority_4** [15]: RESERVE [14]: RESERVE

Bit(s)	Name	Description
		[13]: WACS_P2P [12]: WACS1 (MD SW1) [11]: WACS2 (AP SW) [10]: GPSINF [9]: STAUPD [8]: MD_ADCINF [7]: DCXO_NFCINF [6]: DCXO_CONNINF [5]: WACS3(C2K SW) [4]: DVFSINF (SPMINF) [3]: WACS0 (MD SW0) [2]: MD_DVFSINF [1]: C2kINF [0]: MDINF
15:12	ARBITER_SEL_CH3	**Selects the user of the priority_3** [15]: RESERVE [14]: RESERVE [13]: WACS_P2P [12]: WACS1 (MD SW1) [11]: WACS2 (AP SW) [10]: GPSINF [9]: STAUPD [8]: MD_ADCINF [7]: DCXO_NFCINF [6]: DCXO_CONNINF [5]: WACS3(C2K SW) [4]: DVFSINF (SPMINF) [3]: WACS0 (MD SW0) [2]: MD_DVFSINF [1]: C2kINF [0]: MDINF
11:8	ARBITER_SEL_CH2	**Selects the user of the priority_2** [15]: RESERVE [14]: RESERVE [13]: WACS_P2P [12]: WACS1 (MD SW1) [11]: WACS2 (AP SW) [10]: GPSINF [9]: STAUPD [8]: MD_ADCINF [7]: DCXO_NFCINF [6]: DCXO_CONNINF [5]: WACS3(C2K SW) [4]: DVFSINF (SPMINF) [3]: WACS0 (MD SW0) [2]: MD_DVFSINF [1]: C2kINF [0]: MDINF
7:4	ARBITER_SEL_CH1	**Selects the user of the priority_1** [15]: RESERVE [14]: RESERVE [13]: WACS_P2P [12]: WACS1 (MD SW1) [11]: WACS2 (AP SW) [10]: GPSINF [9]: STAUPD [8]: MD_ADCINF [7]: DCXO_NFCINF [6]: DCXO_CONNINF [5]: WACS3(C2K SW) [4]: DVFSINF (SPMINF)

Bit(s)	Name	Description
		[3]: WACS0 (MD SW0) [2]: MD_DVFSINF [1]: C2kINF [0]: MDINF
3:0	ARBITER_SEL_CH0	**Selects the user of the priority_0** [15]: RESERVE [14]: RESERVE [13]: WACS_P2P [12]: WACS1 (MD SW1) [11]: WACS2 (AP SW) [10]: GPSINF [9]: STAUPD [8]: MD_ADCINF [7]: DCXO_NFCINF [6]: DCXO_CONNINF [5]: WACS3(C2K SW) [4]: DVFSINF (SPMINF) [3]: WACS0 (MD SW0) [2]: MD_DVFSINF [1]: C2kINF [0]: MDINF

1000D28C PRIORITY_USER_SEL_1 ARBITER_PRIORITY_USER_SEL_1 FEDCBA98

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARBITER_SEL_CH15				ARBITER_SEL_CH14				ARBITER_SEL_CH13				ARBITER_SEL_CH12			
Type	RW				RW				RW				RW			
Reset	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARBITER_SEL_CH11				ARBITER_SEL_CH10				ARBITER_SEL_CH9				ARBITER_SEL_CH8			
Type	RW				RW				RW				RW			
Reset	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0

Bit(s)	Name	Description
31:28	ARBITER_SEL_CH15	**Selects the user of the priority_15** [15]: RESERVE [14]: RESERVE [13]: WACS_P2P [12]: WACS1 (MD SW1) [11]: WACS2 (AP SW) [10]: GPSINF [9]: STAUPD [8]: MD_ADCINF [7]: DCXO_NFCINF [6]: DCXO_CONNINF [5]: WACS3(C2K SW) [4]: DVFSINF (SPMINF) [3]: WACS0 (MD SW0) [2]: MD_DVFSINF [1]: C2kINF [0]: MDINF
27:24	ARBITER_SEL_CH14	**Selects the user of the priority_14** [15]: RESERVE [14]: RESERVE [13]: WACS_P2P [12]: WACS1 (MD SW1) [11]: WACS2 (AP SW)

Bit(s)	Name	Description
		[10]: GPSINF [9]: STAUPD [8]: MD_ADCINF [7]: DCXO_NFCINF [6]: DCXO_CONNINF [5]: WACS3(C2K SW) [4]: DVFSINF (SPMINF) [3]: WACS0 (MD SW0) [2]: MD_DVFSINF [1]: C2kINF [0]: MDINF
23:20	ARBITER_SEL_CH13	**Selects the user of the priority_13** [15]: RESERVE [14]: RESERVE [13]: WACS_P2P [12]: WACS1 (MD SW1) [11]: WACS2 (AP SW) [10]: GPSINF [9]: STAUPD [8]: MD_ADCINF [7]: DCXO_NFCINF [6]: DCXO_CONNINF [5]: WACS3(C2K SW) [4]: DVFSINF (SPMINF) [3]: WACS0 (MD SW0) [2]: MD_DVFSINF [1]: C2kINF [0]: MDINF
19:16	ARBITER_SEL_CH12	**Selects the user of the priority_12** [15]: RESERVE [14]: RESERVE [13]: WACS_P2P [12]: WACS1 (MD SW1) [11]: WACS2 (AP SW) [10]: GPSINF [9]: STAUPD [8]: MD_ADCINF [7]: DCXO_NFCINF [6]: DCXO_CONNINF [5]: WACS3(C2K SW) [4]: DVFSINF (SPMINF) [3]: WACS0 (MD SW0) [2]: MD_DVFSINF [1]: C2kINF [0]: MDINF
15:12	ARBITER_SEL_CH11	**Selects the user of the priority_11** [15]: RESERVE [14]: RESERVE [13]: WACS_P2P [12]: WACS1 (MD SW1) [11]: WACS2 (AP SW) [10]: GPSINF [9]: STAUPD [8]: MD_ADCINF [7]: DCXO_NFCINF [6]: DCXO_CONNINF [5]: WACS3(C2K SW) [4]: DVFSINF (SPMINF) [3]: WACS0 (MD SW0) [2]: MD_DVFSINF [1]: C2kINF

Bit(s)	Name	Description
		[0]: MDINF
11:8	ARBITER_SEL_CH10	**Selects the user of the priority_10** [15]: RESERVE [14]: RESERVE [13]: WACS_P2P [12]: WACS1 (MD SW1) [11]: WACS2 (AP SW) [10]: GPSINF [9]: STAUPD [8]: MD_ADCINF [7]: DCXO_NFCINF [6]: DCXO_CONNINF [5]: WACS3(C2K SW) [4]: DVFSINF (SPMINF) [3]: WACS0 (MD SW0) [2]: MD_DVFSINF [1]: C2kINF [0]: MDINF
7:4	ARBITER_SEL_CH9	**Selects the user of the priority_9** [15]: RESERVE [14]: RESERVE [13]: WACS_P2P [12]: WACS1 (MD SW1) [11]: WACS2 (AP SW) [10]: GPSINF [9]: STAUPD [8]: MD_ADCINF [7]: DCXO_NFCINF [6]: DCXO_CONNINF [5]: WACS3(C2K SW) [4]: DVFSINF (SPMINF) [3]: WACS0 (MD SW0) [2]: MD_DVFSINF [1]: C2kINF [0]: MDINF
3:0	ARBITER_SEL_CH8	**Selects the user of the priority_8** [15]: RESERVE [14]: RESERVE [13]: WACS_P2P [12]: WACS1 (MD SW1) [11]: WACS2 (AP SW) [10]: GPSINF [9]: STAUPD [8]: MD_ADCINF [7]: DCXO_NFCINF [6]: DCXO_CONNINF [5]: WACS3(C2K SW) [4]: DVFSINF (SPMINF) [3]: WACS0 (MD SW0) [2]: MD_DVFSINF [1]: C2kINF [0]: MDINF

1000D290 **ARBITER_OUT_SEL_0** **ARBITER_OUT_SEL_0** **76543210**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARBITER_OUT_DCXO_				ARBITER_OUT_DCXO_				ARBITER_OUT_WACS3				ARBITER_OUT_SPMIN			

	NFCINF_SEL				CONNINF_SEL				_SEL				F_SEL			
Type	RW				RW				RW				RW			
Reset	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARBITER_OUT_WACSo_SEL				ARBITER_OUT_MD_DVFSINF_SEL				ARBITER_OUT_C2KINF_SEL				ARBITER_OUT_MDINF_SEL			
Type	RW				RW				RW				RW			
Reset	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:28	ARBITER_OUT_DCXO_NFCINF_SEL	**Selects which priority output as DCXO_NFCINF rdata** [15]: RESERVE [14]: RESERVE [13]: priority_13 [12]: priority_12 [11]: priority_11 [10]: priority_10 [9]: priority_9 [8]: priority_8 [7]: priority_7 [6]: priority_6 [5]: priority_5 [4]: priority_4 [3]: priority_3 [2]: priority_2 [1]: priority_1 [0]: priority_0
27:24	ARBITER_OUT_DCXO_CONNINF_SEL	**Selects which priority output as DCXO_CONNINF rdata** [15]: RESERVE [14]: RESERVE [13]: priority_13 [12]: priority_12 [11]: priority_11 [10]: priority_10 [9]: priority_9 [8]: priority_8 [7]: priority_7 [6]: priority_6 [5]: priority_5 [4]: priority_4 [3]: priority_3 [2]: priority_2 [1]: priority_1 [0]: priority_0
23:20	ARBITER_OUT_WACS3_SEL	**Selects which priority output as WACS3 rdata** [15]: RESERVE [14]: RESERVE [13]: priority_13 [12]: priority_12 [11]: priority_11 [10]: priority_10 [9]: priority_9 [8]: priority_8 [7]: priority_7 [6]: priority_6 [5]: priority_5 [4]: priority_4 [3]: priority_3 [2]: priority_2 [1]: priority_1 [0]: priority_0

Bit(s)	Name	Description
19:16	ARBITER_OUT_SPMINF_SEL	**Selects which priority output as SPMINF rdata** [15]: RESERVE [14]: RESERVE [13]: priority_13 [12]: priority_12 [11]: priority_11 [10]: priority_10 [9]: priority_9 [8]: priority_8 [7]: priority_7 [6]: priority_6 [5]: priority_5 [4]: priority_4 [3]: priority_3 [2]: priority_2 [1]: priority_1 [0]: priority_0
15:12	ARBITER_OUT_WACS0_SEL	**Selects which priority output as WACS0 rdata** [15]: RESERVE [14]: RESERVE [13]: priority_13 [12]: priority_12 [11]: priority_11 [10]: priority_10 [9]: priority_9 [8]: priority_8 [7]: priority_7 [6]: priority_6 [5]: priority_5 [4]: priority_4 [3]: priority_3 [2]: priority_2 [1]: priority_1 [0]: priority_0
11:8	ARBITER_OUT_MD_DVFSINF_SEL	**Selects which priority output as MD_DVSFINF rdata** [15]: RESERVE [14]: RESERVE [13]: priority_13 [12]: priority_12 [11]: priority_11 [10]: priority_10 [9]: priority_9 [8]: priority_8 [7]: priority_7 [6]: priority_6 [5]: priority_5 [4]: priority_4 [3]: priority_3 [2]: priority_2 [1]: priority_1 [0]: priority_0
7:4	ARBITER_OUT_C2KINF_SEL	**Selects which priority output as C2KINF rdata** [15]: RESERVE [14]: RESERVE [13]: priority_13 [12]: priority_12 [11]: priority_11 [10]: priority_10 [9]: priority_9 [8]: priority_8 [7]: priority_7

Bit(s)	Name	Description
		[6]: priority_6 [5]: priority_5 [4]: priority_4 [3]: priority_3 [2]: priority_2 [1]: priority_1 [0]: priority_0
3:0	ARBITER_OUT_MDINF_SEL	**Selects which priority output as MDINF rdata** [15]: RESERVE [14]: RESERVE [13]: priority_13 [12]: priority_12 [11]: priority_11 [10]: priority_10 [9]: priority_9 [8]: priority_8 [7]: priority_7 [6]: priority_6 [5]: priority_5 [4]: priority_4 [3]: priority_3 [2]: priority_2 [1]: priority_1 [0]: priority_0

1000D294 ARBITER_OUT_SEL_1 ARBITER_OUT_SEL_1 FEDCBA98

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARBITER_OUT_RESERVE2_SEL				ARBITER_OUT_RESERVE1_SEL				ARBITER_OUT_RESERVE0_SEL				ARBITER_OUT_WACS1_SEL			
Type	RW				RW				RW				RW			
Reset	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARBITER_OUT_WACS2_SEL				ARBITER_OUT_GPSINF_SEL				ARBITER_OUT_STAUPD_SEL				ARBITER_OUT_MD_ADCINF_SEL			
Type	RW				RW				RW				RW			
Reset	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0

Bit(s)	Name	Description
31:28	ARBITER_OUT_RESERVE2_SEL	**Reserved** [15]: RESERVE [14]: RESERVE [13]: priority_13 [12]: priority_12 [11]: priority_11 [10]: priority_10 [9]: priority_9 [8]: priority_8 [7]: priority_7 [6]: priority_6 [5]: priority_5 [4]: priority_4 [3]: priority_3 [2]: priority_2 [1]: priority_1 [0]: priority_0
27:24	ARBITER_OUT_RES	**RESERVED**

Bit(s)	Name	Description
	ERVE1_SEL	[15]: RESERVE [14]: RESERVE [13]: priority_13 [12]: priority_12 [11]: priority_11 [10]: priority_10 [9]: priority_9 [8]: priority_8 [7]: priority_7 [6]: priority_6 [5]: priority_5 [4]: priority_4 [3]: priority_3 [2]: priority_2 [1]: priority_1 [0]: priority_0
23:20	ARBITER_OUT_RESERVE0_SEL	**Selects which priority output as WACS_P2P rdata** [15]: RESERVE [14]: RESERVE [13]: priority_13 [12]: priority_12 [11]: priority_11 [10]: priority_10 [9]: priority_9 [8]: priority_8 [7]: priority_7 [6]: priority_6 [5]: priority_5 [4]: priority_4 [3]: priority_3 [2]: priority_2 [1]: priority_1 [0]: priority_0
19:16	ARBITER_OUT_WACS1_SEL	**Selects which priority output as WACS1 rdata** [15]: RESERVE [14]: RESERVE [13]: priority_13 [12]: priority_12 [11]: priority_11 [10]: priority_10 [9]: priority_9 [8]: priority_8 [7]: priority_7 [6]: priority_6 [5]: priority_5 [4]: priority_4 [3]: priority_3 [2]: priority_2 [1]: priority_1 [0]: priority_0
15:12	ARBITER_OUT_WACS2_SEL	**Selects which priority output as WACS2 rdata** [15]: RESERVE [14]: RESERVE [13]: priority_13 [12]: priority_12 [11]: priority_11 [10]: priority_10 [9]: priority_9 [8]: priority_8 [7]: priority_7 [6]: priority_6

Bit(s)	Name	Description
		[5]: priority_5 [4]: priority_4 [3]: priority_3 [2]: priority_2 [1]: priority_1 [0]: priority_0
11:8	ARBITER_OUT_GPSINF_SEL	**Selects which priority output as GPSINF rdata** [15]: RESERVE [14]: RESERVE [13]: priority_13 [12]: priority_12 [11]: priority_11 [10]: priority_10 [9]: priority_9 [8]: priority_8 [7]: priority_7 [6]: priority_6 [5]: priority_5 [4]: priority_4 [3]: priority_3 [2]: priority_2 [1]: priority_1 [0]: priority_0
7:4	ARBITER_OUT_STAUPD_SEL	**Selects which priority output as STAUPD rdata** [15]: RESERVE [14]: RESERVE [13]: priority_13 [12]: priority_12 [11]: priority_11 [10]: priority_10 [9]: priority_9 [8]: priority_8 [7]: priority_7 [6]: priority_6 [5]: priority_5 [4]: priority_4 [3]: priority_3 [2]: priority_2 [1]: priority_1 [0]: priority_0
3:0	ARBITER_OUT_MD_ADCINF_SEL	**Selects which priority output as MD_ADCINF rdata (co-clock)** [15]: RESERVE [14]: RESERVE [13]: priority_13 [12]: priority_12 [11]: priority_11 [10]: priority_10 [9]: priority_9 [8]: priority_8 [7]: priority_7 [6]: priority_6 [5]: priority_5 [4]: priority_4 [3]: priority_3 [2]: priority_2 [1]: priority_1 [0]: priority_0

1000D298 STARV_COUNTER_0 STARV_COUNTER_0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						STARV_COUNTER0_ENABLE	STARV_COUNTER0_TARGET									
Type						RW	RW									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	STARV_COUNTER0_ENABLE	**Enables the priority_0 starvation machenism** 0:Disable 1: Enable
9:0	STARV_COUNTER0_TARGET	**priority_0 stravation threshold** 1: One command pending (~1us) N: N command pednging (~Nus)

1000D29C STARV_COUNTER_1 STARV_COUNTER_1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						STARV_COUNTER1_ENABLE	STARV_COUNTER1_TARGET									
Type						RW	RW									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	STARV_COUNTER1_ENABLE	**Enables the priority_1 starvation machenism** 0: Disable 1: Enable
9:0	STARV_COUNTER1_TARGET	**priority_1 stravation threshold** 1: One command pending (~1us) N: N command pednging (~Nus)

1000D2A0 STARV_COUNTER_2 STARV_COUNTER_2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						STARV_COUNTER2_ENABLE	STARV_COUNTER2_TARGET									
Type						RW	RW									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	STARV_COUNTER2_ENABLE	**Enables the priority_2 starvation machenism** 0: Disable 1: Enable
9:0	STARV_COUNTER2_TARGET	**priority_2 stravation threshold** 1: One command pending (~1us) N: N command pednging (~Nus)

1000D2A4 STARV_COUNTER_3 STARV_COUNTER_3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						STARV_COUNTER3_ENABLE	STARV_COUNTER3_TARGET									
Type						RW	RW									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	STARV_COUNTER3_ENABLE	**Enables the priority_3 starvation machenism** 0: Disable 1: Enable
9:0	STARV_COUNTER3_TARGET	**priority_3 stravation threshold** 1: One command pending (~1us) N: N command pednging (~Nus)

1000D2A8 STARV_COUNTER_4 STARV_COUNTER_4 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						STARV_COUNTER4_ENABLE	STARV_COUNTER4_TARGET									
Type						RW	RW									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	STARV_COUNTER4_ENABLE	**Enables the priority_4 starvation machenism** 0: Disable 1: Enable
9:0	STARV_COUNTER4_TARGET	**priority_4 stravation threshold** 1: One command pending (~1us) N: N command pednging (~Nus)

1000D2AC STARV_COUN STARV_COUNTER_5 0000

TER_5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						STARV_COUNTER5_ENABLE	STARV_COUNTER5_TARGET									
Type						RW	RW									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	STARV_COUNTER5_ENABLE	**Enables the priority_4 starvation machenism** 0: Disable 1: Enable
9:0	STARV_COUNTER5_TARGET	**priority_5 stravation threshold** 1: One command pending (~1us) N: N command pednging (~Nus)

1000D2B0 STARV_COUNTER_6 STARV_COUNTER_6 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						STARV_COUNTER6_ENABLE	STARV_COUNTER6_TARGET									
Type						RW	RW									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	STARV_COUNTER6_ENABLE	**Enables the priority_6 starvation machenism** 0: Disable 1: Enable
9:0	STARV_COUNTER6_TARGET	**priority_6 stravation threshold** 1: One command pending (~1us) N: N command pednging (~Nus)

1000D2B4 STARV_COUNTER_7 STARV_COUNTER_7 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						STARV_COUNTER7_ENABLE	STARV_COUNTER7_TARGET									
Type						RW	RW									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
10	STARV_COUNTER7_ENABLE	**Enables the priority_7 starvation machenism** 0: Disable 1: Enable
9:0	STARV_COUNTER7_TARGET	**priority_7 stravation threshold** 1: One command pending (~1us) N: N command pednging (~Nus)

1000D2B8 STARV_COUNTER_8 STARV_COUNTER_8 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						STARV_COUNTER8_ENABLE	STARV_COUNTER8_TARGET									
Type						RW	RW									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	STARV_COUNTER8_ENABLE	**Enables the priority_8 starvation machenism** 0: Disable 1: Enable
9:0	STARV_COUNTER8_TARGET	**priority_8 stravation threshold** 1: One command pending (~1us) N: N command pednging (~Nus)

1000D2BC STARV_COUNTER_9 STARV_COUNTER_9 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						STARV_COUNTER9_ENABLE	STARV_COUNTER9_TARGET									
Type						RW	RW									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	STARV_COUNTER9_ENABLE	**Enables the priority_9 starvation machenism** 0: Disable 1: Enable
9:0	STARV_COUNTER9_TARGET	**priority_9 stravation threshold** 1: One command pending (~1us) N: N command pednging (~Nus)

1000D2C0 STARV_COUN STARV_COUNTER_10 0000

TER_10

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						STARV_COUNTER10_ENABLE	STARV_COUNTER10_TARGET									
Type						RW	RW									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	STARV_COUNTER10_ENABLE	**Enables the priority_10 starvation machenism** 0: Disable 1: Enable
9:0	STARV_COUNTER10_TARGET	**priority_10 stravation threshold** 1: One command pending (~1us) N: N command pednging (~Nus)

1000D2C4 STARV_COUNTER_11 STARV_COUNTER_11 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						STARV_COUNTER11_ENABLE	STARV_COUNTER11_TARGET									
Type						RW	RW									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	STARV_COUNTER11_ENABLE	**Enables the priority_11 starvation machenism** 0: Disable 1: Enable
9:0	STARV_COUNTER11_TARGET	**priority_11 stravation threshold** 1: One command pending (~1us) N: N command pednging (~Nus)

1000D2C8 STARV_COUNTER_12 STARV_COUNTER_12 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						STARV_COUNTER12_ENABLE	STARV_COUNTER12_TARGET									
Type						RW	RW									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
10	STARV_COUNTER12_ENABLE	**Enables the priority_12 starvation machenism** 0: Disable 1: Enable
9:0	STARV_COUNTER12_TARGET	**priority_12 stravation threshold** 1: One command pending (~1us) N: N command pednging (~Nus)

1000D2CC STARV_COUNTER_13 STARV_COUNTER_13 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						STARV_COUNTER13_ENABLE	STARV_COUNTER13_TARGET									
Type						RW	RW									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	STARV_COUNTER13_ENABLE	**Enables the priority_13 starvation machenism** 0: Disable 1: Enable
9:0	STARV_COUNTER13_TARGET	**priority_13 stravation threshold** 1: One command pending (~1us) N: N command pednging (~Nus)

1000D2D0 STARV_COUNTER_14 STARV_COUNTER_14 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						STARV_COUNTER14_ENABLE	STARV_COUNTER14_TARGET									
Type						RW	RW									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	STARV_COUNTER14_ENABLE	**Enables the priority_14 starvation machenism** 0: Disable 1: Enable
9:0	STARV_COUNTER14_TARGET	**priority_14 stravation threshold** 1: One command pending (~1us) N: N command pednging (~Nus)

1000D2D4 STARV_COUN STARV_COUNTER_15 0000

TER_15

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						STARV_COUNTER15_ENABLE	STARV_COUNTER15_TARGET									
Type						RW	RW									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	STARV_COUNTER15_ENABLE	**Enables the priority_15 starvation machenism** 0: Disable 1: Enable
9:0	STARV_COUNTER15_TARGET	**priority_15 stravation threshold** 1: One command pending (~1us) N: N command pednging (~Nus)

1000D2D8 STARV_COUNTER_0_STATUS STARV_COUNTER_0_STATUS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													STARV_COUNTER0[9:6]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STARV_COUNTER0[5:0]						STARV_COUNTER0_GATED									
Type	RU						RU									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:10	STARV_COUNTER0	**The priority_0 stravation counted number**
9:0	STARV_COUNTER0_GATED	**The priority_0 stravation counted number when any other priority reaches the starvation treshold**

1000D2DC STARV_COUNTER_1_STATUS STARV_COUNTER_1_STATUS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													STARV_COUNTER1[9:6]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STARV_COUNTER1[5:0]						STARV_COUNTER1_GATED									
Type	RU						RU									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:10	STARV_COUNTER1	riority_1 stravation counted number

Bit(s)	Name	Description
9:0	STARV_COUNTER1_GATED	priority_1 stravation counted number when any other priority reaches the starvation treshold

1000D2E0 STARV_COUNTER_2_STATUS STARV_COUNTER_2_STATUS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													STARV_COUNTER2[9:6]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STARV_COUNTER2[5:0]						STARV_COUNTER2_GATED									
Type	RU						RU									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:10	STARV_COUNTER2	priority_2 stravation counted number
9:0	STARV_COUNTER2_GATED	priority_2 stravation counted number when any other priority reaches the starvation treshold

1000D2E4 STARV_COUNTER_3_STATUS STARV_COUNTER_3_STATUS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													STARV_COUNTER3[9:6]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STARV_COUNTER3[5:0]						STARV_COUNTER3_GATED									
Type	RU						RU									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:10	STARV_COUNTER3	priority_3 stravation counted number
9:0	STARV_COUNTER3_GATED	priority_3 stravation counted number when any other priority reaches the starvation treshold

1000D2E8 STARV_COUNTER_4_STATUS STARV_COUNTER_4_STATUS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													STARV_COUNTER4[9:6]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	STARV_COUNTER4[5:0]						STARV_COUNTER4_GATED									
Type	RU						RU									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:10	STARV_COUNTER4	priority_4 stravation counted number
9:0	STARV_COUNTER4_GATED	priority_4 stravation counted number when any other priority reaches the starvation treshold

1000D2EC STARV_COUNTER_5_STATUS STARV_COUNTER_5_STATUS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													STARV_COUNTER5[9:6]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STARV_COUNTER5[5:0]						STARV_COUNTER5_GATED									
Type	RU						RU									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:10	STARV_COUNTER5	priority_5 stravation counted number
9:0	STARV_COUNTER5_GATED	priority_5 stravation counted number when any other priority reaches the starvation treshold

1000D2F0 STARV_COUNTER_6_STATUS STARV_COUNTER_6_STATUS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													STARV_COUNTER6[9:6]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STARV_COUNTER6[5:0]						STARV_COUNTER6_GATED									
Type	RU						RU									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:10	STARV_COUNTER6	priority_6 stravation counted number
9:0	STARV_COUNTER6_GATED	priority_6 stravation counted number when any other priority reaches the starvation treshold

1000D2F4 STARV_COUNTER_7_STATUS STARV_COUNTER_7_STATUS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													STARV_COUNTER7[9:6]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STARV_COUNTER7[5:0]						STARV_COUNTER7_GATED									
Type	RU						RU									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:10	STARV_COUNTER7	priority_7 stravation counted number
9:0	STARV_COUNTER7_GATED	priority_7 stravation counted number when any other priority reaches the starvation treshold

1000D2F8 STARV_COUNTER_8_STATUS STARV_COUNTER_8_STATUS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													STARV_COUNTER8[9:6]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STARV_COUNTER8[5:0]						STARV_COUNTER8_GATED									
Type	RU						RU									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:10	STARV_COUNTER8	priority_8 stravation counted number
9:0	STARV_COUNTER8_GATED	priority_8 stravation counted number when any other priority reaches the starvation treshold

1000D2FC STARV_COUNTER_9_STATUS STARV_COUNTER_9_STATUS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													STARV_COUNTER9[9:6]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STARV_COUNTER9[5:0]						STARV_COUNTER9_GATED									
Type	RU						RU									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:10	STARV_COUNTER9	priority_9 stravation counted number
9:0	STARV_COUNTER9_GATED	priority_9 stravation counted number when any other priority reaches the starvation treshold

1000D300 STARV_COUNTER_10_STATUS — STARV_COUNTER_10_STATUS — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													STARV_COUNTER10[9:6]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STARV_COUNTER10[5:0]						STARV_COUNTER10_GATED									
Type	RU						RU									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:10	STARV_COUNTER10	priority_10 stravation counted number
9:0	STARV_COUNTER10_GATED	priority_10 stravation counted number when any other priority reaches the starvation treshold

1000D304 STARV_COUNTER_11_STATUS — STARV_COUNTER_11_STATUS — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													STARV_COUNTER11[9:6]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STARV_COUNTER11[5:0]						STARV_COUNTER11_GATED									
Type	RU						RU									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:10	STARV_COUNTER11	priority_11 stravation counted number
9:0	STARV_COUNTER11_GATED	priority_11 stravation counted number when any other priority reaches the starvation treshold

1000D308 STARV_COUNTER_12_STATUS — STARV_COUNTER_12_STATUS — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													STARV_COUNTER12[9:6]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STARV_COUNTER12[5:0]						STARV_COUNTER12_GATED									
Type	RU						RU									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
19:10	STARV_COUNTER12	priority_12 stravation counted number
9:0	STARV_COUNTER12_GATED	priority_12 stravation counted number when any other priority reaches the starvation treshold

1000D30C STARV_COUNTER_13_STATUS STARV_COUNTER_13_STATUS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													STARV_COUNTER13[9:6]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STARV_COUNTER13[5:0]						STARV_COUNTER13_GATED									
Type	RU						RU									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:10	STARV_COUNTER13	priority_13 stravation counted number
9:0	STARV_COUNTER13_GATED	priority_13 stravation counted number when any other priority reaches the starvation treshold

1000D310 STARV_COUNTER_14_STATUS STARV_COUNTER_14_STATUS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													STARV_COUNTER14[9:6]			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STARV_COUNTER14[5:0]						STARV_COUNTER14_GATED									
Type	RU						RU									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:10	STARV_COUNTER14	priority_14 stravation counted number
9:0	STARV_COUNTER14_GATED	priority_14 stravation counted number when any other priority reaches the starvation treshold

1000D314 STARV_COUNTER_15_STATUS STARV_COUNTER_15_STATUS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													STARV_COUNTER15[9:6]			
Type													RU			

Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STARV_COUNTER15[5:0]						STARV_COUNTER15_GATED									
Type	RU						RU									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:10	STARV_COUNTER15	priority_15 stravation counted number
9:0	STARV_COUNTER15 _GATED	priority_15 stravation counted number when any other priority reaches the starvation treshold

1000D318 STARV_COUNTER_CLR STARV_COUNTER_CLR 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STARV_COUNTER15_CLR	STARV_COUNTER14_CLR	STARV_COUNTER13_CLR	STARV_COUNTER12_CLR	STARV_COUNTER11_CLR	STARV_COUNTER10_CLR	STARV_COUNTER9_CLR	STARV_COUNTER8_CLR	STARV_COUNTER7_CLR	STARV_COUNTER6_CLR	STARV_COUNTER5_CLR	STARV_COUNTER4_CLR	STARV_COUNTER3_CLR	STARV_COUNTER2_CLR	STARV_COUNTER1_CLR	STARV_COUNTER0_CLR
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	STARV_COUNTER15 _CLR	Clears the priority_15 starvation counter
14	STARV_COUNTER14 _CLR	Clears the priority_14 starvation counter
13	STARV_COUNTER13 _CLR	Clears the priority_13 starvation counter
12	STARV_COUNTER12 _CLR	Clears the priority_12 starvation counter
11	STARV_COUNTER11_ CLR	Clears the priority_11 starvation counter
10	STARV_COUNTER10 _CLR	Clears the priority_10 starvation counter
9	STARV_COUNTER9_ CLR	Clears the priority_9 starvation counter
8	STARV_COUNTER8_ CLR	Clears the priority_8 starvation counter
7	STARV_COUNTER7_ CLR	Clears the priority_7 starvation counter
6	STARV_COUNTER6_ CLR	Clears the priority_6 starvation counter
5	STARV_COUNTER5_ CLR	Clears the priority_5 starvation counter
4	STARV_COUNTER4_ CLR	Clears the priority_4 starvation counter
3	STARV_COUNTER3_ CLR	Clears the priority_3 starvation counter
2	STARV_COUNTER2_ CLR	Clears the priority_2 starvation counter
1	STARV_COUNTER1_	Clears the priority_1 starvation counter

Bit(s)	Name	Description
	CLR	
0	STARV_COUNTER0_CLR	Clears the priority_0 starvation counter

1000D31C STARV_PRIO_STATUS STARV_PRIO_STATUS 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AG_ARB_HPRIO_STARV													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	AG_ARB_HPRIO_STARV	Recordes the starvation priority

1000D320 DEBUG_STATUS DEBUG_STATUS 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DEBUG_INIT		DEBUG_COUNTER_MAX					
Type									RW		RU					
Reset									0		0	0	0	0	0	0

Bit(s)	Name	Description
7	DEBUG_INIT	Initializes the debug counter
5:0	DEBUG_COUNTER_MAX	Records the debug counter

1000D324 DEBUG_SQUENCE_0 DEBUG_SQUENCE_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_SQ7				DEBUG_SQ6				DEBUG_SQ5				DEBUG_SQ4			
Type	RU				RU				RU				RU			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_SQ3				DEBUG_SQ2				DEBUG_SQ1				DEBUG_SQ0			
Type	RU				RU				RU				RU			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	DEBUG_SQ7	Past command sequence_7
27:24	DEBUG_SQ6	Past command sequence_6
23:20	DEBUG_SQ5	Past command sequence_5
19:16	DEBUG_SQ4	Past command sequence_4

Bit(s)	Name	Description
15:12	DEBUG_SQ3	Past command sequence_3
11:8	DEBUG_SQ2	Past command sequence_2
7:4	DEBUG_SQ1	Past command sequence_1
3:0	DEBUG_SQ0	Past command sequence_0 (the oldest)

1000D328 DEBUG_SQUENCE_1 DEBUG_SQUENCE_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_SQ15				DEBUG_SQ14				DEBUG_SQ13				DEBUG_SQ12			
Type	RU				RU				RU				RU			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_SQ11				DEBUG_SQ10				DEBUG_SQ9				DEBUG_SQ8			
Type	RU				RU				RU				RU			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	DEBUG_SQ15	Past command sequence_15
27:24	DEBUG_SQ14	Past command sequence_14
23:20	DEBUG_SQ13	Past command sequence_13
19:16	DEBUG_SQ12	Past command sequence_12
15:12	DEBUG_SQ11	Past command sequence_11
11:8	DEBUG_SQ10	Past command sequence_10
7:4	DEBUG_SQ9	Past command sequence_9
3:0	DEBUG_SQ8	Past command sequence_8

1000D32C DEBUG_SQUENCE_2 DEBUG_SQUENCE_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_SQ23				DEBUG_SQ22				DEBUG_SQ21				DEBUG_SQ20			
Type	RU				RU				RU				RU			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_SQ19				DEBUG_SQ18				DEBUG_SQ17				DEBUG_SQ16			
Type	RU				RU				RU				RU			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	DEBUG_SQ23	Past command sequence_23
27:24	DEBUG_SQ22	Past command sequence_22
23:20	DEBUG_SQ21	Past command sequence_21
19:16	DEBUG_SQ20	Past command sequence_20
15:12	DEBUG_SQ19	Past command sequence_19
11:8	DEBUG_SQ18	Past command sequence_18
7:4	DEBUG_SQ17	Past command sequence_17
3:0	DEBUG_SQ16	Past command sequence_16

1000D330 DEBUG_SQUENCE_3 DEBUG_SQUENCE_3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_SQ31				DEBUG_SQ30				DEBUG_SQ29				DEBUG_SQ28			
Type	RU				RU				RU				RU			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_SQ27				DEBUG_SQ26				DEBUG_SQ25				DEBUG_SQ24			
Type	RU				RU				RU				RU			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	DEBUG_SQ31	Past command sequence_31
27:24	DEBUG_SQ30	Past command sequence_30
23:20	DEBUG_SQ29	Past command sequence_29
19:16	DEBUG_SQ28	Past command sequence_28
15:12	DEBUG_SQ27	Past command sequence_27
11:8	DEBUG_SQ26	Past command sequence_26
7:4	DEBUG_SQ25	Past command sequence_25
3:0	DEBUG_SQ24	Past command sequence_24

1000D334 DEBUG_SQUENCE_4 DEBUG_SQUENCE_4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_SQ39				DEBUG_SQ38				DEBUG_SQ37				DEBUG_SQ36			
Type	RU				RU				RU				RU			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_SQ35				DEBUG_SQ34				DEBUG_SQ33				DEBUG_SQ32			
Type	RU				RU				RU				RU			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	DEBUG_SQ39	Past command sequence_39
27:24	DEBUG_SQ38	Past command sequence_38
23:20	DEBUG_SQ37	Past command sequence_37
19:16	DEBUG_SQ36	Past command sequence_36
15:12	DEBUG_SQ35	Past command sequence_35
11:8	DEBUG_SQ34	Past command sequence_34
7:4	DEBUG_SQ33	Past command sequence_33
3:0	DEBUG_SQ32	Past command sequence_32

1000D338 DEBUG_SQUENCE_5 DEBUG_SQUENCE_5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_SQ47				DEBUG_SQ46				DEBUG_SQ45				DEBUG_SQ44			
Type	RU				RU				RU				RU			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_SQ43				DEBUG_SQ42				DEBUG_SQ41				DEBUG_SQ40			
Type	RU				RU				RU				RU			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	DEBUG_SQ47	Past command sequence_47
27:24	DEBUG_SQ46	Past command sequence_46
23:20	DEBUG_SQ45	Past command sequence_45
19:16	DEBUG_SQ44	Past command sequence_44
15:12	DEBUG_SQ43	Past command sequence_43
11:8	DEBUG_SQ42	Past command sequence_42
7:4	DEBUG_SQ41	Past command sequence_41
3:0	DEBUG_SQ40	Past command sequence_40

1000D33C DEBUG_SQUENCE_6 DEBUG_SQUENCE_6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_SQ55				DEBUG_SQ54				DEBUG_SQ53				DEBUG_SQ52			
Type	RU				RU				RU				RU			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_SQ51				DEBUG_SQ50				DEBUG_SQ49				DEBUG_SQ48			
Type	RU				RU				RU				RU			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	DEBUG_SQ55	Past command sequence_55 (latest)
27:24	DEBUG_SQ54	Past command sequence_54
23:20	DEBUG_SQ53	Past command sequence_53
19:16	DEBUG_SQ52	Past command sequence_52
15:12	DEBUG_SQ51	Past command sequence_51
11:8	DEBUG_SQ50	Past command sequence_50
7:4	DEBUG_SQ49	Past command sequence_49
3:0	DEBUG_SQ48	Past command sequence_48

Module name: PMIC_WRAP_P2P Base address: (+100AB000h)

Address	Name	Width	Register Function
100AB200	WACS_P2P_EN	8	Wrapper Access (#0) Enable
100AB204	INIT_DONE_P2P	8	Initialization Done
100AB208	WACS_P2P_CMD	32	Wrapper Access (#0) Command

100AB20C	WACS_P2P_RDATA	32	Wrapper Access (#0) Read Data
100AB210	WACS_P2P_VLDCLR	8	Wapper Access (#0) Valid Clear

100AB200 WACS_P2P_EN Wrapper Access (#0) Enable 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WACS_P2P_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	WACS_P2P_EN	**Enables wrapper access** Set to disable will reset the FSM. 0: Disable 1: Enable

100AB204 INIT_DONE_P2P Initialization Done 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INIT_DONE_P2P
Type																RW
Reset																0

Bit(s)	Name	Description
0	INIT_DONE_P2P	**Indicates initialization is finished.** During SPI transactions, if this bit is detected low, then current transaction may fail, which requires re-do or debugging. 0: Initialization is not yet finished. 1: Initialization is finished.

100AB208 WACS_P2P_CMD Wrapper Access (#0) Command 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WACS_P2P_WRITE	WACS_P2P_ADR														
Type	RW	RW														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WACS_P2P_WDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	WACS_P2P_WRITE	**Wrapper access: Read/write direction** 0: Read 1: Write
30:16	WACS_P2P_ADR	**Wrapper access: Address[15:1]**
15:0	WACS_P2P_WDATA	**Wrapper access: Write data[15:0]**

100AB20C WACS_P2P_RDATA Wrapper Access (#0) Read Data 80500000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WACS_P2P_FIFO_FREECNT				WACS_P2P_FIFO_FILLCNT					SYS_IDLE_P2P	INIT_DONE_P2P	SYNC_IDLE_P2P	WACS_P2P_REQ	WACS_P2P_FSM		
Type	RU				RU					RU	RU	RU	RU	RU		
Reset	1	0	0	0	0	0	0	0		1	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WACS_P2P_RDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	WACS_P2P_FIFO_FREECNT	**Records the number of data can be filled into FIFO**
27:24	WACS_P2P_FIFO_FILLCNT	**Records the number of data filled into FIFO**
22	SYS_IDLE_P2P	**PMIC_WRAP busy status indicator:** 1. WACS 0/1/2 idle 2. no arbitor request 3, no spi_wrap to mux request 4. no waiting read data 5. spi_man is idle 6. spI_sync is idle 0: PMIC_WRAP is busy 1: PMIC_WRAP is IDLE
21	INIT_DONE_P2P	**Indicates initialization is finished.** During SPI transactions, if this bit is detected low, then current transaction may fail, which requires re-do or debugging. (This is equivalent to INIT_DONE) 0: Initialization is not yet finished 1: Initialization is finished.
20	SYNC_IDLE_P2P	**SYNC module busy status.** It is used to judge if the request has reached SYNC module. 0: SYNC module is busy 1: SYNC module is IDLE
19	WACS_P2P_REQ	**Wrapper access request indicator.** 0: No WACS request is awaiting grant. 1: One WACS Request is still awaiting grant.
18:16	WACS_P2P_FSM	**Current WACS FSM states.** 0x0: IDLE 0x2: REQ. Request in process 0x4: WFDLE. Wait for read data 0x6: WFVLDCLR. Wait for valid flag clearing

Bit(s)	Name	Description
		Others: Reserved
15:0	WACS_P2P_RDATA	**Wrapper Access: read data.** SW must check if valid flag equals to 1 before using this read data.

100AB210 WACS_P2P_VLDCLR Wapper Access (#0) Valid Clear 00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WACS_P2P_VLDCLR
Type																WO
Reset																0

Bit(s)	Name	Description
0	WACS_P2P_VLDCLR	Write 1 to clear valid flag.

3 Peripherals

3.1 Pericfg Controller

Module name: PERICFG Base address: (+10003000h)

Address	Name	Width	Register Function
10003050	PERI_GLOBALCON_DCMCTL	32	Peripheral DCM Control Register
1000305C	PERI_GLOBALCON_CKSEL	32	
10003200	PERIAXI_BUS_CTL1	32	Peripheral AXI Bus Control 1
10003204	PERIAXI_BUS_CTL2	32	Peripheral AXI Bus Control 2
10003208	PERIAXI_BUS_CTL3	32	Peripheral AXI Bus Control 3
1000320C	PERIAXI_SI0_CTL	32	Peripheral AXI SI0 Control
10003210	PERIAXI_SI1_CTL	32	Peripheral AXI SI1 Control
10003214	PERIAXI_MI_STA	32	Peripheral AXI MI Status
10003218	PERIAXI_BUS_CTL4	32	Peripheral AXI Bus Control 4
1000321C	PERIAXI_BUS_CTL5	32	Peripheral AXI Bus Control 5
10003300	PERIAXI_AHB_LMT_CON1	32	Peripheral AHB Bus 0 Bandwidth Limiter
10003304	PERIAXI_AHB_LMT_CON2	32	Peripheral AHB Bus 0 Bandwidth Limiter
10003308	PERIAXI_AHB_LMT_CON3	32	Peripheral AHB Bus 1 Bandwidth Limiter
1000330C	PERIAXI_AHB_LMT_CON4	32	Peripheral AHB Bus 1 Bandwidth Limiter
10003310	PERIAXI_AHB_LMT_CON5	32	Peripheral AHB Bus 2 Bandwidth Limiter
10003314	PERIAXI_AHB_LMT_CON6	32	Peripheral AHB Bus 2 Bandwidth Limiter
10003318	PERIAXI_AHB_LMT_CON7	32	Peripheral AHB Bus 3 Bandwidth Limiter
1000331C	PERIAXI_AHB_LMT_CON8	32	Peripheral AHB Bus 3 Bandwidth Limiter
10003320	PERIAXI_AXI_LMT_CON1	32	Peripheral AXI MST0 Bandwidth Limiter
10003324	PERIAXI_AXI_LMT_CON2	32	Peripheral AXI MST1 Bandwidth Limiter
10003328	PERIAXI_AXI_LMT_CON3	32	Peripheral AXI MST2 Bandwidth Limiter
1000332C	PERIAXI_AXI_LMT_CON4	32	Peripheral AP DMA Bandwidth Limiter
10003330	PERIAXI_AXI_LMT_CON5	32	Peripheral AXI MSDC0 Bandwidth Limiter
10003334	PERIAXI_AXI_LMT_CON6	32	Peripheral AXI USB30 Bandwidth Limiter
10003400	PERI_USB_WAKEUP_DEC_CON0	32	Peripheral USB Wakeup Control 0
10003404	PERI_USB_WAKEU	32	Peripheral USB Wakeup Control 1

Address	Name	Width	Register Function
	P_DEC_CON1		
10003408	PERI_USB_WAKEUP_DEC_CON2	32	Peripheral USB Wakeup Control 2
10003410	PERI_I2C_MODE_ENABLE	32	Peripheral I2C Mode Enable
10003420	PERI_DVFS0_TX_APB_ASYNC_STA	32	Peri DVFS0 TX APB Async Status
10003424	PERI_DVFS1_TX_APB_ASYNC_STA	32	Peri DVFS1 TX APB Async Status

10003050 PERI_GLOBALCON_DCMCTL **Peripheral DCM Control Register** **000000F2**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																dcm_idle_bypass_en
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcm_idle_bypass_en								PERIAHB_BUS_SLPREQ						AXI_CLOCK_GATED_EN	
Type	RW								RW						RW	
Reset	0	0	0	0	0	0	0	0	1	1	1	1			1	

Bit(s)	Mnemonic	Name	Description
16:8	dcm_idle_bypass_en	dcm_idle_bypas s_en	
7:4	PERIAHB_BUS_SLPREQ	PERIAHB_BUS_SLPREQ	**No use** 0: No use
1	AXI_CLOCK_GATED_EN	AXI_CLOCK_GATED_EN	**AXI clock gated** 0: Disable 1: Enable

1000305C PERI_GLOBALCON_CKSEL **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																haxi_peribus_sel
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
0	**haxi_peribus_s el**	haxi_peribus_s el	

10003200 PERIAXI_BUS_CTL1 **Peripheral AXI Bus Control 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AHB0_SHARE_EN				AHB1_SHARE_EN				AHB0_ULTRA				AHB1_ULTRA			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AHB2_ULTRA				AHB0_PRE_ULTRA				AHB1_PRE_ULTRA				AHB2_PRE_ULTRA			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**AHB0_SHARE_EN**	AHB0_SHARE_EN	**Enables AHB bus 0 share attribute** Bit 0: Enable ICUSB share attribute when set to 1'b1 Bit 1: Enable AUDIO share attribute when set to 1'b1 Bit 2: Enable MSDC3 share attribute when set to 1'b1 Bit 3: Enable USB20 share attribute when set to 1'b1
27:24	**AHB1_SHARE_EN**	AHB1_SHARE_EN	**Enables AHB bus 1 share attribute** Bit 0: Enable PWM share attribute when set to 1'b1 Bit 1: Enable MSDC1 share attribute when set to 1'b1 Bit 2: Enable MSDC2 share attribute when set to 1'b1 Bit 3: Enable SPI share attribute when set to 1'b1
23:20	**AHB0_ULTRA**	AHB0_ULTRA	**AHB bus 0 ULTRA** Bit 0: IC-USB ULTRA Bit 1: AUDIO ULTRA Bit 2: MSDC3 ULTRA Bit 3: USB20 ULTRA
19:16		AHB1_ULTRA	**AHB bus 1 ULTRA** Bit 0: PWM ULTRA Bit 1: MSDC1 ULTRA Bit 2: MSDC2 ULTRA Bit 3: SPI ULTRA
15:12		AHB2_ULTRA	**AHB bus 2 ULTRA** Bit 0: SPI1 ULTRA Bit 1: SPM ULTRA Bit 2: MD32 ULTRA Bit 3: THERM ULTRA
11:8		AHB0_PRE_ULTRA	**AHB bus 0 PER_ULTRA** Bit 0: IC-USB PER_ULTRA Bit 1: AUDIO PER_ULTRA Bit 2: MSDC3 PER_ULTRA Bit 3: USB20 PER_ULTRA
7:4		AHB1_PRE_ULTRA	**AHB bus 1 PER_ULTRA** Bit 0: PWM PER_ULTRA Bit 1: MSDC1 PER_ULTRA Bit 2: MSDC2 PER_ULTRA Bit 3: SPI PER_ULTRA
3:0		AHB2_PRE_ULTRA	**AHB bu s2 PER_ULTRA** Bit 0: SP1 PER_ULTRA

Bit(s)	Mnemonic	Name	Description
			Bit 1: SPM PER_ULTRA Bit 2: MD32 PER_ULTRA Bit 3: THERM PER_ULTRA

10003204 PERIAXI_BUS_CTL2 **Peripheral AXI Bus Control 2** **10224FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AHB2_SHARE_EN								AHB0_READ_AHEAD_BW	AHB0_FIFO_THRESHOLD			AHB1_READ_AHEAD_BW	AHB1_FIFO_THRESHOLD		
Type	RW								RW	RW			RW	RW		
Reset	0	0	0	1					0	0	1	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AHB2_READ_AHEAD_BW	AHB2_FIFO_THRESHOLD			AHB_SECURE_EN				AHB_BUFFER_EN				AHB_MERGE_EN			
Type	RW	RW			RW				RW				RW			
Reset	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:28	**AHB2_SHARE_EN**	AHB2_SHARE_EN	**Enables AHB bus 2 share attribute** Bit 0: Enable SPI1 share attribute when set to 1'b1 Bit 1: Enable SPM share attribute when set to 1'b1 Bit 2: Enable MD32 share attribute when set to 1'b1 Bit 3: Enable THERM share attribute when set to 1'b1
23		AHB0_READ_AHEAD_BW	**Read transaction can pass through bufferable write trnasaction for AHB2AXI bridge 0.** 0: Disable 1: Enable
22:20		AHB0_FIFO_THRESHOLD	**Launch AXI side awvalid depending on how many write data are received at AHB side** For AHB2AXI bridge 0. 000: First command 001: 1/4 burst length 010: 1/2 burst length 011: 3/4 burst length 100: Full burst length
19		AHB1_READ_AHEAD_BW	**Read trnasaction can pass through bufferable write trnasaction for AHB2AXI bridge 1** 0: Disable 1: Enable
18:16		AHB1_FIFO_THRESHOLD	**Launch AXI side awvalid depending on how many write data are received at AHB side. For AHB2AXI bridge 1** 000: First command 001: 1/4 burst length 010: 1/2 burst length 011: 3/4 burst length 100: Full burst length
15		AHB2_READ_AHEAD_BW	**Read transaction can pass through bufferable write trnasaction for AHB2AXI bridge 2**

Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable
14:12		AHB2_FIFO_THRESHOLD	**Launch AXI side awvalid depending on how many write data are received at AHB side** For AHB2AXI bridge 2. 000: First command 001: 1/4 burst length 010: 1/2 burst length 011: 3/4 burst length 100: Full burst length
11:8	**AHB_SECURE_EN**	AHB_SECURE_EN	**Enables AHB2AXI secure attribute**
7:4	**AHB_BUFFER_EN**	AHB_BUFFER_EN	**Enables AHB2AXI buffer attribute**
3:0	**AHB_MERGE_EN**	AHB_MERGE_EN	**Enables AHB2AXI merge attribute**

10003208 PERIAXI_BUS_CTL3 **Peripheral AXI Bus Control 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AHB3_CACHE				AHB0_CACHE				AHB1_CACHE				AHB2_CACHE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AHB3_IOMMU				AHB0_IOMMU				AHB1_IOMMU				AHB2_IOMMU			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**AHB3_CACHE**	AHB3_CACHE	
27:24	**AHB0_CACHE**	AHB0_CACHE	**AHB bus 0 CACHE** Bit 0: IC-USB CACHE Bit 1: AUDIO CACHE Bit 2: MSDC3 CACHE Bit 3: USB20 CACHE
23:20	**AHB1_CACHE**	AHB1_CACHE	**AHB bus 1 CACHE** Bit 0: PWM CACHE Bit 1: MSDC1 CACHE Bit 2: MSDC2 CACHE Bit 3: SPI CACHE
19:16	**AHB2_CACHE**	AHB2_CACHE	**AHB bus 2 CACHE** Bit 0: DBG_I2C CACHE Bit 1: SPM CACHE Bit 2: MD32 CACHE Bit 3: THERM CACHE
15:12	**AHB3_IOMMU**	AHB3_IOMMU	
11:8	**AHB0_IOMMU**	AHB0_IOMMU	**AHB bus 0 IOMMU** Bit 0: IC-USB IOMMU Bit 1: AUDIO IOMMU Bit 2: MSDC3 IOMMU Bit 3: USB20 IOMMU
7:4	**AHB1_IOMMU**	AHB1_IOMMU	**AHB bus 1 IOMMU** Bit 0: PWM IOMMU Bit 1: MSDC1 IOMMU Bit 2: MSDC2 IOMMU

Bit(s)	Mnemonic	Name	Description
3:0	**AHB2_IOMMU**	AHB2_IOMMU	Bit 3: SPI IOMMU **AHB bus 2 IOMMU** Bit 0: DBG_I2C IOMMU Bit 1: SPM IOMMU Bit 2: MD32 IOMMU Bit 3: THERM IOMMU

1000320C PERIAXI_SI0_CTL **Peripheral AXI SIo Control** **00000300**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PERIAXI_CG_DISABLE							PERIAXI_SIo_WR_OT_BUSY	PERIAXI_SIo_RD_OT_BUSY	PERIAXI_SIo_DFSLV_SET_RID_MISS	PERIAXI_SIo_DFSLV_SET_BID_MISS	PERIAXI_SIo_DFSLV_SET_WIRQ	PERIAXI_SIo_DFSLV_SET_RIRQ	PERIAXI_R_CHNL_SEL		
Type	RW							RO	RO	RO	RO	RO	RO	RO		
Reset	0							0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERIAXI_SIo_B_CHNL_SEL			PERIAXI_SIo_CTRL_BYPASS			PERIAXI_SIo_WAY_EN									PERIAXI_SIo_OUSTANDING_DISABLE
Type	RO			RW			RW									RW
Reset	0	0	0	0			1	1								0

Bit(s)	Mnemonic	Name	Description
31	**PERIAXI_CG_DISABLE**	PERIAXI_CG_DISABLE	**Controls PERIAXI CG disable** 0: Enable CG 1: Disable CG
24	**PERIAXI_SIo_WR_OT_BUSY**	PERIAXI_SIo_WR_OT_BUSY	**Bypasses PERIAXI control** 0: Disable 1: Enable
23	**PERIAXI_SIo_RD_OT_BUSY**	PERIAXI_SIo_RD_OT_BUSY	**Bypasses PERIAXI control** 0: Disable 1: Enable
22	**PERIAXI_SIo_DFSLV_SET_RID_MISS**	PERIAXI_SIo_DFSLV_SET_RID_MISS	**Bypasses PERIAXI control** 0: Disable 1: Enable
21	**PERIAXI_SIo_DFSLV_SET_BID_MISS**	PERIAXI_SIo_DFSLV_SET_BID_MISS	**Bypasses PERIAXI control** 0: Disable 1: Enable
20	**PERIAXI_SIo_DFSLV_SET_WIRQ**	PERIAXI_SIo_DFSLV_SET_WIRQ	**Bypasses PERIAXI control** 0: Disable 1: Enable
19	**PERIAXI_SIo_DFSLV_SET_RIRQ**	PERIAXI_SIo_DFSLV_SET_RIRQ	**Bypasses PERIAXI control** 0: Disable 1: Enable
18:16	**PERIAXI_SIo_R_CHNL_SEL**	PERIAXI_SIo_R_CHNL_SEL	**Bypasses PERIAXI control** 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable
15:13	**PERIAXI_SIo_B_CHNL_SEL**	PERIAXI_SIo_B_CHNL_SEL	**Bypasses PERIAXI control** 0: Disable 1: Enable
12	**PERIAXI_SIo_CTRL_BYPASS**	PERIAXI_SIo_CTRL_BYPASS	**Bypasses PERIAXI control** 0: Disable 1: Enable
9:8	**PERIAXI_SIo_WAY_EN**	PERIAXI_SIo_WAY_EN	**Enables PERIAXI SIo way**
0	**PERIAXI_SIo_OUSTANDING_DISABLE**	PERIAXI_SIo_OUSTANDING_DISABLE	**Disables PERIAXI SIo oustanding**

10003210 PERIAXI_SI1_CTL **Peripheral AXI SI1 Control** **00000300**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								PERIAXI_SI1_WR_OT_BUSY	PERIAXI_SI1_RD_OT_BUSY	PERIAXI_SI1_DFSLV_SET_RID_MISS	PERIAXI_SI1_DFSLV_SET_BID_MISS	PERIAXI_SI1_DFSLV_SET_WIRQ	PERIAXI_SI1_DFSLV_SET_RIRQ	PERIAXI_SI1_R_CHNL_SEL		
Type								RO	RO	RO	RO	RO	RO	RO		
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERIAXI_SI1_B_CHNL_SEL			PERIAXI_SI1_CTRL_BYPASS			PERIAXI_SI1_WAY_EN									PERIAXI_SI1_OUSTANDING_DISABLE
Type	RO			RW			RW									RW
Reset	0	0	0	0			1	1								0

Bit(s)	Mnemonic	Name	Description
24	**PERIAXI_SI1_WR_OT_BUSY**	PERIAXI_SI1_WR_OT_BUSY	**Bypasses PERIAXI control** 0: Disable 1: Enable
23	**PERIAXI_SI1_RD_OT_BUSY**	PERIAXI_SI1_RD_OT_BUSY	**Bypasses PERIAXI control** 0: Disable 1: Enable
22	**PERIAXI_SI1_DFSLV_SET_RID_MISS**	PERIAXI_SI1_DFSLV_SET_RID_MISS	**Bypasses PERIAXI control** 0: Disable 1: Enable
21	**PERIAXI_SI1_DFSLV_SET_BID_MISS**	PERIAXI_SI1_DFSLV_SET_BID_MISS	**Bypasses PERIAXI control** 0: Disable 1: Enable
20	**PERIAXI_SI1_DFSLV_SET_WIRQ**	PERIAXI_SI1_DFSLV_SET_WIRQ	**Bypasses PERIAXI control** 0: Disable 1: Enable
19	**PERIAXI_SI1_DFSLV_SET_RIRQ**	PERIAXI_SI1_DFSLV_SET_RIRQ	**Bypasses PERIAXI control** 0: Disable 1: Enable

Bit(s)	Mnemonic	Name	Description
18:16	**PERIAXI_SI1_R_CHNL_SEL**	PERIAXI_SI1_R_CHNL_SEL	**Bypasses PERIAXI control** 0: Disable 1: Enable
15:13	**PERIAXI_SI1_B_CHNL_SEL**	PERIAXI_SI1_B_CHNL_SEL	**Bypasses PERIAXI control** 0: Disable 1: Enable
12	**PERIAXI_SI1_CTRL_BYPASS**	PERIAXI_SI1_CTRL_BYPASS	**Bypasses PERIAXI control** 0: Disable 1: Enable
9:8	**PERIAXI_SI1_WAY_EN**	PERIAXI_SI1_WAY_EN	**Enables PERIAXI SI1 way**
0	**PERIAXI_SI1_OUSTANDING_DISABLE**	PERIAXI_SI1_OUSTANDING_DISAB LE	**Disables PERIAXI SI1 oustanding**

10003214 PERIAXI_MI_STA **Peripheral AXI MI Status** **00000040**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**MI1_W_BUSY**	**MI1_R_BUSY**	**MI1_ERRMID_SET_BIRQ**	**MI1_ERRMID_SET_RIRQ**	**MIo_W_BUSY**	**MIo_R_BUSY**	**MIo_ERRMID_SET_BIRQ**	**MIo_ERRMID_SET_RIRQ**
Type									RO	RO	RO	RO	RO	RO	RO	RO
Reset									0	1	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7	**MI1_W_BUSY**	MI1_W_BUSY	**PERIAXI MI1 write busy** 0: MI1 not write busy 1: MI1 write busy
6	**MI1_R_BUSY**	MI1_R_BUSY	**PERIAXI MI1 read busy** 0: MI1 not read busy 1: MI1 read busy
5	**MI1_ERRMID_SET_BIRQ**	MI1_ERRMID_SET_BIRQ	**PERIAXI MI1 write error** 0: MI1 no wite error MID 1: MI1 write error MID
4	**MI1_ERRMID_SET_RIRQ**	MI1_ERRMID_SET_RIRQ	**PERIAXI MI1 read error** 0: MI1 no read error MID 1: MI1 read error MID
3	**MIo_W_BUSY**	MIo_W_BUSY	**PERIAXI MIo write busy** 0: MIo not write busy 1: MIo write busy
2	**MIo_R_BUSY**	MIo_R_BUSY	**PERIAXI MIo read busy** 0: MIo not read busy 1: MIo read busy
1	**MIo_ERRMID_SET_BIRQ**	MIo_ERRMID_SET_BIRQ	**PERIAXI MIo write error** 0: MIo no wite error MID 1: MIo write error MID
0	**MIo_ERRMID_SET_RIRQ**	MIo_ERRMID_SET_RIRQ	**PERIAXI MIo read error** 0: MIo no read error MID

Bit(s)	Mnemonic	Name	Description
			1: MI0 read error MID

10003218 PERIAXI_BUS_CTL4 **Peripheral AXI Bus Control 4** **00004000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ahb3_user															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ahb3_read_ahead_bw	ahb3_fifo_threshold			ahb3_share_en				ahb3_ultra				ahb3_pre_ultra			
Type	RW	RW			RW				RW				RW			
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	**ahb3_user**	ahb3_user	
15	**ahb3_read_ahead_bw**	ahb3_read_ahea d_bw	**Read transaction can pass through bufferable write trnasaction for AHB2AXI bridge 2** 0: Disable 1: Enable
14:12	**ahb3_fifo_threshold**	ahb3_fifo_thre shold	**Launch AXI side awvalid depending on how many write data are received at AHB side** For AHB2AXI bridge 0. 000: First command 001: 1/4 burst length 010: 1/2 burst length 011: 3/4 burst length 100: Full burst length
11:8	**ahb3_share_en**	ahb3_share_en	**Enables AHB bus3 share attribute** Bit 0: Enable SPI2 share attribute when set to 1'b1 Bit 1: Enable SPI3 share attribute when set to 1'b1 Bit 2: Enable SPI4 share attribute when set to 1'b1 Bit 3: Enable SPI5 share attribute when set to 1'b1
7:4	**ahb3_ultra**	ahb3_ultra	**AHB bus 3 ULTRA** Bit 0: SPI2 ULTRA Bit 1: SPI3 ULTRA Bit 2: SPI4 ULTRA Bit 3: SPI5 ULTRA
3:0	**ahb3_pre_ultra**	ahb3_pre_ultra	**AHB bus 3 PER_ULTRA** Bit 0: SPI2 PRE_ULTRA Bit 1: SPI3 PRE_ULTRA Bit 2: SPI4 PRE_ULTRA Bit 3: SPI5 PRE_ULTRA

1000321C PERIAXI_BUS_CTL5 **Peripheral AXI Bus Control 5** **0000003F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											peri2h_64_awhburst			peri2h_64_arhburst		
Type											RW			RW		
Reset											1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
5:3	**peri2h_64_awhburst**	peri2h_64_awhb urst	
2:0	**peri2h_64_arhburst**	peri2h_64_arhb urst	

10003300 PERIAXI_AHB_LMT_CON1 **Peripheral AHB Bus 0 Bandwidth Limiter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						MSDC0_EMI_ULTRA	BUFFER_MODE	BUFFER_EN	Dummy							
Type						RW	RW	RW	RW							
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
10	**MSDC0_EMI_ULTRA**	MSDC0_EMI_ULTR A	
9	**BUFFER_MODE**	BUFFER_MODE	**Condition of early response of per2conn_ahb_bridge_f2s depends on hprot[2] signal of AHB.** 0: Always 1: Conditional
8	**BUFFER_EN**	BUFFER_EN	**Enables early response ability of per2conn_ahb_bridge_f2s** 0: Disable 1: Enable early response
7:0	**Dummy**	Dummy	

10003304 PERIAXI_AHB_LMT_CON2 **Peripheral AHB Bus 0 Bandwidth Limiter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Dummy								Audio_BUS_GNT_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ICUSB_BUS_GNT_CNT								SOFT_LIMIT_EN				FILTER_C	FILTER_LEN		FILTER_E

													KEN				N
Type	RW								RW				RW	RW			RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0

Bit(s)	Mnemonic	Name	Description
31:24	**Dummy**	Dummy	
23:16	**Audio_BUS_GNT_CNT**	Audio_BUS_GNT_CNT	**Audio bus grant count**
15:8	**ICUSB_BUS_GNT_CNT**	ICUSB_BUS_GNT_CNT	**ICUSB bus grant count**
7:4	**SOFT_LIMIT_EN**	SOFT_LIMIT_EN	**Enables AHB bus 0 bandwidth soft-limiter**
3	**FILTER_CKEN**	FILTER_CKEN	**Enables AHB bus 0 bandwidth limiter filter clock**
2:1	**FILTER_LEN**	FILTER_LEN	**AHB bus 0 bandwidth limiter filter length** 00: 256 01: 512 10: 1024 11: 2048
0	**FILTER_EN**	FILTER_EN	**Enables AHB bus 0 bandwidth limiter filter**

10003308 PERIAXI_AHB_LMT_CON3 — **Peripheral AHB Bus 1 Bandwidth Limiter** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SPI0_BUS_GNT_CNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**SPI0_BUS_GNT_CNT**	SPI0_BUS_GNT_CNT	SPI0 bus grant count

1000330C PERIAXI_AHB_LMT_CON4 — **Peripheral AHB Bus 1 Bandwidth Limiter** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MSDC2_BUS_GNT_CNT								MSDC1_BUS_GNT_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PWM_BUS_GNT_CNT								SOFT_LIMIT_EN				FILTER_CKEN	FILTER_LEN		FILTER_EN
Type	RW								RW				RW	RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**MSDC2_BUS_GNT_**	MSDC2_BUS_GNT_	MSDC2 bus grant count

Bit(s)	Mnemonic	Name	Description
	CNT	CNT	
23:16	**MSDC1_BUS_GNT_CNT**	MSDC1_BUS_GNT_CNT	**MSDC1 bus grant count**
15:8	**PWM_BUS_GNT_CNT**	PWM_BUS_GNT_CNT	**PWM bus grant count**
7:4	**SOFT_LIMIT_EN**	SOFT_LIMIT_EN	**Enables AHB bus 1 bandwidth soft-limiter**
3	**FILTER_CKEN**	FILTER_CKEN	**Enables AHB bus 1 bandwidth limiter filter clock**
2:1	**FILTER_LEN**	FILTER_LEN	**AHB bus 1 bandwidth limiter filter length** 00: 256 01: 512 10: 1024 11: 2048
0	**FILTER_EN**	FILTER_EN	**Enables AHB bus 1 bandwidth limiter filter**

10003310 PERIAXI_AHB_LMT_CON5 **Peripheral AHB Bus 2 Bandwidth Limiter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									reg_ahb2_bw_ctrl_7_0							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**reg_ahb2_bw_ctrl_7_0**	reg_ahb2_bw_ctrl_7_0	

10003314 PERIAXI_AHB_LMT_CON6 **Peripheral AHB Bus 2 Bandwidth Limiter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_ahb2_bw_ctrl_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_ahb2_bw_ctrl_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**reg_ahb2_bw_ctrl_31_0**	reg_ahb2_bw_ctrl_31_0	

10003318 PERIAXI_AHB_LMT_CON7 **Peripheral AHB Bus 3 Bandwidth Limiter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SPI5_BUS_GNT_CNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**SPI5_BUS_GNT_CNT**	SPI5_BUS_GNT_CNT	SPI5 bus grant count

1000331C PERIAXI_AHB_LMT_CON8 **Peripheral AHB Bus 3 Bandwidth Limiter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI4_BUS_GNT_CNT								SPI3_BUS_GNT_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI2_BUS_GNT_CNT								SOFT_LIMIT_EN				FILTER_CKEN	FILTER_LEN		FILTER_EN
Type	RW								RW				RW	RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**SPI4_BUS_GNT_CNT**	SPI4_BUS_GNT_CNT	**SPI4 bus grant count**
23:16	**SPI3_BUS_GNT_CNT**	SPI3_BUS_GNT_CNT	**SPI3 bus grant count**
15:8	**SPI2_BUS_GNT_CNT**	SPI2_BUS_GNT_CNT	**SPI2 bus grant count**
7:4	**SOFT_LIMIT_EN**	SOFT_LIMIT_EN	**Enables AHB bus 3 bandwidth soft-limiter**
3	**FILTER_CKEN**	FILTER_CKEN	**Enables AHB bus 3 bandwidth limiter filter clock**
2:1	**FILTER_LEN**	FILTER_LEN	**AHB bus 3 bandwidth limiter filter length** 00: 256 01: 512 10: 1024 11: 2048
0	**FILTER_EN**	FILTER_EN	**Enables AHB bus 3 bandwidth limiter filter**

10003320 PERIAXI_AXI_LMT_CON1 **Peripheral AXI MST0 Bandwidth Limiter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SOFT_LIMIT_EN
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name					FILTER_CKEN	BW_FILTER_EN	FILTER_LEN		AXI_MST0_BUS_GNT_CNT							
Type					RW	RW	RW		RW							
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**SOFT_LIMIT_EN**	SOFT_LIMIT_EN	**Enables AXI MST0 soft bandwidth limiter** 0: Disable 1: Enable
11	**FILTER_CKEN**	FILTER_CKEN	**Enables AHB bus 0 bandwidth limiter filter clock**
10	**BW_FILTER_EN**	BW_FILTER_EN	**Enables AXI MST0 soft bandwidth soft-limiter** 0: Disable 1: Enable
9:8	**FILTER_LEN**	FILTER_LEN	**Enables AXI MST0 bandwidth limiter filter clock** 00: 256 01: 512 10: 1024 11: 2048
7:0	**AXI_MST0_BUS_GNT_CNT**	AXI_MST0_BUS_GNT_CNT	**Enables AXI MST0 bandwidth limiter**

10003324 PERIAXI_AXI_LMT_CON2 **Peripheral AXI MST1 Bandwidth Limiter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SW_EFUSE_MP0_DIS			SOFT_LIMIT_EN
Type													RW			RW
Reset													0			0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FILTER_CKEN	BW_FILTER_EN	FILTER_LEN		AXI_MST1_BUS_GNT_CNT							
Type					RW	RW	RW		RW							
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19	**SW_EFUSE_MP0_DIS**	SW_EFUSE_MP0_DIS	**1 of 2 conditions of SW mode** 0: Disable 1: Enable
16	**SOFT_LIMIT_EN**	SOFT_LIMIT_EN	**Enables AXI MST1 soft bandwidth soft-limiter** 0: Disable 1: Enable
11	**FILTER_CKEN**	FILTER_CKEN	**Enables AXI MST1 bandwidth limiter filter clock**
10	**BW_FILTER_EN**	BW_FILTER_EN	**Enables AXI MST1 bandwidth limiter** 0: Disable 1: Enable
9:8	**FILTER_LEN**	FILTER_LEN	**AXI MST1 bandwidth limiter filter length** 00: 256 01: 512

Bit(s)	Mnemonic	Name	Description
			10: 1024 11: 2048
7:0	**AXI_MST1_BUS_GNT_CNT**	AXI_MST1_BUS_GNT_CNT	**AXI MST1 bus grant count**

10003328 PERIAXI_AXI_LMT_CON3 **Peripheral AXI MST2 Bandwidth Limiter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SOFT_LIMIT_EN
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FILTER_CKEN	BW_FILTER_EN	FILTER_LEN		AXI_MST2_BUS_GNT_CNT							
Type					RW	RW	RW		RW							
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**SOFT_LIMIT_EN**	SOFT_LIMIT_EN	**Enables AXI MST2 soft bandwidth soft-limiter** 0: Disable 1: Enable
11	**FILTER_CKEN**	FILTER_CKEN	**Enables AXI MST2 bandwidth limiter filter clock**
10	**BW_FILTER_EN**	BW_FILTER_EN	**Enables AXI MST2 bandwidth limiter** 0: Disable 1: Enable
9:8	**FILTER_LEN**	FILTER_LEN	**AXI MST2 bandwidth limiter filter length** 00: 256 01: 512 10: 1024 11: 2048
7:0	**AXI_MST2_BUS_GNT_CNT**	AXI_MST2_BUS_GNT_CNT	**AXI MST2 bus grant count**

1000332C PERIAXI_AXI_LMT_CON4 **Peripheral AP DMA Bandwidth Limiter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SOFT_LIMIT_EN
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FILTER_CKEN	BW_FILTER_EN	FILTER_LEN		AXI_DMA_BUS_GNT_CNT							
Type					RW	RW	RW		RW							

Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**SOFT_LIMIT_EN**	SOFT_LIMIT_EN	**Enables AP DMA AXI soft bandwidth soft-limiter** 0: Disable 1: Enable
11	**FILTER_CKEN**	FILTER_CKEN	**Enables AP DMA AXI master bandwidth limiter filter clock**
10	**BW_FILTER_EN**	BW_FILTER_EN	**Enables AP DMA bandwidth limiter** 0: Disable 1: Enable
9:8	**FILTER_LEN**	FILTER_LEN	**AP DMA bandwidth limiter filter length** 00: 256 01: 512 10: 1024 11: 2048
7:0	**AXI_DMA_BUS_GNT_CNT**	AXI_DMA_BUS_GNT_CNT	**AP DMA bus grant count**

10003330 PERIAXI_AXI_LMT_CON5 **Peripheral AXI MSDC0 Bandwidth Limiter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SOFT_LIMIT_EN
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FILTER_CKEN	BW_FILTER_EN	FILTER_LEN		AXI_DMA_BUS_GNT_CNT							
Type					RW	RW	RW		RW							
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**SOFT_LIMIT_EN**	SOFT_LIMIT_EN	**Enables AXI MSDC0 soft bandwidth limiter** 0: Disable 1: Enable
11	**FILTER_CKEN**	FILTER_CKEN	**Enables AXI MSDC0 bandwidth limiter filter clock**
10	**BW_FILTER_EN**	BW_FILTER_EN	**Enables AXI MSDC0 bandwidth limiter** 0: Disable 1: Enable
9:8	**FILTER_LEN**	FILTER_LEN	**AXI MSDC0 bandwidth limiter filter length** 00: 256 01: 512 10: 1024 11: 2048
7:0	**AXI_DMA_BUS_GNT_CNT**	AXI_DMA_BUS_GNT_CNT	**AXI MSDC0 bus grant count**

10003334 PERIAXI_AXI_LMT_CON6 — **Peripheral AXI USB30 Bandwidth Limiter** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SOFT_LIMIT_EN
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FILTER_CKEN	BW_FILTER_EN	FILTER_LEN		AXI_DMA_BUS_GNT_CNT							
Type					RW	RW	RW		RW							
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**SOFT_LIMIT_EN**	SOFT_LIMIT_EN	**Enables AXI USB30 soft bandwidth limiter** 0: Disable 1: Enable
11	**FILTER_CKEN**	FILTER_CKEN	**Enables AXI USB30 bandwidth limiter filter clock**
10	**BW_FILTER_EN**	BW_FILTER_EN	**Enables AXI USB30 bandwidth limiter** 0: Disable 1: Enable
9:8	**FILTER_LEN**	FILTER_LEN	**AXI USB30 bandwidth limiter filter length** 00: 256 01: 512 10: 1024 11: 2048
7:0	**AXI_DMA_BUS_GNT_CNT**	AXI_DMA_BUS_GNT_CNT	**AXI USB30 bus grant count**

10003400 PERI_USB_WAKEUP_DEC_CON0 — **Peripheral USB Wakeup Control 0** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								ssusb_ip_sleep_spm_enable	ssusb_linestate_spm_enable	ssusb_vbusvalid_spm_enable	ssusb_iddig_spm_enable	USB0_CDDEBOUNCE				USB0_CDEN
Type								RW	RW	RW	RW	RW				RW
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8	**ssusb_ip_sleep_spm_enable**	ssusb_ip_sleep_spm_enable	
7	**ssusb_linestat**	ssusb_linestat	

Bit(s)	Mnemonic	Name	Description
	e_spm_enable	e_spm_enable	
6	**ssusb_vbusvali d_spm_enable**	ssusb_vbusvali d_spm_enable	
5	**ssusb_iddig_sp m_enable**	ssusb_iddig_sp m_enable	
4:1	**USB0_CDDEBOUNC E**	USB0_CDDEBOUNC E	**USB0 debounce clock number (0~15)** 0000: 0 0001: 1 0010: 2 1111: 15
0	**USB0_CDEN**	USB0_CDEN	**Enables USB0 clock debounce** 0: Disable 1: Enable

10003404 PERI_USB_WAKEUP_DEC_CON1 **Peripheral USB Wakeup Control 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			ssusb0_cddebounce				ssusb0_cden	ssusb1_cddebounce				ssusb1_cden	ssusb2_cddebounce			
Type			RW				RW	RW				RW	RW			
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ssusb2_cden	ssusb3_cddebounce				ssusb3_cden	ssusb4_cddebounce				ssusb4_cden	USB1_CDDEBOUNCE				USB1_CDEN
Type	RW	RW				RW	RW				RW	RW				RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:26	**ssusb0_cddebou nce**	ssusb0_cddebou nce	
25	**ssusb0_cden**	ssusb0_cden	
24:21	**ssusb1_cddebou nce**	ssusb1_cddebou nce	
20	**ssusb1_cden**	ssusb1_cden	
19:16	**ssusb2_cddebou nce**	ssusb2_cddebou nce	
15	**ssusb2_cden**	ssusb2_cden	
14:11	**ssusb3_cddebou nce**	ssusb3_cddebou nce	
10	**ssusb3_cden**	ssusb3_cden	
9:6	**ssusb4_cddebou nce**	ssusb4_cddebou nce	
5	**ssusb4_cden**	ssusb4_cden	
4:1	**USB1_CDDEBOUNC E**	USB1_CDDEBOUNC E	**USB1 debounce clock number (0~15)** 0000: 0 0001: 1 0010: 2 1111: 15
0	**USB1_CDEN**	USB1_CDEN	**Enables USB1 clock debounce** 0: Disable 1: Enable

10003408 PERI_USB_WAKEUP_DEC_ **Peripheral USB Wakeup Control 2** **00000000**

CON2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											ssusb_lnst_dm_cden	ssusb_lnst_dp_cden	ssusb_lnst_dm_spm_fall_enable	ssusb_lnst_dm_spm_rise_enable	ssusb_lnst_dp_spm_fall_enable	ssusb_lnst_dp_spm_rise_enable
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ssusb_lnst_dm_cddebounce				ssusb_lnst_dp_cddebounce				reg_u3_sleep_event_cden	reg_u3_sleep_event_debounce	reg_u3_sleep_event_cddebounce				reg_u3_sleep_event_mux	
Type	RW				RW				RW	RW	RW				RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21	**ssusb_lnst_dm_cden**	ssusb_lnst_dm_ cden	
20	**ssusb_lnst_dp_cden**	ssusb_lnst_dp_ cden	
19	**ssusb_lnst_dm_spm_fall_enable**	ssusb_lnst_dm_ spm_fall_enable	
18	**ssusb_lnst_dm_spm_rise_enable**	ssusb_lnst_dm_ spm_rise_enable	
17	**ssusb_lnst_dp_spm_fall_enable**	ssusb_lnst_dp_ spm_fall_enable	
16	**ssusb_lnst_dp_spm_rise_enable**	ssusb_lnst_dp_ spm_rise_enable	
15:12	**ssusb_lnst_dm_cddebounce**	ssusb_lnst_dm_ cddebounce	
11:8	**ssusb_lnst_dp_cddebounce**	ssusb_lnst_dp_ cddebounce	
7	**reg_u3_sleep_event_cden**	reg_u3_sleep_e vent_cden	
6	**reg_u3_sleep_event_debounce**	reg_u3_sleep_e vent_debounce	
5:2	**reg_u3_sleep_event_cddebounce**	reg_u3_sleep_e vent_cddebounc e	
1:0	**reg_u3_sleep_event_mux**	reg_u3_sleep_e vent_mux	

10003410 PERI_I2C_MODE_ENABLE **Peripheral I2C Mode Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															i2c3_mod	i2c2_mod

															e_enable	e_enable
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	i2c3_mode_enable	i2c3_mode_enable	
0	i2c2_mode_enable	i2c2_mode_enable	

10003420 PERI_DVFS0_TX_APB_ASYNC_STA **Peri DVFS0 TX APB Async Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																apb_async_dvfs_proco_tx_timer_en
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	apb_async_dvfs_proco_tx_timer_en	apb_async_dvfs_proco_tx_timer_en	

10003424 PERI_DVFS1_TX_APB_ASYNC_STA **Peri DVFS1 TX APB Async Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																apb_async_dvfs_proc1_tx_timer_en
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
0	**apb_async_dvfs_proc1_tx_timer_en**	apb_async_dvfs_proc1_tx_timer_en	

3.2 GPIO Control

Module name: GPIO Base address: (+10005000h)

Address	Name	Width	Register Function
10005000	GPIO_DIR0	32	GPIO Direction Control
10005010	GPIO_DIR1	32	GPIO Direction Control
10005020	GPIO_DIR2	32	GPIO Direction Control
10005030	GPIO_DIR3	32	GPIO Direction Control
10005040	GPIO_DIR4	32	GPIO Direction Control
10005050	GPIO_DIR5	32	GPIO Direction Control
10005060	GPIO_DIR6	32	GPIO Direction Control
10005070	GPIO_DIR7	32	GPIO Direction Control
10005080	GPIO_DIR8	32	GPIO Direction Control
10005004	GPIO_DIR0_SET	32	GPIO Direction Control
10005014	GPIO_DIR1_SET	32	GPIO Direction Control
10005024	GPIO_DIR2_SET	32	GPIO Direction Control
10005034	GPIO_DIR3_SET	32	GPIO Direction Control
10005044	GPIO_DIR4_SET	32	GPIO Direction Control
10005054	GPIO_DIR5_SET	32	GPIO Direction Control
10005064	GPIO_DIR6_SET	32	GPIO Direction Control
10005074	GPIO_DIR7_SET	32	GPIO Direction Control
10005084	GPIO_DIR8_SET	32	GPIO Direction Control
10005008	GPIO_DIR0_CLR	32	GPIO Direction Control
10005018	GPIO_DIR1_CLR	32	GPIO Direction Control
10005028	GPIO_DIR2_CLR	32	GPIO Direction Control
10005038	GPIO_DIR3_CLR	32	GPIO Direction Control
10005048	GPIO_DIR4_CLR	32	GPIO Direction Control
10005058	GPIO_DIR5_CLR	32	GPIO Direction Control
10005068	GPIO_DIR6_CLR	32	GPIO Direction Control
10005078	GPIO_DIR7_CLR	32	GPIO Direction Control
10005088	GPIO_DIR8_CLR	32	GPIO Direction Control
10005100	GPIO_DOUT0	32	GPIO Output Data Control
10005110	GPIO_DOUT1	32	GPIO Output Data Control
10005120	GPIO_DOUT2	32	GPIO Output Data Control
10005130	GPIO_DOUT3	32	GPIO Output Data Control
10005140	GPIO_DOUT4	32	GPIO Output Data Control
10005150	GPIO_DOUT5	32	GPIO Output Data Control
10005160	GPIO_DOUT6	32	GPIO Output Data Control
10005170	GPIO_DOUT7	32	GPIO Output Data Control
10005180	GPIO_DOUT8	32	GPIO Output Data Control
10005104	GPIO_DOUT0_SET	32	GPIO Output Data Control
10005114	GPIO_DOUT1_SET	32	GPIO Output Data Control
10005124	GPIO_DOUT2_SET	32	GPIO Output Data Control
10005134	GPIO_DOUT3_SET	32	GPIO Output Data Control
10005144	GPIO_DOUT4_SET	32	GPIO Output Data Control
10005154	GPIO_DOUT5_SET	32	GPIO Output Data Control
10005164	GPIO_DOUT6_SET	32	GPIO Output Data Control

Address	Name	Width	Register Function
10005174	GPIO_DOUT7_SET	32	GPIO Output Data Control
10005184	GPIO_DOUT8_SET	32	GPIO Output Data Control
10005108	GPIO_DOUT0_CLR	32	GPIO Output Data Control
10005118	GPIO_DOUT1_CLR	32	GPIO Output Data Control
10005128	GPIO_DOUT2_CLR	32	GPIO Output Data Control
10005138	GPIO_DOUT3_CLR	32	GPIO Output Data Control
10005148	GPIO_DOUT4_CLR	32	GPIO Output Data Control
10005158	GPIO_DOUT5_CLR	32	GPIO Output Data Control
10005168	GPIO_DOUT6_CLR	32	GPIO Output Data Control
10005178	GPIO_DOUT7_CLR	32	GPIO Output Data Control
10005188	GPIO_DOUT8_CLR	32	GPIO Output Data Control
10005200	GPIO_DIN0	32	GPIO Data Input Value
10005210	GPIO_DIN1	32	GPIO Data Input Value
10005220	GPIO_DIN2	32	GPIO Data Input Value
10005230	GPIO_DIN3	32	GPIO Data Input Value
10005240	GPIO_DIN4	32	GPIO Data Input Value
10005250	GPIO_DIN5	32	GPIO Data Input Value
10005260	GPIO_DIN6	32	GPIO Data Input Value
10005270	GPIO_DIN7	32	GPIO Data Input Value
10005280	GPIO_DIN8	32	GPIO Data Input Value
10005300	GPIO_MODE0	32	GPIO Mode Control
10005310	GPIO_MODE1	32	GPIO Mode Control
10005320	GPIO_MODE2	32	GPIO Mode Control
10005330	GPIO_MODE3	32	GPIO Mode Control
10005340	GPIO_MODE4	32	GPIO Mode Control
10005350	GPIO_MODE5	32	GPIO Mode Control
10005360	GPIO_MODE6	32	GPIO Mode Control
10005370	GPIO_MODE7	32	GPIO Mode Control
10005380	GPIO_MODE8	32	GPIO Mode Control
10005390	GPIO_MODE9	32	GPIO Mode Control
100053A0	GPIO_MODE10	32	GPIO Mode Control
100053B0	GPIO_MODE11	32	GPIO Mode Control
100053C0	GPIO_MODE12	32	GPIO Mode Control
100053D0	GPIO_MODE13	32	GPIO Mode Control
100053E0	GPIO_MODE14	32	GPIO Mode Control
100053F0	GPIO_MODE15	32	GPIO Mode Control
10005400	GPIO_MODE16	32	GPIO Mode Control
10005410	GPIO_MODE17	32	GPIO Mode Control
10005420	GPIO_MODE18	32	GPIO Mode Control
10005430	GPIO_MODE19	32	GPIO Mode Control
10005440	GPIO_MODE20	32	GPIO Mode Control
10005450	GPIO_MODE21	32	GPIO Mode Control
10005460	GPIO_MODE22	32	GPIO Mode Control
10005470	GPIO_MODE23	32	GPIO Mode Control
10005480	GPIO_MODE24	32	GPIO Mode Control
10005490	GPIO_MODE25	32	GPIO Mode Control

Address	Name	Width	Register Function
100054A0	GPIO_MODE26	32	GPIO Mode Control
100054B0	GPIO_MODE27	32	GPIO Mode Control
100054C0	GPIO_MODE28	32	GPIO Mode Control
100054D0	GPIO_MODE29	32	GPIO Mode Control
100054E0	GPIO_MODE30	32	GPIO Mode Control
100054F0	GPIO_MODE31	32	GPIO Mode Control
10005500	GPIO_MODE32	32	GPIO Mode Control
10005304	GPIO_MODE0_SET	32	GPIO Mode Control
10005314	GPIO_MODE1_SET	32	GPIO Mode Control
10005324	GPIO_MODE2_SET	32	GPIO Mode Control
10005334	GPIO_MODE3_SET	32	GPIO Mode Control
10005344	GPIO_MODE4_SET	32	GPIO Mode Control
10005354	GPIO_MODE5_SET	32	GPIO Mode Control
10005364	GPIO_MODE6_SET	32	GPIO Mode Control
10005374	GPIO_MODE7_SET	32	GPIO Mode Control
10005384	GPIO_MODE8_SET	32	GPIO Mode Control
10005394	GPIO_MODE9_SET	32	GPIO Mode Control
100053A4	GPIO_MODE10_SET	32	GPIO Mode Control
100053B4	GPIO_MODE11_SET	32	GPIO Mode Control
100053C4	GPIO_MODE12_SET	32	GPIO Mode Control
100053D4	GPIO_MODE13_SET	32	GPIO Mode Control
100053E4	GPIO_MODE14_SET	32	GPIO Mode Control
100053F4	GPIO_MODE15_SET	32	GPIO Mode Control
10005404	GPIO_MODE16_SET	32	GPIO Mode Control
10005414	GPIO_MODE17_SET	32	GPIO Mode Control
10005424	GPIO_MODE18_SET	32	GPIO Mode Control
10005434	GPIO_MODE19_SET	32	GPIO Mode Control
10005444	GPIO_MODE20_SET	32	GPIO Mode Control
10005454	GPIO_MODE21_SET	32	GPIO Mode Control
10005464	GPIO_MODE22_SET	32	GPIO Mode Control
10005474	GPIO_MODE23_SET	32	GPIO Mode Control
10005484	GPIO_MODE24_SET	32	GPIO Mode Control
10005494	GPIO_MODE25_SET	32	GPIO Mode Control
100054A4	GPIO_MODE26_SET	32	GPIO Mode Control
100054B4	GPIO_MODE27_SET	32	GPIO Mode Control
100054C4	GPIO_MODE28_SET	32	GPIO Mode Control
100054D4	GPIO_MODE29_SET	32	GPIO Mode Control
100054E4	GPIO_MODE30_SET	32	GPIO Mode Control
100054F4	GPIO_MODE31_SET	32	GPIO Mode Control
10005504	GPIO_MODE32_SET	32	GPIO Mode Control
10005308	GPIO_MODE0_CLR	32	GPIO Mode Control
10005318	GPIO_MODE1_CLR	32	GPIO Mode Control
10005328	GPIO_MODE2_CLR	32	GPIO Mode Control
10005338	GPIO_MODE3_CLR	32	GPIO Mode Control
10005348	GPIO_MODE4_CLR	32	GPIO Mode Control
10005358	GPIO_MODE5_CLR	32	GPIO Mode Control

Address	Name	Width	Register Function
10005368	GPIO_MODE6_CLR	32	GPIO Mode Control
10005378	GPIO_MODE7_CLR	32	GPIO Mode Control
10005388	GPIO_MODE8_CLR	32	GPIO Mode Control
10005398	GPIO_MODE9_CLR	32	GPIO Mode Control
100053A8	GPIO_MODE10_CLR	32	GPIO Mode Control
100053B8	GPIO_MODE11_CLR	32	GPIO Mode Control
100053C8	GPIO_MODE12_CLR	32	GPIO Mode Control
100053D8	GPIO_MODE13_CLR	32	GPIO Mode Control
100053E8	GPIO_MODE14_CLR	32	GPIO Mode Control
100053F8	GPIO_MODE15_CLR	32	GPIO Mode Control
10005408	GPIO_MODE16_CLR	32	GPIO Mode Control
10005418	GPIO_MODE17_CLR	32	GPIO Mode Control
10005428	GPIO_MODE18_CLR	32	GPIO Mode Control
10005438	GPIO_MODE19_CLR	32	GPIO Mode Control
10005448	GPIO_MODE20_CLR	32	GPIO Mode Control
10005458	GPIO_MODE21_CLR	32	GPIO Mode Control
10005468	GPIO_MODE22_CLR	32	GPIO Mode Control
10005478	GPIO_MODE23_CLR	32	GPIO Mode Control
10005488	GPIO_MODE24_CLR	32	GPIO Mode Control
10005498	GPIO_MODE25_CLR	32	GPIO Mode Control
100054A8	GPIO_MODE26_CLR	32	GPIO Mode Control
100054B8	GPIO_MODE27_CLR	32	GPIO Mode Control
100054C8	GPIO_MODE28_CLR	32	GPIO Mode Control
100054D8	GPIO_MODE29_CLR	32	GPIO Mode Control
100054E8	GPIO_MODE30_CLR	32	GPIO Mode Control
100054F8	GPIO_MODE31_CLR	32	GPIO Mode Control
10005508	GPIO_MODE32_CLR	32	GPIO Mode Control
1000530C	GPIO_MODE0_MOD	32	GPIO Mode Control
1000531C	GPIO_MODE1_MOD	32	GPIO Mode Control
1000532C	GPIO_MODE2_MOD	32	GPIO Mode Control
1000533C	GPIO_MODE3_MOD	32	GPIO Mode Control
1000534C	GPIO_MODE4_MOD	32	GPIO Mode Control
1000535C	GPIO_MODE5_MOD	32	GPIO Mode Control
1000536C	GPIO_MODE6_MOD	32	GPIO Mode Control
1000537C	GPIO_MODE7_MOD	32	GPIO Mode Control
1000538C	GPIO_MODE8_MOD	32	GPIO Mode Control
1000539C	GPIO_MODE9_MOD	32	GPIO Mode Control
100053AC	GPIO_MODE10_MOD	32	GPIO Mode Control
100053BC	GPIO_MODE11_MOD	32	GPIO Mode Control
100053CC	GPIO_MODE12_MOD	32	GPIO Mode Control
100053DC	GPIO_MODE13_MOD	32	GPIO Mode Control
100053EC	GPIO_MODE14_MOD	32	GPIO Mode Control
100053FC	GPIO_MODE15_MO	32	GPIO Mode Control

Address	Name	Width	Register Function
	D		
1000540C	GPIO_MODE16_MOD	32	GPIO Mode Control
1000541C	GPIO_MODE17_MOD	32	GPIO Mode Control
1000542C	GPIO_MODE18_MOD	32	GPIO Mode Control
1000543C	GPIO_MODE19_MOD	32	GPIO Mode Control
1000544C	GPIO_MODE20_MOD	32	GPIO Mode Control
1000545C	GPIO_MODE21_MOD	32	GPIO Mode Control
1000546C	GPIO_MODE22_MOD	32	GPIO Mode Control
1000547C	GPIO_MODE23_MOD	32	GPIO Mode Control
1000548C	GPIO_MODE24_MOD	32	GPIO Mode Control
1000549C	GPIO_MODE25_MOD	32	GPIO Mode Control
100054AC	GPIO_MODE26_MOD	32	GPIO Mode Control
100054BC	GPIO_MODE27_MOD	32	GPIO Mode Control
100054CC	GPIO_MODE28_MOD	32	GPIO Mode Control
100054DC	GPIO_MODE29_MOD	32	GPIO Mode Control
100054EC	GPIO_MODE30_MOD	32	GPIO Mode Control
100054FC	GPIO_MODE31_MOD	32	GPIO Mode Control
1000550C	GPIO_MODE32_MOD	32	GPIO Mode Control
10005600	MISC	32	GPIO Related Misc Control
10005604	MISC_SET	32	GPIO Related Misc Control
10005608	MISC_CLR	32	GPIO Related Misc Control

10005000 GPIO_DIR0 GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG0	GPIO_DIR for GPIO 31~0

Bit(s)	Mnemonic	Name	Description
			[31:0] for GPIO31~0 0: GPIO as input 1: GPIO as output

10005010 GPIO_DIR1 GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG1	**GPIO_DIR for GPIO 63~32** [31:0] for GPIO63~32 0: GPIO as input 1: GPIO as output

10005020 GPIO_DIR2 GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG2	**GPIO_DIR for GPIO 95~64** [31:0] for GPIO95~64 0: GPIO as input 1: GPIO as output

10005030 GPIO_DIR3 GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
31:0		CFG3	**GPIO_DIR for GPIO 127~96** [31:0] for GPIO127~96 0: GPIO as input 1: GPIO as output

10005040 GPIO_DIR4 GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG4	**GPIO_DIR for GPIO 159~128** [31:0] for GPIO159~128 0: GPIO as input 1: GPIO as output

10005050 GPIO_DIR5 GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG5	**GPIO_DIR for GPIO 191~160** [31:0] for GPIO191~160 0: GPIO as input 1: GPIO as output

10005060 GPIO_DIR6 GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG6	**GPIO_DIR for GPIO 223~192** [31:0] for GPIO223~192 0: GPIO as input 1: GPIO as output

10005070 GPIO_DIR7 GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG7	**GPIO_DIR for GPIO 255~224** [31:0] for GPIO255~224 0: GPIO as input 1: GPIO as output

10005080 GPIO_DIR8 GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											CFG8					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		CFG8	**GPIO_DIR for GPIO 261~256** [5:0] for GPIO261~256 0: GPIO as input 1: GPIO as output

10005004 GPIO_DIR0_SET GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG0	**Bitwise SET operation of GPIO_DIR0** [31:0] for GPIO31~0 0: Keep 1: SET bits

10005014 GPIO_DIR1_SET GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG1	**Bitwise SET operation of GPIO_DIR1** [31:0] for GPIO63~32 0: Keep 1: SET bits

10005024 GPIO_DIR2_SET GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG2	**Bitwise SET operation of GPIO_DIR2** [31:0] for GPIO95~64 0: Keep 1: SET bits

10005034 GPIO_DIR3_SET GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	CFG3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG3	**Bitwise SET operation of GPIO_DIR3** [31:0] for GPIO127~96 0: Keep 1: SET bits

10005044 GPIO_DIR4_SET **GPIO Direction Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG4	**Bitwise SET operation of GPIO_DIR4** [31:0] for GPIO159~128 0: Keep 1: SET bits

10005054 GPIO_DIR5_SET **GPIO Direction Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG5	**Bitwise SET operation of GPIO_DIR5** [31:0] for GPIO191~160 0: Keep 1: SET bits

10005064 GPIO_DIR6_SET **GPIO Direction Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG6															

Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG6	**Bitwise SET operation of GPIO_DIR6** [31:0] for GPIO223~192 0: Keep 1: SET bits

10005074 GPIO_DIR7_SET **GPIO Direction Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG7															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG7															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG7	**Bitwise SET operation of GPIO_DIR7** [31:0] for GPIO255~224 0: Keep 1: SET bits

10005084 GPIO_DIR8_SET **GPIO Direction Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											CFG8					
Type											WO					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		CFG8	**Bitwise SET operation of GPIO_DIR8** [5:0] for GPIO258~256 0: Keep 1: SET bits

10005008 GPIO_DIR0_CLR **GPIO Direction Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG0	**Bitwise CLR operation of GPIO_DIR0** [31:0] for GPIO31~0 0: Keep 1: CLR bits

10005018 GPIO_DIR1_CLR **GPIO Direction Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG1	**Bitwise CLR operation of GPIO_DIR1** [31:0] for GPIO63~32 0: Keep 1: CLR bits

10005028 GPIO_DIR2_CLR **GPIO Direction Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG2	**Bitwise CLR operation of GPIO_DIR2** [31:0] for GPIO95~64 0: Keep 1: CLR bits

Bit(s)	Mnemonic	Name	Description

10005038 GPIO_DIR3_CLR **GPIO Direction Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG3	**Bitwise CLR operation of GPIO_DIR3** [31:0] for GPIO127~96 0: Keep 1: CLR bits

10005048 GPIO_DIR4_CLR **GPIO Direction Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG4	**Bitwise CLR operation of GPIO_DIR4** [31:0] for GPIO159~128 0: Keep 1: CLR bits

10005058 GPIO_DIR5_CLR **GPIO Direction Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
31:0		CFG5	**Bitwise CLR operation of GPIO_DIR5** [31:0] for GPIO191~160 0: Keep 1: CLR bits

10005068 GPIO_DIR6_CLR **GPIO Direction Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG6	**Bitwise CLR operation of GPIO_DIR6** [31:0] for GPIO223~192 0: Keep 1: CLR bits

10005078 GPIO_DIR7_CLR **GPIO Direction Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG7															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG7															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG7	**Bitwise CLR operation of GPIO_DIR7** [31:0] for GPIO255~224 0: Keep 1: CLR bits

10005088 GPIO_DIR8_CLR **GPIO Direction Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											CFG8					

Type											WO					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		CFG8	**Bitwise CLR operation of GPIO_DIR8** [31:0] for GPIO261~256 0: Keep 1: CLR bits

10005100 GPIO_DOUT0 GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG0	**GPIO_DOUT for GPIO 31~0** [31:0] for GPIO31~0 0: GPIO output LO 1: GPIO output HI

10005110 GPIO_DOUT1 GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG1	**GPIO_DOUT for GPIO 63~32** [31:0] for GPIO63~32 0: GPIO output LO 1: GPIO output HI

10005120 GPIO_DOUT2 GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG2															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG2	**GPIO_DOUT for GPIO 95~64** [31:0] for GPIO95~64 0: GPIO output LO 1: GPIO output HI

10005130 GPIO_DOUT3 GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG3	**GPIO_DOUT for GPIO 127~96** [31:0] for GPIO127~96 0: GPIO output LO 1: GPIO output HI

10005140 GPIO_DOUT4 GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG4	**GPIO_DOUT for GPIO 159~128** [31:0] for GPIO159~128 0: GPIO output LO 1: GPIO output HI

10005150 GPIO_DOUT5 GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG5															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG5	**GPIO_DOUT for GPIO 191~160** [31:0] for GPIO191~160 0: GPIO output LO 1: GPIO output HI

10005160 GPIO_DOUT6 GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG6	**GPIO_DOUT for GPIO 223~192** [31:0] for GPIO223~192 0: GPIO output LO 1: GPIO output HI

10005170 GPIO_DOUT7 GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG7	**GPIO_DOUT for GPIO 255~224** [31:0] for GPIO255~224 0: GPIO output LO 1: GPIO output HI

10005180 GPIO_DOUT8 GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											CFG8					

Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		CFG8	**GPIO_DOUT for GPIO 261~256** [5:0] for GPIO261~256 0: GPIO output LO 1: GPIO output HI

10005104 GPIO_DOUT0_SET GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG0	**Bitwise SET operation of GPIO_DOUT0** [31:0] for GPIO31~0 0: Keep 1: SET bits

10005114 GPIO_DOUT1_SET GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG1	**Bitwise SET operation of GPIO_DOUT1** [31:0] for GPIO63~32 0: Keep 1: SET bits

10005124 GPIO_DOUT2_SET GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG2															
Type	WO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG2	**Bitwise SET operation of GPIO_DOUT2** [31:0] for GPIO95~64 0: Keep 1: SET bits

10005134 GPIO_DOUT3_SET GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG3	**Bitwise SET operation of GPIO_DOUT3** [31:0] for GPIO127~96 0: Keep 1: SET bits

10005144 GPIO_DOUT4_SET GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG4	**Bitwise SET operation of GPIO_DOUT4** [31:0] for GPIO159~128 0: Keep 1: SET bits

10005154 GPIO_DOUT5_SET GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG5	**Bitwise SET operation of GPIO_DOUT5** [31:0] for GPIO191~160 0: Keep 1: SET bits

10005164 GPIO_DOUT6_SET GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG6	**Bitwise SET operation of GPIO_DOUT6** [31:0] for GPIO223~192 0: Keep 1: SET bits

10005174 GPIO_DOUT7_SET GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG7															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG7															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG7	**Bitwise SET operation of GPIO_DOUT7** [31:0] for GPIO255~224 0: Keep 1: SET bits

10005184 GPIO_DOUT8_SET GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											CFG8					
Type											WO					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		CFG8	**Bitwise SET operation of GPIO_DOUT8** [5:0] for GPIO261~256 0: Keep 1: SET bits

10005108 GPIO_DOUT0_CLR GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG0	**Bitwise CLR operation of GPIO_DOUT0** [31:0] for GPIO31~0 0: Keep 1: CLR bits

10005118 GPIO_DOUT1_CLR GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG1	**Bitwise CLR operation of GPIO_DOUT1** [31:0] for GPIO63~32 0: Keep

Bit(s)	Mnemonic	Name	Description
			1: CLR bits

10005128 GPIO_DOUT2_CLR GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG2	**Bitwise CLR operation of GPIO_DOUT2** [31:0] for GPIO95~64 0: Keep 1: CLR bits

10005138 GPIO_DOUT3_CLR GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG3	**Bitwise CLR operation of GPIO_DOUT3** [31:0] for GPIO127~96 0: Keep 1: CLR bits

10005148 GPIO_DOUT4_CLR GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG4	**Bitwise CLR operation of GPIO_DOUT4** [31:0] for GPIO159~128 0: Keep 1: CLR bits

10005158 GPIO_DOUT5_CLR GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG5	**Bitwise CLR operation of GPIO_DOUT5** [31:0] for GPIO191~160 0: Keep 1: CLR bits

10005168 GPIO_DOUT6_CLR GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG6	**Bitwise CLR operation of GPIO_DOUT6** [31:0] for GPIO223~192 0: Keep 1: CLR bits

10005178 GPIO_DOUT7_CLR GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG7															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG7															

Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CFG7	**Bitwise CLR operation of GPIO_DOUT7** [31:0] for GPIO255~224 0: Keep 1: CLR bits

10005188 GPIO_DOUT8_CLR **GPIO Output Data Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											CFG8					
Type											WO					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		CFG8	**Bitwise CLR operation of GPIO_DOUT8** [5:0] for GPIO261~256 0: Keep 1: CLR bits

10005200 GPIO_DIN0 **GPIO Data Input Value** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		DATA0	**GPIO_DIN for GPIO 31~0** [31:0] value of GPIO31~0

10005210 GPIO_DIN1 **GPIO Data Input Value** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA1															

Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		DATA1	**GPIO_DIN for GPIO 63~32** [31:0] value of GPIO63~32

10005220 GPIO_DIN2 GPIO Data Input Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		DATA2	**GPIO_DIN for GPIO 95~64** [31:0] value of GPIO95~64

10005230 GPIO_DIN3 GPIO Data Input Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		DATA3	**GPIO_DIN for GPIO 127~96** [31:0] value of GPIO127~96

10005240 GPIO_DIN4 GPIO Data Input Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA4															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA4															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		DATA4	**GPIO_DIN for GPIO 159~128** [31:0] value of GPIO159~128

Bit(s)	Mnemonic	Name	Description

10005250 GPIO_DIN5 GPIO Data Input Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA5															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA5															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		DATA5	**GPIO_DIN for GPIO 191~160** [31:0] value of GPIO191~160

10005260 GPIO_DIN6 GPIO Data Input Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA6															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA6															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		DATA6	**GPIO_DIN for GPIO 223~192** [31:0] value of GPIO223~192

10005270 GPIO_DIN7 GPIO Data Input Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA7															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA7															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		DATA7	**GPIO_DIN for GPIO 255~224** [31:0] value of GPIO255~224

10005280 GPIO_DIN8 GPIO Data Input Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DATA8					
Type											RU					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		DATA8	**GPIO_DIN for GPIO 261~256** [5:0] value of GPIO261~256

10005300 GPIO_MODE0 GPIO Mode Control 11111111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 7				GPIO 6				GPIO5				GPIO4		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO3				GPIO2				GPIO1				GPIO0		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO7	**Aux mode of RDN1** 000: GPI7_x000D_ 001: CSI0B_L0N_T0B
26:24		GPIO6	**Aux mode of RDP1** 000: GPI6_x000D_ 001: CSI0B_L0P_T0A
22:20		GPIO5	**Aux mode of RCN** 000: GPI5_x000D_ 001: CSI0A_L2N_T1C
18:16		GPIO4	**Aux mode of RCP** 000: GPI4_x000D_ 001: CSI0A_L2P_T1B
14:12		GPIO3	**Aux mode of RDN0** 000: GPI3_x000D_ 001: CSI0A_L1N_T1A
10:8		GPIO2	**Aux mode of RDP0** 000: GPI2_x000D_ 001: CSI0A_L1P_T0C
6:4		GPIO1	**Aux mode of RDN2** 000: GPI1_x000D_ 001: CSI0A_L0N_T0B
2:0		GPIO0	**Aux mode of RDP2** 000: GPI0_x000D_ 001: CSI0A_L0P_T0A

10005310 GPIO_MODE1 GPIO Mode Control 11111111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 15				GPIO 14				GPIO13				GPIO12		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO11				GPIO10				GPIO9				GPIO8		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO15	**Aux mode of RCN_A** 000: GPI15_x000D_ 001: CSI1A_L2N_T1C
26:24		GPIO14	**Aux mode of RCP_A** 000: GPI14_x000D_ 001: CSI1A_L2P_T1B
22:20		GPIO13	**Aux mode of RDN0_A** 000: GPI13_x000D_ 001: CSI1A_L1N_T1A
18:16		GPIO12	**Aux mode of RDP0_A** 000: GPI12_x000D_ 001: CSI1A_L1P_T0C
14:12		GPIO11	**Aux mode of RDN2_A** 000: GPI11_x000D_ 001: CSI1A_L0N_T0B
10:8		GPIO10	**Aux mode of RDP2_A** 000: GPI10_x000D_ 001: CSI1A_L0P_T0A
6:4		GPIO9	**Aux mode of RDN3** 000: GPI9_x000D_ 001: CSI0B_L1N_T1A
2:0		GPIO8	**Aux mode of RDP3** 000: GPI8_x000D_ 001: CSI0B_L1P_T0C

10005320 GPIO_MODE2 **GPIO Mode Control** **11111111**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 23				GPIO 22				GPIO21				GPIO20		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO19				GPIO18				GPIO17				GPIO16		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO23	**Aux mode of RDN0_B** 000: GPI23_x000D_ 001: CSI2_L0N_T0B
26:24		GPIO22	**Aux mode of RDP0_B** 000: GPI22_x000D_

Bit(s)	Mnemonic	Name	Description
			001: CSI2_L0P_T0A
22:20		GPIO21	**Aux mode of RDN1_C** 000: GPI21_x000D_ 001: CSI1B_L2N_T1C
18:16		GPIO20	**Aux mode of RDP1_C** 000: GPI20_x000D_ 001: CSI1B_L2P_T1B
14:12		GPIO19	**Aux mode of RDN3_A** 000: GPI19_x000D_ 001: CSI1B_L1N_T1A
10:8		GPIO18	**Aux mode of RDP3_A** 000: GPI18_x000D_ 001: CSI1B_L1P_T0C
6:4		GPIO17	**Aux mode of RDN1_A** 000: GPI17_x000D_ 001: CSI1B_L0N_T0B
2:0		GPIO16	**Aux mode of RDP1_A** 000: GPI16_x000D_ 001: CSI1B_L0P_T0A

10005330 GPIO_MODE3 **GPIO Mode Control** **00001111**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 31				GPIO 30				GPIO29				GPIO28		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO27				GPIO26				GPIO25				GPIO24		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO31	**Aux mode of CAM_CLK1** 000: GPIO31_x000D_ 001: CMMCLK1_x000D_ 111: MD_CLKM1
26:24		GPIO30	**Aux mode of CAM_CLK0** 000: GPIO30_x000D_ 001: CMMCLK0_x000D_ 111: MD_CLKM0
22:20		GPIO29	**Aux mode of CAM_PDN1** 000: GPIO29_x000D_ 001: SPI5_MI_A_x000D_ 010: DAP_SIB1_SWD_x000D_ 011: UDI_TMS_x000D_ 100: SCP_JTAG_TMS_x000D_ 101: CONN_MCU_TMS_x000D_ 110: CONN_MCU_AICE_TMSC_x000D_ 111: C2K_DM_OTMS
18:16		GPIO28	**Aux mode of CAM_PDN0** 000: GPIO28_x000D_ 001: SPI5_CLK_A_x000D_

Bit(s)	Mnemonic	Name	Description
			010: IRTX_OUT_x000D_
			011: UDI_TDO_x000D_
			100: SCP_JTAG_TDO_x000D_
			101: CONN_MCU_TDO_x000D_
			110: PWM_A_x000D_
			111: C2K_DM_OTDO
14:12		GPIO27	**Aux mode of RDN1_B**
			000: GPI27_x000D_
			001: CSI2_L2N_T1C
10:8		GPIO26	**Aux mode of RDP1_B**
			000: GPI26_x000D_
			001: CSI2_L2P_T1B
6:4		GPIO25	**Aux mode of RCN_B**
			000: GPI25_x000D_
			001: CSI2_L1N_T1A
2:0		GPIO24	**Aux mode of RCP_B**
			000: GPI24_x000D_
			001: CSI2_L1P_T0C

10005340 GPIO_MODE4 **GPIO Mode Control** **01100000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 39				GPIO 38				GPIO37				GPIO36		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	1		0	0	1		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO35				GPIO34				GPIO33				GPIO32		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO39	**Aux mode of DPI_D0**
			000: GPIO39_x000D_
			001: DPI_D0_x000D_
			010: SPI1_CLK_A_x000D_
			011: PCM0_SYNC_x000D_
			100: I2S0_LRCK_x000D_
			101: CONN_MCU_TRST_B_x000D_
			110: URXD3_x000D_
			111: C2K_NTRST
26:24		GPIO38	**Aux mode of SDA0**
			000: GPIO38_x000D_
			001: SDA0_0
22:20		GPIO37	**Aux mode of SCL0**
			000: GPIO37_x000D_
			001: SCL0_0
18:16		GPIO36	**Aux mode of CAM_CLK2**
			000: GPIO36_x000D_
			001: CMMCLK2_x000D_
			010: CLKM2_x000D_
			011: MD_UTXD1_x000D_
			100: PTA_TXD_x000D_

Bit(s)	Mnemonic	Name	Description
			101: CONN_MCU_DBGI_N_x000D_
			110: PWM_C_x000D_
			111: EXT_FRAME_SYNC
14:12		GPIO35	**Aux mode of CAM_RST2**
			000: GPIO35_x000D_
			001: CMMCLK3_x000D_
			010: CLKM1_x000D_
			011: MD_URXD1_x000D_
			100: PTA_RXD_x000D_
			101: CONN_MCU_DBGACK_N_x000D_
			110: PWM_B_x000D_
			111: PCC_PPC_IO
10:8		GPIO34	**Aux mode of CAM_PDN2**
			000: GPIO34_x000D_
			001: CMFLASH_x000D_
			010: CLKM0_x000D_
			011: UDI_NTRST_x000D_
			100: SCP_JTAG_TRSTN_x000D_
			101: CONN_MCU_TRST_B_x000D_
			110: MD_UTXD0_x000D_
			111: C2K_DM_JTINTP
6:4		GPIO33	**Aux mode of CAM_RST1**
			000: GPIO33_x000D_
			001: SPI5_MO_A_x000D_
			010: CMFLASH_x000D_
			011: UDI_TDI_x000D_
			100: SCP_JTAG_TDI_x000D_
			101: CONN_MCU_TDI_x000D_
			110: MD_URXD0_x000D_
			111: C2K_DM_OTDI
2:0		GPIO32	**Aux mode of CAM_RST0**
			000: GPIO32_x000D_
			001: SPI5_CS_A_x000D_
			010: DAP_SIB1_SWCK_x000D_
			011: UDI_TCK_XI_x000D_
			100: SCP_JTAG_TCK_x000D_
			101: CONN_MCU_TCK_x000D_
			110: CONN_MCU_AICE_TCKC_x000D_
			111: C2K_DM_OTCK

10005350 GPIO_MODE5 **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 47				GPIO 46				GPIO45				GPIO44		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO43				GPIO42				GPIO41				GPIO40		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
30:28		GPIO47	**Aux mode of DPI_D8** 000: GPIO47_x000D_ 001: DPI_D8_x000D_ 010: CLKM0_x000D_ 011: PCM1_DO1_x000D_ 100: I2S0_MCK_x000D_ 101: ANT_SEL1_x000D_ 110: PTA_RXD_x000D_ 111: C2K_URXD0
26:24		GPIO46	**Aux mode of DPI_D7** 000: GPIO46_x000D_ 001: DPI_D7_x000D_ 010: SPI2_MO_A_x000D_ 011: PCM1_DO0_x000D_ 100: I2S1_DO_x000D_ 101: ANT_SEL0_x000D_ 110: MD_UTXD0
22:20		GPIO45	**Aux mode of DPI_D6** 000: GPIO45_x000D_ 001: DPI_D6_x000D_ 010: SPI2_CS_A_x000D_ 011: PCM1_DI_x000D_ 100: I2S2_DI_x000D_ 101: CONN_MCU_DBGI_N_x000D_ 110: MD_URXD0
18:16		GPIO44	**Aux mode of DPI_D5** 000: GPIO44_x000D_ 001: DPI_D5_x000D_ 010: SPI2_MI_A_x000D_ 011: PCM1_CLK_x000D_ 100: I2S2_BCK_x000D_ 101: CONN_MCU_TCK_x000D_ 110: CONN_MCU_AICE_TCKC_x000D_ 111: C2K_RTCK
14:12		GPIO43	**Aux mode of DPI_D4** 000: GPIO43_x000D_ 001: DPI_D4_x000D_ 010: SPI2_CLK_A_x000D_ 011: PCM1_SYNC_x000D_ 100: I2S2_LRCK_x000D_ 101: CONN_MCU_TMS_x000D_ 110: CONN_MCU_AICE_TMSC_x000D_ 111: C2K_TDO
10:8		GPIO42	**Aux mode of DPI_D3** 000: GPIO42_x000D_ 001: DPI_D3_x000D_ 010: SPI1_MO_A_x000D_ 011: PCM0_DI_x000D_ 100: I2S0_DI_x000D_ 101: CONN_MCU_TDI_x000D_ 110: UCTS3_x000D_ 111: C2K_TMS
6:4		GPIO41	**Aux mode of DPI_D2** 000: GPIO41_x000D_ 001: DPI_D2_x000D_

Bit(s)	Mnemonic	Name	Description
			010: SPI1_CS_A_x000D_
			011: PCM0_DO_x000D_
			100: I2S3_DO_x000D_
			101: CONN_MCU_DBGACK_N_x000D_
			110: URTS3_x000D_
			111: C2K_TDI
2:0		GPIO40	**Aux mode of DPI_D1**
			000: GPIO40_x000D_
			001: DPI_D1_x000D_
			010: SPI1_MI_A_x000D_
			011: PCM0_CLK_x000D_
			100: I2S0_BCK_x000D_
			101: CONN_MCU_TDO_x000D_
			110: UTXD3_x000D_
			111: C2K_TCK

10005360 GPIO_MODE6 **GPIO Mode Control** **10000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 55				GPIO 54				GPIO53				GPIO52		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO51				GPIO50				GPIO49				GPIO48		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO55	**Aux mode of SCL1**
			000: GPIO55_x000D_
			001: SCL1_0
26:24		GPIO54	**Aux mode of DPI_VSYNC**
			000: GPIO54_x000D_
			001: DPI_VSYNC_x000D_
			010: SPI4_MO_A_x000D_
			011: SPI4_MI_A_x000D_
			100: SDA1_1_x000D_
			101: PWM_A_x000D_
			110: MD_UTXD2_x000D_
			111: EXT_FRAME_SYNC
22:20		GPIO53	**Aux mode of DPI_HSYNC**
			000: GPIO53_x000D_
			001: DPI_HSYNC_x000D_
			010: SPI4_CS_A_x000D_
			011: CMFLASH_x000D_
			100: SCL1_1_x000D_
			101: ANT_SEL7_x000D_
			110: MD_URXD2_x000D_
			111: PCC_PPC_IO
18:16		GPIO52	**Aux mode of DPI_CK**
			000: GPIO52_x000D_
			001: DPI_CK_x000D_

Bit(s)	Mnemonic	Name	Description
			010: SPI4_MI_A_x000D_
			011: SPI4_MO_A_x000D_
			100: SDA0_1_x000D_
			101: ANT_SEL6_x000D_
			111: C2K_URXD1
14:12		GPIO51	**Aux mode of DPI_DE**
			000: GPIO51_x000D_
			001: DPI_DE_x000D_
			010: SPI4_CLK_A_x000D_
			011: IRTX_OUT_x000D_
			100: SCL0_1_x000D_
			101: ANT_SEL5_x000D_
			111: C2K_UTXD1
10:8		GPIO50	**Aux mode of DPI_D11**
			000: GPIO50_x000D_
			001: DPI_D11_x000D_
			010: MD_INT2_x000D_
			011: PWM_D_x000D_
			100: CLKM2_x000D_
			101: ANT_SEL4_x000D_
			110: MD_UTXD1
6:4		GPIO49	**Aux mode of DPI_D10**
			000: GPIO49_x000D_
			001: DPI_D10_x000D_
			010: MD_INT1_C2K_UIM1_HOT_PLUG_IN_x000D_
			011: PWM_C_x000D_
			100: IRTX_OUT_x000D_
			101: ANT_SEL3_x000D_
			110: MD_URXD1
2:0		GPIO48	**Aux mode of DPI_D9**
			000: GPIO48_x000D_
			001: DPI_D9_x000D_
			010: CLKM1_x000D_
			011: CMFLASH_x000D_
			100: I2S2_MCK_x000D_
			101: ANT_SEL2_x000D_
			110: PTA_TXD_x000D_
			111: C2K_UTXD0

10005370 GPIO_MODE7 GPIO Mode Control 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 63				GPIO 62				GPIO61				GPIO60		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO59				GPIO58				GPIO57				GPIO56		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO63	**Aux mode of EINT2**

Bit(s)	Mnemonic	Name	Description
			000: GPIO63_x000D_ 001: EINT2_x000D_ 010: IRTX_OUT_x000D_ 011: SPI4_MO_B_x000D_ 100: I2S0_MCK_x000D_ 101: PCM0_DI_x000D_ 111: C2K_DM_EINT0
26:24		GPIO62	**Aux mode of EINT1** 000: GPIO62_x000D_ 001: EINT1_x000D_ 010: USB_DRVVBUS_x000D_ 011: SPI4_MI_B_x000D_ 100: I2S0_BCK_x000D_ 101: PCM0_CLK_x000D_ 111: C2K_EINT1
22:20		GPIO61	**Aux mode of EINT0** 000: GPIO61_x000D_ 001: EINT0_x000D_ 010: IDDIG_x000D_ 011: SPI4_CLK_B_x000D_ 100: I2S0_LRCK_x000D_ 101: PCM0_SYNC_x000D_ 111: C2K_EINT0
18:16		GPIO60	**Aux mode of SPI0_CS** 000: GPIO60_x000D_ 001: SPI0_CS_x000D_ 010: SDA0_2_x000D_ 011: SCL1_2_x000D_ 100: UCTS3_x000D_ 101: PCM0_DI
14:12		GPIO59	**Aux mode of SPI0_MO** 000: GPIO59_x000D_ 001: SPI0_MO_x000D_ 010: SPI0_MI_x000D_ 011: PWM_C_x000D_ 100: URTS3_x000D_ 101: PCM0_DO
10:8		GPIO58	**Aux mode of SPI0_MI** 000: GPIO58_x000D_ 001: SPI0_MI_x000D_ 010: SPI0_MO_x000D_ 011: SDA1_2_x000D_ 100: URXD3_x000D_ 101: PCM0_CLK
6:4		GPIO57	**Aux mode of SPI0_CK** 000: GPIO57_x000D_ 001: SPI0_CLK_x000D_ 010: SCL0_2_x000D_ 011: PWM_B_x000D_ 100: UTXD3_x000D_ 101: PCM0_SYNC
2:0		GPIO56	**Aux mode of SDA1** 000: GPIO56_x000D_ 001: SDA1_0

Bit(s)	Mnemonic	Name	Description

10005380 GPIO_MODE8 **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 71				GPIO 70				GPIO69				GPIO68		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO67				GPIO66				GPIO65				GPIO64		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO71	**Aux mode of I2S0_MCK** 000: GPIO71_x000D_ 001: I2S0_MCK_x000D_ 010: I2S3_MCK_x000D_ 011: I2S1_MCK_x000D_ 100: I2S2_MCK_x000D_ 111: DBG_MON_A4
26:24		GPIO70	**Aux mode of I2S0_BCK** 000: GPIO70_x000D_ 001: I2S0_BCK_x000D_ 010: I2S3_BCK_x000D_ 011: I2S1_BCK_x000D_ 100: I2S2_BCK_x000D_ 111: DBG_MON_A3
22:20		GPIO69	**Aux mode of I2S0_LRCK** 000: GPIO69_x000D_ 001: I2S0_LRCK_x000D_ 010: I2S3_LRCK_x000D_ 011: I2S1_LRCK_x000D_ 100: I2S2_LRCK_x000D_ 111: DBG_MON_A2
18:16		GPIO68	**Aux mode of EINT7** 000: GPIO68_x000D_ 001: EINT7_x000D_ 010: CLKM3_x000D_ 011: SPI5_CS_B_x000D_ 100: I2S1_DO_x000D_ 101: PWM_D_x000D_ 111: DBG_MON_A1
14:12		GPIO67	**Aux mode of EINT6** 000: GPIO67_x000D_ 001: EINT6_x000D_ 010: CLKM2_x000D_ 011: SPI5_MO_B_x000D_ 100: I2S1_MCK_x000D_ 101: PWM_C_x000D_ 111: DBG_MON_A0
10:8		GPIO66	**Aux mode of EINT5** 000: GPIO66_x000D_

Bit(s)	Mnemonic	Name	Description
			001: EINT5_x000D_ 010: CLKM1_x000D_ 011: SPI5_MI_B_x000D_ 100: I2S1_BCK_x000D_ 101: PWM_B_x000D_ 111: C2K_DM_EINT3
6:4		GPIO65	**Aux mode of EINT4** 000: GPIO65_x000D_ 001: EINT4_x000D_ 010: CLKM0_x000D_ 011: SPI5_CLK_B_x000D_ 100: I2S1_LRCK_x000D_ 101: PWM_A_x000D_ 111: C2K_DM_EINT2
2:0		GPIO64	**Aux mode of EINT3** 000: GPIO64_x000D_ 001: EINT3_x000D_ 010: CMFLASH_x000D_ 011: SPI4_CS_B_x000D_ 100: I2S0_DI_x000D_ 101: PCM0_DO_x000D_ 111: C2K_DM_EINT1

10005390 GPIO_MODE9 GPIO Mode Control 11111100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 79				GPIO 78				GPIO77				GPIO76		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO75				GPIO74				GPIO73				GPIO72		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO79	**Aux mode of CONN_WB_PTA** 000: GPIO79_x000D_ 001: CONN_WB_PTA_x000D_ 111: C2K_DM_EINT3
26:24		GPIO78	**Aux mode of CONN_TOP_DATA** 000: GPIO78_x000D_ 001: CONN_TOP_DATA_x000D_ 111: C2K_DM_EINT2
22:20		GPIO77	**Aux mode of CONN_TOP_CLK** 000: GPIO77_x000D_ 001: CONN_TOP_CLK_x000D_ 111: C2K_DM_EINT1
18:16		GPIO76	**Aux mode of CONN_HRST_B** 000: GPIO76_x000D_ 001: CONN_HRST_B_x000D_ 111: C2K_DM_EINT0
14:12		GPIO75	**Aux mode of SDA3**

Bit(s)	Mnemonic	Name	Description
			000: GPIO75_x000D_
			001: SDA3_0_x000D_
			111: AUXIF_ST1
10:8		GPIO74	**Aux mode of SCL3**
			000: GPIO74_x000D_
			001: SCL3_0_x000D_
			111: AUXIF_CLK1
6:4		GPIO73	**Aux mode of I2S3_DO**
			000: GPIO73_x000D_
			001: I2S3_DO_x000D_
			010: I2S3_DO_x000D_
			011: I2S1_DO_x000D_
			100: I2S1_DO_x000D_
			111: DBG_MON_A6
2:0		GPIO72	**Aux mode of I2S0_DI**
			000: GPIO72_x000D_
			001: I2S0_DI_x000D_
			010: I2S0_DI_x000D_
			011: I2S2_DI_x000D_
			100: I2S2_DI_x000D_
			111: DBG_MON_A5

100053A0 GPIO_MODE1 **GPIO Mode Control** **00011111**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 87				GPIO 86				GPIO85				GPIO84		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO83				GPIO82				GPIO81				GPIO80		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO87	**Aux mode of EINT10**
			000: GPIO87_x000D_
			001: EINT10_x000D_
			010: I2S1_MCK_x000D_
			011: I2S2_MCK_x000D_
			100: URTS1_x000D_
			101: MD_URXD1_x000D_
			111: DBG_MON_A9
26:24		GPIO86	**Aux mode of EINT9**
			000: GPIO86_x000D_
			001: EINT9_x000D_
			010: I2S1_BCK_x000D_
			011: I2S2_BCK_x000D_
			100: UTXD1_x000D_
			101: MD_UTXD0_x000D_
			111: DBG_MON_A8
22:20		GPIO85	**Aux mode of EINT8**
			000: GPIO85_x000D_

Bit(s)	Mnemonic	Name	Description
			001: EINT8_x000D_ 010: I2S1_LRCK_x000D_ 011: I2S2_LRCK_x000D_ 100: URXD1_x000D_ 101: MD_URXD0_x000D_ 111: DBG_MON_A7
18:16		GPIO84	**Aux mode of CONN_BT_DATA** 000: GPIO84_x000D_ 001: CONN_BT_DATA
14:12		GPIO83	**Aux mode of CONN_BT_CLK** 000: GPIO83_x000D_ 001: CONN_BT_CLK_x000D_ 111: MD_CLKM1
10:8		GPIO82	**Aux mode of CONN_WF_CTRL2** 000: GPIO82_x000D_ 001: CONN_WF_HB2_x000D_ 111: MD_CLKM0
6:4		GPIO81	**Aux mode of CONN_WF_CTRL1** 000: GPIO81_x000D_ 001: CONN_WF_HB1_x000D_ 111: C2K_EINT1
2:0		GPIO80	**Aux mode of CONN_WF_CTRL0** 000: GPIO80_x000D_ 001: CONN_WF_HB0_x000D_ 111: C2K_EINT0

100053B0 GPIO_MODE11 **GPIO Mode Control** **10000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 95				GPIO 94				GPIO93				GPIO92		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO91				GPIO90				GPIO89				GPIO88		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO95	**Aux mode of SDA2** 000: GPIO95_x000D_ 001: SDA2_0_x000D_ 111: AUXIF_ST0
26:24		GPIO94	**Aux mode of DRVBUS** 000: GPIO94_x000D_ 001: USB_DRVVBUS_x000D_ 010: PWM_C_x000D_ 011: CLKM5
22:20		GPIO93	**Aux mode of EINT16** 000: GPIO93_x000D_ 001: EINT16_x000D_ 010: IDDIG_x000D_

Bit(s)	Mnemonic	Name	Description
			011: CLKM4_x000D_ 100: PCM1_DO1_x000D_ 101: MD_INT2_x000D_ 111: DROP_ZONE
18:16		GPIO92	**Aux mode of EINT15** 000: GPIO92_x000D_ 001: EINT15_x000D_ 010: PWM_B_x000D_ 011: CLKM3_x000D_ 100: PCM1_DO0_x000D_ 101: SCL0_3
14:12		GPIO91	**Aux mode of EINT14** 000: GPIO91_x000D_ 001: EINT14_x000D_ 010: PWM_A_x000D_ 011: CLKM2_x000D_ 100: PCM1_DI_x000D_ 101: SDA0_3_x000D_ 111: C2K_DM_EINT1
10:8		GPIO90	**Aux mode of EINT13** 000: GPIO90_x000D_ 001: EINT13_x000D_ 010: CMFLASH_x000D_ 011: CLKM1_x000D_ 100: PCM1_CLK_x000D_ 101: UCTS0_x000D_ 111: C2K_DM_EINT0
6:4		GPIO89	**Aux mode of EINT12** 000: GPIO89_x000D_ 001: EINT12_x000D_ 010: IRTX_OUT_x000D_ 011: CLKM0_x000D_ 100: PCM1_SYNC_x000D_ 101: URTS0_x000D_ 111: DBG_MON_A11
2:0		GPIO88	**Aux mode of EINT11** 000: GPIO88_x000D_ 001: EINT11_x000D_ 010: I2S1_DO_x000D_ 011: I2S2_DI_x000D_ 100: UCTS1_x000D_ 101: MD_UTXD1_x000D_ 111: DBG_MON_A10

100053C0 GPIO_MODE12 **GPIO Mode Control** **11001111**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 103				GPIO 102				GPIO101				GPIO100		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO99				GPIO98				GPIO97				GPIO96		

Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO103	**Aux mode of SRCLKENA1** 000: GPIO103_x000D_ 001: SRCLKENA1
26:24		GPIO102	**Aux mode of SRCLKENA0** 000: GPIO102_x000D_ 001: SRCLKENA0
22:20		GPIO101	**Aux mode of SRCLKENAI1** 000: GPIO101_x000D_ 001: SRCLKENAI1
18:16		GPIO100	**Aux mode of SRCLKENAI0** 000: GPIO100_x000D_ 001: SRCLKENAI0
14:12		GPIO99	**Aux mode of RTC32K_CK** 000: GPIO99_x000D_ 001: RTC32K_CK
10:8		GPIO98	**Aux mode of UTXD0** 000: GPIO98_x000D_ 001: UTXD0_x000D_ 010: URXD0_x000D_ 011: MD_UTXD0_x000D_ 100: MD_UTXD1_x000D_ 101: MD_UTXD2_x000D_ 110: C2K_UTXD0_x000D_ 111: C2K_UTXD1
6:4		GPIO97	**Aux mode of URXD0** 000: GPIO97_x000D_ 001: URXD0_x000D_ 010: UTXD0_x000D_ 011: MD_URXD0_x000D_ 100: MD_URXD1_x000D_ 101: MD_URXD2_x000D_ 110: C2K_URXD0_x000D_ 111: C2K_URXD1
2:0		GPIO96	**Aux mode of SCL2** 000: GPIO96_x000D_ 001: SCL2_0_x000D_ 111: AUXIF_CLK0

100053D0 GPIO_MODE13 **GPIO Mode Control** **00100111**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 111				GPIO 110				GPIO109				GPIO108		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	1		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO107				GPIO106				GPIO105				GPIO104		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	1		0	0	1		0	0	1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO111	**Aux mode of KPCOL2** 000: GPIO111_x000D_ 001: KPCOL2_x000D_ 010: SCL1_3_x000D_ 011: PWM_C_x000D_ 100: DISP_PWM_x000D_ 101: I2S1_MCK_x000D_ 111: C2K_DM_EINT2
26:24		GPIO110	**Aux mode of KPCOL1** 000: GPIO110_x000D_ 001: KPCOL1_x000D_ 010: SDA1_3_x000D_ 011: PWM_B_x000D_ 100: CLKM0_x000D_ 101: I2S1_DO_x000D_ 111: C2K_DM_EINT3
22:20		GPIO109	**Aux mode of KPCOL0** 000: GPIO109_x000D_ 001: KPCOL0
18:16		GPIO108	**Aux mode of KPROW2** 000: GPIO108_x000D_ 001: KPROW2_x000D_ 010: USB_DRVVBUS_x000D_ 011: PWM_A_x000D_ 100: CMFLASH_x000D_ 101: I2S1_LRCK_x000D_ 111: DAP_SIB1_SWCK
14:12		GPIO107	**Aux mode of KPROW1** 000: GPIO107_x000D_ 001: KPROW1_x000D_ 010: IDDIG_x000D_ 011: CLKM5_x000D_ 100: TP_GPIO1_AO_x000D_ 101: I2S1_BCK_x000D_ 111: DAP_SIB1_SWD
10:8		GPIO106	**Aux mode of KPROW0** 000: GPIO106_x000D_ 001: KPROW0_x000D_ 010: CMFLASH_x000D_ 011: CLKM4_x000D_ 100: TP_GPIO0_AO_x000D_ 101: IRTX_OUT
6:4		GPIO105	**Aux mode of WATCHDOG** 000: GPIO105_x000D_ 001: WATCHDOG
2:0		GPIO104	**Aux mode of SYSRSTB** 000: GPIO104_x000D_ 001: SYSRSTB

100053E0 GPIO_MODE14 **GPIO Mode Control** **11111100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 119				GPIO 118				GPIO117				GPIO116		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO115				GPIO114				GPIO113				GPIO112		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO119	**Aux mode of MSDC0_DAT5** 000: GPIO119_x000D_ 001: MSDC0_DAT5
26:24		GPIO118	**Aux mode of MSDC0_DAT4** 000: GPIO118_x000D_ 001: MSDC0_DAT4
22:20		GPIO117	**Aux mode of MSDC0_DAT3** 000: GPIO117_x000D_ 001: MSDC0_DAT3
18:16		GPIO116	**Aux mode of MSDC0_DAT2** 000: GPIO116_x000D_ 001: MSDC0_DAT2
14:12		GPIO115	**Aux mode of MSDC0_DAT1** 000: GPIO115_x000D_ 001: MSDC0_DAT1
10:8		GPIO114	**Aux mode of MSDC0_DAT0** 000: GPIO114_x000D_ 001: MSDC0_DAT0
6:4		GPIO113	**Aux mode of INT_SIM2** 000: GPIO113_x000D_ 001: MD_INT0_C2K_UIM0_HOT_PLUG_IN_x000D_ 111: C2K_DM_EINT0
2:0		GPIO112	**Aux mode of INT_SIM1** 000: GPIO112_x000D_ 001: MD_INT1_C2K_UIM1_HOT_PLUG_IN_x000D_ 111: C2K_DM_EINT1

100053F0 GPIO_MODE15 **GPIO Mode Control** **00111111**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 127				GPIO 126				GPIO125				GPIO124		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO123				GPIO122				GPIO121				GPIO120		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO127	**Aux mode of SIM1_SRST** 000: GPIO127_x000D_

Bit(s)	Mnemonic	Name	Description
			001: MD1_SIM1_SRST_x000D_ 010: MD1_SIM2_SRST_x000D_ 011: C2K_UIM0_RST_x000D_ 100: C2K_UIM1_RST
26:24		GPIO126	**Aux mode of SIM1_SCLK** 000: GPIO126_x000D_ 001: MD1_SIM1_SCLK_x000D_ 010: MD1_SIM2_SCLK_x000D_ 011: C2K_UIM0_CLK_x000D_ 100: C2K_UIM1_CLK
22:20		GPIO125	**Aux mode of MSDC0_RSTB** 000: GPIO125_x000D_ 001: MSDC0_RSTB
18:16		GPIO124	**Aux mode of MSDC0_DSL** 000: GPIO124_x000D_ 001: MSDC0_DSL
14:12		GPIO123	**Aux mode of MSDC0_CLK** 000: GPIO123_x000D_ 001: MSDC0_CLK
10:8		GPIO122	**Aux mode of MSDC0_CMD** 000: GPIO122_x000D_ 001: MSDC0_CMD
6:4		GPIO121	**Aux mode of MSDC0_DAT7** 000: GPIO121_x000D_ 001: MSDC0_DAT7
2:0		GPIO120	**Aux mode of MSDC0_DAT6** 000: GPIO120_x000D_ 001: MSDC0_DAT6

10005400 GPIO_MODE16 GPIO Mode Control 01111110

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 135				GPIO 134				GPIO133				GPIO132		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO131				GPIO130				GPIO129				GPIO128		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO135	**Aux mode of TDM_LRCK** 000: GPIO135_x000D_ 001: TDM_LRCK_x000D_ 010: I2S0_LRCK_x000D_ 011: CLKM0_x000D_ 100: PCM1_SYNC_x000D_ 101: PWM_A_x000D_ 111: DBG_MON_A12
26:24		GPIO134	**Aux mode of MSDC1_CLK** 000: GPIO134_x000D_

Bit(s)	Mnemonic	Name	Description
			001: MSDC1_CLK_x000D_ 010: CONN_DSP_JCK_x000D_ 011: LTE_JTAG_TCK_x000D_ 100: UDI_TCK_XI_x000D_ 101: C2K_TCK
22:20		GPIO133	**Aux mode of MSDC1_DAT3** 000: GPIO133_x000D_ 001: MSDC1_DAT3_x000D_ 010: CONN_DSP_JINTP_x000D_ 011: LTE_JTAG_TRSTN_x000D_ 100: UDI_NTRST_x000D_ 101: C2K_NTRST
18:16		GPIO132	**Aux mode of MSDC1_DAT2** 000: GPIO132_x000D_ 001: MSDC1_DAT2_x000D_ 101: C2K_RTCK
14:12		GPIO131	**Aux mode of MSDC1_DAT1** 000: GPIO131_x000D_ 001: MSDC1_DAT1_x000D_ 010: CONN_DSP_JDO_x000D_ 011: LTE_JTAG_TDO_x000D_ 100: UDI_TDO_x000D_ 101: C2K_TDO
10:8		GPIO130	**Aux mode of MSDC1_DAT0** 000: GPIO130_x000D_ 001: MSDC1_DAT0_x000D_ 010: CONN_DSP_JDI_x000D_ 011: LTE_JTAG_TDI_x000D_ 100: UDI_TDI_x000D_ 101: C2K_TDI
6:4		GPIO129	**Aux mode of MSDC1_CMD** 000: GPIO129_x000D_ 001: MSDC1_CMD_x000D_ 010: CONN_DSP_JMS_x000D_ 011: LTE_JTAG_TMS_x000D_ 100: UDI_TMS_x000D_ 101: C2K_TMS
2:0		GPIO128	**Aux mode of SIM1_SIO** 000: GPIO128_x000D_ 001: MD1_SIM1_SIO_x000D_ 010: MD1_SIM2_SIO_x000D_ 011: C2K_UIM0_IO_x000D_ 100: C2K_UIM1_IO

10005410 GPIO_MODE17 GPIO Mode Control 11000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 143				GPIO 142				GPIO141				GPIO140		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO139				GPIO138				GPIO137				GPIO136		

Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO143	**Aux mode of PWRAP_SPI0_MO** 000: GPIO143_x000D_ 001: PWRAP_SPI0_MO_x000D_ 010: PWRAP_SPI0_MI
26:24		GPIO142	**Aux mode of PWRAP_SPI0_MI** 000: GPIO142_x000D_ 001: PWRAP_SPI0_MI_x000D_ 010: PWRAP_SPI0_MO
22:20		GPIO141	**Aux mode of TDM_DATA3** 000: GPIO141_x000D_ 001: TDM_DATA3_x000D_ 010: CMFLASH_x000D_ 011: IRTX_OUT_x000D_ 100: SCL1_4_x000D_ 101: ANT_SEL0_x000D_ 110: UTXD3_x000D_ 111: DBG_MON_A18
18:16		GPIO140	**Aux mode of TDM_DATA2** 000: GPIO140_x000D_ 001: TDM_DATA2_x000D_ 010: DISP_PWM_x000D_ 011: CLKM5_x000D_ 100: SDA1_4_x000D_ 101: ANT_SEL1_x000D_ 110: URXD3_x000D_ 111: DBG_MON_A17
14:12		GPIO139	**Aux mode of TDM_DATA1** 000: GPIO139_x000D_ 001: TDM_DATA1_x000D_ 010: I2S3_DO_x000D_ 011: CLKM4_x000D_ 100: PCM1_DO1_x000D_ 101: ANT_SEL2_x000D_ 110: SCL3_1_x000D_ 111: DBG_MON_A16
10:8		GPIO138	**Aux mode of TDM_DATA0** 000: GPIO138_x000D_ 001: TDM_DATA0_x000D_ 010: I2S0_DI_x000D_ 011: CLKM3_x000D_ 100: PCM1_DO0_x000D_ 101: PWM_C_x000D_ 110: SDA3_1_x000D_ 111: DBG_MON_A15
6:4		GPIO137	**Aux mode of TDM_MCK** 000: GPIO137_x000D_ 001: TDM_MCK_x000D_ 010: I2S0_MCK_x000D_ 011: CLKM2_x000D_ 100: PCM1_DI_x000D_ 101: IRTX_OUT_x000D_

Bit(s)	Mnemonic	Name	Description
			111: DBG_MON_A14
2:0		GPIO136	**Aux mode of TDM_BCK** 000: GPIO136_x000D_ 001: TDM_BCK_x000D_ 010: I2S0_BCK_x000D_ 011: CLKM1_x000D_ 100: PCM1_CLK_x000D_ 101: PWM_B_x000D_ 111: DBG_MON_A13

10005420 GPIO_MODE18 **GPIO Mode Control** **11111111**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 151				GPIO 150				GPIO149				GPIO148		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO147				GPIO146				GPIO145				GPIO144		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO151	**Aux mode of SCL6** 000: GPIO151_x000D_ 001: SCL6_0
26:24		GPIO150	**Aux mode of ANC_DAT_MOSI** 000: GPIO150_x000D_ 001: ANC_DAT_MOSI
22:20		GPIO149	**Aux mode of VOW_CLK_MISO** 000: GPIO149_x000D_ 001: VOW_CLK_MISO
18:16		GPIO148	**Aux mode of AUD_DAT_MOSI** 000: GPIO148_x000D_ 001: AUD_DAT_MOSI_x000D_ 010: AUD_DAT_MISO
14:12		GPIO147	**Aux mode of AUD_DAT_MISO** 000: GPIO147_x000D_ 001: AUD_DAT_MISO_x000D_ 010: AUD_DAT_MOSI_x000D_ 011: VOW_DAT_MISO
10:8		GPIO146	**Aux mode of AUD_CLK_MOSI** 000: GPIO146_x000D_ 001: AUD_CLK_MOSI
6:4		GPIO145	**Aux mode of PWRAP_SPI0_CSN** 000: GPIO145_x000D_ 001: PWRAP_SPI0_CSN
2:0		GPIO144	**Aux mode of PWRAP_SPI0_CK** 000: GPIO144_x000D_ 001: PWRAP_SPI0_CK

10005430 GPIO_MODE19 **GPIO Mode Control** **11000111**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 159				GPIO 158				GPIO157				GPIO156		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO155				GPIO154				GPIO153				GPIO152		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	1		0	0	1		0	0	1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO159	**Aux mode of TDN0** 000: GPI159_x000D_ 001: MIPI_TDN0
26:24		GPIO158	**Aux mode of TDP0** 000: GPI158_x000D_ 001: MIPI_TDP0
22:20		GPIO157	**Aux mode of SIM2_SIO** 000: GPIO157_x000D_ 001: MD1_SIM2_SIO_x000D_ 010: MD1_SIM1_SIO_x000D_ 011: C2K_UIM0_IO_x000D_ 100: C2K_UIM1_IO
18:16		GPIO156	**Aux mode of SIM2_SRST** 000: GPIO156_x000D_ 001: MD1_SIM2_SRST_x000D_ 010: MD1_SIM1_SRST_x000D_ 011: C2K_UIM0_RST_x000D_ 100: C2K_UIM1_RST
14:12		GPIO155	**Aux mode of SIM2_SCLK** 000: GPIO155_x000D_ 001: MD1_SIM2_SCLK_x000D_ 010: MD1_SIM1_SCLK_x000D_ 011: C2K_UIM0_CLK_x000D_ 100: C2K_UIM1_CLK
10:8		GPIO154	**Aux mode of SDA7** 000: GPIO154_x000D_ 001: SDA7_0
6:4		GPIO153	**Aux mode of SCL7** 000: GPIO153_x000D_ 001: SCL7_0
2:0		GPIO152	**Aux mode of SDA6** 000: GPIO152_x000D_ 001: SDA6_0

10005440 GPIO_MODE2 **GPIO Mode Control** **11111111**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 167				GPIO 166				GPIO165				GPIO164		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name		GPIO163				GPIO162				GPIO161				GPIO160		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO167	**Aux mode of TDN3** 000: GPI167_x000D_ 001: MIPI_TDN3
26:24		GPIO166	**Aux mode of TDP3** 000: GPI166_x000D_ 001: MIPI_TDP3
22:20		GPIO165	**Aux mode of TDN2** 000: GPI165_x000D_ 001: MIPI_TDN2
18:16		GPIO164	**Aux mode of TDP2** 000: GPI164_x000D_ 001: MIPI_TDP2
14:12		GPIO163	**Aux mode of TCN** 000: GPI163_x000D_ 001: MIPI_TCN
10:8		GPIO162	**Aux mode of TCP** 000: GPI162_x000D_ 001: MIPI_TCP
6:4		GPIO161	**Aux mode of TDN1** 000: GPI161_x000D_ 001: MIPI_TDN1
2:0		GPIO160	**Aux mode of TDP1** 000: GPI160_x000D_ 001: MIPI_TDP1

10005450 GPIO_MODE21 **GPIO Mode Control** **11111111**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 175				GPIO 174				GPIO173				GPIO172		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO171				GPIO170				GPIO169				GPIO168		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO175	**Aux mode of TDN2_A** 000: GPI175_x000D_ 001: MIPI_TDN2_A
26:24		GPIO174	**Aux mode of TDP2_A** 000: GPI174_x000D_ 001: MIPI_TDP2_A
22:20		GPIO173	**Aux mode of TCN_A** 000: GPI173_x000D_ 001: MIPI_TCN_A
18:16		GPIO172	**Aux mode of TCP_A**

Bit(s)	Mnemonic	Name	Description
			000: GPI172_x000D_
			001: MIPI_TCP_A
14:12		GPIO171	**Aux mode of TDN1_A**
			000: GPI171_x000D_
			001: MIPI_TDN1_A
10:8		GPIO170	**Aux mode of TDP1_A**
			000: GPI170_x000D_
			001: MIPI_TDP1_A
6:4		GPIO169	**Aux mode of TDN0_A**
			000: GPI169_x000D_
			001: MIPI_TDN0_A
2:0		GPIO168	**Aux mode of TDP0_A**
			000: GPI168_x000D_
			001: MIPI_TDP0_A

10005460 GPIO_MODE22 **GPIO Mode Control** **11000011**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 183				GPIO 182				GPIO181				GPIO180		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO179				GPIO178				GPIO177				GPIO176		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	1		0	0	1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO183	**Aux mode of RFIC0_BSI_CK**
			000: GPIO183_x000D_
			001: RFIC0_BSI_CK_x000D_
			010: SPM_BSI_CK_x000D_
			111: DBG_MON_B27
26:24		GPIO182	**Aux mode of TESTMODE**
			000: GPIO182_x000D_
			001: TESTMODE
22:20		GPIO181	**Aux mode of IDDIG**
			000: GPIO181_x000D_
			001: IDDIG_x000D_
			010: DSI_TE1_x000D_
			111: DBG_MON_A22
18:16		GPIO180	**Aux mode of LCM_RST**
			000: GPIO180_x000D_
			001: LCM_RST_x000D_
			010: DSI_TE1_x000D_
			111: DBG_MON_A21
14:12		GPIO179	**Aux mode of DSI_TE**
			000: GPIO179_x000D_
			001: DSI_TE0_x000D_
			111: DBG_MON_A20
10:8		GPIO178	**Aux mode of DISP_PWM**
			000: GPIO178_x000D_

Bit(s)	Mnemonic	Name	Description
			001: DISP_PWM_x000D_
			010: PWM_D_x000D_
			011: CLKM5_x000D_
			111: DBG_MON_A19
6:4		GPIO177	**Aux mode of TDN3_A**
			000: GPI177_x000D_
			001: MIPI_TDN3_A
2:0		GPIO176	**Aux mode of TDP3_A**
			000: GPI176_x000D_
			001: MIPI_TDP3_A

10005470 GPIO_MODE23 GPIO Mode Control 11111111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 191				GPIO 190				GPIO189				GPIO188		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO187				GPIO186				GPIO185				GPIO184		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO191	**Aux mode of MISC_MIPI_DO_1**
			000: GPIO191_x000D_
			001: MIPI1_SDATA
26:24		GPIO190	**Aux mode of MISC_MIPI_CK_1**
			000: GPIO190_x000D_
			001: MIPI1_SCLK
22:20		GPIO189	**Aux mode of MISC_MIPI_DO_0**
			000: GPIO189_x000D_
			001: MIPI0_SDATA
18:16		GPIO188	**Aux mode of MISC_MIPI_CK_0**
			000: GPIO188_x000D_
			001: MIPI0_SCLK_x000D_
			111: DBG_MON_B32
14:12		GPIO187	**Aux mode of RFIC0_BSI_D2**
			000: GPIO187_x000D_
			001: RFIC0_BSI_D2_x000D_
			010: SPM_BSI_D2_x000D_
			111: DBG_MON_B31
10:8		GPIO186	**Aux mode of RFIC0_BSI_D1**
			000: GPIO186_x000D_
			001: RFIC0_BSI_D1_x000D_
			010: SPM_BSI_D1_x000D_
			111: DBG_MON_B30
6:4		GPIO185	**Aux mode of RFIC0_BSI_D0**
			000: GPIO185_x000D_
			001: RFIC0_BSI_D0_x000D_
			010: SPM_BSI_D0_x000D_
			111: DBG_MON_B29

Bit(s)	Mnemonic	Name	Description
2:0		GPIO184	**Aux mode of RFICo_BSI_EN** 000: GPIO184_x000D_ 001: RFICo_BSI_EN_x000D_ 010: SPM_BSI_EN_x000D_ 111: DBG_MON_B28

10005480 GPIO_MODE24 **GPIO Mode Control** **11111111**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 199				GPIO 198				GPIO197				GPIO196		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO195				GPIO194				GPIO193				GPIO192		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO199	**Aux mode of BPI_BUS11** 000: GPIO199_x000D_ 001: BPI_BUS11_x000D_ 111: DBG_MON_B6
26:24		GPIO198	**Aux mode of BPI_BUS10** 000: GPIO198_x000D_ 001: BPI_BUS10_x000D_ 111: DBG_MON_B5
22:20		GPIO197	**Aux mode of BPI_BUS9** 000: GPIO197_x000D_ 001: BPI_BUS9_x000D_ 111: DBG_MON_B4
18:16		GPIO196	**Aux mode of BPI_BUS8** 000: GPIO196_x000D_ 001: BPI_BUS8_x000D_ 111: DBG_MON_B3
14:12		GPIO195	**Aux mode of BPI_BUS7** 000: GPIO195_x000D_ 001: BPI_BUS7_x000D_ 111: DBG_MON_B2
10:8		GPIO194	**Aux mode of BPI_BUS6** 000: GPIO194_x000D_ 001: BPI_BUS6_x000D_ 111: DBG_MON_B1
6:4		GPIO193	**Aux mode of BPI_BUS5** 000: GPIO193_x000D_ 001: BPI_BUS5_x000D_ 111: DBG_MON_Bo
2:0		GPIO192	**Aux mode of BPI_BUS4** 000: GPIO192_x000D_ 001: BPI_BUS4

10005490 GPIO_MODE25 **GPIO Mode Control** **22221111**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 207				GPIO 206				GPIO205				GPIO204		
Type		RW				RW				RW				RW		
Reset		0	1	0		0	1	0		0	1	0		0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO203				GPIO202				GPIO201				GPIO200		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO207	**Aux mode of BPI_BUS19_SWP1** 000: GPIO207_x000D_ 001: BPI_BUS19_x000D_ 010: TX_SWAP1_x000D_ 111: DBG_MON_B14
26:24		GPIO206	**Aux mode of BPI_BUS18_SWP0** 000: GPIO206_x000D_ 001: BPI_BUS18_x000D_ 010: TX_SWAP0_x000D_ 111: DBG_MON_B13
22:20		GPIO205	**Aux mode of BPI_BUS17_VM1** 000: GPIO205_x000D_ 001: BPI_BUS17_x000D_ 010: PA_VM1_x000D_ 111: DBG_MON_B12
18:16		GPIO204	**Aux mode of BPI_BUS16_VM0** 000: GPIO204_x000D_ 001: BPI_BUS16_x000D_ 010: PA_VM0_x000D_ 111: DBG_MON_B11
14:12		GPIO203	**Aux mode of BPI_BUS15_ANT3** 000: GPIO203_x000D_ 001: BPI_BUS15_x000D_ 111: DBG_MON_B10
10:8		GPIO202	**Aux mode of BPI_BUS14_ANT2** 000: GPIO202_x000D_ 001: BPI_BUS14_x000D_ 111: DBG_MON_B9
6:4		GPIO201	**Aux mode of BPI_BUS13_ANT1** 000: GPIO201_x000D_ 001: BPI_BUS13_x000D_ 111: DBG_MON_B8
2:0		GPIO200	**Aux mode of BPI_BUS12_ANT0** 000: GPIO200_x000D_ 001: BPI_BUS12_x000D_ 111: DBG_MON_B7

100054A0 GPIO_MODE26 **GPIO Mode Control** **11112222**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name		GPIO 215				GPIO 214				GPIO213				GPIO212		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO211				GPIO210				GPIO209				GPIO208		
Type		RW				RW				RW				RW		
Reset		0	1	0		0	1	0		0	1	0		0	1	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO215	**Aux mode of BPI_BUS3** 000: GPIO215_x000D_ 001: BPI_BUS3_x000D_ 111: DBG_MON_B22
26:24		GPIO214	**Aux mode of BPI_BUS2** 000: GPIO214_x000D_ 001: BPI_BUS2_x000D_ 111: DBG_MON_B21
22:20		GPIO213	**Aux mode of BPI_BUS1** 000: GPIO213_x000D_ 001: BPI_BUS1_x000D_ 111: DBG_MON_B20
18:16		GPIO212	**Aux mode of BPI_BUS0** 000: GPIO212_x000D_ 001: BPI_BUS0_x000D_ 111: DBG_MON_B19
14:12		GPIO211	**Aux mode of BPI_BUS23_DET1** 000: GPIO211_x000D_ 001: BPI_BUS23_x000D_ 010: DET_BPI1_x000D_ 111: DBG_MON_B18
10:8		GPIO210	**Aux mode of BPI_BUS22_DET0** 000: GPIO210_x000D_ 001: BPI_BUS22_x000D_ 010: DET_BPI0_x000D_ 111: DBG_MON_B17
6:4		GPIO209	**Aux mode of BPI_BUS21_SWP3** 000: GPIO209_x000D_ 001: BPI_BUS21_x000D_ 010: TX_SWAP3_x000D_ 111: DBG_MON_B16
2:0		GPIO208	**Aux mode of BPI_BUS20_SWP2** 000: GPIO208_x000D_ 001: BPI_BUS20_x000D_ 010: TX_SWAP2_x000D_ 111: DBG_MON_B15

100054B0 GPIO_MODE27 **GPIO Mode Control** **11111111**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 223				GPIO 222				GPIO221				GPIO220		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO219				GPIO218				GPIO217				GPIO216		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO223	**Aux mode of WF_QN** 001: CONN_WF_QN
26:24		GPIO222	**Aux mode of WF_QP** 001: CONN_WF_QP
22:20		GPIO221	**Aux mode of WF_IN** 001: CONN_WF_IN
18:16		GPIO220	**Aux mode of WF_IP** 001: CONN_WF_IP
14:12		GPIO219	**Aux mode of MISC_MIPI_DO_3** 000: GPIO219_x000D_ 001: MIPI3_SDATA_x000D_ 111: DBG_MON_B26
10:8		GPIO218	**Aux mode of MISC_MIPI_CK_3** 000: GPIO218_x000D_ 001: MIPI3_SCLK_x000D_ 111: DBG_MON_B25
6:4		GPIO217	**Aux mode of MISC_MIPI_DO_2** 000: GPIO217_x000D_ 001: MIPI2_SDATA_x000D_ 111: DBG_MON_B24
2:0		GPIO216	**Aux mode of MISC_MIPI_CK_2** 000: GPIO216_x000D_ 001: MIPI2_SCLK_x000D_ 111: DBG_MON_B23

100054C0 GPIO_MODE28 **GPIO Mode Control** **11111111**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 231				GPIO 230				GPIO229				GPIO228		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO227				GPIO226				GPIO225				GPIO224		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO231	**Aux mode of GPS_QN** 001: CONN_GPS_QN
26:24		GPIO230	**Aux mode of GPS_QP** 001: CONN_GPS_QP
22:20		GPIO229	**Aux mode of GPS_IN** 001: CONN_GPS_IN
18:16		GPIO228	**Aux mode of GPS_IP** 001: CONN_GPS_IP
14:12		GPIO227	**Aux mode of BT_QN**

Bit(s)	Mnemonic	Name	Description
			001: CONN_BT_QN
10:8		GPIO226	**Aux mode of BT_QP**
			001: CONN_BT_QP
6:4		GPIO225	**Aux mode of BT_IN**
			001: CONN_BT_IN
2:0		GPIO224	**Aux mode of BT_IP**
			001: CONN_BT_IP

100054D0 GPIO_MODE29 **GPIO Mode Control** **11000011**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 239				GPIO 238				GPIO237				GPIO236		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO235				GPIO234				GPIO233				GPIO232		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	1		0	0	1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO239	**Aux mode of SCL4**
			000: GPIO239_x000D_
			001: SCL4_0
26:24		GPIO238	**Aux mode of SDA4**
			000: GPIO238_x000D_
			001: SDA4_0
22:20		GPIO237	**Aux mode of SPI1_CS**
			000: GPIO237_x000D_
			001: SPI1_CS_B_x000D_
			010: TP_URXD1_AO_x000D_
			011: SDA5_1_x000D_
			100: UCTS0_x000D_
			110: CLKM1_x000D_
			111: DBG_MON_A26
18:16		GPIO236	**Aux mode of SPI1_MO**
			000: GPIO236_x000D_
			001: SPI1_MO_B_x000D_
			010: SPI1_MI_B_x000D_
			011: SCL5_1_x000D_
			100: URTS0_x000D_
			110: PWM_B_x000D_
			111: DBG_MON_A25
14:12		GPIO235	**Aux mode of SPI1_MI**
			000: GPIO235_x000D_
			001: SPI1_MI_B_x000D_
			010: SPI1_MO_B_x000D_
			011: SDA4_1_x000D_
			100: URXD0_x000D_
			110: CLKM0_x000D_
			111: DBG_MON_A24
10:8		GPIO234	**Aux mode of SPI1_CK**

Bit(s)	Mnemonic	Name	Description
			000: GPIO234_x000D_
			001: SPI1_CLK_B_x000D_
			010: TP_UTXD1_AO_x000D_
			011: SCL4_1_x000D_
			100: UTXD0_x000D_
			110: PWM_A_x000D_
			111: DBG_MON_A23
6:4		GPIO233	**Aux mode of UTXD1**
			000: GPIO233_x000D_
			001: UTXD1_x000D_
			010: URXD1_x000D_
			011: MD_UTXD0_x000D_
			100: MD_UTXD1_x000D_
			101: MD_UTXD2_x000D_
			110: C2K_UTXD0_x000D_
			111: C2K_UTXD1
2:0		GPIO232	**Aux mode of URXD1**
			000: GPIO232_x000D_
			001: URXD1_x000D_
			010: UTXD1_x000D_
			011: MD_URXD0_x000D_
			100: MD_URXD1_x000D_
			101: MD_URXD2_x000D_
			110: C2K_URXD0_x000D_
			111: C2K_URXD1

100054E0 GPIO_MODE3 **GPIO Mode Control** **00000011**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 247				GPIO 246				GPIO245				GPIO244		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO243				GPIO242				GPIO241				GPIO240		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	1		0	0	1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO247	**Aux mode of I2S1_BCK**
			000: GPIO247_x000D_
			001: I2S1_BCK_x000D_
			010: I2S2_BCK_x000D_
			011: I2S0_BCK_x000D_
			100: I2S3_BCK_x000D_
			101: PCM0_CLK_x000D_
			110: SPI5_MI_C_x000D_
			111: DBG_MON_A32
26:24		GPIO246	**Aux mode of I2S1_LRCK**
			000: GPIO246_x000D_
			001: I2S1_LRCK_x000D_
			010: I2S2_LRCK_x000D_
			011: I2S0_LRCK_x000D_

Bit(s)	Mnemonic	Name	Description
			100: I2S3_LRCK_x000D_
			101: PCM0_SYNC_x000D_
			110: SPI5_CLK_C_x000D_
			111: DBG_MON_A31
22:20		GPIO245	**Aux mode of SPI2_CS**
			000: GPIO245_x000D_
			001: SPI2_CS_B_x000D_
			010: TP_URXD2_AO_x000D_
			011: SDA5_2_x000D_
			100: UCTS1_x000D_
			101: URXD3_x000D_
			110: CLKM3_x000D_
			111: DBG_MON_A30
18:16		GPIO244	**Aux mode of SPI2_MO**
			000: GPIO244_x000D_
			001: SPI2_MO_B_x000D_
			010: SPI2_MI_B_x000D_
			011: SCL5_2_x000D_
			100: URTS1_x000D_
			101: UTXD3_x000D_
			110: PWM_D_x000D_
			111: DBG_MON_A29
14:12		GPIO243	**Aux mode of SPI2_MI**
			000: GPIO243_x000D_
			001: SPI2_MI_B_x000D_
			010: SPI2_MO_B_x000D_
			011: SDA4_2_x000D_
			100: URXD1_x000D_
			101: UCTS3_x000D_
			110: CLKM2_x000D_
			111: DBG_MON_A28
10:8		GPIO242	**Aux mode of SPI2_CK**
			000: GPIO242_x000D_
			001: SPI2_CLK_B_x000D_
			010: TP_UTXD2_AO_x000D_
			011: SCL4_2_x000D_
			100: UTXD1_x000D_
			101: URTS3_x000D_
			110: PWM_C_x000D_
			111: DBG_MON_A27
6:4		GPIO241	**Aux mode of SCL5**
			000: GPIO241_x000D_
			001: SCL5_0
2:0		GPIO240	**Aux mode of SDA5**
			000: GPIO240_x000D_
			001: SDA5_0

100054F0 GPIO_MODE31 **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 255				GPIO 254				GPIO253				GPIO252		
Type		RW				RW				RW				RW		

Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO251				GPIO250				GPIO249				GPIO248		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO255	**Aux mode of AUD_INTN** 000: GPIO255_x000D_ 001: CLKM1_x000D_ 010: DISP_PWM_x000D_ 011: PWM_B_x000D_ 110: TP_GPIO1_AO_x000D_ 111: C2K_TDO
26:24		GPIO254	**Aux mode of I2S1_MCK** 000: GPIO254_x000D_ 001: I2S1_MCK_x000D_ 010: I2S2_MCK_x000D_ 011: I2S0_MCK_x000D_ 100: I2S3_MCK_x000D_ 101: CLKM0_x000D_ 111: C2K_TDI
22:20		GPIO253	**Aux mode of SPI3_CS** 000: GPIO253_x000D_ 001: SPI3_CS_x000D_ 010: SDA0_4_x000D_ 011: PWM_A_x000D_ 111: C2K_TCK
18:16		GPIO252	**Aux mode of SPI3_CK** 000: GPIO252_x000D_ 001: SPI3_CLK_x000D_ 010: SCL0_4_x000D_ 011: PWM_D_x000D_ 111: C2K_TMS
14:12		GPIO251	**Aux mode of SPI3_MO** 000: GPIO251_x000D_ 001: SPI3_MO_x000D_ 010: SPI3_MI_x000D_ 011: CMFLASH_x000D_ 110: TP_UTXD1_AO_x000D_ 111: C2K_RTCK
10:8		GPIO250	**Aux mode of SPI3_MI** 000: GPIO250_x000D_ 001: SPI3_MI_x000D_ 010: SPI3_MO_x000D_ 011: IRTX_OUT_x000D_ 110: TP_URXD1_AO_x000D_ 111: DROP_ZONE
6:4		GPIO249	**Aux mode of I2S1_DO** 000: GPIO249_x000D_ 001: I2S1_DO_x000D_ 010: I2S1_DO_x000D_ 011: I2S3_DO_x000D_ 100: I2S3_DO_x000D_ 101: PCM0_DO_x000D_

Bit(s)	Mnemonic	Name	Description
			110: SPI5_MO_C_x000D_
			111: TRAP_SRAM_PWR_BYPASS
2:0		GPIO248	**Aux mode of I2S2_DI**
			000: GPIO248_x000D_
			001: I2S2_DI_x000D_
			010: I2S2_DI_x000D_
			011: I2S0_DI_x000D_
			100: I2S0_DI_x000D_
			101: PCM0_DI_x000D_
			110: SPI5_CS_C

10005500 GPIO_MODE32 **GPIO Mode Control** **00011110**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										GPIO 261				GPIO260		
Type										RW				RW		
Reset										0	0	0		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO259				GPIO258				GPIO257				GPIO256		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	0

Bit(s)	Mnemonic	Name	Description
22:20		GPIO261	**Aux mode of JTRST_B**
			000: GPIO261_x000D_
			010: LTE_JTAG_TRSTN_x000D_
			011: DFD_NTRST_x000D_
			101: ANC_JTAG_TRSTN_x000D_
			110: SCP_JTAG_TRSTN_x000D_
			111: C2K_DM_JTINTP
18:16		GPIO260	**Aux mode of JTDO**
			000: GPIO260_x000D_
			001: IO_JTAG_TDO_x000D_
			010: LTE_JTAG_TDO_x000D_
			011: DFD_TDO_x000D_
			101: ANC_JTAG_TDO_x000D_
			110: SCP_JTAG_TDO_x000D_
			111: C2K_DM_OTDO
14:12		GPIO259	**Aux mode of JTDI**
			000: GPIO259_x000D_
			001: IO_JTAG_TDI_x000D_
			010: LTE_JTAG_TDI_x000D_
			011: DFD_TDI_x000D_
			101: ANC_JTAG_TDI_x000D_
			110: SCP_JTAG_TDI_x000D_
			111: C2K_DM_OTDI
10:8		GPIO258	**Aux mode of JTCK**
			000: GPIO258_x000D_
			001: IO_JTAG_TCK_x000D_
			010: LTE_JTAG_TCK_x000D_
			011: DFD_TCK_XI_x000D_

Bit(s)	Mnemonic	Name	Description
			100: DAP_SIB1_SWCK_x000D_ 101: ANC_JTAG_TCK_x000D_ 110: SCP_JTAG_TCK_x000D_ 111: C2K_DM_OTCK
6:4		GPIO257	**Aux mode of JTMS** 000: GPIO257_x000D_ 001: IO_JTAG_TMS_x000D_ 010: LTE_JTAG_TMS_x000D_ 011: DFD_TMS_x000D_ 100: DAP_SIB1_SWD_x000D_ 101: ANC_JTAG_TMS_x000D_ 110: SCP_JTAG_TMS_x000D_ 111: C2K_DM_OTMS
2:0		GPIO256	**Aux mode of AUD_PDN** 000: GPIO256_x000D_ 001: CLKM2_x000D_ 010: IRTX_OUT_x000D_ 011: PWM_C_x000D_ 110: TP_GPIO0_AO_x000D_ 111: C2K_NTRST

10005304 GPIO_MODE0_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 7				GPIO 6				GPIO5				GPIO4		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO3				GPIO2				GPIO1				GPIO0		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO7	**Bitwise SET of Aux mode of CSI0B_L0N_T0B** [2:0] 0: Keep 1: SET bits
26:24		GPIO6	**Bitwise SET of Aux mode of CSI0B_L0P_T0A**
22:20		GPIO5	**Bitwise SET of Aux mode of CSI0A_L2N_T1C**
18:16		GPIO4	**Bitwise SET of Aux mode of CSI0A_L2P_T1B**
14:12		GPIO3	**Bitwise SET of Aux mode of CSI0A_L1N_T1A**
10:8		GPIO2	**Bitwise SET of Aux mode of CSI0A_L1P_T0C**
6:4		GPIO1	**Bitwise SET of Aux mode of CSI0A_L0N_T0B**
2:0		GPIO0	**Bitwise SET of Aux mode of CSI0A_L0P_T0A**

10005314 GPIO_MODE1_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 15				GPIO 14				GPIO13				GPIO12		

Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO11				GPIO10				GPIO9				GPIO8		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO15	**Bitwise SET of Aux mode of CSI1A_L2N_T1C** [2:0] 0: Keep 1: SET bits
26:24		GPIO14	**Bitwise SET of Aux mode of CSI1A_L2P_T1B**
22:20		GPIO13	**Bitwise SET of Aux mode of CSI1A_L1N_T1A**
18:16		GPIO12	**Bitwise SET of Aux mode of CSI1A_L1P_T0C**
14:12		GPIO11	**Bitwise SET of Aux mode of CSI1A_L0N_T0B**
10:8		GPIO10	**Bitwise SET of Aux mode of CSI1A_L0P_T0A**
6:4		GPIO9	**Bitwise SET of Aux mode of CSI0B_L1N_T1A**
2:0		GPIO8	**Bitwise SET of Aux mode of CSI0B_L1P_T0C**

10005324 GPIO_MODE2_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 23				GPIO 22				GPIO21				GPIO20		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO19				GPIO18				GPIO17				GPIO16		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO23	**Bitwise SET of Aux mode of CSI2_L0N_T0B** [2:0] 0: Keep 1: SET bits
26:24		GPIO22	**Bitwise SET of Aux mode of CSI2_L0P_T0A**
22:20		GPIO21	**Bitwise SET of Aux mode of CSI1B_L2N_T1C**
18:16		GPIO20	**Bitwise SET of Aux mode of CSI1B_L2P_T1B**
14:12		GPIO19	**Bitwise SET of Aux mode of CSI1B_L1N_T1A**
10:8		GPIO18	**Bitwise SET of Aux mode of CSI1B_L1P_T0C**
6:4		GPIO17	**Bitwise SET of Aux mode of CSI1B_L0N_T0B**
2:0		GPIO16	**Bitwise SET of Aux mode of CSI1B_L0P_T0A**

10005334 GPIO_MODE3_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 31				GPIO 30				GPIO29				GPIO28		

Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO27				GPIO26				GPIO25				GPIO24		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO31	**Bitwise SET of Aux mode of CAM_CLK1** [2:0] 0: Keep 1: SET bits
26:24		GPIO30	**Bitwise SET of Aux mode of CAM_CLK0**
22:20		GPIO29	**Bitwise SET of Aux mode of CAM_PDN1**
18:16		GPIO28	**Bitwise SET of Aux mode of CAM_PDN0**
14:12		GPIO27	**Bitwise SET of Aux mode of CSI2_L2N_T1C**
10:8		GPIO26	**Bitwise SET of Aux mode of CSI2_L2P_T1B**
6:4		GPIO25	**Bitwise SET of Aux mode of CSI2_L1N_T1A**
2:0		GPIO24	**Bitwise SET of Aux mode of CSI2_L1P_T0C**

10005344 GPIO_MODE4_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 39				GPIO 38				GPIO37				GPIO36		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO35				GPIO34				GPIO33				GPIO32		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO39	**Bitwise SET of Aux mode of DPI_D0** [2:0] 0: Keep 1: SET bits
26:24		GPIO38	**Bitwise SET of Aux mode of SDA0**
22:20		GPIO37	**Bitwise SET of Aux mode of SCL0**
18:16		GPIO36	**Bitwise SET of Aux mode of CAM_CLK2**
14:12		GPIO35	**Bitwise SET of Aux mode of CAM_RST2**
10:8		GPIO34	**Bitwise SET of Aux mode of CAM_PDN2**
6:4		GPIO33	**Bitwise SET of Aux mode of CAM_RST1**
2:0		GPIO32	**Bitwise SET of Aux mode of CAM_RST0**

10005354 GPIO_MODE5_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 47				GPIO 46				GPIO45				GPIO44		

Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO43				GPIO42				GPIO41				GPIO40		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO47	**Bitwise SET of Aux mode of DPI_D8** [2:0] 0: Keep 1: SET bits
26:24		GPIO46	**Bitwise SET of Aux mode of DPI_D7**
22:20		GPIO45	**Bitwise SET of Aux mode of DPI_D6**
18:16		GPIO44	**Bitwise SET of Aux mode of DPI_D5**
14:12		GPIO43	**Bitwise SET of Aux mode of DPI_D4**
10:8		GPIO42	**Bitwise SET of Aux mode of DPI_D3**
6:4		GPIO41	**Bitwise SET of Aux mode of DPI_D2**
2:0		GPIO40	**Bitwise SET of Aux mode of DPI_D1**

10005364 GPIO_MODE6_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 55				GPIO 54				GPIO53				GPIO52		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO51				GPIO50				GPIO49				GPIO48		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO55	**Bitwise SET of Aux mode of SCL1** [2:0] 0: Keep 1: SET bits
26:24		GPIO54	**Bitwise SET of Aux mode of DPI_VSYNC**
22:20		GPIO53	**Bitwise SET of Aux mode of DPI_HSYNC**
18:16		GPIO52	**Bitwise SET of Aux mode of DPI_CK**
14:12		GPIO51	**Bitwise SET of Aux mode of DPI_DE**
10:8		GPIO50	**Bitwise SET of Aux mode of DPI_D11**
6:4		GPIO49	**Bitwise SET of Aux mode of DPI_D10**
2:0		GPIO48	**Bitwise SET of Aux mode of DPI_D9**

10005374 GPIO_MODE7_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 63				GPIO 62				GPIO61				GPIO60		

Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO59				GPIO58				GPIO57				GPIO56		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO63	**Bitwise SET of Aux mode of EINT2** [2:0] 0: Keep 1: SET bits
26:24		GPIO62	**Bitwise SET of Aux mode of EINT1**
22:20		GPIO61	**Bitwise SET of Aux mode of EINT0**
18:16		GPIO60	**Bitwise SET of Aux mode of SPI0_CS**
14:12		GPIO59	**Bitwise SET of Aux mode of SPI0_MO**
10:8		GPIO58	**Bitwise SET of Aux mode of SPI0_MI**
6:4		GPIO57	**Bitwise SET of Aux mode of SPI0_CK**
2:0		GPIO56	**Bitwise SET of Aux mode of SDA1**

10005384 GPIO_MODE8_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 71				GPIO 70				GPIO69				GPIO68		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO67				GPIO66				GPIO65				GPIO64		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO71	**Bitwise SET of Aux mode of I2S0_MCK** [2:0] 0: Keep 1: SET bits
26:24		GPIO70	**Bitwise SET of Aux mode of I2S0_BCK**
22:20		GPIO69	**Bitwise SET of Aux mode of I2S0_LRCK**
18:16		GPIO68	**Bitwise SET of Aux mode of EINT7**
14:12		GPIO67	**Bitwise SET of Aux mode of EINT6**
10:8		GPIO66	**Bitwise SET of Aux mode of EINT5**
6:4		GPIO65	**Bitwise SET of Aux mode of EINT4**
2:0		GPIO64	**Bitwise SET of Aux mode of EINT3**

10005394 GPIO_MODE9_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 79				GPIO 78				GPIO77				GPIO76		

Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO75				GPIO74				GPIO73				GPIO72		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO79	**Bitwise SET of Aux mode of CONN_WB_PTA** [2:0] 0: Keep 1: SET bits
26:24		GPIO78	**Bitwise SET of Aux mode of CONN_TOP_DATA**
22:20		GPIO77	**Bitwise SET of Aux mode of CONN_TOP_CLK**
18:16		GPIO76	**Bitwise SET of Aux mode of CONN_HRST_B**
14:12		GPIO75	**Bitwise SET of Aux mode of SDA3**
10:8		GPIO74	**Bitwise SET of Aux mode of SCL3**
6:4		GPIO73	**Bitwise SET of Aux mode of I2S3_DO**
2:0		GPIO72	**Bitwise SET of Aux mode of I2S0_DI**

100053A4 GPIO_MODE10_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 87				GPIO 86				GPIO85				GPIO84		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO83				GPIO82				GPIO81				GPIO80		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO87	**Bitwise SET of Aux mode of EINT10** [2:0] 0: Keep 1: SET bits
26:24		GPIO86	**Bitwise SET of Aux mode of EINT9**
22:20		GPIO85	**Bitwise SET of Aux mode of EINT8**
18:16		GPIO84	**Bitwise SET of Aux mode of CONN_BT_DATA**
14:12		GPIO83	**Bitwise SET of Aux mode of CONN_BT_CLK**
10:8		GPIO82	**Bitwise SET of Aux mode of CONN_WF_CTRL2**
6:4		GPIO81	**Bitwise SET of Aux mode of CONN_WF_CTRL1**
2:0		GPIO80	**Bitwise SET of Aux mode of CONN_WF_CTRL0**

100053B4 GPIO_MODE11_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 95				GPIO 94				GPIO93				GPIO92		

Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO91				GPIO90				GPIO89				GPIO88		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO95	**Bitwise SET of Aux mode of SDA2** [2:0] 0: Keep 1: SET bits
26:24		GPIO94	**Bitwise SET of Aux mode of DRVBUS**
22:20		GPIO93	**Bitwise SET of Aux mode of EINT16**
18:16		GPIO92	**Bitwise SET of Aux mode of EINT15**
14:12		GPIO91	**Bitwise SET of Aux mode of EINT14**
10:8		GPIO90	**Bitwise SET of Aux mode of EINT13**
6:4		GPIO89	**Bitwise SET of Aux mode of EINT12**
2:0		GPIO88	**Bitwise SET of Aux mode of EINT11**

100053C4 GPIO_MODE12_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 103				GPIO 102				GPIO101				GPIO100		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO99				GPIO98				GPIO97				GPIO96		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO103	**Bitwise SET of Aux mode of SRCLKENA1** [2:0] 0: Keep 1: SET bits
26:24		GPIO102	**Bitwise SET of Aux mode of SRCLKENA0**
22:20		GPIO101	**Bitwise SET of Aux mode of SRCLKENAI1**
18:16		GPIO100	**Bitwise SET of Aux mode of SRCLKENAI0**
14:12		GPIO99	**Bitwise SET of Aux mode of RTC32K_CK**
10:8		GPIO98	**Bitwise SET of Aux mode of UTXD0**
6:4		GPIO97	**Bitwise SET of Aux mode of URXD0**
2:0		GPIO96	**Bitwise SET of Aux mode of SCL2**

100053D4 GPIO_MODE13_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 111				GPIO 110				GPIO109				GPIO108		

Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO107				GPIO106				GPIO105				GPIO104		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO111	**Bitwise SET of Aux mode of KPCOL2** [2:0] 0: Keep 1: SET bits
26:24		GPIO110	**Bitwise SET of Aux mode of KPCOL1**
22:20		GPIO109	**Bitwise SET of Aux mode of KPCOL0**
18:16		GPIO108	**Bitwise SET of Aux mode of KPROW2**
14:12		GPIO107	**Bitwise SET of Aux mode of KPROW1**
10:8		GPIO106	**Bitwise SET of Aux mode of KPROW0**
6:4		GPIO105	**Bitwise SET of Aux mode of WATCHDOG**
2:0		GPIO104	**Bitwise SET of Aux mode of SYSRSTB**

100053E4 GPIO_MODE14_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 119				GPIO 118				GPIO117				GPIO116		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO115				GPIO114				GPIO113				GPIO112		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO119	**Bitwise SET of Aux mode of MSDC0_DAT5** [2:0] 0: Keep 1: SET bits
26:24		GPIO118	**Bitwise SET of Aux mode of MSDC0_DAT4**
22:20		GPIO117	**Bitwise SET of Aux mode of MSDC0_DAT3**
18:16		GPIO116	**Bitwise SET of Aux mode of MSDC0_DAT2**
14:12		GPIO115	**Bitwise SET of Aux mode of MSDC0_DAT1**
10:8		GPIO114	**Bitwise SET of Aux mode of MSDC0_DAT0**
6:4		GPIO113	**Bitwise SET of Aux mode of INT_SIM2**
2:0		GPIO112	**Bitwise SET of Aux mode of INT_SIM1**

100053F4 GPIO_MODE15_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 127				GPIO 126				GPIO125				GPIO124		

Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO123				GPIO122				GPIO121				GPIO120		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO127	**Bitwise SET of Aux mode of SIM1_SRST** [2:0] 0: Keep 1: SET bits
26:24		GPIO126	**Bitwise SET of Aux mode of SIM1_SCLK**
22:20		GPIO125	**Bitwise SET of Aux mode of MSDC0_RSTB**
18:16		GPIO124	**Bitwise SET of Aux mode of MSDC0_DSL**
14:12		GPIO123	**Bitwise SET of Aux mode of MSDC0_CLK**
10:8		GPIO122	**Bitwise SET of Aux mode of MSDC0_CMD**
6:4		GPIO121	**Bitwise SET of Aux mode of MSDC0_DAT7**
2:0		GPIO120	**Bitwise SET of Aux mode of MSDC0_DAT6**

10005404 GPIO_MODE16_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 135				GPIO 134				GPIO133				GPIO132		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO131				GPIO130				GPIO129				GPIO128		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO135	**Bitwise SET of Aux mode of TDM_LRCK** [2:0] 0: Keep 1: SET bits
26:24		GPIO134	**Bitwise SET of Aux mode of MSDC1_CLK**
22:20		GPIO133	**Bitwise SET of Aux mode of MSDC1_DAT3**
18:16		GPIO132	**Bitwise SET of Aux mode of MSDC1_DAT2**
14:12		GPIO131	**Bitwise SET of Aux mode of MSDC1_DAT1**
10:8		GPIO130	**Bitwise SET of Aux mode of MSDC1_DAT0**
6:4		GPIO129	**Bitwise SET of Aux mode of MSDC1_CMD**
2:0		GPIO128	**Bitwise SET of Aux mode of SIM1_SIO**

10005414 GPIO_MODE17_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 143				GPIO 142				GPIO141				GPIO140		

Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO139				GPIO138				GPIO137				GPIO136		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO143	**Bitwise SET of Aux mode of PWRAP_SPI0_MO** [2:0] 0: Keep 1: SET bits
26:24		GPIO142	**Bitwise SET of Aux mode of PWRAP_SPI0_MI**
22:20		GPIO141	**Bitwise SET of Aux mode of TDM_DATA3**
18:16		GPIO140	**Bitwise SET of Aux mode of TDM_DATA2**
14:12		GPIO139	**Bitwise SET of Aux mode of TDM_DATA1**
10:8		GPIO138	**Bitwise SET of Aux mode of TDM_DATA0**
6:4		GPIO137	**Bitwise SET of Aux mode of TDM_MCK**
2:0		GPIO136	**Bitwise SET of Aux mode of TDM_BCK**

10005424 GPIO_MODE18_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 151				GPIO 150				GPIO149				GPIO148		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO147				GPIO146				GPIO145				GPIO144		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO151	**Bitwise SET of Aux mode of SCL6** [2:0] 0: Keep 1: SET bits
26:24		GPIO150	**Bitwise SET of Aux mode of ANC_DAT_MOSI**
22:20		GPIO149	**Bitwise SET of Aux mode of VOW_CLK_MISO**
18:16		GPIO148	**Bitwise SET of Aux mode of AUD_DAT_MOSI**
14:12		GPIO147	**Bitwise SET of Aux mode of AUD_DAT_MISO**
10:8		GPIO146	**Bitwise SET of Aux mode of AUD_CLK_MOSI**
6:4		GPIO145	**Bitwise SET of Aux mode of PWRAP_SPI0_CSN**
2:0		GPIO144	**Bitwise SET of Aux mode of PWRAP_SPI0_CK**

10005434 GPIO_MODE19_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 159				GPIO 158				GPIO157				GPIO156		

Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO155				GPIO154				GPIO153				GPIO152		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO159	**Bitwise SET of Aux mode of TDN0** [2:0] 0: Keep 1: SET bits
26:24		GPIO158	**Bitwise SET of Aux mode of TDP0**
22:20		GPIO157	**Bitwise SET of Aux mode of SIM2_SIO**
18:16		GPIO156	**Bitwise SET of Aux mode of SIM2_SRST**
14:12		GPIO155	**Bitwise SET of Aux mode of SIM2_SCLK**
10:8		GPIO154	**Bitwise SET of Aux mode of SDA7**
6:4		GPIO153	**Bitwise SET of Aux mode of SCL7**
2:0		GPIO152	**Bitwise SET of Aux mode of SDA6**

10005444 GPIO_MODE20_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 167				GPIO 166				GPIO165				GPIO164		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO163				GPIO162				GPIO161				GPIO160		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO167	**Bitwise SET of Aux mode of TDN3** [2:0] 0: Keep 1: SET bits
26:24		GPIO166	**Bitwise SET of Aux mode of TDP3**
22:20		GPIO165	**Bitwise SET of Aux mode of TDN2**
18:16		GPIO164	**Bitwise SET of Aux mode of TDP2**
14:12		GPIO163	**Bitwise SET of Aux mode of TCN**
10:8		GPIO162	**Bitwise SET of Aux mode of TCP**
6:4		GPIO161	**Bitwise SET of Aux mode of TDN1**
2:0		GPIO160	**Bitwise SET of Aux mode of TDP1**

10005454 GPIO_MODE21_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 175				GPIO 174				GPIO173				GPIO172		

Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO171				GPIO170				GPIO169				GPIO168		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO175	**Bitwise SET of Aux mode of TDN2_A** [2:0] 0: Keep 1: SET bits
26:24		GPIO174	**Bitwise SET of Aux mode of TDP2_A**
22:20		GPIO173	**Bitwise SET of Aux mode of TCN_A**
18:16		GPIO172	**Bitwise SET of Aux mode of TCP_A**
14:12		GPIO171	**Bitwise SET of Aux mode of TDN1_A**
10:8		GPIO170	**Bitwise SET of Aux mode of TDP1_A**
6:4		GPIO169	**Bitwise SET of Aux mode of TDN0_A**
2:0		GPIO168	**Bitwise SET of Aux mode of TDP0_A**

10005464 GPIO_MODE22_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 183				GPIO 182				GPIO181				GPIO180		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO179				GPIO178				GPIO177				GPIO176		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO183	**Bitwise SET of Aux mode of RFIC0_BSI_CK** [2:0] 0: Keep 1: SET bits
26:24		GPIO182	**Bitwise SET of Aux mode of TESTMODE**
22:20		GPIO181	**Bitwise SET of Aux mode of IDDIG**
18:16		GPIO180	**Bitwise SET of Aux mode of LCM_RST**
14:12		GPIO179	**Bitwise SET of Aux mode of DSI_TE**
10:8		GPIO178	**Bitwise SET of Aux mode of DISP_PWM**
6:4		GPIO177	**Bitwise SET of Aux mode of TDN3_A**
2:0		GPIO176	**Bitwise SET of Aux mode of TDP3_A**

10005474 GPIO_MODE23_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 191				GPIO 190				GPIO189				GPIO188		

Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO187				GPIO186				GPIO185				GPIO184		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO191	**Bitwise SET of Aux mode of MISC_MIPI_DO_1** [2:0] 0: Keep 1: SET bits
26:24		GPIO190	**Bitwise SET of Aux mode of MISC_MIPI_CK_1**
22:20		GPIO189	**Bitwise SET of Aux mode of MISC_MIPI_DO_0**
18:16		GPIO188	**Bitwise SET of Aux mode of MISC_MIPI_CK_0**
14:12		GPIO187	**Bitwise SET of Aux mode of RFIC0_BSI_D2**
10:8		GPIO186	**Bitwise SET of Aux mode of RFIC0_BSI_D1**
6:4		GPIO185	**Bitwise SET of Aux mode of RFIC0_BSI_D0**
2:0		GPIO184	**Bitwise SET of Aux mode of RFIC0_BSI_EN**

10005484 GPIO_MODE24_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 199				GPIO 198				GPIO197				GPIO196		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO195				GPIO194				GPIO193				GPIO192		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO199	**Bitwise SET of Aux mode of BPI_BUS11** [2:0] 0: Keep 1: SET bits
26:24		GPIO198	**Bitwise SET of Aux mode of BPI_BUS10**
22:20		GPIO197	**Bitwise SET of Aux mode of BPI_BUS9**
18:16		GPIO196	**Bitwise SET of Aux mode of BPI_BUS8**
14:12		GPIO195	**Bitwise SET of Aux mode of BPI_BUS7**
10:8		GPIO194	**Bitwise SET of Aux mode of BPI_BUS6**
6:4		GPIO193	**Bitwise SET of Aux mode of BPI_BUS5**
2:0		GPIO192	**Bitwise SET of Aux mode of BPI_BUS4**

10005494 GPIO_MODE25_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 207				GPIO 206				GPIO205				GPIO204		

Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO203				GPIO202				GPIO201				GPIO200		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO207	**Bitwise SET of Aux mode of BPI_BUS19_SWP1** [2:0] 0: Keep 1: SET bits
26:24		GPIO206	**Bitwise SET of Aux mode of BPI_BUS18_SWP0**
22:20		GPIO205	**Bitwise SET of Aux mode of BPI_BUS17_VM1**
18:16		GPIO204	**Bitwise SET of Aux mode of BPI_BUS16_VM0**
14:12		GPIO203	**Bitwise SET of Aux mode of BPI_BUS15_ANT3**
10:8		GPIO202	**Bitwise SET of Aux mode of BPI_BUS14_ANT2**
6:4		GPIO201	**Bitwise SET of Aux mode of BPI_BUS13_ANT1**
2:0		GPIO200	**Bitwise SET of Aux mode of BPI_BUS12_ANT0**

100054A4 GPIO_MODE26_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 215				GPIO 214				GPIO213				GPIO212		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO211				GPIO210				GPIO209				GPIO208		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO215	**Bitwise SET of Aux mode of BPI_BUS3** [2:0] 0: Keep 1: SET bits
26:24		GPIO214	**Bitwise SET of Aux mode of BPI_BUS2**
22:20		GPIO213	**Bitwise SET of Aux mode of BPI_BUS1**
18:16		GPIO212	**Bitwise SET of Aux mode of BPI_BUS0**
14:12		GPIO211	**Bitwise SET of Aux mode of BPI_BUS23_DET1**
10:8		GPIO210	**Bitwise SET of Aux mode of BPI_BUS22_DET0**
6:4		GPIO209	**Bitwise SET of Aux mode of BPI_BUS21_SWP3**
2:0		GPIO208	**Bitwise SET of Aux mode of BPI_BUS20_SWP2**

100054B4 GPIO_MODE27_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 223				GPIO 222				GPIO221				GPIO220		

Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO219				GPIO218				GPIO217				GPIO216		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO223	**Bitwise SET of Aux mode of WF_QN** [2:0] 0: Keep 1: SET bits
26:24		GPIO222	**Bitwise SET of Aux mode of WF_QP**
22:20		GPIO221	**Bitwise SET of Aux mode of WF_IN**
18:16		GPIO220	**Bitwise SET of Aux mode of WF_IP**
14:12		GPIO219	**Bitwise SET of Aux mode of MISC_MIPI_DO_3**
10:8		GPIO218	**Bitwise SET of Aux mode of MISC_MIPI_CK_3**
6:4		GPIO217	**Bitwise SET of Aux mode of MISC_MIPI_DO_2**
2:0		GPIO216	**Bitwise SET of Aux mode of MISC_MIPI_CK_2**

100054C4 GPIO_MODE28_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 231				GPIO 230				GPIO229				GPIO228		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO227				GPIO226				GPIO225				GPIO224		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO231	**Bitwise SET of Aux mode of GPS_QN** [2:0] 0: Keep 1: SET bits
26:24		GPIO230	**Bitwise SET of Aux mode of GPS_QP**
22:20		GPIO229	**Bitwise SET of Aux mode of GPS_IN**
18:16		GPIO228	**Bitwise SET of Aux mode of GPS_IP**
14:12		GPIO227	**Bitwise SET of Aux mode of BT_QN**
10:8		GPIO226	**Bitwise SET of Aux mode of BT_QP**
6:4		GPIO225	**Bitwise SET of Aux mode of BT_IN**
2:0		GPIO224	**Bitwise SET of Aux mode of BT_IP**

100054D4 GPIO_MODE29_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 239				GPIO 238				GPIO237				GPIO236		

Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO235				GPIO234				GPIO233				GPIO232		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO239	**Bitwise SET of Aux mode of SCL4** [2:0] 0: Keep 1: SET bits
26:24		GPIO238	**Bitwise SET of Aux mode of SDA4**
22:20		GPIO237	**Bitwise SET of Aux mode of SPI1_CS**
18:16		GPIO236	**Bitwise SET of Aux mode of SPI1_MO**
14:12		GPIO235	**Bitwise SET of Aux mode of SPI1_MI**
10:8		GPIO234	**Bitwise SET of Aux mode of SPI1_CK**
6:4		GPIO233	**Bitwise SET of Aux mode of UTXD1**
2:0		GPIO232	**Bitwise SET of Aux mode of URXD1**

100054E4 GPIO_MODE30_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 247				GPIO 246				GPIO245				GPIO244		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO243				GPIO242				GPIO241				GPIO240		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO247	**Bitwise SET of Aux mode of I2S1_BCK** [2:0] 0: Keep 1: SET bits
26:24		GPIO246	**Bitwise SET of Aux mode of I2S1_LRCK**
22:20		GPIO245	**Bitwise SET of Aux mode of SPI2_CS**
18:16		GPIO244	**Bitwise SET of Aux mode of SPI2_MO**
14:12		GPIO243	**Bitwise SET of Aux mode of SPI2_MI**
10:8		GPIO242	**Bitwise SET of Aux mode of SPI2_CK**
6:4		GPIO241	**Bitwise SET of Aux mode of SCL5**
2:0		GPIO240	**Bitwise SET of Aux mode of SDA5**

100054F4 GPIO_MODE31_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 255				GPIO 254				GPIO253				GPIO252		

Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO251				GPIO250				GPIO249				GPIO248		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO255	**Bitwise SET of Aux mode of AUD_INTN** [2:0] 0: Keep 1: SET bits
26:24		GPIO254	**Bitwise SET of Aux mode of I2S1_MCK**
22:20		GPIO253	**Bitwise SET of Aux mode of SPI3_CS**
18:16		GPIO252	**Bitwise SET of Aux mode of SPI3_CK**
14:12		GPIO251	**Bitwise SET of Aux mode of SPI3_MO**
10:8		GPIO250	**Bitwise SET of Aux mode of SPI3_MI**
6:4		GPIO249	**Bitwise SET of Aux mode of I2S1_DO**
2:0		GPIO248	**Bitwise SET of Aux mode of I2S2_DI**

10005504 GPIO_MODE32_SET **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										GPIO 261				GPIO260		
Type										WO				WO		
Reset										0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO259				GPIO258				GPIO257				GPIO256		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
22:20		GPIO261	**Bitwise SET of Aux mode of JTRST_B** [2:0] 0: Keep 1: SET bits
18:16		GPIO260	**Bitwise SET of Aux mode of JTDO**
14:12		GPIO259	**Bitwise SET of Aux mode of JTDI**
10:8		GPIO258	**Bitwise SET of Aux mode of JTCK**
6:4		GPIO257	**Bitwise SET of Aux mode of JTMS**
2:0		GPIO256	**Bitwise SET of Aux mode of AUD_PDN**

10005308 GPIO_MODE0_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 7				GPIO 6				GPIO5				GPIO4		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO3				GPIO2				GPIO1				GPIO0		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO7	**Bitwise CLR of Aux mode of CSI0B_L0N_T0B** [2:0] 0: Keep 1: CLR bits
26:24		GPIO6	**Bitwise CLR of Aux mode of CSI0B_L0P_T0A**
22:20		GPIO5	**Bitwise CLR of Aux mode of CSI0A_L2N_T1C**
18:16		GPIO4	**Bitwise CLR of Aux mode of CSI0A_L2P_T1B**
14:12		GPIO3	**Bitwise CLR of Aux mode of CSI0A_L1N_T1A**
10:8		GPIO2	**Bitwise CLR of Aux mode of CSI0A_L1P_T0C**
6:4		GPIO1	**Bitwise CLR of Aux mode of CSI0A_L0N_T0B**
2:0		GPIO0	**Bitwise CLR of Aux mode of CSI0A_L0P_T0A**

10005318 GPIO_MODE1_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 15				GPIO 14				GPIO13				GPIO12		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO11				GPIO10				GPIO9				GPIO8		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO15	**Bitwise CLR of Aux mode of CSI1A_L2N_T1C** [2:0] 0: Keep 1: CLR bits
26:24		GPIO14	**Bitwise CLR of Aux mode of CSI1A_L2P_T1B**
22:20		GPIO13	**Bitwise CLR of Aux mode of CSI1A_L1N_T1A**
18:16		GPIO12	**Bitwise CLR of Aux mode of CSI1A_L1P_T0C**
14:12		GPIO11	**Bitwise CLR of Aux mode of CSI1A_L0N_T0B**
10:8		GPIO10	**Bitwise CLR of Aux mode of CSI1A_L0P_T0A**
6:4		GPIO9	**Bitwise CLR of Aux mode of CSI0B_L1N_T1A**
2:0		GPIO8	**Bitwise CLR of Aux mode of CSI0B_L1P_T0C**

10005328 GPIO_MODE2_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 23				GPIO 22				GPIO21				GPIO20		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO19				GPIO18				GPIO17				GPIO16		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO23	**Bitwise CLR of Aux mode of CSI2_L0N_T0B** [2:0] 0: Keep 1: CLR bits
26:24		GPIO22	**Bitwise CLR of Aux mode of CSI2_L0P_T0A**
22:20		GPIO21	**Bitwise CLR of Aux mode of CSI1B_L2N_T1C**
18:16		GPIO20	**Bitwise CLR of Aux mode of CSI1B_L2P_T1B**
14:12		GPIO19	**Bitwise CLR of Aux mode of CSI1B_L1N_T1A**
10:8		GPIO18	**Bitwise CLR of Aux mode of CSI1B_L1P_T0C**
6:4		GPIO17	**Bitwise CLR of Aux mode of CSI1B_L0N_T0B**
2:0		GPIO16	**Bitwise CLR of Aux mode of CSI1B_L0P_T0A**

10005338 GPIO_MODE3_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 31				GPIO 30				GPIO29				GPIO28		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO27				GPIO26				GPIO25				GPIO24		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO31	**Bitwise CLR of Aux mode of CAM_CLK1** [2:0] 0: Keep 1: CLR bits
26:24		GPIO30	**Bitwise CLR of Aux mode of CAM_CLK0**
22:20		GPIO29	**Bitwise CLR of Aux mode of CAM_PDN1**
18:16		GPIO28	**Bitwise CLR of Aux mode of CAM_PDN0**
14:12		GPIO27	**Bitwise CLR of Aux mode of CSI2_L2N_T1C**
10:8		GPIO26	**Bitwise CLR of Aux mode of CSI2_L2P_T1B**
6:4		GPIO25	**Bitwise CLR of Aux mode of CSI2_L1N_T1A**
2:0		GPIO24	**Bitwise CLR of Aux mode of CSI2_L1P_T0C**

10005348 GPIO_MODE4_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 39				GPIO 38				GPIO37				GPIO36		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO35				GPIO34				GPIO33				GPIO32		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO39	**Bitwise CLR of Aux mode of DPI_D0** [2:0] 0: Keep 1: CLR bits
26:24		GPIO38	**Bitwise CLR of Aux mode of SDA0**
22:20		GPIO37	**Bitwise CLR of Aux mode of SCL0**
18:16		GPIO36	**Bitwise CLR of Aux mode of CAM_CLK2**
14:12		GPIO35	**Bitwise CLR of Aux mode of CAM_RST2**
10:8		GPIO34	**Bitwise CLR of Aux mode of CAM_PDN2**
6:4		GPIO33	**Bitwise CLR of Aux mode of CAM_RST1**
2:0		GPIO32	**Bitwise CLR of Aux mode of CAM_RST0**

10005358 GPIO_MODE5_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 47				GPIO 46				GPIO45				GPIO44		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO43				GPIO42				GPIO41				GPIO40		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO47	**Bitwise CLR of Aux mode of DPI_D8** [2:0] 0: Keep 1: CLR bits
26:24		GPIO46	**Bitwise CLR of Aux mode of DPI_D7**
22:20		GPIO45	**Bitwise CLR of Aux mode of DPI_D6**
18:16		GPIO44	**Bitwise CLR of Aux mode of DPI_D5**
14:12		GPIO43	**Bitwise CLR of Aux mode of DPI_D4**
10:8		GPIO42	**Bitwise CLR of Aux mode of DPI_D3**
6:4		GPIO41	**Bitwise CLR of Aux mode of DPI_D2**
2:0		GPIO40	**Bitwise CLR of Aux mode of DPI_D1**

10005368 GPIO_MODE6_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 55				GPIO 54				GPIO53				GPIO52		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO51				GPIO50				GPIO49				GPIO48		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO55	**Bitwise CLR of Aux mode of SCL1** [2:0] 0: Keep 1: CLR bits
26:24		GPIO54	**Bitwise CLR of Aux mode of DPI_VSYNC**
22:20		GPIO53	**Bitwise CLR of Aux mode of DPI_HSYNC**
18:16		GPIO52	**Bitwise CLR of Aux mode of DPI_CK**
14:12		GPIO51	**Bitwise CLR of Aux mode of DPI_DE**
10:8		GPIO50	**Bitwise CLR of Aux mode of DPI_D11**
6:4		GPIO49	**Bitwise CLR of Aux mode of DPI_D10**
2:0		GPIO48	**Bitwise CLR of Aux mode of DPI_D9**

10005378 GPIO_MODE7_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 63				GPIO 62				GPIO61				GPIO60		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO59				GPIO58				GPIO57				GPIO56		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO63	**Bitwise CLR of Aux mode of EINT2** [2:0] 0: Keep 1: CLR bits
26:24		GPIO62	**Bitwise CLR of Aux mode of EINT1**
22:20		GPIO61	**Bitwise CLR of Aux mode of EINT0**
18:16		GPIO60	**Bitwise CLR of Aux mode of SPI0_CS**
14:12		GPIO59	**Bitwise CLR of Aux mode of SPI0_MO**
10:8		GPIO58	**Bitwise CLR of Aux mode of SPI0_MI**
6:4		GPIO57	**Bitwise CLR of Aux mode of SPI0_CK**
2:0		GPIO56	**Bitwise CLR of Aux mode of SDA1**

10005388 GPIO_MODE8_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 71				GPIO 70				GPIO69				GPIO68		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO67				GPIO66				GPIO65				GPIO64		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO71	**Bitwise CLR of Aux mode of I2S0_MCK** [2:0] 0: Keep 1: CLR bits
26:24		GPIO70	**Bitwise CLR of Aux mode of I2S0_BCK**
22:20		GPIO69	**Bitwise CLR of Aux mode of I2S0_LRCK**
18:16		GPIO68	**Bitwise CLR of Aux mode of EINT7**
14:12		GPIO67	**Bitwise CLR of Aux mode of EINT6**
10:8		GPIO66	**Bitwise CLR of Aux mode of EINT5**
6:4		GPIO65	**Bitwise CLR of Aux mode of EINT4**
2:0		GPIO64	**Bitwise CLR of Aux mode of EINT3**

10005398 GPIO_MODE9_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 79				GPIO 78				GPIO77				GPIO76		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO75				GPIO74				GPIO73				GPIO72		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO79	**Bitwise CLR of Aux mode of CONN_WB_PTA** [2:0] 0: Keep 1: CLR bits
26:24		GPIO78	**Bitwise CLR of Aux mode of CONN_TOP_DATA**
22:20		GPIO77	**Bitwise CLR of Aux mode of CONN_TOP_CLK**
18:16		GPIO76	**Bitwise CLR of Aux mode of CONN_HRST_B**
14:12		GPIO75	**Bitwise CLR of Aux mode of SDA3**
10:8		GPIO74	**Bitwise CLR of Aux mode of SCL3**
6:4		GPIO73	**Bitwise CLR of Aux mode of I2S3_DO**
2:0		GPIO72	**Bitwise CLR of Aux mode of I2S0_DI**

100053A8 GPIO_MODE10_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 87				GPIO 86				GPIO85				GPIO84		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO83				GPIO82				GPIO81				GPIO80		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO87	**Bitwise CLR of Aux mode of EINT10** [2:0] 0: Keep 1: CLR bits
26:24		GPIO86	**Bitwise CLR of Aux mode of EINT9**
22:20		GPIO85	**Bitwise CLR of Aux mode of EINT8**
18:16		GPIO84	**Bitwise CLR of Aux mode of CONN_BT_DATA**
14:12		GPIO83	**Bitwise CLR of Aux mode of CONN_BT_CLK**
10:8		GPIO82	**Bitwise CLR of Aux mode of CONN_WF_CTRL2**
6:4		GPIO81	**Bitwise CLR of Aux mode of CONN_WF_CTRL1**
2:0		GPIO80	**Bitwise CLR of Aux mode of CONN_WF_CTRL0**

100053B8 GPIO_MODE11_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 95				GPIO 94				GPIO93				GPIO92		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO91				GPIO90				GPIO89				GPIO88		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO95	**Bitwise CLR of Aux mode of SDA2** [2:0] 0: Keep 1: CLR bits
26:24		GPIO94	**Bitwise CLR of Aux mode of DRVBUS**
22:20		GPIO93	**Bitwise CLR of Aux mode of EINT16**
18:16		GPIO92	**Bitwise CLR of Aux mode of EINT15**
14:12		GPIO91	**Bitwise CLR of Aux mode of EINT14**
10:8		GPIO90	**Bitwise CLR of Aux mode of EINT13**
6:4		GPIO89	**Bitwise CLR of Aux mode of EINT12**
2:0		GPIO88	**Bitwise CLR of Aux mode of EINT11**

100053C8 GPIO_MODE12_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 103				GPIO 102				GPIO101				GPIO100		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO99				GPIO98				GPIO97				GPIO96		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO103	**Bitwise CLR of Aux mode of SRCLKENA1** [2:0] 0: Keep 1: CLR bits
26:24		GPIO102	**Bitwise CLR of Aux mode of SRCLKENA0**
22:20		GPIO101	**Bitwise CLR of Aux mode of SRCLKENAI1**
18:16		GPIO100	**Bitwise CLR of Aux mode of SRCLKENAI0**
14:12		GPIO99	**Bitwise CLR of Aux mode of RTC32K_CK**
10:8		GPIO98	**Bitwise CLR of Aux mode of UTXD0**
6:4		GPIO97	**Bitwise CLR of Aux mode of URXD0**
2:0		GPIO96	**Bitwise CLR of Aux mode of SCL2**

100053D8 GPIO_MODE13_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 111				GPIO 110				GPIO109				GPIO108		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO107				GPIO106				GPIO105				GPIO104		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO111	**Bitwise CLR of Aux mode of KPCOL2** [2:0] 0: Keep 1: CLR bits
26:24		GPIO110	**Bitwise CLR of Aux mode of KPCOL1**
22:20		GPIO109	**Bitwise CLR of Aux mode of KPCOL0**
18:16		GPIO108	**Bitwise CLR of Aux mode of KPROW2**
14:12		GPIO107	**Bitwise CLR of Aux mode of KPROW1**
10:8		GPIO106	**Bitwise CLR of Aux mode of KPROW0**
6:4		GPIO105	**Bitwise CLR of Aux mode of WATCHDOG**
2:0		GPIO104	**Bitwise CLR of Aux mode of SYSRSTB**

100053E8 GPIO_MODE14_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 119				GPIO 118				GPIO117				GPIO116		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO115				GPIO114				GPIO113				GPIO112		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO119	**Bitwise CLR of Aux mode of MSDC0_DAT5** [2:0] 0: Keep 1: CLR bits
26:24		GPIO118	**Bitwise CLR of Aux mode of MSDC0_DAT4**
22:20		GPIO117	**Bitwise CLR of Aux mode of MSDC0_DAT3**
18:16		GPIO116	**Bitwise CLR of Aux mode of MSDC0_DAT2**
14:12		GPIO115	**Bitwise CLR of Aux mode of MSDC0_DAT1**
10:8		GPIO114	**Bitwise CLR of Aux mode of MSDC0_DAT0**
6:4		GPIO113	**Bitwise CLR of Aux mode of INT_SIM2**
2:0		GPIO112	**Bitwise CLR of Aux mode of INT_SIM1**

100053F8 GPIO_MODE15_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 127				GPIO 126				GPIO125				GPIO124		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO123				GPIO122				GPIO121				GPIO120		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO127	**Bitwise CLR of Aux mode of SIM1_SRST** [2:0] 0: Keep 1: CLR bits
26:24		GPIO126	**Bitwise CLR of Aux mode of SIM1_SCLK**
22:20		GPIO125	**Bitwise CLR of Aux mode of MSDC0_RSTB**
18:16		GPIO124	**Bitwise CLR of Aux mode of MSDC0_DSL**
14:12		GPIO123	**Bitwise CLR of Aux mode of MSDC0_CLK**
10:8		GPIO122	**Bitwise CLR of Aux mode of MSDC0_CMD**
6:4		GPIO121	**Bitwise CLR of Aux mode of MSDC0_DAT7**
2:0		GPIO120	**Bitwise CLR of Aux mode of MSDC0_DAT6**

10005408 GPIO_MODE16_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 135				GPIO 134				GPIO133				GPIO132		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO131				GPIO130				GPIO129				GPIO128		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO135	**Bitwise CLR of Aux mode of TDM_LRCK** [2:0] 0: Keep 1: CLR bits
26:24		GPIO134	**Bitwise CLR of Aux mode of MSDC1_CLK**
22:20		GPIO133	**Bitwise CLR of Aux mode of MSDC1_DAT3**
18:16		GPIO132	**Bitwise CLR of Aux mode of MSDC1_DAT2**
14:12		GPIO131	**Bitwise CLR of Aux mode of MSDC1_DAT1**
10:8		GPIO130	**Bitwise CLR of Aux mode of MSDC1_DAT0**
6:4		GPIO129	**Bitwise CLR of Aux mode of MSDC1_CMD**
2:0		GPIO128	**Bitwise CLR of Aux mode of SIM1_SIO**

10005418 GPIO_MODE17_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 143				GPIO 142				GPIO141				GPIO140		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO139				GPIO138				GPIO137				GPIO136		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO143	**Bitwise CLR of Aux mode of PWRAP_SPI0_MO** [2:0] 0: Keep 1: CLR bits
26:24		GPIO142	**Bitwise CLR of Aux mode of PWRAP_SPI0_MI**
22:20		GPIO141	**Bitwise CLR of Aux mode of TDM_DATA3**
18:16		GPIO140	**Bitwise CLR of Aux mode of TDM_DATA2**
14:12		GPIO139	**Bitwise CLR of Aux mode of TDM_DATA1**
10:8		GPIO138	**Bitwise CLR of Aux mode of TDM_DATA0**
6:4		GPIO137	**Bitwise CLR of Aux mode of TDM_MCK**
2:0		GPIO136	**Bitwise CLR of Aux mode of TDM_BCK**

10005428 GPIO_MODE18_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 151				GPIO 150				GPIO149				GPIO148		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO147				GPIO146				GPIO145				GPIO144		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO151	**Bitwise CLR of Aux mode of SCL6** [2:0] 0: Keep 1: CLR bits
26:24		GPIO150	**Bitwise CLR of Aux mode of ANC_DAT_MOSI**
22:20		GPIO149	**Bitwise CLR of Aux mode of VOW_CLK_MISO**
18:16		GPIO148	**Bitwise CLR of Aux mode of AUD_DAT_MOSI**
14:12		GPIO147	**Bitwise CLR of Aux mode of AUD_DAT_MISO**
10:8		GPIO146	**Bitwise CLR of Aux mode of AUD_CLK_MOSI**
6:4		GPIO145	**Bitwise CLR of Aux mode of PWRAP_SPI0_CSN**
2:0		GPIO144	**Bitwise CLR of Aux mode of PWRAP_SPI0_CK**

10005438 GPIO_MODE19_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 159				GPIO 158				GPIO157				GPIO156		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO155				GPIO154				GPIO153				GPIO152		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO159	**Bitwise CLR of Aux mode of TDN0** [2:0] 0: Keep 1: CLR bits
26:24		GPIO158	**Bitwise CLR of Aux mode of TDP0**
22:20		GPIO157	**Bitwise CLR of Aux mode of SIM2_SIO**
18:16		GPIO156	**Bitwise CLR of Aux mode of SIM2_SRST**
14:12		GPIO155	**Bitwise CLR of Aux mode of SIM2_SCLK**
10:8		GPIO154	**Bitwise CLR of Aux mode of SDA7**
6:4		GPIO153	**Bitwise CLR of Aux mode of SCL7**
2:0		GPIO152	**Bitwise CLR of Aux mode of SDA6**

10005448 GPIO_MODE20_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 167				GPIO 166				GPIO165				GPIO164		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO163				GPIO162				GPIO161				GPIO160		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO167	**Bitwise CLR of Aux mode of TDN3** [2:0] 0: Keep 1: CLR bits
26:24		GPIO166	**Bitwise CLR of Aux mode of TDP3**
22:20		GPIO165	**Bitwise CLR of Aux mode of TDN2**
18:16		GPIO164	**Bitwise CLR of Aux mode of TDP2**
14:12		GPIO163	**Bitwise CLR of Aux mode of TCN**
10:8		GPIO162	**Bitwise CLR of Aux mode of TCP**
6:4		GPIO161	**Bitwise CLR of Aux mode of TDN1**
2:0		GPIO160	**Bitwise CLR of Aux mode of TDP1**

10005458 GPIO_MODE21_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 175				GPIO 174				GPIO173				GPIO172		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO171				GPIO170				GPIO169				GPIO168		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO175	**Bitwise CLR of Aux mode of TDN2_A** [2:0] 0: Keep 1: CLR bits
26:24		GPIO174	**Bitwise CLR of Aux mode of TDP2_A**
22:20		GPIO173	**Bitwise CLR of Aux mode of TCN_A**
18:16		GPIO172	**Bitwise CLR of Aux mode of TCP_A**
14:12		GPIO171	**Bitwise CLR of Aux mode of TDN1_A**
10:8		GPIO170	**Bitwise CLR of Aux mode of TDP1_A**
6:4		GPIO169	**Bitwise CLR of Aux mode of TDN0_A**
2:0		GPIO168	**Bitwise CLR of Aux mode of TDP0_A**

10005468 GPIO_MODE22_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 183				GPIO 182				GPIO181				GPIO180		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO179				GPIO178				GPIO177				GPIO176		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO183	**Bitwise CLR of Aux mode of RFICo_BSI_CK** [2:0] 0: Keep 1: CLR bits
26:24		GPIO182	**Bitwise CLR of Aux mode of TESTMODE**
22:20		GPIO181	**Bitwise CLR of Aux mode of IDDIG**
18:16		GPIO180	**Bitwise CLR of Aux mode of LCM_RST**
14:12		GPIO179	**Bitwise CLR of Aux mode of DSI_TE**
10:8		GPIO178	**Bitwise CLR of Aux mode of DISP_PWM**
6:4		GPIO177	**Bitwise CLR of Aux mode of TDN3_A**
2:0		GPIO176	**Bitwise CLR of Aux mode of TDP3_A**

10005478 GPIO_MODE23_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 191				GPIO 190				GPIO189				GPIO188		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO187				GPIO186				GPIO185				GPIO184		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO191	**Bitwise CLR of Aux mode of MISC_MIPI_DO_1** [2:0] 0: Keep 1: CLR bits
26:24		GPIO190	**Bitwise CLR of Aux mode of MISC_MIPI_CK_1**
22:20		GPIO189	**Bitwise CLR of Aux mode of MISC_MIPI_DO_0**
18:16		GPIO188	**Bitwise CLR of Aux mode of MISC_MIPI_CK_0**
14:12		GPIO187	**Bitwise CLR of Aux mode of RFICo_BSI_D2**
10:8		GPIO186	**Bitwise CLR of Aux mode of RFICo_BSI_D1**
6:4		GPIO185	**Bitwise CLR of Aux mode of RFICo_BSI_Do**
2:0		GPIO184	**Bitwise CLR of Aux mode of RFICo_BSI_EN**

10005488 GPIO_MODE24_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 199				GPIO 198				GPIO197				GPIO196		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO195				GPIO194				GPIO193				GPIO192		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO199	**Bitwise CLR of Aux mode of BPI_BUS11** [2:0] 0: Keep 1: CLR bits
26:24		GPIO198	**Bitwise CLR of Aux mode of BPI_BUS10**
22:20		GPIO197	**Bitwise CLR of Aux mode of BPI_BUS9**
18:16		GPIO196	**Bitwise CLR of Aux mode of BPI_BUS8**
14:12		GPIO195	**Bitwise CLR of Aux mode of BPI_BUS7**
10:8		GPIO194	**Bitwise CLR of Aux mode of BPI_BUS6**
6:4		GPIO193	**Bitwise CLR of Aux mode of BPI_BUS5**
2:0		GPIO192	**Bitwise CLR of Aux mode of BPI_BUS4**

10005498 GPIO_MODE25_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 207				GPIO 206				GPIO205				GPIO204		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO203				GPIO202				GPIO201				GPIO200		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO207	**Bitwise CLR of Aux mode of BPI_BUS19_SWP1** [2:0] 0: Keep 1: CLR bits
26:24		GPIO206	**Bitwise CLR of Aux mode of BPI_BUS18_SWP0**
22:20		GPIO205	**Bitwise CLR of Aux mode of BPI_BUS17_VM1**
18:16		GPIO204	**Bitwise CLR of Aux mode of BPI_BUS16_VM0**
14:12		GPIO203	**Bitwise CLR of Aux mode of BPI_BUS15_ANT3**
10:8		GPIO202	**Bitwise CLR of Aux mode of BPI_BUS14_ANT2**
6:4		GPIO201	**Bitwise CLR of Aux mode of BPI_BUS13_ANT1**
2:0		GPIO200	**Bitwise CLR of Aux mode of BPI_BUS12_ANT0**

100054A8 GPIO_MODE26_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 215				GPIO 214				GPIO213				GPIO212		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO211				GPIO210				GPIO209				GPIO208		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO215	**Bitwise CLR of Aux mode of BPI_BUS3** [2:0] 0: Keep 1: CLR bits
26:24		GPIO214	**Bitwise CLR of Aux mode of BPI_BUS2**
22:20		GPIO213	**Bitwise CLR of Aux mode of BPI_BUS1**
18:16		GPIO212	**Bitwise CLR of Aux mode of BPI_BUS0**
14:12		GPIO211	**Bitwise CLR of Aux mode of BPI_BUS23_DET1**
10:8		GPIO210	**Bitwise CLR of Aux mode of BPI_BUS22_DET0**
6:4		GPIO209	**Bitwise CLR of Aux mode of BPI_BUS21_SWP3**
2:0		GPIO208	**Bitwise CLR of Aux mode of BPI_BUS20_SWP2**

100054B8 GPIO_MODE27_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 223				GPIO 222				GPIO221				GPIO220		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO219				GPIO218				GPIO217				GPIO216		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO223	**Bitwise CLR of Aux mode of WF_QN** [2:0] 0: Keep 1: CLR bits
26:24		GPIO222	**Bitwise CLR of Aux mode of WF_QP**
22:20		GPIO221	**Bitwise CLR of Aux mode of WF_IN**
18:16		GPIO220	**Bitwise CLR of Aux mode of WF_IP**
14:12		GPIO219	**Bitwise CLR of Aux mode of MISC_MIPI_DO_3**
10:8		GPIO218	**Bitwise CLR of Aux mode of MISC_MIPI_CK_3**
6:4		GPIO217	**Bitwise CLR of Aux mode of MISC_MIPI_DO_2**
2:0		GPIO216	**Bitwise CLR of Aux mode of MISC_MIPI_CK_2**

100054C8 GPIO_MODE28_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 231				GPIO 230				GPIO229				GPIO228		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO227				GPIO226				GPIO225				GPIO224		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO231	**Bitwise CLR of Aux mode of GPS_QN** [2:0] 0: Keep 1: CLR bits
26:24		GPIO230	**Bitwise CLR of Aux mode of GPS_QP**
22:20		GPIO229	**Bitwise CLR of Aux mode of GPS_IN**
18:16		GPIO228	**Bitwise CLR of Aux mode of GPS_IP**
14:12		GPIO227	**Bitwise CLR of Aux mode of BT_QN**
10:8		GPIO226	**Bitwise CLR of Aux mode of BT_QP**
6:4		GPIO225	**Bitwise CLR of Aux mode of BT_IN**
2:0		GPIO224	**Bitwise CLR of Aux mode of BT_IP**

100054D8 GPIO_MODE29_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 239				GPIO 238				GPIO237				GPIO236		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO235				GPIO234				GPIO233				GPIO232		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO239	**Bitwise CLR of Aux mode of SCL4** [2:0] 0: Keep 1: CLR bits
26:24		GPIO238	**Bitwise CLR of Aux mode of SDA4**
22:20		GPIO237	**Bitwise CLR of Aux mode of SPI1_CS**
18:16		GPIO236	**Bitwise CLR of Aux mode of SPI1_MO**
14:12		GPIO235	**Bitwise CLR of Aux mode of SPI1_MI**
10:8		GPIO234	**Bitwise CLR of Aux mode of SPI1_CK**
6:4		GPIO233	**Bitwise CLR of Aux mode of UTXD1**
2:0		GPIO232	**Bitwise CLR of Aux mode of URXD1**

100054E8 GPIO_MODE30_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 247				GPIO 246				GPIO245				GPIO244		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO243				GPIO242				GPIO241				GPIO240		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO247	**Bitwise CLR of Aux mode of I2S1_BCK** [2:0] 0: Keep 1: CLR bits
26:24		GPIO246	**Bitwise CLR of Aux mode of I2S1_LRCK**
22:20		GPIO245	**Bitwise CLR of Aux mode of SPI2_CS**
18:16		GPIO244	**Bitwise CLR of Aux mode of SPI2_MO**
14:12		GPIO243	**Bitwise CLR of Aux mode of SPI2_MI**
10:8		GPIO242	**Bitwise CLR of Aux mode of SPI2_CK**
6:4		GPIO241	**Bitwise CLR of Aux mode of SCL5**
2:0		GPIO240	**Bitwise CLR of Aux mode of SDA5**

100054F8 GPIO_MODE31_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO 255				GPIO 254				GPIO253				GPIO252		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO251				GPIO250				GPIO249				GPIO248		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO255	**Bitwise CLR of Aux mode of AUD_INTN** [2:0] 0: Keep 1: CLR bits
26:24		GPIO254	**Bitwise CLR of Aux mode of I2S1_MCK**
22:20		GPIO253	**Bitwise CLR of Aux mode of SPI3_CS**
18:16		GPIO252	**Bitwise CLR of Aux mode of SPI3_CK**
14:12		GPIO251	**Bitwise CLR of Aux mode of SPI3_MO**
10:8		GPIO250	**Bitwise CLR of Aux mode of SPI3_MI**
6:4		GPIO249	**Bitwise CLR of Aux mode of I2S1_DO**
2:0		GPIO248	**Bitwise CLR of Aux mode of I2S2_DI**

10005508 GPIO_MODE32_CLR **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										GPIO 261				GPIO260		
Type										WO				WO		
Reset										0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO259				GPIO258				GPIO257				GPIO256		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
22:20		GPIO261	**Bitwise CLR of Aux mode of JTRST_B** [2:0] 0: Keep 1: CLR bits
18:16		GPIO260	**Bitwise CLR of Aux mode of JTDO**
14:12		GPIO259	**Bitwise CLR of Aux mode of JTDI**
10:8		GPIO258	**Bitwise CLR of Aux mode of JTCK**
6:4		GPIO257	**Bitwise CLR of Aux mode of JTMS**
2:0		GPIO256	**Bitwise CLR of Aux mode of AUD_PDN**

1000530C GPIO_MODE0_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO7				GPIO6				GPIO5				GPIO4			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO3				GPIO2				GPIO1				GPIO0			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO7	**Alternative way to set up Aux mode of CSI0B_L0N_T0B** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO6	**Alternative way to set up Aux mode of CSI0B_L0P_T0A**
23:20		GPIO5	**Alternative way to set up Aux mode of CSI0A_L2N_T1C**
19:16		GPIO4	**Alternative way to set up Aux mode of CSI0A_L2P_T1B**
15:12		GPIO3	**Alternative way to set up Aux mode of CSI0A_L1N_T1A**
11:8		GPIO2	**Alternative way to set up Aux mode of CSI0A_L1P_T0C**
7:4		GPIO1	**Alternative way to set up Aux mode of CSI0A_L0N_T0B**
3:0		GPIO0	**Alternative way to set up Aux mode of CSI0A_L0P_T0A**

1000531C GPIO_MODE1_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	GPIO15				GPIO14				GPIO13				GPIO12			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO11				GPIO10				GPIO9				GPIO8			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO15	**Alternative way to set up Aux mode of CSI1A_L2N_T1C** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO14	**Alternative way to set up Aux mode of CSI1A_L2P_T1B**
23:20		GPIO13	**Alternative way to set up Aux mode of CSI1A_L1N_T1A**
19:16		GPIO12	**Alternative way to set up Aux mode of CSI1A_L1P_T0C**
15:12		GPIO11	**Alternative way to set up Aux mode of CSI1A_L0N_T0B**
11:8		GPIO10	**Alternative way to set up Aux mode of CSI1A_L0P_T0A**
7:4		GPIO9	**Alternative way to set up Aux mode of CSI0B_L1N_T1A**
3:0		GPIO8	**Alternative way to set up Aux mode of CSI0B_L1P_T0C**

1000532C GPIO_MODE2_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO23				GPIO22				GPIO21				GPIO20			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO19				GPIO18				GPIO17				GPIO16			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO23	**Alternative way to set up Aux mode of CSI2_L0N_T0B** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO22	**Alternative way to set up Aux mode of CSI2_L0P_T0A**
23:20		GPIO21	**Alternative way to set up Aux mode of CSI1B_L2N_T1C**
19:16		GPIO20	**Alternative way to set up Aux mode of CSI1B_L2P_T1B**
15:12		GPIO19	**Alternative way to set up Aux mode of**

Bit(s)	Mnemonic	Name	Description
			CSI1B_L1N_T1A
11:8		GPIO18	**Alternative way to set up Aux mode of CSI1B_L1P_T0C**
7:4		GPIO17	**Alternative way to set up Aux mode of CSI1B_L0N_T0B**
3:0		GPIO16	**Alternative way to set up Aux mode of CSI1B_L0P_T0A**

1000533C GPIO_MODE3_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31				GPIO30				GPIO29				GPIO28			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO27				GPIO26				GPIO25				GPIO24			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO31	**Alternative way to set up Aux mode of CAM_CLK1** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO30	**Alternative way to set up Aux mode of CAM_CLK0**
23:20		GPIO29	**Alternative way to set up Aux mode of CAM_PDN1**
19:16		GPIO28	**Alternative way to set up Aux mode of CAM_PDN0**
15:12		GPIO27	**Alternative way to set up Aux mode of CSI2_L2N_T1C**
11:8		GPIO26	**Alternative way to set up Aux mode of CSI2_L2P_T1B**
7:4		GPIO25	**Alternative way to set up Aux mode of CSI2_L1N_T1A**
3:0		GPIO24	**Alternative way to set up Aux mode of CSI2_L1P_T0C**

1000534C GPIO_MODE4_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO39				GPIO38				GPIO37				GPIO36			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO35				GPIO34				GPIO33				GPIO32			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO39	**Alternative way to set up Aux mode of DPI_D0** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO38	**Alternative way to set up Aux mode of SDA0**
23:20		GPIO37	**Alternative way to set up Aux mode of SCL0**
19:16		GPIO36	**Alternative way to set up Aux mode of CAM_CLK2**
15:12		GPIO35	**Alternative way to set up Aux mode of CAM_RST2**
11:8		GPIO34	**Alternative way to set up Aux mode of CAM_PDN2**
7:4		GPIO33	**Alternative way to set up Aux mode of CAM_RST1**
3:0		GPIO32	**Alternative way to set up Aux mode of CAM_RST0**

1000535C GPIO_MODE5_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO47				GPIO46				GPIO45				GPIO44			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO43				GPIO42				GPIO41				GPIO40			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO47	**Alternative way to set up Aux mode of DPI_D8** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO46	**Alternative way to set up Aux mode of DPI_D7**
23:20		GPIO45	**Alternative way to set up Aux mode of DPI_D6**
19:16		GPIO44	**Alternative way to set up Aux mode of DPI_D5**
15:12		GPIO43	**Alternative way to set up Aux mode of DPI_D4**
11:8		GPIO42	**Alternative way to set up Aux mode of DPI_D3**
7:4		GPIO41	**Alternative way to set up Aux mode of DPI_D2**
3:0		GPIO40	**Alternative way to set up Aux mode of DPI_D1**

1000536C GPIO_MODE6_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO55				GPIO54				GPIO53				GPIO52			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO51				GPIO50				GPIO49				GPIO48			

Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO55	**Alternative way to set up Aux mode of SCL1** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO54	**Alternative way to set up Aux mode of DPI_VSYNC**
23:20		GPIO53	**Alternative way to set up Aux mode of DPI_HSYNC**
19:16		GPIO52	**Alternative way to set up Aux mode of DPI_CK**
15:12		GPIO51	**Alternative way to set up Aux mode of DPI_DE**
11:8		GPIO50	**Alternative way to set up Aux mode of DPI_D11**
7:4		GPIO49	**Alternative way to set up Aux mode of DPI_D10**
3:0		GPIO48	**Alternative way to set up Aux mode of DPI_D9**

1000537C GPIO_MODE7_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO63				GPIO62				GPIO61				GPIO60			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO59				GPIO58				GPIO57				GPIO56			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO63	**Alternative way to set up Aux mode of EINT2** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO62	**Alternative way to set up Aux mode of EINT1**
23:20		GPIO61	**Alternative way to set up Aux mode of EINT0**
19:16		GPIO60	**Alternative way to set up Aux mode of SPI0_CS**
15:12		GPIO59	**Alternative way to set up Aux mode of SPI0_MO**
11:8		GPIO58	**Alternative way to set up Aux mode of SPI0_MI**
7:4		GPIO57	**Alternative way to set up Aux mode of SPI0_CK**
3:0		GPIO56	**Alternative way to set up Aux mode of SDA1**

1000538C GPIO_MODE8_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO71				GPIO70				GPIO69				GPIO68			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	GPIO67				GPIO66				GPIO65				GPIO64			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO71	**Alternative way to set up Aux mode of I2S0_MCK** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO70	**Alternative way to set up Aux mode of I2S0_BCK**
23:20		GPIO69	**Alternative way to set up Aux mode of I2S0_LRCK**
19:16		GPIO68	**Alternative way to set up Aux mode of EINT7**
15:12		GPIO67	**Alternative way to set up Aux mode of EINT6**
11:8		GPIO66	**Alternative way to set up Aux mode of EINT5**
7:4		GPIO65	**Alternative way to set up Aux mode of EINT4**
3:0		GPIO64	**Alternative way to set up Aux mode of EINT3**

1000539C GPIO_MODE9_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO79				GPIO78				GPIO77				GPIO76			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO75				GPIO74				GPIO73				GPIO72			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO79	**Alternative way to set up Aux mode of CONN_WB_PTA** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO78	**Alternative way to set up Aux mode of CONN_TOP_DATA**
23:20		GPIO77	**Alternative way to set up Aux mode of CONN_TOP_CLK**
19:16		GPIO76	**Alternative way to set up Aux mode of CONN_HRST_B**
15:12		GPIO75	**Alternative way to set up Aux mode of SDA3**
11:8		GPIO74	**Alternative way to set up Aux mode of SCL3**
7:4		GPIO73	**Alternative way to set up Aux mode of I2S3_DO**
3:0		GPIO72	**Alternative way to set up Aux mode of I2S0_DI**

100053AC GPIO_MODE10_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	GPIO87				GPIO86				GPIO85				GPIO84			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO83				GPIO82				GPIO81				GPIO80			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO87	**Alternative way to set up Aux mode of EINT10** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO86	**Alternative way to set up Aux mode of EINT9**
23:20		GPIO85	**Alternative way to set up Aux mode of EINT8**
19:16		GPIO84	**Alternative way to set up Aux mode of CONN_BT_DATA**
15:12		GPIO83	**Alternative way to set up Aux mode of CONN_BT_CLK**
11:8		GPIO82	**Alternative way to set up Aux mode of CONN_WF_CTRL2**
7:4		GPIO81	**Alternative way to set up Aux mode of CONN_WF_CTRL1**
3:0		GPIO80	**Alternative way to set up Aux mode of CONN_WF_CTRL0**

100053BC GPIO_MODE11_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO95				GPIO94				GPIO93				GPIO92			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO91				GPIO90				GPIO89				GPIO88			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO95	**Alternative way to set up Aux mode of SDA2** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO94	**Alternative way to set up Aux mode of DRVBUS**
23:20		GPIO93	**Alternative way to set up Aux mode of EINT16**
19:16		GPIO92	**Alternative way to set up Aux mode of EINT15**
15:12		GPIO91	**Alternative way to set up Aux mode of EINT14**
11:8		GPIO90	**Alternative way to set up Aux mode of EINT13**
7:4		GPIO89	**Alternative way to set up Aux mode of EINT12**
3:0		GPIO88	**Alternative way to set up Aux mode of EINT11**

100053CC GPIO_MODE12_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO103				GPIO102				GPIO101				GPIO100			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO99				GPIO98				GPIO97				GPIO96			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO103	**Alternative way to set up Aux mode of SRCLKENA1** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO102	**Alternative way to set up Aux mode of SRCLKENA0**
23:20		GPIO101	**Alternative way to set up Aux mode of SRCLKENAI1**
19:16		GPIO100	**Alternative way to set up Aux mode of SRCLKENAI0**
15:12		GPIO99	**Alternative way to set up Aux mode of RTC32K_CK**
11:8		GPIO98	**Alternative way to set up Aux mode of UTXD0**
7:4		GPIO97	**Alternative way to set up Aux mode of URXD0**
3:0		GPIO96	**Alternative way to set up Aux mode of SCL2**

100053DC GPIO_MODE13_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO111				GPIO110				GPIO109				GPIO108			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO107				GPIO106				GPIO105				GPIO104			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO111	**Alternative way to set up Aux mode of KPCOL2** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO110	**Alternative way to set up Aux mode of KPCOL1**
23:20		GPIO109	**Alternative way to set up Aux mode of KPCOL0**
19:16		GPIO108	**Alternative way to set up Aux mode of KPROW2**
15:12		GPIO107	**Alternative way to set up Aux mode of KPROW1**
11:8		GPIO106	**Alternative way to set up Aux mode of KPROW0**
7:4		GPIO105	**Alternative way to set up Aux mode of**

Bit(s)	Mnemonic	Name	Description
3:0		GPIO104	**WATCHDOG** **Alternative way to set up Aux mode of SYSRSTB**

100053EC GPIO_MODE14_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO119				GPIO118				GPIO117				GPIO116			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO115				GPIO114				GPIO113				GPIO112			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO119	**Alternative way to set up Aux mode of MSDC0_DAT5** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO118	**Alternative way to set up Aux mode of MSDC0_DAT4**
23:20		GPIO117	**Alternative way to set up Aux mode of MSDC0_DAT3**
19:16		GPIO116	**Alternative way to set up Aux mode of MSDC0_DAT2**
15:12		GPIO115	**Alternative way to set up Aux mode of MSDC0_DAT1**
11:8		GPIO114	**Alternative way to set up Aux mode of MSDC0_DAT0**
7:4		GPIO113	**Alternative way to set up Aux mode of INT_SIM2**
3:0		GPIO112	**Alternative way to set up Aux mode of INT_SIM1**

100053FC GPIO_MODE15_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO127				GPIO126				GPIO125				GPIO124			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO123				GPIO122				GPIO121				GPIO120			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO127	**Alternative way to set up Aux mode of SIM1_SRST** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set.

Bit(s)	Mnemonic	Name	Description
			1: Mode is set.
27:24		GPIO126	**Alternative way to set up Aux mode of SIM1_SCLK**
23:20		GPIO125	**Alternative way to set up Aux mode of MSDC0_RSTB**
19:16		GPIO124	**Alternative way to set up Aux mode of MSDC0_DSL**
15:12		GPIO123	**Alternative way to set up Aux mode of MSDC0_CLK**
11:8		GPIO122	**Alternative way to set up Aux mode of MSDC0_CMD**
7:4		GPIO121	**Alternative way to set up Aux mode of MSDC0_DAT7**
3:0		GPIO120	**Alternative way to set up Aux mode of MSDC0_DAT6**

1000540C GPIO_MODE16_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO135				GPIO134				GPIO133				GPIO132			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO131				GPIO130				GPIO129				GPIO128			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO135	**Alternative way to set up Aux mode of TDM_LRCK** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO134	**Alternative way to set up Aux mode of MSDC1_CLK**
23:20		GPIO133	**Alternative way to set up Aux mode of MSDC1_DAT3**
19:16		GPIO132	**Alternative way to set up Aux mode of MSDC1_DAT2**
15:12		GPIO131	**Alternative way to set up Aux mode of MSDC1_DAT1**
11:8		GPIO130	**Alternative way to set up Aux mode of MSDC1_DAT0**
7:4		GPIO129	**Alternative way to set up Aux mode of MSDC1_CMD**
3:0		GPIO128	**Alternative way to set up Aux mode of SIM1_SIO**

1000541C GPIO_MODE17_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO143				GPIO142				GPIO141				GPIO140			
Type	WO				WO				WO				WO			

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO139				GPIO138				GPIO137				GPIO136			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO143	**Alternative way to set up Aux mode of PWRAP_SPI0_MO** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO142	**Alternative way to set up Aux mode of PWRAP_SPI0_MI**
23:20		GPIO141	**Alternative way to set up Aux mode of TDM_DATA3**
19:16		GPIO140	**Alternative way to set up Aux mode of TDM_DATA2**
15:12		GPIO139	**Alternative way to set up Aux mode of TDM_DATA1**
11:8		GPIO138	**Alternative way to set up Aux mode of TDM_DATA0**
7:4		GPIO137	**Alternative way to set up Aux mode of TDM_MCK**
3:0		GPIO136	**Alternative way to set up Aux mode of TDM_BCK**

1000542C GPIO_MODE18_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO151				GPIO150				GPIO149				GPIO148			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO147				GPIO146				GPIO145				GPIO144			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO151	**Alternative way to set up Aux mode of SCL6** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO150	**Alternative way to set up Aux mode of ANC_DAT_MOSI**
23:20		GPIO149	**Alternative way to set up Aux mode of VOW_CLK_MISO**
19:16		GPIO148	**Alternative way to set up Aux mode of AUD_DAT_MOSI**
15:12		GPIO147	**Alternative way to set up Aux mode of AUD_DAT_MISO**
11:8		GPIO146	**Alternative way to set up Aux mode of AUD_CLK_MOSI**
7:4		GPIO145	**Alternative way to set up Aux mode of**

Bit(s)	Mnemonic	Name	Description
3:0		GPIO144	**PWRAP_SPI0_CSN** **Alternative way to set up Aux mode of PWRAP_SPI0_CK**

1000543C GPIO_MODE19_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO159				GPIO158				GPIO157				GPIO156			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO155				GPIO154				GPIO153				GPIO152			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO159	**Alternative way to set up Aux mode of TDN0** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO158	**Alternative way to set up Aux mode of TDP0**
23:20		GPIO157	**Alternative way to set up Aux mode of SIM2_SIO**
19:16		GPIO156	**Alternative way to set up Aux mode of SIM2_SRST**
15:12		GPIO155	**Alternative way to set up Aux mode of SIM2_SCLK**
11:8		GPIO154	**Alternative way to set up Aux mode of SDA7**
7:4		GPIO153	**Alternative way to set up Aux mode of SCL7**
3:0		GPIO152	**Alternative way to set up Aux mode of SDA6**

1000544C GPIO_MODE20_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO167				GPIO166				GPIO165				GPIO164			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO163				GPIO162				GPIO161				GPIO160			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO167	**Alternative way to set up Aux mode of TDN3** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO166	**Alternative way to set up Aux mode of TDP3**
23:20		GPIO165	**Alternative way to set up Aux mode of TDN2**

Bit(s)	Mnemonic	Name	Description
19:16		GPIO164	**Alternative way to set up Aux mode of TDP2**
15:12		GPIO163	**Alternative way to set up Aux mode of TCN**
11:8		GPIO162	**Alternative way to set up Aux mode of TCP**
7:4		GPIO161	**Alternative way to set up Aux mode of TDN1**
3:0		GPIO160	**Alternative way to set up Aux mode of TDP1**

1000545C GPIO_MODE21_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO175				GPIO174				GPIO173				GPIO172			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO171				GPIO170				GPIO169				GPIO168			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO175	**Alternative way to set up Aux mode of TDN2_A** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO174	**Alternative way to set up Aux mode of TDP2_A**
23:20		GPIO173	**Alternative way to set up Aux mode of TCN_A**
19:16		GPIO172	**Alternative way to set up Aux mode of TCP_A**
15:12		GPIO171	**Alternative way to set up Aux mode of TDN1_A**
11:8		GPIO170	**Alternative way to set up Aux mode of TDP1_A**
7:4		GPIO169	**Alternative way to set up Aux mode of TDN0_A**
3:0		GPIO168	**Alternative way to set up Aux mode of TDP0_A**

1000546C GPIO_MODE22_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO183				GPIO182				GPIO181				GPIO180			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO179				GPIO178				GPIO177				GPIO176			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO183	**Alternative way to set up Aux mode of RFIC0_BSI_CK** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.

Bit(s)	Mnemonic	Name	Description
27:24		GPIO182	**Alternative way to set up Aux mode of TESTMODE**
23:20		GPIO181	**Alternative way to set up Aux mode of IDDIG**
19:16		GPIO180	**Alternative way to set up Aux mode of LCM_RST**
15:12		GPIO179	**Alternative way to set up Aux mode of DSI_TE**
11:8		GPIO178	**Alternative way to set up Aux mode of DISP_PWM**
7:4		GPIO177	**Alternative way to set up Aux mode of TDN3_A**
3:0		GPIO176	**Alternative way to set up Aux mode of TDP3_A**

1000547C GPIO_MODE23_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO191				GPIO190				GPIO189				GPIO188			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO187				GPIO186				GPIO185				GPIO184			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO191	**Alternative way to set up Aux mode of MISC_MIPI_DO_1** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO190	**Alternative way to set up Aux mode of MISC_MIPI_CK_1**
23:20		GPIO189	**Alternative way to set up Aux mode of MISC_MIPI_DO_0**
19:16		GPIO188	**Alternative way to set up Aux mode of MISC_MIPI_CK_0**
15:12		GPIO187	**Alternative way to set up Aux mode of RFIC0_BSI_D2**
11:8		GPIO186	**Alternative way to set up Aux mode of RFIC0_BSI_D1**
7:4		GPIO185	**Alternative way to set up Aux mode of RFIC0_BSI_D0**
3:0		GPIO184	**Alternative way to set up Aux mode of RFIC0_BSI_EN**

1000548C GPIO_MODE24_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO199				GPIO198				GPIO197				GPIO196			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO195				GPIO194				GPIO193				GPIO192			
Type	WO				WO				WO				WO			

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO199	**Alternative way to set up Aux mode of BPI_BUS11** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO198	**Alternative way to set up Aux mode of BPI_BUS10**
23:20		GPIO197	**Alternative way to set up Aux mode of BPI_BUS9**
19:16		GPIO196	**Alternative way to set up Aux mode of BPI_BUS8**
15:12		GPIO195	**Alternative way to set up Aux mode of BPI_BUS7**
11:8		GPIO194	**Alternative way to set up Aux mode of BPI_BUS6**
7:4		GPIO193	**Alternative way to set up Aux mode of BPI_BUS5**
3:0		GPIO192	**Alternative way to set up Aux mode of BPI_BUS4**

1000549C GPIO_MODE25_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO207				GPIO206				GPIO205				GPIO204			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO203				GPIO202				GPIO201				GPIO200			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO207	**Alternative way to set up Aux mode of BPI_BUS19_SWP1** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO206	**Alternative way to set up Aux mode of BPI_BUS18_SWP0**
23:20		GPIO205	**Alternative way to set up Aux mode of BPI_BUS17_VM1**
19:16		GPIO204	**Alternative way to set up Aux mode of BPI_BUS16_VM0**
15:12		GPIO203	**Alternative way to set up Aux mode of BPI_BUS15_ANT3**
11:8		GPIO202	**Alternative way to set up Aux mode of BPI_BUS14_ANT2**
7:4		GPIO201	**Alternative way to set up Aux mode of BPI_BUS13_ANT1**
3:0		GPIO200	**Alternative way to set up Aux mode of BPI_BUS12_ANT0**

100054AC GPIO_MODE26_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO215				GPIO214				GPIO213				GPIO212			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO211				GPIO210				GPIO209				GPIO208			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO215	**Alternative way to set up Aux mode of BPI_BUS3** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO214	**Alternative way to set up Aux mode of BPI_BUS2**
23:20		GPIO213	**Alternative way to set up Aux mode of BPI_BUS1**
19:16		GPIO212	**Alternative way to set up Aux mode of BPI_BUS0**
15:12		GPIO211	**Alternative way to set up Aux mode of BPI_BUS23_DET1**
11:8		GPIO210	**Alternative way to set up Aux mode of BPI_BUS22_DET0**
7:4		GPIO209	**Alternative way to set up Aux mode of BPI_BUS21_SWP3**
3:0		GPIO208	**Alternative way to set up Aux mode of BPI_BUS20_SWP2**

100054BC GPIO_MODE27_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO223				GPIO222				GPIO221				GPIO220			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO219				GPIO218				GPIO217				GPIO216			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO223	**Alternative way to set up Aux mode of WF_QN** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO222	**Alternative way to set up Aux mode of WF_QP**
23:20		GPIO221	**Alternative way to set up Aux mode of WF_IN**
19:16		GPIO220	**Alternative way to set up Aux mode of WF_IP**
15:12		GPIO219	**Alternative way to set up Aux mode of MISC_MIPI_DO_3**
11:8		GPIO218	**Alternative way to set up Aux mode of MISC_MIPI_CK_3**
7:4		GPIO217	**Alternative way to set up Aux mode of MISC_MIPI_DO_2**
3:0		GPIO216	**Alternative way to set up Aux mode of**

Bit(s)	Mnemonic	Name	Description
			MISC_MIPI_CK_2

100054CC GPIO_MODE28_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO231				GPIO230				GPIO229				GPIO228			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO227				GPIO226				GPIO225				GPIO224			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO231	**Alternative way to set up Aux mode of GPS_QN** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO230	**Alternative way to set up Aux mode of GPS_QP**
23:20		GPIO229	**Alternative way to set up Aux mode of GPS_IN**
19:16		GPIO228	**Alternative way to set up Aux mode of GPS_IP**
15:12		GPIO227	**Alternative way to set up Aux mode of BT_QN**
11:8		GPIO226	**Alternative way to set up Aux mode of BT_QP**
7:4		GPIO225	**Alternative way to set up Aux mode of BT_IN**
3:0		GPIO224	**Alternative way to set up Aux mode of BT_IP**

100054DC GPIO_MODE29_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO239				GPIO238				GPIO237				GPIO236			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO235				GPIO234				GPIO233				GPIO232			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO239	**Alternative way to set up Aux mode of SCL4** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO238	**Alternative way to set up Aux mode of SDA4**
23:20		GPIO237	**Alternative way to set up Aux mode of SPI1_CS**
19:16		GPIO236	**Alternative way to set up Aux mode of SPI1_MO**
15:12		GPIO235	**Alternative way to set up Aux mode of SPI1_MI**
11:8		GPIO234	**Alternative way to set up Aux mode of SPI1_CK**

Bit(s)	Mnemonic	Name	Description
7:4		GPIO233	**Alternative way to set up Aux mode of UTXD1**
3:0		GPIO232	**Alternative way to set up Aux mode of URXD1**

100054EC GPIO_MODE30_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO247				GPIO246				GPIO245				GPIO244			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO243				GPIO242				GPIO241				GPIO240			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO247	**Alternative way to set up Aux mode of I2S1_BCK** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO246	**Alternative way to set up Aux mode of I2S1_LRCK**
23:20		GPIO245	**Alternative way to set up Aux mode of SPI2_CS**
19:16		GPIO244	**Alternative way to set up Aux mode of SPI2_MO**
15:12		GPIO243	**Alternative way to set up Aux mode of SPI2_MI**
11:8		GPIO242	**Alternative way to set up Aux mode of SPI2_CK**
7:4		GPIO241	**Alternative way to set up Aux mode of SCL5**
3:0		GPIO240	**Alternative way to set up Aux mode of SDA5**

100054FC GPIO_MODE31_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO255				GPIO254				GPIO253				GPIO252			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO251				GPIO250				GPIO249				GPIO248			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		GPIO255	**Alternative way to set up Aux mode of AUD_INTN** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24		GPIO254	**Alternative way to set up Aux mode of I2S1_MCK**
23:20		GPIO253	**Alternative way to set up Aux mode of SPI3_CS**
19:16		GPIO252	**Alternative way to set up Aux mode of SPI3_CK**

Bit(s)	Mnemonic	Name	Description
15:12		GPIO251	**Alternative way to set up Aux mode of SPI3_MO**
11:8		GPIO250	**Alternative way to set up Aux mode of SPI3_MI**
7:4		GPIO249	**Alternative way to set up Aux mode of I2S1_DO**
3:0		GPIO248	**Alternative way to set up Aux mode of I2S2_DI**

1000550C GPIO_MODE32_MOD **GPIO Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									GPIO261				GPIO260			
Type									WO				WO			
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO259				GPIO258				GPIO257				GPIO256			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:20		GPIO261	**Alternative way to set up Aux mode of JTRST_B** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
19:16		GPIO260	**Alternative way to set up Aux mode of JTDO**
15:12		GPIO259	**Alternative way to set up Aux mode of JTDI**
11:8		GPIO258	**Alternative way to set up Aux mode of JTCK**
7:4		GPIO257	**Alternative way to set up Aux mode of JTMS**
3:0		GPIO256	**Alternative way to set up Aux mode of AUD_PDN**

10005600 MISC **GPIO Related Misc Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		DUMMY	**Chip related misc options** [0]: test_in_utmi_en [1]: usb_i2c_mode_en [3]: wbg gpi enable [4]: pta_pin_to_lte_en [5]: pta_pin_to_conn_en [31]: osc_out_mon_en

10005604 MISC_SET **GPIO Related Misc Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		DUMMY	**Bitwise SET operation of MISC** 0: Keep 1: SET bits

10005608 MISC_CLR GPIO Related Misc Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		DUMMY	**Bitwise CLR operation of MISC** 0: Keep 1: SET bits

Module name: IO_CFG_L Base address: (+10002000h)

Address	Name	Width	Register Function
10002000	IES_CFG0	32	IES Control
10002004	IES_CFG0_SET	32	IES Control
10002008	IES_CFG0_CLR	32	IES Control
10002010	IES_CFG1	32	IES Control
10002014	IES_CFG1_SET	32	IES Control
10002018	IES_CFG1_CLR	32	IES Control
10002020	SR_CFG0	32	SR Control
10002024	SR_CFG0_SET	32	SR Control
10002028	SR_CFG0_CLR	32	SR Control
10002030	SR_CFG1	32	SR Control
10002034	SR_CFG1_SET	32	SR Control
10002038	SR_CFG1_CLR	32	SR Control
10002040	SMT_CFG0	32	SMT Control
10002044	SMT_CFG0_SET	32	SMT Control
10002048	SMT_CFG0_CLR	32	SMT Control

Address	Name	Width	Register Function
10002050	SMT_CFG1	32	SMT Control
10002054	SMT_CFG1_SET	32	SMT Control
10002058	SMT_CFG1_CLR	32	SMT Control
10002060	TDSEL_CFG0	32	TDSEL Control
10002064	TDSEL_CFG0_SET	32	TDSEL Control
10002068	TDSEL_CFG0_CLR	32	TDSEL Control
10002070	TDSEL_CFG1	32	TDSEL Control
10002074	TDSEL_CFG1_SET	32	TDSEL Control
10002078	TDSEL_CFG1_CLR	32	TDSEL Control
10002080	TDSEL_CFG2	32	TDSEL Control
10002084	TDSEL_CFG2_SET	32	TDSEL Control
10002088	TDSEL_CFG2_CLR	32	TDSEL Control
10002090	RDSEL_CFG0	32	RDSEL Control
10002094	RDSEL_CFG0_SET	32	RDSEL Control
10002098	RDSEL_CFG0_CLR	32	RDSEL Control
100020A0	RDSEL_CFG1	32	RDSEL Control
100020A4	RDSEL_CFG1_SET	32	RDSEL Control
100020A8	RDSEL_CFG1_CLR	32	RDSEL Control
100020B0	PU_CFG0	32	PU Control
100020B4	PU_CFG0_SET	32	PU Control
100020B8	PU_CFG0_CLR	32	PU Control
100020C0	PU_CFG1	32	PU Control
100020C4	PU_CFG1_SET	32	PU Control
100020C8	PU_CFG1_CLR	32	PU Control
100020D0	PD_CFG0	32	PD Control
100020D4	PD_CFG0_SET	32	PD Control
100020D8	PD_CFG0_CLR	32	PD Control
100020E0	PD_CFG1	32	PD Control
100020E4	PD_CFG1_SET	32	PD Control
100020E8	PD_CFG1_CLR	32	PD Control
100020F0	DRV_CFG0	32	DRV Control
100020F4	DRV_CFG0_SET	32	DRV Control
100020F8	DRV_CFG0_CLR	32	DRV Control
10002100	DRV_CFG1	32	DRV Control
10002104	DRV_CFG1_SET	32	DRV Control
10002108	DRV_CFG1_CLR	32	DRV Control
10002110	PUDD_CFG0	32	PUPD Control
10002114	PUDD_CFG0_SET	32	PUPD Control
10002118	PUDD_CFG0_CLR	32	PUPD Control
10002120	R0_CFG0	32	R0 Control
10002124	R0_CFG0_SET	32	R0 Control
10002128	R0_CFG0_CLR	32	R0 Control
10002130	R1_CFG0	32	R1 Control

Address	Name	Width	Register Function
10002134	R1_CFG0_SET	32	R1 Control
10002138	R1_CFG0_CLR	32	R1 Control
10002200	DUMMY	32	DUMMY
10002204	DUMMY_SET	32	DUMMY
10002208	DUMMY_CLR	32	DUMMY

10002000 IES_CFG0 **IES Control** **0FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DPI_L											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DPI_L				URO_L		CAM_L									
Type	RW				RW		RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
27:12		DPI_L	**IES control of DPI IO** [0]: DPI_D0 0: Disable 1: Enable [1]: DPI_D1 [2]: DPI_D2 [3]: DPI_D3 [4]: DPI_D4 [5]: DPI_D5 [6]: DPI_D6 [7]: DPI_D7 [8]: DPI_D8 [9]: DPI_D9 [10]: DPI_D10 [11]: DPI_D11 [12]: DPI_DE [13]: DPI_CK [14]: DPI_HSYNC [15]: DPI_VSYNC
11:10		URO_L	**IES control of URO IO** [0]: URXD0 [1]: UTXD0
9:0		CAM_L	**IES control of CAM IO** [0]: CAM_PDN0 [1]: CAM_PDN1 [2]: CAM_CLK0 [3]: CAM_CLK1 [4]: CAM_RST0 [5]: CAM_RST1 [6]: CAM_PDN2 [7]: CAM_RST2 [8]: CAM_CLK2 [9]: Reserved

10002004 IES_CFG0_SET IES Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DPI_L											
Type					WO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DPI_L				URo_L		CAM_L									
Type	WO				WO		WO									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:12		DPI_L	**Bitwise SET operation for IES control of DPI IO** 0: Keep 1: SET bits
11:10		URo_L	**Bitwise SET operation for IES control of URo IO**
9:0		CAM_L	**Bitwise SET operation for IES control of CAM IO**

10002008 IES_CFG0_CLR IES Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DPI_L											
Type					WO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DPI_L				URo_L		CAM_L									
Type	WO				WO		WO									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:12		DPI_L	**Bitwise CLR operation for IES control of DPI IO** 0: Keep 1: CLR bits
11:10		URo_L	**Bitwise CLR operation for IES control of URo IO**
9:0		CAM_L	**Bitwise CLR operation for IES control of CAM IO**

10002010 IES_CFG1 IES Control FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I2S2_L							CONN_L								
Type	RW							RW								
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2S1_L							I2C3_L		I2C2_L		JTG_L				
Type	RW							RW		RW		RW				
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:25		I2S2_L	**Reserved**

Bit(s)	Mnemonic	Name	Description
			[6:0]: Reserved
24:16		CONN_L	**IES control of CONN IO** [0]: CONN_HRST_B 0: Disable 1: Enable [1]: CONN_TOP_DATA [2]: CONN_TOP_CLK [3]: CONN_WB_PTA [4]: CONN_WF_CTRL2 [5]: CONN_WF_CTRL1 [6]: CONN_WF_CTRL0 [7]: CONN_BT_CLK [8]: CONN_BT_DATA
15:9		I2S1_L	**IES control of I2S1 IO** [0]: TDM_LRCK [1]: TDM_BCK [2]: TDM_MCK [3]: TDM_DATA0 [4]: TDM_DATA1 [5]: TDM_DATA2 [6]: TDM_DATA3
8:7		I2C3_L	**IES control of I2C3 IO** [0]: SCL3 [1]: SDA3
6:5		I2C2_L	**IES control of I2C2 IO** [0]: SCL2 [1]: SDA2
4:0		JTG_L	**IES control of JTG IO** [0]: JTMS [1]: JTCK [2]: JTDI [3]: JTDO [4]: JTRST_B

10002014 IES_CFG1_SET **IES Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I2S2_L							CONN_L								
Type	WO							WO								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2S1_L							I2C3_L		I2C2_L		JTG_L				
Type	WO							WO		WO		WO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		I2S2_L	**Reserved** 0: Keep 1: SET bits
24:16		CONN_L	**Bitwise SET operation for IES control of CONN IO**
15:9		I2S1_L	**Bitwise SET operation for IES control of I2S1 IO**
8:7		I2C3_L	**Bitwise SET operation for IES control of I2C3 IO**
6:5		I2C2_L	**Bitwise SET operation for IES control of I2C2 IO**
4:0		JTG_L	**Bitwise SET operation for IES control of JTG IO**

Bit(s)	Mnemonic	Name	Description

10002018 IES_CFG1_CLR **IES Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I2S2_L							CONN_L								
Type	WO							WO								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2S1_L							I2C3_L		I2C2_L		JTG_L				
Type	WO							WO		WO		WO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:25		I2S2_L	**Reserved** 0: Keep 1: CLR bits
24:16		CONN_L	**Bitwise CLR operation for IES control of CONN IO**
15:9		I2S1_L	**Bitwise CLR operation for IES control of I2S1 IO**
8:7		I2C3_L	**Bitwise CLR operation for IES control of I2C3 IO**
6:5		I2C2_L	**Bitwise CLR operation for IES control of I2C2 IO**
4:0		JTG_L	**Bitwise CLR operation for IES control of JTG IO**

10002020 SR_CFG0 **SR Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													I2S1_L			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2C3_L	I2C2_L	JTG_L			DPI_L					URo_L	CAM_L				
Type	RW	RW	RW			RW					RW	RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:16		I2S1_L	**SR control of I2S1 IO** [0]: TDM_LRCK 0: Disable 1: Enable [1]: TDM_BCK [2]: TDM_MCK [3]: TDM_DATA0, TDM_DATA1, TDM_DATA2, TDM_DATA3
15		I2C3_L	**Reserved** [0]: Reserved
14		I2C2_L	**Reserved** [0]: Reserved
13:11		JTG_L	**SR control of JTG IO** [0]: JTMS, JTDO, JTRST_B [1]: JTCK [2]: JTDI

Bit(s)	Mnemonic	Name	Description
10:6		DPI_L	**SR control of DPI IO** [0]: DPI_D0, DPI_D1, DPI_D2, DPI_D3 [1]: DPI_D4, DPI_D5, DPI_D6, DPI_D7 [2]: DPI_D8, DPI_D9, DPI_D10, DPI_D11 [3]: DPI_DE, DPI_HSYNC, DPI_VSYNC [4]: DPI_CK
5		UR0_L	**SR control of UR0 IO** [0]: URXD0, UTXD0
4:0		CAM_L	**SR control of CAM IO** [0]: CAM_PDN0, CAM_PDN1 [1]: CAM_CLK0, CAM_CLK1 [2]: CAM_RST0, CAM_RST1 [3]: CAM_PDN2 [4]: CAM_RST2, CAM_CLK2

10002024 SR_CFG0_SET **SR Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													I2S1_L			
Type													WO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2C3_L	I2C2_L	JTG_L			DPI_L					UR0_L	CAM_L				
Type	WO	WO	WO			WO					WO	WO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:16		I2S1_L	**Bitwise SET operation for SR control of I2S1 IO** 0: Keep 1: SET bits
15		I2C3_L	**Reserved**
14		I2C2_L	**Reserved**
13:11		JTG_L	**Bitwise SET operation for SR control of JTG IO**
10:6		DPI_L	**Bitwise SET operation for SR control of DPI IO**
5		UR0_L	**Bitwise SET operation for SR control of UR0 IO**
4:0		CAM_L	**Bitwise SET operation for SR control of CAM IO**

10002028 SR_CFG0_CLR **SR Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													I2S1_L			
Type													WO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2C3_L	I2C2_L	JTG_L			DPI_L					UR0_L	CAM_L				
Type	WO	WO	WO			WO					WO	WO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:16		I2S1_L	**Bitwise CLR operation for SR control of I2S1 IO** 0: Keep 1: CLR bits
15		I2C3_L	**Reserved**
14		I2C2_L	**Reserved**
13:11		JTG_L	**Bitwise CLR operation for SR control of JTG IO**
10:6		DPI_L	**Bitwise CLR operation for SR control of DPI IO**
5		UR0_L	**Bitwise CLR operation for SR control of UR0 IO**
4:0		CAM_L	**Bitwise CLR operation for SR control of CAM IO**

10002030 SR_CFG1 SR Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CONN_L				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		CONN_L	**SR control of CONN IO** [0]: CONN_HRST_B, CONN_TOP_CLK 0: Disable 1: Enable [1]: CONN_TOP_DATA [2]: CONN_WB_PTA, CONN_WF_CTRL2, CONN_WF_CTRL1, CONN_WF_CTRL0 [3]: CONN_BT_CLK [4]: CONN_BT_DATA

10002034 SR_CFG1_SET SR Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CONN_L				
Type												WO				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		CONN_L	Bitwise SET operation for SR control of CONN IO

10002038 SR_CFG1_CLR **SR Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**CONN_L**				
Type												WO				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		CONN_L	Bitwise CLR operation for SR control of CONN IO

10002040 SMT_CFG0 **SMT Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													**I2S1_L**			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**I2C3_L**	**I2C2_L**	**JTG_L**			**DPI_L**					**URO_L**	**CAM_L**				
Type	RW	RW	RW			RW					RW	RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:16		I2S1_L	**SMT control of I2S1 IO** [0]: TDM_LRCK 0: Disable 1: Enable [1]: TDM_BCK [2]: TDM_MCK [3]: TDM_DATA0, TDM_DATA1, TDM_DATA2, TDM_DATA3
15		I2C3_L	**SMT control of I2C3 IO** [0]: SCL3, SDA3
14		I2C2_L	**SMT control of I2C2 IO** [0]: SCL2, SDA2
13:11		JTG_L	**SMT control of JTG IO** [0]: JTMS, JTDO, JTRST_B [1]: JTCK [2]: JTDI
10:6		DPI_L	**SMT control of DPI IO** [0]: DPI_D0, DPI_D1, DPI_D2, DPI_D3 [1]: DPI_D4, DPI_D5, DPI_D6, DPI_D7 [2]: DPI_D8, DPI_D9, DPI_D10, DPI_D11 [3]: DPI_DE, DPI_HSYNC, DPI_VSYNC [4]: DPI_CK
5		URO_L	**SMT control of URO IO** [0]: URXD0, UTXD0
4:0		CAM_L	**SMT control of CAM IO** [0]: CAM_PDN0, CAM_PDN1 [1]: CAM_CLK0, CAM_CLK1

Bit(s)	Mnemonic	Name	Description
			[2]: CAM_RST0, CAM_RST1 [3]: CAM_PDN2 [4]: CAM_RST2, CAM_CLK2

10002044 SMT_CFG0_SET **SMT Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													I2S1_L			
Type													WO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2C3_L	I2C2_L	JTG_L			DPI_L					URO_L	CAM_L				
Type	WO	WO	WO			WO					WO	WO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:16		I2S1_L	**Bitwise SET operation for SMT control of I2S1 IO** 0: Keep 1: SET bits
15		I2C3_L	**Bitwise SET operation for SMT control of I2C3 IO**
14		I2C2_L	**Bitwise SET operation for SMT control of I2C2 IO**
13:11		JTG_L	**Bitwise SET operation for SMT control of JTG IO**
10:6		DPI_L	**Bitwise SET operation for SMT control of DPI IO**
5		URO_L	**Bitwise SET operation for SMT control of URO IO**
4:0		CAM_L	**Bitwise SET operation for SMT control of CAM IO**

10002048 SMT_CFG0_CLR **SMT Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													I2S1_L			
Type													WO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2C3_L	I2C2_L	JTG_L			DPI_L					URO_L	CAM_L				
Type	WO	WO	WO			WO					WO	WO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:16		I2S1_L	**Bitwise CLR operation for SMT control of I2S1 IO** 0: Keep 1: CLR bits
15		I2C3_L	**Bitwise CLR operation for SMT control of I2C3 IO**

Bit(s)	Mnemonic	Name	Description
14		I2C2_L	**Bitwise CLR operation for SMT control of I2C2 IO**
13:11		JTG_L	**Bitwise CLR operation for SMT control of JTG IO**
10:6		DPI_L	**Bitwise CLR operation for SMT control of DPI IO**
5		URO_L	**Bitwise CLR operation for SMT control of URO IO**
4:0		CAM_L	**Bitwise CLR operation for SMT control of CAM IO**

10002050 SMT_CFG1 SMT Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CONN_L				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		CONN_L	**SMT control of CONN IO** [0]: CONN_HRST_B, CONN_TOP_CLK 0: Disable 1: Enable [1]: CONN_TOP_DATA [2]: CONN_WB_PTA, CONN_WF_CTRL2, CONN_WF_CTRL1, CONN_WF_CTRL0 [3]: CONN_BT_CLK [4]: CONN_BT_DATA

10002054 SMT_CFG1_SET SMT Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CONN_L				
Type												WO				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		CONN_L	**Bitwise SET operation for SMT control of CONN IO** 0: Keep 1: SET bits

10002058 SMT_CFG1_CLR **SMT Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CONN_L				
Type												WO				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		CONN_L	**Bitwise CLR operation for SMT control of CONN IO** 0: Keep 1: CLR bits

10002060 TDSEL_CFG0 **TDSEL Control** **0F000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					SLP				URo_L				CAM_L			
Type					RW				RW				RW			
Reset					1	1	1	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAM_L															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24		SLP	**TDSEL value for sleep mode** [3:0]: TDSEL value of IOs in left side in sleep mode Suggested value: 0xF
23:20		URo_L	**TDSEL control of URo IO** [3:0]: URXD0, UTXD0
19:0		CAM_L	**TDSEL control of CAM IO** [3:0]: CAM_PDN0, CAM_PDN1 [7:4]: CAM_CLK0, CAM_CLK1 [11:8]: CAM_RST0, CAM_RST1 [15:12]: CAM_PDN2 [19:16]: CAM_RST2, CAM_CLK2

10002064 TDSEL_CFG0_SET **TDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					SLP				URo_L				CAM_L			
Type					WO				WO				WO			
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAM_L															
Type	WO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24		SLP	**Bitwise SET operation for TDSEL value fpr Sleep mode** 0: Keep 1: SET bits
23:20		URo_L	**Bitwise SET operation for TDSEL control of URo IO**
19:0		CAM_L	**Bitwise SET operation for TDSEL control of CAM IO**

10002068 TDSEL_CFG0_CLR TDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					SLP				URo_L				CAM_L			
Type					WO				WO				WO			
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAM_L															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24		SLP	**Bitwise CLR operation for TDSEL value fpr Sleep mode** 0: Keep 1: CLR bits
23:20		URo_L	**Bitwise CLR operation for TDSEL control of URo IO**
19:0		CAM_L	**Bitwise CLR operation for TDSEL control of CAM IO**

10002070 TDSEL_CFG1 TDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I2C3_L				I2C2_L				JTG_L				DPI_L			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DPI_L															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		I2C3_L	**TDSEL control of I2C3 IO** [3:0]: SCL2, SDA2
27:24		I2C2_L	**TDSEL control of I2C2 IO** [3:0]: SCL2, SDA2
23:20		JTG_L	**TDSEL control of JTG IO** [3:0]: JTMS, JTDO, JTRST_B, JTCK, JTDI
19:0		DPI_L	**TDSEL control of DPI IO**

Bit(s)	Mnemonic	Name	Description
			[3:0]: DPI_D0, DPI_D1, DPI_D2, DPI_D3 [7:4]: DPI_D4, DPI_D5, DPI_D6, DPI_D7 [11:8]: DPI_D8, DPI_D9, DPI_D10, DPI_D11 [15:12]: DPI_DE, DPI_HSYNC, DPI_VSYNC [19:16]: DPI_CK

10002074 TDSEL_CFG1_SET TDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I2C3_L				I2C2_L				JTG_L				DPI_L			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DPI_L															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		I2C3_L	**Bitwise SET operation for TDSEL control of I2C3 IO** 0: Keep 1: SET bits
27:24		I2C2_L	**Bitwise SET operation for TDSEL control of I2C2 IO**
23:20		JTG_L	**Bitwise SET operation for TDSEL control of JTG IO**
19:0		DPI_L	**Bitwise SET operation for TDSEL control of DPI IO**

10002078 TDSEL_CFG1_CLR TDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I2C3_L				I2C2_L				JTG_L				DPI_L			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DPI_L															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		I2C3_L	**Bitwise CLR operation for TDSEL control of I2C3 IO** 0: Keep 1: CLR bits
27:24		I2C2_L	**Bitwise CLR operation for TDSEL control of I2C2 IO**
23:20		JTG_L	**Bitwise CLR operation for TDSEL control of JTG IO**
19:0		DPI_L	**Bitwise CLR operation for TDSEL control of DPI IO**

Bit(s)	Mnemonic	Name	Description

10002080 TDSEL_CFG2 TDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CONN_L											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CONN_L								I2S1_L							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:8		CONN_L	**TDSEL control of CONN IO** [3:0]: CONN_HRST_B, CONN_TOP_CLK [7:4]: CONN_TOP_DATA [11:8]: CONN_WB_PTA, CONN_WF_CTRL2, CONN_WF_CTRL1, CONN_WF_CTRL0 [15:12]: CONN_BT_CLK [19:16]: CONN_BT_DATA
7:0		I2S1_L	**TDSEL control of I2S1 IO** [3:0]: TDM_LRCK, TDM_BCK, TDM_MCK [7:4]: TDM_DATA0, TDM_DATA1, TDM_DATA2, TDM_DATA3

10002084 TDSEL_CFG2_SET TDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CONN_L											
Type					WO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CONN_L								I2S1_L							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:8		CONN_L	**Bitwise SET operation for TDSEL control of CONN IO** 0: Keep 1: SET bits
7:0		I2S1_L	**Bitwise SET operation for TDSEL control of I2S1 IO**

10002088 TDSEL_CFG2_CLR TDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CONN_L											

Type					WO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CONN_L								I2S1_L							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:8		CONN_L	**Bitwise CLR operation for TDSEL control of CONN IO** 0: Keep 1: CLR bits
7:0		I2S1_L	**Bitwise CLR operation for TDSEL control of I2S1 IO**

10002090 RDSEL_CFG0 RDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I2S1_L				I2C3_L		I2C2_L		JTG_L		DPI_L					
Type	RW				RW		RW		RW		RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DPI_L				UR0_L		CAM_L									
Type	RW				RW		RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		I2S1_L	**RDSEL control of I2S1 IO** [1:0]: TDM_LRCK, TDM_BCK, TDM_MCK [3:2]: TDM_DATA0, TDM_DATA1, TDM_DATA2, TDM_DATA3
27:26		I2C3_L	**RDSEL control of I2C3 IO** [1:0]: SCL2, SDA2
25:24		I2C2_L	**RDSEL control of I2C2 IO** [1:0]: SCL2, SDA2
23:22		JTG_L	**RDSEL control of JTG IO** [1:0]: JTMS, JTDO, JTRST_B, JTCK, JTDI
21:12		DPI_L	**RDSEL control of DPI IO** [1:0]: DPI_D0, DPI_D1, DPI_D2, DPI_D3 [3:2]: DPI_D4, DPI_D5, DPI_D6, DPI_D7 [5:4]: DPI_D8, DPI_D9, DPI_D10, DPI_D11 [7:6]: DPI_DE, DPI_HSYNC, DPI_VSYNC [9:8]: DPI_CK
11:10		UR0_L	**RDSEL control of UR0 IO** [1:0]: URXD0, UTXD0
9:0		CAM_L	**RDSEL control of CAM IO** [1:0]: CAM_PDN0, CAM_PDN1 [3:2]: CAM_CLK0, CAM_CLK1 [5:4]: CAM_RST0, CAM_RST1 [7:6]: CAM_PDN2 [9:8]: CAM_RST2, CAM_CLK2

10002094 RDSEL_CFG0_SET RDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I2S1_L				I2C3_L		I2C2_L		JTG_L		DPI_L					
Type	WO				WO		WO		WO		WO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DPI_L				URo_L		CAM_L									
Type	WO				WO		WO									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		I2S1_L	**Bitwise SET operation for RDSEL control of I2S1 IO** 0: Keep 1: SET bits
27:26		I2C3_L	**Bitwise SET operation for RDSEL control of I2C3 IO**
25:24		I2C2_L	**Bitwise SET operation for RDSEL control of I2C2 IO**
23:22		JTG_L	**Bitwise SET operation for RDSEL control of JTG IO**
21:12		DPI_L	**Bitwise SET operation for RDSEL control of DPI IO**
11:10		URo_L	**Bitwise SET operation for RDSEL control of URo IO**
9:0		CAM_L	**Bitwise SET operation for RDSEL control of CAM IO**

10002098 RDSEL_CFG0_CLR RDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I2S1_L				I2C3_L		I2C2_L		JTG_L		DPI_L					
Type	WO				WO		WO		WO		WO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DPI_L				URo_L		CAM_L									
Type	WO				WO		WO									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		I2S1_L	**Bitwise CLR operation for RDSEL control of I2S1 IO** 0: Keep 1: CLR bits
27:26		I2C3_L	**Bitwise CLR operation for RDSEL control of I2C3 IO**
25:24		I2C2_L	**Bitwise CLR operation for RDSEL control of I2C2 IO**
23:22		JTG_L	**Bitwise CLR operation for RDSEL control of JTG IO**
21:12		DPI_L	**Bitwise CLR operation for RDSEL control of DPI IO**
11:10		URo_L	**Bitwise CLR operation for RDSEL control of URo IO**
9:0		CAM_L	**Bitwise CLR operation for RDSEL control of CAM IO**

Bit(s)	Mnemonic	Name	Description

100020A0 RDSEL_CFG1 RDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			CONN_L										UR1_L			
Type			RW										RW			
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13:4		CONN_L	**RDSEL control of CONN IO** [1:0]: CONN_HRST_B, CONN_TOP_CLK [3:2]: CONN_TOP_DATA [5:4]: CONN_WB_PTA, CONN_WF_CTRL2, CONN_WF_CTRL1, CONN_WF_CTRL0 [7:6]: CONN_BT_CLK [9:8]: CONN_BT_DATA
3:0		UR1_L	**RDSEL control of UR1 IO** [1:0]: URXD0, UTXD0 [3:2]: Reserved

100020A4 RDSEL_CFG1_SET RDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			CONN_L										UR1_L			
Type			WO										WO			
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13:4		CONN_L	**Bitwise SET operation for RDSEL control of CONN IO** 0: Keep 1: SET bits
3:0		UR1_L	**Bitwise SET operation for RDSEL control of UR1 IO**

100020A8 RDSEL_CFG1_CLR RDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			CONN_L										UR1_L			
Type			WO										WO			
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13:4		CONN_L	**Bitwise CLR operation for RDSEL control of CONN IO** 0: Keep 1: CLR bits
3:0		UR1_L	**Bitwise CLR operation for RDSEL control of UR1 IO**

100020B0 PU_CFG0 **PU Control** **00000400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DPI_L											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DPI_L				UR0_L		CAM_L									
Type	RW				RW		RW									
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:12		DPI_L	**Pull-up control of DPI IO** [0]: DPI_D0 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: DPI_D1 [2]: DPI_D2 [3]: DPI_D3 [4]: DPI_D4 [5]: DPI_D5 [6]: DPI_D6 [7]: DPI_D7 [8]: DPI_D8 [9]: DPI_D9 [10]: DPI_D10 [11]: DPI_D11 [12]: DPI_DE [13]: DPI_CK [14]: DPI_HSYNC [15]: DPI_VSYNC
11:10		UR0_L	**Pull-up control of UR0 IO** [0]: URXD0 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm

Bit(s)	Mnemonic	Name	Description
9:0		CAM_L	1/1: N/A [1]: UTXD0 **Pull-up control of CAM IO** [0]: CAM_PDN0 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: CAM_PDN1 [2]: CAM_CLK0 [3]: CAM_CLK1 [4]: CAM_RST0 [5]: CAM_RST1 [6]: CAM_PDN2 [7]: CAM_RST2 [8]: CAM_CLK2 [9]: Reserved

100020B4 PU_CFG0_SET **PU Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DPI_L											
Type					WO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DPI_L				URo_L		CAM_L									
Type	WO				WO		WO									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:12		DPI_L	**Bitwise SET operation for pull-up control of DPI IO** 0: Keep 1: SET bits
11:10		URo_L	**Bitwise SET operation for pull-up control of URo IO**
9:0		CAM_L	**Bitwise SET operation for pull-up control of CAM IO**

100020B8 PU_CFG0_CLR **PU Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DPI_L											
Type					WO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DPI_L				URo_L		CAM_L									
Type	WO				WO		WO									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:12		DPI_L	**Bitwise CLR operation for pull-up control of DPI IO** 0: Keep 1: CLR bits
11:10		UR0_L	**Bitwise CLR operation for pull-up control of UR0 IO**
9:0		CAM_L	**Bitwise CLR operation for pull-up control of CAM IO**

10002C0 PU_CFG1 **PU Control** **00000007**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CONN_L					
Type											RW					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CONN_L			I2S1_L							JTG_L					
Type	RW			RW							RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
21:13		CONN_L	**Pull-up control of CONN IO** [0]: CONN_HRST_B PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: CONN_TOP_DATA [2]: CONN_TOP_CLK [3]: CONN_WB_PTA [4]: CONN_WF_CTRL2 [5]: CONN_WF_CTRL1 [6]: CONN_WF_CTRL0 [7]: CONN_BT_CLK [8]: CONN_BT_DATA
12:6		I2S1_L	**Pull-up control of I2S1 IO** [0]: TDM_LRCK PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: TDM_BCK [2]: TDM_MCK [3]: TDM_DATA0 [4]: TDM_DATA1 [5]: TDM_DATA2 [6]: TDM_DATA3
5:0		JTG_L	**Pull-up control of JTG IO** [0]: JTMS PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: JTCK

Bit(s)	Mnemonic	Name	Description
			[2]: JTDI [3]: JTDO [4]: JTRST_B [5]: Reserved

100020C4 PU_CFG1_SET **PU Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CONN_L					
Type											WO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CONN_L			I2S1_L							JTG_L					
Type	WO			WO							WO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:13		CONN_L	**Bitwise SET operation for pull-up control of CONN IO** 0: Keep 1: SET bits
12:6		I2S1_L	**Bitwise SET operation for pull-up control of I2S1 IO**
5:0		JTG_L	**Bitwise SET operation for pull-up control of JTG IO**

100020C8 PU_CFG1_CLR **PU Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CONN_L					
Type											WO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CONN_L			I2S1_L							JTG_L					
Type	WO			WO							WO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:13		CONN_L	**Bitwise CLR operation for pull-up control of CONN IO** 0: Keep 1: CLR bits
12:6		I2S1_L	**Bitwise CLR operation for pull-up control of I2S1 IO**
5:0		JTG_L	**Bitwise CLR operation for pull-up control of JTG IO**

100020D0 PD_CFG0 **PD Control** **0FFFF3FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I2C3_L		I2C2_L		DPI_L											
Type	RW		RW		RW											
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DPI_L				URo_L		CAM_L									
Type	RW				RW		RW									
Reset	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:30		I2C3_L	**Pull-down control of I2C3 IO** [0]: SCL3 0: N/A 1: Pull down with 75Kohm [1]: SDA3
29:28		I2C2_L	**Pull-down control of I2C2 IO** [0]: SCL2 0: N/A 1: Pull down with 75Kohm [1]: SDA2
27:12		DPI_L	**Pull-down control of DPI IO** [0]: DPI_D0 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: DPI_D1 [2]: DPI_D2 [3]: DPI_D3 [4]: DPI_D4 [5]: DPI_D5 [6]: DPI_D6 [7]: DPI_D7 [8]: DPI_D8 [9]: DPI_D9 [10]: DPI_D10 [11]: DPI_D11 [12]: DPI_DE [13]: DPI_CK [14]: DPI_HSYNC [15]: DPI_VSYNC
11:10		URo_L	**Pull-down control of URo IO** [0]: URXD0 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: UTXD0
9:0		CAM_L	**Pull-down control of CAM IO** [0]: CAM_PDN0 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: CAM_PDN1 [2]: CAM_CLK0 [3]: CAM_CLK1

Bit(s)	Mnemonic	Name	Description
			[4]: CAM_RST0 [5]: CAM_RST1 [6]: CAM_PDN2 [7]: CAM_RST2 [8]: CAM_CLK2 [9]: Reserved

100020D4 PD_CFG0_SET **PD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I2C3_L		I2C2_L		DPI_L											
Type	WO		WO		WO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DPI_L				URo_L		CAM_L									
Type	WO				WO		WO									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:30		I2C3_L	**Bitwise SET operation for pull-down control of I2C3 IO** 0: Keep 1: SET bits
29:28		I2C2_L	**Bitwise SET operation for pull-down control of I2C2 IO**
27:12		DPI_L	**Bitwise SET operation for pull-down control of DPI IO**
11:10		URo_L	**Bitwise SET operation for pull-down control of URo IO**
9:0		CAM_L	**Bitwise SET operation for pull-down control of CAM IO**

100020D8 PD_CFG0_CLR **PD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I2C3_L		I2C2_L		DPI_L											
Type	WO		WO		WO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DPI_L				URo_L		CAM_L									
Type	WO				WO		WO									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:30		I2C3_L	**Bitwise CLR operation for pull-down control of I2C3 IO** 0: Keep 1: CLR bits
29:28		I2C2_L	**Bitwise CLR operation for pull-down control of I2C2 IO**
27:12		DPI_L	**Bitwise CLR operation for pull-down control of**

Bit(s)	Mnemonic	Name	Description
			DPI IO
11:10		UR0_L	**Bitwise CLR operation for pull-down control of UR0 IO**
9:0		CAM_L	**Bitwise CLR operation for pull-down control of CAM IO**

100020E0 PD_CFG1 **PD Control** **003FFFD8**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CONN_L					
Type											RW					
Reset											1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CONN_L			I2S1_L							JTG_L					
Type	RW			RW							RW					
Reset	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	0

Bit(s)	Mnemonic	Name	Description
21:13		CONN_L	**Pull-down control of CONN IO** [0]: DPI_D0 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: DPI_D1 [2]: DPI_D2 [3]: DPI_D3 [4]: DPI_D4 [5]: DPI_D5 [6]: DPI_D6 [7]: DPI_D7 [8]: DPI_D8 [9]: DPI_D9 [10]: DPI_D10 [11]: DPI_D11 [12]: DPI_DE [13]: DPI_CK [14]: DPI_HSYNC [15]: DPI_VSYNC
12:6		I2S1_L	**Pull-down control of I2S1 IO** [0]: TDM_LRCK PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: TDM_BCK [2]: TDM_MCK [3]: TDM_DATA0 [4]: TDM_DATA1 [5]: TDM_DATA2 [6]: TDM_DATA3
5:0		JTG_L	**Pull-down control of JTG IO** [0]: JTMS PU/PD: 0/0: N/A

Bit(s)	Mnemonic	Name	Description
			1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: JTCK [2]: JTDI [3]: JTDO [4]: JTRST_B [5]: Reserved

100020E4 PD_CFG1_SET **PD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CONN_L					
Type											WO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CONN_L			I2S1_L							JTG_L					
Type	WO			WO							WO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:13		CONN_L	**Bitwise SET operation for pull-down control of CONN IO** 0: Keep 1: SET bits
12:6		I2S1_L	**Bitwise SET operation for pull-down control of I2S1 IO**
5:0		JTG_L	**Bitwise SET operation for pull-down control of JTG IO**

100020E8 PD_CFG1_CLR **PD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CONN_L					
Type											WO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CONN_L			I2S1_L							JTG_L					
Type	WO			WO							WO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:13		CONN_L	**Bitwise CLR operation for pull-down control of CONN IO** 0: Keep 1: CLR bits
12:6		I2S1_L	**Bitwise CLR operation for pull-down control of I2S1 IO**
5:0		JTG_L	**Bitwise CLR operation for pull-down control of JTG IO**

Bit(s)	Mnemonic	Name	Description

100020F0 DRV_CFG0 DRV Control 05555555

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					JTG_L						DPI_L					
Type					RW						RW					
Reset					0	1	0	1	0	1	0	1	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DPI_L				URo_L		CAM_L									
Type	RW				RW		RW									
Reset	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
27:22		JTG_L	**DRV control of JTG IO** [1:0]: JTMS, JTDO, JTRST_B 00: 4mA 01: 8mA 10: 12mA 11: 16mA [3:2]: JTCK [5:4]: JTDI
21:12		DPI_L	**DRV control of DPI IO** [1:0]: DPI_D0, DPI_D1, DPI_D2, DPI_D3 00: 4mA 01: 8mA 10: 12mA 11: 16mA [3:2]: DPI_D4, DPI_D5, DPI_D6, DPI_D7 [5:4]: DPI_D8, DPI_D9, DPI_D10, DPI_D11 [7:6]: DPI_DE, DPI_HSYNC, DPI_VSYNC [9:8]: DPI_CK
11:10		URo_L	**DRV control of URo IO** [1:0]: URXD0, UTXD0 00: 4mA 01: 8mA 10: 12mA 11: 16mA
9:0		CAM_L	**DRV control of CAM IO** [1:0]: CAM_PDN0, CAM_PDN1 00: 2mA 01: 4mA 10: 6mA 11: 8mA [3:2]: CAM_CLK0, CAM_CLK1 [5:4]: CAM_RST0, CAM_RST1 [7:6]: CAM_PDN2 [9:8]: CAM_RST2, CAM_CLK2

100020F4 DRV_CFG0_SET DRV Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					JTG_L						DPI_L					

Type					WO						WO					
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DPI_L				URo_L		CAM_L									
Type	WO				WO		WO									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:22		JTG_L	**Bitwise SET operation for driving control of JTG IO** 0: Keep 1: SET bits
21:12		DPI_L	**Bitwise SET operation for driving control of DPI IO**
11:10		URo_L	**Bitwise SET operation for driving control of URo IO**
9:0		CAM_L	**Bitwise SET operation for driving control of CAM IO**

100020F8 DRV_CFG0_CLR **DRV Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					JTG_L						DPI_L					
Type					WO						WO					
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DPI_L				URo_L		CAM_L									
Type	WO				WO		WO									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:22		JTG_L	**Bitwise CLR operation for driving control of JTG IO** 0: Keep 1: CLR bits
21:12		DPI_L	**Bitwise CLR operation for driving control of DPI IO**
11:10		URo_L	**Bitwise CLR operation for driving control of URo IO**
9:0		CAM_L	**Bitwise CLR operation for driving control of CAM IO**

10002100 DRV_CFG1 **DRV Control** **00555555**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CONN_L							
Type									RW							
Reset									0	1	0	1	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CONN_L								I2S1_L				I2C3_L		I2C2_L	
Type	RW								RW				RW		RW	

Reset	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
23:8		CONN_L	**Driving control of CONN IO** [1:0]: CONN_HRST_B 00: 2mA 01: 4mA 10: 6mA 11: 8mA [2]: Reserved [4:3]: CONN_TOP_DATA [5]: Reserved [7:6]: CONN_TOP_CLK [8]: Reserved [10:9]: CONN_WB_PTA, CONN_WF_CTRL2, CONN_WF_CTRL1 [11]: Reserved [13:12]: CONN_WF_CTRL0, CONN_BT_DATA [15:14]: CONN_BT_CLK
7:4		I2S1_L	**Driving control of I2S1 IO** [1:0]: TDM_LRCK, TDM_BCK, TDM_MCK 00: 2mA 01: 4mA 10: 6mA 11: 8mA [3:2]: TDM_DATA0, TDM_DATA1, TDM_DATA2, TDM_DATA3
3:2		I2C3_L	**Driving control of I2C3 IO** [0]: SCL3 0: Weak output low driving strength 1: Strong output low driving strength [1]: SDA3
1:0		I2C2_L	**Driving control of I2C2 IO** [0]: SCL2 0: Weak output low driving strength 1: Strong output low driving strength [1]: SDA2

10002104 DRV_CFG1_SET **DRV Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CONN_L							
Type									WO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CONN_L								I2S1_L				I2C3_L		I2C2_L	
Type	WO								WO				WO		WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:8		CONN_L	**Bitwise SET operation for driving control of CONN IO** 0: Keep 1: SET bits
7:4		I2S1_L	**Bitwise SET operation for driving control of I2S1**

Bit(s)	Mnemonic	Name	Description
			IO
3:2		I2C3_L	**Bitwise SET operation for driving control of I2C3 IO**
1:0		I2C2_L	**Bitwise SET operation for driving control of I2C2 IO**

10002108 DRV_CFG1_CLR DRV Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CONN_L							
Type									WO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CONN_L								I2S1_L				I2C3_L		I2C2_L	
Type	WO								WO				WO		WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:8		CONN_L	**Bitwise CLR operation for driving control of CONN IO** 0: Keep 1: CLR bits
7:4		I2S1_L	**Bitwise CLR operation for driving control of I2S1 IO**
3:2		I2C3_L	**Bitwise CLR operation for driving control of I2C3 IO**
1:0		I2C2_L	**Bitwise CLR operation for driving control of I2C2 IO**

10002110 PUDD_CFG0 PUPD Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								CONN_L								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		CONN_L	**Reserved** [8:0] Reserved

10002114 PUDD_CFG0_SET PUPD Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								CONN_L								
Type								WO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		CONN_L	**Reserved** 0: Keep 1: SET bits

10002118 PUDD_CFG0_CLR **PUPD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								CONN_L								
Type								WO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		CONN_L	**Reserved** 0: Keep 1: CLR bits

10002120 R0_CFG0 **R0 Control** **00000200**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							CAM_L	CONN_L								
Type							RW	RW								
Reset							1	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
9		CAM_L	**G control of CAM IO** [0]: CAM_CLK2 0: Analog GPIO mode 1: Digital GPIO mode
8:0		CONN_L	**Reserved** [8:0] Reserved

Bit(s)	Mnemonic	Name	Description

10002124 R0_CFG0_SET **R0 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							CAM_L	CONN_L								
Type							WO	WO								
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
9		CAM_L	**Bitwise SET operation for A control of CAM IO** 0: Keep 1: SET bits
8:0		CONN_L	**Reserved**

10002128 R0_CFG0_CLR **R0 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							CAM_L	CONN_L								
Type							WO	WO								
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
9		CAM_L	**Bitwise CLR operation for R0 control of CAM IO** 0: Keep 1: CLR bits
8:0		CONN_L	**Reserved**

10002130 R1_CFG0 **R1 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								CONN_L								
Type								RW								

Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		CONN_L	**Reserved** [8:0] Reserved

10002134 R1_CFG0_SET R1 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								CONN_L								
Type								WO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		CONN_L	**Reserved** 0: Keep 1: SET bits

10002138 R1_CFG0_CLR R1 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								CONN_L								
Type								WO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		CONN_L	**Reserved** 0: Keep 1: CLR bits

10002200 DUMMY DUMMY 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DUMMY							

Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		DUMMY	**Dummy register** [7:0]: Dummy register

10002204 DUMMY_SET DUMMY 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DUMMY							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		DUMMY	**Bitwise SET operation for dummy register** 0: Keep 1: SET bits

10002208 DUMMY_CLR DUMMY 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DUMMY							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		DUMMY	**Bitwise CLR operation for dummy register** 0: Keep 1: CLR bits

Module name: IO_CFG_B Base address: (+10002400h)

Address	Name	Width	Register Function
10002400	IES_CFG0	32	IES Control
10002404	IES_CFG0_SET	32	IES Control
10002408	IES_CFG0_CLR	32	IES Control
10002410	IES_CFG1	32	IES Control
10002414	IES_CFG1_SET	32	IES Control

Address	Name	Width	Register Function
10002418	IES_CFG1_CLR	32	IES Control
10002420	IES_CFG2	32	IES Control
10002424	IES_CFG2_SET	32	IES Control
10002428	IES_CFG2_CLR	32	IES Control
10002430	SR_CFG0	32	SR Control
10002434	SR_CFG0_SET	32	SR Control
10002438	SR_CFG0_CLR	32	SR Control
10002440	SR_CFG1	32	SR Control
10002444	SR_CFG1_SET	32	SR Control
10002448	SR_CFG1_CLR	32	SR Control
10002450	SMT_CFG0	32	SMT Control
10002454	SMT_CFG0_SET	32	SMT Control
10002458	SMT_CFG0_CLR	32	SMT Control
10002460	SMT_CFG1	32	SMT Control
10002464	SMT_CFG1_SET	32	SMT Control
10002468	SMT_CFG1_CLR	32	SMT Control
10002470	RDSEL_CFG0	32	RDSEL Control
10002474	RDSEL_CFG0_SET	32	RDSEL Control
10002478	RDSEL_CFG0_CLR	32	RDSEL Control
10002480	RDSEL_CFG1	32	RDSEL Control
10002484	RDSEL_CFG1_SET	32	RDSEL Control
10002488	RDSEL_CFG1_CLR	32	RDSEL Control
10002490	RDSEL_CFG2	32	RDSEL Control
10002494	RDSEL_CFG2_SET	32	RDSEL Control
10002498	RDSEL_CFG2_CLR	32	RDSEL Control
100024A0	RDSEL_CFG3	32	RDSEL Control
100024A4	RDSEL_CFG3_SET	32	RDSEL Control
100024A8	RDSEL_CFG3_CLR	32	RDSEL Control
100024B0	TDSEL_CFG0	32	TDSEL Control
100024B4	TDSEL_CFG0_SET	32	TDSEL Control
100024B8	TDSEL_CFG0_CLR	32	TDSEL Control
100024C0	TDSEL_CFG1	32	TDSEL Control
100024C4	TDSEL_CFG1_SET	32	TDSEL Control
100024C8	TDSEL_CFG1_CLR	32	TDSEL Control
100024D0	TDSEL_CFG2	32	TDSEL Control
100024D4	TDSEL_CFG2_SET	32	TDSEL Control
100024D8	TDSEL_CFG2_CLR	32	TDSEL Control
100024E0	TDSEL_CFG3	32	TDSEL Control
100024E4	TDSEL_CFG3_SET	32	TDSEL Control
100024E8	TDSEL_CFG3_CLR	32	TDSEL Control
100024F0	TDSEL_CFG4	32	TDSEL Control
100024F4	TDSEL_CFG4_SET	32	TDSEL Control
100024F8	TDSEL_CFG4_CLR	32	TDSEL Control

Address	Name	Width	Register Function
10002500	PUPD_CFG0	32	PUPD Control
10002504	PUPD_CFG0_SET	32	PUPD Control
10002508	PUPD_CFG0_CLR	32	PUPD Control
10002510	R0_CFG0	32	R0 Control
10002514	R0_CFG0_SET	32	R0 Control
10002518	R0_CFG0_CLR	32	R0 Control
10002520	R1_CFG0	32	R1 Control
10002524	R1_CFG0_SET	32	R1 Control
10002528	R1_CFG0_CLR	32	R1 Control
10002530	PD_CFG0	32	PD Control
10002534	PD_CFG0_SET	32	PD Control
10002538	PD_CFG0_CLR	32	PD Control
10002540	PD_CFG1	32	PD Control
10002544	PD_CFG1_SET	32	PD Control
10002548	PD_CFG1_CLR	32	PD Control
10002550	PD_CFG2	32	PD Control
10002554	PD_CFG2_SET	32	PD Control
10002558	PD_CFG2_CLR	32	PD Control
10002560	PU_CFG0	32	PU Control
10002564	PU_CFG0_SET	32	PU Control
10002568	PU_CFG0_CLR	32	PU Control
10002570	PU_CFG1	32	PU Control
10002574	PU_CFG1_SET	32	PU Control
10002578	PU_CFG1_CLR	32	PU Control
10002580	PU_CFG2	32	PU Control
10002584	PU_CFG2_SET	32	PU Control
10002588	PU_CFG2_CLR	32	PU Control
10002590	DRV_CFG0	32	DRV Control
10002594	DRV_CFG0_SET	32	DRV Control
10002598	DRV_CFG0_CLR	32	DRV Control
100025A0	DRV_CFG1	32	DRV Control
100025A4	DRV_CFG1_SET	32	DRV Control
100025A8	DRV_CFG1_CLR	32	DRV Control
100025B0	DRV_CFG2	32	DRV Control
100025B4	DRV_CFG2_SET	32	DRV Control
100025B8	DRV_CFG2_CLR	32	DRV Control
10002600	DUMMY	32	DUMMY
10002604	DUMMY_SET	32	DUMMY
10002608	DUMMY_CLR	32	DUMMY

10002400 IES_CFG0 IES Control FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	EINT_D															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D	SPIo_D							KEY_D						I2Co_D	
Type	RW	RW							RW						RW	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:15		EINT_D	**IES control of EINT IO** [9:0]: Reserved [10]: EINT10 0: Disable 1: Enable [11]: EINT11 [12]: EINT12 [13]: EINT13 [14]: EINT14 [15]: EINT15 [16]: EINT16
14:8		SPIo_D	**IES control of SPIo IO** [0]: SPIo_CK [1]: SPIo_MI [2]: SPIo_MO [3]: SPIo_CS [6:4]: Reserved
7:2		KEY_D	**IES control of KEY IO** [0]: KPROW0 [1]: KPROW1 [2]: KPROW2 [3]: KPCOL0 [4]: KPCOL1 [5]: KPCOL2
1:0		I2Co_D	**IES control of I2Co IO** [0]: SDA0 [1]: SCL0

10002404 IES_CFG0_SET IES Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_D															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D	SPIo_D							KEY_D						I2Co_D	
Type	WO	WO							WO						WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:15		EINT_D	**Bitwise SET operation for IES control of EINT IO** 0: Keep 1: SET bits
14:8		SPIo_D	**Bitwise SET operation for IES control of SPIo IO**

Bit(s)	Mnemonic	Name	Description
7:2		KEY_D	**Bitwise SET operation for IES control of KEY IO**
1:0		I2C0_D	**Bitwise SET operation for IES control of I2C0 IO**

10002408 IES_CFG0_CLR **IES Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_D															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D	SPI0_D							KEY_D						I2C0_D	
Type	WO	WO							WO						WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:15		EINT_D	**Bitwise CLR operation for IES control of EINT IO** 0: Keep 1: CLR bits
14:8		SPI0_D	**Bitwise CLR operation for IES control of SPI0 IO**
7:2		KEY_D	**Bitwise CLR operation for IES control of KEY IO**
1:0		I2C0_D	**Bitwise CLR operation for IES control of I2C0 IO**

10002410 IES_CFG1 **IES Control** **00FFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AUD_CTL_D			SPI3_D				I2S0_D
Type									RW			RW				RW
Reset									1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2S0_D				SPI2_D				I2C5_D		I2C4_D		SPI1_D			
Type	RW				RW				RW		RW		RW			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
23:21		AUD_CTL_D	**IES control of AUD_CTL IO** [0]: AUD_INTN 0: Disable 1: Enable [1]: AUD_PDN [2]: Reserved
20:17		SPI3_D	**IES control of SPI3 IO** [0]: SPI3_MI [1]: SPI3_MO [2]: SPI3_CK [3]: SPI3_CS
16:12		I2S0_D	**IES control of I2S0 IO** [0]: I2S0_LRCK [1]: I2S0_BCK [2]: I2S0_MCK

Bit(s)	Mnemonic	Name	Description
			[3]: I2S0_DI [4]: I2S3_DO
11:8		SPI2_D	**IES control of SPI2 IO** [0]: SPI2_CK [1]: SPI2_MI [2]: SPI2_MO [3]: SPI2_CS
7:6		I2C5_D	**IES control of I2C5 IO** [0]: SDA5 [1]: SCL5
5:4		I2C4_D	**IES control of I2C4 IO** [0]: SDA4 [1]: SCL4
3:0		SPI1_D	**IES control of SPI1 IO** [0]: SPI1_CK [1]: SPI1_MI [2]: SPI1_MO [3]: SPI1_CS

10002414 IES_CFG1_SET **IES Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AUD_CTL_D			SPI3_D				I2S0_D
Type									WO			WO				WO
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2S0_D				SPI2_D				I2C5_D		I2C4_D		SPI1_D			
Type	WO				WO				WO		WO		WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:21		AUD_CTL_D	**Bitwise SET operation for IES control of AUD_CTL IO** 0: Keep 1: SET bits
20:17		SPI3_D	**Bitwise SET operation for IES control of SPI3 IO**
16:12		I2S0_D	**Bitwise SET operation for IES control of I2S0 IO**
11:8		SPI2_D	**Bitwise SET operation for IES control of SPI2 IO**
7:6		I2C5_D	**Bitwise SET operation for IES control of I2C5 IO**
5:4		I2C4_D	**Bitwise SET operation for IES control of I2C4 IO**
3:0		SPI1_D	**Bitwise SET operation for IES control of SPI1 IO**

10002418 IES_CFG1_CLR **IES Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AUD_CTL_D			SPI3_D				I2S0_D
Type									WO			WO				WO
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	I2S0_D				SPI2_D				I2C5_D		I2C4_D		SPI1_D			
Type	WO				WO				WO		WO		WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:21		AUD_CTL_D	**Bitwise CLR operation for IES control of AUD_CTL IO** 0: Keep 1: CLR bits
20:17		SPI3_D	**Bitwise CLR operation for IES control of SPI3 IO**
16:12		I2S0_D	**Bitwise CLR operation for IES control of I2S0 IO**
11:8		SPI2_D	**Bitwise CLR operation for IES control of SPI2 IO**
7:6		I2C5_D	**Bitwise CLR operation for IES control of I2C5 IO**
5:4		I2C4_D	**Bitwise CLR operation for IES control of I2C4 IO**
3:0		SPI1_D	**Bitwise CLR operation for IES control of SPI1 IO**

10002420 IES_CFG2 **IES Control** **7FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		MSDC1_D						SIM2_D				SIM1_D				I2S2_D
Type		RW						RW				RW				RW
Reset		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2S2_D				MSDC0_D											
Type	RW				RW											
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30:25		MSDC1_D	**IES control of MSDC1 IO** [0]: MSDC1_CMD 0: Disable 1: Enable [1]: MSDC1_DAT0 [2]: MSDC1_DAT1 [3]: MSDC1_DAT2 [4]: MSDC1_DAT3 [5]: MSDC1_CLK
24:21		SIM2_D	**IES control of SIM2 IO** [0]: SIM2_SCLK [1]: SIM2_SRST [2]: SIM2_SIO [3]: INT_SIM2
20:17		SIM1_D	**IES control of SIM1 IO** [0]: SIM1_SCLK [1]: SIM1_SRST [2]: SIM1_SIO [3]: INT_SIM1
16:12		I2S2_D	**IES control of I2S2 IO** [0]: I2S1_LRCK [1]: I2S1_BCK [2]: I2S2_DI [3]: I2S1_DO [4]: I2S1_MCK
11:0		MSDC0_D	**IES control of MSDC0 IO** [0]: MSDC0_DAT0

Bit(s)	Mnemonic	Name	Description
			[1]: MSDC0_DAT1 [2]: MSDC0_DAT2 [3]: MSDC0_DAT3 [4]: MSDC0_DAT4 [5]: MSDC0_DAT5 [6]: MSDC0_DAT6 [7]: MSDC0_DAT7 [8]: MSDC0_CMD [9]: MSDC0_CLK [10]: MSDC0_DSL [11]: MSDC0_RSTB

10002424 IES_CFG2_SET **IES Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		MSDC1_D						SIM2_D				SIM1_D				I2S2_D
Type		WO						WO				WO				WO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2S2_D				MSDC0_D											
Type	WO				WO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:25		MSDC1_D	**Bitwise SET operation for IES control of MSDC1 IO** 0: Keep 1: SET bits
24:21		SIM2_D	**Bitwise SET operation for IES control of SIM2 IO**
20:17		SIM1_D	**Bitwise SET operation for IES control of SIM1 IO**
16:12		I2S2_D	**Bitwise SET operation for IES control of I2S2 IO**
11:0		MSDC0_D	**Bitwise SET operation for IES control of MSDC0 IO**

10002428 IES_CFG2_CLR **IES Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		MSDC1_D						SIM2_D				SIM1_D				I2S2_D
Type		WO						WO				WO				WO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2S2_D				MSDC0_D											
Type	WO				WO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:25		MSDC1_D	**Bitwise CLR operation for IES control of MSDC1 IO** 0: Keep

Bit(s)	Mnemonic	Name	Description
			1: CLR bits
24:21		SIM2_D	**Bitwise CLR operation for IES control of SIM2 IO**
20:17		SIM1_D	**Bitwise CLR operation for IES control of SIM1 IO**
16:12		I2S2_D	**Bitwise CLR operation for IES control of I2S2 IO**
11:0		MSDC0_D	**Bitwise CLR operation for IES control of MSDC0 IO**

10002430 SR_CFG0 SR Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MSDC1_D			I2S0_D					AUD_CTL_D		SPI3_D			MSDC0_D		
Type	RW			RW					RW		RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC0_D	SPI2_D		SPI1_D			EINT_D				SPI0_D			KEY_D		
Type	RW	RW		RW			RW				RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:29		MSDC1_D	**SR control of MSDC1 IO** [0]: MSDC1_CMD 0: Disable 1: Enable [1]: MSDC1_DAT0, MSDC1_DAT1, MSDC1_DAT2, MSDC1_DAT3 [2]: MSDC1_CLK
28:24		I2S0_D	**SR control of I2S0 IO** [0]: I2S0_LRCK [1]: I2S0_BCK [2]: I2S0_MCK [3]: I2S0_DI, I2S3_DO
23:22		AUD_CTL_D	**SR control of AUD_CTL IO** [0]: AUD_INTN [1]: AUD_PDN
21:19		SPI3_D	**SR control of SPI3 IO** [0]: SPI3_MI [1]: SPI3_MO [2]: SPI3_CS, SPI3_CK
18:15		MSDC0_D	**SR control of MSDC0 IO** [0]: MSDC0_DAT0, MSDC0_DAT1, MSDC0_DAT2, MSDC0_DAT3 [1]: MSDC0_DAT4, MSDC0_DAT5, MSDC0_DAT6, MSDC0_DAT7 [2]: MSDC0_CMD, MSDC0_DSL, MSDC0_RSTB [3]: MSDC0_CLK
14:12		SPI2_D	**SR control of SPI2 IO** [0]: SPI2_CK [1]: SPI2_MI [2]: SPI2_MO, SPI1_CS
11:9		SPI1_D	**SR control of SPI1 IO** [0]: SPI1_CK [1]: SPI1_MI [2]: SPI1_MO, SPI1_CS
8:5		EINT_D	**SR control of EINT IO**

Bit(s)	Mnemonic	Name	Description
			[1:0]: Reserved [2]: EINT10, EINT11 [3]: EINT12, EINT13, EINT14, EINT15, EINT16
4:2		SPI0_D	**SR control of SPI0 IO** [0]: SPI0_CK [1]: SPI0_MI [2]: SPI0_MO, SPI1_CS
1:0		KEY_D	**SR control of KEY IO** [0]: KPROW0, KPROW1, KPROW2 [1]: KPCOL0, KPCOL1, KPCOL2

10002434 SR_CFG0_SET SR Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MSDC1_D			I2S0_D					AUD_CTL_D		SPI3_D			MSDC0_D		
Type	WO			WO					WO		WO			WO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC0_D	SPI2_D			SPI1_D			EINT_D				SPI0_D			KEY_D	
Type	WO	WO			WO			WO				WO			WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:29		MSDC1_D	**Bitwise SET operation for SR control of MSDC1 IO** 0: Keep 1: SET bits
28:24		I2S0_D	**Bitwise SET operation for SR control of I2S0 IO**
23:22		AUD_CTL_D	**Bitwise SET operation for SR control of AUD_CTL IO**
21:19		SPI3_D	**Bitwise SET operation for SR control of SPI3 IO**
18:15		MSDC0_D	**Bitwise SET operation for SR control of MSDC0 IO**
14:12		SPI2_D	**Bitwise SET operation for SR control of SPI2 IO**
11:9		SPI1_D	**Bitwise SET operation for SR control of SPI1 IO**
8:5		EINT_D	**Bitwise SET operation for SR control of EINT IO**
4:2		SPI0_D	**Bitwise SET operation for SR control of SPI0 IO**
1:0		KEY_D	**Bitwise SET operation for SR control of KEY IO**

10002438 SR_CFG0_CLR SR Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MSDC1_D			I2S0_D					AUD_CTL_D		SPI3_D			MSDC0_D		
Type	WO			WO					WO		WO			WO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC0_D	SPI2_D			SPI1_D			EINT_D				SPI0_D			KEY_D	
Type	WO	WO			WO			WO				WO			WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:29		MSDC1_D	**Bitwise CLR operation for SR control of MSDC1 IO** 0: Keep 1: CLR bits
28:24		I2S0_D	**Bitwise CLR operation for SR control of I2S0 IO**
23:22		AUD_CTL_D	**Bitwise CLR operation for SR control of AUD_CTL IO**
21:19		SPI3_D	**Bitwise CLR operation for SR control of SPI3 IO**
18:15		MSDC0_D	**Bitwise CLR operation for SR control of MSDC0 IO**
14:12		SPI2_D	**Bitwise CLR operation for SR control of SPI2 IO**
11:9		SPI1_D	**Bitwise CLR operation for SR control of SPI1 IO**
8:5		EINT_D	**Bitwise CLR operation for SR control of EINT IO**
4:2		SPI0_D	**Bitwise CLR operation for SR control of SPI0 IO**
1:0		KEY_D	**Bitwise CLR operation for SR control of KEY IO**

10002440 SR_CFG1 **SR Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														SIM2_D		
Type														RW		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIM2_D			SIM1_D						I2S2_D			I2S3_D			
Type	RW			RW						RW			RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
18:13		SIM2_D	**SR control of SIM2 IO** [1:0]: SIM2_SCLK 0: Disable 1: Enable [3:2]: SIM2_SRST, SIM2_SIO [4]: Reserved [5]: INT_SIM2
12:7		SIM1_D	**SR control of SIM1 IO** [1:0]: SIM1_SCLK [3:2]: SIM1_SRST, SIM1_SIO [4]: Reserved [5]: INT_SIM1
6:4		I2S2_D	**SR control of I2S2 IO** [0]: I2S1_LRCK [1]: I2S1_BCK, I2S1_MCK [2]: I2S2_DI, I2S1_DO
3:0		I2S3_D	**Reserved** [3:0]: Reserved

10002444 SR_CFG1_SET **SR Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														SIM2_D		

Type														WO		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIM2_D			SIM1_D						I2S2_D			I2S3_D			
Type	WO			WO						WO			WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
18:13		SIM2_D	**Bitwise SET operation for SR control of SIM2 IO** 0: Keep 1: SET bits
12:7		SIM1_D	**Bitwise SET operation for SR control of SIM1 IO**
6:4		I2S2_D	**Bitwise SET operation for SR control of I2S2 IO**
3:0		I2S3_D	**Reserved**

10002448 SR_CFG1_CLR **SR Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														SIM2_D		
Type														WO		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIM2_D			SIM1_D						I2S2_D			I2S3_D			
Type	WO			WO						WO			WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
18:13		SIM2_D	**Bitwise CLR operation for SR control of SIM2 IO** 0: Keep 1: CLR bits
12:7		SIM1_D	**Bitwise CLR operation for SR control of SIM1 IO**
6:4		I2S2_D	**Bitwise CLR operation for SR control of I2S2 IO**
3:0		I2S3_D	**Reserved**

10002450 SMT_CFG0 **SMT Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SPI4_D			AUD_CTL_D		SPI3_D			SPI2_D	
Type							RW			RW		RW			RW	
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI2_D	I2C5_D	I2C4_D	SPI1_D			EINT_D			SPI0_D			KEY_D			I2C0_D
Type	RW	RW	RW	RW			RW			RW			RW			RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25:23		SPI4_D	**Reserved** [2:0]: Reserved

Bit(s)	Mnemonic	Name	Description
22:21		AUD_CTL_D	**SMT control of AUD_CTL IO** [0]: AUD_INTN 0: Disable 1: Enable [1]: AUD_PDN
20:18		SPI3_D	**SMT control of SPI3 IO** [0]: SPI3_MI [1]: SPI3_MO [2]: SPI3_CS, SPI3_CK
17:15		SPI2_D	**SMT control of SPI2 IO** [0]: SPI2_CK [1]: SPI2_MI [2]: SPI2_MO, SPI2_CS
14		I2C5_D	**SMT control of I2C5 IO** [0]: SCL5, SDA5
13		I2C4_D	**SMT control of I2C4 IO** [0]: SCL4, SDA4
12:10		SPI1_D	**SMT control of SPI1 IO** [0]: SPI1_CK [1]: SPI1_MI [2]: SPI1_MO, SPI1_CS
9:6		EINT_D	**SMT control of EINT IO** [1:0]: Reserved [2]: EINT10, EINT11 [3]: EINT12, EINT13, EINT14, EINT15, EINT16
5:3		SPI0_D	**SMT control of SPI0 IO** [0]: SPI0_CK [1]: SPI0_MI [2]: SPI0_MO, SPI0_CS
2:1		KEY_D	**SMT control of KEY IO** [0]: KPROW0, KPROW1, KPROW2 [1]: KPCOL0, KPCOL1, KPCOL2
0		I2C0_D	**SMT control of I2C0 IO** [0]: SCL0, SDA0

10002454 SMT_CFG0_SET **SMT Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SPI4_D			AUD_CTL_D		SPI3_D			SPI2_D	
Type							WO			WO		WO			WO	
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI2_D	I2C5_D	I2C4_D	SPI1_D			EINT_D			SPI0_D				KEY_D		I2C0_D
Type	WO	WO	WO	WO			WO			WO				WO		WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25:23		SPI4_D	**Reserved** 0: Keep 1: SET bits
22:21		AUD_CTL_D	**Bitwise SET operation for SMT control of AUD_CTL IO**
20:18		SPI3_D	**Bitwise SET operation for SMT control of SPI3 IO**

Bit(s)	Mnemonic	Name	Description
17:15		SPI2_D	**Bitwise SET operation for SMT control of SPI2 IO**
14		I2C5_D	**Bitwise SET operation for SMT control of I2C5 IO**
13		I2C4_D	**Bitwise SET operation for SMT control of I2C4 IO**
12:10		SPI1_D	**Bitwise SET operation for SMT control of SPI1 IO**
9:6		EINT_D	**Bitwise SET operation for SMT control of EINT IO**
5:3		SPI0_D	**Bitwise SET operation for SMT control of SPI0 IO**
2:1		KEY_D	**Bitwise SET operation for SMT control of KEY IO**
0		I2C0_D	**Bitwise SET operation for SMT control of I2C0 IO**

10002458 SMT_CFG0_CLR **SMT Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SPI4_D			AUD_CTL_D		SPI3_D			SPI2_D	
Type							WO			WO		WO			WO	
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI2_D	I2C5_D	I2C4_D	SPI1_D			EINT_D				SPI0_D			KEY_D		I2C0_D
Type	WO	WO	WO	WO			WO				WO			WO		WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25:23		SPI4_D	**Reserved** 0: Keep 1: CLR bits
22:21		AUD_CTL_D	**Bitwise CLR operation for SMT control of AUD_CTL IO**
20:18		SPI3_D	**Bitwise CLR operation for SMT control of SPI3 IO**
17:15		SPI2_D	**Bitwise CLR operation for SMT control of SPI2 IO**
14		I2C5_D	**Bitwise CLR operation for SMT control of I2C5 IO**
13		I2C4_D	**Bitwise CLR operation for SMT control of I2C4 IO**
12:10		SPI1_D	**Bitwise CLR operation for SMT control of SPI1 IO**
9:6		EINT_D	**Bitwise CLR operation for SMT control of EINT IO**
5:3		SPI0_D	**Bitwise CLR operation for SMT control of SPI0 IO**
2:1		KEY_D	**Bitwise CLR operation for SMT control of KEY IO**
0		I2C0_D	**Bitwise CLR operation for SMT control of I2C0 IO**

10002460 SMT_CFG1 SMT Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													MSDC1_D			SIM2_D
Type													RW			RW
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIM2_D		SIM1_D			I2S0_D				I2S2_D			MSDC0_D			
Type	RW		RW			RW				RW			RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:17		MSDC1_D	**SMT control of MSDC1 IO** [2:0]: Reserved
16:14		SIM2_D	**SMT control of SIM2 IO** [0]: SIM2_SCLK 0: Disable 1: Enable [1]: SIM2_SRST, SIM2_SIO [2]: INT_SIM2
13:11		SIM1_D	**SMT control of SIM1 IO** [0]: SIM1_SCLK [1]: SIM1_SRST, SIM1_SIO [2]: INT_SIM1
10:7		I2S0_D	**SMT control of I2S0 IO** [0]: I2S0_LRCK [1]: I2S0_BCK [2]: I2S0_MCK [3]: I2S0_DI, I2S3_DO
6:4		I2S2_D	**SMT control of I2S2 IO** [0]: I2S1_LRCK [1]: I2S1_BCK, I2S1_MCK [2]: I2S2_DI, I2S1_DO
3:0		MSDC0_D	**SMT control of MSDC0 IO** [0]: MSDC0_DAT0, MSDC0_DAT1, MSDC0_DAT2, MSDC0_DAT3 [1]: MSDC0_DAT4, MSDC0_DAT5, MSDC0_DAT6, MSDC0_DAT7 [2]: MSDC0_CMD, MSDC0_DSL, MSDC0_RSTB [3]: MSDC0_CLK

10002464 SMT_CFG1_SET SMT Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													MSDC1_D			SIM2_D
Type													WO			WO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIM2_D		SIM1_D			I2S0_D				I2S2_D			MSDC0_D			
Type	WO		WO			WO				WO			WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:17		MSDC1_D	**Bitwise SET operation for SMT control of MSDC1**

Bit(s)	Mnemonic	Name	Description
			IO 0: Keep 1: SET bits
16:14		SIM2_D	**Bitwise SET operation for SMT control of SIM2 IO**
13:11		SIM1_D	**Bitwise SET operation for SMT control of SIM1 IO**
10:7		I2S0_D	**Bitwise SET operation for SMT control of I2S0 IO**
6:4		I2S2_D	**Bitwise SET operation for SMT control of I2S2 IO**
3:0		MSDC0_D	**Bitwise SET operation for SMT control of MSDC0 IO**

10002468 SMT_CFG1_CLR **SMT Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													MSDC1_D			SIM2_D
Type													WO			WO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIM2_D		SIM1_D			I2S0_D				I2S2_D			MSDC0_D			
Type	WO		WO			WO				WO			WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:17		MSDC1_D	**Bitwise CLR operation for SMT control of MSDC1 IO** 0: Keep 1: CLR bits
16:14		SIM2_D	**Bitwise CLR operation for SMT control of SIM2 IO**
13:11		SIM1_D	**Bitwise CLR operation for SMT control of SIM1 IO**
10:7		I2S0_D	**Bitwise CLR operation for SMT control of I2S0 IO**
6:4		I2S2_D	**Bitwise CLR operation for SMT control of I2S2 IO**
3:0		MSDC0_D	**Bitwise CLR operation for SMT control of MSDC0 IO**

10002470 RDSEL_CFG0 **RDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AUD_CTL_D		AUD_I2S_D		SPI3_D		SPI2_D		I2C5_D		I2C4_D		SPI1_D	
Type			RW		RW		RW		RW		RW		RW		RW	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D								SPI0_D		KEY_D				I2C0_D	
Type	RW								RW		RW				RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:28		AUD_CTL_D	**RDSEL control of AUD_CTL IO** [1:0]: AUD_INTN, AUD_PDN
27:26		AUD_I2S_D	**Reserved** [1:0]: Reserved
25:24		SPI3_D	**RDSEL control of SPI3 IO** [1:0]: SPI3_CK, SPI3_MO, SPI3_MI, SPI3_CS
23:22		SPI2_D	**RDSEL control of SPI2 IO** [1:0]: SPI2_CK, SPI2_MO, SPI2_MI, SPI2_CS
21:20		I2C5_D	**RDSEL control of I2C5 IO** [1:0]: SCL5, SDA5
19:18		I2C4_D	**RDSEL control of I2C4 IO** [1:0]: SCL4, SDA4
17:16		SPI1_D	**RDSEL control of SPI1 IO** [1:0]: SPI1_CK, SPI1_MO, SPI1_MI, SPI1_CS
15:8		EINT_D	**RDSEL control of EINT IO** [3:0]: Reserved [5:4]: EINT10, EINT11 [7:6]: EINT12, EINT13, EINT14, EINT15, EINT16
7:6		SPI0_D	**RDSEL control of SPI0 IO** [1:0]: SPI0_CK, SPI0_MO, SPI0_MI, SPI0_CS
5:2		KEY_D	**RDSEL control of KEY IO** [1:0]: KPROW0, KPROW1, KPROW2 [3:2]: KPCOL0, KPCOL1, KPCOL2
1:0		I2C0_D	**RDSEL control of I2C0 IO** [1:0]: SCL0, SDA0

10002474 RDSEL_CFG0_SET **RDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AUD_CTL_D		AUD_I2S_D		SPI3_D		SPI2_D		I2C5_D		I2C4_D		SPI1_D	
Type			WO		WO		WO		WO		WO		WO		WO	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D								SPI0_D		KEY_D				I2C0_D	
Type	WO								WO		WO				WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:28		AUD_CTL_D	**Bitwise SET operation for RDSEL control of AUD_CTL IO** 0: Keep 1: SET bits
27:26		AUD_I2S_D	**Reserved**
25:24		SPI3_D	**Bitwise SET operation for RDSEL control of SPI3 IO**
23:22		SPI2_D	**Bitwise SET operation for RDSEL control of SPI2 IO**
21:20		I2C5_D	**Bitwise SET operation for RDSEL control of I2C5 IO**
19:18		I2C4_D	**Bitwise SET operation for RDSEL control of I2C4 IO**
17:16		SPI1_D	**Bitwise SET operation for RDSEL control of SPI1 IO**
15:8		EINT_D	**Bitwise SET operation for RDSEL control of EINT IO**

Bit(s)	Mnemonic	Name	Description
7:6		SPI0_D	**Bitwise SET operation for RDSEL control of SPI0 IO**
5:2		KEY_D	**Bitwise SET operation for RDSEL control of KEY IO**
1:0		I2C0_D	**Bitwise SET operation for RDSEL control of I2C0 IO**

10002478 RDSEL_CFG0_CLR **RDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AUD_CTL_D		AUD_I2S_D		SPI3_D		SPI2_D		I2C5_D		I2C4_D		SPI1_D	
Type			WO		WO		WO		WO		WO		WO		WO	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D								SPI0_D		KEY_D				I2C0_D	
Type	WO								WO		WO				WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:28		AUD_CTL_D	**Bitwise CLR operation for RDSEL control of AUD_CTL IO** 0: Keep 1: CLR bits
27:26		AUD_I2S_D	**Reserved**
25:24		SPI3_D	**Bitwise CLR operation for RDSEL control of SPI3 IO**
23:22		SPI2_D	**Bitwise CLR operation for RDSEL control of SPI2 IO**
21:20		I2C5_D	**Bitwise CLR operation for RDSEL control of I2C5 IO**
19:18		I2C4_D	**Bitwise CLR operation for RDSEL control of I2C4 IO**
17:16		SPI1_D	**Bitwise CLR operation for RDSEL control of SPI1 IO**
15:8		EINT_D	**Bitwise CLR operation for RDSEL control of EINT IO**
7:6		SPI0_D	**Bitwise CLR operation for RDSEL control of SPI0 IO**
5:2		KEY_D	**Bitwise CLR operation for RDSEL control of KEY IO**
1:0		I2C0_D	**Bitwise CLR operation for RDSEL control of I2C0 IO**

10002480 RDSEL_CFG1 **RDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SIM1_D												MSDC0_D	
Type			RW												RW	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC0_D															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:18		SIM1_D	**RDSEL control of SIM1 IO** [5:0]: SIM1_SCLK [11:6]: INT_SIM1, SIM1_SRST, SIM1_SIO
17:0		MSDC0_D	**RDSEL control of MSDC0 IO** [5:0]: MSDC0_DAT0, MSDC0_DAT1, MSDC0_DAT2, MSDC0_DAT3 [11:6]: MSDC0_DAT4, MSDC0_DAT5, MSDC0_DAT6, MSDC0_DAT7 [17:12]: MSDC0_CMD, MSDC0_DSL, MSDC0_RSTB, MSDC0_CLK

10002484 RDSEL_CFG1_SET RDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SIM1_D												MSDC0_D	
Type			WO												WO	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC0_D															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:18		SIM1_D	**Bitwise SET operation for RDSEL control of SIM1 IO** 0: Keep 1: SET bits
17:0		MSDC0_D	**Bitwise SET operation for RDSEL control of MSDC0 IO**

10002488 RDSEL_CFG1_CLR RDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SIM1_D												MSDC0_D	
Type			WO												WO	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC0_D															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:18		SIM1_D	**Bitwise CLR operation for RDSEL control of SIM1 IO** 0: Keep 1: CLR bits
17:0		MSDC0_D	**Bitwise CLR operation for RDSEL control of MSDC0 IO**

Bit(s)	Mnemonic	Name	Description

10002490 RDSEL_CFG2 RDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					SIM2_D											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2S1_D								I2S0_D							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16		SIM2_D	**RDSEL control of SIM2 IO** [5:0]: SIM2_SCLK [11:6]: INT_SIM2, SIM2_SRST, SIM2_SIO
15:8		I2S1_D	**Reserved** [7:0]: Reserved
7:0		I2S0_D	**RDSEL control of I2S0 IO** [1:0]: I2S0_LRCK [3:2]: I2S0_BCK [5:4]: I2S0_MCK [7:6]: I2S0_DI, I2S3_DO

10002494 RDSEL_CFG2_SET RDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					SIM2_D											
Type					WO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2S1_D								I2S0_D							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16		SIM2_D	**Bitwise SET operation for RDSEL control of SIM2 IO** 0: Keep 1: SET bits
15:8		I2S1_D	**Reserved**
7:0		I2S0_D	**Bitwise SET operation for RDSEL control of I2S0 IO**

10002498 RDSEL_CFG2_CLR RDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					SIM2_D											

Type					WO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2S1_D								I2S0_D							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16		SIM2_D	**Bitwise CLR operation for RDSEL control of SIM2 IO** 0: Keep 1: CLR bits
15:8		I2S1_D	**Reserved**
7:0		I2S0_D	**Bitwise CLR operation for RDSEL control of I2S0 IO**

100024A0 RDSEL_CFG3 **RDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							MSDC1_D									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC1_D								I2S2_D							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25:8		MSDC1_D	**RDSEL control of MSDC1 IO** Suggested value: 0x0 for 1.8V mode, 0x0C for 3.0V mode [5:0]: MSDC1_CMD [11:6]: MSDC1_DAT0, MSDC1_DAT1, MSDC1_DAT2, MSDC1_DAT3 [17:12]: MSDC1_CLK
7:0		I2S2_D	**RDSEL control of I2S2 IO** [1:0]: I2S1_LRCK [3:2]: I2S1_BCK [5:4]: I2S1_MCK [7:6]: I2S2_DI, I2S1_DO

100024A4 RDSEL_CFG3_SET **RDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							MSDC1_D									
Type							WO									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC1_D								I2S2_D							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25:8		MSDC1_D	**Bitwise SET operation for RDSEL control of MSDC1 IO** 0: Keep 1: SET bits
7:0		I2S2_D	**Bitwise SET operation for RDSEL control of I2S2 IO**

100024A8 RDSEL_CFG3_CLR **RDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							MSDC1_D									
Type							WO									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC1_D								I2S2_D							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25:8		MSDC1_D	**Bitwise CLR operation for RDSEL control of MSDC1 IO** 0: Keep 1: CLR bits
7:0		I2S2_D	**Bitwise CLR operation for RDSEL control of I2S2 IO**

100024B0 TDSEL_CFG0 **TDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_D															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI0_D				KEY_D								I2C0_D			
Type	RW				RW								RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		EINT_D	**TDSEL control of EINT IO** [7:0]: Reserved [11:8]: EINT10, EINT11 [15:12]: EINT12, EINT13, EINT14, EINT15, EINT16
15:12		SPI0_D	**TDSEL control of SPI0 IO** [3:0]: SPI0_CK, SPI0_MO, SPI0_MI, SPI0_CS
11:4		KEY_D	**TDSEL control of KEY IO** [3:0]: KPROW0, KPROW1, KPROW2 [7:4]: KPCOL0, KPCOL1, KPCOL2
3:0		I2C0_D	**TDSEL control of I2C0 IO** [3:0]: SCL0, SDA0

Bit(s)	Mnemonic	Name	Description

100024B4 TDSEL_CFG0_SET **TDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_D															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI0_D				KEY_D								I2C0_D			
Type	WO				WO								WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		EINT_D	**Bitwise SET operation for TDSEL control of EINT IO** 0: Keep 1: SET bits
15:12		SPI0_D	**Bitwise SET operation for TDSEL control of SPI0 IO**
11:4		KEY_D	**Bitwise SET operation for TDSEL control of KEY IO**
3:0		I2C0_D	**Bitwise SET operation for TDSEL control of I2C0 IO**

100024B8 TDSEL_CFG0_CLR **TDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_D															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI0_D				KEY_D								I2C0_D			
Type	WO				WO								WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		EINT_D	**Bitwise CLR operation for TDSEL control of EINT IO** 0: Keep 1: CLR bits
15:12		SPI0_D	**Bitwise CLR operation for TDSEL control of SPI0 IO**
11:4		KEY_D	**Bitwise CLR operation for TDSEL control of KEY IO**
3:0		I2C0_D	**Bitwise CLR operation for TDSEL control of I2C0 IO**

100024C0 TDSEL_CFG1 **TDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI3_D				MSDC1_D											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI2_D				I2C5_D				I2C4_D				SPI1_D			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		SPI3_D	**TDSEL control of SPI3 IO** [3:0]: SPI3_CK, SPI3_MO, SPI3_MI, SPI3_CS
27:16		MSDC1_D	**TDSEL control of MSDC1 IO** Suggested value: 0xA [3:0]: MSDC1_CMD [7:4]: MSDC1_DAT0, MSDC1_DAT1, MSDC1_DAT2, MSDC1_DAT3 [11:8]: MSDC1_CLK
15:12		SPI2_D	**TDSEL control of SPI2 IO** [3:0]: SPI2_CK, SPI2_MO, SPI2_MI, SPI2_CS
11:8		I2C5_D	**TDSEL control of I2C5 IO** [3:0]: SCL5, SDA5
7:4		I2C4_D	**TDSEL control of I2C4 IO** [3:0]: SCL4, SDA4
3:0		SPI1_D	**TDSEL control of SPI1 IO** [3:0]: SPI1_CK, SPI1_MO, SPI1_MI, SPI1_CS

100024C4 TDSEL_CFG1_SET **TDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI3_D				MSDC1_D											
Type	WO				WO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI2_D				I2C5_D				I2C4_D				SPI1_D			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		SPI3_D	**Bitwise SET operation for TDSEL control of SPI3 IO** 0: Keep 1: SET bits
27:16		MSDC1_D	**Bitwise SET operation for TDSEL control of MSDC1 IO**
15:12		SPI2_D	**Bitwise SET operation for TDSEL control of SPI2 IO**
11:8		I2C5_D	**Bitwise SET operation for TDSEL control of I2C5 IO**
7:4		I2C4_D	**Bitwise SET operation for TDSEL control of I2C4 IO**
3:0		SPI1_D	**Bitwise SET operation for TDSEL control of SPI1 IO**

100024C8 TDSEL_CFG1_CLR **TDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI3_D				MSDC1_D											
Type	WO				WO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI2_D				I2C5_D				I2C4_D				SPI1_D			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		SPI3_D	**Bitwise CLR operation for TDSEL control of SPI3 IO** 0: Keep 1: CLR bits
27:16		MSDC1_D	**Bitwise CLR operation for TDSEL control of MSDC1 IO**
15:12		SPI2_D	**Bitwise CLR operation for TDSEL control of SPI2 IO**
11:8		I2C5_D	**Bitwise CLR operation for TDSEL control of I2C5 IO**
7:4		I2C4_D	**Bitwise CLR operation for TDSEL control of I2C4 IO**
3:0		SPI1_D	**Bitwise CLR operation for TDSEL control of SPI1 IO**

100024D0 TDSEL_CFG2 **TDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SIM2_D								SIM1_D							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC0_D															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		SIM2_D	**TDSEL control of SIM2 IO** Suggested value: 0xA [3:0]: SIM2_SCLK [7:4]: INT_SIM2, SIM2_SRST, SIM2_SIO
23:16		SIM1_D	**TDSEL control of SIM1 IO** Suggested value: 0xA [3:0]: SIM1_SCLK [7:4]: INT_SIM1, SIM1_SRST, SIM1_SIO
15:0		MSDC0_D	**TDSEL control of MSDC0 IO** [3:0]: MSDC0_DAT0, MSDC0_DAT1, MSDC0_DAT2, MSDC0_DAT3 [7:4]: MSDC0_DAT4, MSDC0_DAT5, MSDC0_DAT6, MSDC0_DAT7 [11:8]: MSDC0_CMD, MSDC0_DSL, MSDC0_RSTB [15:12]: MSDC0_CLK

100024D4 TDSEL_CFG2_SET **TDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SIM2_D								SIM1_D							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC0_D															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		SIM2_D	**Bitwise SET operation for TDSEL control of SIM2 IO** 0: Keep 1: SET bits
23:16		SIM1_D	**Bitwise SET operation for TDSEL control of SIM1 IO**
15:0		MSDC0_D	**Bitwise SET operation for TDSEL control of MSDC0 IO**

100024D8 TDSEL_CFG2_CLR **TDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SIM2_D								SIM1_D							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC0_D															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		SIM2_D	**Bitwise CLR operation for TDSEL control of SIM2 IO** 0: Keep 1: CLR bits
23:16		SIM1_D	**Bitwise CLR operation for TDSEL control of SIM1 IO**
15:0		MSDC0_D	**Bitwise CLR operation for TDSEL control of MSDC0 IO**

100024E0 TDSEL_CFG3 **TDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I2S2_D															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2S0_D															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		I2S2_D	**TDSEL control of I2S2 IO** [3:0]: I2S1_LRCK [7:4]: I2S1_BCK [11:8]: I2S1_MCK [15:12]: I2S2_DI, I2S1_DO
15:0		I2S0_D	**TDSEL control of I2S0 IO** [3:0]: I2S0_LRCK [7:4]: I2S0_BCK [11:8]: I2S0_MCK [15:12]: I2S0_DI, I2S3_DO

100024E4 TDSEL_CFG3_SET TDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I2S2_D															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2S0_D															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		I2S2_D	**Bitwise SET operation for TDSEL control of I2S2 IO** 0: Keep 1: SET bits
15:0		I2S0_D	**Bitwise SET operation for TDSEL control of I2S0 IO**

100024E8 TDSEL_CFG3_CLR TDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I2S2_D															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2S0_D															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		I2S2_D	**Bitwise CLR operation for TDSEL control of I2S2 IO** 0: Keep 1: CLR bits
15:0		I2S0_D	**Bitwise CLR operation for TDSEL control of I2S0**

Bit(s)	Mnemonic	Name	Description
			IO

100024F0 TDSEL_CFG4 TDSEL Control 000000F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SLP				AUD_CTL_D			
Type									RW				RW			
Reset									1	1	1	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:4		SLP	**TDSEL value for sleep mode** [3:0]: TDSEL value of IOs in bottom side in sleep mode Suggested value: 0xF
3:0		AUD_CTL_D	**TDSEL control of AUD_CTL IO** [3:0]: AUD_INTN, AUD_PDN

100024F4 TDSEL_CFG4_SET TDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SLP				AUD_CTL_D			
Type									WO				WO			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:4		SLP	**Bitwise CLR operation for TDSEL value fpr Sleep mode** 0: Keep 1: SET bits
3:0		AUD_CTL_D	**Bitwise SET operation for TDSEL control of AUD_CTL IO**

100024F8 TDSEL_CFG4_CLR TDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name									SLP				AUD_CTL_D			
Type									WO				WO			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:4		SLP	**Bitwise CLR operation for TDSEL value fpr Sleep mode** 0: Keep 1: CLR bits
3:0		AUD_CTL_D	**Bitwise CLR operation for TDSEL control of AUD_CTL IO**

10002500 PUPD_CFG0 PUPD Control 3F818036

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SIM2_D			SIM1_D			MSDC1_D						MSDC0_D	
Type			RW			RW			RW						RW	
Reset			1	1	1	1	1	1	1	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC0_D										KEY_D					
Type	RW										RW					
Reset	1	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0

Bit(s)	Mnemonic	Name	Description
29:27		SIM2_D	**PUPD control of SIM2 IO** [0]: SIM2_SCLK PUPD/R1/R0: 0/0/0: High-Z 0/0/1: Pull-up with 20Kohm 0/1/0: Pull-up with 5Kohm 0/1/1: Pull-up with 5Kohm//20Kohm 1/0/0: High-Z 1/0/1: Pull-down with 75Kohm 1/1/0: Pull-down with 75Kohm 1/1/1: Pull-down with 75Kohm//75Kohm [1]: SIM2_SRST [2]: SIM2_SIO
26:24		SIM1_D	**PUPD control of SIM1 IO** [0]: SIM1_SCLK PUPD/R1/R0: 0/0/0: High-Z 0/0/1: Pull-up with 20Kohm 0/1/0: Pull-up with 5Kohm 0/1/1: Pull-up with 5Kohm//20Kohm 1/0/0: High-Z 1/0/1: Pull-down with 75Kohm 1/1/0: Pull-down with 75Kohm 1/1/1: Pull-down with 75Kohm//75Kohm [1]: SIM1_SRST [2]: SIM1_SIO
23:18		MSDC1_D	**PUPD control of MSDC1 IO** [0]: MSDC1_CMD PUPD/R1/R0: 0/0/0: High-Z 0/0/1: Pull-up with 10Kohm 0/1/0: Pull-up with 50Kohm

Bit(s)	Mnemonic	Name	Description
			0/1/1: Pull-up with 10Kohm//50Kohm 1/0/0: High-Z 1/0/1: Pull-down with 10Kohm 1/1/0: Pull-down with 50Kohm 1/1/1: Pull-down with 10Kohm//50Kohm [1]: MSDC1_DAT0 [2]: MSDC1_DAT1 [3]: MSDC1_DAT2 [4]: MSDC1_DAT3 [5]: MSDC1_CLK
17:6		MSDC0_D	**PUPD control of MSDC0 IO** [0]: MSDC0_DAT0 PUPD/R1/R0: 0/0/0: High-Z 0/0/1: Pull-up with 10Kohm 0/1/0: Pull-up with 50Kohm 0/1/1: Pull-up with 10Kohm//50Kohm 1/0/0: High-Z 1/0/1: Pull-down with 10Kohm 1/1/0: Pull-down with 50Kohm 1/1/1: Pull-down with 10Kohm//50Kohm [1]: MSDC0_DAT1 [2]: MSDC0_DAT2 [3]: MSDC0_DAT3 [4]: MSDC0_DAT4 [5]: MSDC0_DAT5 [6]: MSDC0_DAT6 [7]: MSDC0_DAT7 [8]: MSDC0_CMD [9]: MSDC0_CLK [10]: MSDC0_DSL [11]: MSDC0_RSTB
5:0		KEY_D	**PUPD control of KEY IO** [0]: KPCOL0 PUPD/R1/R0: 0/0/0: High-Z 0/0/1: Pull-up with 75Kohm 0/1/0: Pull-up with 200Kohm 0/1/1: Pull-up with 75Kohm//200Kohm 1/0/0: High-Z 1/0/1: Pull-down with 75Kohm 1/1/0: Pull-down with 200Kohm 1/1/1: Pull-down with 75Kohm//200Kohm [1]: KPCOL1 [2]: KPCOL2 [3]: KPROW0 PUPD/R1/R0: 0/0/0: High-Z 0/0/1: Pull-up with 75Kohm 0/1/0: Pull-up with 2Kohm 0/1/1: Pull-up with 2Kohm//75Kohm 1/0/0: High-Z 1/0/1: Pull-down with 75Kohm 1/1/0: Pull-down with 2Kohm 1/1/1: Pull-down with 2Kohm//75Kohm [4]: KPROW1 [5]: KPROW2

10002504 PUPD_CFG0_SET **PUPD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SIM2_D			SIM1_D			MSDC1_D						MSDC0_D	
Type			WO			WO			WO						WO	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC0_D										KEY_D					
Type	WO										WO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:27		SIM2_D	**Bitwise SET operation for PUPD control of SIM2 IO** 0: Keep 1: SET bits
26:24		SIM1_D	**Bitwise SET operation for PUPD control of SIM1 IO**
23:18		MSDC1_D	**Bitwise SET operation for PUPD control of MSDC1 IO**
17:6		MSDC0_D	**Bitwise SET operation for PUPD control of MSDC0 IO**
5:0		KEY_D	**Bitwise SET operation for PUPD control of KEY IO**

10002508 PUPD_CFG0_CLR **PUPD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SIM2_D			SIM1_D			MSDC1_D						MSDC0_D	
Type			WO			WO			WO						WO	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC0_D										KEY_D					
Type	WO										WO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:27		SIM2_D	**Bitwise CLR operation for PUPD control of SIM2 IO** 0: Keep 1: CLR bits
26:24		SIM1_D	**Bitwise CLR operation for PUPD control of SIM1 IO**
23:18		MSDC1_D	**Bitwise CLR operation for PUPD control of MSDC1 IO**
17:6		MSDC0_D	**Bitwise CLR operation for PUPD control of MSDC0 IO**
5:0		KEY_D	**Bitwise CLR operation for PUPD control of KEY IO**

10002510 R0_CFG0 **R0 Control** **40000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		EINT_D	SIM2_D			SIM1_D			MSDC1_D						MSDCo_D	
Type		RW	RW			RW			RW						RW	
Reset		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDCo_D										KEY_D					
Type	RW										RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30		EINT_D	**G control of EINT IO** [0]: EINT16 0: Analog GPIO mode 1: Digital GPIO mode
29:27		SIM2_D	**Ro control of SIM2 IO** SIM mode: [R0:R1]=[1:0] or [1:1] [0]: SIM2_SCLK PUPD/R1/R0: 0/0/0: High-Z 0/0/1: Pull-up with 20Kohm 0/1/0: Pull-up with 5Kohm 0/1/1: Pull-up with 5Kohm//20Kohm 1/0/0: High-Z 1/0/1: Pull-down with 75Kohm 1/1/0: Pull-down with 75Kohm 1/1/1: Pull-down with 75Kohm//75Kohm [1]: SIM2_SRST [2]: SIM2_SIO
26:24		SIM1_D	**Ro control of SIM1 IO** SIM mode: [R0:R1]=[1:0] or [1:1] [0]: SIM1_SCLK PUPD/R1/R0: 0/0/0: High-Z 0/0/1: Pull-up with 20Kohm 0/1/0: Pull-up with 5Kohm 0/1/1: Pull-up with 5Kohm//20Kohm 1/0/0: High-Z 1/0/1: Pull-down with 75Kohm 1/1/0: Pull-down with 75Kohm 1/1/1: Pull-down with 75Kohm//75Kohm [1]: SIM1_SRST [2]: SIM1_SIO
23:18		MSDC1_D	**Ro control of MSDC1 IO** [0]: MSDC1_CMD PUPD/R1/R0: 0/0/0: High-Z 0/0/1: Pull-up with 10Kohm 0/1/0: Pull-up with 50Kohm 0/1/0: Pull-up with 10Kohm//50Kohm 1/0/0: High-Z 1/0/1: Pull-down with 10Kohm 1/1/0: Pull-down with 50Kohm 1/1/0: Pull-down with 10Kohm//50Kohm [1]: MSDC1_DAT0 [2]: MSDC1_DAT1 [3]: MSDC1_DAT2 [4]: MSDC1_DAT3 [5]: MSDC1_CLK

Bit(s)	Mnemonic	Name	Description
17:6		MSDC0_D	**R0 control of MSDC0 IO** [0]: MSDC0_DAT0 PUPD/R1/R0: 0/0/0: High-Z 0/0/1: Pull-up with 10Kohm 0/1/0: Pull-up with 50Kohm 0/1/1: Pull-up with 10Kohm//50Kohm 1/0/0: High-Z 1/0/1: Pull-down with 10Kohm 1/1/0: Pull-down with 50Kohm 1/1/1: Pull-down with 10Kohm//50Kohm [1]: MSDC0_DAT1 [2]: MSDC0_DAT2 [3]: MSDC0_DAT3 [4]: MSDC0_DAT4 [5]: MSDC0_DAT5 [6]: MSDC0_DAT6 [7]: MSDC0_DAT7 [8]: MSDC0_CMD [9]: MSDC0_CLK [10]: MSDC0_DSL [11]: MSDC0_RSTB
5:0		KEY_D	**R0 control of KEY IO** [0]: KPCOL0 PUPD/R1/R0: 0/0/0: High-Z 0/0/1: Pull-up with 75Kohm 0/1/0: Pull-up with 200Kohm 0/1/1: Pull-up with 75Kohm//200Kohm 1/0/0: High-Z 1/0/1: Pull-down with 75Kohm 1/1/0: Pull-down with 200Kohm 1/1/1: Pull-down with 75Kohm//200Kohm [1]: KPCOL1 [2]: KPCOL2 [3]: KPROW0 PUPD/R1/R0: 0/0/0: High-Z 0/0/1: Pull-up with 75Kohm 0/1/0: Pull-up with 2Kohm 0/1/1: Pull-up with 2Kohm//75Kohm 1/0/0: High-Z 1/0/1: Pull-down with 75Kohm 1/1/0: Pull-down with 2Kohm 1/1/1: Pull-down with 2Kohm//75Kohm [4]: KPROW1 [5]: KPROW2

10002514 R0_CFG0_SET **R0 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		EINT_D	SIM2_D			SIM1_D			MSDC1_D						MSDC0_D	
Type		WO	WO			WO			WO						WO	
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC0_D										KEY_D					

Type	WO										WO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30		EINT_D	**Bitwise SET operation for R0 control of EINT IO** 0: Keep 1: SET bits
29:27		SIM2_D	**Bitwise SET operation for R0 control of SIM2 IO**
26:24		SIM1_D	**Bitwise SET operation for R0 control of SIM1 IO**
23:18		MSDC1_D	**Bitwise SET operation for R0 control of MSDC1 IO**
17:6		MSDC0_D	**Bitwise SET operation for R0 control of MSDC0 IO**
5:0		KEY_D	**Bitwise SET operation for R0 control of KEY IO**

10002518 R0_CFG0_CLR **R0 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		EINT_D	SIM2_D			SIM1_D			MSDC1_D						MSDC0_D	
Type		WO	WO			WO			WO						WO	
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC0_D										KEY_D					
Type	WO										WO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30		EINT_D	**Bitwise CLR operation for R0 control of EINT IO** 0: Keep 1: CLR bits
29:27		SIM2_D	**Bitwise CLR operation for R0 control of SIM2 IO**
26:24		SIM1_D	**Bitwise CLR operation for R0 control of SIM1 IO**
23:18		MSDC1_D	**Bitwise CLR operation for R0 control of MSDC1 IO**
17:6		MSDC0_D	**Bitwise CLR operation for R0 control of MSDC0 IO**
5:0		KEY_D	**Bitwise CLR operation for R0 control of KEY IO**

10002520 R1_CFG0 **R1 Control** **3FFFFFF7**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SIM2_D			SIM1_D			MSDC1_D						MSDC0_D	
Type			RW			RW			RW						RW	
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC0_D										KEY_D					
Type	RW										RW					
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1

Bit(s)	Mnemonic	Name	Description
29:27		SIM2_D	**R1 control of SIM2 IO** SIM mode: [R0:R1]=[1:0] or [1:1] [0]: SIM2_SCLK PUPD/R1/R0: 0/0/0: High-Z 0/0/1: Pull-up with 20Kohm 0/1/0: Pull-up with 5Kohm 0/1/1: Pull-up with 5Kohm//20Kohm 1/0/0: High-Z 1/0/1: Pull-down with 75Kohm 1/1/0: Pull-down with 75Kohm 1/1/1: Pull-down with 75Kohm//75Kohm [1]: SIM2_SRST [2]: SIM2_SIO
26:24		SIM1_D	**R1 control of SIM1 IO** SIM mode: [R0:R1]=[1:0] or [1:1] [0]: SIM1_SCLK PUPD/R1/R0: 0/0/0: High-Z 0/0/1: Pull-up with 20Kohm 0/1/0: Pull-up with 5Kohm 0/1/1: Pull-up with 5Kohm//20Kohm 1/0/0: High-Z 1/0/1: Pull-down with 75Kohm 1/1/0: Pull-down with 75Kohm 1/1/1: Pull-down with 75Kohm//75Kohm [1]: SIM1_SRST [2]: SIM1_SIO
23:18		MSDC1_D	**R1 control of MSDC1 IO** [0]: MSDC1_CMD PUPD/R1/R0: 0/0/0: High-Z 0/0/1: Pull-up with 10Kohm 0/1/0: Pull-up with 50Kohm 0/1/1: Pull-up with 10Kohm//50Kohm 1/0/0: High-Z 1/0/1: Pull-down with 10Kohm 1/1/0: Pull-down with 50Kohm 1/1/1: Pull-down with 10Kohm//50Kohm [1]: MSDC1_DAT0 [2]: MSDC1_DAT1 [3]: MSDC1_DAT2 [4]: MSDC1_DAT3 [5]: MSDC1_CLK
17:6		MSDC0_D	**R1 control of MSDC0 IO** [0]: MSDC0_DAT0 PUPD/R1/R0: 0/0/0: High-Z 0/0/1: Pull-up with 10Kohm 0/1/0: Pull-up with 50Kohm 0/1/1: Pull-up with 10Kohm//50Kohm 1/0/0: High-Z 1/0/1: Pull-down with 10Kohm 1/1/0: Pull-down with 50Kohm 1/1/1: Pull-down with 10Kohm//50Kohm [1]: MSDC0_DAT1 [2]: MSDC0_DAT2 [3]: MSDC0_DAT3 [4]: MSDC0_DAT4 [5]: MSDC0_DAT5 [6]: MSDC0_DAT6

Bit(s)	Mnemonic	Name	Description
			[7]: MSDC0_DAT7 [8]: MSDC0_CMD [9]: MSDC0_CLK [10]: MSDC0_DSL [11]: MSDC0_RSTB
5:0		KEY_D	**R1 control of KEY IO** [0]: KPCOL0 PUPD/R1/R0: 0/0/0: High-Z 0/0/1: Pull-up with 75Kohm 0/1/0: Pull-up with 200Kohm 0/1/1: Pull-up with 75Kohm//200Kohm 1/0/0: High-Z 1/0/1: Pull-down with 75Kohm 1/1/0: Pull-down with 200Kohm 1/1/1: Pull-down with 75Kohm//200Kohm [1]: KPCOL1 [2]: KPCOL2 [3]: KPROW0 PUPD/R1/R0: 0/0/0: High-Z 0/0/1: Pull-up with 75Kohm 0/1/0: Pull-up with 2Kohm 0/1/1: Pull-up with 2Kohm//75Kohm 1/0/0: High-Z 1/0/1: Pull-down with 75Kohm 1/1/0: Pull-down with 2Kohm 1/1/1: Pull-down with 2Kohm//75Kohm [4]: KPROW1 [5]: KPROW2

10002524 R1_CFG0_SET **R1 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SIM2_D			SIM1_D			MSDC1_D						MSDC0_D	
Type			WO			WO			WO						WO	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC0_D										KEY_D					
Type	WO										WO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:27		SIM2_D	**Bitwise SET operation for R1 control of SIM2 IO** 0: Keep 1: SET bits
26:24		SIM1_D	**Bitwise SET operation for R1 control of SIM1 IO**
23:18		MSDC1_D	**Bitwise SET operation for R1 control of MSDC1 IO**
17:6		MSDC0_D	**Bitwise SET operation for R1 control of MSDC0 IO**
5:0		KEY_D	**Bitwise SET operation for R1 control of KEY IO**

10002528 R1_CFG0_CLR **R1 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SIM2_D			SIM1_D			MSDC1_D						MSDC0_D	
Type			WO			WO			WO						WO	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC0_D										KEY_D					
Type	WO										WO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:27		SIM2_D	**Bitwise CLR operation for R1 control of SIM2 IO** 0: Keep 1: CLR bits
26:24		SIM1_D	**Bitwise CLR operation for R1 control of SIM1 IO**
23:18		MSDC1_D	**Bitwise CLR operation for R1 control of MSDC1 IO**
17:6		MSDC0_D	**Bitwise CLR operation for R1 control of MSDC0 IO**
5:0		KEY_D	**Bitwise CLR operation for R1 control of KEY IO**

10002530 PD_CFG0 **PD Control** **07FFFFFC**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		I2C5_D		I2C4_D		SPI1_D				EINT_D						
Type		RW		RW		RW				RW						
Reset		0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D										SPI0_D				I2C0_D	
Type	RW										RW				RW	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
30:29		I2C5_D	**Pull-down control of I2C5 IO** [0]: SDA5 0: N/A 1: Pull down with 75Kohm [1]: SCL5
28:27		I2C4_D	**Pull-down control of I2C4 IO** [0]: SDA4 0: N/A 1: Pull down with 75Kohm [1]: SCL4
26:23		SPI1_D	**Pull-down control of SPI1 IO** [0]: SPI1_CK PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: SPI1_MI [2]: SPI1_MO [3]: SPI1_CS

Bit(s)	Mnemonic	Name	Description
22:6		EINT_D	**Pull-down control of EINT IO** [9:0]: Reserved PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [10]: EINT10 [11]: EINT11 [12]: EINT12 [13]: EINT13 [14]: EINT14 [15]: EINT15 [16]: EINT16
5:2		SPI0_D	**Pull-down control of SPI0 IO** [0]: SPI0_CK PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: SPI0_MI [2]: SPI0_MO [3]: SPI0_CS
1:0		I2C0_D	**Pull-down control of I2C0 IO** [0]: SDA0 0: N/A 1: Pull down with 75Kohm [1]: SCL0

10002534 PD_CFG0_SET **PD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		I2C5_D		I2C4_D		SPI1_D				EINT_D						
Type		WO		WO		WO				WO						
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D										SPI0_D				I2C0_D	
Type	WO										WO				WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:29		I2C5_D	**Bitwise SET operation for pull-down control of I2C5 IO** 0: Keep 1: SET bits
28:27		I2C4_D	**Bitwise SET operation for pull-down control of I2C4 IO**
26:23		SPI1_D	**Bitwise SET operation for pull-down control of SPI1 IO**
22:6		EINT_D	**Bitwise SET operation for pull-down control of EINT IO**
5:2		SPI0_D	**Bitwise SET operation for pull-down control of SPI0 IO**
1:0		I2C0_D	**Bitwise SET operation for pull-down control of**

Bit(s)	Mnemonic	Name	Description
			I2C0 IO

10002538 PD_CFG0_CLR **PD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		I2C5_D		I2C4_D		SPI1_D				EINT_D						
Type		WO		WO		WO				WO						
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D										SPI0_D				I2C0_D	
Type	WO										WO				WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:29		I2C5_D	**Bitwise CLR operation for pull-down control of I2C5 IO** 0: Keep 1: CLR bits
28:27		I2C4_D	**Bitwise CLR operation for pull-down control of I2C4 IO**
26:23		SPI1_D	**Bitwise CLR operation for pull-down control of SPI1 IO**
22:6		EINT_D	**Bitwise CLR operation for pull-down control of EINT IO**
5:2		SPI0_D	**Bitwise CLR operation for pull-down control of SPI0 IO**
1:0		I2C0_D	**Bitwise CLR operation for pull-down control of I2C0 IO**

10002540 PD_CFG1 **PD Control** **0E00FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					MSDC0_D											
Type					RW											
Reset					1	1	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUD_CTL_D			SPI3_D				I2S0_D					SPI2_D			
Type	RW			RW				RW					RW			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
27:16		MSDC0_D	**Pull-down control of MSDC0 IO** [11:0]: Reserved
15:13		AUD_CTL_D	**Pull-down control of AUD_CTL IO** [0]: AUD_INTN PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: AUD_PDN [2]: Reserved

Bit(s)	Mnemonic	Name	Description
12:9		SPI3_D	**Pull-down control of SPI3 IO** [0]: SPI3_MI PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: SPI3_MO [2]: SPI3_CK [3]: SPI3_CS
8:4		I2S0_D	**Pull-down control of I2S0 IO** [0]: I2S0_LRCK PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: I2S0_BCK [2]: I2S0_MCK [3]: I2S0_DI [4]: I2S3_DO
3:0		SPI2_D	**Pull-down control of SPI2 IO** [0]: SPI2_CK PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: SPI2_MI [2]: SPI2_MO [3]: SPI2_CS

10002544 PD_CFG1_SET **PD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					MSDC0_D											
Type					WO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUD_CTL_D			SPI3_D				I2S0_D					SPI2_D			
Type	WO			WO				WO					WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16		MSDC0_D	**Bitwise SET operation for pull-down control of MSDC0 IO** 0: Keep 1: SET bits
15:13		AUD_CTL_D	**Bitwise SET operation for pull-down control of AUD_CTL IO**
12:9		SPI3_D	**Bitwise SET operation for pull-down control of SPI3 IO**
8:4		I2S0_D	**Bitwise SET operation for pull-down control of I2S0 IO**
3:0		SPI2_D	**Bitwise SET operation for pull-down control of**

Bit(s)	Mnemonic	Name	Description
			SPI2 IO

10002548 PD_CFG1_CLR **PD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					MSDC0_D											
Type					WO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUD_CTL_D			SPI3_D				I2S0_D					SPI2_D			
Type	WO			WO				WO					WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16		MSDC0_D	**Bitwise CLR operation for pull-down control of MSDC0 IO** 0: Keep 1: CLR bits
15:13		AUD_CTL_D	**Bitwise CLR operation for pull-down control of AUD_CTL IO**
12:9		SPI3_D	**Bitwise CLR operation for pull-down control of SPI3 IO**
8:4		I2S0_D	**Bitwise CLR operation for pull-down control of I2S0 IO**
3:0		SPI2_D	**Bitwise CLR operation for pull-down control of SPI2 IO**

10002550 PD_CFG2 **PD Control** **0000007F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										I2S2_D					SIM2_D	SIM1_D
Type										RW					RW	RW
Reset										1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
6:2		I2S2_D	**Pull-down control of I2S2 IO** [0]: I2S1_LRCK PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: I2S1_BCK [2]: I2S2_DI [3]: I2S1_DO [4]: I2S1_MCK

Bit(s)	Mnemonic	Name	Description
1		SIM2_D	**Pull-down control of SIM2_INT IO** [0]: INT_SIM2 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A
0		SIM1_D	**Pull-down control of SIM1_INT IO** [0]: INT_SIM1 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A

10002554 PD_CFG2_SET **PD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										I2S2_D					SIM2_D	SIM1_D
Type										WO					WO	WO
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6:2		I2S2_D	**Bitwise SET operation for pull-down control of I2S2 IO** 0: Keep 1: SET bits
1		SIM2_D	**Bitwise SET operation for pull-down control of SIM2 IO**
0		SIM1_D	**Bitwise SET operation for pull-down control of SIM1 IO**

10002558 PD_CFG2_CLR **PD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										I2S2_D					SIM2_D	SIM1_D
Type										WO					WO	WO
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
6:2		I2S2_D	**Bitwise CLR operation for pull-down control of I2S2 IO** 0: Keep 1: CLR bits
1		SIM2_D	**Bitwise CLR operation for pull-down control of SIM2 IO**
0		SIM1_D	**Bitwise CLR operation for pull-down control of SIM1 IO**

10002560 PU_CFG0 **PU Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				SPI2_D				SPI1_D				EINT_D				
Type				RW				RW				RW				
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D												SPI0_D			
Type	RW												RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:25		SPI2_D	**Pull-up control of SPI2 IO** [0]: SPI2_CK PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: SPI2_MI [2]: SPI2_MO [3]: SPI2_CS
24:21		SPI1_D	**Pull-up control of SPI1 IO** [0]: SPI1_CK PU/PD: 0/0: N/A 1/0: Pull up 0/1: Pull down 1/1: N/A [1]: SPI1_MI [2]: SPI1_MO [3]: SPI1_CS
20:4		EINT_D	**Pull-up control of EINT IO** [9:0]: Reserved PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [10]: EINT10 [11]: EINT11 [12]: EINT12 [13]: EINT13 [14]: EINT14 [15]: EINT15 [16]: EINT16
3:0		SPI0_D	**Pull-up control of SPI0 IO**

Bit(s)	Mnemonic	Name	Description
			[0]: SPI0_CK PU/PD: 0/0: N/A 1/0: Pull up with 75K 0/1: Pull down 1/1: N/A [1]: SPI0_MI [2]: SPI0_MO [3]: SPI0_CS

10002564 PU_CFG0_SET **PU Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				SPI2_D				SPI1_D				EINT_D				
Type				WO				WO				WO				
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D												SPI0_D			
Type	WO												WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:25		SPI2_D	**Bitwise SET operation for pull-up control of SPI2 IO** 0: Keep 1: SET bits
24:21		SPI1_D	**Bitwise SET operation for pull-up control of SPI1 IO**
20:4		EINT_D	**Bitwise SET operation for pull-up control of EINT IO**
3:0		SPI0_D	**Bitwise SET operation for pull-up control of SPI0 IO**

10002568 PU_CFG0_CLR **PU Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				SPI2_D				SPI1_D				EINT_D				
Type				WO				WO				WO				
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D												SPI0_D			
Type	WO												WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:25		SPI2_D	**Bitwise CLR operation for pull-up control of SPI2 IO** 0: Keep 1: CLR bits
24:21		SPI1_D	**Bitwise CLR operation for pull-up control of**

Bit(s)	Mnemonic	Name	Description
			SPI1 IO
20:4		EINT_D	**Bitwise CLR operation for pull-up control of EINT IO**
3:0		SPI0_D	**Bitwise CLR operation for pull-up control of SPI0 IO**

10002570 PU_CFG1 **PU Control** **001FF000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									MSDC0_D							
Type									RW							
Reset									0	0	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC0_D				AUD_CTL_D				SPI3_D				I2S0_D			
Type	RW				RW				RW				RW			
Reset	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:12		MSDC0_D	**Pull-up control of MSDC0 IO** [11:0]: Reserved
11:9		AUD_CTL_D	**Pull-up control of AUD_CTL IO** [0]: AUD_INTN PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: AUD_PDN [2]: Reserved
8:5		SPI3_D	**Pull-up control of SPI3 IO** [0]: SPI3_MI PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: SPI3_MO [2]: SPI3_CK [3]: SPI3_CS
4:0		I2S0_D	**Pull-up control of I2S0 IO** [0]: I2S0_LRCK PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: I2S0_BCK [2]: I2S0_MCK [3]: I2S0_DI [4]: I2S3_DO

10002574 PU_CFG1_SET **PU Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name									MSDCo_D							
Type									WO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDCo_D				AUD_CTL_D				SPI3_D				I2So_D			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:12		MSDCo_D	**Bitwise SET operation for pull-up control of MSDCo IO** 0: Keep 1: SET bits
11:9		AUD_CTL_D	**Bitwise SET operation for pull-up control of AUD_CTL IO**
8:5		SPI3_D	**Bitwise SET operation for pull-up control of SPI3 IO**
4:0		I2So_D	**Bitwise SET operation for pull-up control of I2So IO**

10002578 PU_CFG1_CLR PU Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									MSDCo_D							
Type									WO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDCo_D				AUD_CTL_D				SPI3_D				I2So_D			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:12		MSDCo_D	**Bitwise CLR operation for pull-up control of MSDCo IO** 0: Keep 1: CLR bits
11:9		AUD_CTL_D	**Bitwise CLR operation for pull-up control of AUD_CTL IO**
8:5		SPI3_D	**Bitwise CLR operation for pull-up control of SPI3 IO**
4:0		I2So_D	**Bitwise CLR operation for pull-up control of I2So IO**

10002580 PU_CFG2 PU Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				I2S2_D					SIM2_D				SIM1_D			

Type				RW					RW				RW			
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:8		I2S2_D	**Pull-up control of I2S2 IO** [0]: I2S1_LRCK PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: I2S1_BCK [2]: I2S2_DI [3]: I2S1_DO [4]: I2S1_MCK
7:4		SIM2_D	**INS/Pull-up control of SIM2 IO** [0]: SIM2_SCLK 0: Normal mode 1: Special mode [1]: SIM2_SRST 0: Normal mode 1: Special mode [2]: SIM2_SIO 0: Normal mode 1: Special mode [3]:INT_SIM2 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A
3:0		SIM1_D	**INS/Pull-up control of SIM1 IO** [0]: SIM1_SCLK 0: Normal mode 1: Special mode [1]: SIM1_SRST 0: Normal mode 1: Special mode [2]: SIM1_SIO 0: Normal mode 1: Special mode [3]: INT_SIM1 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A

10002584 PU_CFG2_SET **PU Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				I2S2_D					SIM2_D				SIM1_D			

Type				WO					WO				WO			
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:8		I2S2_D	**Bitwise SET operation for pull-up control of I2S2 IO** 0: Keep 1: SET bits
7:4		SIM2_D	**Bitwise SET operation for INS/pull-up control of SIM2 IO**
3:0		SIM1_D	**Bitwise SET operation for INS/pull-up control of SIM1 IO**

10002588 PU_CFG2_CLR **PU Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				I2S2_D					SIM2_D				SIM1_D			
Type				WO					WO				WO			
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:8		I2S2_D	**Bitwise CLR operation for pull-up control of I2S2 IO** 0: Keep 1: CLR bits
7:4		SIM2_D	**Bitwise CLR operation for INS/pull-up control of SIM2 IO**
3:0		SIM1_D	**Bitwise CLR operation for INS/pull-up control of SIM1 IO**

10002590 DRV_CFG0 **DRV Control** **15555555**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AUD_CTL_D		SPI3_D		AUD_I2S_D		SPI2_D		I2C5_D		I2C4_D		SPI1_D	
Type			RW		RW		RW		RW		RW		RW		RW	
Reset			0	1	0	1	0	1	0	1	0	1	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D								SPI0_D		KEY_D				I2C0_D	
Type	RW								RW		RW				RW	
Reset	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
29:28		AUD_CTL_D	**Driving control of AUD_CTL IO** [1:0]: AUD_INTN, AUD_PDN 00: 2mA 01: 4mA

Bit(s)	Mnemonic	Name	Description
			10: 6mA 11: 8mA
27:26		SPI3_D	**Driving control of SPI3 IO** [1:0]: SPI3_CK, SPI3_MO, SPI3_MI, SPI3_CS 00: 2mA 01: 4mA 10: 6mA 11: 8mA
25:24		AUD_I2S_D	**Reserved** [1:0]: Reserved
23:22		SPI2_D	**Driving control of SPI2 IO** [1:0]: SPI2_CK, SPI2_MO, SPI2_MI, SPI2_CS 00: 2mA 01: 4mA 10: 6mA 11: 8mA
21:20		I2C5_D	**Driving control of I2C5 IO** [0]: SDA5 0: Weak output low driving strength 1: Strong output low driving strength [1]: SCL5
19:18		I2C4_D	**Driving control of I2C4 IO** [0]: SDA4 0: Weak output low driving strength 1: Strong output low driving strength [1]: SCL4
17:16		SPI1_D	**Driving control of SPI1 IO** [1:0]: SPI1_CK, SPI1_MO, SPI1_MI, SPI1_CS 00: 2mA 01: 4mA 10: 6mA 11: 8mA
15:8		EINT_D	**Driving control of EINT IO** [3:0]: Reserved 00: 2mA 01: 4mA 10: 6mA 11: 8mA [5:4]: EINT10, EINT11 [7:6]: EINT12, EINT13, EINT14, EINT15, EINT16
7:6		SPI0_D	**Driving control of SPI0 IO** [1:0]: SPI0_CK, SPI0_MO, SPI0_MI, SPI0_CS 00: 2mA 01: 4mA 10: 6mA 11: 8mA
5:2		KEY_D	**Driving control of KEY IO** [1:0]: KPROW0, KPROW1, KPROW2 00: 2mA 01: 4mA 10: 6mA 11: 8mA [3:2]: KPCOL0, KPCOL1, KPCOL2
1:0		I2C0_D	**Driving control of I2C0 IO** [0]: SDA0 0: Weak output low driving strength 1: Strong output low driving strength [1]: SCL0

Bit(s)	Mnemonic	Name	Description

10002594 DRV_CFG0_SET DRV Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AUD_CTL_D		SPI3_D		AUD_I2S_D		SPI2_D		I2C5_D		I2C4_D		SPI1_D	
Type			WO		WO		WO		WO		WO		WO		WO	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D								SPI0_D		KEY_D				I2C0_D	
Type	WO								WO		WO				WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:28		AUD_CTL_D	**Bitwise SET operation for driving control of AUD_CTL IO** 0: Keep 1: SET bits
27:26		SPI3_D	**Bitwise SET operation for driving control of SPI3 IO**
25:24		AUD_I2S_D	**Reserved**
23:22		SPI2_D	**Bitwise SET operation for driving control of SPI2 IO**
21:20		I2C5_D	**Bitwise SET operation for driving control of I2C5 IO**
19:18		I2C4_D	**Bitwise SET operation for driving control of I2C4 IO**
17:16		SPI1_D	**Bitwise SET operation for driving control of SPI1 IO**
15:8		EINT_D	**Bitwise SET operation for driving control of EINT IO**
7:6		SPI0_D	**Bitwise SET operation for driving control of SPI0 IO**
5:2		KEY_D	**Bitwise SET operation for driving control of KEY IO**
1:0		I2C0_D	**Bitwise SET operation for driving control of I2C0 IO**

10002598 DRV_CFG0_CLR DRV Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AUD_CTL_D		SPI3_D		AUD_I2S_D		SPI2_D		I2C5_D		I2C4_D		SPI1_D	
Type			WO		WO		WO		WO		WO		WO		WO	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D								SPI0_D		KEY_D				I2C0_D	
Type	WO								WO		WO				WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:28		AUD_CTL_D	**Bitwise CLR operation for driving control of AUD_CTL IO**

Bit(s)	Mnemonic	Name	Description
			0: Keep 1: CLR bits
27:26		SPI3_D	**Bitwise CLR operation for driving control of SPI3 IO**
25:24		AUD_I2S_D	**Reserved**
23:22		SPI2_D	**Bitwise CLR operation for driving control of SPI2 IO**
21:20		I2C5_D	**Bitwise CLR operation for driving control of I2C5 IO**
19:18		I2C4_D	**Bitwise CLR operation for driving control of I2C4 IO**
17:16		SPI1_D	**Bitwise CLR operation for driving control of SPI1 IO**
15:8		EINT_D	**Bitwise CLR operation for driving control of EINT IO**
7:6		SPI0_D	**Bitwise CLR operation for driving control of SPI0 IO**
5:2		KEY_D	**Bitwise CLR operation for driving control of KEY IO**
1:0		I2C0_D	**Bitwise CLR operation for driving control of I2C0 IO**

100025A0 DRV_CFG1 **DRV Control** **140A06DB**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SIM2_D				SIM2B_D					SIM1_D				SIM1B_D
Type			RW				RW					RW				RW
Reset			0	1	0	1	0	0	0	0	0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIM1B_D				MSDC0_D											
Type	RW				RW											
Reset	0	0	0	0	0	1	1	0	1	1	0	1	1	0	1	1

Bit(s)	Mnemonic	Name	Description
29:26		SIM2_D	**Driving control of SIM2 IO** [1:0]: SIM2_SCLK 00: 4mA 01: 8mA 10: 12mA 11: 16mA [3:2]: INT_SIM2, SIM2_SRST, SIM2_SIO
25:21		SIM2B_D	**TUNE control of SIM2B IO** Suggested value: 0x5 [4:0]: BIAS tune of SIM2 IOs
20:17		SIM1_D	**Driving control of SIM1 IO** [1:0]: SIM1_SCLK 00: 4mA 01: 8mA 10: 12mA 11: 16mA [3:2]: INT_SIM1, SIM1_SRST, SIM1_SIO
16:12		SIM1B_D	**TUNE control of SIM1B IO** Suggested value: 0x5 [4:0]: BIAS Tune of SIM1 IOs
11:0		MSDC0_D	**Driving control of MSDC0 IO** [2:0]: MSDC0_DAT0, MSDC0_DAT1, MSDC0_DAT2,

Bit(s)	Mnemonic	Name	Description
			MSDC0_DAT3 000: 2mA 001: 4mA 010: 6mA 011: 8mA 100: 10mA 101: 12mA 110: 14mA 111: 16mA [5:3]: MSDC0_DAT4, MSDC0_DAT5, MSDC0_DAT6, MSDC0_DAT7 [8:6]: MSDC0_CMD, MSDC0_DSL, MSDC0_RSTB [11:9]: MSDC0_CLK

100025A4 DRV_CFG1_SET **DRV Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SIM2_D				SIM2B_D					SIM1_D				SIM1B_D
Type			WO				WO					WO				WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIM1B_D				MSDC0_D											
Type	WO				WO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:26		SIM2_D	**Bitwise SET operation for driving control of SIM2 IO** 0: Keep 1: SET bits
25:21		SIM2B_D	**Bitwise SET operation for driving control of SIM2B IO**
20:17		SIM1_D	**Bitwise SET operation for driving control of SIM1 IO**
16:12		SIM1B_D	**Bitwise SET operation for driving control of SIM1B IO**
11:0		MSDC0_D	**Bitwise SET operation for driving control of MSDC0 IO**

100025A8 DRV_CFG1_CLR **DRV Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SIM2_D				SIM2B_D					SIM1_D				SIM1B_D
Type			WO				WO					WO				WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIM1B_D				MSDC0_D											
Type	WO				WO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:26		SIM2_D	**Bitwise CLR operation for driving control of SIM2 IO** 0: Keep 1: CLR bits
25:21		SIM2B_D	**Bitwise CLR operation for driving control of SIM2B IO**
20:17		SIM1_D	**Bitwise CLR operation for driving control of SIM1 IO**
16:12		SIM1B_D	**Bitwise CLR operation for driving control of SIM1B IO**
11:0		MSDC0_D	**Bitwise CLR operation for driving control of MSDC0 IO**

100025B0 DRV_CFG2 DRV Control 1B605555

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			MSDC1_D									MSDC1B_D				
Type			RW									RW				
Reset			0	1	1	0	1	1	0	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2S2_D								I2S0_D							
Type	RW								RW							
Reset	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
29:21		MSDC1_D	**Driving control of MSDC1 IO** [2:0]: MSDC1_CMD 000: 2mA 001: 4mA 010: 6mA 011: 8mA 100: 10mA 101: 12mA 110: 14mA 111: 16mA [5:3]: MSDC1_DAT0, MSDC1_DAT1, MSDC1_DAT2, MSDC1_DAT3 [8:6]: MSDC1_CLK
20:16		MSDC1B_D	**TUNE control of MSDC1B IO** Suggested value: 0x5 [4:0]: BIAS tune of MSDC1 IOs
15:8		I2S2_D	**Driving control of I2S2 IO** [1:0]: I2S1_LRCK 00: 2mA 01: 4mA 10: 6mA 11: 8mA [3:2]: I2S1_BCK [5:4]: I2S1_MCK [7:6]: I2S2_DI, I2S1_DO
7:0		I2S0_D	**Driving control of I2S0 IO** [1:0]: I2S0_LRCK 00: 2mA 01: 4mA 10: 6mA 11: 8mA

Bit(s)	Mnemonic	Name	Description
			[3:2]: I2So_BCK [5:4]: I2So_MCK [7:6]: I2So_DI, I2S3_DO

100025B4 DRV_CFG2_SET **DRV Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			MSDC1_D									MSDC1B_D				
Type			WO									WO				
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2S2_D								I2So_D							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:21		MSDC1_D	**Bitwise SET operation for driving control of MSDC1 IO** 0: Keep 1: SET bits
20:16		MSDC1B_D	**Bitwise SET operation for driving control of MSDC1B IO**
15:8		I2S2_D	**Bitwise SET operation for driving control of I2S2 IO**
7:0		I2So_D	**Bitwise SET operation for driving control of I2So IO**

100025B8 DRV_CFG2_CLR **DRV Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			MSDC1_D									MSDC1B_D				
Type			WO									WO				
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2S2_D								I2So_D							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:21		MSDC1_D	**Bitwise CLR operation for driving control of MSDC1 IO** 0: Keep 1: CLR bits
20:16		MSDC1B_D	**Bitwise CLR operation for driving control of MSDC1B IO**
15:8		I2S2_D	**Bitwise CLR operation for driving control of I2S2 IO**
7:0		I2So_D	**Bitwise CLR operation for driving control of I2So IO**

Bit(s)	Mnemonic	Name	Description

10002600 DUMMY **DUMMY** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DUMMY							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		DUMMY	**Dummy register** [7:0]: Dummy register

10002604 DUMMY_SET **DUMMY** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DUMMY							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		DUMMY	**Bitwise SET operation for dummy register** 0: Keep 1: SET bits

10002608 DUMMY_CLR **DUMMY** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DUMMY							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		DUMMY	**Bitwise CLR operation for dummy register** 0: Keep

Bit(s)	Mnemonic	Name	Description
			1: CLR bits

Module name: IO_CFG_R Base address: (+10002800h)

Address	Name	Width	Register Function
10002800	IES_CFG0	32	IES Control
10002804	IES_CFG0_SET	32	IES Control
10002808	IES_CFG0_CLR	32	IES Control
10002810	IES_CFG1	32	IES Control
10002814	IES_CFG1_SET	32	IES Control
10002818	IES_CFG1_CLR	32	IES Control
10002820	SR_CFG0	32	SR Control
10002824	SR_CFG0_SET	32	SR Control
10002828	SR_CFG0_CLR	32	SR Control
10002830	SMT_CFG0	32	SMT Control
10002834	SMT_CFG0_SET	32	SMT Control
10002838	SMT_CFG0_CLR	32	SMT Control
10002840	RDSEL_CFG0	32	RDSEL Control
10002844	RDSEL_CFG0_SET	32	RDSEL Control
10002848	RDSEL_CFG0_CLR	32	RDSEL Control
10002850	RDSEL_CFG1	32	RDSEL Control
10002854	RDSEL_CFG1_SET	32	RDSEL Control
10002858	RDSEL_CFG1_CLR	32	RDSEL Control
10002860	TDSEL_CFG0	32	TDSEL Control
10002864	TDSEL_CFG0_SET	32	TDSEL Control
10002868	TDSEL_CFG0_CLR	32	TDSEL Control
10002870	TDSEL_CFG1	32	TDSEL Control
10002874	TDSEL_CFG1_SET	32	TDSEL Control
10002878	TDSEL_CFG1_CLR	32	TDSEL Control
10002880	PUPD_CFG0	32	PUPD Control
10002884	PUPD_CFG0_SET	32	PUPD Control
10002888	PUPD_CFG0_CLR	32	PUPD Control
10002890	R0_CFG0	32	R0 Control
10002894	R0_CFG0_SET	32	R0 Control
10002898	R0_CFG0_CLR	32	R0 Control
100028A0	R1_CFG0	32	R1 Control
100028A4	R1_CFG0_SET	32	R1 Control
100028A8	R1_CFG0_CLR	32	R1 Control
100028B0	PD_CFG0	32	PD Control
100028B4	PD_CFG0_SET	32	PD Control
100028B8	PD_CFG0_CLR	32	PD Control
100028C0	PD_CFG1	32	PD Control

Address	Name	Width	Register Function
100028C4	PD_CFG1_SET	32	PD Control
100028C8	PD_CFG1_CLR	32	PD Control
100028D0	PU_CFG0	32	PU Control
100028D4	PU_CFG0_SET	32	PU Control
100028D8	PU_CFG0_CLR	32	PU Control
100028E0	PU_CFG1	32	PU Control
100028E4	PU_CFG1_SET	32	PU Control
100028E8	PU_CFG1_CLR	32	PU Control
100028F0	DRV_CFG0	32	DRV Control
100028F4	DRV_CFG0_SET	32	DRV Control
100028F8	DRV_CFG0_CLR	32	DRV Control
10002900	DRV_CFG1	32	DRV Control
10002904	DRV_CFG1_SET	32	DRV Control
10002908	DRV_CFG1_CLR	32	DRV Control
10002A00	DUMMY	32	DUMMY
10002A04	DUMMY_SET	32	DUMMY
10002A08	DUMMY_CLR	32	DUMMY

10002800 IES_CFG0 **IES Control** **3FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AUD_CTL_R		SYS_R								PMIC_R			
Type			RW		RW								RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMIC_R					I2So_R					MSDC1_R					
Type	RW					RW					RW					
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
29:28		AUD_CTL_R	**Reserved** [1:0]: Reserved
27:20		SYS_R	**IES control of SYS IO** [0]: RTC32K_CK 0: Disable 1: Enable [1]: SRCLKENAI0 [2]: SRCLKENAI1 [3]: SRCLKENA0 [4]: SRCLKENA1 [5]: Reserved [6]: WATCHDOG [7]: DRVBUS
19:11		PMIC_R	**IES control of PMIC IO** [0]: PWRAP_SPI0_MI 0: Disable 1: Enable [1]: PWRAP_SPI0_MO [2]: PWRAP_SPI0_CK [3]: PWRAP_SPI0_CSN

Bit(s)	Mnemonic	Name	Description
			[4]: AUD_CLK_MOSI [5]: AUD_DAT_MISO [6]: AUD_DAT_MOSI [7]: VOW_CLK_MISO [8]: ANC_DAT_MOSI
10:6		I2S0_R	**Reserved** [4:0]: Reserved
5:0		MSDC1_R	**Reserved** [5:0]: Reserved

10002804 IES_CFG0_SET **IES Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AUD_CTL_R		SYS_R								PMIC_R			
Type			WO		WO								WO			
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMIC_R					I2S0_R					MSDC1_R					
Type	WO					WO					WO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:28		AUD_CTL_R	**Bitwise SET operation for IES control of AUD_CTL IO** 0: Keep 1: SET bits
27:20		SYS_R	**Bitwise SET operation for IES control of SYS IO**
19:11		PMIC_R	**Bitwise SET operation for IES control of PMIC IO**
10:6		I2S0_R	**Reserved**
5:0		MSDC1_R	**Reserved**

10002808 IES_CFG0_CLR **IES Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AUD_CTL_R		SYS_R								PMIC_R			
Type			WO		WO								WO			
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMIC_R					I2S0_R					MSDC1_R					
Type	WO					WO					WO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:28		AUD_CTL_R	**Reserved** 0: Keep 1: CLR bits
27:20		SYS_R	**Bitwise CLR operation for IES control of SYS IO**
19:11		PMIC_R	**Bitwise CLR operation for IES control of PMIC**

Bit(s)	Mnemonic	Name	Description
			IO
10:6		I2S0_R	**Reserved**
5:0		MSDC1_R	**Reserved**

10002810 IES_CFG1 IES Control 0003FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															EINT_R	
Type															RW	
Reset															1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_R								UR1_R		I2C7_R		I2C6_R		I2C1_R	
Type	RW								RW		RW		RW		RW	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
17:8		EINT_R	**IES control of EINT IO** [0]: EINT0 0: Disable 1: Enable [1]: EINT1 [2]: EINT2 [3]: EINT3 [4]: EINT4 [5]: EINT5 [6]: EINT6 [7]: EINT7 [8]: EINT8 [9]: EINT9
7:6		UR1_R	**IES control of UR1 IO** [0]: URXD1 [1]: UTXD1
5:4		I2C7_R	**IES control of I2C7 IO** [0]: SCL7 [1]: SDA7
3:2		I2C6_R	**IES control of I2C6 IO** [0]: SCL6 [1]: SDA6
1:0		I2C1_R	**IES control of I2C1 IO** [0]: SCL1 [1]: SDA1

10002814 IES_CFG1_SET IES Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															EINT_R	
Type															WO	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_R								UR1_R		I2C7_R		I2C6_R		I2C1_R	
Type	WO								WO		WO		WO		WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:8		EINT_R	**Bitwise SET operation for IES control of EINT IO** 0: Keep 1: SET bits
7:6		UR1_R	**Bitwise SET operation for IES control of UR1 IO**
5:4		I2C7_R	**Bitwise SET operation for IES control of I2C7 IO**
3:2		I2C6_R	**Bitwise SET operation for IES control of I2C6 IO**
1:0		I2C1_R	**Bitwise SET operation for IES control of I2C1 IO**

10002818 IES_CFG1_CLR **IES Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															EINT_R	
Type															WO	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_R								UR1_R		I2C7_R		I2C6_R		I2C1_R	
Type	WO								WO		WO		WO		WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:8		EINT_R	**Bitwise CLR operation for IES control of EINT IO** 0: Keep 1: CLR bits
7:6		UR1_R	**Bitwise CLR operation for IES control of UR1 IO**
5:4		I2C7_R	**Bitwise CLR operation for IES control of I2C7 IO**
3:2		I2C6_R	**Bitwise CLR operation for IES control of I2C6 IO**
1:0		I2C1_R	**Bitwise CLR operation for IES control of I2C1 IO**

10002820 SR_CFG0 **SR Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				EINT_R				AUD_CTL_R	UR1_R	SYS_R						
Type				RW				RW	RW	RW						
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYS_R	I2C7_R	I2C6_R	PMIC_R						I2S0_R				MSDC1_R		
Type	RW	RW	RW	RW						RW				RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:25		EINT_R	**SR control of EINT IO** [0]: EINT0, EINT1, EINT2, EINT3 0: Disable 1: Enable [1]: EINT4, EINT5, EINT6, EINT7

Bit(s)	Mnemonic	Name	Description
			[2]: EINT8, EINT9 [3]: Reserved
24		AUD_CTL_R	**SR control of AUD_CTL IO** [0]: Reserved
23		UR1_R	**SR control of UR1 IO** [0]: URXD1, UTXD1
22:15		SYS_R	**SR control of SYS IO** [0]: RTC32K_CK [1]: SRCLKENAI0 [2]: SRCLKENAI1 [3]: SRCLKENA0 [4]: SRCLKENA1 [5]: SYSRSTB [6]: WATCHDOG [7]: DRVBUS
14		I2C7_R	**SR control of I2C7 IO** [0]: SCL7, SDA7
13		I2C6_R	**SR control of I2C6 IO** [0]: SCL6, SDA6
12:7		PMIC_R	**SR control of PMIC IO** [0]: PWRAP_SPI0_MI, PWRAP_SPI0_MO, PWRAP_SPI0_CSN [1]: PWRAP_SPI0_CK [2]: AUD_CLK_MOSI [3]: AUD_DAT_MISO, AUD_DAT_MOSI [4]: VOW_CLK_MISO [5]: ANC_DAT_MOSI
6:3		I2S0_R	**SR control of I2S0 IO** [3:0]: Reserved
2:0		MSDC1_R	**Reserved** [2:0]: Reserved

10002824 SR_CFG0_SET SR Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				EINT_R				AUD_CTL_R	UR1_R	SYS_R						
Type				WO				WO	WO	WO						
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYS_R	I2C7_R	I2C6_R	PMIC_R						I2S0_R				MSDC1_R		
Type	WO	WO	WO	WO						WO				WO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:25		EINT_R	**Bitwise SET operation for SR control of EINT IO** 0: Keep 1: SET bits
24		AUD_CTL_R	**Bitwise SET operation for SR control of AUD_CTL IO**
23		UR1_R	**Bitwise SET operation for SR control of UR1 IO**
22:15		SYS_R	**Bitwise SET operation for SR control of SYS IO**
14		I2C7_R	**Bitwise SET operation for SR control of I2C7 IO**

Bit(s)	Mnemonic	Name	Description
13		I2C6_R	**Bitwise SET operation for SR control of I2C6 IO**
12:7		PMIC_R	**Bitwise SET operation for SR control of PMIC IO**
6:3		I2S0_R	**Bitwise SET operation for SR control of I2S0 IO**
2:0		MSDC1_R	**Reserved**

10002828 SR_CFG0_CLR SR Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				EINT_R				AUD_CTL_R	UR1_R	SYS_R						
Type				WO				WO	WO	WO						
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYS_R	I2C7_R	I2C6_R	PMIC_R						I2S0_R				MSDC1_R		
Type	WO	WO	WO	WO						WO				WO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:25		EINT_R	**Bitwise CLR operation for SR control of EINT IO** 0: Keep 1: CLR bits
24		AUD_CTL_R	**Bitwise CLR operation for SR control of AUD_CTL IO**
23		UR1_R	**Bitwise CLR operation for SR control of UR1 IO**
22:15		SYS_R	**Bitwise CLR operation for SR control of SYS IO**
14		I2C7_R	**Bitwise CLR operation for SR control of I2C7 IO**
13		I2C6_R	**Bitwise CLR operation for SR control of I2C6 IO**
12:7		PMIC_R	**Bitwise CLR operation for SR control of PMIC IO**
6:3		I2S0_R	**Bitwise CLR operation for SR control of I2S0 IO**
2:0		MSDC1_R	**Reserved**

10002830 SMT_CFG0 SMT Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			EINT_R				AUD_CTL_R	UR1_R	SYS_R							
Type			RW				RW	RW	RW							
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2C7_R	I2C6_R	I2C1_R	PMIC_R						I2S0_R				MSDC1_R		
Type	RW	RW	RW	RW						RW				RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:26		EINT_R	**SMT control of EINT IO** [0]: EINT0, EINT1, EINT2, EINT3 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable [1]: EINT4, EINT5, EINT6, EINT7 [2]: EINT8, EINT9 [3]: Reserved
25		AUD_CTL_R	**Reserved** [0]: Reserved
24		UR1_R	**SMT control of UR1 IO** [0]: URXD1, UTXD1
23:16		SYS_R	**SMT control of SYS IO** [0]: RTC32K_CK [1]: SRCLKENAI0 [2]: SRCLKENAI1 [3]: SRCLKENA0 [4]: SRCLKENA1 [5]: Reserved [6]: WATCHDOG [7]: DRVBUS
15		I2C7_R	**SMT control of I2C7 IO** [0]: SCL7, SDA7
14		I2C6_R	**SMT control of I2C6 IO** [0]: SCL6, SDA6
13		I2C1_R	**SMT control of I2C1 IO** [0]: SCL1, SDA1
12:7		PMIC_R	**SMT control of PMIC IO** [0]: PWRAP_SPI0_MI, PWRAP_SPI0_MO, PWRAP_SPI0_CSN [1]: PWRAP_SPI0_CK [2]: AUD_CLK_MOSI [3]: AUD_DAT_MISO, AUD_DAT_MOSI [4]: VOW_CLK_MISO [5]: ANC_DAT_MOSI
6:3		I2S0_R	**Reserved** [3:0]: Reserved
2:0		MSDC1_R	**SMT control of MSDC1 IO** [0]: MSDC1_CMD [1]: MSDC1_DAT0, MSDC1_DAT1, MSDC1_DAT2, MSDC1_DAT3 [2]: MSDC1_CLK

10002834 SMT_CFG0_SET **SMT Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			EINT_R				AUD_CTL_R	UR1_R	SYS_R							
Type			WO				WO	WO	WO							
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2C7_R	I2C6_R	I2C1_R	PMIC_R						I2S0_R				MSDC1_R		
Type	WO	WO	WO	WO						WO				WO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:26		EINT_R	**Bitwise SET operation for SMT control of EINT IO**

Bit(s)	Mnemonic	Name	Description
			0: Keep 1: SET bits
25		AUD_CTL_R	**Reserved**
24		UR1_R	**Bitwise SET operation for SMT control of UR1 IO**
23:16		SYS_R	**Bitwise SET operation for SMT control of SYS IO**
15		I2C7_R	**Bitwise SET operation for SMT control of I2C7 IO**
14		I2C6_R	**Bitwise SET operation for SMT control of I2C6 IO**
13		I2C1_R	**Bitwise SET operation for SMT control of I2C1 IO**
12:7		PMIC_R	**Bitwise SET operation for SMT control of PMIC IO**
6:3		I2S0_R	**Reserved**
2:0		MSDC1_R	**Bitwise SET operation for SMT control of MSDC1 IO**

10002838 SMT_CFG0_CLR SMT Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			EINT_R				AUD_CTL_R	UR1_R	SYS_R							
Type			WO				WO	WO	WO							
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I2C7_R	I2C6_R	I2C1_R	PMIC_R						I2S0_R				MSDC1_R		
Type	WO	WO	WO	WO						WO				WO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:26		EINT_R	**Bitwise CLR operation for SMT control of EINT IO** 0: Keep 1: CLR bits
25		AUD_CTL_R	**Reserved**
24		UR1_R	**Bitwise CLR operation for SMT control of UR1 IO**
23:16		SYS_R	**Bitwise CLR operation for SMT control of SYS IO**
15		I2C7_R	**Bitwise CLR operation for SMT control of I2C7 IO**
14		I2C6_R	**Bitwise CLR operation for SMT control of I2C6 IO**
13		I2C1_R	**Bitwise CLR operation for SMT control of I2C1 IO**
12:7		PMIC_R	**Bitwise CLR operation for SMT control of PMIC IO**
6:3		I2S0_R	**Reserved**
2:0		MSDC1_R	**Bitwise CLR operation for SMT control of MSDC1 IO**

10002840 RDSEL_CFG0 RDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									SYS_R		EINT_R					
Type									RW		RW					
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_R												AUD_CTL_R		I2S2_R	
Type	RW												RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:22		SYS_R	**RDSEL control of SYS IO** [1:0]: RTC32K_CK, SRCLKENAI0, SRCLKENAI1, SRCLKENA0, SRCLKENA1, SYSRSTB, WATCHDOG, DRVBUS
21:4		EINT_R	**RDSEL control of EINT IO** [1:0]: EINT0, EINT1, EINT2, EINT3 [3:2]: EINT4, EINT5, EINT6, EINT7 [5:4]: EINT8, EINT9 [17:6]: Reserved
3:2		AUD_CTL_R	**Reserved** [1:0]: Reserved
1:0		I2S2_R	**Reserved** [1:0]: Reserved

10002844 RDSEL_CFG0_SET RDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									SYS_R		EINT_R					
Type									WO		WO					
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_R												AUD_CTL_R		I2S2_R	
Type	WO												WO		WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:22		SYS_R	**Bitwise SET operation for RDSEL control of SYS IO** 0: Keep 1: SET bits
21:4		EINT_R	**Bitwise SET operation for RDSEL control of EINT IO**
3:2		AUD_CTL_R	**Reserved**
1:0		I2S2_R	**Reserved**

10002848 RDSEL_CFG0_CLR RDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									SYS_R		EINT_R					

Type									WO		WO					
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_R												AUD_CTL_R		I2S2_R	
Type	WO												WO		WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:22		SYS_R	**Bitwise CLR operation for RDSEL control of SYS IO** 0: Keep 1: CLR bits
21:4		EINT_R	**Bitwise CLR operation for RDSEL control of EINT IO**
3:2		AUD_CTL_R	**Reserved**
1:0		I2S2_R	**Reserved**

10002850 RDSEL_CFG1 RDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UR1_R		I2C7_R		I2C6_R		I2C1_R		PMIC_R							
Type	RW		RW		RW		RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:14		UR1_R	**RDSEL control of UR1 IO** [1:0]: URXD1, UTXD1
13:12		I2C7_R	**RDSEL control of I2C7 IO** [1:0]: SCL7, SDA7
11:10		I2C6_R	**RDSEL control of I2C6 IO** [1:0]: SCL6, SDA6
9:8		I2C1_R	**RDSEL control of I2C1 IO** [1:0]: SCL1, SDA1
7:0		PMIC_R	**RDSEL control of PMIC IO** [1:0]: PWRAP_SPI0_MI, PWRAP_SPI0_MO, PWRAP_SPI0_CSN [3:2]: PWRAP_SPI0_CK [5:4]: AUD_CLK_MOSI [7:6]: AUD_DAT_MISO, AUD_DAT_MOSI, VOW_CLK_MISO, ANC_DAT_MOSI

10002854 RDSEL_CFG1_SET RDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	UR1_R		I2C7_R		I2C6_R		I2C1_R		PMIC_R							
Type	WO		WO		WO		WO		WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:14		UR1_R	**Bitwise SET operation for RDSEL control of UR1 IO** 0: Keep 1: SET bits
13:12		I2C7_R	**Bitwise SET operation for RDSEL control of I2C7 IO**
11:10		I2C6_R	**Bitwise SET operation for RDSEL control of I2C6 IO**
9:8		I2C1_R	**Bitwise SET operation for RDSEL control of I2C1 IO**
7:0		PMIC_R	**Bitwise SET operation for RDSEL control of PMIC IO**

10002858 RDSEL_CFG1_CLR **RDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UR1_R		I2C7_R		I2C6_R		I2C1_R		PMIC_R							
Type	WO		WO		WO		WO		WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:14		UR1_R	**Bitwise CLR operation for RDSEL control of UR1 IO** 0: Keep 1: CLR bits
13:12		I2C7_R	**Bitwise CLR operation for RDSEL control of I2C7 IO**
11:10		I2C6_R	**Bitwise CLR operation for RDSEL control of I2C6 IO**
9:8		I2C1_R	**Bitwise CLR operation for RDSEL control of I2C1 IO**
7:0		PMIC_R	**Bitwise CLR operation for RDSEL control of PMIC IO**

10002860 TDSEL_CFG0 **TDSEL Control** **F0000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SLP				SYS_R				EINT_R							
Type	RW				RW				RW							
Reset	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_R								AUD_CTL_R				I2S2_R			
Type	RW								RW				RW			

Reset	0	0	0	0					0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		SLP	**TDSEL value for sleep mode** [3:0]: TDSEL value of IOs in right side in sleep mode Suggested value: 0xF
27:24		SYS_R	**TDSEL control of SYS IO** [3:0]: RTC32K_CK, SRCLKENAI0, SRCLKENAI1, SRCLKENA0, SRCLKENA1, SYSRSTB, WATCHDOG, DRVBUS
23:12		EINT_R	**TDSEL control of EINT IO** [3:0]: EINT0, EINT1, EINT2, EINT3 [7:4]: EINT4, EINT5, EINT6, EINT7 [11:8]: EINT8, EINT9
7:4		AUD_CTL_R	**Reserved** [3:0]: Reserved
3:0		I2S2_R	**Reserved** [3:0]: Reserved

10002864 TDSEL_CFG0_SET **TDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SLP				SYS_R				EINT_R							
Type	WO				WO				WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_R								AUD_CTL_R				I2S2_R			
Type	WO								WO				WO			
Reset	0	0	0	0					0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		SLP	**Bitwise SET operation for TDSEL value fpr Sleep mode** 0: Keep 1: SET bits
27:24		SYS_R	**Bitwise SET operation for TDSEL control of SYS IO**
23:12		EINT_R	**Bitwise SET operation for TDSEL control of EINT IO**
7:4		AUD_CTL_R	**Reserved**
3:0		I2S2_R	**Reserved**

10002868 TDSEL_CFG0_CLR **TDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SLP				SYS_R				EINT_R							
Type	WO				WO				WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_R								AUD_CTL_R				I2S2_R			
Type	WO								WO				WO			

Reset	0	0	0	0					0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		SLP	**Bitwise CLR operation for TDSEL value for sleep mode** 0: Keep 1: CLR bits
27:24		SYS_R	**Bitwise CLR operation for TDSEL control of SYS IO**
23:12		EINT_R	**Bitwise CLR operation for TDSEL control of EINT IO**
7:4		AUD_CTL_R	**Reserved**
3:0		I2S2_R	**Reserved**

10002870 TDSEL_CFG1 TDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UR1_R				I2C7_R				I2C6_R				I2C1_R			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMIC_R															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		UR1_R	**TDSEL control of UR1 IO** [3:0]: URXD1, UTXD1
27:24		I2C7_R	**TDSEL control of I2C7 IO** [3:0]: SCL7, SDA7
23:20		I2C6_R	**TDSEL control of I2C6 IO** [3:0]: SCL6, SDA6
19:16		I2C1_R	**TDSEL control of I2C1 IO** [3:0]: SCL1, SDA1
15:0		PMIC_R	**TDSEL control of PMIC IO** [3:0]: PWRAP_SPI0_MI, PWRAP_SPI0_MO, PWRAP_SPI0_CSN [7:4]: PWRAP_SPI0_CK [11:8]: AUD_CLK_MOSI [15:12]: AUD_DAT_MISO, AUD_DAT_MOSI, VOW_CLK_MISO, ANC_DAT_MOSI

10002874 TDSEL_CFG1_SET TDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UR1_R				I2C7_R				I2C6_R				I2C1_R			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMIC_R															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		UR1_R	**Bitwise SET operation for TDSEL control of UR1 IO** 0: Keep 1: SET bits
27:24		I2C7_R	**Bitwise SET operation for TDSEL control of I2C7 IO**
23:20		I2C6_R	**Bitwise SET operation for TDSEL control of I2C6 IO**
19:16		I2C1_R	**Bitwise SET operation for TDSEL control of I2C1 IO**
15:0		PMIC_R	**Bitwise SET operation for TDSEL control of PMIC IO**

10002878 TDSEL_CFG1_CLR **TDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UR1_R				I2C7_R				I2C6_R				I2C1_R			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMIC_R															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		UR1_R	**Bitwise CLR operation for TDSEL control of UR1 IO** 0: Keep 1: CLR bits
27:24		I2C7_R	**Bitwise CLR operation for TDSEL control of I2C7 IO**
23:20		I2C6_R	**Bitwise CLR operation for TDSEL control of I2C6 IO**
19:16		I2C1_R	**Bitwise CLR operation for TDSEL control of I2C1 IO**
15:0		PMIC_R	**Bitwise CLR operation for TDSEL control of PMIC IO**

10002880 PUPD_CFG0 **PUPD Control** **00000020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MSDC1_R					
Type											RW					
Reset											1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		MSDC1_R	**Reserved** [5:0] Reserved

Bit(s)	Mnemonic	Name	Description

10002884 PUPD_CFG0_SET **PUPD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MSDC1_R					
Type											WO					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		MSDC1_R	**Bitwise SET operation for PUPD control of MSDC1 IO** 0: Keep 1: SET bits

10002888 PUPD_CFG0_CLR **PUPD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MSDC1_R					
Type											WO					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		MSDC1_R	**Bitwise CLR operation for PUPD control of MSDC1 IO** 0: Keep 1: CLR bits

10002890 R0_CFG0 **R0 Control** **00000040**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										PMIC_R	MSDC1_R					
Type										RW	RW					

Reset										1	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6		PMIC_R	**A control of PMIC IO** [0]: VOW_CLK_MISO 0: Digital GPIO mode 1: Analog GPIO mode
5:0		MSDC1_R	**Reserved** [5:0] Reserved

10002894 R0_CFG0_SET **R0 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										PMIC_R	MSDC1_R					
Type										WO	WO					
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6		PMIC_R	**Bitwise SET operation for A control of PMIC IO** 0: Keep 1: SET bits
5:0		MSDC1_R	**Reserved**

10002898 R0_CFG0_CLR **R0 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										PMIC_R	MSDC1_R					
Type										WO	WO					
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6		PMIC_R	**Bitwise CLR operation for A control of PMIC IO** 0: Keep 1: CLR bits
5:0		MSDC1_R	**Reserved**

100028A0 R1_CFG0 **R1 Control** **0000003F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MSDC1_R					
Type											RW					
Reset											1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
5:0		MSDC1_R	**Reserved** [5:0] Reserved

100028A4 R1_CFG0_SET **R1 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MSDC1_R					
Type											WO					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		MSDC1_R	**Reserved** 0: Keep 1: SET bits

100028A8 R1_CFG0_CLR **R1 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MSDC1_R					
Type											WO					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		MSDC1_R	**Reserved** 0: Keep 1: CLR bits

100028B0 PD_CFG0 **PD Control** **1C301FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AUD_CTL_R		SYS_R								PMIC_R		
Type				RW		RW								RW		
Reset				1	1	1	0	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMIC_R						I2S0_R					I2S2_R				
Type	RW						RW					RW				
Reset	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
28:27		AUD_CTL_R	**Reserved** [1:0]: Reserved
26:19		SYS_R	**Pull-down Control of SYS IO** [0]: RTC32K_CK PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: SRCLKENAI0 [2]: SRCLKENAI1 [3]: SRCLKENA0 [4]: SRCLKENA1 [5]: SYSRSTB [6]: WATCHDOG [7]: DRVBUS
18:10		PMIC_R	**Pull-down control of PMIC IO** Note: PU/PD control of PWRAP_SPI0_MO is different from others. [0]: PWRAP_SPI0_MI PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: PWRAP_SPI0_MO PU/PD: 0/0: N/A 1/0: Pull down with 75Kohm 0/1: Pull up with 75Kohm 1/1: N/A [2]: PWRAP_SPI0_CK PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [3]: PWRAP_SPI0_CSN [4]: AUD_CLK_MOSI [5]: AUD_DAT_MISO [6]: AUD_DAT_MOSI [7]: VOW_CLK_MISO [8]: ANC_DAT_MOSI
9:5		I2S0_R	**Reserved** [4:0]: Reserved
4:0		I2S2_R	**Reserved** [4:0]: Reserved

100028B4 PD_CFG0_SET **PD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AUD_CTL_R		SYS_R								PMIC_R		
Type				WO		WO								WO		
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMIC_R						I2S0_R					I2S2_R				
Type	WO						WO					WO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:27		AUD_CTL_R	**Reserved** 0: Keep 1: SET bits
26:19		SYS_R	**Bitwise SET operation for pull-down control of SYS IO**
18:10		PMIC_R	**Bitwise SET operation for pull-down control of PMIC IO**
9:5		I2S0_R	**Reserved**
4:0		I2S2_R	**Reserved**

100028B8 PD_CFG0_CLR **PD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AUD_CTL_R		SYS_R								PMIC_R		
Type				WO		WO								WO		
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMIC_R						I2S0_R					I2S2_R				
Type	WO						WO					WO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:27		AUD_CTL_R	**Reserved** 0: Keep 1: CLR bits
26:19		SYS_R	**Bitwise CLR operation for pull-down control of SYS IO**
18:10		PMIC_R	**Bitwise CLR operation for pull-down control of PMIC IO**
9:5		I2S0_R	**Reserved**
4:0		I2S2_R	**Reserved**

100028C0 PD_CFG1 **PD Control** **0003FF00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															EINT_R	
Type															RW	

Reset															1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_R								UR1_R		I2C7_R		I2C6_R		I2C1_R	
Type	RW								RW		RW		RW		RW	
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:8		EINT_R	**Pull-down control of EINT IO** [0]: EINT0 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: EINT1 [2]: EINT2 [3]: EINT3 [4]: EINT4 [5]: EINT5 [6]: EINT6 [7]: EINT7 [8]: EINT8 [9]: EINT9
7:6		UR1_R	**Pull-down control of UR1 IO** [0]: URXD1 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: UTXD1
5:4		I2C7_R	**Pull-down control of I2C7 IO** [0]: SCL7 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: SDA7
3:2		I2C6_R	**Pull-down control of I2C6 IO** [0]: SCL6 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: SDA6
1:0		I2C1_R	**Pull-down control of I2C1 IO** [0]: SCL1 0: N/A 1: Pull down with 75Kohm [1]: SDA1

100028C4 PD_CFG1_SET **PD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															EINT_R	

Type															WO	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_R								UR1_R		I2C7_R		I2C6_R		I2C1_R	
Type	WO								WO		WO		WO		WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:8		EINT_R	**Bitwise SET operation for pull-down control of MSDC1 IO** 0: Keep 1: SET bits
7:6		UR1_R	**Bitwise SET operation for pull-down control of UR1 IO**
5:4		I2C7_R	**Bitwise SET operation for pull-down control of I2C7 IO**
3:2		I2C6_R	**Bitwise SET operation for pull-down control of I2C6 IO**
1:0		I2C1_R	**Bitwise SET operation for pull-down control of I2C1 IO**

100028C8 PD_CFG1_CLR **PD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															EINT_R	
Type															WO	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_R								UR1_R		I2C7_R		I2C6_R		I2C1_R	
Type	WO								WO		WO		WO		WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:8		EINT_R	Bitwise CLR operation for pull-down control of MSDC1 IO
7:6		UR1_R	Bitwise CLR operation for pull-down control of UR1 IO
5:4		I2C7_R	Bitwise CLR operation for pull-down control of I2C7 IO
3:2		I2C6_R	Bitwise CLR operation for pull-down control of I2C6 IO
1:0		I2C1_R	Bitwise CLR operation for pull-down control of I2C1 IO

100028D0 PU_CFG0 **PU Control** **61000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		I2C7_R		AUD_CTL_R		SYS_R								PMIC_R		
Type		RW		RW		RW								RW		
Reset		1	1	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMIC_R						I2S0_R					I2S2_R				
Type	RW						RW					RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:29		I2C7_R	**Pull-up control of I2C7 IO** [0]: SCL7 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: SDA7
28:27		AUD_CTL_R	**Reserved** [1:0]: Reserved
26:19		SYS_R	**Pull-up control of SYS IO** [0]: RTC32K_CK PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: SRCLKENAI0 [2]: SRCLKENAI1 [3]: SRCLKENA0 [4]: SRCLKENA1 [5]: SYSRSTB [6]: WATCHDOG [7]: DRVBUS
18:10		PMIC_R	**Pull-up control of PMIC IO** Note: PU/PD control of PWRAP_SPI0_MO is different from others. [0]: PWRAP_SPI0_MI PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: PWRAP_SPI0_MO PU/PD: 0/0: N/A 1/0: Pull down with 75Kohm 0/1: Pull up with 75Kohm 1/1: N/A [2]: PWRAP_SPI0_CK PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [3]: PWRAP_SPI0_CSN [4]: AUD_CLK_MOSI [5]: AUD_DAT_MISO [6]: AUD_DAT_MOSI [7]: VOW_CLK_MISO [8]: ANC_DAT_MOSI
9:5		I2S0_R	**Reserved** [4:0]: Reserved
4:0		I2S2_R	**Reserved** [4:0]: Reserved

100028D4 PU_CFG0_SET **PU Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		I2C7_R		AUD_CTL_R		SYS_R								PMIC_R		
Type		WO		WO		WO								WO		
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMIC_R						I2So_R					I2S2_R				
Type	WO						WO					WO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:29		I2C7_R	**Bitwise SET operation for pull-up control of I2C7 IO** 0: Keep 1: SET bits
28:27		AUD_CTL_R	**Reserved**
26:19		SYS_R	**Bitwise SET operation for pull-up control of SYS IO**
18:10		PMIC_R	**Bitwise SET operation for pull-up control of PMIC IO**
9:5		I2So_R	**Reserved**
4:0		I2S2_R	**Reserved**

100028D8 PU_CFG0_CLR **PU Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		I2C7_R		AUD_CTL_R		SYS_R								PMIC_R		
Type		WO		WO		WO								WO		
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMIC_R						I2So_R					I2S2_R				
Type	WO						WO					WO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:29		I2C7_R	**Bitwise CLR operation for pull-up control of I2C7 IO** 0: Keep 1: CLR bits
28:27		AUD_CTL_R	**Reserved**
26:19		SYS_R	**Bitwise CLR operation for pull-up control of SYS IO**
18:10		PMIC_R	**Bitwise CLR operation for pull-up control of PMIC IO**
9:5		I2So_R	**Reserved**
4:0		I2S2_R	**Reserved**

100028E0 PU_CFG1 **PU Control** **0000004C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															EINT_R	
Type															RW	

Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_R								UR1_R		UR7_R		I2C6_R		I2C1_R	
Type	RW								RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0

Bit(s)	Mnemonic	Name	Description
17:8		EINT_R	**Pull-up control of EINT IO** [0]: EINT0 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: EINT1 [2]: EINT2 [3]: EINT3 [4]: EINT4 [5]: EINT5 [6]: EINT6 [7]: EINT7 [8]: EINT8 [9]: EINT9
7:6		UR1_R	**Pull-up control of UR1 IO** [0]: URXD1 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: UTXD1
5:4		UR7_R	**Reserved** [1:0]: Reserved
3:2		I2C6_R	**Pull-up control of I2C6 IO** [0]: SCL6 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: SDA6
1:0		I2C1_R	**Reserved** [1:0]: Reserved

100028E4 PU_CFG1_SET **PU Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															EINT_R	
Type															WO	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_R								UR1_R		UR7_R		I2C6_R		I2C1_R	
Type	WO								WO		WO		WO		WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:8		EINT_R	**Bitwise SET operation for pull-up control of EINT IO** 0: Keep 1: SET bits
7:6		UR1_R	**Bitwise SET operation for pull-up control of UR1 IO**
5:4		UR7_R	**Reserved**
3:2		I2C6_R	**Bitwise SET operation for pull-up control of I2C6 IO**
1:0		I2C1_R	**Reserved**

100028E8 PU_CFG1_CLR **PU Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															EINT_R	
Type															WO	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_R								UR1_R		UR7_R		I2C6_R		I2C1_R	
Type	WO								WO		WO		WO		WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:8		EINT_R	**Bitwise CLR operation for pull-up control of EINT IO** 0: Keep 1: CLR bits
7:6		UR1_R	**Bitwise CLR operation for pull-up control of UR1 IO**
5:4		UR7_R	**Reserved**
3:2		I2C6_R	**Bitwise CLR operation for pull-up control of I2C6 IO**
1:0		I2C1_R	**Reserved**

100028F0 DRV_CFG0 **DRV Control** **05555555**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					SYS_R		PMIC_R									
Type					RW		RW									
Reset					0	1	0	1	0	1	0	1	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMIC_R		EINT_R										AUD_CTL_R		I2S2_R	
Type	RW		RW										RW		RW	
Reset	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
27:26		SYS_R	**Driving control of SYS IO** [1:0]: RTC32K_CK, SRCLKENAI0, SRCLKENAI1, SRCLKENA0, SRCLKENA1, SYSRSTB, WATCHDOG, DRVBUS 00: 2mA

Bit(s)	Mnemonic	Name	Description
			01: 4mA 10: 6mA 11: 8mA
25:14		PMIC_R	**Driving control of PMIC IO** [1:0]: PWRAP_SPI0_MI, PWRAP_SPI0_MO, PWRAP_SPI0_CSN 00: 2mA 01: 4mA 10: 6mA 11: 8mA [3:2]: PWRAP_SPI0_CK [5:4]: AUD_CLK_MOSI [7:6]: AUD_DAT_MISO, AUD_DAT_MOSI [9:8]: VOW_CLK_MISO, ANC_DAT_MOSI [11:10]: Reserved
13:4		EINT_R	**Driving control of EINT IO** [1:0]: EINT0, EINT1, EINT2, EINT3 00: 2mA 01: 4mA 10: 6mA 11: 8mA [3:2]: EINT4, EINT5, EINT6, EINT7 [5:4]: EINT8, EINT9 [9:6]: Reserved
3:2		AUD_CTL_R	**Reserved** [1:0]: Reserved
1:0		I2S2_R	**Reserved** [1:0]: Reserved

100028F4 DRV_CFG0_SET **DRV Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					SYS_R		PMIC_R									
Type					WO		WO									
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMIC_R		EINT_R										AUD_CTL_R		I2S2_R	
Type	WO		WO										WO		WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:26		SYS_R	**Bitwise SET operation for driving control of SYS IO** 0: Keep 1: SET bits
25:14		PMIC_R	**Bitwise SET operation for driving control of PMIC IO**
13:4		EINT_R	**Bitwise SET operation for driving control of EINT IO**
3:2		AUD_CTL_R	**Reserved**
1:0		I2S2_R	**Reserved**

100028F8 DRV_CFG0_CLR **DRV Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					SYS_R		PMIC_R									
Type					WO		WO									
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMIC_R		EINT_R										AUD_CTL_R		I2S2_R	
Type	WO		WO										WO		WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:26		SYS_R	**Bitwise CLR operation for driving control of SYS IO** 0: Keep 1: CLR bits
25:14		PMIC_R	**Bitwise CLR operation for driving control of PMIC IO**
13:4		EINT_R	**Bitwise CLR operation for driving control of EINT IO**
3:2		AUD_CTL_R	**Reserved**
1:0		I2S2_R	**Reserved**

10002900 DRV_CFG1 **DRV Control** **0000002A**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										UR1_R		I2C7_R		I2C6_R		I2C1_R
Type										RW		RW		RW		RW
Reset										0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
6:5		UR1_R	**Driving control of UR1 IO** [1:0]: UTXD1, URXD1 00: 4mA 01: 8mA 10: 12mA 11: 16mA
4:3		I2C7_R	**Driving control of I2C7 IO** [1:0]: SCL7, SDA7 00: 2mA 01: 4mA 10: 6mA 11: 8mA
2:1		I2C6_R	**Driving control of I2C6 IO** [1:0]: SCL6, SDA6 00: 2mA 01: 4mA 10: 6mA

Bit(s)	Mnemonic	Name	Description
			11: 8mA
0		I2C1_R	**Driving control of I2C1 IO** [0]: SCL1 0: Weak output low driving strength 1: Strong output low driving strength [1]: SDA1

10002904 DRV_CFG1_SET **DRV Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										UR1_R		I2C7_R		I2C6_R		I2C1_R
Type										WO		WO		WO		WO
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6:5		UR1_R	**Bitwise SET operation for driving control of UR1 IO** 0: Keep 1: SET bits
4:3		I2C7_R	**Bitwise SET operation for driving control of I2C7 IO**
2:1		I2C6_R	**Bitwise SET operation for driving control of I2C6 IO**
0		I2C1_R	**Bitwise SET operation for driving control of I2C1 IO**

10002908 DRV_CFG1_CLR **DRV Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										UR1_R		I2C7_R		I2C6_R		I2C1_R
Type										WO		WO		WO		WO
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6:5		UR1_R	**Bitwise CLR operation for driving control of UR1 IO** 0: Keep 1: CLR bits
4:3		I2C7_R	**Bitwise CLR operation for driving control of I2C7 IO**

Bit(s)	Mnemonic	Name	Description
2:1		I2C6_R	**Bitwise CLR operation for driving control of I2C6 IO**
0		I2C1_R	**Bitwise CLR operation for driving control of I2C1 IO**

10002A00 DUMMY **DUMMY** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DUMMY							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		DUMMY	**Dummy register** [7:0]: Dummy register

10002A04 DUMMY_SET **DUMMY** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DUMMY							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		DUMMY	**Bitwise SET operation for dummy register** 0: Keep 1: SET bits

10002A08 DUMMY_CLR **DUMMY** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DUMMY							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		DUMMY	**Bitwise CLR operation for dummy register** 0: Keep 1: CLR bits

Module name: IO_CFG_T Base address: (+10002c00h)

Address	Name	Width	Register Function
10002C00	**IES_CFG0**	32	IES Control
10002C04	**IES_CFG0_SET**	32	IES Control
10002C08	**IES_CFG0_CLR**	32	IES Control
10002C10	**IES_CFG1**	32	IES Control
10002C14	**IES_CFG1_SET**	32	IES Control
10002C18	**IES_CFG1_CLR**	32	IES Control
10002C20	**SR_CFG0**	32	SMT Control
10002C24	**SR_CFG0_SET**	32	SMT Control
10002C28	**SR_CFG0_CLR**	32	SMT Control
10002C30	**SMT_CFG0**	32	SMT Control
10002C34	**SMT_CFG0_SET**	32	SMT Control
10002C38	**SMT_CFG0_CLR**	32	SMT Control
10002C40	**RDSEL_CFG0**	32	RDSEL Control
10002C44	**RDSEL_CFG0_SET**	32	RDSEL Control
10002C48	**RDSEL_CFG0_CLR**	32	RDSEL Control
10002C50	**TDSEL_CFG0**	32	TDSEL Control
10002C54	**TDSEL_CFG0_SET**	32	TDSEL Control
10002C58	**TDSEL_CFG0_CLR**	32	TDSEL Control
10002C60	**TDSEL_CFG1**	32	TDSEL Control
10002C64	**TDSEL_CFG1_SET**	32	TDSEL Control
10002C68	**TDSEL_CFG1_CLR**	32	TDSEL Control
10002C70	**PD_CFG0**	32	PD Control
10002C74	**PD_CFG0_SET**	32	PD Control
10002C78	**PD_CFG0_CLR**	32	PD Control
10002C80	**PD_CFG1**	32	PD Control
10002C84	**PD_CFG1_SET**	32	PD Control
10002C88	**PD_CFG1_CLR**	32	PD Control
10002C90	**PU_CFG0**	32	PU Control
10002C94	**PU_CFG0_SET**	32	PU Control
10002C98	**PU_CFG0_CLR**	32	PU Control
10002CA0	**PU_CFG1**	32	PU Control
10002CA4	**PU_CFG1_SET**	32	PU Control
10002CA8	**PU_CFG1_CLR**	32	PU Control
10002CB0	**DRV_CFG0**	32	DRV Control
10002CB4	**DRV_CFG0_SET**	32	DRV Control
10002CB8	**DRV_CFG0_CLR**	32	DRV Control
10002D00	**DUMMY**	32	DUMMY

Address	Name	Width	Register Function
10002D04	DUMMY_SET	32	DUMMY
10002D08	DUMMY_CLR	32	DUMMY

10002C00 IES_CFG0 IES Control 007FFFC0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										BSI_U						
Type										RW						
Reset										1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI_U						SYS_U									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1						

Bit(s)	Mnemonic	Name	Description
22:10		BSI_U	**IES control of BSI IO** [0]: MISC_MIPI_CK_2 0: Disable 1: Enable [1]: MISC_MIPI_DO_2 [2]: MISC_MIPI_CK_3 [3]: MISC_MIPI_DO_3 [4]: MISC_MIPI_CK_0 [5]: MISC_MIPI_DO_0 [6]: MISC_MIPI_CK_1 [7]: MISC_MIPI_DO_1 [8]: RFIC0_BSI_CK [9]: RFIC0_BSI_EN [10]: RFIC0_BSI_D0 [11]: RFIC0_BSI_D1 [12]: RFIC0_BSI_D2
9:6		SYS_U	**IES control of SYS IO** [0]: DISP_PWM [1]: DSI_TE [2]: LCM_RST [3]: IDDIG

10002C04 IES_CFG0_SET IES Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										BSI_U						
Type										WO						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI_U						SYS_U									
Type	WO						WO									
Reset	0	0	0	0	0	0	0	0	0	0						

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
22:10		BSI_U	**Bitwiese SET operation for IES control of BSI IO** 0: Keep 1: SET bits
9:6		SYS_U	**Bitwiese SET operation for IES control of SYS IO**

10002C08 IES_CFG0_CLR **IES Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										BSI_U						
Type										WO						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI_U						SYS_U									
Type	WO						WO									
Reset	0	0	0	0	0	0	0	0	0	0						

Bit(s)	Mnemonic	Name	Description
22:10		BSI_U	**Bitwiese CLR operation for IES control of BSI IO** 0: Keep 1: CLR bits
9:6		SYS_U	**Bitwiese CLR operation for IES control of SYS IO**

10002C10 IES_CFG1 **IES Control** **00FFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BPI_U							
Type									RW							
Reset									1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPI_U															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
23:0		BPI_U	**IES control of BPI IO** [0]: BPI_BUS23_DET1 0:Disable 1:Enable [1]: BPI_BUS22_DET0 [2]: BPI_BUS21_SWP3 [3]: BPI_BUS20_SWP2 [4]: BPI_BUS19_SWP1 [5]: BPI_BUS18_SWP0 [6]: BPI_BUS17_VM1 [7]: BPI_BUS16_VM0 [8]: BPI_BUS15_ANT3 [9]: BPI_BUS14_ANT2 [10]: BPI_BUS13_ANT1 [11]: BPI_BUS12_ANT0 [12]: BPI_BUS11

Bit(s)	Mnemonic	Name	Description
			[13]: BPI_BUS10 [14]: BPI_BUS9 [15]: BPI_BUS8 [16]: BPI_BUS7 [17]: BPI_BUS6 [18]: BPI_BUS5 [19]: BPI_BUS4 [20]: BPI_BUS0 [21]: BPI_BUS1 [22]: BPI_BUS2 [23]: BPI_BUS3

10002C14 IES_CFG1_SET **IES Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BPI_U							
Type									WO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPI_U															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		BPI_U	**Bitwise SET operation for IES control of BPI IO** 0: Keep 1: SET bits

10002C18 IES_CFG1_CLR **IES Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BPI_U							
Type									WO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPI_U															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		BPI_U	**Bitwise CLR operation for IES control of BPI IO** 0: Keep 1: CLR bits

10002C20 SR_CFG0 **SMT Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										BSI_U						

Type										RW						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI_U				BPI_U							SYS_U				
Type	RW				RW							RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
22:12		BSI_U	**SR control of BSI IO** [0]: MISC_MIPI_CK_2 0: Disable 1: Enable [1]: MISC_MIPI_DO_2 [2]: MISC_MIPI_CK_3 [3]: MISC_MIPI_DO_3 [4]: MISC_MIPI_CK_0 [5]: MISC_MIPI_DO_0 [6]: MISC_MIPI_CK_1 [7]: MISC_MIPI_DO_1 [8]: RFIC0_BSI_CK [9]: RFIC0_BSI_EN [10]: RFIC0_BSI_D0, RFIC0_BSI_D1, RFIC0_BSI_D2
11:5		BPI_U	**SR control of BPI IO** [0]: BPI_BUS23_DET1 [1]: BPI_BUS18_SWP0, BPI_BUS19_SWP1, BPI_BUS20_SWP2, BPI_BUS21_SWP3, BPI_BUS22_DET0 [2]: BPI_BUS16_VM0, BPI_BUS17_VM1 [3]: BPI_BUS12_ANT0, BPI_BUS13_ANT1, BPI_BUS14_ANT2, BPI_BUS15_ANT3 [4]: BPI_BUS8, BPI_BUS9, BPI_BUS10, BPI_BUS11 [5]: BPI_BUS4, BPI_BUS5, BPI_BUS6, BPI_BUS7 [6]: BPI_BUS0, BPI_BUS1, BPI_BUS2, BPI_BUS3
4:0		SYS_U	**SR control of SYS IO** [0]: DISP_PWM [1]: DSI_TE [2]: LCM_RST [3]: IDDIG [4]: TESTMODE

10002C24 SR_CFG0_SET **SMT Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										BSI_U						
Type										WO						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI_U				BPI_U							SYS_U				
Type	WO				WO							WO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
22:12		BSI_U	**Bitwise SET operation for SR control of BSI IO** 0: Keep

Bit(s)	Mnemonic	Name	Description
			1: SET bits
11:5		BPI_U	**Bitwise SET operation for SR control of BPI IO**
4:0		SYS_U	**Bitwise SET operation for SR control of SYS IO**

10002C28 SR_CFG0_CLR **SMT Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										BSI_U						
Type										WO						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI_U				BPI_U							SYS_U				
Type	WO				WO							WO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
22:12		BSI_U	**Bitwise CLR operation for SR control of BSI IO** 0: Keep 1: CLR bits
11:5		BPI_U	**Bitwise CLR operation for SR control of BPI IO**
4:0		SYS_U	**Bitwise CLR operation for SR control of SYS IO**

10002C30 SMT_CFG0 **SMT Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											BSI_U					
Type											RW					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI_U					BPI_U							SYS_U			
Type	RW					RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:11		BSI_U	**SMT control of BSI IO** [0]: MISC_MIPI_CK_2 0: Disable 1: Enable [1]: MISC_MIPI_DO_2 [2]: MISC_MIPI_CK_3 [3]: MISC_MIPI_DO_3 [4]: MISC_MIPI_CK_0 [5]: MISC_MIPI_DO_0 [6]: MISC_MIPI_CK_1 [7]: MISC_MIPI_DO_1 [8]: RFIC0_BSI_CK [9]: RFIC0_BSI_EN [10]: RFIC0_BSI_D0, RFIC0_BSI_D1, RFIC0_BSI_D2
10:4		BPI_U	**SMT control of BPI IO** [0]: BPI_BUS23_DET1 [1]: BPI_BUS18_SWP0, BPI_BUS19_SWP1,

Bit(s)	Mnemonic	Name	Description
			BPI_BUS20_SWP2, BPI_BUS21_SWP3, BPI_BUS22_DET0 [2]: BPI_BUS16_VM0, BPI_BUS17_VM1 [3]: BPI_BUS12_ANT0, BPI_BUS13_ANT1, BPI_BUS14_ANT2, BPI_BUS15_ANT3 [4]: BPI_BUS8, BPI_BUS9, BPI_BUS10, BPI_BUS11 [5]: BPI_BUS4, BPI_BUS5, BPI_BUS6, BPI_BUS7 [6]: BPI_BUS0, BPI_BUS1, BPI_BUS2, BPI_BUS3
3:0		SYS_U	**SMT control of SYS IO** [0]: DISP_PWM [1]: DSI_TE [2]: LCM_RST [3]: IDDIG [4]: TESTMODE

10002C34 SMT_CFG0_SET **SMT Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											BSI_U					
Type											WO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI_U					BPI_U							SYS_U			
Type	WO					WO							WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:11		BSI_U	**Bitwise SET operation for SMT Control of BSI IO** 0: Keep 1: SET bits
10:4		BPI_U	**Bitwise SET operation for SMT Control of BPI IO**
3:0		SYS_U	**Bitwise SET operation for SMT Control of SYS IO**

10002C38 SMT_CFG0_CLR **SMT Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											BSI_U					
Type											WO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI_U					BPI_U							SYS_U			
Type	WO					WO							WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:11		BSI_U	**Bitwise CLR operation for SMT Control of BSI IO** 0: Keep 1: CLR bits
10:4		BPI_U	**Bitwise CLR operation for SMT Control of BPI IO**

Bit(s)	Mnemonic	Name	Description
3:0		SYS_U	**Bitwise CLR operation for SMT Control of SYS IO**

10002C40 RDSEL_CFG0 RDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													BSI_U			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI_U		BPI_U												SYS_U	
Type	RW		RW												RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:14		BSI_U	**RDSEL Control of BSI IO** [1:0]: MISC_MIPI_CK_2, MISC_MIPI_DO_2, MISC_MIPI_CK_3, MISC_MIPI_DO_3 [3:2]: MISC_MIPI_CK_0, MISC_MIPI_DO_0, MISC_MIPI_CK_1, MISC_MIPI_DO_1 [5:4]: RFIC0_BSI_D0, RFIC0_BSI_D1, RFIC0_BSI_D2, RFIC0_BSI_CK, RFIC0_BSI_EN
13:2		BPI_U	**RDSEL Control of BPI IO** [1:0]: BPI_BUS23_DET1, BPI_BUS22_DET0, BPI_BUS21_SWP3, BPI_BUS20_SWP2 [3:2]: BPI_BUS19_SWP1, BPI_BUS18_SWP0, BPI_BUS17_VM1, BPI_BUS16_VM0 [5:4]: BPI_BUS13_ANT1, BPI_BUS12_ANT0, BPI_BUS15_ANT3, BPI_BUS14_ANT2 [7:6]: BPI_BUS11, BPI_BUS10, BPI_BUS9, BPI_BUS8 [9:8]: BPI_BUS7, BPI_BUS6, BPI_BUS5, BPI_BUS4 [11:10]: BPI_BUS3, BPI_BUS2, BPI_BUS1, BPI_BUS0
1:0		SYS_U	**RDSEL control of SYS IO** [1:0]: DISP_PWM, DSI_TE, LCM_RST, IDDIG, TESTMODE

10002C44 RDSEL_CFG0_SET RDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													BSI_U			
Type													WO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI_U		BPI_U												SYS_U	
Type	WO		WO												WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:14		BSI_U	**Bitwise SET operation for RDSEL control of BSI IO** 0: Keep

Bit(s)	Mnemonic	Name	Description
			1: SET bits
13:2		BPI_U	**Bitwise SET operation for RDSEL control of BPI IO**
1:0		SYS_U	**Bitwise SET operation for RDSEL control of SYS IO**

10002C48 RDSEL_CFG0_CLR **RDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													BSI_U			
Type													WO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI_U		BPI_U												SYS_U	
Type	WO		WO												WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:14		BSI_U	**Bitwise CLR operation for RDSEL control of BSI IO** 0: Keep 1: CLR bits
13:2		BPI_U	**Bitwise CLR operation for RDSEL control of BPI IO**
1:0		SYS_U	**Bitwise CLR operation for RDSEL control of SYS IO**

10002C50 TDSEL_CFG0 **TDSEL Control** **000F0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SLP			
Type													RW			
Reset													1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI_U												SYS_U			
Type	RW												RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:16		SLP	**TDSEL value for sleep mode** [3:0]: TDSEL value of IOs in top side in sleep mode Suggested value: 0xF
15:4		BSI_U	**TDSEL control of BSI IO** [3:0]: MISC_MIPI_CK_2, MISC_MIPI_DO_2, MISC_MIPI_CK_3, MISC_MIPI_DO_3 [7:4]: MISC_MIPI_CK_0, MISC_MIPI_DO_0, MISC_MIPI_CK_1, MISC_MIPI_DO_1 [11:8]: RFIC0_BSI_D0, RFIC0_BSI_D1, RFIC0_BSI_D2, RFIC0_BSI_CK, RFIC0_BSI_EN
3:0		SYS_U	**TDSEL control of SYS IO** [3:0]: DISP_PWM, DSI_TE, LCM_RST, IDDIG, TESTMODE

Bit(s)	Mnemonic	Name	Description

10002C54 TDSEL_CFG0_SET **TDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SLP			
Type													WO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI_U												SYS_U			
Type	WO												WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:16		SLP	**Bitwise SET operation for TDSEL value for sleep mode** 0: Keep 1: SET bits
15:4		BSI_U	**Bitwise SET operation for TDSEL control of BSI IO**
3:0		SYS_U	**Bitwise SET operation for TDSEL control of SYS IO**

10002C58 TDSEL_CFG0_CLR **TDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SLP			
Type													WO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI_U												SYS_U			
Type	WO												WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:16		SLP	**Bitwise CLR operation for TDSEL value for sleep mode** 0: Keep 1: CLR bits
15:4		BSI_U	**Bitwise CLR operation for TDSEL control of BSI IO**
3:0		SYS_U	**Bitwise CLR operation for TDSEL control of SYS IO**

10002C60 TDSEL_CFG1 **TDSEL Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BPI_U							
Type									RW							

Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPI_U															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		BPI_U	**TDSEL control of BPI IO** [3:0]: BPI_BUS23_DET1, BPI_BUS22_DET0, BPI_BUS21_SWP3, BPI_BUS20_SWP2 [7:4]: BPI_BUS19_SWP1, BPI_BUS18_SWP0, BPI_BUS17_VM1, BPI_BUS16_VM0 [11:8]: BPI_BUS13_ANT1, BPI_BUS12_ANT0, BPI_BUS15_ANT3, BPI_BUS14_ANT2 [15:12]: BPI_BUS11, BPI_BUS10, BPI_BUS9, BPI_BUS8 [19:16]: BPI_BUS7, BPI_BUS6, BPI_BUS5, BPI_BUS4 [23:20]: BPI_BUS3, BPI_BUS2, BPI_BUS1, BPI_BUS0

10002C64 TDSEL_CFG1_SET TDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BPI_U							
Type									WO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPI_U															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		BPI_U	**Bitwise SET operation for TDSEL control of BPI IO** 0: Keep 1: SET bits

10002C68 TDSEL_CFG1_CLR TDSEL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BPI_U							
Type									WO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPI_U															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		BPI_U	**Bitwise CLR operation for TDSEL control of BPI IO** 0: Keep

Bit(s)	Mnemonic	Name	Description
			1: CLR bits

10002C70 PD_CFG0 PD Control 0003FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															BSI_U	
Type															RW	
Reset															1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI_U											SYS_U				
Type	RW											RW				
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
17:5		BSI_U	**Pull-down control of BSI IO** [0]: MISC_MIPI_CK_2 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: MISC_MIPI_DO_2 [2]: MISC_MIPI_CK_3 [3]: MISC_MIPI_DO_3 [4]: MISC_MIPI_CK_0 [5]: MISC_MIPI_DO_0 [6]: MISC_MIPI_CK_1 [7]: MISC_MIPI_DO_1 [8]: RFIC0_BSI_CK [9]: RFIC0_BSI_EN [10]: RFIC0_BSI_D0 [11]: RFIC0_BSI_D1 [12]: RFIC0_BSI_D2
4:0		SYS_U	**Pull-down control of SYS IO** [0]: DISP_PWM PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: DSI_TE [2]: LCM_RST [3]: IDDIG [4]: TESTMODE

10002C74 PD_CFG0_SET PD Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															BSI_U	
Type															WO	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI_U											SYS_U				

Type	WO											WO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:5		BSI_U	**Bitwise SET operation for pull-down control of BSI IO** 0: Keep 1: SET bits
4:0		SYS_U	**Bitwise SET operation for pull-down control of SYS IO**

10002C78 PD_CFG0_CLR **PD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															BSI_U	
Type															WO	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI_U											SYS_U				
Type	WO											WO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:5		BSI_U	**Bitwise CLR operation for pull-down control of BSI IO** 0: Keep 1: CLR bits
4:0		SYS_U	**Bitwise CLR operation for pull-down control of SYS IO**

10002C80 PD_CFG1 **PD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BPI_U							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPI_U															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		BPI_U	**Pull-down control of BPI IO** [0]: BPI_BUS23_DET1 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: BPI_BUS22_DET0 [2]: BPI_BUS21_SWP3

Bit(s)	Mnemonic	Name	Description
			[3]: BPI_BUS20_SWP2 [4]: BPI_BUS19_SWP1 [5]: BPI_BUS18_SWP0 [6]: BPI_BUS17_VM1 [7]: BPI_BUS16_VM0 [8]: BPI_BUS15_ANT3 [9]: BPI_BUS14_ANT2 [10]: BPI_BUS13_ANT1 [11]: BPI_BUS12_ANT0 [12]: BPI_BUS11 [13]: BPI_BUS10 [14]: BPI_BUS9 [15]: BPI_BUS8 [16]: BPI_BUS7 [17]: BPI_BUS6 [18]: BPI_BUS5 [19]: BPI_BUS4 [20]: BPI_BUS0 [21]: BPI_BUS1 [22]: BPI_BUS2 [23]: BPI_BUS3

10002C84 PD_CFG1_SET **PD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BPI_U							
Type									WO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPI_U															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		BPI_U	**Bitwise SET operation for pull-down control of BPI IO** 0: Keep 1: SET bits

10002C88 PD_CFG1_CLR **PD Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BPI_U							
Type									WO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPI_U															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		BPI_U	**Bitwise CLR operation for pull-down control of BPI IO** 0: Keep 1: CLR bits

10002C90 PU_CFG0 PU Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															BSI_U	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI_U											SYS_U				
Type	RW											RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:5		BSI_U	**Pull-up control of BSI IO** [0]: MISC_MIPI_CK_2 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: MISC_MIPI_DO_2 [2]: MISC_MIPI_CK_3 [3]: MISC_MIPI_DO_3 [4]: MISC_MIPI_CK_0 [5]: MISC_MIPI_DO_0 [6]: MISC_MIPI_CK_1 [7]: MISC_MIPI_DO_1 [8]: RFIC0_BSI_CK [9]: RFIC0_BSI_EN [10]: RFIC0_BSI_D0 [11]: RFIC0_BSI_D1 [12]: RFIC0_BSI_D2
4:0		SYS_U	**Pull-up control of SYS IO** [0]: DISP_PWM PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm 1/1: N/A [1]: DSI_TE [2]: LCM_RST [3]: IDDIG [4]: TESTMODE

10002C94 PU_CFG0_SET PU Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															BSI_U	
Type															WO	

Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI_U											SYS_U				
Type	WO											WO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:5		BSI_U	**Bitwise SET operation for pull-up control of BSI IO** 0: Keep 1: SET bits
4:0		SYS_U	**Bitwise SET operation for pull-up control of SYS IO**

10002C98 PU_CFG0_CLR **PU Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															BSI_U	
Type															WO	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI_U											SYS_U				
Type	WO											WO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:5		BSI_U	**Bitwise CLR operation for pull-up control of BSI IO** 0: Keep 1: CLR bits
4:0		SYS_U	**Bitwise CLR operation for pull-up control of SYS IO**

10002CA0 PU_CFG1 **PU Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BPI_U							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPI_U															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		BPI_U	**Pull-up control of BPI IO** [0]: BPI_BUS23_DET1 PU/PD: 0/0: N/A 1/0: Pull up with 75Kohm 0/1: Pull down with 75Kohm

Bit(s)	Mnemonic	Name	Description
			1/1: N/A [1]: BPI_BUS22_DET0 [2]: BPI_BUS21_SWP3 [3]: BPI_BUS20_SWP2 [4]: BPI_BUS19_SWP1 [5]: BPI_BUS18_SWP0 [6]: BPI_BUS17_VM1 [7]: BPI_BUS16_VM0 [8]: BPI_BUS15_ANT3 [9]: BPI_BUS14_ANT2 [10]: BPI_BUS13_ANT1 [11]: BPI_BUS12_ANT0 [12]: BPI_BUS11 [13]: BPI_BUS10 [14]: BPI_BUS9 [15]: BPI_BUS8 [16]: BPI_BUS7 [17]: BPI_BUS6 [18]: BPI_BUS5 [19]: BPI_BUS4 [20]: BPI_BUS0 [21]: BPI_BUS1 [22]: BPI_BUS2 [23]: BPI_BUS3

10002CA4 PU_CFG1_SET **PU Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BPI_U							
Type									WO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPI_U															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		BPI_U	**Bitwise SET operation for pull-up control of BPI IO** 0: Keep 1: SET bits

10002CA8 PU_CFG1_CLR **PU Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BPI_U							
Type									WO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPI_U															
Type	WO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		BPI_U	**Bitwise CLR operation for pull-up control of BPI IO** 0: Keep 1: CLR bits

10002CB0 DRV_CFG0 **DRV Control** **00555555**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BPI_U							
Type									RW							
Reset									0	1	0	1	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPI_U				BSI_U										SYS_U	
Type	RW				RW										RW	
Reset	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
23:12		BPI_U	**Driving control of BPI IO** [1:0]: BPI_BUS23_DET1, BPI_BUS22_DET0, BPI_BUS21_SWP3, BPI_BUS20_SWP2 00: 2mA 01: 4mA 10: 6mA 11: 8mA [3:2]: BPI_BUS19_SWP1, BPI_BUS18_SWP0, BPI_BUS17_VM1, BPI_BUS16_VM0 [5:4]: BPI_BUS13_ANT1, BPI_BUS12_ANT0, BPI_BUS15_ANT3, BPI_BUS14_ANT2 [7:6]: BPI_BUS11, BPI_BUS10, BPI_BUS9, BPI_BUS8 [9:8]: BPI_BUS7, BPI_BUS6, BPI_BUS5, BPI_BUS4 [11:10]: BPI_BUS3, BPI_BUS2, BPI_BUS1, BPI_BUS0
11:2		BSI_U	**Driving control of SYS IO** [1:0]: MISC_MIPI_CK_2, MISC_MIPI_DO_2, MISC_MIPI_CK_3, MISC_MIPI_DO_3 00: 2mA 01: 4mA 10: 6mA 11: 8mA [3:2]: MISC_MIPI_CK_0, MISC_MIPI_DO_0, MISC_MIPI_CK_1, MISC_MIPI_DO_1 [5:4]: RFIC0_BSI_D0, RFIC0_BSI_D1, RFIC0_BSI_D2, RFIC0_BSI_CK, RFIC0_BSI_EN [7:6]: Reserved [9:8]: Reserved
1:0		SYS_U	**Driving control of SYS IO** [1:0]: DISP_PWM, DSI_TE, LCM_RST, IDDIG, TESTMODE 00: 2mA 01: 4mA 10: 6mA 11: 8mA

10002CB4 DRV_CFG0_SET **DRV Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BPI_U							
Type									WO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPI_U				BSI_U										SYS_U	
Type	WO				WO										WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:12		BPI_U	**Bitwise SET operation for driving Control of BPI IO** 0: Keep 1: SET bits
11:2		BSI_U	**Bitwise SET operation for driving control of BSI IO**
1:0		SYS_U	**Bitwise SET operation for driving control of SYS IO**

10002CB8 DRV_CFG0_CLR **DRV Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BPI_U							
Type									WO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPI_U				BSI_U										SYS_U	
Type	WO				WO										WO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:12		BPI_U	**Bitwise CLR operation for driving Control of BPI IO** 0: Keep 1: CLR bits
11:2		BSI_U	**Bitwise CLR operation for driving Control of BSI IO**
1:0		SYS_U	**Bitwise CLR operation for driving Control of SYS IO**

10002D00 DUMMY **DUMMY** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name									DUMMY							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		DUMMY	**Dummy register** [7:0]: Dummy register

10002D04 DUMMY_SET **DUMMY** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DUMMY							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		DUMMY	**Bitwise SET operation for dummy register** 0: Keep 1: SET bits

10002D08 DUMMY_CLR **DUMMY** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DUMMY							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		DUMMY	**Bitwise CLR operation for dummy register** 0: Keep 1: CLR bits

3.3 Keypad Scanner

Module name: KP Base address: (+10010000h)

Address	Name	Width	Register Function
10010000	KP_STA	16	Keypad Status
10010004	KP_MEM1	16	Keypad Scanning Output Register
10010008	KP_MEM2	16	Keypad Scanning Output Register
1001000C	KP_MEM3	16	Keypad Scanning Output Register
10010010	KP_MEM4	16	Keypad Scanning Output Register
10010014	KP_MEM5	16	Keypad Scanning Output Register
10010018	KP_DEBOUNCE	16	De-bounce Period Setting
1001001C	KP_SCAN_TIMING	16	Keypad Scan Timing Adjustment Register
10010020	KP_SEL	16	Keypad Selection Register
10010024	KP_EN	16	Keypad Enable Register

10010000 KP_STA Keypad Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STA
Type																RO
Reset																0

Bit(s)	Mnemonic	Name	Description
0	STA	STA	**Indicates keypad status** This register will not be cleared by the read operation. 0: No key pressed 1: Key pressed

10010004 KP_MEM1 Keypad Scanning Output Register 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY15	KEY14	KEY13	KEY12	KEY11	KEY10	KEY9	KEY8	KEY7	KEY6	KEY5	KEY4	KEY3	KEY2	KEY1	KEY0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
15	KEY15	KEY15	
14	KEY14	KEY14	
13	KEY13	KEY13	

Bit(s)	Mnemonic	Name	Description
12	**KEY12**	KEY12	
11	**KEY11**	KEY11	
10	**KEY10**	KEY10	
9	**KEY9**	KEY9	
8	**KEY8**	KEY8	
7	**KEY7**	KEY7	
6	**KEY6**	KEY6	
5	**KEY5**	KEY5	
4	**KEY4**	KEY4	
3	**KEY3**	KEY3	
2	**KEY2**	KEY2	
1	**KEY1**	KEY1	
0	**KEY0**	KEY0	

10010008 KP_MEM2 **Keypad Scanning Output Register** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY31	KEY30	KEY29	KEY28	KEY27	KEY26	KEY25	KEY24	KEY23	KEY22	KEY21	KEY20	KEY19	KEY18	KEY17	KEY16
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
15	**KEY31**	KEY31	
14	**KEY30**	KEY30	
13	**KEY29**	KEY29	
12	**KEY28**	KEY28	
11	**KEY27**	KEY27	
10	**KEY26**	KEY26	
9	**KEY25**	KEY25	
8	**KEY24**	KEY24	
7	**KEY23**	KEY23	
6	**KEY22**	KEY22	
5	**KEY21**	KEY21	
4	**KEY20**	KEY20	
3	**KEY19**	KEY19	
2	**KEY18**	KEY18	
1	**KEY17**	KEY17	
0	**KEY16**	KEY16	

1001000C KP_MEM3 **Keypad Scanning Output Register** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY47	KEY46	KEY45	KEY44	KEY43	KEY42	KEY41	KEY40	KEY39	KEY38	KEY37	KEY36	KEY35	KEY34	KEY33	KEY32
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
15	**KEY47**	KEY47	
14	**KEY46**	KEY46	
13	**KEY45**	KEY45	
12	**KEY44**	KEY44	
11	**KEY43**	KEY43	
10	**KEY42**	KEY42	
9	**KEY41**	KEY41	
8	**KEY40**	KEY40	
7	**KEY39**	KEY39	
6	**KEY38**	KEY38	
5	**KEY37**	KEY37	
4	**KEY36**	KEY36	
3	**KEY35**	KEY35	
2	**KEY34**	KEY34	
1	**KEY33**	KEY33	
0	**KEY32**	KEY32	

10010010 KP_MEM4 **Keypad Scanning Output Register** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY63	KEY62	KEY61	KEY60	KEY59	KEY58	KEY57	KEY56	KEY55	KEY54	KEY53	KEY52	KEY51	KEY50	KEY49	KEY48
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
15	**KEY63**	KEY63	
14	**KEY62**	KEY62	
13	**KEY61**	KEY61	
12	**KEY60**	KEY60	
11	**KEY59**	KEY59	
10	**KEY58**	KEY58	
9	**KEY57**	KEY57	
8	**KEY56**	KEY56	
7	**KEY55**	KEY55	
6	**KEY54**	KEY54	
5	**KEY53**	KEY53	
4	**KEY52**	KEY52	
3	**KEY51**	KEY51	
2	**KEY50**	KEY50	
1	**KEY49**	KEY49	
0	**KEY48**	KEY48	

Bit(s)	Mnemonic	Name	Description

10010014 KP_MEM5 **Keypad Scanning Output Register** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY1		KEY77	KEY76	KEY75	KEY74	KEY73	KEY72	KEY71	KEY70	KEY69	KEY68	KEY67	KEY66	KEY65	KEY64
Type	RO		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
15:14	**DUMMY1**	DUMMY1	
13	**KEY77**	KEY77	
12	**KEY76**	KEY76	
11	**KEY75**	KEY75	
10	**KEY74**	KEY74	
9	**KEY73**	KEY73	
8	**KEY72**	KEY72	
7	**KEY71**	KEY71	
6	**KEY70**	KEY70	
5	**KEY69**	KEY69	
4	**KEY68**	KEY68	
3	**KEY67**	KEY67	
2	**KEY66**	KEY66	
1	**KEY65**	KEY65	
0	**KEY64**	KEY64	

10010018 KP_DEBOUNCE **De-bounce Period Setting** **00000400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEBOUNCE													
Type			RW													
Reset			0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13:0	**DEBOUNCE**	DEBOUNCE	De-bounce time = KP_DEBOUNCE/32 ms.

1001001C KP_SCAN_TIMING **Keypad Scan Timing Adjustment Register** **00000011**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COL_HIGH_PULSE				ROW_HIGH_PULSE				COL_SCAN_DIV				ROW_SCAN_DIV			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1

Bit(s)	Mnemonic	Name	Description
15:12	**COL_ HIGH_PULSE**	COL_HIGH_PULSE	**Sets up the COL SCAN high pulse, i.e. cycles of the scan high pulse** Default 0 means the high scan pulse needs 1 cycle.
11:8	**ROW_ HIGH_PULSE**	ROW_HIGH_PULSE	**Sets up the ROW SCAN high pulse, i.e. cycles of the scan high pulse** Default 0 means the high scan pulse needs 1 cycle.
7:4	**COL_SCAN_DIV**	COL_SCAN_DIV	**Sets up the COL SCAN cycle which includes COL_INTERVAL_DIV and the high pulse period** Default 1 means there are 2 cycles for each scan, including 1 cycle high pulse and 1 cycle interval.
3:0	**ROW_SCAN_DIV**	ROW_SCAN_DIV	**Sets up the ROW SCAN cycle which includes ROW_INTERVAL_DIV and the high pulse period** Default 1 means there are 2 cycles for each scan, including 1 cycle high pulse and 1 cycle interval.

10010020 KP_SEL **Keypad Selection Register** **00001C70**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KP1_COL_SEL						KP1_ROW_SEL						DUMMY2			KP_SEL
Type	RW						RW						RW			DC
Reset	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:10	**KP1_COL_SEL**	KP1_COL_SEL	**Selects which cols are used when double keypad is used** MT6797 supports maximum 3*3 double. col2, col1 and col0 can be used. 0: Disable corresponding column 1: Enable corresponding column
9:4	**KP1_ROW_SEL**	KP1_ROW_SEL	**Selects which rows are used when double keypad is used** MT6797 supports maximum 3*3 double. row2, row1 and row0 can be used. 0: Disable corresponding row 1: Enable corresponding row
3:1	**DUMMY2**	DUMMY2	
0	**KP_SEL**	KP_SEL	**Selects to use single keypad or double keypad** 0: Use single keypad 1: Use double keypad

Bit(s)	Mnemonic	Name	Description

10010024 KP_EN **Keypad Enable Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																KP_EN
Type																RW
Reset																1

Bit(s)	Mnemonic	Name	Description
0	KP_EN	KP_EN	

3.4 UART

Module name: UARTo Base address: (+11002000h)

Address	Name	Width	Register Function
11002000	RBR	8	RX Buffer Register
11002004	IER	8	Interrupt Enable Register
11002000	THR	8	TX Holding Register
11002008	IIR	8	Interrupt Identification Register
1100200C	LCR	8	Line Control Register
11002008	FCR	8	FIFO Control Register
11002010	MCR	8	Modem Control Register
11002014	LSR	8	Line Status Register
11002018	MSR	8	Modem Status Register
1100201C	SCR	8	Scratch Register
11002090	DLL	8	Divisor Latch (LS)
11002094	DLM	8	Divisor Latch (MS)
11002098	EFR	8	Enhanced Feature Register
110020A0	XON1	8	XON1 Char Register
110020A4	XON2	8	XON2 Char Register
110020A8	XOFF1	8	XOFF1 Char Register
110020AC	XOFF2	8	XOFF2 Char Register
11002020	AUTOBAUD_EN	8	Auto Baud Detect Enable Register
11002024	HIGHSPEED	8	High Speed Mode Register
11002028	SAMPLE_COUNT	8	Sample Counter Register
1100202C	SAMPLE_POINT	8	Sample Point Register
11002030	AUTOBAUD_REG	8	Auto Baud Monitor Register
11002034	RATEFIX_AD	8	Clock Rate Fix Register
11002038	AUTOBAUDSAMPLE	8	Auto Baud Sample Register
1100203C	GUARD	8	Guard time added Register
11002040	ESCAPE_DAT	8	Escape Character Register
11002044	ESCAPE_EN	8	Escape Enable Register
11002048	SLEEP_EN	8	Sleep Enable Register
1100204C	DMA_EN	8	DMA Enable Register
11002050	RXTRI_AD	8	Rx Trigger Address
11002054	FRACDIV_L	8	Fractional Divider LSB Address
11002058	FRACDIV_M	8	Fractional Divider MSB Address
1100205C	FCR_RD	8	FIFO Control Register
1100209C	FEATURE_SEL	8	UART Feature Select Register
110020B4	SLEEP_REQ	8	UART Sleep request Register
110020B8	SLEEP_ACK	8	UART Idle Register
110020BC	SPM_SEL	8	SPM Interface Selection Register

11002000 RBR **RX Buffer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RBR							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RBR	**Read-only register** The received data can be read by accessing this register.

11002004 IER **Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CTSI	RTSI	XOFFI		EDSSI	ELSI	ETBEI	ERBFI
Type									RW	RW	RW		RW	RW	RW	RW
Reset									0	0	0		0	0	0	0

Bit(s)	Name	Description
7	CTSI	**Masks an interrupt that is generated when a rising edge is detected on the CTS modem control line.** *Note: This interrupt is only enabled when hardware flow control is enabled.* 0: Mask an interrupt that is generated when a rising edge is detected on the CTS modem control line. 1: Unmask an interrupt that is generated when a rising edge is detected on the CTS modem control line.
6	RTSI	**Masks an interrupt that is generated when a rising edge is detected on the RTS modem control line.** *Note: This interrupt is only enabled when hardware flow control is enabled.* 0: Mask an interrupt that is generated when a rising edge is detected on the RTS modem control line. 1: Unmask an interrupt that is generated when a rising edge is detected on the RTS modem control line.
5	XOFFI	**Masks an interrupt that is generated when an XOFF character is received.** *Note: This interrupt is only enabled when software flow control is enabled.* 0: Mask an interrupt that is generated when an XOFF character is received. 1: Unmask an interrupt that is generated when an XOFF character is received.
3	EDSSI	**When set to 1, an interrupt will be generated if DCTS (MSR[0]) becomes set.** 0: No interrupt is generated if DCTS (MSR[0]) becomes set. 1: An interrupt is generated if DCTS (MSR[0]) becomes set.
2	ELSI	**When set to 1, an interrupt will be generated if BI, FE, PE or OE (LSR[4:1]) becomes set.** 0: No interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.

Bit(s)	Name	Description
		1: An interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.
1	ETBEI	**When set to 1, an interrupt will be generated if TX holding register is empty or the contents of TX FIFO are reduced to its trigger level.** 0: No interrupt will be generated if TX holding register is empty or the contents of TX FIFO are reduced to its trigger level. 1: An interrupt will be generated if TX holding register is empty or the contents of TX FIFO are reduced to its trigger level
0	ERBFI	**When set to 1, an interrupt will be generated if RX data are placed in RX buffer register or RX trigger level is reached.** 0: No interrupt will be generated if RX data are placed in RX buffer register or RX trigger level is reached. 1: An interrupt will be generated if RX data are placed in RX buffer register or RX trigger level is reached.

11002000 THR **TX Holding Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									THR							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	THR	**TX holding register (write only)** The data to be transmitted are written to this register then sent to the PC via serial communication.

11002008 IIR **Interrupt Identification Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFOE		ID					
Type									RO		RU					
Reset									0	0	0	0	0	0	0	1

Bit(s)	Name	Description
7:6	FIFOE	
5:0	ID	**IIR[5:0] Priority level interrupt source** 000001 - No interrupt pending 000110 1 Line status interrupt: BI, FE, PE or OE set in LSR (under IER[2]=1) 001100 2 RX data timeout: Timeout on character in RX FIFO (under IER[0]=1) 000100 3 RX data received: RX data received or RX trigger level reached (under IER[0]=1)

Bit(s)	Name	Description
		000010 4 TX holding register empty: TX holding register empty or TX FIFO trigger level reached (under IER[1]=1) 000000 5 Modem status change: DDCD, TERI, DDSR or DCTS set in MSR (under IER[3]=1) 010000 6 Software flow control: XOFF character received (under IER[5]=1) 100000 7 Hardware flow control: CTS or RTS rising edge (under IER[7]=1 or IER[6]=1) Line status interrupt: A RX line status interrupt (IIR[5:0]=000110b) will be generated if ELSI (IER[2]) is set and any of BI, FE, PE or OE (LSR[4:1]) becomes set. The interrupt is cleared by reading the line status register. RX data timeout interrupt: When virtual FIFO mode is disabled, RX data timeout interrupt will be generated if all the following apply: 1. FIFO contains at least one character; 2. The most recent character was received longer than four character periods ago (including all start, parity and stop bits); 3. The most recent CPU read of the FIFO was longer than four character periods ago. The timeout timer is restarted upon receipt of a new byte from the RX shift register or on a CPU read from the RX FIFO. The RX data timeout interrupt is enabled by setting EFRBI (IER[0]) to 1 and cleared by reading RX FIFO. When virtual FIFO mode is enabled, RX data timeout interrupt will be generated if all the following apply: 1. FIFO is empty; 2. The most recent character was received longer than four character periods ago (including all start, parity and stop bits); 3. The most recent CPU read of the FIFO was longer than four character periods ago. The timeout timer is restarted upon receipt of a new byte from the RX shift register or reading DMA_EN register. The RX data timeout interrupt is enabled by setting EFRBI (IER[0]) to 1 and cleared by reading DMA_EN register. RX data received interrupt: A RX received interrupt (IER[5:0]=000100b) will be generated if EFRBI (IER[0]) is set and either RX data are placed in the RX buffer register or the RX trigger level is reached. The interrupt is cleared by reading the RX buffer register or the RX FIFO (if enabled). TX holding register empty interrupt: A TX holding register empty interrupt (IIR[5:0]=000010b) will be generated if ETRBI (IER[1]) is set and either the TX holding register is empty or the contents of TX FIFO are reduced to its trigger level. The interrupt is cleared by writing TX holding register or TX FIFO if FIFO enabled. Modem status change interrupt: A modem status change interrupt (IIR[5:0]=000000b) will be generated if EDSSI (IER[3]) is set and either DDCD, TERI, DDSR or DCTS (MSR[3:0]) becomes set. The interrupt is cleared by reading the modem status register.

Bit(s)	Name	Description
		Software flow control interrupt: A software flow control interrupt (IIR[5:0]=010000b) will be generated if software flow control is enabled and XOFFI (IER[5]) becomes set, indicating that an XOFF character has been received. The interrupt is cleared by reading the interrupt identification register. Hardware flow control interrupt: A hardware flow control interrupt (IER[5:0]=100000b) will be generated if hardware flow control is enabled and either RTSI (IER[6]) or CTSI (IER[7]) becomes set, indicating that a rising edge has been detected on either the RTS/CTS modem control line. The interrupt is cleared by reading the interrupt identification register.

1100200C LCR **Line Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLAB	SB	SP	EPS	PEN	STB	WLS1_WLS0	
Type									RW	RW	RW	RW	RW	RW	RW	
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	DLAB	**Divisor latch access bit** 0: The RX and TX Registers are read/written at Address 0 and the IER register is read/written at Address 4. 1: The Divisor Latch LS is read/written at Address 0 and the Divisor Latch MS is read/written at Address 4.
6	SB	**Sets up break** 0: No effect 1: SOUT signal is forced into the 0 state.
5	SP	**Stick parity** 0: No effect 1: The parity bit is forced into a defined state, depending on the states of EPS and PEN: If EPS=1 & PEN=1, the parity bit will be set and checked = 0. If EPS=0 and PEN=1, the parity bit will be set and checked = 1.
4	EPS	**Selects even parity** 0: When EPS=0, an odd number of ones is sent and checked. 1: When EPS=1, an even number of ones is sent and checked.
3	PEN	**Enables parity** 0: The parity is neither transmitted nor checked. 1: The parity is transmitted and checked.
2	STB	**Number of STOP bits** 0: One STOP bit is always added. 1: Two STOP bits are added after each character is sent; unless the character length is 5 when 1 STOP bit is added.
1:0	WLS1_WLS0	**Selects word length** 0: 5 bits 1: 6 bits 2: 7 bits 3: 8 bits

11002008 FCR **FIFO Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**RFTL1_RFTL0**		**TFTL1_TFTL0**			**CLRT**	**CLRR**	**FIFOE**
Type									WO		WO			WO	WO	WO
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
7:6	RFTL1_RFTL0	**RX FIFO trigger threshold** RX FIFO contains total 32 bytes. 0: 1 1: 6 2: 12 3: RXTRIG
5:4	TFTL1_TFTL0	**TX FIFO trigger threshold** TX FIFO contains total 32 bytes. 0: 1 1: 4 2: 8 3: 14
2	CLRT	**Control bit to clear TX FIFO** 0: No effect 1: Clear TX FIFO
1	CLRR	**Control bit to clear RX FIFO** 0: No effect 1: Clear RX FIFO
0	FIFOE	**Enables FIFO** This bit should be set to 1 for any of the other bits in the registers to have any effect. 0: Disable both RX and TX FIFOs. 1: Enable both RX and TX FIFOs.

11002010 MCR **Modem Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**XOFF_STATUS**			**Loop**			**RTS**	
Type									RU			RW			RW	
Reset									0			0			0	

Bit(s)	Name	Description
7	XOFF_STATUS	**This is a read-only bit.** 0: When an XON character is received. 1: When an XOFF character is received.

Bit(s)	Name	Description
4	Loop	**Loop-back control bit** 0: No loop-back is enabled. 1: Loop-back mode is enabled.
1	RTS	**Controls the state of the output NRTS, even in loop mode** 0: RTS will always output 1. 1: RTS's output will be controlled by flow control condition.

11002014 LSR **Line Status Register** **00000060**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFO ERR	TEMT	THRE	BI	FE	PE	OE	DR
Type									RU	RU	RU	RU	RU	RU	RU	RU
Reset									0	1	1	0	0	0	0	0

Bit(s)	Name	Description
7	FIFOERR	**RX FIFO error indicator** 0: No PE, FE, BI set in RX FIFO 1: Set to 1 when there is at least one PE, FE or BI in RX FIFO.
6	TEMT	**TX holding register (or TX FIFO) and TX shift register are empty.** 0: Empty conditions below are not met. 1: If FIFOs are enabled, the bit will be set whenever TX FIFO and TX shift register are empty. If FIFOs are disabled, the bit will be set whenever TX holding register and TX shift register are empty.
5	THRE	**Indicates if there is room for TX holding register or TX FIFO is reduced to its trigger level** 0: Reset whenever the contents of TX FIFO are more than its trigger level (FIFOs are enabled), or whenever TX holding register is not empty (FIFOs are disabled). 1: Set whenever the contents of TX FIFO are reduced to its trigger level (FIFOs are enabled), or whenever TX holding register is empty and ready to accept new data (FIFOs are disabled).
4	BI	**Break interrupt** 0: Reset by the CPU reading this register 1: If the FIFOs are disabled, this bit will be set whenever the SIN is held in the 0 state for more than one transmission time (START bit + DATA bits + PARITY + STOP bits). If the FIFOs are enabled, this error will be associated with a corresponding character in FIFO and is flagged when this byte is at the top of the FIFO. When a break occurs, only one zero character is loaded into FIFO: the next character transfer will be enabled when SIN enters the marking state and receives the next valid start bit.
3	FE	**Framing error** 0: Reset by the CPU reading this register 1: If the FIFOs are disabled, this bit will be set if the received data did not have a valid STOP bit. If the FIFOs are enabled, the state of this bit will be revealed when the byte it refers to is the next to be read.
2	PE	**Parity error** 0: Reset by the CPU reading this register 1: If the FIFOs are disabled, this bit will be set if the received data did not have a valid parity bit. If the FIFOs are enabled, the state of this

Bit(s)	Name	Description
		bit will be revealed when the referred byte is the next to be read.
1	OE	**Overrun error** 0: Reset by the CPU reading this register. 1: If the FIFOs are disabled, this bit will be set if the RX buffer was not read by the CPU before new data from the RX shift register overwrote the previous contents. If the FIFOs are enabled, an overrun error will occur when RX FIFO is full and RX shift register becomes full. OE is set as soon as this happens. The character in the shift register is then overwritten but not transferred to the FIFO.
0	DR	**Data ready** 0: Cleared by CPU reading RX buffer or by reading all FIFO bytes. 1: Set by RX buffer becoming full or by FIFO becoming not empty.

11002018 MSR **Modem Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CTS				DCTS
Type												RU				RW
Reset												0				0

Bit(s)	Name	Description
4	CTS	**Clear to send** When Loop = 0, this value is the complement of the NCTS input signal. When Loop = 1, this value is equal to the RTS bit in modem control register.
0	DCTS	**Delta clear to send** 0: Cleared if the state of CTS has not changed since this register was last read. 1: Set if the state of CTS has changed since this register was last read.

1100201C SCR **Scratch Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SCR							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SCR	**General-purpose read/write register** After reset, its value will be un-defined.

11002090 DLL **Divisor Latch (LS)** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLL							
Type									RW							
Reset									0	0	0	0	0	0	0	1

Bit(s)	Name	Description
7:0	DLL	**Divisor latch low 8-bit data**

11002094 DLM **Divisor Latch (MS)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLM							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DLM	**Divisor latch high 8-bit data** *Note: Division by 1 generates a BAUD signal that is constantly high. DLL and DLM setting formula is {DLH,DLL}=(system clock frequency/baud_pulse/baud_rate).* When RATE_FIX(RATEFIX_AD[0])=0, system clock frequency = 52MHz. When RATE_FIX(RATEFIX_AD[0])=1 and RATE_FIX(RATEFIX_AD[2])=0, system clock frequency = 26MHz. When RATE_FIX(RATEFIX_AD[0])=1 and RATE_FIX(RATEFIX_AD[2])=1, system clock frequency = 13MHz. For baud_pulse value, refer to HIGH_SPEED(offset=24H) register, e.g. when 52MHz, default speed mode and 115200 baud rate, the {DLH,DLL}=52MHz/16/115200=28.

11002098 EFR **Enhanced Feature Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AUTO_CTS	AUTO_RTS		ENABLE_E	SW_FLOW_CONT			
Type									RW	RW		RW	RW			
Reset									0	0		0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
7	AUTO_CTS	**Enables hardware transmission flow control** 0: Disable 1: Enable
6	AUTO_RTS	**Enables hardware reception flow control** 0: Disable 1: Enable
4	ENABLE_E	**Enables enhancement feature** 0: Disable 1: Enable
3:0	SW_FLOW_CONT	**Software flow control bits** 00xx: No TX flow control 10xx: Transmit XON1/XOFF1 as flow control bytes 01xx: Transmit XON2/XOFF2 as flow control bytes xx00: No RX Flow Control xx10: Receive XON1/XOFF1 as flow control bytes xx01: Receive XON2/XOFF2 as flow control bytes

110020A0 XON1 **XON1 Char Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON1							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XON1	XON1 character for software flow control

110020A4 XON2 **XON2 Char Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XON2	XON2 character for software flow control

110020A8 XOFF1 **XOFF1 Char Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF1							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XOFF1	XOFF1 character for software flow control

110020AC XOFF2 XOFF2 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XOFF2	XOFF2 character for software flow control

11002020 AUTOBAUD_EN Auto Baud Detect Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														sleep_ack_sel	AUTOBAUD_SEL	AUTOBAUD_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	sleep_ack_sel	0: Send sleep_ack when autobaud_en is enabled and autobaud state machine and RX is idle . 1: Cannot send sleep_ack when autobaud_en is enabled.
1	AUTOBAUD_SEL	**Selects auto-baud** 0: Support standard baud rate detection 1: Support non_standard baud rate detection (only support baud from 300 to 115200; use 52MHZ to auto fix)
0	AUTOBAUD_EN	**Auto-baud enable signal** 0: Disable auto-baud function 1: Enable auto-baud function (UARTn+0024h SPEED should be set to 0) Note: When AUTOBAUD_EN is active, there should not be A*/a*

Bit(s)	Name	Description
		char before the auto baud char AT/at. If the A*/a* is inevitable, the autobaud will fail. Disable AUTOBAUD_EN to reset autobaud and autobaud_en again.

11002024 HIGHSPEED High Speed Mode Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SPEED	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	SPEED	**UART sample counter base** 0: Based on 16*baud_pulse, baud_rate = system clock frequency/16/{DLH, DLL} 1: Based on 8*baud_pulse, baud_rate = system clock frequency/8/{DLH, DLL} 2: Based on 4*baud_pulse, baud_rate = system clock frequency/4/{DLH, DLL} 3: Based on sampe_count*baud_pulse, baud_rate = system clock frequency/(sampe_count+1)/{DLM, DLL}

11002028 SAMPLE_COUNT Sample Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SAMPLECOUNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SAMPLECOUNT	Only useful when HIGHSPEED mode=3

1100202C SAMPLE_POINT Sample Point Register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SAMPLEPOINT							

Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	SAMPLEPOINT	**SAMPLE_POINT = (SAMPLE_COUNT-1)/2 without the decimal.** Sample point is effective only when HIGHSPEED=3.

11002030 AUTOBAUD_REG **Auto Baud Monitor Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BAUD_STAT				BAUD_RATE			
Type									RU				RU			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:4	BAUD_STAT	**Autobaud format** 0: Autobaud is detecting. 1: AT_7N1 2: AT_7O1 3: AT_7E1 4:AT_8N1 5: AT_8O1 6: AT_8E1 7: at_7N1 8: at_7E1 9: at_7O1 10: at_8N1 11: at_8E1 12: at_8O1 13: Autobaud detection fails.
3:0	BAUD_RATE	**Autobaud baud rate** 0: 115200 1: 57600 2: 38400 3: 19200 4: 9600 5: 4800 6: 2400 7: 1200 8: 300 9: 110

11002034 RATEFIX_AD **Clock Rate Fix Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FREQ_SEL	AUTOBAUD_RATE_FIX	RATE_FIX
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FREQ_SEL	0: system clock = UART_CLK_SRC/2 1: system clock = UART_CLK_SRC/4
1	AUTOBAUD_RATE_FIX	0: System clock = UART_CLK_SRC/1 (UART_CLK_SRC = 52MHz or 26MHz) 1: System clock = UART_CLK_SRC/2 or UART_CLK_SRC/4 (depending on FREQ_SEL)
0	RATE_FIX	0: System clock = UART_CLK_SRC/1 (UART_CLK_SRC = 52MHz or 26MHz) 1: System clock = UART_CLK_SRC/2 or UART_CLK_SRC/4 (depending on FREQ_SEL)

11002038 AUTOBAUDSAMPLE Auto Baud Sample Register 0000000D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											AUTOBAUDSAMPLE					
Type											RW					
Reset											0	0	1	1	0	1

Bit(s)	Name	Description
5:0	AUTOBAUDSAMPLE	**Detects clk division for autobaud rate** For standard baud rate detection. system clk 52m: 'd 27 system clk 26m: 'd 13 system clk 13m: 'd 6 For non-standard baud rate detection: :15

1100203C GUARD Guard time added Register 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												GUARD_EN	GUARD_CNT			
Type												RW	RW			

Reset												0	1	1	1	1

Bit(s)	Name	Description
4	GUARD_EN	**Guard interval add enable signal** 0: No guard interval added 1: Add guard interval after stop bit
3:0	GUARD_CNT	**Guard interval count value** Guard interval = [1/(system clock/div_step/div)]*GUARD_CNT

11002040 ESCAPE_DAT **Escape Character Register** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ESCAPE_DAT							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	ESCAPE_DAT	**Escape character added before software flow control data and escape character** That is, if TX data are xon (31h), with esc_en =1, UART will transmit data as esc + CEh (~xon).

11002044 ESCAPE_EN **Escape Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ESC_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	ESC_EN	**Adds escape character in transmitter and removes escape character in receiver by UART** 0: Does not deal with the escape character 1: Add escape character in transmitter and remove escape character in receiver

11002048 SLEEP_EN **Sleep Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SLEEP_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	SLEEP_EN	**For sleep mode issue** 0: Does not deal with sleep mode indication signal 1: Activate HW flow control or software control according to software initial setting when chip enters sleep mode. Release HW flow when chip wakes up. For software control, UART sends xon when awakens and FIFO does not reach threshold level.

1100204C DMA_EN **DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													FIFO_lsr_sel	TO_CNT_AUTORST	TX_DMA_EN	RX_DMA_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	FIFO_lsr_sel	**Selects FIFO LSR mode** 0: LSR will hold the first line status error state until you read the LSR register. 1: LSR will update automatically with read data from RX FIFO.
2	TO_CNT_AUTORST	**Timeout counter auto reset register** 0: After RX timeout happens, SW should reset the interrupt by reading UART 0x4C. 1: The timeout counter will be auto reset. Set up this register when new DMA is used.
1	TX_DMA_EN	**TX_DMA mechanism enable signal** 0: Does not use DMA in TX. 1: Use DMA in TX. When this reguster is enabled, the flow control is based on the DMA threshold and generates a timeout interrupt for DMA.
0	RX_DMA_EN	**RX_DMA mechanism enable signal** 0: Does not use DMA in RX 1: Use DMA in RX. When this reguster is enabled, the flow control is based on the DMA threshold and generates a timeout interrupt.

11002050 RXTRI_AD **Rx Trigger Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RXTRIG			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RXTRIG	**When {rtm,rtl}=2'b11, the RX FIFO threshold will be Rxtrig.** Make the value smaller than half of RX FIFO size, which is 32 bytes.

11002054 FRACDIV_L **Fractional Divider LSB Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FRACDIV_L							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FRACDIV_L	**Adds sampling count (+1) from state data7 to data0 to contribute fractional divisor** Only when high_speed=3.

11002058 FRACDIV_M **Fractional Divider MSB Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FRACDIV_M	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	FRACDIV_M	**Adds sampling count when in state stop to parity to contribute fractional divisor** Only when high_speed=3.

1100205C FCR_RD **FIFO Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name									RFTL1_RFTL0		TFTL1_TFTL0			CLRT	CLRR	FIFOE
Type									RO		RO			RO	RO	RO
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
7:6	RFTL1_RFTL0	**RX FIFO trigger threshold** RX FIFO contains total 32 bytes. 0: 1 1: 6 2: 12 3: RXTRIG
5:4	TFTL1_TFTL0	**TX FIFO trigger threshold** TX FIFO contains total 32 bytes. 0: 1 1: 4 2: 8 3: 14
2	CLRT	0: TX FIFO is not cleared. 1: TX FIFO is cleared.
1	CLRR	0: RX FIFO is not cleared. 1: RX FIFOis cleared.
0	FIFOE	**Enables FIFO** Set this bit to 1 for any of the other bits in the registers to have any effect. 0: RX and TX FIFOs are not enabled. 1: RX and TX FIFOs are enabled.

1100209C FEATURE_SEL UART Feature Select Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FEATURE_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	FEATURE_SEL	**For AP MCU side UART, if new UART register map is used, feature_sel should be kept at 1.** 0: Disable new register map 1: Enable new register map

110020B4 SLEEP_REQ UART Sleep request Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SLEEP_REQ
Type																RW
Reset																0

Bit(s)	Name	Description
0	SLEEP_REQ	0: Cancel sleep request to UART (after wakeup sent by CPU) 1: Send sleep request to UART (before sleep sent by CPU)

110020B8 SLEEP_ACK **UART Idle Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SLEEP_ACK
Type																RU
Reset																1

Bit(s)	Name	Description
0	SLEEP_ACK	0: UART is not in idle state (CPU can poll this register to get the UART state). 1: UART is in idle state (CPU can poll this register to get the UART state).

110020BC SPM_SEL **SPM Interface Selection Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SPM_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	SPM_SEL	0: SPM sleep interface will not be used. 1: SPM sleep interface will be used.

3.5 USB 2.0 High Speed Dual-Role Controller

Module name: Unified_USB Base address: (+11200000h)

Address	Name	Width	Register Function
11200000	FADDR	8	Function Address Register (Device Mode Only)
11200001	POWER_PERI	8	Power Management Register
11200001	POWER_HOST	8	Power Management Register
11200002	INTRTX	16	Tx Interrupt Status Register
11200004	INTRRX	16	Rx Interrupt Status Register
11200006	INTRTXE	16	Tx Interrupt Enable Register
11200008	INTRRXE	16	Rx Interrupt Enable Register
1120000A	INTRUSB	8	Common USB Interrupt Register
1120000B	INTRUSBE	8	Common USB Interrupt Enable Register
1120000C	FRAME	16	Frame Number Register
1120000E	INDEX	8	Endpoint Selection Index Register
1120000F	TESTMODE	8	Test Mode Enable Register
11200010	TXMAP	16	TXMAP Register
11200012	TXCSR_PERI	16	TX CSR Register
11200012	TXCSR_HOST	16	TX CSR Register
11200014	RXMAP	16	RXMAP Register
11200016	RXCSR_PERI	16	RX CSR Register
11200016	RXCSR_HOST	16	RX CSR Register
11200018	RXCOUNT	16	RX Count Register
1120001A	TXTYPE	8	TxType Register
1120001B	TXINTERVAL	8	TxInterval Register
1120001C	RXTYPE	8	RxType Register
1120001D	RXINTERVAL	8	RxInterval Register
1120001F	FIFOSIZE	8	Configured FIFO Size Register
11200020	FIFO0	32	USB Endpoint 0 FIFO Register
11200024	FIFO1	32	USB Endpoint 1 FIFO Register
11200060	DEVCTL	8	Device Control Register
11200061	PWRUPCNT	8	Power Up Counter Register
11200062	TXFIFOSZ	8	TX FIFO Size Register
11200063	RXFIFOSZ	8	RX FIFO Size Register
11200064	TXFIFOADD	16	TX FIFO Address Register
11200066	RXFIFOADD	16	RX FIFO Address Register
1120006C	HWCAPS	16	Hardware Capability Register
1120006E	HWSVERS	16	Version Register
11200070	BUSPERF1	16	USB Bus Performance Register 1
11200072	BUSPERF2	16	USB Bus Performance Register 2
11200074	BUSPERF3	16	USB Bus Performance Register 3
11200078	EPINFO	8	Number of TX and RX Register
11200079	RAMINFO	8	Width of RAM and Number of DMA Channel Register
1120007A	LINKINFO	8	Delay to be Applied Register
1120007B	VPLEN	8	Vbus Pulsing Charge Register
1120007C	HS_EOF1	8	Time Buffer Available on HS Transaction Register
1120007D	FS_EOF1	8	Time Buffer Available on FS Transaction Register

Address	Name	Width	Register Function
1120007E	LS_EOF1	8	Time Buffer Available on LS Transaction Register
1120007F	RST_INFO	8	Reset Information Register
11200080	RXTOG	16	Rx Data Toggle Set/Status Register
11200082	RXTOGEN	16	Rx Data Toggle Enable Register
11200084	TXTOG	16	Tx Data Toggle Set/Status Register
11200086	TXTOGEN	16	Tx Data Toggle Enable Register
112000A0	USB_L1INTS	32	USB Level 1 Interrupt Status Register
112000A4	USB_L1INTM	32	USB Level 1 Interrupt Mask Register
112000A8	USB_L1INTP	32	USB Level 1 Interrupt Polarity Register
112000AC	USB_L1INTC	32	USB Level 1 Interrupt Control Register
11200102	CSR0_PERI	16	EP0 Control Status Register
11200102	CSR0_HOST	16	EP0 Control Status Register
11200108	COUNT0	16	EP0 Received Bytes Register
1120010A	Type0	8	EP0 Type Register
1120010B	NAKLIMT0	8	NAK Limit Register
1120010C	SRAMCONFIGSIZE	16	SRAM Size Register
1120010E	HBCONFIGDATA	8	High Bind-width Configuration Register
1120010F	CONFIGDATA	8	Core Configuration Register
11200110	TX1MAP	16	TX1MAP Register
11200112	TX1CSR_PERI	16	Tx1 CSR Register
11200112	TX1CSR_HOST	16	Tx1 CSR Register
11200114	RX1MAP	16	RX1MAP Register
11200116	RX1CSR_PERI	16	RX1 CSR Register
11200116	RX1CSR_HOST	16	Rx1 CSR Register
11200118	RX1COUNT	16	Rx1 Count Register
1120011A	TX1TYPE	8	Tx1Type Register
1120011B	TX1INTERVAL	8	Tx1Interval Register
1120011C	RX1TYPE	8	Rx1Type Register
1120011D	RX1INTERVAL	8	Rx1Interval Register
1120011F	FIFOSIZE1	8	EP1 Configured FIFO Size Register
11200200	DMA_INTR	32	DMA Interrupt Status Register
11200210	DMA_LIMITER	32	DMA Limiter Register
11200220	DMA_CONFIG	32	DMA Configuration Register
11200204	DMA_CNTL_0	16	DMA Channel 0 Control Register
11200208	DMA_ADDR_0	32	DMA Channel 0 Address Register
1120020C	DMA_COUNT_0	32	DMA Channel 0 Byte Count Register
11200304	EP1RXPKTCOUNT	16	EP1 RxPktCount Register
11200480	T0FUNCADDR	16	T0 Function Address Register
11200488	T1FUNCADDR	16	T1 Function Address Register
11200482	T0HUBADDR	16	T0 HUB Address Register
1120048A	T1HUBADDR	16	T1 HUB Address Register
1120048C	R1FUNCADDR	16	R1 Function Address Register
1120048E	R1HUBADDR	16	R1 HUB Address Register
11200604	TM1	16	Test Mode 1 Register
11200608	HWVER_DATE	32	HW Version Control Register
11200684	SRAMA	32	SRAM Address Register

Address	Name	Width	Register Function
11200688	SRAMD	32	SRAM Data Register
11200690	RISC_SIZE	32	RISC Size Register
11200700	RESREG	32	Reserved Register
11200730	OTG20_CSRL	8	OTG20 Related Control Register L
11200731	OTG20_CSRH	8	OTG20 Related Control Register H

11200000 FADDR **Function Address Register (Device Mode Only)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										FUNCTION_ADDRESS						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	FUNCTION_ADDRESS	**FAddr is an 8-bit register that should be written with the 7-bit address of the peripheral part of the transaction.** When the USB2.0 controller is used In peripheral mode (DevCtl.bit2=0), this register should be written with the address received through a SET_ADDRESS command, which will then be used for decoding the function address in subsequent token packets. When the USB2.0 controller is used In host mode (DevCtl.bit2=1), Function address is configured by TXFUNCADDR and RXFUNCADDR.

11200001 POWER_PERI **Power Management Register** **00000020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ISOUPDATE	SOFTCONN	HSENAB	HSMODE	RESET	RESUME	SUSPENDMODE	ENABLESUSPENDM
Type									RW	RW	RW	RU	RU	RW	RU	RW
Reset									0	0	1	0	0	0	0	0

Bit(s)	Name	Description
7	ISOUPDATE	**When set by the CPU, the USB2.0 controller will wait for an SOF token from the time TxPktRdy is set before sending the packet.** If an IN token is received before an SOF token, a 0 length data packet will be sent. *Note: Only valid In peripheral mode. Also, This bit only affectss*

Bit(s)	Name	Description
		endpoints performing Isochronous transfers.
6	SOFTCONN	**If Soft Connect/Disconnect feature is enabled, the USB D+/D- lines is enabled when this bit will be set by the CPU and tri-stated when this bit is cleared by the CPU.** In Peripheral FS mode, clearing the Softcon bit may need the execution of latency until USB BUS SE0 is detected by HW. Execution Latency ~= 1ms. Such as SOF Packet EOP or RESET In Peripheral HS mode, clear Softcon bit still need execution latency until USB BUS SE0 is detected by HW. Execution Latency ~= 1us. Note: Set this bit only In peripheral mode. For Host mode, this bit will be set if DEVCTL[0] session bit is set. This bit should also be cleared if session bit is cleared by CPU.
5	HSENAB	**When set by the CPU, the USB2.0 controller will negotiate for high-speed mode when the device is reset by the hub.** If not set, the device will only operate in full-speed mode.
4	HSMODE	**When set, this read-only bit indicates the high-speed mode is successfully negotiated during USB reset.** In peripheral mode, it becomes valid when USB reset is completed (as indicated by USB reset interrupt). In host mode, it becomes valid when the Reset bit is cleared. Remains valid for the duration of the session. *Note: Allowance is made for Tiny-J signaling in determining the transfer speed to select.*
3	RESET	**Set when Reset signaling is present on the bus.** Note: This bit is read/write from the CPU in host mode but read-only In peripheral mode.
2	RESUME	**Set by the CPU to generate resume signaling when the function is in Suspend mode.** The CPU clears this bit after 10ms (max. 15ms) to end resume signaling. In host mode, this bit is also automatically set when resume signaling from the target is detected while the USB2.0 controller is suspended.
1	SUSPENDMODE	**In host mode, this bit is set by the CPU to enter suspend mode.** In peripheral mode, this bit is set on entryo into suspend mode. It is cleared when the CPU reads the interrupt register or sets up the Resume bit above.
0	ENABLESUSPENDM	**Set by the CPU to enable the SUSPENDM output**

11200001 POWER_HOST Power Management Register 00000020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**HSENAB**	**HSMODE**	**RESET**	**RESUME**	**SUSPENDMODE**	**ENABLESUSPENDM**
Type											RW	RU	RW	RW	A0	RW
Reset											1	0	0	0	0	0

Bit(s)	Name	Description
5	HSENAB	**When set by the CPU, the USB2.0 controller will**

Bit(s)	Name	Description
		negotiate for high-speed mode when the device is reset by the hub. If not set, the device will only operate in full-speed mode.
4	HSMODE	**When set, this read-only bit indicates the high-speed mode is successfully negotiated during USB reset.** In peripheral mode, it becomes valid when USB reset is completed (as indicated by USB reset interrupt). In host mode, it becomes valid when the Reset bit is cleared. Remains valid for the duration of the session. *Note: Allowance is made for Tiny-J signaling in determining the transfer speed to select.*
3	RESET	**Set when Reset signaling is present on the bus.** *Note: This bit is read/write from the CPU in host mode but read-only In peripheral mode.*
2	RESUME	**Set by the CPU to generate resume signaling when the function is in Suspend mode.** The CPU clears this bit after 10ms (max. 15ms) to end resume signaling. In host mode, this bit is also automatically set when resume signaling from the target is detected while the USB2.0 controller is suspended.
1	SUSPENDMODE	**In host mode, this bit is set by the CPU to enter suspend mode.** In peripheral mode, this bit is set on entryo into suspend mode. It is cleared when the CPU reads the interrupt register or sets up the Resume bit above.
0	ENABLESUSPENDM	**Set by the CPU to enable the SUSPENDM output**

11200002 INTRTX **Tx Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															EP1_TX	EP0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	EP1_TX	T1 Endpoint N interrupt event
0	EP0	Endpointo interrupt event

11200004 INTRRX **Rx Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															EP1_RX	
Type															W1C	
Reset															0	

Bit(s)	Name	Description
1	EP1_RX	

11200006 INTRTXE Tx Interrupt Enable Register 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															EP1_TXE	EP0_E
Type															RW	RW
Reset															1	1

Bit(s)	Name	Description
1	EP1_TXE	1'b0: Disable TX Endpoint N interrupt event 1'b1: Enable TX Endpoint N interrupt event
0	EP0_E	1'b0: Disable TX Endpoint N interrupt event 1'b1: Enable TX Endpoint N interrupt event

11200008 INTRRXE Rx Interrupt Enable Register 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															EP1_RXE	
Type															RW	
Reset															1	

Bit(s)	Name	Description
1	EP1_RXE	1'b0: Disable RX Endpoint N interrupt event 1'b1: Enable RX Endpoint N interrupt event

1120000A INTRUSB Common USB Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									VBUSERROR	SESSREQ	DISCON	CONN	SOF	RESET_BABLE	RESUME	SUSPEND
Type									W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	VBUSERROR	**Set when VBus drops below the VBus Valid threshold during a session.** Only valid when USB2.0 controller is 'A' device.
6	SESSREQ	**Set when session request signaling has been detected.** Only valid when USB2.0 controller is 'A' device.
5	DISCON	**Set In host mode when a device disconnect is detected. Set In peripheral mode when a session ends.** Valid at all transaction speeds.
4	CONN	**Set when a device connection is detected.** Only valid in host mode. Valid at all transaction speeds.
3	SOF	**Set when a new frame starts.**
2	RESET_BABLE	**Set In peripheral mode when Reset signaling is detected on the bus. Set In host mode when babble is detected.** *Note: Only active after the first SOF has been sent.*
1	RESUME	**Set when resume signaling is detected on the bus while the USB2.0 controller is in Suspend mode.**
0	SUSPEND	**Set when suspend signaling is detected on the bus.** Only valid In peripheral mode.

1120000B INTRUSBE **Common USB Interrupt Enable Register** **00000006**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									VBUSERROR_E	SESSREQ_E	DISCON_E	CONN_E	SOF_E	RESET_BABLE_E	RESEUM_E	SUSPEND_E
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	1	1	0

Bit(s)	Name	Description
7	VBUSERROR_E	Enables VBusError interrupt
6	SESSREQ_E	Enables SessReq interrupt
5	DISCON_E	Enables Discon interrupt
4	CONN_E	Enables Conn interrupt
3	SOF_E	Enables SOF interrupt
2	RESET_BABLE_E	Enables Reset/Babble interrupt
1	RESEUM_E	Enables Resume interrupt
0	SUSPEND_E	Enables Suspend interrupt

1120000C FRAME **Frame Number Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						FRAME_NUMBER										
Type						RU										

Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	FRAME_NUMBER	Frame is a 11-bit read-only register that holds the last received frame number.

1120000E INDEX **Endpoint Selection Index Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SELECTED_ENDPOINT			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	SELECTED_ENDPOINT	**Each TX endpoint and each RX endpoint has its own set of control/status registers located between USB+100h - USB+1FFh.** In addition, one set of TX control/status and one set of RX control/status registers appear at USB+010h - USB+01Fh. Index is a 4-bit register that determines which endpoint control/status registers are accessed. Before accessing an endpoint's control/status registers at USB+010h - USB+01Fh, the endpoint number should be written to the Index register to ensure that the correct control/status registers appear in the memory map.

1120000F TESTMODE **Test Mode Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FORCE_HOST	FIFO_ACCESS	FORCE_FS	FORCE_HS	TEST_PACKET	TEST_K	TEST_J	TEST_SEo_NAK
Type									RW	A0	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	FORCE_HOST	**The CPU sets up this bit to instruct the core to enter Host mode when the Session bit is set, regardless of whether it is connected to any peripheral.** The state of the CID input, HostDisconnect and LineState signals are ignored. The core will then remain In host mode until the Session bit is cleared, even if a device is disconnected, and if the Force_Host bit remains set, will re-enter Host mode the next time the Session bit is set.While in this mode, the status of the HOSTDISCON signal from the PHY may be read from bit 7 of the

Bit(s)	Name	Description
		ACTLR0.DevCtl register. The operating speed is determined from the Force_HS and Force_FS bits as follows. USB2.0 IP only Force_HS Force_FS Operating Speed 0 0 Low Speed 0 1 Full Speed 1 0 High Speed 1 1 Undefined
6	FIFO_ACCESS	**The CPU sets up this bit to transfer the packet in the Endpoint 0 TX FIFO to the Endpoint 0 RX FIFO** It is cleared automatically. USB2.0 IP only.
5	FORCE_FS	**The CPU sets up this bit either in conjunction with bit 7 above or to force the USB2.0 controller into full speed mode when it receives a USB reset**
4	FORCE_HS	**The CPU sets up this bit either in conjunction with bit 7 above or to force the USB2.0 controller into high-speed mode when it receives a USB reset.** USB2.0 IP only.
3	TEST_PACKET	**(HS_MODE) The CPU sets up this bit to enter the Test_Packet test mode.** In this mode, the USB2.0 controller repetitively transmits on the bus a 53-byte test packet, the form of which is defined in the Universal Serial Bus Specification Revision 2.0, Section 7.1.20. *Note: The test packet has a fixed format and must be loaded into the Endpoint 0 FIFO before the test mode is entered. USB2.0 IP only.*
2	TEST_K	**(HS_MODE) The CPU sets up this bit to enter the Test_K test mode.** In this mode, the USB2.0 controller transmits a continuous K on the bus. USB2.0 IP only.
1	TEST_J	**(HS_MODE) The CPU sets up this bit to enter the Test_J test mode.** In this mode, the USB2.0 controller transmits a continuous J on the bus. USB2.0 IP only.
0	TEST_SE0_NAK	**(HS_MODE) The CPU sets up this bit to enter the Test_SE0_NAK test mode.** In this mode, the USB2.0 controller remains in high-speed mode but responds to any valid IN token with a NAK. USB2.0 IP only.

11200010 TXMAP **TXMAP Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**M_1**		**MAXIMUM_PAYLOAD_TRANSACTION**										
Type				RW		RW										
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:11	M_1	**Maximum payload size for indexed TX endpoint, M-1 Packet multiplier m maximum payload transaction register**
10:0	MAXIMUM_PAYLOAD_TRANSACTION	**The TxMaxP register defines the maximum amount of data that can be transferred through the selected TX endpoint in asingle operation.** There is a TxMaxP register for each TX endpoint (except for

Bit(s)	Name	Description
		Endpoint 0). Bits 10:0 define (in bytes) the maximum payload transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in full-speed and high-speed operations. Where the option of High-bandwidth Isochronous endpoints or of packet splitting on Bulk endpoints has been taken when the core is configured, the register includes either 2 or 5 further bits that define a multiplier m which is equal to one more than the value recorded. In the case of Bulk endpoints with the packet splitting option enabled, the multiplier m can be up to 32 and defines the maximum number of 'USB' packets (i.e. packets for transmission over the USB) of the specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. (If the packet splitting option is not enabled, bit15-13 will not be implemented and bit12-11 (if included) will be ignored.) Note: The data packet is required to be an exact multiple of the payload specified by bits 10:0, which is itself required to be either 8, 16, 32, 64 or (in the case of high-speed transfers) 512 bytes. for isochronous endpoints operating in high-speed mode and with the high-bandwidth option enabled, m may only be either 2 or 3 (corresponding to bit 11 set or bit 12 set, respectively) and it specifies the maximum number of such transactions that can take place in a single microframe. If either bit 11 or bit 12 is non-0, the USB2.0 controller will automatically split any data packet written to the FIFO into up to 2 or 3 'USB' packets, each containing the specified payload (or less). The maximum payload for each transaction is 1024 bytes, so this allows up to 3072 bytes to be transmitted in each microframe. (For Isochronous/Interrupt transfers in Full-speed mod, bits 11 and 12 are ignored.) The value written to bits 10:0 (multiplied by m in the case of high-bandwidth Isochronous transfers) must match the value given in the wMaxPacketSize field of the Standard Endpoint Descriptor for the associated endpoint . A mismatch can cause unexpected results. The total amount of data represented by the value written to this register (specified payload * m) must not exceed the FIFO size for the TX endpoint and should not exceed half the FIFO size if double-buffering is required. If this register is changed after packets have been sent from the endpoint, the TX endpoint FIFO should be completely flushed (using the FlushFIFO bit in TxCSR) after writing the new value to this register.

11200012 TXCSR_PERI TX CSR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOSET	ISO		DMAREQEN	FRCDATATOG	DMAREQMODE		SETTXPKTRDY_TWICE	INCOMPTX	CLRDATATOG	SENTSTALL	SENDSTALL	FLUSHFIFO	UNDERRUN	FIFONOTEMPTY	TXPKTRDY

Type	RW	RW		RW	RW	RW		A1	A1	A0	A1	RW	A0	A1	RU	A0
Reset	0	0		0	0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUTOSET	**If The CPU sets up this bit, TxPktRdy will be automatically set when data of the maximum packet size (value in TxMaxP) is loaded into the TxFIFO.** If a packet of less than the maximum packet size is loaded, TxPktRdy will have to be set manually.
14	ISO	**The CPU sets up this bit to enable the TX endpoint for isochronous transfers and clears it to enable the TX endpoint for bulk or interrupt transfers.** *Note: This bit only has any effect In peripheral mode. In host mode, it always returns to 0.*
12	DMAREQEN	**The CPU sets up this bit to enable the DMA request for the TX endpoint.**
11	FRCDATATOG	**The CPU sets up this bit to force the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received.** This can be used by Interrupt TX endpoints that are used to communicate rate feedback for isochronous endpoints.
10	DMAREQMODE	**The CPU sets up this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0.** *Note: This bit must not be cleared either before or in the same cycle as the DMAReqEn bit is cleared.*
8	SETTXPKTRDY_TWICE	**Indicates TxPktRdy had been set when it is 1'b1 already** Write 0 to clear it.
7	INCOMPTX	**When the endpoint is used for high-bandwidth isochronous/interrupt transfers, this bit is set to indicate where a large packet has been split into 2 or 3 packets for transmission but insufficient IN tokens have been received to send all the parts.** *Note: In anything other than a high-bandwidth transfer, this bit will always return to 0. Write 0 to clear it.*
6	CLRDATATOG	**The CPU writes 1 to this bit to reset the endpoint data toggle to 0.**
5	SENTSTALL	**This bit is set when a STALL handshake is transmitted.** The FIFO is flushed, TX interrupt is generated if enabled and the TxPktRdy bit is cleared. Cleared by CPU. Write 0 to clear it.
4	SENDSTALL	**The CPU writes 1 to this bit to issue a STALL handshake to an IN token. The CPU clears this bit to terminate the stall condition.** Note: This bit has no effect where the endpoint is used for isochronous transfer. Otherwise, CPU should wait for SENTSTALL interrupt being generated before clearing the SENDSTALL bit.
3	FLUSHFIFO	**The CPU writes 1 to this bit to flush the latest packet from the endpoint TxFIFO.** The FIFO pointer is reset, the TxPktRdy bit is cleared and an interrupt is generated. May be set simultaneously with TxPktRdy to abort the packet that is currently being loaded into the FIFO. *Note: FlushFIFO should only be used when TxPktRdy is set. In other cases, it may cause data corruption. If the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.*
2	UNDERRUN	**The USB sets up this bit if an IN token is received when the TxPktRdy bit not set.** Cleared by CPU. Write 0 to clear it.
1	FIFONOTEMPTY	**The USB sets up this bit when there is at least 1 packet in TxFIFO.** This bit will be asserted automatically when TXPKTRDY is set by

Bit(s)	Name	Description
0	TXPKTRDY	CPU and de-asserteded when CPU flushes FIFO or sends a STALL packet. **The CPU sets up this bit after loading a data packet into FIFO.** It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled). TxPktRdy is also automatically cleared (interrupt is generated) prior to loading a second packet into a double-buffered FIFO.

11200012 TXCSR_HOST TX CSR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOSET			DMAREQEN	FRCDATATOG	DMAREQMODE		SETTXPKTRDY_TWICE	NAKTIMEOUT_INCOMPTX	CLRDATAOG	RXSTALL		FLUSHFIFO	ERROR	FIFONOTEMPTY	TXPKTRDY
Type	RW			RW	RW	RW		A1	A1	A0	A1		A0	A1	RU	A0
Reset	0			0	0	0		0	0	0	0		0	0	0	0

Bit(s)	Name	Description
15	AUTOSET	**If The CPU sets up this bit, TxPktRdy will be automatically set when data of the maximum packet size (value in TxMaxP) is loaded into the TxFIFO.** If a packet of less than the maximum packet size is loaded, TxPktRdy will have to be set manually.
12	DMAREQEN	**The CPU sets up this bit to enable the DMA request for the TX endpoint.**
11	FRCDATATOG	**The CPU sets up this bit to force the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received.** This can be used by Interrupt TX endpoints that are used to communicate rate feedback for isochronous endpoints.
10	DMAREQMODE	**The CPU sets up this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0.** Note: This bit must not be cleared either before or in the same cycle as the DMAReqEn bit is cleared.
8	SETTXPKTRDY_TWICE	**Indicates TxPktRdy had been set when it is 1'b1 already** Write 0 to clear it.
7	NAKTIMEOUT_INCOMPTX	**Bulk endpoints only: This bit will be set when the TX endpoint is halted following the receipt of NAK responses for longer than the time set as the NAK Limit by the TxInterval register.** The CPU clears this bit to allow the endpoint to continue. Write 0 to clear it.
6	CLRDATAOG	**The CPU writes 1 to this bit to reset the endpoint data toggle to 0.**
5	RXSTALL	**This bit is set when a STALL handshake is received.** When this bit is set, any DMA request that is in progress is topped, the FIFO is completely flushed, TX interrupt is generated if enabled and the TxPktRdy bit is cleared. Cleared by CPU. Write 0 to clear it.

Bit(s)	Name	Description
3	FLUSHFIFO	**The CPU writes 1 to this bit to flush the latest packet from the endpoint TxFIFO.** The FIFO pointer is reset, the TxPktRdy bit is cleared and an interrupt is generated. May be set simultaneously with TxPktRdy to abort the packet that is currently being loaded into the FIFO. *Note: FlushFIFO should only be used when TxPktRdy is set. In other cases, it may cause data corruption. If the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.*
2	ERROR	**The USB sets up this bit when 3 attempts have been made to send a packet and no handshake packet has been received.** When the bit is set, an interrupt will be generated, TxPktRdy cleared and FIFO completely flushed. Cleared by CPU. Valid only when the endpoint is operating in Bulk or Interrupt mode. Write 0 to clear it.
1	FIFONOTEMPTY	**The USB sets up this bit when there is at least 1 packet in TxFIFO.** This bit will be asserted automatically when TXPKTRDY is set by CPU and de-asserteded when CPU flushes FIFO or sends a STALL packet.
0	TXPKTRDY	**The CPU sets up this bit after loading a data packet into FIFO.** It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled). TxPktRdy is also automatically cleared (interrupt is generated) prior to loading a second packet into a double-buffered FIFO.

11200014 RXMAP **RXMAP Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**M_1**		**MAXIMUM_PAYLOAD_TRANSACTION**										
Type				RW		RW										
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:11	M_1	**Maximum payload size for indexed RX endpoint , M-1 Packet multiplier m**
10:0	MAXIMUM_PAYLOAD_TRANSACTION	**The RxMaxP register defines the maximum amount of data that can be transferred through the selected RX endpoint in a single operation.** There is a RxMaxP register for each RX endpoint (except for Endpoint 0). Bits 10:0 define (in bytes) the maximum payload transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-speed and High-speed operations. Where the option of High-bandwidth Isochronous endpoints or of combining Bulk packets has been taken when the core is configured, the register includes either 2 or 5 further bits

Bit(s)	Name	Description
		that define a multiplier m which is equal to one more than the value recorded. For Bulk endpoints with the packet combining option enabled, the multiplier m can be up to 32 and defines the number of USB packets of the specified payload which are to be combined into a single data packet within the FIFO. (If the packet splitting option is not enabled, bit15-bit13 is not implemented and bit12-bit11 (if included) is ignored.) for isochronous endpoints operating in high-speed mode and with the high-bandwidth option enabled, m may only be either 2 or 3 (corresponding to bit 11 set or bit 12 set, respectively) and it specifies the maximum number of such transactions that can take place in a single microframe. If either bit 11 or bit 12 is non-0, the USB2.0 controller will automatically combine the separate USB packets received in any microframe into a single packet within the RX FIFO. The maximum payload for each transaction is 1024 bytes, so this allows up to 3072 bytes to be received in each microframe. (For Isochronous/Interrupt transfers in full-speed mode or if High-bandwidth is not enabled, bits 11 and 12 are ignored.) The value written to bits 10:0 (multiplied by m in the case of high-bandwidth Isochronous transfers) must match the value given in the wMaxPacketSize field of the Standard Endpoint Descriptor for the associated endpoint . A mismatch can cause unexpected results. The total amount of data represented by the value written to this register (specified payload * m) must not exceed the FIFO size for the OUT endpoint and should not exceed half the FIFO size if double-buffering is required.

11200016 RXCSR_PERI RX CSR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOCLEAR	ISO	DMAREQEN	DISNYET_PIDERR	DMAREQMODE		KEEPERRSTATUS	INCOMPRX	CLRDATOG	SENTSTALL	SENDSTALL	FLUSHFIFO	DATAERR	OVERRUN	FIFOFULL	RXPKTRDY
Type	RW	RW	RW	RW	RW		RW	A1	A0	A1	RW	A0	RU	A1	RU	A1
Reset	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUTOCLEAR	**If CPU sets up this bit then the RxPktRdy bit will be automatically cleared when a packet of RxMaxP bytes has been unloaded from the RxFIFO.** When packets of less than the maximum packet size are unloaded, RxPktRdy will have to be cleared manually. *Note: The maximum packet size -3, -2, -1 is handled like the maximum packet size which is auto cleared by HW.*
14	ISO	**The CPU sets up this bit to enable the RX endpoint for isochronous transfers and clears it to enable the RX endpoint for bulk/interrupt transfers.**
13	DMAREQEN	**The CPU sets up this bit to enable the DMA request for the RX endpoint.**

Bit(s)	Name	Description
12	DISNYET_PIDERR	**The CPU sets up this bit to disable the sending of NYET handshakes.** When set, all successfully received Rx packets are ACK'd including at the point at which the RxFIFO becomes full. *Note: This bit only takes effect in high-speed mode in which it should be set for all interrupt endpoints.* This bit is set when there is a PID error in the received packet. It is cleared when RxPktRdy is cleared or write 0 to clear it.
11	DMAREQMODE	**The CPU sets up this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0.** DMA Request Mode 1: RX endpoint interrupt is generated only when DMA Request Mode 1 and received a short packet. RxDMAReq is generated when receiving a Max-Packet-size packet. DMA Request Mode 0: No RX endpoint interrupt. RxDMAReq is generated when RxPktRdy is set.
9	KEEPERRSTATUS	**Used when endpoint works with USBQ and in isochronous mode** When this bit is set, the isochronous error, PIDERROR, INCOMPRX and DATAERROR will be kept and only cleared by SW.
8	INCOMPRX	**This bit will be set in an isochronous transfer if the packet in RxFIFO is incomplete because part of the data are not received.** When KeepErrorStatus = 0, it is cleared when RxPktRdy is cleared or write 0 to clear it. Note: In anything other than an Isochronous transfer, this bit will always return to 0. Write 0 to clear it.
7	CLRDTATOG	**The CPU writes 1 to this bit to reset the endpoint data toggle to 0.**
6	SENTSTALL	**This bit is set when a STALL handshake is transmitted.** Cleared by CPU. An interrupt will be generated when the bit is set. Write 0 to clear it.
5	SENDSTALL	**The CPU writes 1 to this bit to issue a STALL handshake.** The CPU clears this bit to terminate the stall condition. *Note: This bit has no effect where the endpoint is used for ISO transfers.*
4	FLUSHFIFO	**The CPU writes 1 to this bit to flush the next packet to be read from the endpoint RxFIFO.** The RxFIFO pointer is reset and the RxPktRdy bit is cleared. *Note: FlushFIFO should only be used when RxPktRdy is set. In other cases, it may cause data corruption. If RxFIFO is double buffered, FlushFIFO may need to be set twice to completely clear RxFIFO.*
3	DATAERR	**This bit is set when RxPktRdy is set if the data packet has a CRC or bit-stuff error. It is cleared when RxPktRdy is cleared.** *Note: This bit is only valid when the endpoint is operating in ISO mode. In bulk mode, it always returns to 0.*
2	OVERRUN	**This bit is set if an OUT packet cannot be loaded into the RxFIFO. Cleared by CPU (write 0 to clear it).** *Note: This bit is only valid when the endpoint is operating in ISO mode. In bulk mode, it always returns to 0. The new incoming packet will not be written to RxFIFO. Write 0 to clear it.*
1	FIFOFULL	**Set when no more packets can be loaded into RxFIFO.**
0	RXPKTRDY	**Set when a data packet has been received (to RxFIFO)** The CPU clears this bit when the packet has been unloaded from the RxFIFO. An interrupt will be generated when the bit is set. Write 0 to clear it.

11200016 RXCSR_HOST RX CSR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOCLEAR	AUTOREQ	DMAREQENAB	PIDERROR	DMAREQMODE	SETREQPKT_TWICE	KEEPERRSTATUS	INCOMPRX	CLRDATATOG	RXSTALL	REQPKT	FLUSHFIFO	DATAERR_NAKTIMEOUT	ERROR	FIFOFULL	RXPKTRDY
Type	RW	RW	RW	RU	RW	A1	RW	A1	A0	A1	RW	A0	A1	A1	RU	A1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUTOCLEAR	**If CPU sets up this bit then the RxPktRdy bit will be automatically cleared when a packet of RxMaxP bytes has been unloaded from the RxFIFO.** When packets of less than the maximum packet size are unloaded, RxPktRdy will have to be cleared manually. *Note: The maximum packet size -3, -2, -1 is handled like the maximum packet size which is auto cleared by HW.*
14	AUTOREQ	**If CPU sets up this bit, the ReqPkt bit will be automatically set when the RxPktRdy bit is cleared.** *Note: This bit is automatically cleared when a short packet is received.*
13	DMAREQENAB	**The CPU sets up this bit to enable the DMA request for the RX endpoint.**
12	PIDERROR	**ISO transactions only: The core sets up this bit to indicate a PID error in the received packet.** Bulk/Interrupt transactions: The setting of this bit is ignored. Write 0 to clear it. Note: This register is read only in ISO mode but reserved for read/write access in other modes.
11	DMAREQMODE	**The CPU sets up this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0.** DMA Request Mode 1: RX endpoint interrupt is generated only when DMA Request Mode 1 and received a short packet. RxDMAReq is generated when receiving a Max-Packet-size packet. DMA Request Mode 0: No RX endpoint interrupt. RxDMAReq is generated when RxPktRdy is set.
10	SETREQPKT_TWICE	**Indicates the ReqPkt had been set when it is 1 already** Write 0 to clear it.
9	KEEPERRSTATUS	**Used when endpoint works with USBQ and in isochronous mode** When this bit is set, the isochronous error, PIDERROR, INCOMPRX and DATAERROR will be kept and only cleared by SW.
8	INCOMPRX	**This bit will be set in an isochronous transfer if the packet in RxFIFO is incomplete because part of the data are not received.** When KeepErrorStatus = 0, it is cleared when RxPktRdy is cleared or write 0 to clear it. *Note: In anything other than an isochronous transfer, this bit will always return to 0.*
7	CLRDATATOG	**The CPU writes 1 to this bit to reset the endpoint data toggle to 0.**
6	RXSTALL	**When a STALL handshake is received, this bit will be set and an interrupt generated.**

Bit(s)	Name	Description
		Cleared by CPU. Write 0 to clear it.
5	REQPKT	**The CPU writes 1 to this bit to request an IN transaction.** Cleared when RxPktRdy is set.
4	FLUSHFIFO	**The CPU writes 1 to this bit to flush the next packet to be read from the endpoint RxFIFO.** The RxFIFO pointer is reset and the RxPktRdy bit is cleared. *Note: FlushFIFO should only be used when RxPktRdy is set. In other cases, it may cause data corruption. If RxFIFO is double buffered, FlushFIFO may need to be set twice to completely clear RxFIFO.*
3	DATAERR_NAKTIMEOUT	**In bulk mode, this bit will be set when the RX endpoint is halted following the receipt of NAK responses for longer than the time set as the NAK Limit by the RxInterval register.** The CPU clears this bit to allow endpoint to continue. Write 0 to clear it. When operating in ISO mode, this bit is set when RxPktRdy is set if the data packet has a CRC or bit-stuff error and cleared when RxPktRdy is cleared.
2	ERROR	**The USB sets up this bit when 3 attempts have been made to receive a packet and no data packet has been received.** Cleared by CPU. An interrupt will be generated when the bit is set. *Note: This bit is only valid when the RX endpoint is operating in Bulk or Interrupt mode. Write 0 to clear it.* In ISO mode, it always returns to 0.
1	FIFOFULL	**Set when no more packets can be loaded into RxFIFO.**
0	RXPKTRDY	**Set when a data packet has been received (to RxFIFO).** The CPU clears this bit when the packet has been unloaded from the RxFIFO. An interrupt will be generated when the bit is set. Write 0 to clear it.

11200018 RXCOUNT RX Count Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RXCOUNT													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	RXCOUNT	**14-bit read-only register that holds the number of received data bytes in the packet in RxFIFO** *Note: The value returned changes as the FIFO is unloaded and is Only valid when RxPktRdy (RxCSR.D0) is set.*

1120001A TXTYPE TxType Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TX_SPEED		TX_PROTOCOL		TX_TARGET_EP_NUMBER			
Type									RW		RW		RW			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:6	TX_SPEED	**Operating speed of target device when core is configured with multipoint option** When the core is not configured with the multipoint option, these bits should not be accessed. 2'b00: Unused 2'b01: High 2'b10: Full 2'b11: Low
5:4	TX_PROTOCOL	**The CPU sets up this to select the required protocol for TX endpoint.** 2'b00: Illegal 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt
3:0	TX_TARGET_EP_NUMBER	**The CPU sets this value to the endpoint number contained in the TX endpoint descriptor returned to the USB2.0 Controller during device enumeration.**

1120001B TXINTERVAL TxInterval Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TX_POLLING_INTERVAL_NAK_LIMIT_M							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	TX_POLLING_INTERVAL_NAK_LIMIT_M	**(Host mode only) TxInterval Register TxInterval is an 8-bit register that, for Interrupt and Isochronous transfers, defines the polling interval for the currently-selected TX endpoint.** For Bulk endpoints, this register sets the number of frames/microframes after which the endpoint should timeout on receiving a stream of NAK responses. There is a TxInterval register for each configured TX endpoint (except for Endpoint 0). In each case the value that is set defines a number of frames/microframes (High Speed transfers), as follows: Transfer Type | Speed | Valid values (m) | Interpretation Interrupt | Low Speed or Full Speed | 1-255 | Polling interval is m frames. Interrupt | High Speed | 1-16 | Polling interval is 2^(m-1) microframes

Bit(s)	Name	Description
		Isochronous | Full Speed or High Speed | 1-16 | Polling interval is 2^(m-1) frames/microframes Bulk | Full Speed or High Speed | 2-16 | NAK Limit is 2^(m-1) frames/microframes. *Note: Value 0 or 1 disables the NAK timeout function.*

1120001C RXTYPE RxType Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RXSPEED		RX_PROTOCOL		RX_TARGET_EP_NUMBER			
Type									RW		RW		RW			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:6	RXSPEED	**Operating speed of target device when core is configured with multipoint option** When the core is not configured with the multipoint option, these bits should not be accessed. 2'b00: Unused 2'b01: High 2'b10: Full 2'b11: Low
5:4	RX_PROTOCOL	**The CPU sets up this to select the required protocol for TX endpoint.** 2'b00: Illegal 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt
3:0	RX_TARGET_EP_NUMBER	**The CPU sets this value to the endpoint number contained in the TX endpoint descriptor returned to the USB2.0 Controller during device enumeration.**

1120001D RXINTERVAL RxInterval Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_POLLING_INTERVAL_NAK_LIMIT_M							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_POLLING_INTERVAL_NAK_LIMIT_M	**RxInterval Register RxInterval is an 8-bit register that, for Interrupt and Isochronous transfers, defines the polling interval for the currently-selected**

Bit(s)	Name	Description
		RX endpoint. For Bulk endpoints, this register sets the number of frames/microframes after which the endpoint should timeout on receiving a stream of NAK responses. There is a RxInterval register for each configured RX endpoint (except for Endpoint 0). RX POLLING INTERVAL/NAK LIMIT (M), (Host mode only) In each case the value that is set defines a number of frames/microframes (High Speed transfers), as follows: Transfer Type Speed Valid values (m) Interpretation Interrupt Low Speed or Full Speed 1 - 255 Polling interval is m frames. High Speed 1 - 16 Polling interval is 2(m-1) microframes Isochronous Full Speed or High Speed 1 - 16 Polling interval is 2(m-1) frames/microframes Bulk Full Speed or High Speed 2 - 16 NAK Limit is 2(m-1) frames/microframes. *Note: Value 0 or 1 disables the NAK timeout function.*

1120001F FIFOSIZE Configured FIFO Size Register 000000AA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RXFIFOSIZE				TXFIFOSIZE			
Type									DC				DC			
Reset									1	0	1	0	1	0	1	0

Bit(s)	Name	Description
7:4	RXFIFOSIZE	**Indicates RxFIFO size of 2^n bytes** Example: Value 10 means 2^10 = 1024 bytes.
3:0	TXFIFOSIZE	**Indicates TxFIFO size of 2^n bytes** Example: Value 10 means 2^10 = 1024 bytes.

11200020 FIFO0 USB Endpoint 0 FIFO Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_DATA															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_DATA															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FIFO_DATA	**The Endpoint FIFO Registers provides 16 addresses for CPU access to the FIFOs for each endpoint.** Writing to these addresses loads data into the TxFIFO for the corresponding endpoint. Reading from these addresses unloads

Bit(s)	Name	Description
		data from the RxFIFO for the corresponding endpoint. *Note:* *1. Transfers to and from FIFOs may be 8-bit, 16-bit or 32-bit as required, and any combination of access is allowed provided the data accessed is contiguous. However, all the transfers associated with one packet must be of the ame width so that the data is consistently byte-, word- or double-word-aligned. The last transfer may however contain fewer bytes than the previous transfers in order to complete an odd-byte or odd-word transfer. For DC/DTV projects, refer to the RISC_SIZE register to complete FIFO access.* *2. Depending on the size of the FIFO and the expected maximum packet size, the FIFOs support either single-packet or double-packet buffering. However, burst writing of multiple packets is not supported as flags need to be set after each packet is written.* *3. Following a STALL response or a Tx Strike Out error on Endpoint, the associated FIFO is completely flushed.* *(vi) Programmers don't use debug tools to monitor or read the FIFO region. The FIFO pointer will increase and cause unexpected error in MAC state machine.*

11200024 FIFO1 USB Endpoint 1 FIFO Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_DATA															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_DATA															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FIFO_DATA	**The Endpoint FIFO Registers provides 16 addresses for CPU access to the FIFOs for each endpoint.** Writing to these addresses loads data into the TxFIFO for the corresponding endpoint. Reading from these addresses unloads data from the RxFIFO for the corresponding endpoint. *Note:* *1. Transfers to and from FIFOs may be 8-bit, 16-bit or 32-bit as required, and any combination of access is allowed provided the data accessed is contiguous. However, all the transfers associated with one packet must be of the ame width so that the data is consistently byte-, word- or double-word-aligned. The last transfer may however contain fewer bytes than the previous transfers in order to complete an odd-byte or odd-word transfer. For DC/DTV projects, refer to the RISC_SIZE register to complete FIFO access.* *2. Depending on the size of the FIFO and the expected maximum packet size, the FIFOs support either single-packet or double-packet buffering. However, burst writing of multiple packets is not supported as flags need to be set after each packet is written.* *3. Following a STALL response or a Tx Strike Out error on Endpoint, the associated FIFO is completely flushed.* *(vi) Programmers don't use debug tools to monitor or read the FIFO region. The FIFO pointer will increase and cause unexpected error in MAC state machine.*

11200060 DEVCTL **Device Control Register** **00000080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									B_DEVICE	FSDEV	LSDEV	VBUS		HOSTMODE	HOSTREQ	SESSION
Type									RU	RU	RU	RU		RU	OTHER	OTHER
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	B_DEVICE	**This read-only bit indicates whether the USB2.0 controller is operating as the 'A' device or the 'B' device.** Only valid when a session is in progress. *Note: If the core is in Force_Host mode, this bit will indicate the state of the HOSTDISCON input signal from the PHY.* 1'b0: 'A' device 1'b1: 'B' device
6	FSDEV	**This read-only bit is set when a full-speed or high-speed device has been detected being connected to the port.** (High-speed devices are distinguished from full-speed by checking for high-speed chirps when the device is reset.) Only valid in host mode.
5	LSDEV	**This read-only bit is set when a low-speed device has been detected being connected to the port. Only valid in host mode.**
4:3	VBUS	**These read-only bits encode the current VBUS level; only available with OTG function enquipped; else the register value will be undefined.** 2'b00: Below SessionEnd 2'b01: Above SessionEnd, below AValid 2'b10: Above AValid, below VBusValid 2'b11: About VBusValid
2	HOSTMODE	**This read-only bit is set when the USB2.0 controller is acting as a host.**
1	HOSTREQ	**When set, the USB2.0 controller will initiate the Host Negotiation when Suspend mode is entered.** Cleared when Host Negotiation is completed ('B' device only).
0	SESSION	**When operating as an 'A' device, this bit is set or cleared by the CPU to start or end a session.** When operating as a 'B' device, this bit is set/cleared by the USB2.0 controller when a session starts/ends. It is also set by the CPU to initiate the Session Request Protocol. When the USB2.0 controller is in Suspend mode, the bit may be cleared by the CPU to perform a software disconnect. *Note: Clearing this bit when the core is not suspended will result in undefined behavior.*

11200061 PWRUPCNT **Power Up Counter Register** **0000000F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name													PWRUPCNT			
Type													RW			
Reset													1	1	1	1

Bit(s)	Name	Description
3:0	PWRUPCNT	**Power-up counter limit.** The power-up counter is used to count the K state duration during suspend and when it is timed out, the resume interrupt will be issued. The register should be configured according to AHB clock speed.

11200062 TXFIFOSZ TX FIFO Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TXDPB	TXSZ			
Type												RW	RW			
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	TXDPB	**Defines whether double-packet buffering supported for TxFIFO** 0: Support only single-packet buffering 1: Support double-packet buffering
3:0	TXSZ	**Maximum packet size to be allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission)** If TxDPB = 0, the FIFO will also be this size; if TxDPB = 1, the FIFO will be twice this size. TxSZ[3:0] Packet size (bytes) 4'b0000: 8 4'b0001: 16 4'b0010: 32 4'b0011: 64 4'b0100: 128 4'b0101: 256 4'b0110: 512 4'b0111: 1024 4'b1000: 2048 (single-packet buffering only) 4'b1001: 4096 (single-packet buffering only) Others: No support

11200063 RXFIFOSZ RX FIFO Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name												RXDPB	RXSZ			
Type												RW	RW			
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	RXDPB	**Defines whether double-packet buffering supported for TxFIFO** 0: Support only single-packet buffering 1: Support double-packet buffering
3:0	RXSZ	**Maximum packet size to be allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission)** If TxDPB = 0, the FIFO will also be this size; if TxDPB = 1, the FIFO will be twice this size RxSZ[3:0] Packet Size (bytes) 4'b0000: 8 4'b0001: 16 4'b0010: 32 4'b0011: 64 4'b0100: 128 4'b0101: 256 4'b0110: 512 4'b0111: 1024 4'b1000: 2048 (single-packet buffering only) 4'b1001: 4096 (single-packet buffering only) Others: No support

11200064 TXFIFOADD TX FIFO Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TXFIFOADD												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	TXFIFOADD	**TxFIFOadd is a 13-bit register which controls the start address of the selected TX endpoint FIFO.** TxFIFOadd[12:0] Start address 13'h0000: 0000 13'h0001: 0008 13'h0002: 0010 13'h1FFF: FFF8

11200066 RXFIFOADD RX FIFO Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DataErrIntrEn	OverRUNIntrEn		RXFIFOADD												
Type	RW	RW		RW												
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	DataErrIntrEn	**Enables data error interrupt** *Note: This bit is only valid when the endpoint is operating in ISO mode.*
14	OverRUNIntrEn	**Enales over run interrupt** *Note: this bit is only valid when the endpoint is operating in ISO mode.*
12:0	RXFIFOADD	**RxFIFOadd is a 13-bit register which controls the start address of the selected RX endpoint FIFO.** RxFIFOadd[12:0] Start address 13'h0000: 0000 13'h0001: 0008 13'h0002: 0010 13'h1FFF: FFF8

1120006C HWCAPS Hardware Capability Register 00006503

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QMU_SUPPORT	HUB_SUPPORT	USB20_SUPPORT	USB11_SUPPORT	MSTR_WRAP_INTFX		SLAVE_WRAP_INTFX				USB_VERSION_CODE					
Type	RO	RO	RO	RO	DC		DC				RO					
Reset	0	1	1	0	0	1	0	1			0	0	0	0	1	1

Bit(s)	Name	Description
15	QMU_SUPPORT	**Supports QMU feature**
14	HUB_SUPPORT	**Supports HUB feature**
13	USB20_SUPPORT	**Supports USB2.0 feature**
12	USB11_SUPPORT	**Supports USB1.1 feature**
11:10	MSTR_WRAP_INTFX	**Configures AHB master interface** 2'b00: Mentor AHB master interface 2'b01: Asynchronous AHB master interface 2'b10: Asynchronous AXI master interface 2'b11: Asynchronous DX DRAM master interface
9:8	SLAVE_WRAP_INTFX	**Configures AHB slave interface** 2'b00: Mentor AHB slave interface 2'b01: Asynchronous AHB master interface 2'b10: Asynchronous AXI master interface 2'b11: Asynchronous DX CPU slave interface
5:0	USB_VERSION_CODE	**USB hardware version code**

1120006E HWSVERS Version Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									USB_SUB_VERSION_CODE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	USB_SUB_VERSION_CODE	USB software version code

11200070 BUSPERF1 USB Bus Performance Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLRDMAREQEARLY_EN	SOFT_DEBOUNCE	ISO_ERR_CNT_EN	ISO_RTY_DIS		PREAMBLE_DELAY_EN	HOST_WAIT_EPo									
Type	RW	RW	RW	RW		RW	RW									
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	CLRDMAREQEARLY_EN	**If CLRDMAREQEARLY_EN = 1, DMAReq will be cleared when 8 bytes of data remain in FIFO for Rx, or TXMAXP-8 bytes will be loaded in FIFO for TX.** If CLRDMAREQEARLY_EN = 0, DMAReq will only be cleared when RX FIFO is read empty or TXMAXP loaded to TX FIFO.
14	SOFT_DEBOUNCE	**If soft_debounce=0, the debounce will be implemented by HW, i.e. 120ms will be the same as before.** If soft_debounce=1, after DP/DM is stable for 1ms, connection interrupt will be generated, and SW will determine how long the delay is for debounce. This bit only affects the debounce behavior when the cable starts connection but does not affect in HNP when the cable is connected.
13	ISO_ERR_CNT_EN	**Musbhdrc has different behavior with USB spec in HUB ISO mode.** When this bit is set, the Strike out mechanism of re-try failed will be engaged and complete the transaction.
12	ISO_RTY_DIS	**Musbhdrc has different behavior with USB spec in HUB ISO mode.** This bit disables the retry of CSplit @ SOF.
10	PREAMBLE_DELAY_EN	**Host mode only and downstream port connect to hub.** This bit enables the function of host delay to issue a preamble +ack packet after receving data from LS device about 3 LS bit time.
9:0	HOST_WAIT_EPo	**Host waiting time of Endpointo**

Bit(s)	Name	Description
		The written value defines the minimum cycles for controller to issue the next IN/OUT/PING token during idle state. 0: No wait. >0: In idle state, the controller must wait for at least exact cycles which are written before it issues the next IN/OUT/PING token. The cycle unit is as USB system clock cycle.

11200072 BUSPERF2 USB Bus Performance Register 2 0000C000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HSR_ISOICHK_DIS	HST_ISOOCHK_DIS	HOST_WAIT_EPX													
Type	RW	RW	RW													
Reset	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	HSR_ISOICHK_DIS	**Disables ISO Rx 0-packet in host mode** Optional disable selection for ISO Rx 0 packet
14	HST_ISOOCHK_DIS	**Disables ISO Tx 0-packet in host mode** Optional disable selection for ISO Rx 0 packet
13:0	HOST_WAIT_EPX	**Host Waiting Time of all Endpoints except Endpointo** The written value defines the minimum cycles for controller to issue the next IN/OUT/PING token during idle state. 0: No wait. >0: In idle state, the controller must wait for at least exact cycles which are written before it issues the next IN/OUT/PING token. The cycle unit is as USB system clock cycle.

11200074 BUSPERF3 USB Bus Performance Register 3 00000A48

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					VBUSERR_MODE		FLUSH_FIFO_EN		NOISE_STILL_SOF	BAB_CLR_EN			UNDO_SRPFIX	OTG_DEGLITCH_DISABLE	EP_SWRST	DISUSBRESET
Type					RW		RW		RW	RW			RW	RW	Ao	RW
Reset					1		1		0	1			1	0	0	0

Bit(s)	Name	Description
11	VBUSERR_MODE	**Controls whether VBUS error will reset USB controller or only set up the VBUS error bit**

Bit(s)	Name	Description
		1'b0: Set INTRUSB.bit[7] VBUS error only 1'b1: Reset USB controller and set up INTRUSB.bit[7] VBUS error tooDataErr interrupt enable. The DataErr status bit is in RxCSR[3] and should be written 0 to clear. TBD
9	FLUSH_FIFO_EN	**Enables Flush FIFO** 1'b1: Clear USBPtr0, USBPtr1 of EPx Tx by flush FIFO command. 1'b0: USBPtr0, USBPtr1 of EPx Tx cannot be cleared by flush FIFO command.
7	NOISE_STILL_SOF	**Force transmitting SOF as babble interrupt**
6	BAB_CLR_EN	**Controls babble session** 1'b0: Babble interrupt will not close session automatically. 1'b1: Babble interrupt will close session automatically.
3	UNDO_SRPFIX	**The CPU sets up this bit to recover to the original circuit of USB2.0 IP about SRP.**
2	OTG_DEGLITCH_DISABLE	**Set to 1 to disable deglitch circuit of OTG signal group VBUSVALID, AVALID and SESSEND.**
1	EP_SWRST	**SW can reset the USB MAC setting by setting this bit to 1. EP_SWRST will be cleared by HW automatically.** The MAC setting include function address, endpoint interrupt enable/status, endpoint state and EP TX/RX CSR.
0	DISUSBRESET	**If DISUSBRESET is 0, USB MAC setting will be reset to unconfigured condition when USB bus reset is detected. SW can set this bit to 1 to disable USB MAC setting Reset by HW when USB bus reset is detected.** The HW reset MAC settings include: 1. Clear Function address register 2. Clear Index register 3. Flush all endpoint FIFO 4. Clear Control/status register a. EPN TX/RXMAXP b. EPN TX/RXCSR c. EPN TX/RXTYPE d. EPN TX/RXInterval e. EPN RXCOUNT f. EP0 CSR0 g. EP0 COUNT0 5. Enable TX/RX endpoint interrupt & Clear TX/RX interrupt status *Note: EPN TX/RX FIFOSZ/AD are not cleared.*

11200078 EPINFO **Number of TX and RX Register** **00000088**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RXENDPOINTS				TXENDPOINTS			
Type									RO				RO			
Reset									1	0	0	0	1	0	0	0

Bit(s)	Name	Description
7:4	RXENDPOINTS	Number of RX endpoints implemented in the design
3:0	TXENDPOINTS	Number of TX endpoints implemented in the design

11200079 RAMINFO **Width of RAM and Number of DMA Channel Register** **0000001B**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DMACHANS				RAMBITS			
Type									RO				DC			
Reset									0	0	0	1	1	0	1	1

Bit(s)	Name	Description
7:4	DMACHANS	Number of DMA channels implemented in the design
3:0	RAMBITS	Width of the RAM address bus-1

1120007A LINKINFO **Delay to be Applied Register** **0000005C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									WTCON				WTID			
Type									RW				RW			
Reset									0	1	0	1	1	1	0	0

Bit(s)	Name	Description
7:4	WTCON	**Sets up the wait to be applied to allow for the user's connect/disconnect filter in units of 533.3ns.** (The default setting corresponds to 2.667us.) The default value will change to be 4'h8 to meet 2.667us.
3:0	WTID	**Sets up delay to be applied from IDPULLUP being asserted to IDDIG being considered valid in units of 4.369ms.** (The default setting corresponds to 52.43ms.)

1120007B VPLEN **Vbus Pulsing Charge Register** **0000003C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									VPLEN							
Type									RW							
Reset									0	0	1	1	1	1	0	0

Bit(s)	Name	Description
7:0	VPLEN	**Sets up duration of the VBus pulsing charge in units of 136.5us.**

Bit(s)	Name	Description
		(The default setting corresponds to 8.19ms.)

1120007C HS_EOF1 **Time Buffer Available on HS Transaction Register** **00000080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									HS_EOF1							
Type									RW							
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	HS_EOF1	**Sets up high-speed transactions the time before EOF to stop beginning new transactions, in units of 133.3ns.** The default setting corresponds to 17.07us. USB2.0 IP only.

1120007D FS_EOF1 **Time Buffer Available on FS Transaction Register** **00000077**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FS_EOF1							
Type									RW							
Reset									0	1	1	1	0	1	1	1

Bit(s)	Name	Description
7:0	FS_EOF1	**Sets up full-speed transactions the time before EOF to stop beginning new transactions, in units of 533.3ns.** (The default setting corresponds to 63.46us.) The default value will change to be 8'hBE to meet 63.46us.

1120007E LS_EOF1 **Time Buffer Available on LS Transaction Register** **00000072**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LS_EOF1							
Type									RW							
Reset									0	1	1	1	0	0	1	0

Bit(s)	Name	Description
7:0	LS_EOF1	**Sets up Q252low-speed transactions the time before EOF to stop beginning new transactions, in units of 1.067us.** (The default setting corresponds to 121.6us.). USB2.0 IP only. The default value will change to be 8'hB6 to meet 121.6us.

1120007F RST_INFO Reset Information Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									WTFSSE0				WTCHRP			
Type									RW				RW			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:4	WTFSSE0	**Signifies the SE0 signal duration before issuing the reset signal(for Device only).** Duration = 272.8 x WTFSSE0 + 2.5 usec. This register will only be reset when hardware is reset.
3:0	WTCHRP	**Sets up delay to be applied from detecting Reset to sending chirp K (for Device only).** The duration = 272.8 x WTCHRP + 0.1 usec. This register will only be reset when hardware is reset.

11200080 RXTOG Rx Data Toggle Set/Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															EP1RXTOG	
Type															OTHER	
Reset															0	

Bit(s)	Name	Description
1	EP1RXTOG	**Receive Logical Endpoint n Data Toggle Bit Set/Status** When read, these bits indicate the current state of the Endpoint n data toggle. If enable bit is high, the bit may be written with the required setting of the data toggle. If enable is low, any value written is ignored Note: This register is word access. 1'b0: Logical Endpoint n RX data toggle bit = 0 1'b1: Logical Endpoint n RX data toggle bit = 1

11200082 RXTOGEN Rx Data Toggle Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															EP1RXTOGEN	
Type															RW	
Reset															0	

Bit(s)	Name	Description
1	EP1RXTOGEN	**Enables Receive Logical Endpoint n Data Toggle Bit** If enable bit is set, the endpoint n data toggle can be set. *Note: This register is word access.* 1'b0: Forbid RISC writing EP n data toggle status with EP1RXTOG 1'b1: Allow RISC writing EP n data toggle status with EP1RXTOG

11200084 TXTOG **Tx Data Toggle Set/Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															EP1TXTOG	
Type															OTHER	
Reset															0	

Bit(s)	Name	Description
1	EP1TXTOG	**Transmit Logical Endpoint n Data Toggle Bit Set/Status** When read, these bits indicate the current state of the Endpoint n data toggle. If enable bit is high, the bit may be written with the required setting of the data toggle. If enable is low, any value written is ignored *Note: This register is word access.* 1'b0: Logical Endpoint n TX data toggle bit = 0 1'b1: Logical Endpoint n TX data toggle bit = 1

11200086 TXTOGEN **Tx Data Toggle Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															EP1TXTOGEN	
Type															RW	
Reset															0	

Bit(s)	Name	Description
1	EP1TXTOGEN	**Enables Receive Logical Endpoint 1 Data Toggle Bit** If enable bit is set, the endpoint n data toggle can be set. *Note: This register is word access.* 1'b0: Forbid RISC writing EP n data toggle status with EP1RXTOG 1'b1: Allow RISC writing EP n data toggle status with EP1RXTOG

112000A0 USB_L1INTS **USB Level 1 Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					POWERDWN_INT_STATUS	DRVVBUS_INT_STATUS	IDDIG_INT_STATUS	VBUSVALID_INT_STATUS	DPDM_INT_STATUS	QHIF_INT_STATUS	QINT_STATUS	PSR_INT_STATUS	DMA_INT_STATUS	USBCOM_INT_STATUS	RX_INT_STATUS	TX_INT_STATUS
Type					RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	POWERDWN_INT_STATUS	**Power-down interrupt status** When controller is in host suspend mode, VBus is valid, and DP is asserted, this bit will set. When controller is In peripheral mode, Avalid is setting, and DP is asserted, this bit will set. When controller is in idle state, avalid is de-asserted , and linestate is in SE0, this bit will also set.
10	DRVVBUS_INT_STATUS	**DRVVBUS interrupt status** This bit shows the interrupt trigger status of DRVVBUS. The trigger polarity is determined by DRVVBUS_INT_POL. This interrupt is used in USB OTG charge pump control.
9	IDDIG_INT_STATUS	**IDDIG interrupt status** This bit shows the interrupt trigger status of IDDIG. The trigger polarity is determined by IDDIG_INT_POL. This interrupt is used in USB OTG attachment.
8	VBUSVALID_INT_STATUS	**VBUSVALID interrupt status** This bit shows the interrupt trigger status of VBUSVALID. The trigger polarity is determined by VBUSVALID_INT_POL. This interrupt is used in USB attachment to host.
7	DPDM_INT_STATUS	**DPDM interrupt status** This bit shows the interrupt trigger status of DPDM. The trigger condition is whether DP or DM goes high. This interrupt is used in USB HOST mode to detect device attachment.
6	QHIF_INT_STATUS	**USBQ HIF command interrupt status** Only valid when WiMAX Q is available.
5	QINT_STATUS	**USBQ interrupt status** Only valid when USBQ is available.
4	PSR_INT_STATUS	**Packet sequence recorder interrupt status**
3	DMA_INT_STATUS	**DMA interrupt status**
2	USBCOM_INT_STATUS	**USB common interrupt status**
1	RX_INT_STATUS	**Endpoint RX interrupt status**
0	TX_INT_STATUS	**Endpoint TX interrupt status**

Bit(s)	Name	Description

112000A4 USB_L1INTM **USB Level 1 Interrupt Mask Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					POWERDWN_INT_UNMASK	DRVVBUS_INT_UNMASK	IDDIG_INT_UNMASK	VBUSVALID_INT_UNMASK	DPDM_INT_UNMASK	QHIF_INT_UNMASK	QINT_UNMASK	PSR_INT_UNMASK	DMA_INT_UNMASK	USBCOM_INT_UNMASK	RX_INT_UNMASK	TX_INT_UNMASK
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	POWERDWN_INT_UNMASK	**Unmasks POWERDWN interrupt** 1'b0: Mask interrupt 1'b1: Unmask interrupt
10	DRVVBUS_INT_UNMASK	**Unmasks DRVVBUS interrupt** 1'b0: Mask interrupt 1'b1: Unmask interrupt
9	IDDIG_INT_UNMASK	**Unmasks IDDIG interrupt** 1'b0: Mask interrupt 1'b1: Unmask interrupt
8	VBUSVALID_INT_UNMASK	**Unmasks VBUSVALID interrupt** 1'b0: Mask interrupt 1'b1: Unmask interrupt
7	DPDM_INT_UNMASK	**Unmasks DPDM interrupt** 1'b0: Mask interrupt 1'b1: Unmask interrupt
6	QHIF_INT_UNMASK	**Unmasks USBQ HIF command interrupt** Only valid when WiMAX Q is available. 1'b0: Mask interrupt 1'b1: Unmask interrupt
5	QINT_UNMASK	**Unmasks USBQ interrupt** Only valid when USBQ is available. 1'b0: Mask interrupt 1'b1: Unmask interrupt
4	PSR_INT_UNMASK	**Unmasks packet sequence recorder interrupt** 1'b0: Mask interrupt 1'b1: Unmask interrupt
3	DMA_INT_UNMASK	**Unmasks DMA interrupt** 1'b0: Mask interrupt 1'b1: Unmask interrupt
2	USBCOM_INT_UNMASK	**Unmasks USB common interrupt** 1'b0: Mask interrupt 1'b1: Unmask interrupt
1	RX_INT_UNMASK	**Unmasks endpoint RX interrupt** 1'b0: Mask interrupt 1'b1: Unmask interrupt
0	TX_INT_UNMASK	**Unmasks endpoint TX interrupt** 1'b0: Mask interrupt

Bit(s)	Name	Description
		1'b1: Unmask interrupt

112000A8 USB_L1INTP **USB Level 1 Interrupt Polarity Register** **00000200**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					POWERDWN_INT_POL	DRVVBUS_INT_POL	IDDIG_INT_POL	VBUSVALID_INT_POL								
Type					RW	RW	RW	RW								
Reset					0	0	1	0								

Bit(s)	Name	Description
11	POWERDWN_INT_POL	**POWERDWN interrupt polarity** 1'b0: Interrupt trigger when POWERDWN is 1. 1'b1: Interrupt trigger when POWERDWN is 0.
10	DRVVBUS_INT_POL	**DRVVBUS interrupt polarity** 1'b0: Interrupt trigger when DRVVBUS is 1. 1'b1: Interrupt trigger when DRVVBUS is 0.
9	IDDIG_INT_POL	**IDDIG interrupt polarity** 1'b0: Interrupt trigger when IDDIG is 1. 1'b1: Interrupt trigger when IDDIG is 0.
8	VBUSVALID_INT_POL	**VBUSVALID interrupt polarity** 1'b0: Interrupt trigger when VBUSVALID is 1. 1'b1: Interrupt trigger when VBUSVALID is 0.

112000AC USB_L1INTC **USB Level 1 Interrupt Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																USB_INT_SYNC
Type																RW
Reset																0

Bit(s)	Name	Description
0	USB_INT_SYNC	**USB interrupt synchronization** 1'b0: USB output interrupt is output directly. 1'b1: USB output interrupt is synchronized by MCU BUS clock registers.

11200102 CSR0_PERI EP0 Control Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**FLUSHFIFO**	**SERVICESETUPEDN**	**SERVICEDRXPKTRDY**	**SENDSTALL**	**SETUPEND**	**DATAEND**	**SENTSTALL**	**TXPKTRDY**	**RXPKTRDY**
Type								A0	A0	A0	A0	RU	A0	RW	A0	RU
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	FLUSHFIFO	**The CPU writes 1 to this bit to flush the next packet to be transmitted/read from the Endpoint 0 FIFO.** It is cleared automatically. The FIFO pointer is reset and the TxPktRdy/RxPktRdy bit (below) is cleared. May be set simultaneously with TxPktRdy to abort the packet that is currently being loaded into the FIFO. *Note: FlushFIFO should only be used when TxPktRdy/RxPktRdy is set. In other cases, it may cause data corruption.*
7	SERVICESETUPEDN	**The CPU writes 1 to this bit to clear the SetupEnd bit.** It is cleared automatically.
6	SERVICEDRXPKTRDY	**The CPU writes 1 to this bit to clear the RxPktRdy bit.** It is cleared automatically.
5	SENDSTALL	**The CPU writes 1 to this bit to terminate the current transaction.** The STALL handshake will be transmitted and then this bit will be cleared automatically. *Note: The FIFO should be flushed before SendStall is set.*
4	SETUPEND	**This bit will be set when a control transaction ends before the DataEnd bit has been set.** An interrupt will be generated and the FIFO flushed at this time. The bit is cleared by the CPU writing 1 to the ServicedSetupEnd bit.
3	DATAEND	**The CPU sets up this bit: When setting TxPktRdy for the last data packet.** When clearing RxPktRdy after unloading the last data packet. When setting TxPktRdy for a 0 length data packet. It is cleared automatically.
2	SENTSTALL	**This bit is set when a STALL handshake is transmitted. Cleared by CPU.** Write 0 to clear it.
1	TXPKTRDY	**The CPU sets up this bit after loading a data packet into FIFO.** It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled).
0	RXPKTRDY	**This bit is set when a data packet has been received.** An interrupt is generated when this bit is set. The CPU clears this bit by setting up the ServicedRxPktRdy bit.

11200102 CSR0_HOST EP0 Control Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DISPING			FLUSHFIFO	NAKTIMEOUT	STATUSPKT	REQPKT	ERROR	SETUPPKT	RXSTALL	TXPKTRDY	RXPKTRDY
Type					RW			A0	A1	RW	RW	A1	A1	A1	A0	A1
Reset					0			0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	DISPING	**The CPU writes 1 to this bit to disable transmitting PING token.** This bit can be set together with TXPKTRDY. To clear DISPING function, SW can write 0 after each control transfer is done. The DisPing function will be cleared when the next SETUP transaction is finished or OUT transaction receive handshake token with NAK/NYET/Timeout. Read "1" only in USB11 Configuration. Token PING is not supported in FS mode. USB2.0 IP for TX only.
8	FLUSHFIFO	**The CPU writes 1 to this bit to flush the next packet to be transmitted/read from the Endpoint 0 FIFO.** It is cleared automatically. The FIFO pointer is reset and the TxPktRdy/RxPktRdy bit (below) is cleared. May be set simultaneously with TxPktRdy to abort the packet that is currently being loaded into the FIFO. *Note: FlushFIFO should only be used when TxPktRdy/RxPktRdy is set. In other cases, it may cause data corruption.*
7	NAKTIMEOUT	**This bit will be set when Endpoint 0 is halted following the receipt of NAK responses for longer than the time set by the NAKLimit0 register.** The CPU clears this bit to allow the endpoint to continue. Write 0 to clear it.
6	STATUSPKT	**The CPU sets up this bit at the same time as the TxPktRdy or ReqPkt bit is set, to perform a status stage transaction.** Setting up this bit ensures that the data toggle is set to 1 so that a DATA1 packet is used for the Status Stage transaction.
5	REQPKT	**The CPU writes 1 to this bit to request an IN transaction.** Cleared when RxPktRdy is set.
4	ERROR	**This bit will be set when three attempts have been made to perform a transaction with no response from the peripheral.** Cleared by CPU. An interrupt is generated when this bit is set. Write 0 to clear it.
3	SETUPPKT	**The CPU sets up this bit, at the same time as the TxPktRdy bit is set, to send a SETUP token instead of an OUT token for the transaction.** This bit will be automatically clear by HW when setup packet is transmitted. *Note: Setting this bit also clears the DataToggle.*
2	RXSTALL	**This bit is set when a STALL handshake is received.** Cleared by CPU. Write 0 to clear it.
1	TXPKTRDY	**The CPU sets up this bit after loading a data packet into FIFO.** It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled).
0	RXPKTRDY	**This bit is set when a data packet has been received.** An interrupt is generated when this bit is set. The CPU clears this bit by setting up the ServicedRxPktRdy bit. Write 0 to clear it.

11200108 COUNT0 EP0 Received Bytes Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										EP0_RX_COUNT						
Type										RU						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	EP0_RX_COUNT	**Count0 is a 7-bit read-only register that indicates the number of received data bytes in the Endpoint 0 FIFO.** The value returned changes as the contents of the FIFO change and is Only valid when RxPktRdy (IDXEPR0.CSR0.bit0) is set.

1120010A TYPE0 EP0 Type Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EP0_ Type							
Type									RW							
Reset									0	0						

Bit(s)	Name	Description
7:6	EP0_Type	**Operating speed of target device when core is configured with multipoint option.** When the core is not configured with the multipoint option, these bits should not be accessed. 2'b00: Unused 2'b01: High 2'b10: Full 2'b11: Low

1120010B NAKLIMT0 NAK Limit Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												NAKLIMIT0				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
4:0	NAKLIMIT0	**(Host mode only) NAKLimit0 is a 5-bit register that sets the number of frames/microframes (high-speed transfers) after which Endpoint 0 should timeout on receiving a stream of NAK responses.** (Equivalent settings for other endpoints can be made through their TxInterval and RxInterval registers.). The number of frames/microframes selected is 2(m-1) (where m is the value set in the register, valid values 2 - 16). If the host receives NAK responses from the target for more frames than the number represented by the Limit set in this register, the endpoint will be halted. *Note: Value 0 or 1 disables the NAK timeout function.*

1120010C SRAMCONFIGSIZE SRAM Size Register 00000800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRAM_SIZE															
Type	RO															
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SRAM_SIZE	**Depth of SRAM with data bus width 32 bits** For example, if the SRAM is configured to 8KB, SRAM_SIZE will be 16'h800.

1120010E HBCONFIGDATA High Bind-width Configuration Register 00000088

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									NUM_HB_EPR				NUM_HB_EPT			
Type									RO				RO			
Reset									1	0	0	0	1	0	0	0

Bit(s)	Name	Description
7:4	NUM_HB_EPR	Number of high bind-width RX endpoints
3:0	NUM_HB_EPT	Number of high bind-width TX endpoints

1120010F CONFIGDATA Core Configuration Register 0000001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MPRXE	MPTXE	BIGENDIAN	HBRXE	HBTXE	DYNFIFOSIZING	SOFTCONE	UTMIDATAWIDTH
Type									RO	RO	RO	RO	RO	RO	RO	RO
Reset									0	0	0	1	1	1	1	1

Bit(s)	Name	Description
7	MPRXE	**When set to 1, automatic amalgamation of bulk packets will be selected.**
6	MPTXE	**When set to 1, automatic splitting of bulk packets will be selected.**
5	BIGENDIAN	**Set to 1 indicates Big Endian order will be selected.**
4	HBRXE	**Set to 1 indicates High-bandwidth Rx ISO Endpoint Support is selected.**
3	HBTXE	**Set to 1 indicates High-bandwidth Tx ISO Endpoint Support is selected.**
2	DYNFIFOSIZING	**Set to 1 indicates Dynamic FIFO sizing option is selected.**
1	SOFTCONE	**Set to 1 indicates Soft Connect/Disconnect option is selected.**
0	UTMIDATAWIDTH	**Indicates selected UTMI+ data width** 1'b0: 8 bits 1'b1: 16 bits

11200110 TX1MAP TX1MAP Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				M1		MAXIMUM_PAYLOAD_TRANSACTION										
Type				RW		RW										
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:11	M1	**Maximum payload size for indexed TX endpoint, M1 Packet multiplier m maximum payload transaction register**
10:0	MAXIMUM_PAYLOAD_TRANSACTION	**The TxMaxP register defines the maximum amount of data that can be transferred through the selected TX endpoint in asingle operation. =** There is a TxMaxP register for each TX endpoint (except for Endpoint 0).Bits 10:0 define (in bytes) the maximum payload transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in full-speed and high-speed operations. Where the option of High-bandwidth Isochronous endpoints or of packet splitting on Bulk endpoints has been taken when the core is configured, the register includes either 2 or 5 further bits that define a multiplier m which is equal to one more than the value recorded. In the case of Bulk endpoints with the packet

Bit(s)	Name	Description
		splitting option enabled, the multiplier m can be up to 32 and defines the maximum number of 'USB' packets (i.e. packets for transmission over the USB) of the specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. (If the packet splitting option is not enabled, bit15-13 will not be implemented and bit12-11 (if included) will be ignored.) Note: The data packet is required to be an exact multiple of the payload specified by bits 10:0, which is itself required to be either 8, 16, 32, 64 or (in the case of high-speed transfers) 512 bytes. for isochronous endpoints operating in high-speed mode and with the high-bandwidth option enabled, m may only be either 2 or 3 (corresponding to bit 11 set or bit 12 set, respectively) and it specifies the maximum number of such transactions that can take place in a single microframe. If either bit 11 or bit 12 is non-0, the USB2.0 controller will automatically split any data packet written to the FIFO into up to 2 or 3 'USB' packets, each containing the specified payload (or less). The maximum payload for each transaction is 1024 bytes, so this allows up to 3072 bytes to be transmitted in each microframe. (For Isochronous/Interrupt transfers in Full-speed mod, bits 11 and 12 are ignored.) The value written to bits 10:0 (multiplied by m in the case of high-bandwidth Isochronous transfers) must match the value given in the wMaxPacketSize field of the Standard Endpoint Descriptor for the associated endpoint . A mismatch can cause unexpected results. The total amount of data represented by the value written to this register (specified payload * m) must not exceed the FIFO size for the TX endpoint and should not exceed half the FIFO size if double-buffering is required. If this register is changed after packets have been sent from the endpoint, the TX endpoint FIFO should be completely flushed (using the FlushFIFO bit in TxCSR) after writing the new value to this register.

11200112 TX1CSR_PERI Tx1 CSR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOSET	ISO		DMAREQEN	FRCDATATOG	DMAREQMODE		SETTXPKTRDY_TWICE	INCOMPTX	CLRDATATOG	SENTSTALL	SENDSTALL	FLUSHFIFO	UNDERRUN	FIFONOTEMPTY	TXPKTRDY
Type	RW	RW		RW	RW	RW		A1	A1	A0	A1	RW	A0	A1	RU	A0
Reset	0	0		0	0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUTOSET	**If The CPU sets up this bit, TxPktRdy will be automatically set when data of the maximum packet size (value in TxMaxP) is loaded into the TxFIFO.** If a packet of less than the maximum packet size is loaded,

Bit(s)	Name	Description
		TxPktRdy will have to be set manually.
14	ISO	**The CPU sets up this bit to enable the TX endpoint for isochronous transfers and clears it to enable the TX endpoint for bulk or interrupt transfers.** Note: This bit only has any effect In peripheral mode. In host mode, it always returns to 0.
12	DMAREQEN	**The CPU sets up this bit to enable the DMA request for the TX endpoint.**
11	FRCDATATOG	**The CPU sets up this bit to force the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received.** This can be used by Interrupt TX endpoints that are used to communicate rate feedback for isochronous endpoints.
10	DMAREQMODE	**The CPU sets up this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0.** *Note: This bit must not be cleared either before or in the same cycle as the DMAReqEn bit is cleared.*
8	SETTXPKTRDY_TWICE	**Indicates TxPktRdy had been set when it is 1'b1 already Write 0 to clear it.**
7	INCOMPTX	**When the endpoint is used for high-bandwidth isochronous/interrupt transfers, this bit is set to indicate where a large packet has been split into 2 or 3 packets for transmission but insufficient IN tokens have been received to send all the parts.** *Note: In anything other than a high-bandwidth transfer, this bit will always return to 0. Write 0 to clear it.*
6	CLRDATATOG	**The CPU writes 1 to this bit to reset the endpoint data toggle to 0.**
5	SENTSTALL	**This bit is set when a STALL handshake is transmitted.** The FIFO is flushed, TX interrupt is generated if enabled and the TxPktRdy bit is cleared. Cleared by CPU. Write 0 to clear it.
4	SENDSTALL	**The CPU writes 1 to this bit to issue a STALL handshake to an IN token.** The CPU clears this bit to terminate the stall condition. *Note: This bit has no effect where the endpoint is used for isochronous transfer. Otherwise, CPU should wait for SENTSTALL interrupt being generated before clearing the SENDSTALL bit.*
3	FLUSHFIFO	**The CPU writes 1 to this bit to flush the latest packet from the endpoint TxFIFO.** The FIFO pointer is reset, the TxPktRdy bit is cleared and an interrupt is generated. May be set simultaneously with TxPktRdy to abort the packet that is currently being loaded into the FIFO. *Note: FlushFIFO should only be used when TxPktRdy is set. In other cases, it may cause data corruption. If the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.*
2	UNDERRUN	**The USB sets up this bit if an IN token is received when the TxPktRdy bit not set.** Cleared by CPU (write 0 to clear it).
1	FIFONOTEMPTY	**The USB sets up this bit when there is at least 1 packet in TxFIFO.** This bit will be asserted automatically when TXPKTRDY is set by CPU and de-asserted when CPU flushes FIFO or sends a STALL packet.
0	TXPKTRDY	**The CPU sets up this bit after loading a data packet into FIFO.** It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled). TxPktRdy is also automatically cleared (interrupt is generated) prior to loading a second packet into a double-buffered

Bit(s)	Name	Description
		FIFO.

11200112 TX1CSR_HOST Tx1 CSR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOSET			DMAREQEN	FRCDATATOG	DMAREQMODE		SETTXPKTRDY_TWICE	NAKTIMEOUT_INCOMPTX	CLRDATAOG	RXSTALL		FLUSHFIFO	ERROR	FIFONOTEMPTY	TXPKTRDY
Type	RW			RW	RW	RW		A1	A1	A0	A1		A0	A1	RU	A0
Reset	0			0	0	0		0	0	0	0		0	0	0	0

Bit(s)	Name	Description
15	AUTOSET	**If The CPU sets up this bit, TxPktRdy will be automatically set when data of the maximum packet size (value in TxMaxP) is loaded into the TxFIFO.** If a packet of less than the maximum packet size is loaded, TxPktRdy will have to be set manually.
12	DMAREQEN	**The CPU sets up this bit to enable the DMA request for the TX endpoint.**
11	FRCDATATOG	**The CPU sets up this bit to force the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received.** This can be used by Interrupt TX endpoints that are used to communicate rate feedback for isochronous endpoints.
10	DMAREQMODE	**The CPU sets up this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0.** *Note: This bit must not be cleared either before or in the same cycle as the DMAReqEn bit is cleared.*
8	SETTXPKTRDY_TWICE	**Indicates TxPktRdy had been set when it is 1'b1 already** Write 0 to clear it.
7	NAKTIMEOUT_INCOMPTX	**Bulk endpoints only: This bit will be set when the TX endpoint is halted following the receipt of NAK responses for longer than the time set as the NAK Limit by the TxInterval register.** The CPU clears this bit to allow the endpoint to continue. Write 0 to clear it.
6	CLRDATAOG	**The CPU writes 1 to this bit to reset the endpoint data toggle to 0.**
5	RXSTALL	**This bit is set when a STALL handshake is received.** When this bit is set, any DMA request that is in progress is topped, the FIFO is completely flushed, TX interrupt is generated if enabled and the TxPktRdy bit is cleared (see below). Cleared by CPU. Write 0 to clear it.
3	FLUSHFIFO	**The CPU writes 1 to this bit to flush the latest packet from the endpoint TxFIFO.** The FIFO pointer is reset, the TxPktRdy bit is cleared and an interrupt is generated. May be set simultaneously with TxPktRdy to abort the packet that is currently being loaded into the FIFO. *Note: FlushFIFO should only be used when TxPktRdy is set. In*

Bit(s)	Name	Description
		other cases, it may cause data corruption. If the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.
2	ERROR	**The USB sets up this bit when 3 attempts have been made to send a packet and no handshake packet has been received.** When the bit is set, an interrupt will be generated, TxPktRdy cleared and FIFO completely flushed. Cleared by CPU. Valid only when the endpoint is operating in Bulk or Interrupt mode. Write 0 to clear it.
1	FIFONOTEMPTY	**The USB sets up this bit when there is at least 1 packet in TxFIFO.** This bit will be asserted automatically when TXPKTRDY is set by CPU and de-asserted when CPU flushes FIFO or sends a STALL packet.
0	TXPKTRDY	**The CPU sets up this bit after loading a data packet into FIFO.** It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled). TxPktRdy is also automatically cleared (interrupt is generated) prior to loading a second packet into a double-buffered FIFO.

11200114 RX1MAP RX1MAP Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				M1		MAXIMUM_PAYLOAD_TRANSACTION										
Type				RW		RW										
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:11	M1	**Maximum payload size for indexed RX endpoint, M1 Packet multiplier m**
10:0	MAXIMUM_PAYLOAD_TRANSACTION	**The RxMaxP register defines the maximum amount of data that can be transferred through the selected RX endpoint in a single operation.** There is a RxMaxP register for each RX endpoint (except for Endpoint 0). Bits 10:0 define (in bytes) the maximum payload transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-speed and High-speed operations. Where the option of High-bandwidth Isochronous endpoints or of combining Bulk packets has been taken when the core is configured, the register includes either 2 or 5 further bits that define a multiplier m which is equal to one more than the value recorded. For Bulk endpoints with the packet combining option enabled, the multiplier m can be up to 32 and defines the number of USB packets of the specified payload which are to be combined into a single data packet within the FIFO. (If the packet splitting option is not enabled, bit15-bit13 is not

Bit(s)	Name	Description
		implemented and bit12-bit11 (if included) is ignored.) for isochronous endpoints operating in high-speed mode and with the high-bandwidth option enabled, m may only be either 2 or 3 (corresponding to bit 11 set or bit 12 set, respectively) and it specifies the maximum number of such transactions that can take place in a single microframe. If either bit 11 or bit 12 is non-0, the USB2.0 controller will automatically combine the separate USB packets received in any microframe into a single packet within the RX FIFO. The maximum payload for each transaction is 1024 bytes, so this allows up to 3072 bytes to be received in each microframe. (For Isochronous/Interrupt transfers in full-speed mode or if High-bandwidth is not enabled, bits 11 and 12 are ignored.) The value written to bits 10:0 (multiplied by m in the case of high-bandwidth Isochronous transfers) must match the value given in the wMaxPacketSize field of the Standard Endpoint Descriptor for the associated endpoint . A mismatch can cause unexpected results. The total amount of data represented by the value written to this register (specified payload * m) must not exceed the FIFO size for the OUT endpoint and should not exceed half the FIFO size if double-buffering is required.

11200116 RX1CSR_PERI RX1 CSR Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOCLEAR	ISO	DMAREQEN	DISNYET_PIDERR	DMAREQMODE		KEEPERRSTATUS	INCOMPRX	CLRDATOG	SENTSTALL	SENDSTALL	FLUSHFIFO	DATAERR	OVERRUN	FIFOFULL	RXPKTRDY
Type	RW	RW	RW	RW	RW		RW	A1	A0	A1	RW	A0	RU	A1	RU	A1
Reset	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUTOCLEAR	**If CPU sets up this bit then the RxPktRdy bit will be automatically cleared when a packet of RxMaxP bytes has been unloaded from the RxFIFO.** When packets of less than the maximum packet size are unloaded, RxPktRdy will have to be cleared manually. *Note: The maximum packet size -3, -2, -1 is handled like the maximum packet size which is auto cleared by HW.*
14	ISO	**The CPU sets up this bit to enable the RX endpoint for isochronous transfers and clears it to enable the RX endpoint for bulk/interrupt transfers.**
13	DMAREQEN	**The CPU sets up this bit to enable the DMA request for the RX endpoint.**
12	DISNYET_PIDERR	**The CPU sets up this bit to disable the sending of NYET handshakes. When set, all successfully received Rx packets are ACK'd including at the point at which the RxFIFO becomes full.** *Note: This bit only takes effect in high-speed mode in which it should be set for all interrupt endpoints.*

Bit(s)	Name	Description
		This bit is set when there is a PID error in the received packet. It is cleared when RxPktRdy is cleared or write 0 to clear it.
11	DMAREQMODE	**The CPU sets up this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0.** DMA Request Mode 1: RX endpoint interrupt is generated only when DMA Request Mode 1 and received a short packet. RxDMAReq is generated when receiving a Max-Packet-size packet.DMA Request Mode 0: No RX endpoint interrupt. RxDMAReq is generated when RxPktRdy is set.
9	KEEPERRSTATUS	**Used when endpoint works with USBQ and in isochronous mode** When this bit is set, the isochronous error, PIDERROR, INCOMPRX and DATAERROR will be kept and only cleared by SW.
8	INCOMPRX	**This bit will be set in an isochronous transfer if the packet in RxFIFO is incomplete because part of the data are not received.** When KeepErrorStatus = 0, it is cleared when RxPktRdy is cleared or write 0 to clear it. *Note: In anything other than an isochronous transfer, this bit will always return to 0. Write 0 to clear it.*
7	CLRDTATOG	**The CPU writes 1 to this bit to reset the endpoint data toggle to 0.**
6	SENTSTALL	**This bit is set when a STALL handshake is transmitted. Cleared by CPU. An interrupt will be generated when the bit is set.** Write 0 to clear it.
5	SENDSTALL	**The CPU writes 1 to this bit to issue a STALL handshake. The CPU clears this bit to terminate the stall condition.** *Note: This bit has no effect where the endpoint is used for ISO transfers.*
4	FLUSHFIFO	**The CPU writes 1 to this bit to flush the next packet to be read from the endpoint RxFIFO.** The RxFIFO pointer is reset and the RxPktRdy bit is cleared. *Note: FlushFIFO should only be used when RxPktRdy is set. In other cases, it may cause data corruption. If RxFIFO is double buffered, FlushFIFO may need to be set twice to completely clear RxFIFO.*
3	DATAERR	**This bit is set when RxPktRdy is set if the data packet has a CRC or bit-stuff error. It is cleared when RxPktRdy is cleared.** *Note: This bit is only valid when the endpoint is operating in ISO mode. In bulk mode, it always returns to 0.*
2	OVERRUN	**This bit is set if an OUT packet cannot be loaded into the RxFIFO. Cleared by CPU (write 0 to clear it).** *Note: This bit is only valid when the endpoint is operating in ISO mode. In bulk mode, it always returns to 0. The new incoming packet will not be written to RxFIFO.*
1	FIFOFULL	**Set when no more packets can be loaded into RxFIFO.**
0	RXPKTRDY	**Set when a data packet has been received (to RxFIFO)** The CPU clears this bit when the packet has been unloaded from the RxFIFO. An interrupt will be generated when the bit is set. Write 0 to clear it.

11200116 RX1CSR_HOST **Rx1 CSR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOCLEAR	AUTOREQ	DMAREQENAB	PIDERROR	DMAREQMODE	SETREQPKT_TWICE	KEEPERRSTATUS	INCOMPRX	CLRDATATOG	RXSTALL	REQPKT	FLUSHFIFO	DATAERR_NAKTIMEOUT	ERROR	FIFOFULL	RXPKTRDY
Type	RW	RW	RW	RU	RW	A1	RW	A1	A0	A1	RW	A0	A1	A1	RU	A1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUTOCLEAR	**If CPU sets up this bit then the RxPktRdy bit will be automatically cleared when a packet of RxMaxP bytes has been unloaded from the RxFIFO.** When packets of less than the maximum packet size are unloaded, RxPktRdy will have to be cleared manually. Note: The maximum packet size -3, -2, -1 is handled like the maximum packet size which is auto cleared by HW.
14	AUTOREQ	**If CPU sets up this bit, the ReqPkt bit will be automatically set when the RxPktRdy bit is cleared.** *Note: This bit is automatically cleared when a short packet is received.*
13	DMAREQENAB	**The CPU sets up this bit to enable the DMA request for the RX endpoint.**
12	PIDERROR	**ISO transactions only: The core sets up this bit to indicate a PID error in the received packet.** Bulk/Interrupt transactions: The setting of this bit is ignored. Write 0 to clear it. *Note: This register is read only in ISO mode but reserved for read/write access in other modes.*
11	DMAREQMODE	**The CPU sets up this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0.** DMA Request Mode 1: RX endpoint interrupt is generated only when DMA Request Mode 1 and received a short packet. RxDMAReq is generated when receiving a Max-Packet-size packet.DMA Request Mode 0: No RX endpoint interrupt. RxDMAReq is generated when RxPktRdy is set.
10	SETREQPKT_TWICE	**Indicates the ReqPkt had been set when it is 1 already** Write 0 to clear it.
9	KEEPERRSTATUS	**Used when endpoint works with USBQ and in isochronous mode** When this bit is set, the isochronous error, PIDERROR, INCOMPRX and DATAERROR will be kept and only cleared by SW.
8	INCOMPRX	**This bit will be set in an isochronous transfer if the packet in RxFIFO is incomplete because part of the data are not received.** When KeepErrorStatus = 0, it is cleared when RxPktRdy is cleared or write 0 to clear it. *Note: In anything other than an isochronous transfer, this bit will always return to 0.*
7	CLRDATATOG	**The CPU writes 1 to this bit to reset the endpoint data toggle to 0.**
6	RXSTALL	**When a STALL handshake is received, this bit will be set and an interrupt generated.** Cleared by CPU. Write 0 to clear it.
5	REQPKT	**The CPU writes 1 to this bit to request an IN transaction.** Cleared when RxPktRdy is set.
4	FLUSHFIFO	**The CPU writes 1 to this bit to flush the next packet to**

Bit(s)	Name	Description
		be read from the endpoint RxFIFO. The RxFIFO pointer is reset and the RxPktRdy bit is cleared. *Note: FlushFIFO should only be used when RxPktRdy is set. In other cases, it may cause data corruption. If RxFIFO is double buffered, FlushFIFO may need to be set twice to completely clear RxFIFO.*
3	DATAERR_NAKTIMEOUT	**In bulk mode, this bit will be set when the RX endpoint is halted following the receipt of NAK responses for longer than the time set as the NAK Limit by the RxInterval register.** The CPU clears this bit to allow endpoint to continue. Write 0 to clear it. When operating in ISO mode, this bit is set when RxPktRdy is set if the data packet has a CRC or bit-stuff error and cleared when RxPktRdy is cleared.
2	ERROR	**The USB sets up this bit when 3 attempts have been made to receive a packet and no data packet has been received.** Cleared by CPU. An interrupt will be generated when the bit is set. Note: This bit is only valid when the RX endpoint is operating in Bulk or Interrupt mode. In ISO mode, it always returns to 0. Write 0 to clear it.
1	FIFOFULL	**Set when no more packets can be loaded into RxFIFO**
0	RXPKTRDY	**Set when a data packet has been received (to RxFIFO)** The CPU clears this bit when the packet has been unloaded from the RxFIFO. An interrupt will be generated when the bit is set. Write 0 to clear it.

11200118 RX1COUNT Rx1 Count Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RXCOUNT													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	RXCOUNT	**14-bit read-only register that holds the number of received data bytes in the packet in RxFIFO** *Note: The value returned changes as FIFO is unloaded and is only valid when RxPktRdy(RxCSR.D0) is set.*

1120011A TX1TYPE Tx1Type Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TX_SPEED		TX_PROTOCOL		TX_TARGET_EP_NUMBER			

Type									RW		RW		RW			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:6	TX_SPEED	**Operating speed of target device when core is configured with multipoint option** When the core is not configured with the multipoint option, these bits should not be accessed. 2'b00: Unused 2'b01: High 2'b10: Full 2'b11: Low
5:4	TX_PROTOCOL	**The CPU sets up this to select the required protocol for the TX endpoint.** 2'b00: Illegal 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt
3:0	TX_TARGET_EP_NUMBER	**The CPU sets this value to the endpoint number contained in the TX endpoint descriptor returned to the USB2.0 Controller during device enumeration.**

1120011B TX1INTERVAL Tx1Interval Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TX_POLLING_INTERVAL_NAK_LIMIT_M							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	TX_POLLING_INTERVAL_NAK_LIMIT_M	**(Host mode only) TxInterval Register TxInterval is an 8-bit register that, for Interrupt and Isochronous transfers, defines the polling interval for the currently-selected TX endpoint.** For Bulk endpoints, this register sets the number of frames/microframes after which the endpoint should timeout on receiving a stream of NAK responses. There is a TxInterval register for each configured TX endpoint (except for Endpoint 0). In each case the value that is set defines a number of frames/microframes (High Speed transfers), as follows: Transfer Type | Speed | Valid values (m) | Interpretation Interrupt | Low Speed or Full Speed | 1-255 | Polling interval is m frames. Interrupt | High Speed | 1-16 | Polling interval is 2^(m-1) microframes Isochronous | Full Speed or High Speed | 1-16 | Polling interval is 2^(m-1) frames/microframes Bulk | Full Speed or High Speed | 2-16 | NAK Limit is 2^(m-1) frames/microframes.

Bit(s)	Name	Description
		Note: Value 0 or 1 disables the NAK timeout function. The register should be set before TxType for Bulk endpoint.

1120011C RX1TYPE Rx1Type Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RXSPEED		RX_PROTOCOL		RX_TARGET_EP_NUMBER			
Type									RW		RW		RW			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:6	RXSPEED	**Operating speed of target device when core is configured with multipoint option** When the core is not configured with the multipoint option, these bits should not be accessed. 2'b00: Unused 2'b01: High 2'b10: Full 2'b11: Low
5:4	RX_PROTOCOL	**The CPU sets up this to select the required protocol for the TX endpoint.** 2'b00: Illegal 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt
3:0	RX_TARGET_EP_NUMBER	**The CPU sets this value to the endpoint number contained in the TX endpoint descriptor returned to the USB2.0 Controller during device enumeration.**

1120011D RX1INTERVAL Rx1Interval Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_POLLING_INTERVAL_NAK_LIMIT_M							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_POLLING_INTERVAL_NAK_LIMIT_M	**RxInterval Register RxInterval is an 8-bit register that, for Interrupt and Isochronous transfers, defines the polling interval for the currently-selected RX endpoint.** For Bulk endpoints, this register sets the number of

Bit(s)	Name	Description
		frames/microframes after which the endpoint should timeout on receiving a stream of NAK responses. There is a RxInterval register for each configured RX endpoint (except for Endpoint 0). RX POLLING INTERVAL / NAK LIMIT (M), (Host mode only) In each case the value that is set defines a number of frames/microframes (High Speed transfers), as follows: Transfer Type Speed Valid values (m) Interpretation Interrupt Low Speed or Full Speed 1 - 255 Polling interval is m frames. High Speed 1 - 16 Polling interval is 2(m-1) microframes Isochronous Full Speed or High Speed 1 - 16 Polling interval is 2(m-1) frames/microframes Bulk Full Speed or High Speed 2 - 16 NAK Limit is 2(m-1) frames/microframes. *Note: Value 0 or 1 disables the NAK timeout function. The register should be set before RxType for Bulk endpoint.*

1120011F FIFOSIZE1 EP1 Configured FIFO Size Register 000000AA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RXFIFOSIZE				TXFIFOSIZE			
Type									DC				DC			
Reset									1	0	1	0	1	0	1	0

Bit(s)	Name	Description
7:4	RXFIFOSIZE	**Indicates the RxFIFO size of 2^n bytes** Example: Value 10 means 2^10 = 1024 bytes.
3:0	TXFIFOSIZE	**Indicates the TxFIFO size of 2^n bytes** Example: Value 10 means 2^10 = 1024 bytes.

11200200 DMA_INTR DMA Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_INTR_UNMASK_SET								DMA_INTR_UNMASK_CLEAR							
Type	A0								A0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_INTR_UNMASK								DMA_INTR_STATUS							
Type	RU								W1C							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DMA_INTR_UNMASK_SET	**Sets DMA_INTR_UNMASK to 1**
23:16	DMA_INTR_UNMASK_CLEAR	**Clears DMA_INTR_UNMASK to 0**
15:8	DMA_INTR_UNMASK	**Unmasks DMA interrupts** The DMA interrupt will be generated when

Bit(s)	Name	Description
7:0	DMA_INTR_STATUS	DMA_INTR_UNMASK and DMA_INTR_STATUS are both 1. **Indicates DMA complete interrupt status, one bit per DMA channel implemented** Bit 0 is used for DMA channel 1; bit 1 is used for DMA channel 2, and so on. Write 1 to clear it. Note: DMA interrupt will be asserted after DMA enable is disabled when a null packet is received even thought DMA_COUNT_M still does not achieve 0.

11200210 DMA_LIMITER DMA Limiter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DMA_LIMITER							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DMA_LIMITER	**Suppreses bus utilization of DMA channel** The value is from 0 to 255. 0 means no limitation, and 255 means totally banned. The value between 0 and 255 means certain DMA can have permission to use AHB every (4 x n) AHB clock cycles. *Note: It is not recommended to limit the bus utilization of the DMA channels because this increases the latency of response to the masters, and the transfer rate decreases as well. Before using it, make sure that the bus masters have a protection mechanism to avoid entering wrong states.*

11200220 DMA_CONFIG DMA Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DMA_ACTIVE_EN		AHB_HPROT_2_EN			DMAQ_CHAN_SEL					AHBWAIT_SEL	BOUNDARY_1K_CROSS_EN
Type					RW		RW			RW					RW	RW
Reset					0	0	0	0		0	0	0			0	0

Bit(s)	Name	Description
11:10	DMA_ACTIVE_EN	**The two bits control usb_active.** 2'b00: usb_active depends on all DMAEN of DMA channel control registers. 2'b01: usb_active ties to 1 2'b10: usb_active ties to 0

Bit(s)	Name	Description
		2'b11: usb_active depends on ep_active, dma_active and all DMAEN of DMA channel control register(OR logic)
9:8	AHB_HPROT_2_EN	**The two bits control the AHB master interface HPROT2 function operateing in non-bufferable/bufferable/last transfer non-bufferable mode.** 2'b00: All the write transfers of a burst will be accessed by bufferable mode except for the last transfer of a burst. 2'b01: AHB master HPROT2 is always accessed by non-bufferable mode. 2'b10: AHB master HPROT2 is always accessed by bufferable mode. 2'b11: Reserved
6:4	DMAQ_CHAN_SEL	**Selects DMA channel used by USB_DMAQ if it is available.** It will not affect if USB_DMAQ is not available.
1	AHBWAIT_SEL	**Selects AHBWAIT behavior** Set to 1 to return to old DMA master AHB wait condition. This bit is used to test DMA FIFO overflow bug.
0	BOUNDARY_1K_CROSS_EN	**Enables 1k boundary page crossing** Set to 1 to force burst transfer regardless 1k boundary crossing. Note: It will violate AHB 1k boundary specification but gain some bus performance.

11200204 DMA_CNTL_0 DMA Channel 0 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DMAABORT		DMACHEN	BURST_MODE		BUSERR	ENDPNT				INTEN	DMAMODE	DMADIR	DMAEN
Type			A0		RU	RW		RU	RW				RW	RW	RW	OTHER
Reset			0		0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13	DMAABORT	**If SW needs to abort the current DMA transfer, set DMAABORT=1 & DMAEN=0. After the transfer is aborted completely, DMA interrupt will occur.**
11	DMACHEN	**DMA channel enable monitor bit**
10:9	BURST_MODE	2'b00: Burst Mode 0: Bursts of unspecified length 2'b01: Burst Mode 1: INCR4 or unspecified length 2'b10: Burst Mode 2: INCR8, INCR4 or unspecified length 2'b11: Burst Mode 3: INCR16, INCR8, INCR4 or unspecified length
8	BUSERR	**Bus error**
7:4	ENDPNT	**Endpoint which DMA will transfer with**
3	INTEN	**Enables interrupt**
2	DMAMODE	**DMA mode** DMA mode 0: Single packet operation DMA mode 1: Multi packets operation, with the configuraiton of DMAReqMode in RXCSR bit 11 DMA mode 1 can support both known size or unknown size transaction.
1	DMADIR	**Direction** 0: DMA write (RX endpoint) 1: DMA read (TX endpoint)

Bit(s)	Name	Description
0	DMAEN	**Enables DMA** The bit will be cleared when the DMA transfer is completed. Programmers should not disable the DMA_en before the trnsfer is completed. If programeers disable the dma_en when transfering, the dma will not stop immediately untill the last bus transfer is completed.

11200208 DMA_ADDR_0 DMA Channel 0 Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_ADDR_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_ADDR_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DMA_ADDR_0	**32-bit DMA start address** Updated (increased) by USB2.0 controller automatically when multiple packet DMA (DMA Mode = 1) is used.

1120020C DMA_COUNT_ DMA Channel 0 Byte Count Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									DMA_COUNT_0							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_COUNT_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	DMA_COUNT_0	**24-bit DMA transfer count with byte unit** Updated (decreased) by USB2.0 controller automatically while each packet is transferred.

11200304 EP1RXPKTCOUNT EP1 RxPktCount Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EP1RXPKTCOUNT															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	EP1RXPKTCOUNT	**Sets up the number of packets of RX endpoint n size MaxP that are to be transferred in a block transfer** Only used In host mode when AutoReq is set. Has no effect In peripheral mode or when AutoReq is not set. RqPktCount (Host mode only) For each RX endpoint 1 - 15, the USB2.0 controller provides a 16-bit RqPktCount register. This read/write register is used In host mode to specify the number of packets that are to be transferred in a block transfer of one or more Bulk packets of length MaxP to RX endpoint n. The core uses the value recorded in this register to etermine the number of requests to issue where the AutoReq option (included in the RxCSR register) has been set. *Note: Multiple packets combined into a single bulk packet within the FIFO count as one packet.*

11200480 ToFUNCADDR To Function Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										ToFuncAddr						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	ToFuncAddr	**TxFuncAddr are 7-bit read/write registers that record the address of the target function that is to be accessed through the associated endpoint (Endpoint 0).** TxFuncAddr needs to be defined for each TX endpoint that is used. *Note: TxFuncAddr must be defined for Endpoint 0.*

11200488 T1FUNCADDR T1 Function Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										T1FuncAddr						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	T1FuncAddr	**TxFuncAddr are 7-bit read/write registers that record the address of the target function that is to be accessed through the associated endpoint (Endpoint 1).** TxFuncAddr needs to be defined for each TX endpoint that is used. *Note: TxFuncAddr must be defined for Endpoint 0.*

Bit(s)	Name	Description

11200482 ToHUBADDR To HUB Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ToPortAddr							ToMultiTranslator	ToHUBAddr						
Type		RW							RW	RW						
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:8	ToPortAddr	**TxPortAddr only needs to be written where a full or low speed device is connected to TX endpoint n via a high speed USB 2.0 hub which carries out the necessary transaction translation.** In such circumstances, these 7-bit read/write registers need to be used to record the port of that USB 2.0 hub through which the target associated with the endpoint is accessed. *Note: If Endpoint 0 is connected to a hub, TxHubPort must be defined. Only valid if RTL definess USB_HUB. This register is only valid @ FS/LS is plugged in at hub.*
7	ToMultiTranslator	**Bit 8 should record whether the hub has multiple transaction translator.** Only valid if RTL defines USB_HUB. This register is only valid @ FS/LS is plugged in at hub. 1'b0: Single transaction translator 1'b1: Multiple transaction translators
6:0	ToHUBAddr	**TxHUBAddr are 8-bit read/write registers only needs to be written where a full or low speed device is connected to TX endpoint n via a high speed USB2.0 hub which carries out the necessary transaction translation to convert between high speed transmission and full/low speed transmission.** The lower 7 bit should record the address of this USB 2.0 HUB. *Note: If Endpoint 0 is connected to a hub, TxHubAddr must be defined for EP0. Only valid if RTL defines USB_HUB. This register is only valid @ FS/LS is plugged in at hub.*

1120048A T1HUBADDR T1 HUB Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		T1PortAddr							T1MultiTranslator	T1HUBAddr						
Type		RW							RW	RW						

Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:8	T1PortAddr	**TxPortAddr only needs to be written where a full or low speed device is connected to TX endpoint n via a high speed USB 2.0 hub which carries out the necessary transaction translation.** In such circumstances, these 7-bit read/write registers need to be used to record the port of that USB 2.0 hub through which the target associated with the endpoint is accessed. *Note: If Endpoint 1 is connected to a hub, TxHubPort must be defined. Only valid if RTL defines USB_HUB. This register is only valid @ FS/LS is plugged in at hub.*
7	T1MultiTranslator	**Bit 8 should record whether the hub has multiple transaction translator.** Only valid if RTL defines USB_HUB. This register is only valid @ FS/LS is plugged in at hub. 1'b0: Single transaction translator 1'b1: Multiple transaction translators
6:0	T1HUBAddr	**TxHUBAddr are 8-bit read/write registers only needs to be written where a full or low speed device is connected to TX endpoint n via a high speed USB2.0 hub which carries out the necessary transaction translation to convert between high speed transmission and full/low speed transmission.** The lower 7 bit should record the address of this USB 2.0 HUB. *Note: If Endpoint 1 is connected to a hub, TxHubAddr must be defined for EP0. Only valid if RTL defines USB_HUB. This register is only valid @ FS/LS is plugged in at hub.*

1120048C R1FUNCADDR R1 Function Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										R1FuncAddr						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	R1FuncAddr	**RxFuncAddr are 7-bit read/write registers that record the address of the target function that is to be accessed through the associated endpoint (Endpoint 1).** RxFuncAddr needs to be defined for each RX endpoint that is used. *Note: RxFuncAddr does not exist on EP0.*

1120048E R1HUBADDR R1 HUB Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		R1PortAddr							R1MultiTranslator	R1HUBAddr						
Type		RW							RW	RW						
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:8	R1PortAddr	**RxPortAddr only needs to be written where a full or low speed device is connected to RX endpoint n via a high speed USB 2.0 hub which carries out the necessary transaction translation.** In such circumstances, these 7-bit read/write registers need to be used to record the port of that USB 2.0 hub through which the target associated with the endpoint is accessed. *Note: The RxPortAddr doest not exist on EP0. Only valid if RTL defines USB_HUB. This register is only valid @ FS/LS is plugged in at hub.*
7	R1MultiTranslator	**Bit 8 should record whether the hub has multiple transaction translator.** Only valid if RTL defines USB_HUB. This register is only valid @ FS/LS is plugged in at hub. 1'b0: Single transaction translator 1'b1: Multiple transaction translators
6:0	R1HUBAddr	**RxHUBAddr are 8-bit read/write registers only needs to be written where a full or low speed device is connected to RX endpoint n via a high speed USB2.0 hub which carries out the necessary transaction translation to convert between high speed transmission and full/low speed transmission.** The lower 7 bit should record the address of this USB 2.0 HUB. *Note: The RxHubAddr does not exist on EP0. Only valid if RTL defines USB_HUB. This register is only valid @ FS/LS is plugged in at hub.*

11200604 TM1 **Test Mode 1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TM1
Type																RW
Reset																0

Bit(s)	Name	Description
0	TM1	USB IP internal TM1

11200608 HWVER_DATE **HW Version Control Register** **20121214**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HWVER_DATE															
Type	DC															

Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HWVER_DATE															
Type	DC															
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	1	0	0

Bit(s)	Name	Description
31:0	HWVER_DATE	**Hardware version control register date format** 32'hYYYYMMDD

11200684 SRAMA **SRAM Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															EP0_StartAd_TM6_en	SRAMDBG
Type															RW	RW
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRAMA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	EP0_StartAd_TM6_en	**Software can enable this bit to change the EP0 FIFO start address for test mode 6 FIFO loopback test by DMA/PIO.**
16	SRAMDBG	**SRAM_DEBUG_MODE** Software can read the data in SRAM of USB core when this bit is enabled. The related registers are SRAMA, SRAMD. After setting this bit to 1, SW can set up SRAMA (SRAM address) and read the data in register SRAMD (SRAM data). Only for debugging mode and should be disabled in normal operation. 1'b0: Software sets up this bit 0 to disable SRAM_DEBUG_MODE. 1'b1: Software sets up this bit 1 to enable SRAM_DEBUG_MODE.
15:0	SRAMA	**SRAM_ADDRESS** The register is used for RISC to read data from USB SRAM. The unit is 4-byte. For example, to check 0x400 byte address, set this register to 0x100. This register is only available when the register bit SRAM_DEBUG_MODE of the register SRAMDBG is set to 1. When SRAM ADDRESS is set, SRAM DATA will display the data in the address SRAM ADDRESS in SRAM. Only for debugging mode.

11200688 SRAMD **SRAM Data Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRAMDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRAMDATA															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRAMDATA	**SRAM_DATA** The register is used for RISC to read data from USB SRAM. This register is only available when the register bit SRAM_DEBUG_MODE of the register SRAMDBG is set to 1. When SRAM ADDRESS is set, SRAM DATA will display the data in the address SRAM ADDRESS in SRAM. Only for debugging mode.

11200690 RISC_SIZE RISC Size Register 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RISC_SIZE	
Type															RW	
Reset															1	0

Bit(s)	Name	Description
1:0	RISC_SIZE	**Configures RISC wrapper access size** 2'b00: 8-bit byte access 2'b01: 16-bit half word access 2'b10: 32-bit word access 2'b11: Reserved

11200700 RESREG Reserved Register FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESERVEDH												MAC_CG_DIS	USB_CG_DIS	DMA_CG_DIS	MCU_CG_DIS
Type	RW												RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESERVEDL															HSTPWRDWN_OPT
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	RESERVEDH	**Reserved** The register is reserved for future use.
19	MAC_CG_DIS	**Disables USB MAC clock gate to enhance dynamic power**
18	USB_CG_DIS	**Disables USB clock gate**
17	DMA_CG_DIS	**Disables DMA clock gate**
16	MCU_CG_DIS	**Disables MCU clock gate**
15:1	RESERVEDL	**Reserved** The register is reserved for future use.

Bit(s)	Name	Description
0	HSTPWRDWN_OPT	**Host mode device connection detection option** 0: Disable 1: Enable the detection of device connect when MAC clock is off and drive powerdwn wakeup signal to wake up system

11200730 OTG20_CSRL OTG20 Related Control Register L 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DIS_HSUS	EN_A_HFS_WHNP	DIS_B_WTDIS	EN_HHS_SUSP_DIS	DIS_CHARGE_VBUS	EN_HSUS_RESUME_INT	EN_HSUS_RESUME	OTG20_EN
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	DIS_HSUS	**Disables host mode entering C_OPM_HSUS state before entering suspend** Suggested: 1'b1 0: Host mode enters C_OPM_HSUS state before entering suspend. 1: Disable host mode entering C_OPM_HSUS state before entering suspend.
6	EN_A_HFS_WHNP	**If this bit is enabled, FS idle of A device will transfer to HFS_HSUS state first.** Suggested: 1'b1 in all modes (device/host/otg) 0: FS idle of A device will not transfer to HFS_HSUS state first. 1: FS idle of A device will transfer to HFS_HSUS state first.
5	DIS_B_WTDIS	**Disables B device entering C_OPM_B_WTDIS states before switching to host mode** Suggested: 1'b1 0: B device enters C_OPM_B_WTDIS states before switching to host mode. 1: B device does not enter C_OPM_B_WTDIS states before switching to host mode.
4	EN_HHS_SUSP_DIS	**Enables host-hs-suspend entering OPM_FS_WTCON state first while receiving disconnect signal** Suggested: 1'b1 in all modes (device/host/otg). 0: The host mode enters fs_normal mode directly while the device receives the disconnect signal as suspend state in all states. 1: The host mode enters OPM_FS_WTCON mode first while the device receives the disconnect signal as suspend state in all states.
3	DIS_CHARGE_VBUS	**Disables B device charging VBUS function for OTG2.0 feature** 0: B device charges VBUS while B device initiates the SRP protocol. This mode is to make compatible the OTG1.3 related SRP flow. 1: B device does not charge VBUS while B device initiates the SRP protocol. This mode is to satisfy the OTG2.0 protocol.

Bit(s)	Name	Description
2	EN_HSUS_RESUME_INT	**Enables hsus mode of host initializing resuming interrupt while receiving resume K as waiting for HNP** Suggested: 1'b1 for OTG2.0 mode 0: Suspend mode of host does not initialize resuming interrupt as receiving resume K while host is waiting for HNP protocol in OTG20 mode. 1: Suspend mode of host initializes resuming interrupt as receiving resume K while host is waiting for HNP protocol in OTG20 mode.
1	EN_HSUS_RESUME	**Enables hnpsus-mode of host entering host-normal mode as receiving resume K while waiting for HNP** Suggested: 1'b0 while USB works in OTG20 mode 0: hnpsus-mode of host stays in hnpsus-mode as receiving resume K while waiting for HNP. 1: hnpsus-mode of host enters host-normal mode as receiving resume K while waiting for HNP.
0	OTG20_EN	**Enables OTG 2.0 feature** 0: Disable OTG2.0 feature; default OTG1.3 mode. 1: Enable USB OTG20 feature

11200731 OTG20_CSRH OTG20 Related Control Register H 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															DIS_AUTORST	EN_CON_DEB_SHORT
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	DIS_AUTORST	**Informs whether HW sends bus reset automatically while B-device changes to host with HNP** 0: HW sends bus reset automatically while B-device changes to host with HNP. 1: HW does not send bus reset when B-device changes to host mode. SW must set the reset bit for sending bus reset. The bit is added for OTG20 compliance test.
0	EN_CON_DEB_SHORT	**Enable this bit to decrease A device connection denounce waiting timing** Suggested: 1'b1 0: A device connection without denounce waiting timing. 1: Decrease A device connection denounce waiting timing.

3.6 USBPHY Register File

Module name: usb_sifslv_u2phy Base address: (+11210800h)

Address	Name	Width	Register Function
11210800	USBPHYACR0	32	
11210804	USBPHYACR1	32	
11210808	USBPHYACR2	32	
11210810	USBPHYACR4	32	
11210814	USBPHYACR5	32	
11210818	USBPHYACR6	32	
1121081C	U2PHYACR3	32	USB20 PHYA Control 3 Register
11210820	U2PHYACR4	32	USB20 PHYA Control 4 Register
11210824	U2PHYAMON0	32	USB20 PHYA Monitor 0 Register
11210860	U2PHYDCR0	32	USB20 PHYD Control 0 Register
11210864	U2PHYDCR1	32	USB20 PHYD Control 1 Register
11210868	U2PHYDTM0	32	USB20 PHYD Control UTMI 0 Register
1121086C	U2PHYDTM1	32	USB20 PHYD Control UTMI 1 Register
11210870	U2PHYDMON0	32	USB20 PHYD Monitor 0 Register
11210874	U2PHYDMON1	32	USB20 PHYD Monitor 1 Register
11210878	U2PHYDMON2	32	USB20 PHYD Monitor 2 Register
1121087C	U2PHYDMON3	32	USB20 PHYD Monitor 3 Register
11210880	U2PHYCR3	32	USB20 sifslv Control Register
112108FC	REGFCOM	32	USB Common Register
11211700	FMCR0	32	Frequency Meter Control 0 Registers
11211704	FMCR1	32	Frequency Meter Control 1 Registers
11211708	FMCR2	32	Frequency Meter Control 2 Registers
1121170C	FMMONR0	32	Frequency Meter Monitor 0 Registers
11211710	FMMONR1	32	Frequency Meter Monitor 1 Registers

11210800 USBPHYACR0 **00013C6E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_U SB20 _MPX _OUT _SEL				RG_USB20_TX_PH_ROT_SEL				RG_USB20_PLL_DIVEN				RG_USB20_PLL_BR	RG_USB20_PLL_BP	RG_USB20_PLL_BLP
Type		RW				RW				RW				RW	RW	RW
Reset		0	0	0		0	0	0		0	0	0		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_USB20_USBPLL_FORCE_ON	RG_USB20_PLL_FBDIV							RG_USB20_PLL_PREDIV		RG_USB20_INTR_EN	RG_USB20_REF_EN	RG_USB20_BGR_DIV		RG_USB20_CHP_EN	RG_USB20_BGR_EN
Type	RW	RW							RW		RW	RW	RW		RW	RW
Reset	0	0	1	1	1	1	0	0	0	1	1	0	1	1	1	0

Bit(s)	Mnemonic	Name	Description
30:28	MPX_OUT_SEL	RG_USB20_MPX_OUT_SEL	

Bit(s)	Mnemonic	Name	Description
26:24	**TX_PH_ROT_SEL**	RG_USB20_TX_PH _ROT_SEL	**TX clock rotation function** All port will change clock phase at the same time. 000: Phase 0 001: Phase 1 010: Phase 2 011: Phase 3 100: Phase 4 101: Phase 5
22:20	**PLL_DIVEN**	RG_USB20_PLL_D IVEN	**Time domain cap multiplication ratio** 3'd0: x1 3'd1: x2 ... 3'd6: x64
18	**PLL_BR**	RG_USB20_PLL_B R	**Adjusts resistance for bandwidth** 1'b0: BW = Fref/10 1'b1: BW = Fref/20
17	**PLL_BP**	RG_USB20_PLL_B P	**Adjusts capacitance for bandiwdth** 1'b0: When RG_PLL_BR=1'b0 1'b1: When RG_PLL_BR=1'b1
16	**PLL_BLP**	RG_USB20_PLL_B LP	**Selects LPF bandwidth** 1'b0: 40MHz 1'b1: 20MHz
15	**USBPLL_FORCE_O N**	RG_USB20_USBPL L_FORCE_ON	**Power down** 1'b0: Don't care 1'b1: Force PLL on
14:8	**PLL_FBDIV**	RG_USB20_PLL_F BDIV	**Feedback divide ratio** 7'd0: /1 7'd1: /2 ... 7'd127: /128
7:6	**PLL_PREDIV**	RG_USB20_PLL_P REDIV	**Pre-divider ratio** 2'b00: Fref = Fin/1 2'b01: Fref = Fin/2 2'b1X: Fref = Fin/4
5	**INTR_EN**	RG_USB20_INTR_ EN	**Enables VRT internal R architecture** 0: Disable 1: Enable
4	**REF_EN**	RG_USB20_REF_E N	**Enables VRT current generator** 0: Disable 1: Enable
3:2	**BGR_DIV**	RG_USB20_BGR_D IV	**Chopper frequency divider (~3MHz)** 00: REFCLK/2 01: REFCLK/4 10: REFCLK/8 11: REFCLK/16
1	**CHP_EN**	RG_USB20_CHP_E N	**Enable signal of chopper** 0: Disable 1: Enable
0	**BGR_EN**	RG_USB20_BGR_E N	**Enable signal of BGR** 0: Disable 1: Enable

11210804 USBPHYACR1 **44A44400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_USB20_CLKREF_REV								RG_USB20_INTR_CAL					RG_USB20_OTG_ VBUSTH		

Type	RW								RW					RW		
Reset	0	1	0	0	0	1	0	0	1	0	1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_USB20_VRT_VREF_SEL				RG_USB20_TERM_VREF_SEL			RG_USB20_MPX_SEL							
Type		RW				RW			RW							
Reset		1	0	0		1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**CLKREF_REV[7:0]**	RG_USB20_CLKREF_REV	**RG_USB20_CLKREF_REV[2:0] :** **RG_USB20_TERM_VREF_SEL_P1[2:0]** RG_USB20_CLKREF_REV[6:4] : RG_USB20_TERM_VREF_SEL_P2[2:0]
23:19	**INTR_CAL**	RG_USB20_INTR_CAL	**Internal R control** 00000: 6.9K ohm 00001: 6.8K ohm 10010: 5.1K ohm 11110: 3.9K ohm 11111: 3.8K ohm
18:16	**OTG_VBUSTH**	RG_USB20_OTG_VBUSTH	**VBUS threshold level control (shared circuit)** 000: 1.365V 001: 1.385V 010: 1.405V 011: 1.425V 100: 1.445V 101: 1.465V 110: 1.485V 111: 1.505V
14:12	**VRT_VREF_SEL**	RG_USB20_VRT_VREF_SEL	**Selects VRT reference voltage (shared circuit)** 000: 700mV 001: 720mV 010: 740mV 011: 760mV 100: 770mV 101: 780mV 110: 800mV 111: 820mV
10:8	**TERM_VREF_SEL**	RG_USB20_TERM_VREF_SEL	**Selects HS_TX TERM reference voltage (shared circuit)** 000: 320mV 001: 340mV 010: 360mV 011: 380mV 100: 400mV 101: 420mV 110: 440mV 111: 460mV
7:0	**MPX_SEL**	RG_USB20_MPX_SEL	**Selects MPX output signal** MPX_SEL[7]=1 bypass OP to AIO, 0 off and Hi-Z MPX_SEL[6]=1 output AIO by OP, 0 off and Hi-Z MPX_SEL[5:4]=00 output Common part MPX_SEL[5:4]=01 output Port0 part MPX_SEL[5:4]=10 output Port1 part MPX_SEL[5:4]=11 output Port2 part MPX_SEL[3]=0 output AIO MPX_SEL[3]=1 output DIO MPX_SEL[2:0] (common part) 000: OFF and Hi-Z

Bit(s)	Mnemonic	Name	Description
			001: 010: 011:

11210808 USBPHYACR2 **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_USB20_CLKREF_REV							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**CLKREF_REV[15:8]**	RG_USB20_CLKREF_REV	RG_USB20_CLKREF_REV[2:0] : RG_USB20_TERM_VREF_SEL_P1[2:0] RG_USB20_CLKREF_REV[6:4] : RG_USB20_TERM_VREF_SEL_P2[2:0]

11210810 USBPHYACR4 **00004414**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_USB20_DP_ABIST_SOURCE_EN				RG_USB20_DP_ABIST_SELE											RG_USB20_ICUSB_EN
Type	RW				RW											RW
Reset	0				0	0	0	0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_USB20_LS_CR				RG_USB20_FS_CR				RG_USB20_LS_SR				RG_USB20_FS_SR		
Type		RW				RW				RW				RW		
Reset		1	0	0		1	0	0		0	0	1		1	0	0

Bit(s)	Mnemonic	Name	Description
31	**DP_ABIST_SOURCE_EN**	RG_USB20_DP_ABIST_SOURCE_EN	**DP ABIST source enable signal** 0: Disable ABIST source 1: Enable ABIST source
27:24	**DP_ABIST_SELE**	RG_USB20_DP_ABIST_SELE	**DP ABIST source selection signal** Port 0 DP ABIST source selection signal 0000: DP=0V 0001: DP=80mV 0010: DP=100mV 0011: DP=200mV 0100: DP=220mV 0101: DP=500mV 0110: DP=520mV 0111: DP=660mV

Bit(s)	Mnemonic	Name	Description
			1000: DP=680mV 1001: DP=700mV 1010: DP=800mV 1011: DP=900mV 1100: DP=1900mV 1101: DP=2000mV 1110: DP=2100mV 1111: DP=VDD33
16	**ICUSB_EN**	RG_USB20_ICUSB_EN	**IC_USB mode enable signal** 0: Disable 1: Enable
14:12	**LS_CR**	RG_USB20_LS_CR	**Port 0 USB11 low speed mode TX slew rate contral signal**
10:8	**FS_CR**	RG_USB20_FS_CR	**Port 0 USB11 full speed mode TX slew rate contral signal**
6:4	**LS_SR**	RG_USB20_LS_SR	**Port 0 USB11 low speed mode TX slew rate contral signal** 00: Max. rt/ft 01: Normal rt/ft 10: Smaller rt/ft 11: Min. rt/ft
2:0	**FS_SR**	RG_USB20_FS_SR	**Port 0 USB11 full speed mode TX slew rate contral signal** 00: Max. rt/ft 01: Normal rt/ft 10: Smaller rt/ft 11: Min. rt/ft

11210814 USBPHYACR5 **00801000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_USB20_DISC_FIT_EN	RG_USB20_INIT_SQ_EN_DG		RG_USB20_HSTX_TMODE_SEL		RG_USB20_SQD		RG_USB20_DISCD		RG_USB20_HSTX_TMODE_EN	RG_USB20_PHYD_MONEN	RG_USB20_INLPBK_EN	RG_USB20_CHIRP_EN
Type				RW	RW		RW		RW		RW		RW	RW	RW	RW
Reset				0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_USB20_HSTX_SRCAL_EN	RG_USB20_HSTX_SRCTRL			RG_USB20_HS_100U_U3_EN	RG_USB20_GBIAS_ENB			RG_USB20_DM_ABIST_SOURCE_EN				RG_USB20_DM_ABIST_SELE			
Type	RW	RW			RW	RW			RW				RW			
Reset	0	0	0	1	0	0			0				0	0	0	0

Bit(s)	Mnemonic	Name	Description
28	**DISC_FIT_EN**	RG_USB20_DISC_FIT_EN	**DISC deglitch enable signal** 0: Disable 1: Enable
27:26	**INIT_SQ_EN_DG**	RG_USB20_INIT_SQ_EN_DG	
25:24	**HSTX_TMODE_SEL**	RG_USB20_HSTX_	**Selects HS TX test mode signal**

Bit(s)	Mnemonic	Name	Description
		TMODE_SEL	00: 240MHz clock 01: 60MHz clock 10: Hi 11: Lo
23:22	**SQD**	RG_USB20_SQD	**SQ deglitch** 00: Deglitch 1x 01: Deglitch 2x 10: Deglitch 3x 11: Deglitch 6x
21:20	**DISCD**	RG_USB20_DISCD	**DISC deglitch** 00: Deglitch 10n 01: Deglitch 6n 10: Deglitch 4n 11: Deglitch 2n
19	**HSTX_TMODE_EN**	RG_USB20_HSTX_TMODE_EN	**HS TX test mode enable signal** 0: Disable 1: Enable, and output test pattern by TMODE_SEL
18	**PHYD_MONEN**	RG_USB20_PHYD_MONEN	**Digital PHY monitor clock enable signal** 0: Disable 1: Enable
17	**INLPBK_EN**	RG_USB20_INLPBK_EN	**High speed internal loopback enable signal** 0: Disable 1: Enable
16	**CHIRP_EN**	RG_USB20_CHIRP_EN	**Sets chirp level to 0.8V when in chirp mode** 0: Disable 1: Enable
15	**HSTX_SRCAL_EN**	RG_USB20_HSTX_SRCAL_EN	**HS TX SR calibration enable signal** 0: Disable 1: Enable
14:12	**HSTX_SRCTRL**	RG_USB20_HSTX_SRCTRL	**Controls high speed slew rate** 00: Min. rt/ft 11: Max. rt/ft
11	**HS_100U_U3_EN**	RG_USB20_HS_100U_U3_EN	**Selects VRT 100uA source** 0: 100uA from USB2.0 1: 100uA from USB3.0
10	**GBIAS_ENB**	RG_USB20_GBIAS_ENB	**Enables overdrive 3.3V bias** 0: Enable bias 1: Disable bias (select ICUSB mode)
7	**DM_ABIST_SOURCE_EN**	RG_USB20_DM_ABIST_SOURCE_EN	**DM ABIST source enable signal** 0: Disable ABIST source 1: Enable ABIST source
3:0	**DM_ABIST_SELE**	RG_USB20_DM_ABIST_SELE	**DM ABIST source selection signal** Port 0 DM ABIST source selection signal 0000: DM=0V 0001: DM=80mV 0010: DM=100mV 0011: DM=200mV 0100: DM=220mV 0101: DM=500mV 0110: DM=520mV 0111: DM=660mV 1000: DM=680mV 1001: DM=700mV 1010: DM=800mV 1011: DM=900mV 1100: DM=1900mV 1101: DM=2000mV

Bit(s)	Mnemonic	Name	Description
			1110: DM=2100mV 1111: DM=VDD33

11210818 USBPHYACR6 **00900488**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_USB20_PHY_REV								RG_USB20_BC11_SW_EN	RG_USB20_SR_CLK_SEL		RG_USB20_OTG_VBUSCMP_EN	RG_USB20_OTG_ABIST_EN	RG_USB20_OTG_ABIST_SELE		
Type	RW								RW	RW		RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	1	0		1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_USB20_HSRX_MMODE_SELE			RG_USB20_HSRX_BIAS_EN_SEL		RG_USB20_HSRX_TMODE_EN	RG_USB20_DISCTH				RG_USB20_SQTH			
Type			RW			RW		RW	RW				RW			
Reset			0	0		1	0	0	1	0	0	0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**PHY_REV[7:0]**	RG_USB20_PHY_REV	**Reserves INT PHY**
23	**BC11_SW_EN**	RG_USB20_BC11_SW_EN	**BC1.1 switch control** 0: Disable 1: Enable
22	**SR_CLK_SEL**	RG_USB20_SR_CLK_SEL	**Selects SR clock** 0: Slew rate calibration clock 1: 240MHz for ABIST clock
20	**OTG_VBUSCMP_EN**	RG_USB20_OTG_VBUSCMP_EN	**Enables OTG** For U3: Disable 0: Disable 1: Enable
19	**OTG_ABIST_EN**	RG_USB20_OTG_ABIST_EN	**OTG ABIST mode enable signal** 0: Disable 1: Enable
18:16	**OTG_ABIST_SELE**	RG_USB20_OTG_ABIST_SELE	**Selects OTG ABIST voltage** 000: 100mV 001: 200mV 010: 350mV 011: 450mV 100: 700mV 101: 800mV 110: 1400mV 111: 1600mV
13:12	**HSRX_MMODE_SELE**	RG_USB20_HSRX_MMODE_SELE	**Selects HS_RX manual mode** 00: HS_RX in normal mode, switch SQ/DISC function by IDLEB 01: Manual mode, switch SQ (IDLEB=0)/DISC (IDLEB=1) function 10: Force HS_RX in SQ mode 11: Force HS_RX in DISC mode
10:9	**HSRX_BIAS_EN_S**	RG_USB20_HSRX_	**Selects HS RX bias enable signal**

Bit(s)	Mnemonic	Name	Description
	EL	BIAS_EN_SEL	00: ENPLL (always on) 01: IDLEB | RCV_EN (when TX on, RX off, device mode only) 10: !ENPLL | FS_BIAS_EN (keep high in HS mode) 11: RG_USB20_HSRX_TMODE_EN
8	**HSRX_TMODE_EN**	RG_USB20_HSRX_TMODE_EN	**When RG_USB20_HSRX_BIAS_EN_SEL[1:0]=11** HS RX bias will be controlled by this signal. 0: Disable 1: Enable
7:4	**DISCTH**	RG_USB20_DISCT H	**Disconnect threshold (shared for host disconnet and trimming control)** 0000: 400mV 0001: 420mV 0010: 440mV 0011: 460mV 0100: 480mV 0101: 500mV 0110: 520mV 0111: 540mV 1000: 560mV 1001: 580mV 1010: 600mV 1011: 620mV 1100: 640mV 1101: 660mV 1110: 680mV 1111: 700mV
3:0	**SQTH**	RG_USB20_SQTH	**SQ threshold** 0000: 85mV 0001: 90mV 0010: 95mV 0011: 100mV 0100: 105mV 0101: 110mV 0110: 115mV 0111: 120mV 1000: 125mV 1001: 130mV 1010: 135mV 1011: 140mV 1100: 145mV 1101: 150mV 1110: 155mV 1111: 160mV

1121081C U2PHYACR3 USB20 PHYA Control 3 Register C0040000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_USB20_HSTX_DBIST					RG_USB20_HSTX_BIST_EN	RG_USB20_HSTX_I_EN_MODE						RG_USB20_USB11_TMODE_EN	RG_USB20_TMODE_FS_LS_TX_EN	RG_USB20_TMODE_FS_LS_RCV_EN	RG_USB20_TMODE_FS_LS_MODE

Type	RW					RW	RW						RW	RW	RW	RW
Reset	1	1	0	0		0	0	0					0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_USB20_HS_TERM_EN_MODE		RG_USB20_PUPD_BIST_EN	RG_USB20_EN_PU_DM	RG_USB20_EN_PD_DM	RG_USB20_EN_PU_DP	RG_USB20_EN_PD_DP								
Type		RW		RW	RW	RW	RW	RW								
Reset		0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
31:28	**HSTX_DBIST**	RG_USB20_HSTX_DBIST	**HS_TX BIST output data**
26	**HSTX_BIST_EN**	RG_USB20_HSTX_BIST_EN	**High speed TX BIST enable signal** 0: Disable TX BIST 1: Enable TX BIST
25:24	**HSTX_I_EN_MODE**	RG_USB20_HSTX_I_EN_MODE	**HS_TX output current enable mode** 00: Enable TX current when EN_HS_TX_I=1 (toggle mode) 01: Enable TX current when EN_HS_TX_I=1 or EN_HS_TERM=1 10: Force to disable TX current 11: Force to enable TX current
19	**USB11_TMODE_EN**	RG_USB20_USB11_TMODE_EN	**USB11 test mode enable signal** 0: Disable test mode 1: Enable test mode
18	**TMODE_FS_LS_TX_EN**	RG_USB20_TMODE_FS_LS_TX_EN	**USB11 test mode EN_FS_LS_TX0 signal** 0: Disable USB11 TX in test mode 1: Enable USB11 TX in test mode
17	**TMODE_FS_LS_RCV_EN**	RG_USB20_TMODE_FS_LS_RCV_EN	**USB11 test mode EN_FS_LS_TX0 signal** 0: Disable USB11 receiver in test mode 1: Enable USB11 receiver in test mode
16	**TMODE_FS_LS_MODE**	RG_USB20_TMODE_FS_LS_MODE	**USB11 test mode FS_LS_MODE signal** 0: Enable USB11 into low speed mode in test mode 1: Enable USB11 into full speed mode in test mode
14:13	**HS_TERM_EN_MODE**	RG_USB20_HS_TERM_EN_MODE	**HS R45 enable mode** 00: Enable R45 when EN_HS_TERM=1 01: Enable R45 when EN_HS_TERM=1 10: Force to disable R45 11: Force to enable R45
12	**PUPD_BIST_EN**	RG_USB20_PUPD_BIST_EN	
11	**EN_PU_DM**	RG_USB20_EN_PU_DM	
10	**EN_PD_DM**	RG_USB20_EN_PD_DM	
9	**EN_PU_DP**	RG_USB20_EN_PU_DP	
8	**EN_PD_DP**	RG_USB20_EN_PD_DP	

11210820 U2PHYACR4 USB20 PHYA Control 4 Register 0000001A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														rg_usb20_dp_	RG_USB20_DM_	usb20_dp_100

														100k_mode	100K_EN	k_en
Type														RW	RW	RW
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	usb20_gpio_dm_i	usb20_gpio_dp_i	usb20_gpio_dm_oe	usb20_gpio_dp_oe			rg_usb20_gpio_ctl	usb20_gpio_mode			RG_USB20_TX_BIAS_EN	RG_USB20_TX_VCMPDN_EN	RG_USB20_HS_SQ_EN_MODE		RG_USB20_HS_RCV_EN_MODE	
Type	RW	RW	RW	RW			RW	RW			RW	RW	RW		RW	
Reset	0	0	0	0			0	0			0	1	1	0	1	0

Bit(s)	Mnemonic	Name	Description
18		rg_usb20_dp_100k_mode	
17	**DM_100K_EN**	RG_USB20_DM_100K_EN	
16	**DP_100K_EN**	usb20_dp_100k_ en	**RG_USB20_DP_100K_EN = usb20_dp_100k_en when rg_usb20_dp_100k_mode =1** 0: Disable DP 100k 1: Enable DP 100k
15	**usb20_gpio_dm_ i**	usb20_gpio_dm_ i	**USB20 GPIO DP input**
14	**usb20_gpio_dp_ i**	usb20_gpio_dp_ i	**USB20 GPIO DP input**
13	**usb20_gpio_dm_ oe**	usb20_gpio_dm_ oe	**Enables USB20 GPIO DM output**
12	**usb20_gpio_dp_ oe**	usb20_gpio_dp_ oe	**Enables USB20 GPIO DP output**
9	**rg_usb20_gpio_ ctl**	rg_usb20_gpio_ ctl	**USB20 GPIO control** 0: By USB PHY register 1: System register
8	**usb20_gpio_mod e**	usb20_gpio_mod e	**USB20 GPIO Mode enable control** 0: Disable 1: Enable
5	**TX_BIAS_EN**	RG_USB20_TX_BIAS_EN	
4	**TX_VCMPDN_EN**	RG_USB20_TX_VCMPDN_EN	
3:2	**HS_SQ_EN_MODE**	RG_USB20_HS_SQ_EN_MODE	
1:0	**HS_RCV_EN_MODE**	RG_USB20_HS_RCV_EN_MODE	

11210824 U2PHYAMON0 USB20 PHYA Monitor 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RGO_USB20_GPIO_DM_O	RGO_USB20_GPIO_DP_O
Type															RO	RO

Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	**RGO_GPIO_DM_O**	RGO_USB20_GPIO_DM_O	USB20 GPIO DM data output to Reg
0	**RGO_GPIO_DP_O**	RGO_USB20_GPIO_DP_O	USB20 GPIO DP data output to Reg

11210860 U2PHYDCR0 USB20 PHYD Control 0 Register 00000402

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_USB20_CDR_TST		RG_USB20_GATED_ENB		RG_USB20_TESTMODE		RG_USB20_PLL_STABLE	RG_USB20_PLL_FORCE_ON	RG_USB20_PHYD_RESERVE							
Type	RW		RW		RW		RW	RW	RW							
Reset	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_USB20_PHYD_RESERVE								RG_USB20_EBTHRLD	RG_USB20_EARLY_HSTX_I	RG_USB20_TX_TST	RG_USB20_NEGEDGE_ENB	RG_USB20_CDR_FILT			
Type	RW								RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
31:30	**CDR_TST**	RG_USB20_CDR_T ST	**CDR module function option** For debugging.
29	**GATED_ENB**	RG_USB20_GATED_ENB	**Enables high level clock gating** For debugging. 0: Enable 1: Disable
27:26	**TESTMODE**	RG_USB20_TESTMODE	**Selects USB test mode** 00: Normal 01: Enable loopback (set to high to initialize loopback; set to low and check LB_DONE/LB_PASS) 10: Reserved 11: Reserved
25	**PLL_STABLE**	RG_USB20_PLL_STABLE	**PHY clock enable signal** 0: PHY_CLK gated 1: PHY_CLK sent out
24	**PLL_FORCE_ON**	RG_USB20_PLL_FORCE_ON	**PLL on even when both ports suspend** For output DIV_CK. 0: Normal (PLL on when not in suspend mode) 1: Force on (PLL always on)
23:8	**PHYD_RESERVE**	RG_USB20_PHYD_RESERVE	**Reserved** RG_PHYD_RESERVE[1:0]: rg_tapctl[1:0]: tapsel optional +1/-1 2'b00/2'b11: No change 2'b01: tap_sel -1 2'b10: tap_sel +1 RG_PHYD_RESERVE[2]: eco option for fixing DA_USB20_HS_TERM_EN = 0 when in non-driving mode

Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable RG_PHYD_RESERVE[6:3]: rg_sq_option[3:0] RG_PHYD_RESERVE[8:7]: Reserved RG_PHYD_RESERVE[9]: rg_rcven_option RG_PHYD_RESERVE[11:10]: rg_phydmon_option RG_PHYD_RESERVE[14:13]: rg_preamble_t-opt[1:0] RG_PHYD_RESERVE[12]: rg_tap_record_clr RG_PHYD_RESERVE[15]: Enable loopctrl clock CG
7	**EBTHRLD**	RG_USB20_EBTHRLD	**USB20 elastic buffer tholdshold option** 0: wr_ptr = 4 1: wr_ptr = 3
6	**EARLY_HSTX_I**	RG_USB20_EARLY_HSTX_I	**HSTX current source turn-on timing** 0: Normal 1: Earlier
5	**TX_TST**	RG_USB20_TX_TST	**TX macro test option** For debugging.
4	**NEGEDGE_ENB**	RG_USB20_NEGEDGE_ENB	**UTMI output signal aligned to negative edge for hold time issue** 0: Negedge phy_clk registered UTMI output 1: Posedge phy_clk registered UTMI output
3:0	**CDR_FILT**	RG_USB20_CDR_FILT	**Selects CDR low pass filter** For debugging.

11210864 U2PHYDCR1 USB20 PHYD Control 1 Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_USB20_PROBE_SEL								RG_USB20_DRVVBUS	rg_debug_en	RG_USB20_OTG_PROBE		RG_USB20_SW_PLLMODE		RG_USB20_BERTH	
Type	RW								RW	RW	RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_USB20_LBMODE		RG_USB20_FORCE_TAP	RG_USB20_TAPSEL											
Type		RW		RW	RW											
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:24	**PROBE_SEL**	RG_USB20_PROBE_SEL	**[4:0]: Debug signal selection** [7:5]: Reserved
23	**DRVVBUS**	RG_USB20_DRVVBUS	**Controls DRVVBUS signal when force_drvvbus = 1 or utmi_muxsel = 1**
22	**rg_debug_en**	rg_debug_en	**Enables USB UTMI rx_active and tx_valid debugging** 0: Disable 1: Enable
21:20	**OTG_PROBE**	RG_USB20_OTG_PROBE	**Selects OTG signals to USBSIF_PROBE_OUT[4:0]**
19:18	**SW_PLLMODE**	RG_USB20_SW_PLLMODE	**[0]: SW PLL Stable mode** 0: HW pll stable mode, 100usec pll stable time controller by HW 1: SW pll stable mode, 100usec pll stable time controller

Bit(s)	Mnemonic	Name	Description
			by RG_PLL_STABL [1]: PLL stable time option 0: stable time = 8192*free clk perioed (>100usec for 60M)
17:16	**BERTH**	RG_USB20_BERTH	**Loopback bit errors(BER) threshold** When BER > BERTH, loopback will fail. 00: 0 01: 16 10: 64 11: 128
14:13	**LBMODE**	RG_USB20_LBMOD E	**Loop back mode** RG_LBMODE[0]: 0: When compared data mismatch, lb_cmpok is always low. 1: When compared data mismatch, lb_cmpok goes low until compared data match then goes high RG_LBMODE[1]: 0: Expected data are continuous. 1: Expected data will be re-synced.
12	**FORCE_TAP**	RG_USB20_FORCE _TAP	**Forces CDR tap_sel** 0: Disable 1: Enable
11:0	**TAPSEL**	RG_USB20_TAPSE L	**When RG_FORCE_TAP=1, tap_sel = RG_TAPSEL**

11210868 U2PHYDTM0 USB20 PHYD Control UTMI 0 Register 02040000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_uart_mode		force_uart_i	force_uart_bias_en	force_uart_tx_oe	force_uart_en	force_usb_clken	force_drvvbus	force_datain	force_txvalid	force_dm_pulldown	force_dp_pulldown	force_xcvrsel	force_suspendm	force_termsel	force_opmode
Type	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	utmi_muxsel	RG_RESET	RG_DATAIN				RG_TXVALIDH	RG_TXVALID	RG_DMPULLDOWN	RG_DPPULLDOWN	RG_XCVRSEL		RG_SUSPENDM	RG_TERMSEL	RG_OPMODE	
Type	RW	RW	RW				RW	RW	RW	RW	RW		RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:30	**rg_uart_mode**	rg_uart_mode	**UART mode, control RG_DP_100K_EN** 00: RG_DP_100K_EN = DA_USB_UART_EN 01: RG_DP_100K_EN = DA_USB_UART_EN & ~DA_USB_UART_TX_OE 10: RG_DP_100K_EN = 0 11: RG_DP_100K_EN = 1
29	**force_uart_i**	force_uart_i	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing UART_I to RG_UART_I value. 0: Disable 1: Enable
28	**force_uart_bias_en**	force_uart_bias_en	**When in USB PHY FT test mode, bypasses PHY UTMI signals**

Bit(s)	Mnemonic	Name	Description
			Used for forcing USB20_UART_BIAS_EN to RG_UART_BIAS_EN value. 0: Disable 1: Enable
27	**force_uart_tx_ oe**	force_uart_tx_ oe	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing USB20_UART_TX_OE to RG_UART_TX_OE value. 0: Disable 1: Enable
26	**force_uart_en**	force_uart_en	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing USB20_UART_EN to RG_UART_EN value. 0: Disable 1: Enable
25	**force_usb_clke n**	force_usb_clke n	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing USB_CLKEN to RG_USB_CLKEN value. 0: Disable 1: Enable
24	**force_drvvbus**	force_drvvbus	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing USBSIF_DRVVBUS to RG_USB20_DRVVBUS value. 0: Disable 1: Enable
23	**force_datain**	force_datain	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal DATA_IN to a specific value. 0: Disable 1: Enable
22	**force_txvalid**	force_txvalid	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal TXVALID to a specific value. 0: Disable 1: Enable
21	**force_dm_pulld own**	force_dm_pulld own	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal DMPULLDOWN to a specific value. 0: Disable 1: Enable
20	**force_dp_pulld own**	force_dp_pulld own	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal DPPULLDOWN to a specific value. 0: Disable 1: Enable
19	**force_xcvrsel**	force_xcvrsel	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal XCVRSEL to a specific value. 0: Disable 1: Enable
18	**force_suspendm**	force_suspendm	**When in USB PHY FT test mode, bypasses PHY**

Bit(s)	Mnemonic	Name	Description
			UTMI signals Used for forcing PHY UTMI signal SUSPENDM to a specific value. 0: Disable 1: Enable
17	**force_termsel**	force_termsel	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal TERMSEL to a specific value. 0: Disable 1: Enable
16	**force_opmode**	force_opmode	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal OPMODE to a specific value. 0: Disable 1: Enable
15	**utmi_muxsel**	utmi_muxsel	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing all PHY UTMI signals to specific values. 0: Disable 1: Enable
14	**RG_RESET**	RG_RESET	**Used for controlling PHY UTMI signal USB20_RESET = RG_RESET for Soft RESET**
13:10	**RG_DATAIN**	RG_DATAIN	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal DATA_IN[31:0] = 4{RG_DATAIN} when force_datain = 1 or utmi_muxsel = 1.
9	**RG_TXVALIDH**	RG_TXVALIDH	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY utmi signal TXVALIDH when force_txvalid = 1 or utmi_muxsel = 1.
8	**RG_TXVALID**	RG_TXVALID	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal TXVALID when force_txvalid = 1 or utmi_muxsel = 1.
7	**RG_DMPULLDOEN**	RG_DMPULLDOWN	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY utmi signal DMPULLDOWN when force_dm_pulldown = 1 or utmi_muxsel = 1.
6	**RG_DPPULLDOWN**	RG_DPPULLDOWN	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal DPPULLDOWN when force_dp_pulldown = 1 or utmi_muxsel = 1.
5:4	**RG_XCVRSEL**	RG_XCVRSEL	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal XCVRSEL[1:0] when force_xcvrsel = 1 or utmi_muxsel = 1.
3	**RG_SUSPENDM**	RG_SUSPENDM	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY utmi signal SUSPENDM when force_suspendm = 1 or utmi_muxsel = 1.
2	**RG_TERMSEL**	RG_TERMSEL	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal TERMSEL when force_termsel = 1 or utmi_muxsel = 1.
1:0	**RG_OPMODE**	RG_OPMODE	**When in USB PHY FT test mode, bypasses PHY UTMI signals**

Bit(s)	Mnemonic	Name	Description
			Used for controlling PHY UTMI signal OPMODE[1:0] when force_opmode = 1 or utmi_muxsel = 1.

1121086C U2PHYDTM1 USB20 PHYD Control UTMI 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_USB20_PRBS7_EN		RG_USB20_PRBS7_BITCNT						RG_USB20_CLK48M_EN	RG_USB20_CLK60M_EN			RG_UART_I	RG_UART_BIAS_EN	RG_UART_TX_OE	RG_UART_EN
Type	RW		RW						RW	RW			RW	RW	RW	RW
Reset	0		0	0	0	0	0	0	0	0			0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			force_vbusvalid	force_sessend	force_bvalid	force_avalid	force_iddig	force_idpullup			RG_VBUSVALID	RG_SESSEND	RG_BVALID	RG_AVALID	RG_IDDIG	RG_IDPULLUP
Type			RW	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**PRBS7_EN**	RG_USB20_PRBS7_EN	**Enables USB20 on-chip PRBS7 decoder**
29:24	**PRBS7_BITCNT**	RG_USB20_PRBS7_BITCNT	**USB20 on-chip PRBS7 compare bit count = (rg_prbs7_bitcnt+1)*210**
23	**CLK48M_EN**	RG_USB20_CLK48M_EN	**Enables MAC 48MHz clock** 0: Disable 1: Enable
22	**CLK60M_EN**	RG_USB20_CLK60M_EN	**Enables MAC 60MHz clock** 0: Disable 1: Enable
19	**RG_UART_I**	RG_UART_I	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling DA_USB20_UART_I when force_uart_i = 1.
18	**RG_UART_BIAS_EN**	RG_UART_BIAS_EN	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling USB20_UART_BIAS_EN when force_uart_bias_en = 1.
17	**RG_UART_TX_OE**	RG_UART_TX_OE	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling USB20_UART_TX_OE when force_uart_tx_oe = 1.
16	**RG_UART_EN**	RG_UART_EN	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling USB20_UART_EN when force_uart_en = 1.
13	**force_vbusvalid**	force_vbusvalid	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal vbusvalid to a specific value. 0: Disable 1: Enable
12	**force_sessend**	force_sessend	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal sessend to a specific

Bit(s)	Mnemonic	Name	Description
			value. 0: Disable 1: Enable
11	**force_bvalid**	force_bvalid	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal bvalid to a specific value. 0: Disable 1: Enable
10	**force_avalid**	force_avalid	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal avalid to a specific value. 0: Disable 1: Enable
9	**force_iddig**	force_iddig	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal iddig to a specific value. 0: Disable 1: Enable
8	**force_idpullup**	force_idpullup	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for forcing PHY UTMI signal idpullup to a specific value. 0: Disable 1: Enable
5	**RG_VBUSVALID**	RG_VBUSVALID	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal VBUSVALID when force_vbusvalid = 1 or utmi_muxsel = 1.
4	**RG_SESSEND**	RG_SESSEND	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal SESSEND when force_sessend = 1 or utmi_muxsel = 1.
3	**RG_BVALID**	RG_BVALID	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal BVALID when force_bvalid = 1 or utmi_muxsel = 1.
2	**RG_AVALID**	RG_AVALID	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal AVALID when force_avalid = 1 or utmi_muxsel = 1.
1	**RG_IDDIG**	RG_IDDIG	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal IDDIG when force_iddig = 1 or utmi_muxsel = 1.
0	**RG_IDPULLUP**	RG_IDPULLUP	**When in USB PHY FT test mode, bypasses PHY UTMI signals** Used for controlling PHY UTMI signal IDPULLUP when force_idpullup = 1 or utmi_muxsel = 1.

11210870 U2PHYDMON0 USB20 PHYD Monitor 0 Register 000A1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													RG_USB20_ EOP_CTL			
Type													RW			

Reset													1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_USB20_BGLPF_EN_OPT				RG_USB20_BGLPF_FORCE_OFF	RG_USB20_BGLPF_FORCE_ON	RG_USB20_PRBS7_BERTH							
Type			RW				RW	RW	RW							
Reset			0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:16		RG_USB20_EOP_CTL	
13:10		RG_USB20_BGLPF_EN_OPT	**Counter value option** Compare with DA_USB20_PLL_EN,DA_USB20_BGLPF_EN delay time option.
9		RG_USB20_BGLPF_FORCE_OFF	**Forces off LPF resistance** 0: Normal (controlled by other logic) 1: Force off (LPF resistance)
8		RG_USB20_BGLPF_FORCE_ON	**Forces on LPF resistance** 0: Normal (controlled by other logic) 1: Force on (LPF resistance)
7:0	**PRBS7_BERTH**	RG_USB20_PRBS7_BERTH	**USB20 PRBS7 bit error rate pass/fail threshold**

11210874 U2PHYDMON1 USB20 PHYD Monitor 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	USB20_UART_O	RGO_USB20_LB_PASS	RGO_USB20_LB_DONE	AD_USB20_BVALID	USB20_IDDIG	AD_USB20_VBUSVALID	AD_USB20_SESSEND	AD_USB20_AVALID	USB20_LINE_STATE		USB20_HST_DISCON	USB20_TX_READY	USB20_RX_ERROR	USB20_RX_ACTIVE	USB20_RX_VALIDH	USB20_RX_VALID
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO		RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	USB20_DATA_OUT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**USB20_UART_O**	USB20_UART_O	**USB20_UART_O**
30	**RGO_USB20_LB_PASS**	RGO_USB20_LB_PASS	**Loopback passed, active high** Should be checked after loopback_en is disabled.
29	**RGO_USB20_LB_DONE**	RGO_USB20_LB_DONE	**Loopback done, active high** Should be checked after loopback_en is disabled.
28	**BVALID**	AD_USB20_BVALID	**OTG BVALID**
27	**IDDIG**	USB20_IDDIG	**OTG IDDIG**
26	**VBUSVALID**	AD_USB20_VBUSVALID	**OTG VBUSVALID**
25	**SESSEND**	AD_USB20_SESSEND	**OTG SESSEND**
24	**AVALID**	AD_USB20_AVALID	**OTG AVALID**
23:22	**USB20_LINE_STATE**	USB20_LINE_STATE	**Line state**
21	**USB20_HST_DISC**	USB20_HST_DISCON	**Host disconnection (host only)**

Bit(s)	Mnemonic	Name	Description
	ON		
20	**USB20_TX_READY**	USB20_TX_READY	**Transmit data ready**
19	**USB20_RX_ERROR**	USB20_RX_ERROR	**Receive error**
18	**USB20_RX_ACTIV E**	USB20_RX_ACTIV E	**Receive active**
17	**USB20_RX_VALID H**	USB20_RX_VALID H	**Received data high byte valid**
16	**USB20_RX_VALID**	USB20_RX_VALID	**Received data valid**
15:0	**USB20_DATA_OUT**	USB20_DATA_OUT	**USB received data output**

11210878 U2PHYDMON2 USB20 PHYD Monitor 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rgo_txvalid_cnt								rgo_rxactive_cnt							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RGO_USB20_LB_BERCNT								USB20_PROBE_OUT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**rgo_txvalid_cn t**	rgo_txvalid_cn t	**USB PHY UTMI interface USB20_TX_VALID active count** When rg_debug_en = 1, the counter will count tx_valid active times.
23:16	**rgo_rxactive_c nt**	rgo_rxactive_c nt	**USB PHY UTMI Interface USB20_RX_ACTIVE active count** When rg_debug_en = 1, the counter will count rx_active active times.
15:8	**RGO_USB20_LB_B ERCNT**	RGO_USB20_LB_B ERCNT	**Loopback bit error counter**
7:0	**USB20_PROBE_OU T**	USB20_PROBE_OU T	**Debug signal output, selected by RG_PROBE_SEL[4:0]** Connect to GPIO in normal operation debug mode and also connect to registers for ACD ABIST.

1121087C U2PHYDMON3 USB20 PHYD Monitor 3 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RGO_USB20_PRBS7_E RRCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RGO_USB20_PRBS7_DONE	RGO_USB20_PRBS7_LOCK	RGO_USB20_PRBS7_PASS	RGO_USB20_PRBS7_PASSTH
Type													RO	RO	RO	RO
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
31:16	**RGO_PRBS7_ERRCNT**	RGO_USB20_PRBS7_ERRCNT	USB20 PRBS7 Bit error count indicator
3	**RGO_PRBS7_DONE**	RGO_USB20_PRBS7_DONE	USB20 PRBS7 done indicator (finish compare)
2	**RGO_PRBS7_LOCK**	RGO_USB20_PRBS7_LOCK	USB20 PRBS7 lock indicator
1	**RGO_PRBS7_PASS**	RGO_USB20_PRBS7_PASS	USB20 PRBS7 pass indicator (bit error free)
0	**RGO_PRBS7_PASSTH**	RGO_USB20_PRBS7_PASSTH	USB20 PRBS7 pass threshold indicator (bit error < BERTH)

11210880 U2PHYCR3 USB20 sifslv Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														force_linestate	RG_LINESTATE	
Type														RW	RW	
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	**force_linestat e**	force_linestat e	USB20 force linestate
1:0	**RG_LINESTATE**	RG_LINESTATE	USB20 LineState RG

112108FC REGFCOM USB Common Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_PAGE															i2c_mode
Type	RW															RW
Reset	0	0	0	0	0	0	0	0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
31:24	**RG_PAGE**	RG_PAGE	**RG_PAGE [3:0]: Port page index registers for I2C page base registers** The Register is I2C access only. 4'h0: Port 0 4'h1: Port 1 4'h2: Port 2 4'h3: Port 3 4'hx: 4'hf: Port f RG_PAGE[7:0]: Function page index registers for I2C page base registers. The Register is I2C access only.

Bit(s)	Mnemonic	Name	Description
16	**i2c_mode**	i2c_mode	4'h0: USB20 4'h1: USB30 digital 4'h2: USB30 phya 4'hf: Frequency meter **Access registers by AHB or I2C** This register is I2C access only. 0: AHB mode 1: I2C mode

11211700 FMCR0 Frequency Meter Control 0 Registers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_LOCKTH				RG_MONCLK_SEL		RG_FM_MODE	RG_FREQDET_EN	RG_CYCLECNT							
Type	RW				RW		RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CYCLECNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**RG_LOCKTH**	RG_LOCKTH	**Detects PLL lock threshold**
27:26	**RG_MONCLK_SEL**	RG_MONCLK_SEL	**Selects monitor clock** 00: AD_USB_MONCLK 01: AD_USB_MONCLK1 10: AD_USB_MONCLK2 11: AD_USB_MONCLK3
25	**RG_FM_MODE**	RG_FM_MODE	**Frequency meter mode** 0: Normal mode, frequency detection one time only 1: Detect PLL lock mode
24	**RG_FREQDET_EN**	RG_FREQDET_EN	**Enables frequency meter** 0: Disable 1: Enable
23:0	**CYCLECNT**	RG_CYCLECNT	**Cycles of monclk to be measured**

11211704 FMCR1 Frequency Meter Control 1 Registers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_TARGET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_TARGET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RG_TARGET**	RG_TARGET	Adjusts capacitance

11211708 FMCR2 Frequency Meter Control 2 Registers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_OFFSET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OFFSET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RG_OFFSET**	RG_OFFSET	Frequency meter out offset tolerance

1121170C FMMONR0 Frequency Meter Monitor 0 Registers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	USB_FM_OUT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	USB_FM_OUT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**USB_FM_OUT**	USB_FM_OUT	Frequency meter detection result

11211710 FMMONR1 Frequency Meter Monitor 1 Registers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**RG_FRCK_EN**							**USBPLL_LOCK**	**USB_FM_VLD**
Type								RW							RO	RO
Reset								0							0	0

Bit(s)	Mnemonic	Name	Description
8	**RG_FRCK_EN**	RG_FRCK_EN	**Enables free clock** 0: Disable 1: Enable
1	**USBPLL_LOCK**	USBPLL_LOCK	**Monitor clock lock signal**
0	**USB_FM_VLD**	USB_FM_VLD	**Frequency meter detection done**

3.7 SPI Interface Controller

Module name: spio Base address: (+1100a000h)

Address	Name	Width	Register Function
1100A000	SPI_CFG0	32	SPI Configuration 0 Register
1100A004	SPI_CFG1	32	SPI Configuration 1 Register
1100A008	SPI_TX_SRC	32	SPI TX Source Address Register
1100A00C	SPI_RX_DST	32	SPI RX Destination Address Register
1100A010	SPI_TX_DATA	32	SPI TX DATA FIFO
1100A014	SPI_RX_DATA	32	SPI RX DATA FIFO
1100A018	SPI_CMD	32	SPI Command Register
1100A01C	SPI_STATUS0	32	SPI Status 0 Register
1100A020	SPI_STATUS1	32	SPI Status 1 Register
1100A024	SPI_PAD_MACRO_SEL	32	SPI pad_macro selection Register
1100A028	SPI_CFG2	32	SPI Configuration 2 Register

1100A000 SPI_CFG0 SPI Configuration 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CS_SETUP_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CS_HOLD_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	**CS_SETUP_COUNT**	CS_SETUP_COUNT	The chip select setup time = (CS_SETUP_COUNT+1) * CLK_PERIOD, where CLK_PERIOD is the cycle time of the clock the SPI engine adopts.
15:0	**CS_HOLD_COUNT**	CS_HOLD_COUNT	The chip select hold time = (CS_HOLD_COUNT+1) * CLK_PERIOD.

1100A004 SPI_CFG1 SPI Configuration 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GET_TICK_DLY						PACKET_LENGTH									
Type	RW						RW									
Reset	0	0	0				0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PACKET_LOOP_CNT								CS_IDLE_COUNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:29	**GET_TICK_DLY**	GET_TICK_DLY	**If the speed of SPI is not fast enough, these three bits can help tolerance get_tick timing.** The timing range between get_tick is one cycle

Bit(s)	Mnemonic	Name	Description
			depending on SPI system clock.
25:16	**PACKET_LENGTH**	PACKET_LENGTH	
15:8	**PACKET_LOOP_CNT**	PACKET_LOOP_CNT	**The transmission on the SPI bus consists up units bytes. Hence, the PACKET_LENGTH[9:0] define number of bytes in one packet, and PACKET_LOOP_CNT[7:0] defines the number of packets within one transaction.** The number of bytes in one packet = PACKET_LENGTH + 1. The number of packets in one transaction = PACKET_LOOP_CNT + 1. Total bytes of one transaction = (PACKET_LENGTH + 1) * (PACKET_LOOP_CNT + 1).
7:0	**CS_IDLE_COUNT**	CS_IDLE_COUNT	**The chip select idle time between consecutive transaction = (CS_HOLD_COUNT+1) * CLK_PERIOD.**

1100A008 SPI_TX_SRC SPI TX Source Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_TX_SRC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_TX_SRC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SPI_TX_SRC**	SPI_TX_SRC	**If TX_DMA_EN is set, the data to be putted on the MOSI line are kept in memory in advance, and the SPI controller will automatically read the data from memory.** The SPI_TX_SRC define the memory address from which SPI controller starts to read data.

1100A00C SPI_RX_DST SPI RX Destination Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_RX_DST															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_RX_DST															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SPI_RX_DST**	SPI_RX_DST	**If RX_DMA_EN is set, the received data from the MISO line will be move to memory automatically by the SPI controller.** The SPI_RX_DST define the memory address to which the SPI controller starts to store the data.

1100A010 SPI_TX_DATA SPI TX DATA FIFO 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_TX_DATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_TX_DATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SPI_TX_DATA**	SPI_TX_DATA	**The depth of the TX FIFO is 32-bytes. Write to this register will write 4 bytes to the TX FIFO.** The TX FIFO pointer will automatically move toward the next four bytes. Read from this register will read 4 bytes from the FIFO, and the TX FIFO pointer automatically moves toward the next four bytes.

1100A014 SPI_RX_DATA SPI RX DATA FIFO 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_RX_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_RX_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SPI_RX_DATA**	SPI_RX_DATA	**The depth of the RX FIFO is 32-bytes. Read from this register will read 4 bytes from the RX FIFO.** The RX FIFO pointer will automatically move toward the next four bytes. Write to this register will write 4 bytes to the FIFO, and the RX FIFO pointer automatically moves toward the next four bytes.

1100A018 SPI_CMD SPI Command Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															PAUSE_IE	FINISH_IE
Type															RW	RW
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_ENDIAN	RX_ENDIAN	RXMSBF	TXMSBF	TX_DMA_EN	RX_DMA_EN	CPOL	CPHA	CS_POL	SAMPLE_SEL	CS_DEASSERT_EN	PAUSE_EN		RST	RESUME	CMD_ACT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
17	**PAUSE_IE**	PAUSE_IE	**The interrupt enable bit of pause flag in SPI Status register.**
16	**FINISH_IE**	FINISH_IE	**The interrupt enable bit of finish flag in SPI Status register.**
15	**TX_ENDIAN**	TX_ENDIAN	**This bit defines whether to reverse the endian order of the data DMA from memory.** Default (0) is not to reverse. Only support DMA mode.
14	**RX_ENDIAN**	RX_ENDIAN	**This bit defines whether to reverse the endian order of the data DMA to memory.** Default (0) is not to reverse.
13	**RXMSBF**	RXMSBF	**Indicate the data received from MISO line is MSB first or not. Set RXMSBF to 1 for MSB first, otherwise set it to 0.**
12	**TXMSBF**	TXMSBF	**Indicate the data sent on MOSI line is MSB first or not.** Set TXMSBF to 1 for MSB first, otherwise set it to 0.
11	**TX_DMA_EN**	TX_DMA_EN	**This bit is the DMA mode enable bit of the data to be transmitted. Default (0) is not to enable.**
10	**RX_DMA_EN**	RX_DMA_EN	**This bit is the DMA mode enable bit of the data being received. Default (0) is not to enable.**
9	**CPOL**	CPOL	**This bit is the control bit of the SCK polarity. 0 is CPOL = 0, 1 is CPOL = 1.**
8	**CPHA**	CPHA	**This bit defines the SPI Clock Format 0 or SPI Clock Format 1 during transmission.** 0 is CPHA = 0, 1 is CPHA = 1.
7	**CS_POL**	CS_POL	**This bit is the control bit of chip select polarity.** 0 is active low. 1 is active high
6	**SAMPLE_SEL**	SAMPLE_SEL	**This bit is the control bit of sample edge of miso.** 0 is postive edge. 1 is negative edge
5	**CS_DEASSERT_EN**	CS_DEASSERT_EN	**This bit is the enable bit of the chip select de-assertion mode** Set 1 to enable this mode.
4	**PAUSE_EN**	PAUSE_EN	**This bit is the enable bit of the pause mode.** Set 1 to enable this mode.
2	**RST**	RST	**The software reset bit. When this bit is 1, software reset is active high.** The default value is 0.
1	**RESUME**	RESUME	**This bit is used when controller is in PAUSE IDLE state.** Write 1 to this bit triggers the SPI controller resume transfer from PAUSE IDLE state.
0	**CMD_ACT**	CMD_ACT	**The command activate bit.** Write 1 to this bit triggers the SPI controller starts the transaction.

1100A01C SPI_STATUS0 SPI Status 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**PAUSE**	**FINISH**
Type															RC	RC
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	**PAUSE**	PAUSE	**The interrupt status bit in pause mode.** It will be set by the SPI controller when it completes the transaction, entering the PAUSE IDLE state.
0	**FINISH**	FINISH	**The interrupt status bit in non-pause mode.** It will be set by the SPI controller when it completes the transaction, entering the IDLE state.

1100A020 SPI_STATUS1 SPI Status 1 Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BUSY
Type																RO
Reset																1

Bit(s)	Mnemonic	Name	Description
0	**BUSY**	BUSY	**This status flag reflects the SPI controller is busy or not.** This bit is low active, i.e. 0 represents the SPI controller is busy now. 1'b1:idle 1'b0:busy

1100A024 SPI_PAD_MACRO_SEL SPI pad_macro selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PAD_MACRO_SEL		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0	**PAD_MACRO_SEL**	PAD_MACRO_SEL	Selects PAD group spi to use

1100A028 SPI_CFG2 SPI Configuration 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SCK_LOW_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCK_HIGH_COUNT															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	**SCK_LOW_COUNT**	SCK_LOW_COUNT	The SCK clock low time = (SCK_LOW_COUNT+1) * CLK_PERIOD.
15:0	**SCK_HIGH_COUNT**	SCK_HIGH_COUNT	The SCK clock high time = (SCK_HIGH_COUNT+1) * CLK_PERIOD.

3.8 AUXADC

Module name: AUXADC Base address: (+11001000h)

Address	Name	Width	Register Function
11001000	AUXADC_CON0	32	AUXADC Control Register 0
11001004	AUXADC_CON1	32	AUXADC Control Register 1
11001008	AUXADC_CON1_SET	32	AUXADC Control Set Register 1
1100100C	AUXADC_CON1_CLR	32	AUXADC Control Clear Register 1
11001010	AUXADC_CON2	32	AUXADC Control Register 2
11001014~ 11001050	AUXADC_DAT[n] (n=0~15)	32	AUXADC Channel n Register
11001054	AUXADC_TS_DEBT0	32	Touch Screen Debounce Time 0
11001058	AUXADC_TS_DEBT1	32	Touch Screen Debounce Time 1
1100105C	AUXADC_TS_CMD	32	Touch Screen Sample Command
11001060	AUXADC_TS_ADDR	32	Touch Screen Sample Address
11001064	AUXADC_TS_CON0	32	Touch Screen Control 0
11001068	AUXADC_TS_CON1	32	Touch Screen Control 1
1100106C	AUXADC_TS_CON2	32	Touch Screen Control 2
11001070	AUXADC_TS_CON3	32	Touch Screen Control 3 (Removed)
11001074	AUXADC_TS_DAT0	32	Touch Screen Sample Data 0
11001078	AUXADC_TS_DAT1	32	Touch Screen Sample Data 1
1100107C	AUXADC_TS_DAT2	32	Touch Screen Sample Data 2
11001080	AUXADC_TS_DAT3	32	Touch Screen Sample Data 3
11001084	AUXADC_DET_VOLT	32	AUXADC Background Detected Control
11001088	AUXADC_DET_SEL	32	AUXADC Background Detected Channel
1100108C	AUXADC_DET_PERIOD	32	Background Detection Period
11001090	AUXADC_DET_DEBT	32	Background Detection Debounce
11001094	AUXADC_MISC	32	AUXADC Misc Control
11001098	AUXADC_ECC	32	AUXADC ECC Control (Removed)
1100109C	AUXADC_SAMPLE_LIST	32	AUXADC Sample List
110010A0	AUXADC_ABIST_PERIOD	32	AUXADC ABIST Control
110010A4	AUXADC_TST	32	AUXADC Test Control
110010B0	AUXADC_SPL_EN	32	AUXADC SPL Enable
110010B4	AUXADC_SPL_CFG0	32	AUXADC SPL Config 0
110010B8	AUXADC_SPL_CFG1	32	AUXADC SPL Config 1
110010BC	AUXADC_SPL_CFG2	32	AUXADC SPL Config 2
110010C0	AUXADC_SPL_CFG3	32	AUXADC SPL Config 3
110010C4	AUXADC_SPL_CFG4	32	AUXADC SPL Config 4
110010C8	AUXADC_SPL_CFG5	32	AUXADC SPL Config 5
110010CC	AUXADC_SPL_CFG6	32	AUXADC SPL Config 6
110010D0	AUXADC_SPL_CFG7	32	AUXADC SPL Config 7
11001100	AUXADC_TS_RAW_CON	32	AUXADC TS RAW Batch Control

Address	Name	Width	Register Function
11001104	AUXADC_TS_AUTO_TIME_INTVL	32	AUXADC TS Auto Time Interval
11001108	AUXADC_AUXIF_CFG0	32	AUXADC AUXIF Config 0
1100110C	AUXADC_AUXIF_CFG1	32	AUXADC AUXIF Config 1
11001200~1100121C	AUXADC_TS_RAW_X_DAT[n] (n=0~7)	32	AUXADC TS RAW Batch X_DATn
11001220~1100123C	AUXADC_TS_RAW_Y_DAT[n] (n=0~7)	32	AUXADC TS RAW Batch Y_DATn
11001240~1100125C	AUXADC_TS_RAW_Z1_DAT[n] (n=0~7)	32	AUXADC TS RAW Batch Z1_DATn
11001260~1100127C	AUXADC_TS_RAW_Z2_DAT[n] (n=0~7)	32	AUXADC TS RAW Batch Z2_DATn

11001000 AUXADC_CON AUXADC Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOSET15	AUTOSET14	AUTOSET13	AUTOSET12	AUTOSET11	AUTOSET10	AUTOSET9	AUTOSET8	AUTOSET7	AUTOSET6	AUTOSET5	AUTOSET4	AUTOSET3	AUTOSET2	AUTOSET1	AUTOSET0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**AUTOSET15**	AUTOSET15	**Enables auto set for CH15** 0: Not AUTOSET mode 1: AUTOSET mode
14	**AUTOSET14**	AUTOSET14	**Enables auto set for CH14** 0: Not AUTOSET mode 1: AUTOSET mode
13	**AUTOSET13**	AUTOSET13	**Enables auto set for CH13** 0: Not AUTOSET mode 1: AUTOSET mode
12	**AUTOSET12**	AUTOSET12	**Enables auto set for CH12** 0: Not AUTOSET mode 1: AUTOSET mode
11	**AUTOSET11**	AUTOSET11	**Enables auto set for CH11** 0: Not AUTOSET mode 1: AUTOSET mode
10	**AUTOSET10**	AUTOSET10	**Enables auto set for CH10** 0: Not AUTOSET mode 1: AUTOSET mode
9	**AUTOSET9**	AUTOSET9	**Enables auto set for CH09** 0: Not AUTOSET mode 1: AUTOSET mode

Bit(s)	Mnemonic	Name	Description
8	**AUTOSET8**	AUTOSET8	**Enables auto set for CH08** 0: Not AUTOSET mode 1: AUTOSET mode
7	**AUTOSET7**	AUTOSET7	**Enables auto set for CH07** 0: Not AUTOSET mode 1: AUTOSET mode
6	**AUTOSET6**	AUTOSET6	**Enables auto set for CH06** 0: Not AUTOSET mode 1: AUTOSET mode
5	**AUTOSET5**	AUTOSET5	**Enables auto set for CH05** 0: Not AUTOSET mode 1: AUTOSET mode
4	**AUTOSET4**	AUTOSET4	**Enables auto set for CH04** 0: Not AUTOSET mode 1: AUTOSET mode
3	**AUTOSET3**	AUTOSET3	**Enables auto set for CH03** 0: Not AUTOSET mode 1: AUTOSET mode
2	**AUTOSET2**	AUTOSET2	**Enables auto set for CH02** 0: Not AUTOSET mode 1: AUTOSET mode
1	**AUTOSET1**	AUTOSET1	**Enables auto set for CH01** 0: Not AUTOSET mode 1: AUTOSET mode
0	**AUTOSET0**	AUTOSET0	**Enables auto set for CH00** 0: Not AUTOSET mode 1: AUTOSET mode

11001004 AUXADC_CON1 **AUXADC Control Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**IMM15**	**IMM14**	**IMM13**	**IMM12**	**IMM11**	**IMM10**	**IMM9**	**IMM8**	**IMM7**	**IMM6**	**IMM5**	**IMM4**	**IMM3**	**IMM2**	**IMM1**	**IMM0**
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**IMM15**	IMM15	**Channel 15 immediate mode** 0: Channel 15 is not selected. 1: Channel 15 is selected.
14	**IMM14**	IMM14	**Channel 14 immediate mode** 0: Channel 14 is not selected. 1: Channel 14 is selected.
13	**IMM13**	IMM13	**Channel 13 immediate mode** 0: Channel 13 is not selected. 1: Channel 13 is selected.
12	**IMM12**	IMM12	**Channel 12 immediate mode** 0: Channel 12 is not selected. 1: Channel 12 is selected.
11	**IMM11**	IMM11	**Channel 11 immediate mode**

Bit(s)	Mnemonic	Name	Description
			0: Channel 11 is not selected. 1: Channel 11 is selected.
10	**IMM10**	IMM10	**Channel 10 immediate mode** 0: Channel 10 is not selected. 1: Channel 10 is selected.
9	**IMM9**	IMM9	**Channel 9 immediate mode** 0: Channel 9 is not selected. 1: Channel 9 is selected.
8	**IMM8**	IMM8	**Channel 8 immediate mode** 0: Channel 8 is not selected. 1: Channel 8 is selected.
7	**IMM7**	IMM7	**Channel 7 immediate mode** 0: Channel 7 is not selected. 1: Channel 7 is selected.
6	**IMM6**	IMM6	**Channel 6 immediate mode** 0: Channel 6 is not selected. 1: Channel 6 is selected.
5	**IMM5**	IMM5	**Channel 5 immediate mode** 0: Channel 5 is not selected. 1: Channel 5 is selected.
4	**IMM4**	IMM4	**Channel 4 immediate mode** 0: Channel 4 is not selected. 1: Channel 4 is selected.
3	**IMM3**	IMM3	**Channel 3 immediate mode** 0: Channel 3 is not selected. 1: Channel 3 is selected.
2	**IMM2**	IMM2	**Channel 2 immediate mode** 0: Channel 2 is not selected. 1: Channel 2 is selected.
1	**IMM1**	IMM1	**Channel 1 immediate mode** 0: Channel 1 is not selected. 1: Channel 1 is selected.
0	**IMM0**	IMM0	**Channel 0 immediate mode** 0: Channel 0 is not selected. 1: Channel 0 is selected.

11001008 AUXADC_CON1_SET AUXADC Control Set Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SET12	SET11	SET10	SET9	SET8	SET7	SET6	SET5	SET4	SET3	SET2	SET1	SET0
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12	**SET12**	SET12	Sets up Channel 12 immediate mode
11	**SET11**	SET11	Sets up Channel 11 immediate mode
10	**SET10**	SET10	Sets up Channel 10 immediate mode
9	**SET9**	SET9	Sets up Channel 9 immediate mode

Bit(s)	Mnemonic	Name	Description
8	**SET8**	SET8	Sets up Channel 8 immediate mode
7	**SET7**	SET7	Sets up Channel 7 immediate mode
6	**SET6**	SET6	Sets up Channel 6 immediate mode
5	**SET5**	SET5	Sets up Channel 5 immediate mode
4	**SET4**	SET4	Sets up Channel 4 immediate mode
3	**SET3**	SET3	Sets up Channel 3 immediate mode
2	**SET2**	SET2	Sets up Channel 2 immediate mode
1	**SET1**	SET1	Sets up Channel 1 immediate mode
0	**SET0**	SET0	Sets up Channel 0 immediate mode

1100100C AUXADC_CON1_CLR AUXADC Control Clear Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CLR12	CLR11	CLR10	CLR9	CLR8	CLR7	CLR6	CLR5	CLR4	CLR3	CLR2	CLR1	CLR0
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12	**CLR12**	CLR12	Clears Channel 12 immediate mode
11	**CLR11**	CLR11	Clears Channel 11 immediate mode
10	**CLR10**	CLR10	Clears Channel 10 immediate mode
9	**CLR9**	CLR9	Clears Channel 9 immediate mode
8	**CLR8**	CLR8	Clears Channel 8 immediate mode
7	**CLR7**	CLR7	Clears Channel 7 immediate mode
6	**CLR6**	CLR6	Clears Channel 6 immediate mode
5	**CLR5**	CLR5	Clears Channel 5 immediate mode
4	**CLR4**	CLR4	Clears Channel 4 immediate mode
3	**CLR3**	CLR3	Clears Channel 3 immediate mode
2	**CLR2**	CLR2	Clears Channel 2 immediate mode
1	**CLR1**	CLR1	Clears Channel 1 immediate mode
0	**CLR0**	CLR0	Clears Channel 0 immediate mode

11001010 AUXADC_CON2 AUXADC Control Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_TS_STATUS_EN	NEW_SPL_SHREF_EN	NEW_DFMB_EN	NEW_SHREF_PWDB_EN	EN_PUWAIT	DUAL_TOUCH_EN			SOFT_RST							ADC_STA
Type	RW	RW	RW	RW	RW	RW			RW							RO
Reset	0	0	0	0	0	0			0							0

Bit(s)	Mnemonic	Name	Description
15	**OLD_TS_STATUS_EN**	OLD_TS_STATUS_ EN	**Uses old TS STATUS logic (MT6575 method)** 0: Disable 1: Enable
14	**NEW_SPL_SHREF_EN**	NEW_SPL_SHREF_ EN	**Uses new logic** 0: Disable 1: Enable
13	**NEW_DFMB_EN**	NEW_DFMB_EN	**Uses new logic** 0: Disable 1: Enable
12	**NEW_SHREF_PWDB_EN**	NEW_SHREF_PWDB _EN	**Uses new logic** 0: Disable 1: Enable
11	**PUW**	EN_PUWAIT	**Enables power warm-up** This field enables the power warm-up period to ensure power stability before the SAR process takes place. It is unnecessary to activate this field. The warm-up period is about 56 ADC clock cycles. 0: Does not enable 1: Enable
10	**DUAL_TOUCH_EN**	DUAL_TOUCH_EN	**Enables dual touch** 0: Disable 1: Enable
7	**RST**	SOFT_RST	**Software resets AUXADC FSM.**
0	**STA**	ADC_STA	**ADC status of AUXADC** 0: Idle status 1: Busy status

11001014~11001050 AUXADC_DAT[n](n=0~15) — **AUXADC Channel n Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**RDYn**	**DATn**											
Type				RO	RO											
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12	**RDY0**	RDYn	**AUXADC channel n data ready** Cleared after the register is read. 0: Not ready 1: Ready
11:0	**DAT0**	DATn	**AUXADC channel n data** Stores the sampled data for channel n.

11001054 AUXADC_TS_DEBT0 — **Touch Screen Debounce Time 0** — **00002000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			TS_DEB_TIME0													
Type			RW													
Reset			1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13:0	**DEB0**	TS_DEB_TIME0	**TS de-bounce time 0** When the analog touch screen IRQ signal is set from low to high, AUXADC will issue an interrupt after the de-bounce time. De-bounce time = (TS_DEB_TIME0*30) us

11001058 AUXADC_TS_DEBT1 Touch Screen Debounce Time 1 00002000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			TS_DEB_TIME1													
Type			RW													
Reset			1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13:0	**DEB1**	TS_DEB_TIME1	**TS de-bounce time 1** When the analog touch screen IRQ signal is set from high to low, AUXADC will issue an interrupt after the de-bounce time. De-bounce time = (TS_DEB_TIME1*30) us

1100105C AUXADC_TS_CMD Touch Screen Sample Command 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TS_MODE	TS_SEDF	TS_PD	
Type													RW	RW	RW	
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3	**MODE**	TS_MODE	**Selects TS sample bits** Select the sample resolution. 0: 12-bit resolution 1: 10-bit resolution
2	**SEDF**	TS_SEDF	**Selects TS single differential**

Bit(s)	Mnemonic	Name	Description
			Mode selection 0: Differential mode 1: single-end mode
1:0	**PD**	TS_PD	**TS power-down mode** Powers down control for analog IRQ signal and touch screen sample control signal. 2'b00: Turn on Y-_drive signal and PDN_sh_ref 2'b01: Turn on PDN_IRQ and PDN_sh_ref 2'b10: Reserved 2'b11: Turn on PDN_IRQ

11001060 AUXADC_TS_ADDR Touch Screen Sample Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														TS_ADDRESS		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0	**ADR**	TS_ADDRESS	**TS address** Defines which x, y or z data to sample. 3'b001: Y position 3'b011: Z1 position 3'b100: Z2 position 3'b101: X position Others: Reserved

11001064 AUXADC_TS_CON0 Touch Screen Control 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQSEL														TS_STATUS	TS_TIRGGER
Type	RW														A1	RW
Reset	0														0	0

Bit(s)	Mnemonic	Name	Description
15	**IRQSEL**	IRQSEL	**Selects PENIRQ interrupt** 0: Interrupt occurs when touch screen is touched and released. 1: Interrupt occurs only when touch screen is released.
1	**STS**	TS_STATUS	**Touch screen status that is only valid when IRQ**

Bit(s)	Mnemonic	Name	Description
			is accepted 0: Not touched 1: Touched
0	**TRG**	TS_TIRGGER	**Triggers touch screen sample** 0: No action 1: When SW writes 1, AUXADC will trigger the touch screen process. After the finish of the sampling process of touch screen, this bit will be de-asserted.

11001068 AUXADC_TS_CON1 Touch Screen Control 1 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TS_FAV_DELAY								TS_FAV_EN	TS_FAV_COORD_SEL		INVALID	ADD_TWO_SAMPLE	FAVSEL	TS_FAV_ACC_LOOPCNT	
Type	RW								RW	RW		W1C	RW	RW	RW	
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**ADEL**	TS_FAV_DELAY	**TS FAV-Batch mode latency** Delay time between each loop of FAV-Batch mode sampling 8'd0: Add 0 T then start another loop 8'd255: Add 255 T then start another loop
7	**FAVEN**	TS_FAV_EN	**Enables TS FAV-Batch mode** Enables touch screen FAV-Batch mode by setting this bit to 1. When the loop is finshed, it will be de-asserted 0: FAV-Batch mode does not act. 1: FAV-Batch mode acts.
6:5	**COORDSEL**	TS_FAV_COORD_S EL	**Selects TS FAV-Batch mode coordinate** If this register is set to 2'b00, the result will be put to TS_DAT0. If this register is set to 2'b10 or 2'b11, the result will be put to TS_DAT0, TS_DAT1 respectively. If this register is set to 2'b01, the result will be put to TS_DAT0, TS_DAT1, TS_DAT2 and TS_DAT3 respectively. 2'b00: Use AUXADC_TS_ADDR as sample address. Only one address is used. 2'b01: Sample address sequence = X -> Y -> Z1 -> Z2 2'b10: Sample address sequence = X1 -> Y1 -> X2 -> Y2 2'b11: Sample address sequence = Z1 -> Z2
4	**INVALID**	INVALID	**Invalid flag indicating that PENIRQ goes to high and AUXADC is debouncing in FAV-Batch mode,Raw-Bathc mode or auto-fetch sampling** The flag is write-clear. 0: Does not occur 1: Occur (write-clear)
3	**ASAMP**	ADD_TWO_SAMPLE	**Enables additional two samples** If TS_FAV_EN is on, the loop count will be TS_FAV_ACC_LOOPCNT+2, and the maximum and minimum sample will be discarded.

Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable
2	**FAVSEL**	FAVSEL	**Selects TS FAV-Batch mode trigger** 0: Software trigger 1: Hardware automatic time trigger
1:0	**LCNT**	TS_FAV_ACC_LOOPCNT	**Selects TS FAV-Batch mode accumulation mode** If TS_FAV_EN is on and the loop count is selected, the result will be averaged and put to dedicated TS_DATX registers. 2'b00: Auto sequential mode is repeated for 1 time. 2'b01: Auto sequential mode is repeated for 4 times. 2'b10: Auto sequential mode is repeated for 8 times. 2'b11: Auto sequential mode is repeated for 16 times.

1100106C AUXADC_TS_CON2 **Touch Screen Control 2** **00000020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								SPLNUM_TS_EN	SPLNUM_TS							
Type								RW	RW							
Reset								0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8	**SPLNUM_TS_EN**	SPLNUM_TS_EN	**Enables TS SPL signal duration extension** 0: Disable. SPL duration will be 4T of AUXADC clock only. 1: Enable. Use this register for SPL duration
7:0	**SPLNUM_TS**	SPLNUM_TS	**TS SPL/XX_DRV signal duration** 7'd0: Reserved 7'd1: SPL and YP/XP/YM/XM_DRV period = (1+3)T of AUXADC clock 7'd255: SPL and YP/XP/YM/XM_DRV period = (255+3)T of AUXADC clock

11001070 AUXADC_TS_CON3 **Touch Screen Control 3 (Removed)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PULLSEL															
Type	RW															
Reset	0															

Bit(s)	Mnemonic	Name	Description
15	**PULLSEL**	PULLSEL	**Pull-up resistance** 0: 55K ohm 1: 90K ohm

11001074 AUXADC_TS_DAT0 Touch Screen Sample Data 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TS_DAT0											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0	**TDAT0**	TS_DAT0	**TS data register 0** Stores the touch screen sample data 0 and is also used to store data from A/D in TS sample mode (TS_FAV_EN =0). After the auto sequential mode is finished, the 10/12-bit result will be stored in this register [9:0]/[11:0] as normal operation. If the sample mode is 12-bit, the 12-bit data will be stored in the register [11:0]. If the sample mode is 10-bit, the 10-bit data will be stored in the register [9:0].

11001078 AUXADC_TS_DAT1 Touch Screen Sample Data 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TS_DAT1											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0	**TDAT1**	TS_DAT1	**TS data register 1** Stores the touch screen sample data 1 and is also used to store data from A/D in TS sample mode (TS_FAV_EN =0). After the auto sequential mode is finished, the10/12-bit result will be stored in this register [9:0]/[11:0] as normal operation. If the sample mode is 12-bit, the 12-bit data will be stored in the register [11:0]. If the sample mode is 10-bit, the 10-bit data will be stored in the register [9:0].

1100107C AUXADC_TS_DAT2 Touch Screen Sample Data 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TS_DAT2											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0	**TDAT2**	TS_DAT2	**TS data register 2** Stores the touch screen sample data 2 and is also used to store data from A/D in TS sample mode (TS_FAV_EN =0). After the auto sequential mode is finished, the 10/12-bit result will be stored in this register [9:0]/[11:0] as normal operation. If the sample mode is 12-bit, the 12-bit data will be stored in the register [11:0]. If the sample mode is 10-bit, the 10-bit data will be stored in the register [9:0].

11001080 AUXADC_TS_DAT3 Touch Screen Sample Data 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TS_DAT3											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0	**TDAT3**	TS_DAT3	**TS data register 3** Stores the touch screen sample data 3. After the auto sequential mode is finished, the 10/12-bit result will be stored in this register [9:0]/[11:0] as normal operation. If the sample mode is 12-bit, the 12-bit data will be stored in the register [11:0]. If the sample mode is 10-bit, the 10-bit data will be stored in the register [9:0].

11001084 AUXADC_DET_VOLT AUXADC Background Detected Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INV				VOL											
Type	RW				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**INV**	INV	**Controls background detected** When the battery voltage is higher or lower than pre-defined voltage (VOLT), the interrupt will be issued to AP. 0: Lower 1: Higher
11:0	**VOL**	VOL	

11001088 AUXADC_DET_SEL **AUXADC Background Detected Channel** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CHSEL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**CHSEL**	CHSEL	**Channel to be sampled in background** 0x0: Channel 0 0x1: Channel 1 ... 0x8: Channel 8 Others: Reserved

1100108C AUXADC_DET_PERIOD **Background Detection Period** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			BG_DET_PERIOD													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13:0	**BGDET**	BG_DET_PERIOD	**Background sample period** When this value is not 0, the background detection will be activated automatically and other ADC sampling functions will be stopped. The counter counts by 32K

Bit(s)	Mnemonic	Name	Description
			clock. When counter value is bigger than DET_PERIOD, the detection will be activated.

11001090 AUXADC_DET_DEBT Background Detection Debounce 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			BG_DEBT_TIME													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
13:0	**BGTIME**	BG_DEBT_TIME	**Background de-bounce time** When the number of the detected channel is higher or lower than the pre-defined voltage and exceeds "debounce_time", the interrupt will be issued.

11001094 AUXADC_MISC AUXADC Misc Control 00000008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INVALID_NONSTOP						ECC_EN	EN_TS_AUTO_SAMPLE_AFT_IRQ	DIV							
Type	RW						RW	RW	RW							
Reset	0						0	0	0	0	0	0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**NONSTOP**	INVALID_NONSTO P	**FAV-Batch and RAW-Batch mode will terminate the current sampling when INVALID in AUXADC_TS_CON1 occurs.** 0: Stop 1: Non-stop
9	**ECC_EN**	ECC_EN	**Enables ADC ECC control** AUXADC_ECC controls the bit to do ECC. 0: Disable 1: Enable
8	**ENASAMP**	EN_TS_AUTO_SAMPLE_AFT_IRQ	**Auto samples TS data when ts_irq_ana is asserted** 0: Disable 1: Enable

Bit(s)	Mnemonic	Name	Description
7:0	**DIV**	DIV	**Internal divide count value** 0x0~3: Reserved. Should not be used. 0x4: A/D clock = 26MHz clock/4 0x5: A/D clock = 26MHz clock/5 0x6: A/D clock = 26MHz clock/6 0x7: A/D clock = 26MHz clock/7 0x8: A/D clock = 26MHz clock/8 = 3.25MHz (default) 0x9 ~ 0xFF: Programmable

11001098 AUXADC_ECC AUXADC ECC Control (Removed) 00000081

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SAMPLE_LIST16								ECC1				ECCo			
Type	RO								RW				RW			
Reset	0								1	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
15	**SAMPLE_LIST16**	SAMPLE_LIST16	Sample list bit 16 (TS sample)
7:4	**ECC1**	ECC1	
3:0	**ECCo**	ECCo	

1100109C AUXADC_SAMPLE_LIST AUXADC Sample List 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SAMPLE_LIST															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**SAMPLE_LIST**	SAMPLE_LIST	Hardware sample list for debugging

110010A0 AUXADC_ABIST_PERIOD AUXADC ABIST Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TP_ABIST_EN	ABIST_MODE_EN								ABIST_SPL_PERIOD						
Type	RW	RW								RW						
Reset	0	0								0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**EN**	TP_ABIST_EN	**Enables touch panel ABIST mode** TP will sample when TP_ABIST_EN=1 and ABIST_MODE_EN=1. 0: Disable 1: Enable
14	**MODE_EN**	ABIST_MODE_EN	**Enables ABIST mode** 0: Disable 1: Enable
6:0	**PERIOD**	ABIST_SPL_PERI OD	**Period of two different samples** One period is a ADC clock.

110010A4 AUXADC_TST AUXADC Test Control 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_AUTORP T_PRD													AUXADC_AUTORPT_EN	AUXADC_TEST_SEL	AUXADC_TEST_MODE
Type	RW													RW	RW	RW
Reset	0	0	0	0	0	0	0	1						0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**AUXADC_AUTORPT_PRD**	AUXADC_AUTORPT_PRD	**Period of auto-start**
2	**AUXADC_AUTORPT_EN**	AUXADC_AUTORPT_EN	**Enables AUXADC auto start mode_x000D_** 0: Disable 1: Enable
1	**AUXADC_TEST_SEL**	AUXADC_TEST_SE L	**Selects AUXADC test mode_x000D_** 0: In test mode. CHSEL from GPI 1: In test mode. CHSEL from REG
0	**AUXADC_TEST_MODE**	AUXADC_TEST_MO DE	**Enables AUXADC test mode_x000D_** 0: Disable. Normal mode 1: Enable. Use auxadc_test_in from GPI

110010B0 AUXADC_SPL_EN AUXADC SPL Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPLNUM_AUX15_EN	SPLNUM_AUX14_EN	SPLNUM_AUX13_EN	SPLNUM_AUX12_EN	SPLNUM_AUX11_EN	SPLNUM_AUX10_EN	SPLNUM_AUX09_EN	SPLNUM_AUX08_EN	SPLNUM_AUX07_EN	SPLNUM_AUX06_EN	SPLNUM_AUX05_EN	SPLNUM_AUX04_EN	SPLNUM_AUX03_EN	SPLNUM_AUX02_EN	SPLNUM_AUX01_EN	SPLNUM_AUX00_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**SPLNUM_AUX15_EN**	SPLNUM_AUX15_EN	**Enables AUX15 SPL signal duration extension_x000D_** 0: Disable. SPL duration will be 4T of AUXADC clock only._x000D_ 1: Enable. Use SPLNUM_AUX15 for this register for SPL duration.
14	**SPLNUM_AUX14_EN**	SPLNUM_AUX14_EN	**Enables AUX14 SPL signal duration extension_x000D_** 0: Disable. SPL duration will be 4T of AUXADC clock only_x000D_. 1: Enable. Use SPLNUM_AUX14 for this register for SPL duration.
13	**SPLNUM_AUX13_EN**	SPLNUM_AUX13_EN	**Enables AUX13 SPL signal duration extension_x000D_** 0: Disable. SPL duration will be 4T of AUXADC clock only_x000D_. 1: Enable. Use SPLNUM_AUX13 for this register for SPL duration.
12	**SPLNUM_AUX12_EN**	SPLNUM_AUX12_EN	**Enables AUX12 SPL signal duration extension_x000D_** 0: Disable. SPL duration will be 4T of AUXADC clock only_x000D_. 1: Enable. Use SPLNUM_AUX12 for this register for SPL duration.
11	**SPLNUM_AUX11_EN**	SPLNUM_AUX11_EN	**Enables AUX11 SPL signal duration extension_x000D_** 0: Disable. SPL duration will be 4T of AUXADC clock only_x000D_. 1: Enable. Use SPLNUM_AUX11 for this register for SPL duration.
10	**SPLNUM_AUX10_EN**	SPLNUM_AUX10_EN	**Enables AUX10 SPL signal duration extension_x000D_** 0: Disable. SPL duration will be 4T of AUXADC clock only_x000D_. 1: Enable. Use SPLNUM_AUX10 for this register for SPL duration.
9	**SPLNUM_AUX09_EN**	SPLNUM_AUX09_EN	**Enables AUX09 SPL signal duration extension_x000D_** 0: Disable. SPL duration will be 4T of AUXADC clock only_x000D_. 1: Enable. Use SPLNUM_AUX09 for this register for SPL duration.
8	**SPLNUM_AUX08_EN**	SPLNUM_AUX08_EN	**Enables AUX08 SPL signal duration extension_x000D_** 0: Disable. SPL duration will be 4T of AUXADC clock only_x000D_. 1: Enable. Use SPLNUM_AUX08 for this register for SPL duration.
7	**SPLNUM_AUX07_E**	SPLNUM_AUX07_EN	**Enables AUX07 SPL signal duration**

Bit(s)	Mnemonic	Name	Description
	N		**extension_x000D_** 0: Disable. SPL duration will be 4T of AUXADC clock only_x000D_. 1: Enable. Use SPLNUM_AUX07for this register for SPL duration.
6	**SPLNUM_AUX06_EN**	SPLNUM_AUX06_EN	**Enables AUX06 SPL signal duration extension_x000D_** 0: Disable. SPL duration will be 4T of AUXADC clock only_x000D_. 1: Enable. Use SPLNUM_AUX06 for this register for SPL duration.
5	**SPLNUM_AUX05_EN**	SPLNUM_AUX05_EN	**Enables AUX05 SPL signal duration extension_x000D_** 0: Disable. SPL duration will be 4T of AUXADC clock only_x000D_. 1: Enable. Use SPLNUM_AUX05 for this register for SPL duration.
4	**SPLNUM_AUX04_EN**	SPLNUM_AUX04_EN	**Enables AUX04 SPL signal duration extension_x000D_** 0: Disable. SPL duration will be 4T of AUXADC clock only_x000D_. 1: Enable. Use SPLNUM_AUX04 for this register for SPL duration.
3	**SPLNUM_AUX03_EN**	SPLNUM_AUX03_EN	**Enables AUX03 SPL signal duration extension_x000D_** 0: Disable. SPL duration will be 4T of AUXADC clock only_x000D_. 1: Enable. Use SPLNUM_AUX03 for this register for SPL duration.
2	**SPLNUM_AUX02_EN**	SPLNUM_AUX02_EN	**Enables AUX02 SPL signal duration extension_x000D_** 0: Disable. SPL duration will be 4T of AUXADC clock only_x000D_. 1: Enable. Use SPLNUM_AUX02 for this register for SPL duration.
1	**SPLNUM_AUX01_EN**	SPLNUM_AUX01_EN	**Enables AUX01 SPL signal duration extension_x000D_** 0: Disable. SPL duration will be 4T of AUXADC clock only_x000D_. 1: Enable. Use SPLNUM_AUX01 for this register for SPL duration.
0	**SPLNUM_AUX00_EN**	SPLNUM_AUX00_EN	**Enables AUX00 SPL signal duration extension_x000D_** 0: Disable. SPL duration will be 4T of AUXADC clock only_x000D_. 1: Enable. Use SPLNUM_AUX00 for this register for SPL duration.

110010B4 AUXADC_SPL_CFG0 AUXADC SPL Config 0 00002020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SPLNUM_AUX01**								**SPLNUM_AUX00**							
Type	RW								RW							

Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**SPLNUM_AUX01**	SPLNUM_AUX01	
7:0	**SPLNUM_AUX00**	SPLNUM_AUX00	

110010B8 AUXADC_SPL_CFG1 AUXADC SPL Config 1 00002020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPLNUM_AUX03								SPLNUM_AUX02							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**SPLNUM_AUX03**	SPLNUM_AUX03	
7:0	**SPLNUM_AUX02**	SPLNUM_AUX02	

110010BC AUXADC_SPL_CFG2 AUXADC SPL Config 2 00002020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPLNUM_AUX05								SPLNUM_AUX04							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**SPLNUM_AUX05**	SPLNUM_AUX05	
7:0	**SPLNUM_AUX04**	SPLNUM_AUX04	

110010C0 AUXADC_SPL_CFG3 AUXADC SPL Config 3 00002020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPLNUM_AUX07								SPLNUM_AUX06							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**SPLNUM_AUX07**	SPLNUM_AUX07	
7:0	**SPLNUM_AUX06**	SPLNUM_AUX06	

110010C4 AUXADC_SPL_CFG4 **AUXADC SPL Config 4** **00002020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPLNUM_AUX09								SPLNUM_AUX08							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**SPLNUM_AUX09**	SPLNUM_AUX09	
7:0	**SPLNUM_AUX08**	SPLNUM_AUX08	

110010C8 AUXADC_SPL_CFG5 **AUXADC SPL Config 5** **00002020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPLNUM_AUX11								SPLNUM_AUX10							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**SPLNUM_AUX11**	SPLNUM_AUX11	
7:0	**SPLNUM_AUX10**	SPLNUM_AUX10	

110010CC AUXADC_SPL_CFG6 **AUXADC SPL Config 6** **00002020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPLNUM_AUX13								SPLNUM_AUX12							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**SPLNUM_AUX13**	SPLNUM_AUX13	

Bit(s)	Mnemonic	Name	Description
7:0	**SPLNUM_AUX12**	SPLNUM_AUX12	

110010D0 AUXADC_SPL_CFG7 AUXADC SPL Config 7 00002020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPLNUM_AUX15								SPLNUM_AUX14							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**SPLNUM_AUX15**	SPLNUM_AUX15	
7:0	**SPLNUM_AUX14**	SPLNUM_AUX14	

11001100 AUXADC_TS_RAW_CON AUXADC TS RAW Batch Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RAW_BATCH_EN	START	ABORT
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	**EN**	RAW_BATCH_EN	**Used in touch panel Raw-batch mode sampling mode** When the function is enabled, hardware will auto sample touch panel values according to the sample interval TS_AUTO_COUNT. It will sample 8 times for X/Y/Z1/Z2 position.
1	**START**	START	**Triggers RAW-batch mode sample** The read value is only valid in RAW-batch mode.
0	**ABORT**	ABORT	**Aborts RAW-batch mode sample**

11001104 AUXADC_TS_AUTO_TIME_INTVL AUXADC TS Auto Time Interval 000000A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							TS_AUTO_COUNT									
Type							RW									
Reset							0	0	1	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
9:0	**TS_AUTO_COUNT**	TS_AUTO_COUNT	**Sample interval of the RAW-batch and FAV-batch mode** Default valu: 0xA0*30us = 4.8ms

11001108 AUXADC_AUXIF_CFG0 **AUXADC AUXIF Config 0** **00002020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUXIF_AUTORPT_PRD								RG_AUXIF_AUTORPT_EN	RG_AUXIF_START_NUM					RG_AUXIF_START	RG_AUXIF_RSV
Type	RW								RW	RW					RW	RW
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**TS_AUTO_COUNT**	RG_AUXIF_AUTORPT_PRD	**Period of auto-start for auxif**
7		RG_AUXIF_AUTORPT_EN	**Enables auto start mode_x000D_** 0: Disable 1: Enable
6:2		RG_AUXIF_START_NUM	
1		RG_AUXIF_START	
0		RG_AUXIF_RSV	

1100110C AUXADC_AUXIF_CFG1 **AUXADC AUXIF Config 1** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUXIF_RSV0								RG_AUXIF_RSV1						RG_AUXIF_ST_INV	RG_AUXIF_TEST_MODE
Type	RW								RW						RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
15:8		RG_AUXIF_RSV0	
7:2		RG_AUXIF_RSV1	
1		RG_AUXIF_ST_IN V	**Enables auxif inversion mode_x000D_** 0: High active 1: Low active
0		RG_AUXIF_TEST_ MODE	**Enables auxif test mode_x000D_** 0: Disable. Normal mode 1: Enable. Use auxadc_test_in from GPI

11001200~1100121C **AUXADC_TS_RAW_X_DAT[n](n=0~7)** **AUXADC TS RAW Batch X_DATn** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					X_DATn											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0	**X_DATn**	X_DATn	**Stores 12-bit sampled touch panel X-bias data** Used in touch panel RAW-batch mode sampling.

11001220~1100123C **AUXADC_TS_RAW_Y_DAT[n](n=0~7)** **AUXADC TS RAW Batch Y_DATn** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					Y_DATn											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0	**Y_DATn**	Y_DATn	**Stores 12-bit sampled touch panel Y-bias data** Used in touch panel RAW-batch mode sampling.

11001240~1100125C **AUXADC_TS_RAW_Z1_DAT[n](n=0~7)** **AUXADC TS RAW Batch Z1_DATn** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					Z1_DATn											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0	**Z1_DATn**	Z1_DATn	**Stores 12-bit sampled touch panel Z1-bias data** Used in touch panel RAW-batch mode sampling.

11001260~1100127C **AUXADC_TS_RAW_Z2_DAT[n](n=0~7)** **AUXADC TS RAW Batch Z2_DATn** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					Z2_DATn											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0	**Z2_DATn**	Z2_DATn	**Stores 12-bit sampled touch panel Z2-bias data** Used in touch panel RAW-batch mode sampling.

3.9 I2C/SCCB Controller

Module name: i2c0 Base address: (+11007000h)

Address	Name	Width	Register Function
11007000	DATA_PORT	16	Data Port Register
11007004	SLAVE_ADDR	16	Slave Address Register
11007008	INTR_MASK	16	Interrupt Mask Register
1100700C	INTR_STAT	16	Interrupt Status Register
11007010	CONTROL	16	Control Register
11007014	TRANSFER_LEN	16	Transfer Length Register
11007018	TRANSAC_LEN	16	Transaction Length Register (Number of Transfers per Transaction)
1100701C	DELAY_LEN	16	Inter Delay Length Register
11007020	TIMING	16	Timing Control Register
11007024	START	16	Start Register
11007028	EXT_CONF	16	Extension Configuration Register
11007030	FIFO_STAT	16	FIFO Status Register
11007034	FIFO_THRESH	16	FIFO Thresh Register
11007038	FIFO_ADDR_CLR	16	FIFO Address Clear Register
11007040	IO_CONFIG	16	IO Config Register
11007044	DEBUG	16	Reserved Debug Register
11007048	HS	16	High Speed Mode Register
11007050	SOFTRESET	16	Soft Reset Register
11007054	I2C0_I2CREG_HW_CG_EN	16	HW DCM Enable
11007064	DEBUGSTAT	16	Debug Status Register
11007068	DEBUGCTRL	16	Debug Control Register
1100706C	TRANSFER_LEN_AUX	16	Transfer Length Register (Number of Bytes per Transfer)

11007000 DATA_PORT Data Port Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DATA_PORT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	DATA_PORT	DATA_PORT	**This is the FIFO access port.** During master write sequences (slave_addr[0] = 0), this port can be written by APB. During master read sequences (slave_addr[0] = 1), this port can be read by APB. *Note: Slave_addr should be set correctly before accessing the FIFO.* (For debugging only) If the fifo_apb_debug bit is set,

Bit(s)	Mnemonic	Name	Description
			the FIFO can be read and written by APB.

11007004 SLAVE_ADDR Slave Address Register 000000BF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SLAVE_ADDR							
Type									RW							
Reset									1	0	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
7:0	**SLAVE_ADDR**	SLAVE_ADDR	**Specifies slave address of the device to be accessed** Bit 0 is defined by the I2C protocol as a bit that indicates the direction of transfer. 0: Master write 1: Master read

11007008 INTR_MASK Interrupt Mask Register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SPARE				MAS_ARB_LOST	MAS_HS_NACKER	MAS_ACKERR	MAS_TRANSAC_COMP
Type									RW				RW	RW	RW	RW
Reset									1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
7:4	**Spare**	SPARE	Reserved
3	**MAS_ARB_LOST**	MAS_ARB_LOST	Set this value to 0 to mask ARB_LOST interrupt signal.
2	**MAS_HS_NACKER**	MAS_HS_NACKER	Set this value to 0 to mask HS_NACKERR interrupt signal.
1	**MAS_ACKERR**	MAS_ACKERR	Set this value to 0 to mask ACK_ERR interrupt signal.
0	**MAS_TRANSAC_COMP**	MAS_TRANSAC_COMP	Set this value to 0 to mask TRANSAC_COMP interrupt signal.

1100700C INTR_STAT Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RS_MULTIPLE	ARB_LOST	HS_NACKERR	ACKERR	TRANSAC_COMP
Type												W1C	W1C	W1C	W1C	W1C
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4		RS_MULTIPLE	
3	**ARB_LOST**	ARB_LOST	**This status will be asserted if the I2C controller loses arbition.**
2	**HS_NACKERR**	HS_NACKERR	**This status will be asserted if HS master code NACK error detection is enabled.** If enabled, HS master code NACK ERR will cause transaction to end and stop will be issued.
1	**ACKERR**	ACKERR	**This status will be asserted if ACK error detection is enabled.** If enabled, ACKERR will cause transaction to end and stop will be issued.
0	**TRANSAC_COMP**	TRANSAC_COMP	**This status will be asserted when a transaction has completed successfully.**

11007010 CONTROL Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										TRANSFER_LEN_CHANGE	ACKERR_DET_EN	DIR_CHANGE	CLK_EXT_EN	DMA_EN	RS_STOP	
Type										RW	RW	RW	RW	RW	RW	
Reset										0	0	0	0	0	0	

Bit(s)	Mnemonic	Name	Description
6	**TRANSFER_LEN_CHANGE**	TRANSFER_LEN_CHANGE	**Specifies whether or not to change the transfer length after the fist transfer is completed** If enabled, the transfers after the first transfer will use the transfer_len_aux parameter.
5	**ACKERR_DET_EN**	ACKERR_DET_EN	**Enables slave ACK error detection** When enabled, if slave ACK error is detected, the master should terminate the transaction by issuing a STOP condition then asserting ACKERR interrupt. MCU should handle this case appropriately then reset the FIFO address before reissuing the transaction again. If this option is disabled, the controller will ignore slave ACK error and keep on the scheduled transaction. 0: Disable 1: Enable
4	**DIR_CHANGE**	DIR_CHANGE	**For combined transfer format, where the direction of transfer is to be changed from write to read after the first RS condition** Note: When set to 1, the transfers after the direction

Bit(s)	Mnemonic	Name	Description
			change will be based on the transfer_len_aux parameter. 0: Disable 1: Enable
3	**CLK_EXT_EN**	CLK_EXT_EN	**I2C spec allows slaves to hold the SCL line low if it is not yet ready for further processing.** Therefore, if this bit is set to 1, the master controller will enter a high wait state until the slave releases the SCL line.
2	**DMA_EN**	DMA_EN	**By default, this is disabled and FIFO data should be manually prepared by MCU.** This default setting should be used for transfer sizes of smaller than 8 data bytes and no multiple transfer is configured. When enabled, DMA requests are turned on, and the FIFO data should be prepared in memory.
1	**RS_STOP**	RS_STOP	**In LS/FS mode, this bit affects multi-transfer transaction only.** It controls whether or not REPEATED-START condition is used between transfers. The last ending transfer always ends with a STOP. In HS mode, set this bit to 1. 0: Use STOP 1: Use REPEATED-START

11007014 TRANSFER_LEN Transfer Length Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANSFER_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
15:0		TRANSFER_LEN	**Indicates the number of data bytes to be transferred in one transfer unit (excluding slave address byte)** *Note: Set this value to bigger than 1; otherwise no transfer will take place.*

11007018 TRANSAC_LEN Transaction Length Register (Number of Transfers per Transaction) 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TRANSFER_LEN							
Type									RW							

Reset									0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
7:0	**TRANSFER_LEN**	TRANSFER_LEN	**Indicates the number of transfers to be transferred in one transaction** *Note: Set this value to bigger than 1; otherwise no transfer will take place.*

1100701C DELAY_LEN **Inter Delay Length Register** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DELAY_LEN							
Type									RW							
Reset									0	0	0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0	**DELAY_LEN**	DELAY_LEN	**Sets up wait delay between consecutive transfers when RS_STOP bit is set to 0** The unit is the same as half pulse width.

11007020 TIMING **Timing Control Register** **00001303**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_READ_ADJ	DATA_READ_TIME				SAMPLE_CNT_DIV					STEP_CNT_DIV					
Type	RW	RW				RW					RW					
Reset	0	0	0	1		0	1	1			0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
15	**DATA_READ_ADJ**	DATA_READ_ADJ	**When set to 1, data latch in sampling time during master reads will be adjusted according to DATA_READ_TIME value.** Otherwise, by default data are latched in at half of the high pulse width point. Set this value to smaller than or equal to half the high pulse width.
14:12	**DATA_READ_TIME**	DATA_READ_TIME	**This value is valid only when DATA_READ_ADJ is set to 1.** This can be used to adjust so that data are latched in at earlier sampling points (assuming data is settled by then).
10:8	**SAMPLE_CNT_DIV**	SAMPLE_CNT_DIV	**(For LS/FS only) Adjusts width of each sample** Sample width = sample_cnt_div*1/13MHz

Bit(s)	Mnemonic	Name	Description
5:0	**STEP_CNT_DIV**	STEP_CNT_DIV	**Specifies the number of samples per half pulse width (i.e. each high or low pulse)**

11007024 START **Start Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RS_STOP_MULTIPLE_CONFIG**	**RS_STOP_MULTIPLE_TRIG**	**RS_STOP_MULTIPLE_TRIG_CLR**													**START**
Type	RW	RW	RO													RW
Reset	0	0	0													0

Bit(s)	Mnemonic	Name	Description
15	**RS_STOP_MULTIPLE_CONFIG**	RS_STOP_MULTIPLE_CONFIG	**Enables multiple R/W, length and slave address with rs_stop transfer**
14	**RS_STOP_MULTIPLE_TRIG**	RS_STOP_MULTIPLE_TRIG	**Triggers the next transfer when enabling multiple R/W, length and slave address with rs_stop transfer**
13	**RS_STOP_MULTIPLE_TRIG_CLR**	RS_STOP_MULTIPLE_TRIG_CLR	**Clears rs_stop_mul_trig for the next transfer**
0	**START**	START	**Starts transaction on the bus** It is auto de-asserted at the end of the transaction.

11007028 EXT_CONF **Extension Configuration Register** **00001800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EXT_ TIME**															**EXT_EN**
Type	RW															RW
Reset	0	0	0	1	1	0	0	0								0

Bit(s)	Mnemonic	Name	Description
15:8		EXT_TIME	**Configurable extension time of start condition** Time unit: 1/4*BASE_CLOCK_PERIOD *Note: The max. value is {oxFF-SAMPLE_CNT_DIV}.*
0	**EXT_EN**	EXT_EN	**Used for standard mode only (baud rate is up to 100kHz)** This option decides to perform the extension of start/stop condion. If enbaled, perform the extension; otherwise not. 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable

11007030 FIFO_STAT FIFO Status Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RD_ADDR				WR_ADDR				FIFO_OFFSET						WR_FULL	RD_EMPTY
Type	RO				RO				RO						RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	1

Bit(s)	Mnemonic	Name	Description
15:12	**RD_ADDR**	RD_ADDR	**Current RD address pointer** Only bit [2:0] has physical meaning.
11:8	**WR_ADDR**	WR_ADDR	**Current WR address pointer** Only bit [2:0] has physical meaning.
7:4	**FIFO_OFFSET**	FIFO_OFFSET	**wr_addr[3:0] - rd_addr[3:0]**
1	**WR_FULL**	WR_FULL	**Indicates FIFO is full**
0	**RD_EMPTY**	RD_EMPTY	**Indicates FIFO is empty.**

11007034 FIFO_THRESH FIFO Thresh Register 00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						TX_TRIG_THRESH								RX_TRIG_THRESH		
Type						RW								RW		
Reset						1	1	1						0	0	0

Bit(s)	Mnemonic	Name	Description
10:8	**TX_TRIG_THRESH**	TX_TRIG_THRESH	When TX FIFO level is below this value, TX DMA request will be asserted.
2:0	**RX_TRIG_THRESH**	RX_TRIG_THRESH	When RX FIFO level is above this value, RX DMA request will be asserted.

11007038 FIFO_ADDR_CLR FIFO Address Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name																FIFO_ADDR_CLR
Type																WO
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**FIFO_ADDR_CLR**	FIFO_ADDR_CLR	When written 1, a one pulse fifo_addr_clr will be generated to clear the FIFO address back to 0.

11007040 IO_CONFIG **IO Config Register** **00000003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													IDLE_OE_EN	IO_SYNC_EN	SDA_IO_CONFIG	SCL_IO_CONFIG
Type													RW	RW	RW	RW
Reset													0	0	1	1

Bit(s)	Mnemonic	Name	Description
3	**IDLE_OE_EN**	IDLE_OE_EN	
2	**IO_SYNC_EN**	IO_SYNC_EN	(For debugging only) When set to 1, SCL and SDA inputs will be first dual synced by bclk_ck. This should not be required. Only reserved for debugging.
1	**SDA_IO_CONFIG**	SDA_IO_CONFIG	
0	**SCL_IO_CONFIG**	SCL_IO_CONFIG	

11007044 DEBUG **Reserved Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DEBUG		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0	**DEBUG**	DEBUG	

11007048 HS **High Speed Mode Register** **00000102**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		HS_SAMPLE_CNT_DIV				HS_STEP_CNT_DIV				MASTER_CODE					HS_NACKERR_DET_EN	HS_EN
Type		RW				RW				RW					RW	RW
Reset		0	0	0		0	0	1		0	0	0			1	0

Bit(s)	Mnemonic	Name	Description
14:12	**HS_SAMPLE_CNT_DIV**	HS_SAMPLE_CNT_DIV	**When high-speed mode is entered after the master code transfer has been completed, the sample width will become dependent on this parameter.**
10:8	**HS_STEP_CNT_DIV**	HS_STEP_CNT_DIV	**When high-speed mode is entered after the master code transfer has been completed, the number of samples per half pulse width will become dependent on this value.**
6:4	**MASTER_CODE**	MASTER_CODE	**3-bit programmable value for the master code to be transmitted**
1	**HS_NACKERR_DET_EN**	HS_NACKERR_DET_EN	**Enables NACKERR detection during the master code transmission** When enabled, if NACK is not received after master code has been transmitted, the transaction will be terminated with a STOP condition.
0	**HS_EN**	HS_EN	**Enables high-speed transaction** *Note: Also set rs_stop to 1.*

11007050 SOFTRESET Soft Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SOFT_RESET
Type																WO
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**SOFT_RESET**	SOFT_RESET	When written 1, a one pulse soft reset will be used as synchronous reset to reset the I2C internal hardware circuits.

11007054 I2C0_I2CREG_HW_CG_EN HW DCM Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DCM_EN
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		DCM_EN	**Enables HW DCM function** Default: Disable 0: Disable 1: Enable

11007064 DEBUGSTAT Debug Status Register 00000020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BUS_BUSY	MASTER_WRITE	MASTER_READ	MASTER_STATE				
Type									RO	RO	RO	RO				
Reset									0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7	**BUS_BUSY**	BUS_BUSY	**(For debugging only) Valid when bus_detect_en is 1** 1: Start transaction has been detected and no stop condition has been detected yet.
6	**MASTER_WRITE**	MASTER_WRITE	**For debugging only** 1: Current transfer is in the master write dir.
5	**MASTER_READ**	MASTER_READ	**For debugging only** 1: Current transfer is in the master read dir.
4:0	**MASTER_STATE**	MASTER_STATE	**(For debugging only) Reads back the current master_state** 0: Idle state 1: I2C master is preparing for sending out the start bit, SCL=1, SDA=1 2: I2C master is sending out the start bit, SCL=1, SDA=0 3: I2C master/slave is preparing for transmitting data bit, SCL=0, SDA=data bit (data bit can be changed when SCL=0) 4: I2C master/slave is transmitting data bit, SCL=1, SDA=data bit (data bit is stable when SCL=1) 5: I2C master/slave is preparing for transmitting ACK bit, SCL=0, SDA=ack (ACK bit can be changed when SCL=0) 6: I2C master/slave is transmitting ACK bit, SCL=1, SDA=0 (ACK bit is stable when SCL=1) 7: I2C master is preparing for sending out stop bit or repeated-start bit, SCL=0, SDA=0/1 (0: stop bit; 1: repeated-start bit);

Bit(s)	Mnemonic	Name	Description
			8: I2C master is sending out stop bit or repeated-start bit, SCL=1, SDA=1/0 (1: stop bit; 0: repeated-start bit) 9: I2C master is in delay start between two transfers, SCL=1, SDA=1 10: I2C master is in FIFO wait state. For writing transaction, FIFO is empty and I2C master is waiting for DMA controller writing data into FIFO; for reading transaction, FIFO is full and I2C master is waiting for DMA controller reading data from FIFO, SCL=0, SDA=do not care 12: I2C master is preparing for sending out data bit of master code. This state is used only in high-speed transaction, SCL=0, SDA=data bit of master code (data bit of master code can be changed when SCL=0) 13: I2C master is sending out data bit of master code. This state is used only in high-speed transaction, SCL=1, SDA=data bit of master code (data bit of master code is stable when SCL=1) 14: I2C master/slave is preparing for transmitting NACK bit, SCL=0, SDA=nack bit (NACK bit can be changed when SCL=0). This state is used only in high-speed transaction. 15: I2C master/slave is transmitting NACK bit, SCL=1, SDA=1. This state is used only in high-speed transaction.

11007068 DEBUGCTRL Debug Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															APB_DEBUG_RD	FIFO_APB_DEBUG
Type															WO	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	**APB_DEBUG_RD**	APB_DEBUG_RD	**Only valid when fifo_apb_debug = 1** Write this register to generate a one pulsed FIFO APB RD signal for reading the FIFO data.
0	**FIFO_APB_DEBUG**	FIFO_APB_DEBUG	**For trace32 debugging** When using trace32 and the memory map is shown, turn this bit on to block the normal APB read access. APB read access to the FIFO will then be enabled by writing apb_debug_rd. 0: Disable 1: Enable

1100706C TRANSFER_LEN_AUX Transfer Length Register (Number of Bytes per Transfer) 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANSFER_LEN_AUX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
15:0	**TRANSFER_LEN_AUX**	TRANSFER_LEN_AUX	**Only valid when dir_change or transfer_len_change = 1** Indicates the number of data bytes to be transferred in one transfer unit (excluding slave address byte) for the transfers following the direction change. That is, if dir_change =1, the first write transfer length will depend on transfer_len, while the second read transfer length will depend on transfer_len_aux. Dir change is always after the first transfer. *Note: Set this value to bigger than 1; otherwise no transfer will take place.*

Module name: i2c_dual Base address: (+1100e000h)

Address	Name	Width	Register Function
1100E000	**DATA_PORT**	16	Data Port Register
1100E004	**SLAVE_ADDR**	16	Slave Address Register
1100E008	**INTR_MASK**	16	Interrupt Mask Register
1100E00C	**INTR_STAT**	16	Interrupt Status Register
1100E010	**CONTROL**	16	Control Register
1100E014	**TRANSFER_LEN**	16	Transfer Length Register
1100E018	**TRANSAC_LEN**	16	Transaction Length Register (Number of Transfers per Transaction)
1100E01C	**DELAY_LEN**	16	Inter Delay Length Register
1100E020	**TIMING**	16	Timing Control Register
1100E024	**START**	16	Start Register
1100E030	**FIFO_STAT**	16	FIFO Status Register
1100E034	**FIFO_THRESH**	16	FIFO Thresh Register
1100E038	**FIFO_ADDR_CLR**	16	FIFO Address Clear Register
1100E040	**IO_CONFIG**	16	IO Config Register
1100E044	**DEBUG**	16	Reserved Debug Register
1100E048	**HS**	16	High Speed Mode Register
1100E050	**SOFTRESET**	16	Soft Reset Register
1100E064	**DEBUGSTAT**	16	Debug Status Register
1100E068	**DEBUGCTRL**	16	Debug Control Register
1100E080	**CH2_DATA_PORT**	16	Channel 2 Data Port Register
1100E084	**CH2_SLAVE_ADDR**	16	Channel 2 Slave Address Register
1100E088	**CH2_INTR_MASK**	16	Channel 2 Interrupt Mask Register
1100E08C	**CH2_INTR_STAT**	16	Channel 2 Interrupt Status Register

Address	Name	Width	Register Function
1100E090	CH2_CONTROL	16	Channel 2 Control Register
1100E094	CH2_TRANSFER_LEN	16	Channel 2 Transfer Length Register
1100E098	CH2_TRANSAC_LEN	16	Channel 2 Transaction Length Register (Number of Transfers per Transaction)
1100E09C	CH2_DELAY_LEN	16	Channel 2 Inter Delay Length Register
1100E0A0	CH2_TIMING	16	Channel 2 Timing Control Register
1100E0A4	CH2_START	16	Channel 2 Start Register
1100E0B0	CH2_FIFO_STAT	16	Channel 2 FIFO Status Register
1100E0B8	CH2_FIFO_ADDR_CLR	16	Channel 2 FIFO Address Clear Register

1100E000 DATA_PORT **Data Port Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DATA_PORT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	DATA_PORT	DATA_PORT	**This is the FIFO access port.** During master write sequences (slave_addr[0] = 0), this port can be written by APB. During master read sequences (slave_addr[0] = 1), this port can be read by APB. *Note: Slave_addr should be set correctly before accessing the FIFO.* (For debugging only) If the fifo_apb_debug bit is set, the FIFO can be read and written by APB.

1100E004 SLAVE_ADDR **Slave Address Register** **000000BF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SLAVE_ADDR							
Type									RW							
Reset									1	0	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
7:0	SLAVE_ADDR	SLAVE_ADDR	**Specifies slave address of the device to be accessed** Bit 0 is defined by the I2C protocol as a bit that indicates the direction of transfer.

Bit(s)	Mnemonic	Name	Description
			0: Master write 1: Master read

1100E008 INTR_MASK **Interrupt Mask Register** **00000007**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														MAS_HS_NACKER	MAS_ACKERR	MAS_TRANSAC_COMP
Type														RW	RW	RW
Reset														1	1	1

Bit(s)	Mnemonic	Name	Description
2	**MAS_HS_NACKER**	MAS_HS_NACKER	Set this value to 0 to mask HS_NACKERR interrupt signal.
1	**MAS_ACKERR**	MAS_ACKERR	Set this value to 0 to mask ACK_ERR interrupt signal.
0	**MAS_TRANSAC_COMP**	MAS_TRANSAC_COMP	Set this value to 0 to mask TRANSAC_COMP interrupt signal.

1100E00C INTR_STAT **Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														HS_NACKERR	ACKERR	TRANSAC_COMP
Type														W1C	W1C	W1C
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	**HS_NACKERR**	HS_NACKERR	**This status will be asserted if HS master code NACK error detection is enabled.** If enabled, HS master code NACK ERR will cause transaction to end and stop will be issued.
1	**ACKERR**	ACKERR	**This status will be asserted if ACK error detection is enabled.** If enabled, ACKERR will cause transaction to end and stop will be issued.
0	**TRANSAC_COMP**	TRANSAC_COMP	**This status will be asserted when a transaction has completed successfully.**

1100E010 CONTROL **Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										TRANSFER_LEN_CHANGE	ACKERR_DET_EN	DIR_CHANGE	CLK_EXT_EN	DMA_EN	RS_STOP	
Type										RW	RW	RW	RW	RW	RW	
Reset										0	0	0	0	0	0	

Bit(s)	Mnemonic	Name	Description
6	**TRANSFER_LEN_CHANGE**	TRANSFER_LEN_CHANGE	**Specifies whether or not to change the transfer length after the fist transfer is completed** If enabled, the transfers after the first transfer will use the transfer_len_aux parameter.
5	**ACKERR_DET_EN**	ACKERR_DET_EN	**Enables slave ACK error detection** When enabled, if slave ACK error is detected, the master should terminate the transaction by issuing a STOP condition then asserting ACKERR interrupt. MCU should handle this case appropriately then reset the FIFO address before reissuing the transaction again. If this option is disabled, the controller will ignore slave ACK error and keep on the scheduled transaction. 0: Disable 1: Enable
4	**DIR_CHANGE**	DIR_CHANGE	**For combined transfer format, where the direction of transfer is to be changed from write to read after the first RS condition** Note: When set to 1, the transfers after the direction change will be based on the transfer_len_aux parameter. 0: Disable 1: Enable
3	**CLK_EXT_EN**	CLK_EXT_EN	**I2C spec allows slaves to hold the SCL line low if it is not yet ready for further processing.** Therefore, if this bit is set to 1, the master controller will enter a high wait state until the slave releases the SCL line.
2	**DMA_EN**	DMA_EN	**By default, this is disabled and FIFO data should be manually prepared by MCU.** This default setting should be used for transfer sizes of smaller than 8 data bytes and no multiple transfer is configured. When enabled, DMA requests are turned on, and the FIFO data should be prepared in memory.
1	**RS_STOP**	RS_STOP	**In LS/FS mode, this bit affects multi-transfer transaction only.** It controls whether or not REPEATED-START condition is used between transfers. The last ending transfer always ends with a STOP. In HS mode, set this bit to 1. 0: Use STOP 1: Use REPEATED-START

1100E014 TRANSFER_L Transfer Length Register 00000101

EN

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TRANSFER_LEN_AUX					TRANSFER_LEN							
Type				RW					RW							
Reset				0	0	0	0	1	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
12:8		TRANSFER_LEN_AUX	**Valid only when dir_change is set to 1.** Indicates the number of data bytes to be transferred in one transfer unit (excluding slave address byte) for the transfers following the direction change. That is, if dir_change =1, the first write transfer length will depend on transfer_len, and the second read transfer length will depend on transfer_len_aux. Dir change is always after the first transfer. *Note: Set this value to bigger than 1; otherwise no transfer will take place.*
7:0		TRANSFER_LEN	**Indicates the number of data bytes to be transferred in one transfer unit (excluding slave address byte)** *Note: Set this value to bigger than 1; otherwise no transfer will take place.*

1100E018 TRANSAC_LEN **Transaction Length Register (Number of Transfers per Transaction)** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TRANSFER_LEN							
Type									RW							
Reset									0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
7:0	**TRANSFER_LEN**	TRANSFER_LEN	**Indicates the number of transfers to be transferred in one transaction** *Note: Set this value to bigger than 1; otherwise no transfer will take place.*

1100E01C DELAY_LEN **Inter Delay Length Register** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DELAY_LEN							
Type									RW							
Reset									0	0	0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0	**DELAY_LEN**	DELAY_LEN	**Sets up wait delay between consecutive transfers when RS_STOP bit is set to 0** The unit is the same as half pulse width.

1100E020 TIMING **Timing Control Register** **00001303**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_READ_ADJ	DATA_READ_TIME				SAMPLE_CNT_DIV					STEP_CNT_DIV					
Type	RW	RW				RW					RW					
Reset	0	0	0	1		0	1	1			0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
15	**DATA_READ_ADJ**	DATA_READ_ADJ	**When set to 1, data latch in sampling time during master reads will be adjusted according to DATA_READ_TIME value. Otherwise, by default data are latched in at half of the high pulse width point.** Set this value to smaller than or equal to half the high pulse width.
14:12	**DATA_READ_TIME**	DATA_READ_TIME	**This value is valid only when DATA_READ_ADJ is set to 1.** This can be used to adjust so that data are latched in at earlier sampling points (assuming data is settled by then).
10:8	**SAMPLE_CNT_DIV**	SAMPLE_CNT_DIV	**(For LS/FS only) Adjusts width of each sample** Sample width = sample_cnt_div*1/13MHz
5:0	**STEP_CNT_DIV**	STEP_CNT_DIV	**Specifies the number of samples per half pulse width (i.e. each high or low pulse)**

1100E024 START **Start Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RS_STOP_MULTIPLE_CONFIG	RS_STOP_MULTIPLE_TRIG	RS_STOP_MULTIPLE_TRIG_CL													START

			R													
Type	RW	RW	RO													RW
Reset	0	0	0													0

Bit(s)	Mnemonic	Name	Description
15	**RS_STOP_MULTIPLE_CONFIG**	RS_STOP_MULTIPLE_CONFIG	**Enables multiple R/W, length and slave address with rs_stop transfer**
14	**RS_STOP_MULTIPLE_TRIG**	RS_STOP_MULTIPLE_TRIG	**Triggers the next transfer when enabling multiple R/W, length and slave address with rs_stop transfer**
13	**RS_STOP_MULTIPLE_TRIG_CLR**	RS_STOP_MULTIPLE_TRIG_CLR	**Clears rs_stop_mul_trig for the next transfer**
0	**START**	START	**Starts transaction on the bus** It is auto de-asserted at the end of the transaction.

1100E030 FIFO_STAT **FIFO Status Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RD_ADDR				WR_ADDR				FIFO_OFFSET						WR_FULL	RD_EMPTY
Type	RO				RO				RO						RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	1

Bit(s)	Mnemonic	Name	Description
15:12	**RD_ADDR**	RD_ADDR	**Current RD address pointer** Only bit [2:0] has physical meaning.
11:8	**WR_ADDR**	WR_ADDR	**Current WR address pointer** Only bit [2:0] has physical meaning.
7:4	**FIFO_OFFSET**	FIFO_OFFSET	**wr_addr[3:0] - rd_addr[3:0]**
1	**WR_FULL**	WR_FULL	**Indicates FIFO is full**
0	**RD_EMPTY**	RD_EMPTY	**Indicates FIFO is empty.**

1100E034 FIFO_THRESH **FIFO Thresh Register** **00000700**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						TX_TRIG_THRESH								RX_TRIG_THRESH		
Type						RW								RW		
Reset						1	1	1						0	0	0

Bit(s)	Mnemonic	Name	Description
10:8	**TX_TRIG_THRESH**	TX_TRIG_THRESH	When TX FIFO level is below this value, TX DMA request will be asserted.
2:0	**RX_TRIG_THRESH**	RX_TRIG_THRESH	When RX FIFO level is above this value, RX DMA

Bit(s)	Mnemonic	Name	Description
			request will be asserted.

1100E038 FIFO_ADDR_CLR **FIFO Address Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FIFO_ADDR_CLR
Type																WO
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**FIFO_ADDR_CLR**	FIFO_ADDR_CLR	When written 1, a one pulse fifo_addr_clr will be generated to clear the FIFO address back to 0.

1100E040 IO_CONFIG **IO Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													IDLE_OE_EN	IO_SYNC_EN	SDA_IO_CONFIG	SCL_IO_CONFIG
Type													WO	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3	**IDLE_OE_EN**	IDLE_OE_EN	
2	**IO_SYNC_EN**	IO_SYNC_EN	(For debugging only) When set to 1, SCL and SDA inputs will be first dual synced by bclk_ck. This should not be required. Only reserved for debugging.
1	**SDA_IO_CONFIG**	SDA_IO_CONFIG	
0	**SCL_IO_CONFIG**	SCL_IO_CONFIG	

1100E044 DEBUG **Reserved Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name														DEBUG		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0	**DEBUG**	DEBUG	

1100E048 HS **High Speed Mode Register** **00000102**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		HS_SAMPLE_CNT_DIV				HS_STEP_CNT_DIV				MASTER_CODE					HS_NACKERR_DET_EN	HS_EN
Type		RW				RW				RW					RW	RW
Reset		0	0	0		0	0	1		0	0	0			1	0

Bit(s)	Mnemonic	Name	Description
14:12	**HS_SAMPLE_CNT_DIV**	HS_SAMPLE_CNT_DIV	**When high-speed mode is entered after the master code transfer has been completed, the sample width will become dependent on this parameter.**
10:8	**HS_STEP_CNT_DIV**	HS_STEP_CNT_DIV	**When high-speed mode is entered after the master code transfer has been completed, the number of samples per half pulse width will become dependent on this value.**
6:4	**MASTER_CODE**	MASTER_CODE	**3-bit programmable value for the master code to be transmitted**
1	**HS_NACKERR_DET_EN**	HS_NACKERR_DET_EN	**Enables NACKERR detection during the master code transmission** When enabled, if NACK is not received after master code has been transmitted, the transaction will be terminated with a STOP condition.
0	**HS_EN**	HS_EN	**Enables high-speed transaction** *Note: Also set rs_stop to 1.*

1100E050 SOFTRESET **Soft Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SOFT_RESET
Type																WO
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**SOFT_RESET**	SOFT_RESET	When written 1, a one pulse soft reset will be used as synchronous reset to reset the I2C internal hardware circuits.

1100E064 DEBUGSTAT Debug Status Register 00002020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**CH2_MASTER_WRITE**	**CH2_MASTER_READ**	**CH2_MASTER_STATE**					**BUS_BUSY**	**MASTER_WRITE**	**MASTER_READ**	**MASTER_STATE**			
Type			RO	RO	RO					RO	RO	RO	RO			
Reset			1	0	0	0	0	0		0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13		CH2_MASTER_WRITE	
12		CH2_MASTER_READ	
11:8		CH2_MASTER_STATE	
6	**BUS_BUSY**	BUS_BUSY	**(For debugging only) Valid when bus_detect_en is 1** 1: Start transaction has been detected and no stop condition has been detected yet.
5	**MASTER_WRITE**	MASTER_WRITE	**For debugging only** 1: Current transfer is in the master write dir.
4	**MASTER_READ**	MASTER_READ	**For debugging only** 1: Current transfer is in the master read dir.
3:0	**MASTER_STATE**	MASTER_STATE	**(For debugging only) Reads back the current master_state** 0: Idle state 1: I2C master is preparing for sending out the start bit, SCL=1, SDA=1 2: I2C master is sending out the start bit, SCL=1, SDA=0 3: I2C master/slave is preparing for transmitting data bit, SCL=0, SDA=data bit (data bit can be changed when SCL=0) 4: I2C master/slave is transmitting data bit, SCL=1, SDA=data bit (data bit is stable when SCL=1) 5: I2C master/slave is preparing for transmitting ACK bit, SCL=0, SDA=ack (ACK bit can be changed when SCL=0) 6: I2C master/slave is transmitting ACK bit, SCL=1, SDA=0 (ACK bit is stable when SCL=1) 7: I2C master is preparing for sending out stop bit or repeated-start bit, SCL=0, SDA=0/1 (0: stop bit; 1: repeated-start bit); 8: I2C master is sending out stop bit or repeated-start bit, SCL=1, SDA=1/0 (1: stop bit; 0: repeated-start bit) 9: I2C master is in delay start between two transfers, SCL=1, SDA=1 10: I2C master is in FIFO wait state. For writing

Bit(s)	Mnemonic	Name	Description
			transaction, FIFO is empty and I2C master is waiting for DMA controller writing data into FIFO; for reading transaction, FIFO is full and I2C master is waiting for DMA controller reading data from FIFO, SCL=0, SDA=do not care 12: I2C master is preparing for sending out data bit of master code. This state is used only in high-speed transaction, SCL=0, SDA=data bit of master code (data bit of master code can be changed when SCL=0) 13: I2C master is sending out data bit of master code. This state is used only in high-speed transaction, SCL=1, SDA=data bit of master code (data bit of master code is stable when SCL=1) 14: I2C master/slave is preparing for transmitting NACK bit, SCL=0, SDA=nack bit (NACK bit can be changed when SCL=0). This state is used only in high-speed transaction. 15: I2C master/slave is transmitting NACK bit, SCL=1, SDA=1. This state is used only in high-speed transaction.

1100E068 DEBUGCTRL Debug Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CH2_APB_DEBUG_RD	APB_DEBUG_RD	FIFO_APB_DEBUG
Type														WO	WO	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	**CH2_APB_DEBUG**	CH2_APB_DEBUG_RD	
1	**APB_DEBUG_RD**	APB_DEBUG_RD	**Only valid when fifo_apb_debug = 1** Write this register to generate a one pulsed FIFO APB RD signal for reading the FIFO data.
0	**FIFO_APB_DEBUG**	FIFO_APB_DEBUG	**For trace32 debugging** When using trace32 and the memory map is shown, turn this bit on to block the normal APB read access. APB read access to the FIFO will then be enabled by writing apb_debug_rd. 0: Disable 1: Enable

1100E080 CH2_DATA_PORT Channel 2 Data Port Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CH2_DATA_PORT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**CH2_DATA_PORT**	CH2_DATA_PORT	**This is the FIFO access port.** During master write sequences (slave_addr[0] = 0), this port can be written by APB. During master read sequences (slave_addr[0] = 1), this port can be read by APB. *Note: Slave_addr should be set correctly before accessing the FIFO.* (For debugging only) If the fifo_apb_debug bit is set, the FIFO can be read and written by APB.

1100E084 CH2_SLAVE_ADDR **Channel 2 Slave Address Register** **000000BF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CH2_SLAVE_ADDR							
Type									RW							
Reset									1	0	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
7:0	**CH2_SLAVE_ADDR**	CH2_SLAVE_ADDR	**Specifies slave address of the device to be accessed** Bit 0 is defined by the I2C protocol as a bit that indicates the direction of transfer. 0: Master write 1: Master read

1100E088 CH2_INTR_MASK **Channel 2 Interrupt Mask Register** **00000003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CH2_MAS_ACKERR	CH2_MAS_TRANSAC_COMP
Type															RW	RW
Reset															1	1

Bit(s)	Mnemonic	Name	Description
1	**CH2_MAS_ACKERR**	CH2_MAS_ACKERR	Set this value to 0 to mask ACK_ERR interrupt signal.
0	**CH2_MAS_TRANSAC_COMP**	CH2_MAS_TRANSAC_COMP	Set this value to 0 to mask TRANSAC_COMP interrupt signal.

1100E08C CH2_INTR_STAT **Channel 2 Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**CH2_ACKERR**	**CH2_TRANSAC_COMP**
Type															W1C	W1C
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	**CH2_ACKERR**	CH2_ACKERR	**This status will be asserted if ACK error detection is enabled.** If enabled, ACKERR will cause transaction to end and stop will be issued.
0	**CH2_TRANSAC_COMP**	CH2_TRANSAC_COMP	**This status will be asserted when a transaction has completed successfully.**

1100E090 CH2_CONTROL **Channel 2 Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**CH2_TRANSFER_LEN_CHANGE**	**CH2_ACKERR_DET_EN**	**CH2_DIR_CHANGE**	**CH2_CLK_EXT_EN**		**CH2_RS_STOP**	
Type										RW	RW	RW	RW		RW	
Reset										0	0	0	0		0	

Bit(s)	Mnemonic	Name	Description
6	**CH2_TRANSFER_LEN_CHANGE**	CH2_TRANSFER_LEN_CHANGE	**Specifies whether or not to change the transfer length after the fist transfer is completed** If enabled, the transfers after the first transfer will use the transfer_len_aux parameter.
5	**CH2_ACKERR_DET_EN**	CH2_ACKERR_DET_EN	**Enables slave ACK error detection** When enabled, if slave ACK error is detected, the master should terminate the transaction by issuing a STOP condition then asserting ACKERR interrupt. MCU should handle this case appropriately then reset

Bit(s)	Mnemonic	Name	Description
			the FIFO address before reissuing the transaction again. If this option is disabled, the controller will ignore slave ACK error and keep on the scheduled transaction. 0: Disable 1: Enable
4	**CH2_DIR_CHANGE**	CH2_DIR_CHANGE	**For combined transfer format, where the direction of transfer is to be changed from write to read after the first RS condition** Note: When set to 1, the transfers after the direction change will be based on the transfer_len_aux parameter. 0: Disable 1: Enable
3	**CH2_CLK_EXT_EN**	CH2_CLK_EXT_EN	**I2C spec allows slaves to hold the SCL line low if it is not yet ready for further processing.** Therefore, if this bit is set to 1, the master controller will enter a high wait state until the slave releases the SCL line.
1	**CH2_RS_STOP**	CH2_RS_STOP	**In LS/FS mode, this bit affects multi-transfer transaction only.** It controls whether or not REPEATED-START condition is used between transfers. The last ending transfer always ends with a STOP. In HS mode, set this bit to 1. 0: Use STOP 1: Use REPEATED-START

1100E094 CH2_TRANSFER_LEN Channel 2 Transfer Length Register 00000101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**CH2_TRANSFER_LEN_AUX**								**CH2_TRANSFER_LEN**		
Type						RW								RW		
Reset						0	0	1						0	0	1

Bit(s)	Mnemonic	Name	Description
10:8	**CH2_TRANSFER_LEN_AUX**	CH2_TRANSFER_LEN_AUX	**Valid only when dir_change is set to 1.** Indicates the number of data bytes to be transferred in one transfer unit (excluding slave address byte) for the transfers following the direction change. That is, if dir_change =1, the first write transfer length will depend on transfer_len, and the second read transfer length will depend on transfer_len_aux. Dir change is always after the first transfer. Note: Set this value to bigger than 1; otherwise no transfer will take place.
2:0	**CH2_TRANSFER_LEN**	CH2_TRANSFER_LEN	**Indicates the number of data bytes to be transferred in one transfer unit (excluding slave address byte)** *Note: Set this value to bigger than 1; otherwise no*

Bit(s)	Mnemonic	Name	Description
			transfer will take place.

1100E098 CH2_TRANSAC_LEN **Channel 2 Transaction Length Register (Number of Transfers per Transaction)** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CH2_TRANSAC_LEN		
Type														RW		
Reset														0	0	1

Bit(s)	Mnemonic	Name	Description
2:0	**TRANSAC_LEN**	CH2_TRANSAC_LEN	**Indicates the number of transfers to be transferred in one transaction** *Note: Set this value to bigger than 1; otherwise no transfer will take place.*

1100E09C CH2_DELAY_LEN **Channel 2 Inter Delay Length Register** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CH2_DELAY_LEN							
Type									RW							
Reset									0	0	0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0	**CH2_DELAY_LEN**	CH2_DELAY_LEN	**Sets up wait delay between consecutive transfers when RS_STOP bit is set to 0** The unit is the same as half pulse width.

1100E0A0 CH2_TIMING **Channel 2 Timing Control Register** **00001303**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH2_DATA_REA	CH2_DATA_READ_TIME				CH2_SAMPLE_CNT_DIV					CH2_STEP_CNT_DIV					

	D_ADJ															
Type	RW	RW				RW					RW					
Reset	0	0	0	1		0	1	1			0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
15	**CH2_DATA_READ_ADJ**	CH2_DATA_READ_ADJ	**When set to 1, data latch in sampling time during master reads will be adjusted according to DATA_READ_TIME value. Otherwise, by default data are latched in at half of the high pulse width point.** Set this value to smaller than or equal to half the high pulse width.
14:12	**CH2_DATA_READ_TIME**	CH2_DATA_READ_TIME	**This value is valid only when DATA_READ_ADJ is set to 1.** This can be used to adjust so that data are latched in at earlier sampling points (assuming data is settled by then).
10:8	**CH2_SAMPLE_CNT_DIV**	CH2_SAMPLE_CNT_DIV	**(For LS/FS only) Adjusts width of each sample** Sample width = sample_cnt_div*1/13MHz
5:0	**CH2_STEP_CNT_DIV**	CH2_STEP_CNT_D IV	**Specifies the number of samples per half pulse width (i.e. each high or low pulse)**

1100E0A4 CH2_START **Channel 2 Start Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CH2_START
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**CH2_START**	CH2_START	**Starts transaction on the bus** It is auto de-asserted at the end of the transaction.

1100E0B0 CH2_FIFO_STAT **Channel 2 FIFO Status Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH2_RD_AD DR				CH2_WR_ADDR				CH2_FIFO_OFFSET						CH2_WR_FULL	CH2_RD_EMPTY
Type	RO				RO				RO						RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	1

Bit(s)	Mnemonic	Name	Description
15:12	**CH2_RD_ADDR**	CH2_RD_ADDR	**Current RD address pointer** Only bit [2:0] has physical meaning.
11:8	**CH2_WR_ADDR**	CH2_WR_ADDR	**Current WR address pointer** Only bit [2:0] has physical meaning.
7:4	**CH2_FIFO_OFFSE T**	CH2_FIFO_OFFSE T	**wr_addr[3:0] - rd_addr[3:0]**
1	**CH2_WR_FULL**	CH2_WR_FULL	**Indicates FIFO is full**
0	**CH2_RD_EMPTY**	CH2_RD_EMPTY	**Indicates FIFO is empty.**

1100E0B8 CH2_FIFO_ADDR_CLR **Channel 2 FIFO Address Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**CH2_FIFO_ADDR_CLR**
Type																WO
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**CH2_FIFO_ADDR_CLR**	CH2_FIFO_ADDR_CLR	When written 1, a one pulse fifo_addr_clr will be generated to clear the FIFO address back to 0.

3.10 Pulse-Width Modulation (PWM)

Module name: PWM Base address: (+11006000h)

Address	Name	Width	Register Function
11006000	PWM_ENABLE	32	PWM Enable Register
11006010	PWM0_CON	32	PWM0 Control Register
11006014	PWM0_HDURATION	32	PWM0 High Duration Register
11006018	PWM0_LDURATION	32	PWM0 Low Duration Register
1100601C	PWM0_GDURATION	32	PWM0 Guard Duration Register
11006020	PWM0_BUF0_BASE_ADDR	32	
11006024	PWM0_BUF0_SIZE	32	PWM0 Buffer 0 Size Register
11006028	PWM0_BUF1_BASE_ADDR	32	PWM0 Buffer 1 Base Address register
1100602C	PWM0_BUF1_SIZE	32	PWM0 Buffer 1 Size Register
11006030	PWM0_SEND_DATA0	32	PWM0 Send Data 0 Register
11006034	PWM0_SEND_DATA1	32	PWM0 Send Data 1 Register
11006038	PWM0_WAVE_NUM	32	PWM0 Wave Number Register
1100603C	PWM0_DATA_WIDTH	32	PWM0 Data Width Register
11006040	PWM0_THRESH	32	PWM0 Thresh Register
11006044	PWM0_SEND_WAVENUM	32	PWM0 Send Wave Number register
11006048	PWM0_VALID	32	PWM0 Valid Register
11006050	PWM1_CON	32	PWM1 Control Register
11006054	PWM1_HDURATION	32	PWM1 High Duration Register
11006058	PWM1_LDURATION	32	PWM1 Low Duration Register
1100605C	PWM1_GDURATION	32	PWM1 Guard Duration Register
11006060	PWM1_BUF0_BASE_ADDR	32	PWM1 Buffer 0 Base Address register
11006064	PWM1_BUF0_SIZE	32	PWM1 Buffer 0 Size Register
11006068	PWM1_BUF1_BASE_ADDR	32	PWM1 Buffer 1 Base Address register
1100606C	PWM1_BUF1_SIZE	32	PWM1 Buffer 1 Size Register
11006070	PWM1_SEND_DATA0	32	PWM1 Send Data 0 Register
11006074	PWM1_SEND_DATA1	32	PWM1 Send Data 1 Register
11006078	PWM1_WAVE_NUM	32	PWM1 Wave Number Register
1100607C	PWM1_DATA_WIDTH	32	PWM1 Data Width Register
11006080	PWM1_THRESH	32	PWM1 Thresh Register
11006084	PWM1_SEND_WAVENUM	32	PWM1 Send Wave Number register
11006088	PWM1_VALID	32	PWM1 Valid Register
11006090	PWM2_CON	32	PWM2 Control Register
11006094	PWM2_HDURATION	32	PWM2 High Duration Register
11006098	PWM2_LDURATION	32	PWM2 Low Duration Register
1100609C	PWM2_GDURATION	32	PWM2 Guard Duration Register

Address	Name	Width	Register Function
110060A0	PWM2_BUF0_BASE_ADDR	32	PWM2 Buffer 0 Base Address register
110060A4	PWM2_BUF0_SIZE	32	PWM2 Buffer 0 Size Register
110060A8	PWM2_BUF1_BASE_ADDR	32	PWM2 Buffer 1 Base Address register
110060AC	PWM2_BUF1_SIZE	32	PWM2 Buffer 1 Size Register
110060B0	PWM2_SEND_DATA0	32	PWM2 Send Data 0 Register
110060B4	PWM2_SEND_DATA1	32	PWM2 Send Data 1 Register
110060B8	PWM2_WAVE_NUM	32	PWM2 Wave Number Register
110060BC	PWM2_DATA_WIDTH	32	PWM2 Data Width Register
110060C0	PWM2_THRESH	32	PWM2 Thresh Register
110060C4	PWM2_SEND_WAVENUM	32	PWM2 Send Wave Number register
110060C8	PWM2_VALID	32	PWM2 Valid Register
110060D0	PWM3_CON	32	PWM3 Control Register
110060D4	PWM3_HDURATION	32	PWM3 High Duration Register
110060D8	PWM3_LDURATION	32	PWM3 Low Duration Register
110060DC	PWM3_GDURATION	32	PWM3 Guard Duration Register
110060E0	PWM3_BUF0_BASE_ADDR	32	PWM3 Buffer0 Base Address register
110060E4	PWM3_BUF0_SIZE	32	PWM3 Buffer0 Size Register
110060E8	PWM3_BUF1_BASE_ADDR	32	PWM3 Buffer1 Base Address register
110060EC	PWM3_BUF1_SIZE	32	PWM3 Buffer1 Size Register
110060F0	PWM3_SEND_DATA0	32	PWM3 Send Data0 Register
110060F4	PWM3_SEND_DATA1	32	PWM3 Send Data1 Register
110060F8	PWM3_WAVE_NUM	32	PWM3 Wave Number Register
11006104	PWM3_SEND_WAVENUM	32	PWM3 Send Wave Number register
110060FC	PWM3_DATA_WIDTH	32	PWM3 Data Width Register
11006100	PWM3_THRESH	32	PWM3 Thresh Register
11006108	PWM3_VALID	32	PWM3 Valid Register
110061CC	PWM_LOOP_BACK_TEST	32	PWM Loop Back Test
110061D0	PWM_3DLCM	32	PWM Support For 3D LCM
11006200	PWM_INT_ENABLE	32	PWM Interrupt Enable Register
11006204	PWM_INT_STATUS	32	PWM Interrupt Status Register
11006208	PWM_INT_ACK	32	PWM Interrupt Acknowledge Register
1100620C	PWM_EN_STATUS	32	PWM Enable Status Register
11006210	PWM_CK_26M_SEL	32	PWM BCLK Selection

11006000 PWM_ENABLE PWM Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													PWM3_EN	PWM2_EN	PWM1_EN	PWM0_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	PWM3_EN	0: Disabe PWM3 1: Enable PWM3
2	PWM2_EN	0: Disabe PWM2 1: Enable PWM2
1	PWM1_EN	0: Disabe PWM1 1: Enable PWM1
0	PWM0_EN	0: Disabe PWM0 1: Enable PWM0

11006010 PWM0_CON PWM0 Control Register 00007E00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	OLD_PWM_MODE	**Uses old PWM mode** *Note: Using old PWM mode also means using periodical mode.* Therefore, SRCSEL and MODE are ignored in this situation. Only old PWM mode with 32kHz clock however cannot work in system sleep mode. 0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	**Stop bit position for source data in periodical mode** In FIFO mode, it is used to indicate the stop bit position in total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	**PWM0 output value during guard time**
7	IDLE_VALUE	**PWM0 output value in idle state**
6	MODE	**Selects random generator mode** 0: Periodical PWM mode 1: Random PWM mode
5	SRCSEL	**Selects PWM0 data source** 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	0: CLK=32K; CLK is not used. 1: CLK=32K; CLK can be used.
3	CLKSEL	**Selects PWM0 clock** 0: CLK=CLKSRC

Bit(s)	Name	Description
		1: CLK=CLKSRC/1625
2:0	CLKDIV	**Selects PWM0 clock scale** 000b: CLK Hz 001b: CLK/2Hz 010b: CLK/4Hz 011b: CLK/8Hz 100b: CLK/16Hz 101b: CLK/32Hz 110b: CLK/64Hz 111b: CLK/128Hz

11006014 PWM0_HDURATION PWM0 High Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	HDURATION	**PWM0 pulse duration based on the current clock when PWM output is high** If duration =N, program N-1 in this register. *Note: The duration of PWM must not be 0.*

11006018 PWM0_LDURATION PWM0 Low Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	LDURATION	**PWM0 pulse duration based on the current clock when PWM output is low** If duration =N, program N-1 in this register. *Note: The duration of PWM must not be 0.*

1100601C PWM0_GDURATION PWM0 Guard Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GUARD_DURATION	**Guarding interval between individual waveforms and the output is decided by GUARD_VALUE** If it equals N, program N-1 in this register. *Note:* *1. If this duration is 0, it means there is no guarding interval.* *2: The guard duration of old mode is set by PWM_DATA_WIDTH.*

11006020 PWM0_BUF0_BASE_ADDR **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	Base address of memory buffer0 for PWM0's waveform data

11006024 PWM0_BUF0_SIZE **PWM0 Buffer 0 Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	**Length of waveform data in memory buffer0 PWM0 should generate** If it equals N, program N-1 in this register. *Note: The size is in unit of 32-bit data.*

11006028 PWM0_BUF1_BASE_ADDR **PWM0 Buffer 1 Base Address register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	**Base address of memory buffer1 for PWM0's waveform data** *Note: The memory buffer1 is useless in periodical mode.*

1100602C PWM0_BUF1_SIZE **PWM0 Buffer 1 Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	**Length of waveform data in memory buffer1 PWM0 should generate** If it equals N, program N-1 in this register.

11006030 PWM0_SEND_DATA0 **PWM0 Send Data 0 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	**PWM0 local buffer0 of pulse sequence data to be generated** *Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.*

11006034 PWM0_SEND_DATA1 PWM0 Send Data 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	**PWM0 local buffer0 of pulse sequence data to be generated** *Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.*

11006038 PWM0_WAVE_NUM PWM0 Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	**Number by which PWM0 will generate from pulse data repeatedly** *Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.*

1100603C PWM0_DATA_WIDTH PWM0 Data Width Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DATA_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DATA_WIDTH	**PWM0 pulse data width in old PWM mode**

Bit(s)	Name	Description

11006040 PWM0_THRESH PWM0 Thresh Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				THRESH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	THRESH	PWM0 pulse data high/low switching threshold in old PWM mode

11006044 PWM0_SEND_WAVENUM PWM0 Send Wave Number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SEND_WAVENUM	Number by which PWM0 has already generated from specified data source in periodical mode

11006048 PWM0_VALID PWM0 Valid Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	0: Memory1 is empty. 1: Memory1 is not empty. When finishing writing data to memory1, write 1 to inform PWM the data in memory1 are ready.

Bit(s)	Name	Description
0	BUF0_VALID	0: Memory0 is empty. 1: Memory0 is not empty. When finishing writing data to memory0, write 1 to inform PWM the data in memory0 are ready.

11006050 PWM1_CON PWM1 Control Register 00007E00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	OLD_PWM_MODE	**Uses old PWM mode** *Note: Using old PWM mode also means using periodical mode.* Therefore, SRCSEL and MODE are ignored in this situation. Only old PWM mode with 32kHz clock however cannot work in system sleep mode. 0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	*Note: Using old PWM mode also means using periodical mode.* Therefore, SRCSEL and MODE are ignored in this situation. Only old PWM mode with 32kHz clock however cannot work in system sleep mode.
8	GUARD_VALUE	**PWM1 output value during guard time**
7	IDLE_VALUE	**PWM1 output value in idle state**
6	MODE	**Selects random generator mode** 0: Periodical PWM mode 1: Random PWM mode
5	SRCSEL	**Selects PWM1 data source** 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	0: CLK=32K; CLK is not used. 1: CLK=32K; CLK can be used.
3	CLKSEL	**Selects PWM0 clock** 0: CLK=CLKSRC 1: CLK=CLKSRC/1625
2:0	CLKDIV	**Selects PWM1 clock scale** 000b: CLK Hz 001b: CLK/2Hz 010b: CLK/4Hz 011b: CLK/8Hz 100b: CLK/16Hz 101b: CLK/32Hz 110b: CLK/64Hz 111b: CLK/128Hz

11006054 PWM1_HDURA PWM1 High Duration Register 00000001

TION

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	HDURATION	**PWM1 pulse duration based on the current clock when PWM output is high** If duration =N, program N-1 in this register. *Note: The duration of PWM must not be 0.*

11006058 PWM1_LDURATION PWM1 Low Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	LDURATION	**PWM1 pulse duration based on the current clock when PWM output is low** If duration =N, program N-1 in this register. *Note: The duration of PWM must not be 0.*

1100605C PWM1_GDURATION PWM1 Guard Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GUARD_DURATION	**Guarding interval between individual waveforms and the output is decided by GUARD_VALUE** If it equals N, program N-1 in this register. *Note:*

Bit(s)	Name	Description
		1. If this duration is 0, it means there is no guarding interval. *2: The guard duration of old mode is set by PWM_DATA_WIDTH.*

11006060 PWM1_BUF0_BASE_ADDR **PWM1 Buffer 0 Base Address register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	Base address of memory buffer0 for PWM1's waveform data

11006064 PWM1_BUF0_SIZE **PWM1 Buffer 0 Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	**Length of waveform data in memory buffer0 PWM1 should generate** If it equals N, program N-1 in this register. *Note: The size is in unit of 32-bit data.*

11006068 PWM1_BUF1_BASE_ADDR **PWM1 Buffer 1 Base Address register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	**Base address of memory buffer1 for PWM10's waveform data** *Note: The memory buffer1 is useless in periodical mode.*

1100606C PWM1_BUF1_SIZE PWM1 Buffer 1 Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	**Length of waveform data in memory buffer1 PWM1 should generate** If it equals N, program N-1 in this register.

11006070 PWM1_SEND_DATA0 PWM1 Send Data 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	**PWM1 local buffer0 of pulse sequence data to be generated** *Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.*

11006074 PWM1_SEND_DATA1 PWM1 Send Data 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	**PWM1 local buffero of pulse sequence data to be generated** *Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.*

11006078 PWM1_WAVE_NUM PWM1 Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	**Number by which PWM1 will generate from pulse data repeatedly** *Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.*

1100607C PWM1_DATA_WIDTH PWM1 Data Width Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DATA_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DATA_WIDTH	PWM1 pulse data width in old PWM mode

11006080 PWM1_THRESH PWM1 Thresh Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				THRESH												
Type				RW												

Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	THRESH	PWM1 pulse data high/low switching threshold in old PWM mode

11006084 PWM1_SEND_WAVENUM **PWM1 Send Wave Number register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SEND_WAVENUM	Number by which PWM1 has already generated from specified data source in periodical mode

11006088 PWM1_VALID **PWM1 Valid Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	0: Memory1 is empty. 1: Memory1 is not empty. When finishing writing data to memory1, write 1 to inform PWM the data in memory1 are ready.
0	BUF0_VALID	0: Memory0 is empty. 1: Memory0 is not empty. When finishing writing data to memory0, write 1 to inform PWM the data in memory0 are ready.

11006090 PWM2_CON **PWM2 Control Register** **00007E00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_	STOP_BITPOS						GUARD_VA	IDLE_VAL	MODE	SRCSEL	CLKSEL_O	CLKSEL	CLKDIV		

	MODE							LUE	UE			LD				
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	OLD_PWM_MODE	**Uses old PWM mode** *Note: Using old PWM mode also means using periodical mode.* Therefore, SRCSEL and MODE are ignored in this situation. Only old PWM mode with 32kHz clock source however cannot work in system sleep mode. 0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	**Stop bit position for source data in periodical mode** In FIFO mode, it is used to indicate the stop bit position in total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	**PWM2 output value during guard time**
7	IDLE_VALUE	**PWM2 output value in idle state**
6	MODE	**Selects random generator mode** 0: Periodical PWM mode 1: Random PWM mode
5	SRCSEL	**Selects PWM2 data source** 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	0: CLK=32K; CLK is not used. 1: CLK=32K; CLK can be used.
3	CLKSEL	**Selects PWM0 clock** 0: CLK=CLKSRC 1: CLK=CLKSRC/1625
2:0	CLKDIV	**Selects PWM2 clock scale** 000b: CLK Hz 001b: CLK/2Hz 010b: CLK/4Hz 011b: CLK/8Hz 100b: CLK/16Hz 101b: CLK/32Hz 110b: CLK/64Hz 111b: CLK/128Hz

11006094 PWM2_HDURATION PWM2 High Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	HDURATION	**PWM2 pulse duration based on the current clock when PWM output is high** If duration =N, program N-1 in this register. *Note: The duration of PWM must not be 0.*

Bit(s)	Name	Description

11006098 PWM2_LDURATION PWM2 Low Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	LDURATION	**PWM2 pulse duration based on the current clock when PWM output is low** If duration =N, program N-1 in this register. *Note: The duration of PWM must not be 0.*

1100609C PWM2_GDURATION PWM2 Guard Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GUARD_DURATION	**Guarding interval between individual waveforms and the output is decided by GUARD_VALUE** If it equals N, program N-1 in this register. *Note:* *1. If this duration is 0, it means there is no guarding interval.* *2: The guard duration of old mode is set by PWM_DATA_WIDTH.*

110060A0 PWM2_BUF0_BASE_ADDR PWM2 Buffer 0 Base Address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	Base address of memory buffer0 for PWM2's waveform data

110060A4 PWM2_BUF0_SIZE **PWM2 Buffer 0 Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	**Length of waveform data in memory buffer0 PWM2 should generate** If it equals N, program N-1 in this register.

110060A8 PWM2_BUF1_BASE_ADDR **PWM2 Buffer 1 Base Address register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	**Base address of memory buffer1 for PWM2's waveform data** *Note: The memory buffer1 is useless in periodical mode.*

110060AC PWM2_BUF1_SIZE **PWM2 Buffer 1 Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	**Length of waveform data in memory buffer1 PWM2 should generate** If it equals N, program N-1 in this register.

110060B0 PWM2_SEND_DATA0 PWM2 Send Data 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	**PWM2 local buffer0 of pulse sequence data to be generated** *Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.*

110060B4 PWM2_SEND_DATA1 PWM2 Send Data 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	**PWM2 local buffer0 of pulse sequence data to be generated** *Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.*

110060B8 PWM2_WAVE_NUM PWM2 Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	**Number by which PWM2 will generate from pulse data repeatedly** *Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.*

110060BC PWM2_DATA_WIDTH **PWM2 Data Width Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DATA_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DATA_WIDTH	PWM2 pulse data width in old PWM mode

110060C0 PWM2_THRESH **PWM2 Thresh Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				THRESH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	THRESH	PWM2 pulse data high/low switching threshold in old PWM mode

110060C4 PWM2_SEND_WAVENUM **PWM2 Send Wave Number register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SEND_WAVENUM	Number by which PWM2 has already generated from specified data source in periodical mode

110060C8 PWM2_VALID PWM2 Valid Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	0: Memory1 is empty. 1: Memory1 is not empty. When finishing writing data to memory1, write 1 to inform PWM the data in memory1 are ready.
0	BUF0_VALID	0: Memory0 is empty. 1: Memory0 is not empty. When finishing writing data to memory0, write 1 to inform PWM the data in memory0 are ready.

110060D0 PWM3_CON PWM3 Control Register 00007E00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	OLD_PWM_MODE	**Uses old PWM mode** *Note: Using old PWM mode also means using periodical mode.* Therefore, SRCSEL and MODE are ignored in this situation. Only old PWM mode with 32kHz clock source however cannot work in system sleep mode. 0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	**Stop bit position for source data in periodical mode** In FIFO mode, it is used to indicate the stop bit position in total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	**PWM3 output value during guard time**
7	IDLE_VALUE	**PWM3 output value in idle state**
6	MODE	**Selects random generator mode** 0: Periodical PWM mode 1: Random PWM mode

Bit(s)	Name	Description
5	SRCSEL	**Selects PWM3 data source** 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	0: CLK=32K; CLK is not used. 1: CLK=32K; CLK can be used.
3	CLKSEL	**Selects PWM0 clock** 0: CLK=CLKSRC 1: CLK=CLKSRC/1625
2:0	CLKDIV	**Selects PWM3 clock scale** 000b: CLK Hz 001b: CLK/2Hz 010b: CLK/4Hz 011b: CLK/8Hz 100b: CLK/16Hz 101b: CLK/32Hz 110b: CLK/64Hz 111b: CLK/128Hz

110060D4 PWM3_HDURATION PWM3 High Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	HDURATION	**PWM3 pulse duration based on the current clock when PWM output is high** If duration =N, program N-1 in this register. *Note: The duration of PWM must not be 0.*

110060D8 PWM3_LDURATION PWM3 Low Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	LDURATION	**PWM3 pulse duration based on the current clock when PWM output is low** If duration =N, program N-1 in this register.

Bit(s)	Name	Description
		Note: The duration of PWM must not be 0.

110060DC PWM3_GDURATION **PWM3 Guard Duration Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GUARD_DURATION	**Guarding interval between individual waveforms and the output is decided by GUARD_VALUE** If it equals N, program N-1 in this register. *Note:* *1. If this duration is 0, it means there is no guarding interval.* *2: The guard duration of old mode is set by PWM_DATA_WIDTH.*

110060E0 PWM3_BUF0_BASE_ADDR **PWM3 Buffer0 Base Address register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	Base address of memory buffer0 for PWM3's waveform data

110060E4 PWM3_BUF0_SIZE **PWM3 Buffer0 Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	**Length of waveform data in memory buffer0 PWM3 should generate** If it equals N, program N-1 in this register.

110060E8 PWM3_BUF1_BASE_ADDR **PWM3 Buffer1 Base Address register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	**Base address of memory buffer1 for PWM3's waveform data** *Note: The memory buffer1 is useless in periodical mode.*

110060EC PWM3_BUF1_SIZE **PWM3 Buffer1 Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	**Length of waveform data in memory buffer1 PWM3 should generate** If it equals N, program N-1 in this register.

110060F0 PWM3_SEND_DATA0 **PWM3 Send Data0 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	**PWM3 local buffer0 of pulse sequence data to be generated** *Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.*

110060F4 PWM3_SEND_DATA1 **PWM3 Send Data1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	**PWM3 local buffer0 of pulse sequence data to be generated** *Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.*

110060F8 PWM3_WAVE_NUM **PWM3 Wave Number Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	**Number by which PWM3 will generate from pulse data repeatedly** *Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.*

11006104 PWM3_SEND_WAVENUM **PWM3 Send Wave Number register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															

Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SEND_WAVENUM	Number by which PWM3 has already generated from specified data source in periodical mode

110060FC PWM3_DATA_WIDTH **PWM3 Data Width Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DATA_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DATA_WIDTH	PWM3 pulse data width in old PWM mode

11006100 PWM3_THRESH **PWM3 Thresh Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				THRESH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	THRESH	PWM3 pulse data high/low switching threshold in old PWM mode

11006108 PWM3_VALID **PWM3 Valid Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	0: Memory1 is empty. 1: Memory1 is not empty. When finishing writing data to memory1, write 1 to inform PWM the data in memory1 are ready.
0	BUF0_VALID	0: Memory0 is empty. 1: Memory0 is not empty. When finishing writing data to memory0, write 1 to inform PWM the data in memory0 are ready.

110061CC PWM_LOOP_BACK_TEST **PWM Loop Back Test** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													PWM3_STATUS	PWM2_STATUS	PWM1_STATUS	PWM0_STATUS
Type													RU	RU	RU	RU
Reset													0	0	0	0

Bit(s)	Name	Description
3	PWM3_STATUS	0: PWM3 output is low. 1: PWM3 output is high.
2	PWM2_STATUS	0: PWM2 output is low. 1: PWM2 output is high.
1	PWM1_STATUS	0: PWM1 output is low. 1: PWM1 output is high.
0	PWM0_STATUS	0: PWM0 output is low. 1: PWM0 output is high.

110061D0 PWM_3DLCM **PWM Support For 3D LCM** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													PWM_3DLCM_4	PWM_3DLCM_3	PWM_3DLCM_2	PWM_3DLCM_1
Type													RW	RW	RW	RW
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PWM_3DLCM_SYNC			PWM_3DLCM_5_base	PWM_3DLCM_4_base	PWM_3DLCM_3_base	PWM_3DLCM_2_base	PWM_3DLCM_1_base				PWM_3DLCM_4_INV	PWM_3DLCM_3_INV	PWM_3DLCM_2_INV	PWM_3DLCM_1_INV	PWM_3DLCM_EN
Type	RW			RW	RW	RW	RW	RW				RW	RW	RW	RW	RW
Reset	0			0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
19	PWM_3DLCM_4	*Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.* 0: PWM3 is not selected as PWM auxiliary channel. 1: PWM3 is selected as PWM auxiliary channel.

Bit(s)	Name	Description
18	PWM_3DLCM_3	*Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.* 0: PWM2 is not selected as PWM auxiliary channel. 1: PWM2 is selected as PWM auxiliary channel.
17	PWM_3DLCM_2	*Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.* 0: PWM1 is not selected as PWM auxiliary channel. 1: PWM1 is selected as PWM auxiliary channel.
16	PWM_3DLCM_1	*Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.* 0: PWM0 is not selected as PWM auxiliary channel. 1: PWM0 is selected as PWM auxiliary channel.
15	PWM_3DLCM_SYNC	0: PWM auxiliary channel does not keep low when PWM base channel is disabled. 1: PWM auxiliary channel keeps low when PWM base channel is disabled.
12	PWM_3DLCM_5_base	*Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.* 0: PWM4 is not selected as PWM base channel. 1: PWM4 is selected as PWM base channel.
11	PWM_3DLCM_4_base	*Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.* 0: PWM3 is not selected as PWM base channel. 1: PWM3 is selected as PWM base channel.
10	PWM_3DLCM_3_base	*Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.* 0: PWM2 is not selected as PWM base channel. 1: PWM2 is selected as PWM base channel.
9	PWM_3DLCM_2_base	*Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.* 0: PWM1 is not selected as PWM base channel. 1: PWM1 is selected as PWM base channel.
8	PWM_3DLCM_1_base	*Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.* 0: PWM0 is not selected as PWM base channel. 1: PWM0 is selected as PWM base channel.
4	PWM_3DLCM_4_INV	0: PWM3 is the same as PWM base channel when PWM3 is selected as auxiliary channel. 1: PWM3 is inversion of PWM base channel when PWM3 is selected as auxiliary channel.
3	PWM_3DLCM_3_INV	0: PWM2 is the same as PWM base channel when PWM2 is selected as auxiliary channel. 1: PWM2 is inversion of PWM base channel when PWM2 is selected as auxiliary channel.
2	PWM_3DLCM_2_INV	0: PWM1 is the same as PWM base channel when PWM1 is selected as auxiliary channel. 1: PWM1 is inversion of PWM base channel when PWM1 is selected as auxiliary channel.
1	PWM_3DLCM_1_INV	0: PWM0 is the same as PWM base channel when PWM0 is selected as auxiliary channel. 1: PWM0 is inversion of PWM base channel when PWM0 is selected as auxiliary channel.
0	PWM_3DLCM_EN	0: Disable 3D_LCM for PWM 1: Enable 3D_LCM for PWM

11006200 PWM_INT_EN PWM Interrupt Enable Register 00000000

ABLE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									PWM3_INT_UNDERFLOW_EN	PWM3_INT_FINISH_EN	PWM2_INT_UNDERFLOW_EN	PWM2_INT_FINISH_EN	PWM1_INT_UNDERFLOW_EN	PWM1_INT_FINISH_EN	PWM0_INT_UNDERFLOW_EN	PWM0_INT_FINISH_EN
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	PWM3_INT_UNDERFLOW_EN	0: Disable underflow interrupt for PWM3 1: Enable underflow interrupt for PWM3
6	PWM3_INT_FINISH_EN	0: Disable finished interrupt for PWM3 1: Enable finished interrupt for PWM3
5	PWM2_INT_UNDERFLOW_EN	0: Disable underflow interrupt for PWM2 1: Enable underflow interrupt for PWM2
4	PWM2_INT_FINISH_EN	0: Disable finished interrupt for PWM2 1: Enable finished interrupt for PWM2
3	PWM1_INT_UNDERFLOW_EN	0: Disable underflow interrupt for PWM1 1: Enable underflow interrupt for PWM1
2	PWM1_INT_FINISH_EN	0: Disable finished interrupt for PWM1 1: Enable finished interrupt for PWM1
1	PWM0_INT_UNDERFLOW_EN	0: Disable underflow interrupt for PWM0 1: Enable underflow interrupt for PWM0
0	PWM0_INT_FINISH_EN	0: Disable finished interrupt for PWM0 1: Enable finished interrupt for PWM0

11006204 PWM_INT_STATUS PWM Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									PWM3_INT_UNDERFLOW_ST	PWM3_INT_FINISH_ST	PWM2_INT_UNDERFLOW_ST	PWM2_INT_FINISH_ST	PWM1_INT_UNDERFLOW_ST	PWM1_INT_FINISH_ST	PWM0_INT_UNDERFLOW_ST	PWM0_INT_FINISH_ST
Type									RU	RU	RU	RU	RU	RU	RU	RU
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	PWM3_INT_UNDERFLOW_ST	0: PWM3 underflow interrupt has not come. 1: PWM3 underflow interrupt has come.
6	PWM3_INT_FINISH_ST	0: PWM3 finished interrupt has not come. 1: PWM3 finished interrupt has come.

Bit(s)	Name	Description
5	PWM2_INT_UNDERFLOW_ST	0: PWM2 underflow interrupt has not come. 1: PWM2 underflow interrupt has come.
4	PWM2_INT_FINISH_ST	0: PWM2 finished interrupt has not come. 1: PWM2 finished interrupt has come.
3	PWM1_INT_UNDERFLOW_ST	0: PWM1 underflow interrupt has not come. 1: PWM1 underflow interrupt has come.
2	PWM1_INT_FINISH_ST	0: PWM1 finished interrupt has not come. 1: PWM1 finished interrupt has come.
1	PWM0_INT_UNDERFLOW_ST	0: PWM0 underflow interrupt has not come. 1: PWM0 underflow interrupt has come.
0	PWM0_INT_FINISH_ST	0: PWM0 finished interrupt has not come. 1: PWM0 finished interrupt has come.

11006208 PWM_INT_ACK **PWM Interrupt Acknowledge Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									PWM3_INT_UNDERFLOW_ACK	PWM3_INT_FINISH_ACK	PWM2_INT_UNDERFLOW_ACK	PWM2_INT_FINISH_ACK	PWM1_INT_UNDERFLOW_ACK	PWM1_INT_FINISH_ACK	PWM0_INT_UNDERFLOW_ACK	PWM0_INT_FINISH_ACK
Type									WO	WO	WO	WO	WO	WO	WO	WO
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	PWM3_INT_UNDERFLOW_ACK	0: Does not clear PWM3 underflow interrupt 1: Clear PWM3 underflow interrupt
6	PWM3_INT_FINISH_ACK	0: Does not clear PWM3 finished interrupt 1: Clear PWM3 finished interrupt
5	PWM2_INT_UNDERFLOW_ACK	0: Does not clear PWM2 underflow interrupt 1: Clear PWM2 underflow interrupt
4	PWM2_INT_FINISH_ACK	0: Does not clear PWM2 finished interrupt 1: Clear PWM2 finished interrupt
3	PWM1_INT_UNDERFLOW_ACK	0: Does not clear PWM1 underflow interrupt 1: Clear PWM1 underflow interrupt
2	PWM1_INT_FINISH_ACK	0: Does not clear PWM1 finished interrupt 1: Clear PWM1 finished interrupt
1	PWM0_INT_UNDERFLOW_ACK	0: Does not clear PWM0 underflow interrupt 1: Clear PWM0 underflow interrupt
0	PWM0_INT_FINISH_ACK	0: Does not clear PWM0 finished interrupt 1: Clear PWM0 finished interrupt

1100620C PWM_EN_STATUS **PWM Enable Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													PWM3_EN_ST	PWM2_EN_ST	PWM1_EN_ST	PWM0_EN_ST
Type													RO	RO	RO	RO
Reset													0	0	0	0

Bit(s)	Name	Description
3	PWM3_EN_ST	PWM3 enabling status
2	PWM2_EN_ST	PWM2 enabling status
1	PWM1_EN_ST	PWM1 enabling status
0	PWM0_EN_ST	PWM0 enabling status

11006210 PWM_CK_26M_SEL PWM BCLK Selection 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																PWM_26M_SEL
Type																RW
Reset																1

Bit(s)	Name	Description
0	PWM_26M_SEL	0: Select bus CLK as BCLK 1: Select 26M fix CLK as BCLK

3.11 General-Purpose Timer (GPT)

Module name: APXGPT Base address: (+10008000h)

Address	Name	Width	Register Function
10008000	GPT_IRQEN	32	GPT IRQ Enabling
10008004	GPT_IRQSTA	32	GPT IRQ Status
10008008	GPT_IRQACK	32	GPT IRQ Acknowledgement
10008010	GPT1_CON	32	GPT1 Control
10008014	GPT1_CLK	32	GPT1 Clock Setting
10008018	GPT1_COUNT	32	GPT1 Counter
1000801C	GPT1_COMPARE	32	GPT1 Compare Value
10008020	GPT2_CON	32	GPT2 Control
10008024	GPT2_CLK	32	GPT2 Clock Setting
10008028	GPT2_COUNT	32	GPT2 Counter
1000802C	GPT2_COMPARE	32	GPT2 Compare Value
10008030	GPT3_CON	32	GPT3 Control
10008034	GPT3_CLK	32	GPT3 Clock Setting
10008038	GPT3_COUNT	32	GPT3 Counter
1000803C	GPT3_COMPARE	32	GPT3 Compare Value
10008040	GPT4_CON	32	GPT4 Control
10008044	GPT4_CLK	32	GPT4 Clock Setting
10008048	GPT4_COUNT	32	GPT4 Counter
1000804C	GPT4_COMPARE	32	GPT4 Compare Value
10008050	GPT5_CON	32	GPT5 Control
10008054	GPT5_CLK	32	GPT5 Clock Setting
10008058	GPT5_COUNT	32	GPT5 Counter
1000805C	GPT5_COMPARE	32	GPT5 Compare Value
10008060	GPT6_CON	32	GPT6 Control
10008064	GPT6_CLK	32	GPT6 Clock Setting
10008068	GPT6_COUNTL	32	GPT6 Counter L
1000806C	GPT6_COMPAREL	32	GPT6 Compare Value L
10008078	GPT6_COUNTH	32	GPT6 Counter L
1000807C	GPT6_COMPAREH	32	GPT6 Compare Value H
10008080	APXGPT_IRQMASK0	32	APMCU IRQMASK Register
10008084	APXGPT_IRQMASK1	32	MD32 IRQMASK Register
10008090	APXGPT_SW_CG	32	Software Clock Gating

10008000 GPT_IRQEN GPT IRQ Enabling 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											IRQEN					

Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	IRQEN	**Enables interrupt of each GPT** 0: Disable associated interrupt of GPT 1: Enable associated interrupt of GPT

10008004 GPT_IRQSTA **GPT IRQ Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											IRQSTA					
Type											RO					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	IRQSTA	**Interrupt status of each GPT** 0: No associated interrupt is generated 1: Associated interrupt is pending and waiting for service

10008008 GPT_IRQACK **GPT IRQ Acknowledgement** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											IRQACK					
Type											WO					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	IRQACK	**Interrupt acknowledgement for each GPT** 0: No effect 1: Associated interrupt request is acknowledged and should be relinquished

10008010 GPT1_CON **GPT1 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MODE 1				CLR1	EN1

Type											RW				WO	RW
Reset											0	0			0	0

Bit(s)	Name	Description
5:4	MODE1	**Operation mode of GPT1** 00: ONE-SHOT mode 01: REPEAT mode 10: KEEP-GO mode 11: FREERUN mode
1	CLR1	**Clears the counter of GPT1 to 0** 0: No effect 1: Clear
0	EN1	**Enables GPT1** 0: Disable 1: Enable

10008014 GPT1_CLK **GPT1 Clock Setting** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLK1	CLKDIV1			
Type												RW	RW			
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	CLK1	**Sets up clock source of GPT1** 0: System clock (13MHz) 1: RTC clock (32kHz)
3:0	CLKDIV1	**Setting of GPT1 input clock frequency divider** 0000: Clock source divided by 1 0001: Clock source divided by 2 0010: Clock source divided by 3 0011: Clock source divided by 4 0100: Clock source divided by 5 0101: Clock source divided by 6 0110: Clock source divided by 7 0111: Clock source divided by 8 1000: Clock source divided by 9 1001: Clock source divided by 10 1010: Clock source divided by 11 1011: Clock source divided by 12 1100: Clock source divided by 13 1101: Clock source divided by 16 1110: Clock source divided by 32 1111: Clock source divided by 64

10008018 GPT1_COUNT **GPT1 Counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	COUNTER1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNTER1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COUNTER1	Timer counter of GPT1

1000801C GPT1_COMPARE GPT1 Compare Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COMPARE1	Compare value of GPT1

10008020 GPT2_CON GPT2 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MODE 2				CLR2	EN2
Type											RW				WO	RW
Reset											0	0			0	0

Bit(s)	Name	Description
5:4	MODE2	**Operation mode of GPT2** 00: ONE-SHOT mode 01: REPEAT mode 10: KEEP-GO mode 11: FREERUN mode
1	CLR2	**Clears the counter of GPT2 to 0** 0: No effect 1: Clear
0	EN2	**Enables GPT2** 0: Disable 1: Enable

10008024 GPT2_CLK **GPT2 Clock Setting** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLK2	CLKDIV2			
Type												RW	RW			
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	CLK2	**Sets up clock source of GPT2** 0: System clock (13MHz) 1: RTC clock (32kHz)
3:0	CLKDIV2	**Setting of GPT2 input clock frequency divider** 0000: Clock source divided by 1 0001: Clock source divided by 2 0010: Clock source divided by 3 0011: Clock source divided by 4 0100: Clock source divided by 5 0101: Clock source divided by 6 0110: Clock source divided by 7 0111: Clock source divided by 8 1000: Clock source divided by 9 1001: Clock source divided by 10 1010: Clock source divided by 11 1011: Clock source divided by 12 1100: Clock source divided by 13 1101: Clock source divided by 16 1110: Clock source divided by 32 1111: Clock source divided by 64

10008028 GPT2_COUNT **GPT2 Counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COUNTER2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNTER2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COUNTER2	Timer counter of GPT2

1000802C GPT2_COMPARE **GPT2 Compare Value** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMPARE2															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMPARE2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COMPARE2	Compare value of GPT2

10008030 GPT3_CON **GPT3 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MODE 3				CLR3	EN3
Type											RW				WO	RW
Reset											0	0			0	0

Bit(s)	Name	Description
5:4	MODE3	**Operation mode of GPT3** 00: ONE-SHOT mode 01: REPEAT mode 10: KEEP-GO mode 11: FREERUN mode
1	CLR3	**Clears the counter of GPT3 to 0** 0: No effect 1: Clear
0	EN3	**Enables GPT3** 0: Disable 1: Enable

10008034 GPT3_CLK **GPT3 Clock Setting** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLK3	CLKDIV3			
Type												RW	RW			
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	CLK3	**Sets up clock source of GPT3** 0: System clock (13MHz) 1: RTC clock (32kHz)
3:0	CLKDIV3	**Setting of GPT3 input clock frequency divider** 0000: Clock source divided by 1

Bit(s)	Name	Description
		0001: Clock source divided by 2 0010: Clock source divided by 3 0011: Clock source divided by 4 0100: Clock source divided by 5 0101: Clock source divided by 6 0110: Clock source divided by 7 0111: Clock source divided by 8 1000: Clock source divided by 9 1001: Clock source divided by 10 1010: Clock source divided by 11 1011: Clock source divided by 12 1100: Clock source divided by 13 1101: Clock source divided by 16 1110: Clock source divided by 32 1111: Clock source divided by 64

10008038 GPT3_COUNT **GPT3 Counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COUNTER3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNTER3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COUNTER3	Timer counter of GPT3

1000803C GPT3_COMPARE **GPT3 Compare Value** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMPARE3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMPARE3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COMPARE3	Compare value of GPT3

10008040 GPT4_CON **GPT4 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MODE 4				CLR4	EN4
Type											RW				WO	RW
Reset											0	0			0	0

Bit(s)	Name	Description
5:4	MODE4	**Operation mode of GPT4** 00: ONE-SHOT mode 01: REPEAT mode 10: KEEP-GO mode 11: FREERUN mode
1	CLR4	**Clears the counter of GPT4 to 0** 0: No effect 1: Clear
0	EN4	**Enables GPT4** 0: Disable 1: Enable

10008044 GPT4_CLK GPT4 Clock Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLK4	CLKDIV4			
Type												RW	RW			
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	CLK4	**Sets up clock source of GPT4** 0: System clock (13MHz) 1: RTC clock (32kHz)
3:0	CLKDIV4	**Setting of GPT4 input clock frequency divider** 0000: Clock source divided by 1 0001: Clock source divided by 2 0010: Clock source divided by 3 0011: Clock source divided by 4 0100: Clock source divided by 5 0101: Clock source divided by 6 0110: Clock source divided by 7 0111: Clock source divided by 8 1000: Clock source divided by 9 1001: Clock source divided by 10 1010: Clock source divided by 11 1011: Clock source divided by 12 1100: Clock source divided by 13 1101: Clock source divided by 16 1110: Clock source divided by 32 1111: Clock source divided by 64

10008048 GPT4_COUNT **GPT4 Counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COUNTER4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNTER4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COUNTER4	Timer counter of GPT4

1000804C GPT4_COMPARE **GPT4 Compare Value** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMPARE4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMPARE4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COMPARE4	Compare value of GPT4

10008050 GPT5_CON **GPT5 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MODE 5				CLR5	EN5
Type											RW				WO	RW
Reset											0	0			0	0

Bit(s)	Name	Description
5:4	MODE5	**Operation mode of GPT5** 00: ONE-SHOT mode 01: REPEAT mode 10: KEEP-GO mode 11: FREERUN mode
1	CLR5	**Clears the counter of GPT5 to 0** 0: No effect 1: Clear
0	EN5	**Enables GPT5** 0: Disable

Bit(s)	Name	Description
		1: Enable

10008054 GPT5_CLK **GPT5 Clock Setting** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLK5	CLKDIV5			
Type												RW	RW			
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	CLK5	**Sets up clock source of GPT5** 0: System clock (13MHz) 1: RTC clock (32kHz)
3:0	CLKDIV5	**Setting of GPT5 input clock frequency divider** 0000: Clock source divided by 1 0001: Clock source divided by 2 0010: Clock source divided by 3 0011: Clock source divided by 4 0100: Clock source divided by 5 0101: Clock source divided by 6 0110: Clock source divided by 7 0111: Clock source divided by 8 1000: Clock source divided by 9 1001: Clock source divided by 10 1010: Clock source divided by 11 1011: Clock source divided by 12 1100: Clock source divided by 13 1101: Clock source divided by 16 1110: Clock source divided by 32 1111: Clock source divided by 64

10008058 GPT5_COUNT **GPT5 Counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COUNTER5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNTER5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COUNTER5	Timer counter of GPT5

1000805C GPT5_COMPARE — GPT5 Compare Value — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMPARE5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMPARE5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COMPARE5	Compare value of GPT5

10008060 GPT6_CON — GPT6 Control — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MODE 6				CLR6	EN6
Type											RW				WO	RW
Reset											0	0			0	0

Bit(s)	Name	Description
5:4	MODE6	**Operation mode of GPT6** 00: ONE-SHOT mode 01: REPEAT mode 10: KEEP-GO mode 11: FREERUN mode
1	CLR6	**Clears the counter of GPT6 to 0** 0: No effect 1: Clear
0	EN6	**Enables GPT6** 0: Disable 1: Enable

10008064 GPT6_CLK — GPT6 Clock Setting — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLK6	CLKDIV6			
Type												RW	RW			
Reset												0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
4	CLK6	**Sets up clock source of GPT6** 0: System clock (13MHz) 1: RTC clock (32kHz)
3:0	CLKDIV6	**Setting of GPT6 input clock frequency divider** 0000: Clock source divided by 1 0001: Clock source divided by 2 0010: Clock source divided by 3 0011: Clock source divided by 4 0100: Clock source divided by 5 0101: Clock source divided by 6 0110: Clock source divided by 7 0111: Clock source divided by 8 1000: Clock source divided by 9 1001: Clock source divided by 10 1010: Clock source divided by 11 1011: Clock source divided by 12 1100: Clock source divided by 13 1101: Clock source divided by 16 1110: Clock source divided by 32 1111: Clock source divided by 64

10008068 GPT6_COUNTL **GPT6 Counter L** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COUNTER6L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNTER6L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COUNTER6L	**Lower word of timer count of GPT6** The read operation of GPT6_COUNTL will make GPT6_COUNTH fixed until the next read operation of GPT6_COUNTL.

1000806C GPT6_COMPAREL **GPT6 Compare Value L** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMPARE6L															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMPARE6L															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
31:0	COMPARE6L	Lower word of compare value of GPT6

10008078 GPT6_COUNTH **GPT6 Counter L** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COUNTER6H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNTER6H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COUNTER6H	Higher word of timer count of GPT6

1000807C GPT6_COMPAREH **GPT6 Compare Value H** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMPARE6H															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMPARE6H															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COMPARE6H	Higher word of compare of GPT6

10008080 APXGPT_IRQMASK0 **APMCU IRQMASK Register** **00000004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											IRQ_MSK0					
Type											RW					
Reset											0	0	0	1	0	0

Bit(s)	Name	Description
5:0	IRQ_MSK0	By default, APMCU will not receive GPT3's interrupt.

10008084 APXGPT_IRQMASK1 MD32 IRQMASK Register 0000003B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											IRQ_MSK1					
Type											RW					
Reset											1	1	1	0	1	1

Bit(s)	Name	Description
5:0	IRQ_MSK1	By default, MD32 will only receive GPT3's interrupt.

10008090 APXGPT_SW_CG Software Clock Gating 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											SW_CG6	SW_CG5	SW_CG4	SW_CG3	SW_CG2	SW_CG1
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5	SW_CG6	**Stop GPT6's clock if this bit is enabled.** 0: Disable 1: Enable
4	SW_CG5	**Stop GPT5's clock if this bit is enabled.** 0: Disable 1: Enable
3	SW_CG4	**Stop GPT4's clock if this bit is enabled.** 0: Disable 1: Enable
2	SW_CG3	**Stop GPT3's clock if this bit is enabled.** 0: Disable 1: Enable
1	SW_CG2	**Stop GPT2's clock if this bit is enabled.** 0: Disable 1: Enable
0	SW_CG1	**Stop GPT1's clock if this bit is enabled.** 0: Disable 1: Enable

3.12 IRTX

Module name: irtx Base address: (+1101d000h)

Address	Name	Width	Register Function
1101D000	IRTXCFG	32	IRTX Configuration Register
1101D004	IRTXD0	32	IRTX Transmission Data 0 Register
1101D008	IRTXD1	32	IRTX Transmission Data 1 Register
1101D00C	IRTXD2	32	IRTX Transmission Data 2 Register
1101D010	IRTX_L0H	32	IRTX Logic 0 High Period Register
1101D014	IRTX_L0L	32	IRTX Logic 0 Low Period Register
1101D018	IRTX_L1H	32	IRTX Logic 1 High Period Register
1101D01C	IRTX_L1L	32	IRTX Logic 1 Low Period Register
1101D020	IRTXSYNCH	32	IRTX Sync High Period Register
1101D024	IRTXSYNCL	32	IRTX Sync Low Period Register
1101D028	IRTXMT	32	IRTX Modulation Parameter Register

1101D000 IRTXCFG IRTX Configuration Register 00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																HW_DCM
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_INV	IRTX_BITNUM							IRTX_IRINV	IRTX_IROS	IRTX_RODR	IRTX_BODR	IRTX_SWO	IRTX_MODE		IRTX_STRT
Type	RW	RW							RW	RW	RW	RW	RW	RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		HW_DCM	**Enables hardware DCM** Set this bit to 1 to enable hardware DCM. Set this bit to 0 to disable hardware DCM.
15		DATA_INV	**IR N inverter** Set this bit to 1 to invert the IR data waveform only.
14:8		IRTX_BITNUM	**Bit number** Number of IR bits to be transmitted
7		IRTX_IRINV	**IR inverter** Set this bit to 1 to invert IR output.
6		IRTX_IROS	**Selects IR output** 0: IR output is IRTX baseband signal. 1: IR output is IRTX modulated signal.
5		IRTX_RODR	**Register transmission order** 0: IRTX_R0 first, IRTX_R11 last (R0, R1 ~ R11) 1: IRTX_R11 first, IRTX_R0 last (R11, R10 ~R0)
4		IRTX_BODR	**Bit transmission order** 0: MSB first, LSB last (ex. R0[7], R0[6] ~ R0[0]) 1: LSB first, MSB last (ex. R0[0], R0[1] ~ R0[7])
3		IRTX_SWO	**Software output bit** When the IRTX output protocol is set to software mode, the IR output will be the same as SWO.
2:1		IRTX_MODE	**IR output protocol** 0: Pulse-width coded protocol

Bit(s)	Mnemonic	Name	Description
0		IRTX_STRT	1: RC5 protocol 2: RC6 protocol 3: Software mode **IR trigger bit** 0: IR code transfer completed 1: Start to transfer IR code When IRTX output protocol is set to software mode, this bit will be set to 0 to terminate IR transmission.

1101D004 IRTXD0 **IRTX Transmission Data 0 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRTX_R3								IRTX_R2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_R1								IRTX_R0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		IRTX_R3	IRTX byte 3
23:16		IRTX_R2	IRTX byte 2
15:8		IRTX_R1	IRTX byte 1
7:0		IRTX_R0	IRTX byte 0

1101D008 IRTXD1 **IRTX Transmission Data 1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRTX_R7								IRTX_R6							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_R5								IRTX_R4							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		IRTX_R7	IRTX byte 7
23:16		IRTX_R6	IRTX byte 6
15:8		IRTX_R5	IRTX byte 5
7:0		IRTX_R4	IRTX byte 4

1101D00C IRTXD2 **IRTX Transmission Data 2 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRTX_R11								IRTX_R10							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_R9								IRTX_R8							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		IRTX_R11	IRTX byte 11
23:16		IRTX_R10	IRTX byte 10
15:8		IRTX_R9	IRTX byte 9
7:0		IRTX_R8	IRTX byte 8

1101D010 IRTX_L0H IRTX Logic 0 High Period Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									IRTX_L0H							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_L0H															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		IRTX_L0H	**Logic 0 pulse high period** The period is equal to L0H/27MHz. This register is also valid in RC5/RC6 protocol. RC5 T = 24000, so T = 24000/27MHz = 0.889ms

1101D014 IRTX_L0L IRTX Logic 0 Low Period Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									IRTX_L0L							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_L0L															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		IRTX_L0L	**Logic 0 pulse low period** The period is equal to L0L/27MHz. When in SWO, bit[2:0] indicates which PWM channel is selected.

1101D018 IRTX_L1H IRTX Logic 1 High Period Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name									IRTX_L1H							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_L1H															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		IRTX_L1H	**Logic 1 pulse high period** The period is equal to L1H/27MHz.

1101D01C IRTX_L1L **IRTX Logic 1 Low Period Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									IRTX_L1L							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_L1L															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		IRTX_L1L	**Logic 1 pulse low period** The period is equal to L1L/27MHz.

1101D020 IRTXSYNCH **IRTX Sync High Period Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									IRTX_SYNCH							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_SYNCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		IRTX_SYNCH	**SYNCH leading pulse high period** The period is equal to SYNCH/27MHz. SYNCH will be ignored if RC5/RC6 protocol is adopted.

1101D024 IRTXSYNCL **IRTX Sync Low Period Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									IRTX_SYNCL							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_SYNCL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		IRTX_SYNCL	**SYNCL leading pulse low period** The period is equal to SYNCL/27MHz. SYNCL will be ignored if RC5/RC6 protocol is adopted.

1101D028 IRTXMT **IRTX Modulation Parameter Register** **00E602B2**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRTX_CDT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_CWT															
Type	RW															
Reset	0	0	0	0	0	0	1	0	1	0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
31:16		IRTX_CDT	**Carrier waveform duty time** Duty cycle = CDT/CWT Default duty cycle = 230/690 =33%
15:0		IRTX_CWT	**Carrier waveform period**

3.13 Audio System

Module name: AFE Base address: (+11220000h)

Address	Name	Width	Register Function
11220000	AUDIO_TOP_CON0	32	Audio Top Control Register 0
11220004	AUDIO_TOP_CON1	32	Audio Top Control Register 1
1122000C	AUDIO_TOP_CON3	32	Audio Top Control Register 3
11220010	AFE_DAC_CON0	32	AFE Control Register 0
11220014	AFE_DAC_CON1	32	AFE Control Register 1
11220018	AFE_I2S_CON	32	AFE I2S Control Register 0
1122001C	AFE_DAIBT_CON0	32	AFE DAI/BT Control Register 0
11220020	AFE_CONN0	32	AFE Connection Register 0
11220024	AFE_CONN1	32	AFE Connection Register 1
11220028	AFE_CONN2	32	AFE Connection Register 2
1122002C	AFE_CONN3	32	AFE Connection Register 3
11220030	AFE_CONN4	32	AFE Connection Register 4
1122005C	AFE_CONN5	32	AFE Connection Register 5
112200BC	AFE_CONN6	32	AFE Connection Register 6
11220420	AFE_CONN7	32	AFE Connection Register 7
11220438	AFE_CONN8	32	AFE Connection Register 8
11220440	AFE_CONN9	32	AFE Connection Register 9
11220444	AFE_CONN10	32	AFE Connection Register 10
11220448	AFE_CONN11	32	AFE Connection Register 11
1122044C	AFE_CONN12	32	AFE Connection Register 12
11220450	AFE_CONN13	32	AFE Connection Register 13
11220454	AFE_CONN14	32	AFE Connection Register 14
11220458	AFE_CONN15	32	AFE Connection Register 15
1122045C	AFE_CONN16	32	AFE Connection Register 16
11220460	AFE_CONN17	32	AFE Connection Register 17
11220464	AFE_CONN18	32	AFE Connection Register 18
11220468	AFE_CONN19	32	AFE Connection Register 19
1122046C	AFE_CONN20	32	AFE Connection Register 20
11220470	AFE_CONN21	32	AFE Connection Register 21
11220474	AFE_CONN22	32	AFE Connection Register 22
11220478	AFE_CONN23	32	AFE Connection Register 23
1122047C	AFE_CONN24	32	AFE Connection Register 24
112204B0	AFE_CONN25	32	AFE Connection Register 25
112204B4	AFE_CONN26	32	AFE Connection Register 26
112204B8	AFE_CONN27	32	AFE Connection Register 27
112204BC	AFE_CONN28	32	AFE Connection Register 28
112204C0	AFE_CONN29	32	AFE Connection Register 29
11220494	AFE_CONN_RS	32	AFE Connection Right Shift Register
11220498	AFE_CONN_DI	32	AFE Connection Dithering Register
11220034	AFE_I2S_CON1	32	AFE I2S Control Register 1
11220038	AFE_I2S_CON2	32	AFE I2S Control Register 2
1122003C	AFE_MRGIF_CON	32	AFE Merge Interface Control Register
11220040	AFE_DL1_BASE	32	AFE DL1 Base Address Register

Address	Name	Width	Register Function
11220044	AFE_DL1_CUR	32	AFE DL1 Cursor Register
11220048	AFE_DL1_END	32	AFE_DL1_END
1122004C	AFE_I2S_CON3	32	AFE I2S Control Register 3
11220050	AFE_DL2_BASE	32	AFE DL2 Base Address Register
11220054	AFE_DL2_CUR	32	AFE DL2 Cursor Register
11220058	AFE_DL2_END	32	AFE_DL2_END
11220360	AFE_DL3_BASE	32	AFE DL3 Base Address Register
11220364	AFE_DL3_CUR	32	AFE DL3 Cursor Register
11220368	AFE_DL3_END	32	AFE_DL3_END
1122006C	AFE_CONN_24BIT	32	AFE Connection 24-bit Register
11220070	AFE_AWB_BASE	32	AFE AWB Base Address Register
11220078	AFE_AWB_END	32	AFE AWB End Address Register
1122007C	AFE_AWB_CUR	32	AFE AWB Cursor Register
11220080	AFE_VUL_BASE	32	AFE VUL Base Address Register
11220088	AFE_VUL_END	32	AFE VUL End Address Register
1122008C	AFE_VUL_CUR	32	AFE VUL Cursor Register
11220090	AFE_DAI_BASE	32	AFE DAI Base Address Register
1122009C	AFE_DAI_CUR	32	AFE DAI Cursor Register
11220098	AFE_DAI_END	32	AFE_DAI_END
112200CC	AFE_MEMIF_MSB	32	AFE Memory Interface MSB Register
112200D0	AFE_MEMIF_MON0	32	AFE Memory Interface Monitor Register 0
112200D4	AFE_MEMIF_MON1	32	AFE Memory Interface Monitor Register 1
112200D8	AFE_MEMIF_MON2	32	AFE Memory Interface Monitor Register 2
112200E0	AFE_MEMIF_MON4	32	AFE Memory Interface Monitor Register 4
112201D0	AFE_SIDETONE_DEBUG	32	Side-Tone Debug
112201D4	AFE_SIDETONE_MON	32	Side-Tone Debug Monitor
112201E0	AFE_SIDETONE_CON0	32	Side-Tone Control Port 0
112201E4	AFE_SIDETONE_COEFF	32	Side-Tone coefficient Port
112201E8	AFE_SIDETONE_CON1	32	Side-Tone Control Port 1
112201EC	AFE_SIDETONE_GAIN	32	Side-Tone Gain Port
112201F0	AFE_SGEN_CON0	32	AFE Sine-Wave Gen Config 0
11220200	AFE_TOP_CON0	32	AFE Top Control Register 0
11220330	AFE_MOD_DAI_BASE	32	AFE MOD_DAI Base Address Register
11220338	AFE_MOD_DAI_END	32	AFE_MOD_DAI_END
1122033C	AFE_MOD_DAI_CUR	32	AFE MOD_DAI Cursor Register
11220350	AFE_VUL_D2_BASE	32	AFE VUL_D2 Base Address Register
11220358	AFE_VUL_D2_END	32	AFE VUL_D2 End Address Register
1122035C	AFE_VUL_D2_CUR	32	AFE VUL_D2 Cursor Register
112203A0	AFE_IRQ_MCU_CON	32	AFE IRQ MCU Control Register

Address	Name	Width	Register Function
112203A4	AFE_IRQ_MCU_STATUS	32	AFE IRQ MCU Status Register
112203A8	AFE_IRQ_MCU_CLR	32	AFE IRQ Clear Register
112203AC	AFE_IRQ_MCU_CNT1	32	AFE IRQ1 MCU Counter Register
112203B0	AFE_IRQ_MCU_CNT2	32	AFE IRQ2 MCU Counter Register
112203B4	AFE_IRQ_MCU_EN	32	AFE IRQ MCU Enable Register
112203B8	AFE_IRQ_MCU_MON2	32	AFE IRQ MCU MON2 Register
112203C0	AFE_IRQ1_MCU_CNT_MON	32	AFE IRQ1 MCU Count Monitor Register
112203C4	AFE_IRQ2_MCU_CNT_MON	32	AFE IRQ2 MCU Count Monitor Register
112203C8	AFE_IRQ1_MCU_EN_CNT_MON	32	AFE IRQ1 MCU Enable Count Monitor Register
112203D0	AFE_MEMIF_MINLEN	32	AFE MEMIF Min BLength Register
112203D4	AFE_MEMIF_MAXLEN	32	AFE MEMIF Max BLength Register
112203D8	AFE_MEMIF_PBUF_SIZE	32	AFE MEMIF Prefecth Buffer Size
112203F8	AFE_MEMIF_HD_MODE	32	AFE MEMIF HD Mode Register
112203FC	AFE_MEMIF_HDALIGN	32	AFE MEMIF HD ALIGN Register
112203DC	AFE_IRQ_MCU_CNT7	32	AFE IRQ7 MCU Counter Register
112203F0	AFE_APLL1_TUNER_CFG	32	AFE Tuner Control Register
112203F4	AFE_APLL2_TUNER_CFG	32	AFE Tuner 2 Control Register
11220410	AFE_GAIN1_CON0	32	AFE Gain 1 Control Register 0
11220414	AFE_GAIN1_CON1	32	AFE Gain 1 Control Register 1
11220418	AFE_GAIN1_CON2	32	AFE Gain 1 Control Register 2
1122041C	AFE_GAIN1_CON3	32	AFE Gain 1 Control Register 3
11220424	AFE_GAIN1_CUR	32	AFE Gain 1 Cursor Register
11220428	AFE_GAIN2_CON0	32	AFE Gain 2 Control Register 0
1122042C	AFE_GAIN2_CON1	32	AFE Gain 2 Control Register 1
11220430	AFE_GAIN2_CON2	32	AFE Gain 2 Control Register 2
11220434	AFE_GAIN2_CON3	32	AFE Gain 2 Control Register 3
1122043C	AFE_GAIN2_CUR	32	AFE Gain 2 Cursor Register
11220500	AFE_ASRC_CON0	32	ASRC Config 0
11220504	AFE_ASRC_CON1	32	ASRC Config 1
11220508	AFE_ASRC_CON2	32	ASRC Config 2
1122050C	AFE_ASRC_CON3	32	ASRC Config 3
11220510	AFE_ASRC_CON4	32	ASRC Config 4
11220514	AFE_ASRC_CON5	32	ASRC Config 5
11220518	AFE_ASRC_CON6	32	ASRC Config 6
1122051C	AFE_ASRC_CON7	32	ASRC Config 7

Address	Name	Width	Register Function
11220520	AFE_ASRC_CON8	32	ASRC Config 8
11220524	AFE_ASRC_CON9	32	ASRC Config 9
11220528	AFE_ASRC_CON10	32	ASRC Config 10
1122052C	AFE_ASRC_CON11	32	ASRC Config 11
11220530	PCM_INTF_CON1	32	PCM Interface Config 1
11220538	PCM_INTF_CON2	32	PCM Interface Config 2
1122053C	PCM2_INTF_CON	32	PCM2 Interface Config
11220550	AFE_ASRC_CON13	32	ASRC Config 13
11220554	AFE_ASRC_CON14	32	ASRC Config 14
11220558	AFE_ASRC_CON15	32	ASRC Config 15
1122055C	AFE_ASRC_CON16	32	ASRC Config 16
11220560	AFE_ASRC_CON17	32	ASRC Config 17
11220564	AFE_ASRC_CON18	32	ASRC Config 18
11220568	AFE_ASRC_CON19	32	ASRC Config 19
1122056C	AFE_ASRC_CON20	32	ASRC Config 20
11220570	AFE_ASRC_CON21	32	ASRC Config 21
11220108	AFE_ADDA_DL_SRC2_CON0	32	AFE_DL_SRC2 Control Register 0
1122010C	AFE_ADDA_DL_SRC2_CON1	32	AFE_DL_SRC2 Control Register 1 Part
11220114	AFE_ADDA_UL_SRC_CON0	32	AFE Uplink SRC Control Register 0 Part
11220118	AFE_ADDA_UL_SRC_CON1	32	AFE Uplink SRC Control Register 1 Part
11220120	AFE_ADDA_TOP_CON0	16	AFE Top Control Register 0
11220124	AFE_ADDA_UL_DL_CON0	16	Audio UL and DL Control Register 0
1122012C	AFE_ADDA_SRC_DEBUG	32	AFE UL Debug Control
11220130	AFE_ADDA_SRC_DEBUG_MON0	32	AFE Uplink SRC Monitor Register 0
11220134	AFE_ADDA_SRC_DEBUG_MON1	32	AFE Downlink SRC Monitor Register 1
11220138	AFE_ADDA_NEWIF_CFG0	32	AFE MTK ADDA NEWIF Control Register 0
1122013C	AFE_ADDA_NEWIF_CFG1	32	AFE MTK ADDA NEWIF Control Register 1
11220140	AFE_ADDA_NEWIF_CFG2	32	AFE MTK ADDA NEWIF Control Register 2
11220600	AFE_ADDA2_TOP_CON0	32	EVEREST HPANC control register
11220260	AFE_ADDA_PREDIS_CON0	32	AFE Pre-distortion Control Port 0 High Part
11220264	AFE_ADDA_PREDIS_CON1	32	AFE Pre-distortion Control Port 1 High Part
11220270	AFE_MRGIF_MON0	32	AFE Merge Interface Monitor Register 0
11220274	AFE_MRGIF_MON1	32	AFE Merge Interface Monitor Register 1
11220278	AFE_MRGIF_MON2	32	AFE Merge Interface Monitor Register 2
1122027C	AFE_I2S_MON	32	EVEREST FM Connsys Debug Signal

Address	Name	Width	Register Function
112206C0	AFE_ASRC4_CON0	32	ASRC4 Config 0
112206C4	AFE_ASRC4_CON1	32	ASRC4 Config 1
112206C8	AFE_ASRC4_CON2	32	ASRC4 Config 2
112206CC	AFE_ASRC4_CON3	32	ASRC4 Config 3
112206D0	AFE_ASRC4_CON4	32	ASRC4 Config 4
112206D4	AFE_ASRC4_CON5	32	ASRC4 Config 5
112206D8	AFE_ASRC4_CON6	32	ASRC4 Config 6
112206DC	AFE_ASRC4_CON7	32	ASRC4 Config 7
112206E0	AFE_ASRC4_CON8	32	ASRC4 Config 8
112206E4	AFE_ASRC4_CON9	32	ASRC4 Config 9
112206E8	AFE_ASRC4_CON10	32	ASRC4 Config 10
112206EC	AFE_ASRC4_CON11	32	ASRC4 Config 11
112206F0	AFE_ASRC4_CON12	32	ASRC4 Config 12
112206F4	AFE_ASRC4_CON13	32	ASRC4 Config 13
112206F8	AFE_ASRC4_CON14	32	ASRC4 Config 14
11220700	AFE_ASRC2_CON0	32	ASRC2 Config 0
11220704	AFE_ASRC2_CON1	32	ASRC2 Config 1
11220708	AFE_ASRC2_CON2	32	ASRC2 Config 2
1122070C	AFE_ASRC2_CON3	32	ASRC2 Config 3
11220710	AFE_ASRC2_CON4	32	ASRC2 Config 4
11220714	AFE_ASRC2_CON5	32	ASRC2 Config 5
11220718	AFE_ASRC2_CON6	32	ASRC2 Config 6
1122071C	AFE_ASRC2_CON7	32	ASRC2 Config 7
11220720	AFE_ASRC2_CON8	32	ASRC2 Config 8
11220724	AFE_ASRC2_CON9	32	ASRC2 Config 9
11220728	AFE_ASRC2_CON10	32	ASRC2 Config 10
1122072C	AFE_ASRC2_CON11	32	ASRC2 Config 11
11220730	AFE_ASRC2_CON12	32	ASRC2 Config 12
11220734	AFE_ASRC2_CON13	32	ASRC2 Config 13
11220738	AFE_ASRC2_CON14	32	ASRC2 Config 14
11220740	AFE_ASRC3_CON0	32	ASRC3 Config 0
11220744	AFE_ASRC3_CON1	32	ASRC3 Config 1
11220748	AFE_ASRC3_CON2	32	ASRC3 Config 2
1122074C	AFE_ASRC3_CON3	32	ASRC3 Config 3
11220750	AFE_ASRC3_CON4	32	ASRC3 Config 4
11220754	AFE_ASRC3_CON5	32	ASRC3 Config 5
11220758	AFE_ASRC3_CON6	32	ASRC3 Config 6
1122075C	AFE_ASRC3_CON7	32	ASRC3 Config 7
11220760	AFE_ASRC3_CON8	32	ASRC3 Config 8
11220764	AFE_ASRC3_CON9	32	ASRC3 Config 9
11220768	AFE_ASRC3_CON10	32	ASRC3 Config 10
1122076C	AFE_ASRC3_CON11	32	ASRC3 Config 11
11220770	AFE_ASRC3_CON12	32	ASRC3 Config 12
11220774	AFE_ASRC3_CON13	32	ASRC2 Config 13
11220778	AFE_ASRC3_CON14	32	ASRC2 Config 14
112205A0	CLK_AUDDIV_0	32	Audio Clock Selection Register 0

Address	Name	Width	Register Function
112205A4	CLK_AUDDIV_1	32	Audio Clock Selection Register 1
112205A8	CLK_AUDDIV_2	32	Audio Clock Selection Register 2
112205AC	CLK_AUDDIV_3	32	Audio Clock Selection Register 3
11220150	AFE_DMA_CTL	32	AFE DMA Selection Register
11220154	AFE_DMA_MON0	32	AFE DMA Monitor 0 Register
11220158	AFE_DMA_MON1	32	AFE DMA Monitor 1 Regsiter
112203E0	AFE_IRQ7_MCU_CNT_MON	32	AFE IRQ7 MCU Count Monitor Register
112203E4	AFE_IRQ_MCU_CNT3	32	AFE IRQ3 MCU Counter Register
112203E8	AFE_IRQ_MCU_CNT4	32	AFE IRQ4 MCU Counter Register
11220398	AFE_IRQ3_MCU_CNT_MON	32	AFE IRQ3 MCU Count Monitor Register
1122039C	AFE_IRQ4_MCU_CNT_MON	32	AFE IRQ4 MCU Count Monitor Register
112205C8	AUDIO_TOP_DBG_CON	32	Audio Top IP Debug Control
112205CC	AUDIO_TOP_DBG_MON0	32	Audio Top IP Debug Monitor 0
112205D0	AUDIO_TOP_DBG_MON1	32	Audio Top IP Debug Monitor 1
112205D4	AUDIO_TOP_DBG_MON2	32	Audio Top IP Debug Monitor 2
11220800	AFE_GENERAL_REG0	32	Audio General Purpose Register 0
11220804	AFE_GENERAL_REG1	32	Audio General Purpose Register 1
11220808	AFE_GENERAL_REG2	32	Audio General Purpose Register 2
1122080C	AFE_GENERAL_REG3	32	Audio General Purpose Register 3
11220810	AFE_GENERAL_REG4	32	Audio General Purpose Register 4
11220814	AFE_GENERAL_REG5	32	Audio General Purpose Register 5
11220818	AFE_GENERAL_REG6	32	Audio General Purpose Register 6
1122081C	AFE_GENERAL_REG7	32	Audio General Purpose Register 7
11220820	AFE_GENERAL_REG8	32	Audio General Purpose Register 8
11220824	AFE_GENERAL_REG9	32	Audio General Purpose Register 9
11220828	AFE_GENERAL_REG10	32	Audio General Purpose Register 10
1122082C	AFE_GENERAL_REG11	32	Audio General Purpose Register 11
11220830	AFE_GENERAL_REG12	32	Audio General Purpose Register 12
11220834	AFE_GENERAL_REG13	32	Audio General Purpose Register 13
11220838	AFE_GENERAL_RE	32	Audio General Purpose Register 14

Address	Name	Width	Register Function
	G14		
1122083C	AFE_GENERAL_REG15	32	Audio General Purpose Register 15
112203BC	AFE_IRQ_MCU_CNT5	32	AFE IRQ5 MCU Counter Register
112203CC	AFE_IRQ5_MCU_CNT_MON	32	AFE IRQ5 MCU Count Monitor Register
11220548	AFE_TDM_CON1	32	AFE TDM Config 1
1122054C	AFE_TDM_CON2	32	AFE TDM Config 2
11220370	AFE_HDMI_OUT_CON0	32	AFE HDMI_OUT Config Register
11220374	AFE_HDMI_BASE	32	AFE HDMI Base Address Register
11220378	AFE_HDMI_CUR	32	AFE HDMI Cursor Register
1122037C	AFE_HDMI_END	32	AFE HDMI End Address Register
11220390	AFE_HDMI_CONN0	32	AFE HDMI Output Connection Control Register 0
11220840	AFE_CBIP_CFG0	32	
11220844	AFE_CBIP_MON0	32	
11220848	AFE_CBIP_SLV_MUX_MON0	32	
1122084C	AFE_CBIP_SLV_DECODER_MON0	32	
112204F0	AFE_SRAM_DELSEL_CON0	32	Memory DELSEL Control 0
112204F4	AFE_SRAM_DELSEL_CON1	32	Memory DELSEL Control 1
112201FC	AFE_SINEGEN_CON_TDM	32	TDM SGEN control

11220000 AUDIO_TOP_CON0 Audio Top Control Register 0 801C4000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved	ahb_idle_en_int	ahb_idle_en_ext		pdn_tml	pdn_dac_predis	pdn_dac	pdn_adc				pdn_tdm_ck	PDN_APLL_TUNER	PDN_APLL2_TUNER		
Type	RW	RW	RW		RW	RW	RW	RW				RW	RW	RW		
Reset	1	0	0		0	0	0	0				1	1	1		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		APB3_SEL	APB_R2T	APB_W2T			PDN_24M	PDN_22M	PDN_adda4_adc	PDN_I2S				PDN_AFE		
Type		RW	RW	RW			RW	RW	RW	RW				RW		
Reset		1	0	0			0	0	0	0				0		

Bit(s)	Name	Description
31	Reserved	
30	ahb_idle_en_int	**Enables AHB idle for internal bus clock** 0: Disable 1: Enable
29	ahb_idle_en_ext	**Enables AHB idle for external bus clock** 0: Disable

Bit(s)	Name	Description
		1: Enable
27	pdn_tml	**Powers down ADDA ADC sine generator (test model) clock** 0: Does not power down ADDA ADC sine generator 1: Power down ADDA ADC sine generator
26	pdn_dac_predis	**Powers down ADDA DAC pre-distortion clock** 0: Does not power down ADDA DAC pre-distortion 1: Power down ADDA DAC pre-distortion
25	pdn_dac	**Powers down ADDA DAC clock** 0: Does not power down ADDA DAC 1: Power down ADDA DAC
24	pdn_adc	**Powers down ADDA ADC clock** 0: Does not power down ADDA ADC 1: Power down ADDA ADC
20	pdn_tdm_ck	**PDN control for TDM** 0: Power on TDM clock 1: Power down TDM clock
19	PDN_APLL_TUNER	**PDN control for apll tuner** 0: Power on apll_tuner clock 1: Power down apll_tuner clock
18	PDN_APLL2_TUNER	**PDN control for apll2 tuner** 0: Power on apll_tuner clock 1: Power down apll_tuner clock
14	APB3_SEL	**Uses APB 3.0 protocol** 0: Does not use APB 30 1: Use APB 30
13	APB_R2T	**Read cycle for APB write** 0: 1T 1: 2T
12	APB_W2T	**Read cycle for APB read** 0: 1T 1: 2T
9	PDN_24M	**PDN signal for low-jitter 24.576M clock** 0: Power on 24M clock 1: Power down 24M clock
8	PDN_22M	**PDN signal for low-jitter 22.5792M clock** 0: Power on 22M clock 1: Power down 22M clock
7	PDN_adda4_adc	**PDN signal for adda4 clock** 0: Power on ad4 clk 1: Power down adc4 clk
6	PDN_I2S	**PDN signal for I2S input clock** 0: Power on I2S input clock 1: Power down I2S input clock
2	PDN_AFE	**PDN signal for AFE clock** 0: Power on AFE clock 1: Power down AFE clock

11220004 AUDIO_TOP_CON1 Audio Top Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															pdn_adc_hires_tm	pdn_adc_hires

															1	
Type															RW	RW
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									I2S4_BCLK_SW_CG	I2S3_BCLK_SW_CG	I2S2_BCLK_SW_CG	I2S1_BCLK_SW_CG		I2S_SOFT_RST2	I2S_SOFT_RST	
Type									RW	RW	RW	RW		RW	RW	
Reset									0	0	0	0		0	0	

Bit(s)	Name	Description
17	pdn_adc_hires_tml	**Powers down ADDA ADC HIRES sine generator (test model) clock** 0: Does not power down ADDA ADC HIRES sine generator 1: Power down ADDA ADC HIRES sine generator
16	pdn_adc_hires	**Powers down ADDA ADC HIRES clock** 0: Does not power down ADDA ADC HIRES 1: Power down ADDA ADC HIRES
7	I2S4_BCLK_SW_CG	**Sets to 1 to gated I2S4 engine clock** 0: Not clock-gated 1: Clock-gated
6	I2S3_BCLK_SW_CG	**Sets to 1 to gated I2S3 engine clock** 0: Not clock-gated 1: Clock-gated
5	I2S2_BCLK_SW_CG	**Sets to 1 to gated I2S2 engine clock** 0: Not clock-gated 1: Clock-gated
4	I2S1_BCLK_SW_CG	**Sets to 1 to gated I2S1 engine clock** 0: Not clock-gated 1: Clock-gated
2	I2S_SOFT_RST2	**Soft reset bit for 4-wire DAC/ADC i2s mode** Set to 1 before configure AFE_I2S_CON1 and AFE_I2S_CON2. After finishing configure, release it to 0. 0: Normal 1: Soft reset
1	I2S_SOFT_RST	**Soft reset bit for 4-wire i2s mode** Set to 1 before configure AFE_I2S_CON and AFE_I2S_CON3. After finishing configure, release it to 0. 0: Normal 1: Soft reset

1122000C AUDIO_TOP_CON3 **Audio Top Control Register 3** **60000004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUSY	OS_DISABLE	CG_DISABLE													
Type	RW	RW	RW													
Reset	0	1	1													
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														Reserved		CLEAR_FLAG
Type														RW		RW

Reset														1		0

Bit(s)	Name	Description
31	BUSY	
30	OS_DISABLE	
29	CG_DISABLE	
2	Reserved	Reserved
0	CLEAR_FLAG	Clears slave bus decoding error flag

11220010 AFE_DAC_CON0 AFE Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_AWB_RETM	AFE_DL1_data2_RETM	AFE_DL2_RETM	AFE_DL1_RETM	AFE_ON_RETM	MOD_DAI_DUP_WR	DAI_MODE		VUL_data2_MODE				DL1_data2_MODE			
Type	RU	RU	RU	RU	RU	RW	RW		RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DL3_MODE				VUL_data2_R_MONO	VUL_data2_DATA	VUL_data2_ON	DL1_data2_ON	MOD_DAI_ON	AWB_ON	DL3_ON	DAI_ON	VUL_ON	DL2_ON	DL1_ON	AFE_ON
Type	RW				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	AFE_AWB_RETM	**Monitor signal for retiming of AWB_ON**
30	AFE_DL1_data2_RETM	**Monitor signal for retiming of DL1_data2_ON**
29	AFE_DL2_RETM	**Monitor signal for retiming of DL2_ON**
28	AFE_DL1_RETM	**Monitor signal for retiming of DL1_ON**
27	AFE_ON_RETM	**Monitor signal for retiming of AFE_ON**
26	MOD_DAI_DUP_WR	**Controls data write mode for modem PCM memory interface path** 0: Normal write 1: Duplicated write
25:24	DAI_MODE	**Controls the sampling frequency for DAI path** 0: 8k 1: 16k 2: 32k
23:20	VUL_data2_MODE	**Controls the sampling frequency for voice uplink data 2 path** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k

Bit(s)	Name	Description
19:16	DL1_data2_MODE	**Controls the sampling frequency for downlink 1 data 2 path** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k
15:12	DL3_MODE	**Controls the sampling frequency for downlink 3 path.** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k
11	VUL_data2_R_MONO	**Controls the data mono type for vocie uplink memory data 2 interface path** 0: Mono use L channel 1: Mono use R channel
10	VUL_data2_DATA	**Controls the data mode for voice uplink memory data 2 interface path** 0: Stereo 1: Mono
9	VUL_data2_ON	**Controls the enabling of uplink data 2 memory interface path** 0: Off 1: On
8	DL1_data2_ON	**Controls the enabling of downlink 1-data 2 memory interface path** 0: Off 1: On
7	MOD_DAI_ON	**Controls the enabling of modem PCM memory interface path** 0: Off 1: On
6	AWB_ON	**Controls the enabling of AWB memory interface path** 0: Off 1: On
5	DL3_ON	**Controls the enabling of DL3 memory interface path** 0: Off 1: On
4	DAI_ON	**Controls the enabling of DAI memory interface path**

Bit(s)	Name	Description
		0: Off 1: On
3	VUL_ON	**Controls the enabling of uplink memory interface path** 0: Off 1: On
2	DL2_ON	**Controls the enabling of downlink 2 memory interface path** 0: Off 1: On
1	DL1_ON	**Controls the enabling of downlink 1 memory interface path** 0: Off 1: On
0	AFE_ON	**Controls the enabling of the whole AFE module** 0: Off 1: On

11220014 AFE_DAC_CON1 **AFE Control Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MOD_DAI_MODE		DAI_DUP_WR	VUL_R_MONO	VUL_DATA	AXI_2X1_CG_DISABLE	AWB_R_MONO	AWB_DATA	DL3_DATA	DL2_DATA	DL1_DATA	DL1_data2_DATA	VUL_MODE			
Type	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AWB_MODE				I2S_MODE				DL2_MODE				DL1_MODE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	MOD_DAI_MODE	**Controls the sampling frequency for MOD_DAI path** 0: 8k 1: 16k 2: 32k
29	DAI_DUP_WR	**Controls the data write mode for DAI memory interface path** 0: Normal write 1: Duplicated write
28	VUL_R_MONO	**Controls the data mono type for vocie uplink memory interface path** 0: Mono use L channel 1: Mono use R channel
27	VUL_DATA	**Controls the data mode for voice uplink memory interface path** 0: Stereo 1: Mono
26	AXI_2X1_CG_DISABLE	0: Enable 1: Disable
25	AWB_R_MONO	**Controls the data mono type for audio write back memory interface path** 0: Mono use L channel 1: Mono use R channel

Bit(s)	Name	Description
24	AWB_DATA	**Controls the data mode for audio write back memory interface path** 0: Stereo 1: Mono
23	DL3_DATA	**Controls the data mode for downlink 3 memory interface path** 0: Stereo 1: Mono
22	DL2_DATA	**Controls the data mode for downlink 2 memory interface path** 0: Stereo 1: Mono
21	DL1_DATA	**Controls the data mode for downlink 1 memory interface path** 0: Stereo 1: Mono
20	DL1_data2_DATA	**Controls the data mode for downlink 1 data2 memory interface path** 0: Stereo 1: Mono
19:16	VUL_MODE	**Controls the sampling frequency for voice uplink path** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k
15:12	AWB_MODE	**Controls the sampling frequency for audio write back path** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 0111b: 130k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k 1111b: 260k
11:8	I2S_MODE	**Controls the sampling frequency for I2S path** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k

Bit(s)	Name	Description
		0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k
7:4	DL2_MODE	**Controls the sampling frequency for downlink 2 path** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k
3:0	DL1_MODE	**Controls the sampling frequency for downlink 1 path** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k

11220018 AFE_I2S_CON AFE I2S Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		BCK_NEG_LATCH	BCK_INV	I2SIN_PAD_SEL								I2S_LOOPBACK			I2S_ONOFF_NOT_RESET_CK_ENABLE	
Type		RW	RW	RW								RW			RW	
Reset		0	0	0								0			0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				I2S1_HD_EN					INV_PAD_CTRL	I2S_BYPSRC	INV_LRCK		I2S_FMT	I2S_SRC	I2S_WLEN	I2S_EN

Type				RW					RW	RW	RW		RW	RW	RW	RW
Reset				0					0	0	0		0	0	0	0

Bit(s)	Name	Description
30	BCK_NEG_EG_LATCH	**Controls I2S input data latching time** 0: Pos-edge latch 1: Neg-edge latch
29	BCK_INV	**Controls I2S output bck phase** 0: Not inverse bck 1: Inverse bck
28	I2SIN_PAD_SEL	**Controls I2S input source** If it's FM Rx i2s in, choose 0 from connsys. If mATV, choose 1 from io_mux. 0: I2S in from connsys 1: I2S in from io_mux
20	I2S_LOOPBACK	**Controls I2S internal loopback mode** Loopback source is from 2nd I2S output. 0: Normal I2S in 1: I2S in from internal 2nd I2S output
17	I2S_ONOFF_NOT_RESET_CK_ENABLE	**Controls I2S on/off to reset ck_enable or not** 0: On/off reset ck_enable 1: On/off not reset ck_enable
12	I2S1_HD_EN	**Enables low-jitter bck HD audio** 0: Normal h26m clock 1: Low-jitter clock
7	INV_PAD_CTRL	**Decides if the output enabling of I2S pads should be inverted** 0: No inverse 1: Invert
6	I2S_BYPSRC	**Bypasses SRC to I00 I01** 0: Not bypass 1: Bypass
5	INV_LRCK	**Controls the phase of I2S path** 0: Does not invert LRCK 1: Invert LRCK for LJ mode
3	I2S_FMT	**Controls the format for I2S path** 0: EIAJ 1: I2S
2	I2S_SRC	**Controls the master/slave for I2S path** 0: Master mode. Clock goes from AFE. 1: Slave mode. Clock receives from other devices.
1	I2S_WLEN	**Controls the word length of I2S** 0: 16 bits 1: 32 bits
0	I2S_EN	**Controls the enabling of I2S path** 0: Disable I2S 1: Enable I2S

1122001C AFE_DAIBT_CON0 AFE DAI/BT Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				USE_MRGIF_INPUT			DAIBT_MODE	DAI_SEL		BT_LEN			DATA_RDY	BTSYNC	BT_ON	DAIBT_ON
Type				RW			RW	RW		RW			RW	RW	RW	RW
Reset				0			0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
12	USE_MRGIF_INPUT	**Selects input data are from MRGIF or BT** 0: Off 1: On
9	DAIBT_MODE	**Selects data rate of DAI/BT** 0: 8k mode 1: 16k mode
8	DAI_SEL	**Selects H/L word received to DSP** Suggested: 0 0: High word ([31:16]) 1: Low word ([15:0])
6:4	BT_LEN	**Bluetooth PCM long frame sync length = BT_LEN + 1**
3	DATA_RDY	**Indicates DSP is ready to transmit data** 0: Not ready 1: Data ready
2	BTSYNC	**Bluetooth PCM frame sync type** 0: Not ready 1: Ready
1	BT_ON	**Controls the enabling of Bluetooth function** 0: Turn off BT. Turn on DAI if DAIBT_ON = 1 1: Turn on BT
0	DAIBT_ON	**Controls the enabling of DAI/BT function** 0: Disable DAI/BT 1: Enable DAI/BT

11220020 AFE_CONN0 AFE Connection Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I31_O00_S	I30_O00_S	I29_O00_S	I28_O00_S	I27_O00_S	I26_O00_S	I25_O00_S	I24_O00_S	I23_O00_S	I22_O00_S	I21_O00_S	I20_O00_S	I19_O00_S	I18_O00_S	I17_O00_S	I16_O00_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O00_S	I14_O00_S	I13_O00_S	I12_O00_S	I11_O00_S	I10_O00_S	I09_O00_S	I08_O00_S	I07_O00_S	I06_O00_S	I05_O00_S	I04_O00_S	I03_O00_S	I02_O00_S	I01_O00_S	I00_O00_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	I31_O00_S	**Controls the path from I31 to O00** 0: Off 1: On
30	I30_O00_S	**Controls the path from I30 to O00** 0: Off 1: On
29	I29_O00_S	**Controls the path from I29 to O00**

Bit(s)	Name	Description
		0: Off 1: On
28	I28_O00_S	**Controls the path from I28 to O00** 0: Off 1: On
27	I27_O00_S	**Controls the path from I27 to O00** 0: Off 1: On
26	I26_O00_S	**Controls the path from I26 to O00** 0: Off 1: On
25	I25_O00_S	**Controls the path from I25 to O00** 0: Off 1: On
24	I24_O00_S	**Controls the path from I24 to O00** 0: Off 1: On
23	I23_O00_S	**Controls the path from I23 to O00** 0: Off 1: On
22	I22_O00_S	**Controls the path from I22 to O00** 0: Off 1: On
21	I21_O00_S	**Controls the path from I21 to O00** 0: Off 1: On
20	I20_O00_S	**Controls the path from I20 to O00** 0: Off 1: On
19	I19_O00_S	**Controls the path from I19 to O00** 0: Off 1: On
18	I18_O00_S	**Controls the path from I18 to O00** 0: Off 1: On
17	I17_O00_S	**Controls the path from I17 to O00** 0: Off 1: On
16	I16_O00_S	**Controls the path from I16 to O00** 0: Off 1: On
15	I15_O00_S	**Controls the path from I15 to O00** 0: Off 1: On
14	I14_O00_S	**Controls the path from I14 to O00** 0: Off 1: On
13	I13_O00_S	**Controls the path from I13 to O00** 0: Off 1: On
12	I12_O00_S	**Controls the path from I12 to O00** 0: Off 1: On
11	I11_O00_S	**Controls the path from I11 to O00** 0: Off 1: On
10	I10_O00_S	**Controls the path from I10 to O00**

Bit(s)	Name	Description
		0: Off 1: On
9	I09_O00_S	**Controls the path from I09 to O00** 0: Off 1: On
8	I08_O00_S	**Controls the path from I08 to O00** 0: Off 1: On
7	I07_O00_S	**Controls the path from I07 to O00** 0: Off 1: On
6	I06_O00_S	**Controls the path from I06 to O00** 0: Off 1: On
5	I05_O00_S	**Controls the path from I05 to O00** 0: Off 1: On
4	I04_O00_S	**Controls the path from I04 to O00** 0: Off 1: On
3	I03_O00_S	**Controls the path from I03 to O00** 0: Off 1: On
2	I02_O00_S	**Controls the path from I02 to O00** 0: Off 1: On
1	I01_O00_S	**Controls the path from I01 to O00** 0: Off 1: On
0	I00_O00_S	**Controls the path from I00 to O00** 0: Off 1: On

11220024 AFE_CONN1 AFE Connection Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I31_O01_S	I30_O01_S	I29_O01_S	I28_O01_S	I27_O01_S	I26_O01_S	I25_O01_S	I24_O01_S	I23_O01_S	I22_O01_S	I21_O01_S	I20_O01_S	I19_O01_S	I18_O01_S	I17_O01_S	I16_O01_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O01_S	I14_O01_S	I13_O01_S	I12_O01_S	I11_O01_S	I10_O01_S	I09_O01_S	I08_O01_S	I07_O01_S	I06_O01_S	I05_O01_S	I04_O01_S	I03_O01_S	I02_O01_S	I01_O01_S	I00_O01_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	I31_O01_S	**Controls the path from I31 to O01** 0: Off 1: On
30	I30_O01_S	**Controls the path from I30 to O01** 0: Off 1: On
29	I29_O01_S	**Controls the path from I29 to O01**

Bit(s)	Name	Description
		0: Off 1: On
28	I28_O01_S	**Controls the path from I28 to O01** 0: Off 1: On
27	I27_O01_S	**Controls the path from I27 to O01** 0: Off 1: On
26	I26_O01_S	**Controls the path from I26 to O01** 0: Off 1: On
25	I25_O01_S	**Controls the path from I25 to O01** 0: Off 1: On
24	I24_O01_S	**Controls the path from I24 to O01** 0: Off 1: On
23	I23_O01_S	**Controls the path from I23 to O01** 0: Off 1: On
22	I22_O01_S	**Controls the path from I22 to O01** 0: Off 1: On
21	I21_O01_S	**Controls the path from I21 to O01** 0: Off 1: On
20	I20_O01_S	**Controls the path from I20 to O01** 0: Off 1: On
19	I19_O01_S	**Controls the path from I19 to O01** 0: Off 1: On
18	I18_O01_S	**Controls the path from I18 to O01** 0: Off 1: On
17	I17_O01_S	**Controls the path from I17 to O01** 0: Off 1: On
16	I16_O01_S	**Controls the path from I16 to O01** 0: Off 1: On
15	I15_O01_S	**Controls the path from I15 to O01** 0: Off 1: On
14	I14_O01_S	**Controls the path from I14 to O01** 0: Off 1: On
13	I13_O01_S	**Controls the path from I13 to O01** 0: Off 1: On
12	I12_O01_S	**Controls the path from I12 to O01** 0: Off 1: On
11	I11_O01_S	**Controls the path from I11 to O01** 0: Off 1: On
10	I10_O01_S	**Controls the path from I10 to O01**

Bit(s)	Name	Description
		0: Off 1: On
9	I09_O01_S	**Controls the path from I09 to O01** 0: Off 1: On
8	I08_O01_S	**Controls the path from I08 to O01** 0: Off 1: On
7	I07_O01_S	**Controls the path from I07 to O01** 0: Off 1: On
6	I06_O01_S	**Controls the path from I06 to O01** 0: Off 1: On
5	I05_O01_S	**Controls the path from I05 to O01** 0: Off 1: On
4	I04_O01_S	**Controls the path from I04 to O01** 0: Off 1: On
3	I03_O01_S	**Controls the path from I03 to O01** 0: Off 1: On
2	I02_O01_S	**Controls the path from I02 to O01** 0: Off 1: On
1	I01_O01_S	**Controls the path from I01 to O01** 0: Off 1: On
0	I00_O01_S	**Controls the path from I00 to O01** 0: Off 1: On

11220028 AFE_CONN2 AFE Connection Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I31_O02_S	I30_O02_S	I29_O02_S	I28_O02_S	I27_O02_S	I26_O02_S	I25_O02_S	I24_O02_S	I23_O02_S	I22_O02_S	I21_O02_S	I20_O02_S	I19_O02_S	I18_O02_S	I17_O02_S	I16_O02_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O02_S	I14_O02_S	I13_O02_S	I12_O02_S	I11_O02_S	I10_O02_S	I09_O02_S	I08_O02_S	I07_O02_S	I06_O02_S	I05_O02_S	I04_O02_S	I03_O02_S	I02_O02_S	I01_O02_S	I00_O02_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	I31_O02_S	**Controls the path from I31 to O02** 0: Off 1: On
30	I30_O02_S	**Controls the path from I30 to O02** 0: Off 1: On
29	I29_O02_S	**Controls the path from I29 to O02**

Bit(s)	Name	Description
		0: Off 1: On
28	I28_O02_S	**Controls the path from I28 to O02** 0: Off 1: On
27	I27_O02_S	**Controls the path from I27 to O02** 0: Off 1: On
26	I26_O02_S	**Controls the path from I26 to O02** 0: Off 1: On
25	I25_O02_S	**Controls the path from I25 to O02** 0: Off 1: On
24	I24_O02_S	**Controls the path from I24 to O02** 0: Off 1: On
23	I23_O02_S	**Controls the path from I23 to O02** 0: Off 1: On
22	I22_O02_S	**Controls the path from I22 to O02** 0: Off 1: On
21	I21_O02_S	**Controls the path from I21 to O02** 0: Off 1: On
20	I20_O02_S	**Controls the path from I20 to O02** 0: Off 1: On
19	I19_O02_S	**Controls the path from I19 to O02** 0: Off 1: On
18	I18_O02_S	**Controls the path from I18 to O02** 0: Off 1: On
17	I17_O02_S	**Controls the path from I17 to O02** 0: Off 1: On
16	I16_O02_S	**Controls the path from I16 to O02** 0: Off 1: On
15	I15_O02_S	**Controls the path from I15 to O02** 0: Off 1: On
14	I14_O02_S	**Controls the path from I14 to O02** 0: Off 1: On
13	I13_O02_S	**Controls the path from I13 to O02** 0: Off 1: On
12	I12_O02_S	**Controls the path from I12 to O02** 0: Off 1: On
11	I11_O02_S	**Controls the path from I11 to O02** 0: Off 1: On
10	I10_O02_S	**Controls the path from I10 to O02**

Bit(s)	Name	Description
		0: Off 1: On
9	I09_O02_S	**Controls the path from I09 to O02** 0: Off 1: On
8	I08_O02_S	**Controls the path from I08 to O02** 0: Off 1: On
7	I07_O02_S	**Controls the path from I07 to O02** 0: Off 1: On
6	I06_O02_S	**Controls the path from I06 to O02** 0: Off 1: On
5	I05_O02_S	**Controls the path from I05 to O02** 0: Off 1: On
4	I04_O02_S	**Controls the path from I04 to O02** 0: Off 1: On
3	I03_O02_S	**Controls the path from I03 to O02** 0: Off 1: On
2	I02_O02_S	**Controls the path from I02 to O02** 0: Off 1: On
1	I01_O02_S	**Controls the path from I01 to O02** 0: Off 1: On
0	I00_O02_S	**Controls the path from I00 to O02** 0: Off 1: On

1122002C AFE_CONN3 AFE Connection Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I31_O03_S	I30_O03_S	I29_O03_S	I28_O03_S	I27_O03_S	I26_O03_S	I25_O03_S	I24_O03_S	I23_O03_S	I22_O03_S	I21_O03_S	I20_O03_S	I19_O03_S	I18_O03_S	I17_O03_S	I16_O03_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O03_S	I14_O03_S	I13_O03_S	I12_O03_S	I11_O03_S	I10_O03_S	I09_O03_S	I08_O03_S	I07_O03_S	I06_O03_S	I05_O03_S	I04_O03_S	I03_O03_S	I02_O03_S	I01_O03_S	I00_O03_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	I31_O03_S	**Controls the path from I31 to O03** 0: Off 1: On
30	I30_O03_S	**Controls the path from I30 to O03** 0: Off 1: On
29	I29_O03_S	**Controls the path from I29 to O03**

Bit(s)	Name	Description
		0: Off 1: On
28	I28_O03_S	**Controls the path from I28 to O03** 0: Off 1: On
27	I27_O03_S	**Controls the path from I27 to O03** 0: Off 1: On
26	I26_O03_S	**Controls the path from I26 to O03** 0: Off 1: On
25	I25_O03_S	**Controls the path from I25 to O03** 0: Off 1: On
24	I24_O03_S	**Controls the path from I24 to O03** 0: Off 1: On
23	I23_O03_S	**Controls the path from I23 to O03** 0: Off 1: On
22	I22_O03_S	**Controls the path from I22 to O03** 0: Off 1: On
21	I21_O03_S	**Controls the path from I21 to O03** 0: Off 1: On
20	I20_O03_S	**Controls the path from I20 to O03** 0: Off 1: On
19	I19_O03_S	**Controls the path from I19 to O03** 0: Off 1: On
18	I18_O03_S	**Controls the path from I18 to O03** 0: Off 1: On
17	I17_O03_S	**Controls the path from I17 to O03** 0: Off 1: On
16	I16_O03_S	**Controls the path from I16 to O03** 0: Off 1: On
15	I15_O03_S	**Controls the path from I15 to O03** 0: Off 1: On
14	I14_O03_S	**Controls the path from I14 to O03** 0: Off 1: On
13	I13_O03_S	**Controls the path from I13 to O03** 0: Off 1: On
12	I12_O03_S	**Controls the path from I12 to O03** 0: Off 1: On
11	I11_O03_S	**Controls the path from I11 to O03** 0: Off 1: On
10	I10_O03_S	**Controls the path from I10 to O03**

Bit(s)	Name	Description
		0: Off 1: On
9	I09_O03_S	**Controls the path from I09 to O03** 0: Off 1: On
8	I08_O03_S	**Controls the path from I08 to O03** 0: Off 1: On
7	I07_O03_S	**Controls the path from I07 to O03** 0: Off 1: On
6	I06_O03_S	**Controls the path from I06 to O03** 0: Off 1: On
5	I05_O03_S	**Controls the path from I05 to O03** 0: Off 1: On
4	I04_O03_S	**Controls the path from I04 to O03** 0: Off 1: On
3	I03_O03_S	**Controls the path from I03 to O03** 0: Off 1: On
2	I02_O03_S	**Controls the path from I02 to O03** 0: Off 1: On
1	I01_O03_S	**Controls the path from I01 to O03** 0: Off 1: On
0	I00_O03_S	**Controls the path from I00 to O03** 0: Off 1: On

11220030 AFE_CONN4 AFE Connection Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		BYPASS_ASRC		I28_O04_S	I27_O04_S	I26_O04_S	I25_O04_S	I24_O04_S	I23_O04_S	I22_O04_S	I21_O04_S	I20_O04_S	I19_O04_S	I18_O04_S	I17_O04_S	I16_O04_S
Type		RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset		0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O04_S	I14_O04_S	I13_O04_S	I12_O04_S	I11_O04_S	I10_O04_S	I09_O04_S	I08_O04_S	I07_O04_S	I06_O04_S	I05_O04_S	I04_O04_S	I03_O04_S	I02_O04_S	I01_O04_S	I00_O04_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	BYPASS_ASRC	**I2S in I_0, I_1 bypass ASRC** 0: Off 1: On
28	I28_O04_S	**Controls the path from I28 to O04** 0: Off 1: On

Bit(s)	Name	Description
27	I27_O04_S	**Controls the path from I27 to O04** 0: Off 1: On
26	I26_O04_S	**Controls the path from I26 to O04** 0: Off 1: On
25	I25_O04_S	**Controls the path from I25 to O04** 0: Off 1: On
24	I24_O04_S	**Controls the path from I24 to O04** 0: Off 1: On
23	I23_O04_S	**Controls the path from I23 to O04** 0: Off 1: On
22	I22_O04_S	**Controls the path from I22 to O04** 0: Off 1: On
21	I21_O04_S	**Controls the path from I21 to O04** 0: Off 1: On
20	I20_O04_S	**Controls the path from I20 to O04** 0: Off 1: On
19	I19_O04_S	**Controls the path from I19 to O04** 0: Off 1: On
18	I18_O04_S	**Controls the path from I18 to O04** 0: Off 1: On
17	I17_O04_S	**Controls the path from I17 to O04** 0: Off 1: On
16	I16_O04_S	**Controls the path from I16 to O04** 0: Off 1: On
15	I15_O04_S	**Controls the path from I15 to O04** 0: Off 1: On
14	I14_O04_S	**Controls the path from I14 to O04** 0: Off 1: On
13	I13_O04_S	**Controls the path from I13 to O04** 0: Off 1: On
12	I12_O04_S	**Controls the path from I12 to O04** 0: Off 1: On
11	I11_O04_S	**Controls the path from I11 to O04** 0: Off 1: On
10	I10_O04_S	**Controls the path from I10 to O04** 0: Off 1: On
9	I09_O04_S	**Controls the path from I09 to O04** 0: Off 1: On

Bit(s)	Name	Description
8	I08_O04_S	**Controls the path from I08 to O04** 0: Off 1: On
7	I07_O04_S	**Controls the path from I07 to O04** 0: Off 1: On
6	I06_O04_S	**Controls the path from I06 to O04** 0: Off 1: On
5	I05_O04_S	**Controls the path from I05 to O04** 0: Off 1: On
4	I04_O04_S	**Controls the path from I04 to O04** 0: Off 1: On
3	I03_O04_S	**Controls the path from I03 to O04** 0: Off 1: On
2	I02_O04_S	**Controls the path from I02 to O04** 0: Off 1: On
1	I01_O04_S	**Controls the path from I01 to O04** 0: Off 1: On
0	I00_O04_S	**Controls the path from I00 to O04** 0: Off 1: On

1122005C AFE_CONN5 AFE Connection Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I31_O05_S	I30_O05_S	I29_O05_S	I28_O05_S	I27_O05_S	I26_O05_S	I25_O05_S	I24_O05_S	I23_O05_S	I22_O05_S	I21_O05_S	I20_O05_S	I19_O05_S	I18_O05_S	I17_O05_S	I16_O05_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O05_S	I14_O05_S	I13_O05_S	I12_O05_S	I11_O05_S	I10_O05_S	I09_O05_S	I08_O05_S	I07_O05_S	I06_O05_S	I05_O05_S	I04_O05_S	I03_O05_S	I02_O05_S	I01_O05_S	I00_O05_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	I31_O05_S	**Controls the path from I31 to O05** 0: Off 1: On
30	I30_O05_S	**Controls the path from I30 to O05** 0: Off 1: On
29	I29_O05_S	**Controls the path from I29 to O05** 0: Off 1: On
28	I28_O05_S	**Controls the path from I28 to O05** 0: Off 1: On

Bit(s)	Name	Description
27	I27_O05_S	**Controls the path from I27 to O05** 0: Off 1: On
26	I26_O05_S	**Controls the path from I26 to O05** 0: Off 1: On
25	I25_O05_S	**Controls the path from I25 to O05** 0: Off 1: On
24	I24_O05_S	**Controls the path from I24 to O05** 0: Off 1: On
23	I23_O05_S	**Controls the path from I23 to O05** 0: Off 1: On
22	I22_O05_S	**Controls the path from I22 to O05** 0: Off 1: On
21	I21_O05_S	**Controls the path from I21 to O05** 0: Off 1: On
20	I20_O05_S	**Controls the path from I20 to O05** 0: Off 1: On
19	I19_O05_S	**Controls the path from I19 to O05** 0: Off 1: On
18	I18_O05_S	**Controls the path from I18 to O05** 0: Off 1: On
17	I17_O05_S	**Controls the path from I17 to O05** 0: Off 1: On
16	I16_O05_S	**Controls the path from I16 to O05** 0: Off 1: On
15	I15_O05_S	**Controls the path from I15 to O05** 0: Off 1: On
14	I14_O05_S	**Controls the path from I14 to O05** 0: Off 1: On
13	I13_O05_S	**Controls the path from I13 to O05** 0: Off 1: On
12	I12_O05_S	**Controls the path from I12 to O05** 0: Off 1: On
11	I11_O05_S	**Controls the path from I11 to O05** 0: Off 1: On
10	I10_O05_S	**Controls the path from I10 to O05** 0: Off 1: On
9	I09_O05_S	**Controls the path from I09 to O05** 0: Off 1: On

Bit(s)	Name	Description
8	I08_O05_S	**Controls the path from I08 to O05** 0: Off 1: On
7	I07_O05_S	**Controls the path from I07 to O05** 0: Off 1: On
6	I06_O05_S	**Controls the path from I06 to O05** 0: Off 1: On
5	I05_O05_S	**Controls the path from I05 to O05** 0: Off 1: On
4	I04_O05_S	**Controls the path from I04 to O05** 0: Off 1: On
3	I03_O05_S	**Controls the path from I03 to O05** 0: Off 1: On
2	I02_O05_S	**Controls the path from I02 to O05** 0: Off 1: On
1	I01_O05_S	**Controls the path from I01 to O05** 0: Off 1: On
0	I00_O05_S	**Controls the path from I00 to O05** 0: Off 1: On

112200BC AFE_CONN6 AFE Connection Register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I31_O06_S	I30_O06_S	I29_O06_S	I28_O06_S	I27_O06_S	I26_O06_S	I25_O06_S	I24_O06_S	I23_O06_S	I22_O06_S	I21_O06_S	I20_O06_S	I19_O06_S	I18_O06_S	I17_O06_S	I16_O06_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O06_S	I14_O06_S	I13_O06_S	I12_O06_S	I11_O06_S	I10_O06_S	I09_O06_S	I08_O06_S	I07_O06_S	I06_O06_S	I05_O06_S	I04_O06_S	I03_O06_S	I02_O06_S	I01_O06_S	I00_O06_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	I31_O06_S	**Controls the path from I31 to O06** 0: No shift 1: Right shift 1 bit
30	I30_O06_S	**Controls the path from I30 to O06** 0: No shift 1: Right shift 1 bit
29	I29_O06_S	**Controls the path from I29 to O06** 0: Off 1: On
28	I28_O06_S	**Controls the path from I28 to O06** 0: Off 1: On

Bit(s)	Name	Description
27	I27_O06_S	**Controls the path from I27 to O06** 0: Off 1: On
26	I26_O06_S	**Controls the path from I26 to O06** 0: Off 1: On
25	I25_O06_S	**Controls the path from I25 to O06** 0: Off 1: On
24	I24_O06_S	**Controls the path from I24 to O06** 0: Off 1: On
23	I23_O06_S	**Controls the path from I23 to O06** 0: Off 1: On
22	I22_O06_S	**Controls the path from I22 to O06** 0: Off 1: On
21	I21_O06_S	**Controls the path from I21 to O06** 0: Off 1: On
20	I20_O06_S	**Controls the path from I20 to O06** 0: Off 1: On
19	I19_O06_S	**Controls the path from I19 to O06** 0: Off 1: On
18	I18_O06_S	**Controls the path from I18 to O06** 0: Off 1: On
17	I17_O06_S	**Controls the path from I17 to O06** 0: Off 1: On
16	I16_O06_S	**Controls the path from I16 to O06** 0: Off 1: On
15	I15_O06_S	**Controls the path from I15 to O06** 0: Off 1: On
14	I14_O06_S	**Controls the path from I14 to O06** 0: Off 1: On
13	I13_O06_S	**Controls the path from I13 to O06** 0: Off 1: On
12	I12_O06_S	**Controls the path from I12 to O06** 0: Off 1: On
11	I11_O06_S	**Controls the path from I11 to O06** 0: Off 1: On
10	I10_O06_S	**Controls the path from I10 to O06** 0: Off 1: On
9	I09_O06_S	**Controls the path from I09 to O06** 0: Off 1: On

Bit(s)	Name	Description
8	I08_O06_S	**Controls the path from I08 to O06** 0: Off 1: On
7	I07_O06_S	**Controls the path from I07 to O06** 0: Off 1: On
6	I06_O06_S	**Controls the path from I06 to O06** 0: Off 1: On
5	I05_O06_S	**Controls the path from I05 to O06** 0: Off 1: On
4	I04_O06_S	**Controls the path from I04 to O06** 0: Off 1: On
3	I03_O06_S	**Controls the path from I03 to O06** 0: Off 1: On
2	I02_O06_S	**Controls the path from I02 to O06** 0: Off 1: On
1	I01_O06_S	**Controls the path from I01 to O06** 0: Off 1: On
0	I00_O06_S	**Controls the path from I00 to O06** 0: Off 1: On

11220420 AFE_CONN7 AFE Connection Register 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I31_O07_S	I30_O07_S	I29_O07_S	I28_O07_S	I27_O07_S	I26_O07_S	I25_O07_S	I24_O07_S	I23_O07_S	I22_O07_S	I21_O07_S	I20_O07_S	I19_O07_S	I18_O07_S	I17_O07_S	I16_O07_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O07_S	I14_O07_S	I13_O07_S	I12_O07_S	I11_O07_S	I10_O07_S	I09_O07_S	I08_O07_S	I07_O07_S	I06_O07_S	I05_O07_S	I04_O07_S	I03_O07_S	I02_O07_S	I01_O07_S	I00_O07_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	I31_O07_S	**Controls the path from I31 to O07** 0: Off 1: On
30	I30_O07_S	**Controls the path from I30 to O07** 0: Off 1: On
29	I29_O07_S	**Controls the path from I29 to O07** 0: Off 1: On
28	I28_O07_S	**Controls the path from I28 to O07** 0: Off 1: On

Bit(s)	Name	Description
27	I27_O07_S	**Controls the path from I27 to O07** 0: Off 1: On
26	I26_O07_S	**Controls the path from I26 to O07** 0: Off 1: On
25	I25_O07_S	**Controls the path from I25 to O07** 0: Off 1: On
24	I24_O07_S	**Controls the path from I24 to O07** 0: Off 1: On
23	I23_O07_S	**Controls the path from I23 to O07** 0: Off 1: On
22	I22_O07_S	**Controls the path from I22 to O07** 0: Off 1: On
21	I21_O07_S	**Controls the path from I21 to O07** 0: Off 1: On
20	I20_O07_S	**Controls the path from I20 to O07** 0: Off 1: On
19	I19_O07_S	**Controls the path from I19 to O07** 0: Off 1: On
18	I18_O07_S	**Controls the path from I18 to O07** 0: Off 1: On
17	I17_O07_S	**Controls the path from I17 to O07** 0: Off 1: On
16	I16_O07_S	**Controls the path from I16 to O07** 0: Off 1: On
15	I15_O07_S	**Controls the path from I15 to O07** 0: Off 1: On
14	I14_O07_S	**Controls the path from I14 to O07** 0: Off 1: On
13	I13_O07_S	**Controls the path from I13 to O07** 0: Off 1: On
12	I12_O07_S	**Controls the path from I12 to O07** 0: Off 1: On
11	I11_O07_S	**Controls the path from I11 to O07** 0: Off 1: On
10	I10_O07_S	**Controls the path from I10 to O07** 0: Off 1: On
9	I09_O07_S	**Controls the path from I09 to O07** 0: Off 1: On

Bit(s)	Name	Description
8	I08_O07_S	**Controls the path from I08 to O07** 0: Off 1: On
7	I07_O07_S	**Controls the path from I07 to O07** 0: Off 1: On
6	I06_O07_S	**Controls the path from I06 to O07** 0: Off 1: On
5	I05_O07_S	**Controls the path from I05 to O07** 0: Off 1: On
4	I04_O07_S	**Controls the path from I04 to O07** 0: Off 1: On
3	I03_O07_S	**Controls the path from I03 to O07** 0: Off 1: On
2	I02_O07_S	**Controls the path from I02 to O07** 0: Off 1: On
1	I01_O07_S	**Controls the path from I01 to O07** 0: Off 1: On
0	I00_O07_S	**Controls the path from I00 to O07** 0: Off 1: On

11220438 AFE_CONN8 AFE Connection Register 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I31_O08_S	I30_O08_S	I29_O08_S	I28_O08_S	I27_O08_S	I26_O08_S	I25_O08_S	I24_O08_S	I23_O08_S	I22_O08_S	I21_O08_S	I20_O08_S	I19_O08_S	I18_O08_S	I17_O08_S	I16_O08_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O08_S	I14_O08_S	I13_O08_S	I12_O08_S	I11_O08_S	I10_O08_S	I09_O08_S	I08_O08_S	I07_O08_S	I06_O08_S	I05_O08_S	I04_O08_S	I03_O08_S	I02_O08_S	I01_O08_S	I00_O08_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	I31_O08_S	**Controls the path from I31 to O08** 0: No shift 1: Right shift 1 bit
30	I30_O08_S	**Controls the path from I30 to O08** 0: Off 1: On
29	I29_O08_S	**Controls the path from I29 to O08** 0: Off 1: On
28	I28_O08_S	**Controls the path from I28 to O08** 0: Off 1: On

Bit(s)	Name	Description
27	I27_O08_S	**Controls the path from I27 to O08** 0: Off 1: On
26	I26_O08_S	**Controls the path from I26 to O08** 0: Off 1: On
25	I25_O08_S	**Controls the path from I25 to O08** 0: Off 1: On
24	I24_O08_S	**Controls the path from I24 to O08** 0: Off 1: On
23	I23_O08_S	**Controls the path from I23 to O08** 0: Off 1: On
22	I22_O08_S	**Controls the path from I22 to O08** 0: Off 1: On
21	I21_O08_S	**Controls the path from I21 to O08** 0: Off 1: On
20	I20_O08_S	**Controls the path from I20 to O08** 0: Off 1: On
19	I19_O08_S	**Controls the path from I19 to O08** 0: Off 1: On
18	I18_O08_S	**Controls the path from I18 to O08** 0: Off 1: On
17	I17_O08_S	**Controls the path from I17 to O08** 0: Off 1: On
16	I16_O08_S	**Controls the path from I16 to O08** 0: Off 1: On
15	I15_O08_S	**Controls the path from I15 to O08** 0: Off 1: On
14	I14_O08_S	**Controls the path from I14 to O08** 0: Off 1: On
13	I13_O08_S	**Controls the path from I13 to O08** 0: Off 1: On
12	I12_O08_S	**Controls the path from I12 to O08** 0: Off 1: On
11	I11_O08_S	**Controls the path from I11 to O08** 0: Off 1: On
10	I10_O08_S	**Controls the path from I10 to O08** 0: Off 1: On
9	I09_O08_S	**Controls the path from I09 to O08** 0: Off 1: On

Bit(s)	Name	Description
8	I08_O08_S	**Controls the path from I08 to O08** 0: Off 1: On
7	I07_O08_S	**Controls the path from I07 to O08** 0: Off 1: On
6	I06_O08_S	**Controls the path from I06 to O08** 0: Off 1: On
5	I05_O08_S	**Controls the path from I05 to O08** 0: Off 1: On
4	I04_O08_S	**Controls the path from I04 to O08** 0: Off 1: On
3	I03_O08_S	**Controls the path from I03 to O08** 0: Off 1: On
2	I02_O08_S	**Controls the path from I02 to O08** 0: Off 1: On
1	I01_O08_S	**Controls the path from I01 to O08** 0: Off 1: On
0	I00_O08_S	**Controls the path from I00 to O08** 0: Off 1: On

11220440 AFE_CONN9 AFE Connection Register 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			I29_O09_S	I28_O09_S	I27_O09_S	I26_O09_S	I25_O09_S	I24_O09_S	I23_O09_S	I22_O09_S	I21_O09_S	I20_O09_S	I19_O09_S	I18_O09_S	I17_O09_S	I16_O09_S
Type			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O09_S	I14_O09_S	I13_O09_S	I12_O09_S	I11_O09_S	I10_O09_S	I09_O09_S	I08_O09_S	I07_O09_S	I06_O09_S	I05_O09_S	I04_O09_S	I03_O09_S	I02_O09_S	I01_O09_S	I00_O09_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29	I29_O09_S	**Controls the path from I29 to O09** 0: Off 1: On
28	I28_O09_S	**Controls the path from I28 to O09** 0: Off 1: On
27	I27_O09_S	**Controls the path from I27 to O09** 0: Off 1: On
26	I26_O09_S	**Controls the path from I26 to O09** 0: Off

Bit(s)	Name	Description
		1: On
25	I25_O09_S	**Controls the path from I25 to O09** 0: Off 1: On
24	I24_O09_S	**Controls the path from I24 to O09** 0: Off 1: On
23	I23_O09_S	**Controls the path from I23 to O09** 0: Off 1: On
22	I22_O09_S	**Controls the path from I22 to O09** 0: Off 1: On
21	I21_O09_S	**Controls the path from I21 to O09** 0: Off 1: On
20	I20_O09_S	**Controls the path from I20 to O09** 0: Off 1: On
19	I19_O09_S	**Controls the path from I19 to O09** 0: Off 1: On
18	I18_O09_S	**Controls the path from I18 to O09** 0: Off 1: On
17	I17_O09_S	**Controls the path from I17 to O09** 0: Off 1: On
16	I16_O09_S	**Controls the path from I16 to O09** 0: Off 1: On
15	I15_O09_S	**Controls the path from I15 to O09** 0: Off 1: On
14	I14_O09_S	**Controls the path from I14 to O09** 0: Off 1: On
13	I13_O09_S	**Controls the path from I13 to O09** 0: Off 1: On
12	I12_O09_S	**Controls the path from I12 to O09** 0: Off 1: On
11	I11_O09_S	**Controls the path from I11 to O09** 0: Off 1: On
10	I10_O09_S	**Controls the path from I10 to O09** 0: Off 1: On
9	I09_O09_S	**Controls the path from I09 to O09** 0: Off 1: On
8	I08_O09_S	**Controls the path from I08 to O09** 0: Off 1: On
7	I07_O09_S	**Controls the path from I07 to O09** 0: Off

Bit(s)	Name	Description
		1: On
6	I06_O09_S	**Controls the path from I06 to O09** 0: Off 1: On
5	I05_O09_S	**Controls the path from I05 to O09** 0: Off 1: On
4	I04_O09_S	**Controls the path from I04 to O09** 0: Off 1: On
3	I03_O09_S	**Controls the path from I03 to O09** 0: Off 1: On
2	I02_O09_S	**Controls the path from I02 to O09** 0: Off 1: On
1	I01_O09_S	**Controls the path from I01 to O09** 0: Off 1: On
0	I00_O09_S	**Controls the path from I00 to O09** 0: Off 1: On

11220444 AFE_CONN10 AFE Connection Register 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				I28_O10_S	I27_O10_S	I26_O10_S	I25_O10_S	I24_O10_S	I23_O10_S	I22_O10_S	I21_O10_S	I20_O10_S	I19_O10_S	I18_O10_S	I17_O10_S	I16_O10_S
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O10_S	I14_O10_S	I13_O10_S	I12_O10_S	I11_O10_S	I10_O10_S	I09_O10_S	I08_O10_S	I07_O10_S	I06_O10_S	I05_O10_S	I04_O10_S	I03_O10_S	I02_O10_S	I01_O10_S	I00_O10_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	I28_O10_S	**Controls the path from I28 to O10** 0: Off 1: On
27	I27_O10_S	**Controls the path from I27 to O10** 0: Off 1: On
26	I26_O10_S	**Controls the path from I26 to O10** 0: Off 1: On
25	I25_O10_S	**Controls the path from I25 to O10** 0: Off 1: On
24	I24_O10_S	**Controls the path from I24 to O10** 0: Off 1: On
23	I23_O10_S	**Controls the path from I23 to O10**

Bit(s)	Name	Description
		0: Off 1: On
22	I22_O10_S	**Controls the path from I22 to O10** 0: Off 1: On
21	I21_O10_S	**Controls the path from I21 to O10** 0: Off 1: On
20	I20_O10_S	**Controls the path from I20 to O10** 0: Off 1: On
19	I19_O10_S	**Controls the path from I19 to O10** 0: Off 1: On
18	I18_O10_S	**Controls the path from I18 to O10** 0: Off 1: On
17	I17_O10_S	**Controls the path from I17 to O10** 0: Off 1: On
16	I16_O10_S	**Controls the path from I16 to O10** 0: Off 1: On
15	I15_O10_S	**Controls the path from I15 to O10** 0: Off 1: On
14	I14_O10_S	**Controls the path from I14 to O10** 0: Off 1: On
13	I13_O10_S	**Controls the path from I13 to O10** 0: Off 1: On
12	I12_O10_S	**Controls the path from I12 to O10** 0: Off 1: On
11	I11_O10_S	**Controls the path from I11 to O10** 0: Off 1: On
10	I10_O10_S	**Controls the path from I10 to O10** 0: Off 1: On
9	I09_O10_S	**Controls the path from I09 to O10** 0: Off 1: On
8	I08_O10_S	**Controls the path from I08 to O10** 0: Off 1: On
7	I07_O10_S	**Controls the path from I07 to O10** 0: Off 1: On
6	I06_O10_S	**Controls the path from I06 to O10** 0: Off 1: On
5	I05_O10_S	**Controls the path from I05 to O10** 0: Off 1: On
4	I04_O10_S	**Controls the path from I04 to O10**

Bit(s)	Name	Description
		0: Off 1: On
3	I03_O10_S	**Controls the path from I03 to O10** 0: Off 1: On
2	I02_O10_S	**Controls the path from I02 to O10** 0: Off 1: On
1	I01_O10_S	**Controls the path from I01 to O10** 0: Off 1: On
0	I00_O10_S	**Controls the path from I00 to O10** 0: Off 1: On

11220448 AFE_CONN11 AFE Connection Register 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				I28_O11_S	I27_O11_S	I26_O11_S	I25_O11_S	I24_O11_S	I23_O11_S	I22_O11_S	I21_O11_S	I20_O11_S	I19_O11_S	I18_O11_S	I17_O11_S	I16_O11_S
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O11_S	I14_O11_S	I13_O11_S	I12_O11_S	I11_O11_S	I10_O11_S	I09_O11_S	I08_O11_S	I07_O11_S	I06_O11_S	I05_O11_S	I04_O11_S	I03_O11_S	I02_O11_S	I01_O11_S	I00_O11_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	I28_O11_S	**Controls the path from I28 to O11** 0: Off 1: On
27	I27_O11_S	**Controls the path from I27 to O11** 0: Off 1: On
26	I26_O11_S	**Controls the path from I26 to O11** 0: Off 1: On
25	I25_O11_S	**Controls the path from I25 to O11** 0: Off 1: On
24	I24_O11_S	**Controls the path from I24 to O11** 0: Off 1: On
23	I23_O11_S	**Controls the path from I23 to O11** 0: Off 1: On
22	I22_O11_S	**Controls the path from I22 to O11** 0: Off 1: On
21	I21_O11_S	**Controls the path from I21 to O11** 0: Off 1: On

Bit(s)	Name	Description
20	I20_O11_S	**Controls the path from I20 to O11** 0: Off 1: On
19	I19_O11_S	**Controls the path from I19 to O11** 0: Off 1: On
18	I18_O11_S	**Controls the path from I18 to O11** 0: Off 1: On
17	I17_O11_S	**Controls the path from I17 to O11** 0: Off 1: On
16	I16_O11_S	**Controls the path from I16 to O11** 0: Off 1: On
15	I15_O11_S	**Controls the path from I15 to O11** 0: Off 1: On
14	I14_O11_S	**Controls the path from I14 to O11** 0: Off 1: On
13	I13_O11_S	**Controls the path from I13 to O11** 0: Off 1: On
12	I12_O11_S	**Controls the path from I12 to O11** 0: Off 1: On
11	I11_O11_S	**Controls the path from I11 to O11** 0: Off 1: On
10	I10_O11_S	**Controls the path from I10 to O11** 0: Off 1: On
9	I09_O11_S	**Controls the path from I09 to O11** 0: Off 1: On
8	I08_O11_S	**Controls the path from I08 to O11** 0: Off 1: On
7	I07_O11_S	**Controls the path from I07 to O11** 0: Off 1: On
6	I06_O11_S	**Controls the path from I06 to O11** 0: Off 1: On
5	I05_O11_S	**Controls the path from I05 to O11** 0: Off 1: On
4	I04_O11_S	**Controls the path from I04 to O11** 0: Off 1: On
3	I03_O11_S	**Controls the path from I03 to O11** 0: Off 1: On
2	I02_O11_S	**Controls the path from I02 to O11** 0: Off 1: On

Bit(s)	Name	Description
1	I01_O11_S	**Controls the path from I01 to O11** 0: Off 1: On
0	I00_O11_S	**Controls the path from I00 to O11** 0: Off 1: On

1122044C AFE_CONN12 AFE Connection Register 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				I28_O12_S	I27_O12_S	I26_O12_S	I25_O12_S	I24_O12_S	I23_O12_S	I22_O12_S	I21_O12_S	I20_O12_S	I19_O12_S	I18_O12_S	I17_O12_S	I16_O12_S
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O12_S	I14_O12_S	I13_O12_S	I12_O12_S	I11_O12_S	I10_O12_S	I09_O12_S	I08_O12_S	I07_O12_S	I06_O12_S	I05_O12_S	I04_O12_S	I03_O12_S	I02_O12_S	I01_O12_S	I00_O12_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	I28_O12_S	**Controls the path from I28 to O12** 0: Off 1: On
27	I27_O12_S	**Controls the path from I27 to O12** 0: Off 1: On
26	I26_O12_S	**Controls the path from I26 to O12** 0: Off 1: On
25	I25_O12_S	**Controls the path from I25 to O12** 0: Off 1: On
24	I24_O12_S	**Controls the path from I24 to O12** 0: Off 1: On
23	I23_O12_S	**Controls the path from I23 to O12** 0: Off 1: On
22	I22_O12_S	**Controls the path from I22 to O12** 0: Off 1: On
21	I21_O12_S	**Controls the path from I21 to O12** 0: Off 1: On
20	I20_O12_S	**Controls the path from I20 to O12** 0: Off 1: On
19	I19_O12_S	**Controls the path from I19 to O12** 0: Off 1: On
18	I18_O12_S	**Controls the path from I18 to O12** 0: Off

Bit(s)	Name	Description
		1: On
17	I17_O12_S	**Controls the path from I17 to O12** 0: Off 1: On
16	I16_O12_S	**Controls the path from I16 to O12** 0: Off 1: On
15	I15_O12_S	**Controls the path from I15 to O12** 0: Off 1: On
14	I14_O12_S	**Controls the path from I14 to O12** 0: Off 1: On
13	I13_O12_S	**Controls the path from I13 to O12** 0: Off 1: On
12	I12_O12_S	**Controls the path from I12 to O12** 0: Off 1: On
11	I11_O12_S	**Controls the path from I11 to O12** 0: Off 1: On
10	I10_O12_S	**Controls the path from I10 to O12** 0: Off 1: On
9	I09_O12_S	**Controls the path from I09 to O12** 0: Off 1: On
8	I08_O12_S	**Controls the path from I08 to O12** 0: Off 1: On
7	I07_O12_S	**Controls the path from I07 to O12** 0: Off 1: On
6	I06_O12_S	**Controls the path from I06 to O12** 0: Off 1: On
5	I05_O12_S	**Controls the path from I05 to O12** 0: Off 1: On
4	I04_O12_S	**Controls the path from I04 to O12** 0: Off 1: On
3	I03_O12_S	**Controls the path from I03 to O12** 0: Off 1: On
2	I02_O12_S	**Controls the path from I02 to O12** 0: Off 1: On
1	I01_O12_S	**Controls the path from I01 to O12** 0: Off 1: On
0	I00_O12_S	**Controls the path from I00 to O12** 0: Off 1: On

11220450 AFE_CONN13 AFE Connection Register 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				I28_O13_S	I27_O13_S	I26_O13_S	I25_O13_S	I24_O13_S	I23_O13_S	I22_O13_S	I21_O13_S	I20_O13_S	I19_O13_S	I18_O13_S	I17_O13_S	I16_O13_S
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O13_S	I14_O13_S	I13_O13_S	I12_O13_S	I11_O13_S	I10_O13_S	I09_O13_S	I08_O13_S	I07_O13_S	I06_O13_S	I05_O13_S	I04_O13_S	I03_O13_S	I02_O13_S	I01_O13_S	I00_O13_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	I28_O13_S	**Controls the path from I28 to O13** 0: Off 1: On
27	I27_O13_S	**Controls the path from I27 to O13** 0: Off 1: On
26	I26_O13_S	**Controls the path from I26 to O13** 0: Off 1: On
25	I25_O13_S	**Controls the path from I25 to O13** 0: Off 1: On
24	I24_O13_S	**Controls the path from I24 to O13** 0: Off 1: On
23	I23_O13_S	**Controls the path from I23 to O13** 0: Off 1: On
22	I22_O13_S	**Controls the path from I22 to O13** 0: Off 1: On
21	I21_O13_S	**Controls the path from I21 to O13** 0: Off 1: On
20	I20_O13_S	**Controls the path from I20 to O13** 0: Off 1: On
19	I19_O13_S	**Controls the path from I19 to O13** 0: Off 1: On
18	I18_O13_S	**Controls the path from I18 to O13** 0: Off 1: On
17	I17_O13_S	**Controls the path from I17 to O13** 0: Off 1: On
16	I16_O13_S	**Controls the path from I16 to O13** 0: Off 1: On
15	I15_O13_S	**Controls the path from I15 to O13** 0: Off

Bit(s)	Name	Description
		1: On
14	I14_O13_S	**Controls the path from I14 to O13** 0: Off 1: On
13	I13_O13_S	**Controls the path from I13 to O13** 0: Off 1: On
12	I12_O13_S	**Controls the path from I12 to O13** 0: Off 1: On
11	I11_O13_S	**Controls the path from I11 to O13** 0: Off 1: On
10	I10_O13_S	**Controls the path from I10 to O13** 0: Off 1: On
9	I09_O13_S	**Controls the path from I09 to O13** 0: Off 1: On
8	I08_O13_S	**Controls the path from I08 to O13** 0: Off 1: On
7	I07_O13_S	**Controls the path from I07 to O13** 0: Off 1: On
6	I06_O13_S	**Controls the path from I06 to O13** 0: Off 1: On
5	I05_O13_S	**Controls the path from I05 to O13** 0: Off 1: On
4	I04_O13_S	**Controls the path from I04 to O13** 0: Off 1: On
3	I03_O13_S	**Controls the path from I03 to O13** 0: Off 1: On
2	I02_O13_S	**Controls the path from I02 to O13** 0: Off 1: On
1	I01_O13_S	**Controls the path from I01 to O13** 0: Off 1: On
0	I00_O13_S	**Controls the path from I00 to O13** 0: Off 1: On

11220454 AFE_CONN14 AFE Connection Register 14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				I28_O14_S	I27_O14_S	I26_O14_S	I25_O14_S	I24_O14_S	I23_O14_S	I22_O14_S	I21_O14_S	I20_O14_S	I19_O14_S	I18_O14_S	I17_O14_S	I16_O14_S
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O14_S	I14_O14_S	I13_O14_S	I12_O14_S	I11_O14_S	I10_O14_S	I09_O14_S	I08_O14_S	I07_O14_S	I06_O14_S	I05_O14_S	I04_O14_S	I03_O14_S	I02_O14_S	I01_O14_S	I00_O14_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	I28_O14_S	**Controls the path from I28 to O14** 0: Off 1: On
27	I27_O14_S	**Controls the path from I27 to O14** 0: Off 1: On
26	I26_O14_S	**Controls the path from I26 to O14** 0: Off 1: On
25	I25_O14_S	**Controls the path from I25 to O14** 0: Off 1: On
24	I24_O14_S	**Controls the path from I24 to O14** 0: Off 1: On
23	I23_O14_S	**Controls the path from I23 to O14** 0: Off 1: On
22	I22_O14_S	**Controls the path from I22 to O14** 0: Off 1: On
21	I21_O14_S	**Controls the path from I21 to O14** 0: Off 1: On
20	I20_O14_S	**Controls the path from I20 to O14** 0: Off 1: On
19	I19_O14_S	**Controls the path from I19 to O14** 0: Off 1: On
18	I18_O14_S	**Controls the path from I18 to O14** 0: Off 1: On
17	I17_O14_S	**Controls the path from I17 to O14** 0: Off 1: On
16	I16_O14_S	**Controls the path from I16 to O14** 0: Off 1: On
15	I15_O14_S	**Controls the path from I15 to O14** 0: Off 1: On
14	I14_O14_S	**Controls the path from I14 to O14** 0: Off 1: On
13	I13_O14_S	**Controls the path from I13 to O14** 0: Off 1: On
12	I12_O14_S	**Controls the path from I12 to O14**

Bit(s)	Name	Description
		0: Off 1: On
11	I11_O14_S	**Controls the path from I11 to O14** 0: Off 1: On
10	I10_O14_S	**Controls the path from I10 to O14** 0: Off 1: On
9	I09_O14_S	**Controls the path from I09 to O14** 0: Off 1: On
8	I08_O14_S	**Controls the path from I08 to O14** 0: Off 1: On
7	I07_O14_S	**Controls the path from I07 to O14** 0: Off 1: On
6	I06_O14_S	**Controls the path from I06 to O14** 0: Off 1: On
5	I05_O14_S	**Controls the path from I05 to O14** 0: Off 1: On
4	I04_O14_S	**Controls the path from I04 to O14** 0: Off 1: On
3	I03_O14_S	**Controls the path from I03 to O14** 0: Off 1: On
2	I02_O14_S	**Controls the path from I02 to O14** 0: Off 1: On
1	I01_O14_S	**Controls the path from I01 to O14** 0: Off 1: On
0	I00_O14_S	**Controls the path from I00 to O14** 0: Off 1: On

11220458 AFE_CONN15 AFE Connection Register 15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				I28_O15_S	I27_O15_S	I26_O15_S	I25_O15_S	I24_O15_S	I23_O15_S	I22_O15_S	I21_O15_S	I20_O15_S	I19_O15_S	I18_O15_S	I17_O15_S	I16_O15_S
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O15_S	I14_O15_S	I13_O15_S	I12_O15_S	I11_O15_S	I10_O15_S	I09_O15_S	I08_O15_S	I07_O15_S	I06_O15_S	I05_O15_S	I04_O15_S	I03_O15_S	I02_O15_S	I01_O15_S	I00_O15_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
28	I28_O15_S	**Controls the path from I28 to O15** 0: Off 1: On
27	I27_O15_S	**Controls the path from I27 to O15** 0: Off 1: On
26	I26_O15_S	**Controls the path from I26 to O15** 0: Off 1: On
25	I25_O15_S	**Controls the path from I25 to O15** 0: Off 1: On
24	I24_O15_S	**Controls the path from I24 to O15** 0: Off 1: On
23	I23_O15_S	**Controls the path from I23 to O15** 0: Off 1: On
22	I22_O15_S	**Controls the path from I22 to O15** 0: Off 1: On
21	I21_O15_S	**Controls the path from I21 to O15** 0: Off 1: On
20	I20_O15_S	**Controls the path from I20 to O15** 0: Off 1: On
19	I19_O15_S	**Controls the path from I19 to O15** 0: Off 1: On
18	I18_O15_S	**Controls the path from I18 to O15** 0: Off 1: On
17	I17_O15_S	**Controls the path from I17 to O15** 0: Off 1: On
16	I16_O15_S	**Controls the path from I16 to O15** 0: Off 1: On
15	I15_O15_S	**Controls the path from I15 to O15** 0: Off 1: On
14	I14_O15_S	**Controls the path from I14 to O15** 0: Off 1: On
13	I13_O15_S	**Controls the path from I13 to O15** 0: Off 1: On
12	I12_O15_S	**Controls the path from I12 to O15** 0: Off 1: On
11	I11_O15_S	**Controls the path from I11 to O15** 0: Off 1: On
10	I10_O15_S	**Controls the path from I10 to O15** 0: Off 1: On

Bit(s)	Name	Description
9	I09_O15_S	**Controls the path from I09 to O15** 0: Off 1: On
8	I08_O15_S	**Controls the path from I08 to O15** 0: Off 1: On
7	I07_O15_S	**Controls the path from I07 to O15** 0: Off 1: On
6	I06_O15_S	**Controls the path from I06 to O15** 0: Off 1: On
5	I05_O15_S	**Controls the path from I05 to O15** 0: Off 1: On
4	I04_O15_S	**Controls the path from I04 to O15** 0: Off 1: On
3	I03_O15_S	**Controls the path from I03 to O15** 0: Off 1: On
2	I02_O15_S	**Controls the path from I02 to O15** 0: Off 1: On
1	I01_O15_S	**Controls the path from I01 to O15** 0: Off 1: On
0	I00_O15_S	**Controls the path from I00 to O15** 0: Off 1: On

1122045C AFE_CONN16 AFE Connection Register 16 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				I28_O16_S	I27_O16_S	I26_O16_S	I25_O16_S	I24_O16_S	I23_O16_S	I22_O16_S	I21_O16_S	I20_O16_S	I19_O16_S	I18_O16_S	I17_O16_S	I16_O16_S
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O16_S	I14_O16_S	I13_O16_S	I12_O16_S	I11_O16_S	I10_O16_S	I09_O16_S	I08_O16_S	I07_O16_S	I06_O16_S	I05_O16_S	I04_O16_S	I03_O16_S	I02_O16_S	I01_O16_S	I00_O16_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	I28_O16_S	**Controls the path from I28 to O16** 0: Off 1: On
27	I27_O16_S	**Controls the path from I27 to O16** 0: Off 1: On
26	I26_O16_S	**Controls the path from I26 to O16** 0: Off

Bit(s)	Name	Description
		1: On
25	I25_O16_S	**Controls the path from I25 to O16** 0: Off 1: On
24	I24_O16_S	**Controls the path from I24 to O16** 0: Off 1: On
23	I23_O16_S	**Controls the path from I23 to O16** 0: Off 1: On
22	I22_O16_S	**Controls the path from I22 to O16** 0: Off 1: On
21	I21_O16_S	**Controls the path from I21 to O16** 0: Off 1: On
20	I20_O16_S	**Controls the path from I20 to O16** 0: Off 1: On
19	I19_O16_S	**Controls the path from I19 to O16** 0: Off 1: On
18	I18_O16_S	**Controls the path from I18 to O16** 0: Off 1: On
17	I17_O16_S	**Controls the path from I17 to O16** 0: Off 1: On
16	I16_O16_S	**Controls the path from I16 to O16** 0: Off 1: On
15	I15_O16_S	**Controls the path from I15 to O16** 0: Off 1: On
14	I14_O16_S	**Controls the path from I14 to O16** 0: Off 1: On
13	I13_O16_S	**Controls the path from I13 to O16** 0: Off 1: On
12	I12_O16_S	**Controls the path from I12 to O16** 0: Off 1: On
11	I11_O16_S	**Controls the path from I11 to O16** 0: Off 1: On
10	I10_O16_S	**Controls the path from I10 to O16** 0: Off 1: On
9	I09_O16_S	**Controls the path from I09 to O16** 0: Off 1: On
8	I08_O16_S	**Controls the path from I08 to O16** 0: Off 1: On
7	I07_O16_S	**Controls the path from I07 to O16** 0: Off

Bit(s)	Name	Description
		1: On
6	I06_O16_S	**Controls the path from I06 to O16** 0: Off 1: On
5	I05_O16_S	**Controls the path from I05 to O16** 0: Off 1: On
4	I04_O16_S	**Controls the path from I04 to O16** 0: Off 1: On
3	I03_O16_S	**Controls the path from I03 to O16** 0: Off 1: On
2	I02_O16_S	**Controls the path from I02 to O16** 0: Off 1: On
1	I01_O16_S	**Controls the path from I01 to O16** 0: Off 1: On
0	I00_O16_S	**Controls the path from I00 to O16** 0: Off 1: On

11220460 AFE_CONN17 AFE Connection Register 17 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				I28_O17_S	I27_O17_S	I26_O17_S	I25_O17_S	I24_O17_S	I23_O17_S	I22_O17_S	I21_O17_S	I20_O17_S	I19_O17_S	I18_O17_S	I17_O17_S	I16_O17_S
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O17_S	I14_O17_S	I13_O17_S	I12_O17_S	I11_O17_S	I10_O17_S	I09_O17_S	I08_O17_S	I07_O17_S	I06_O17_S	I05_O17_S	I04_O17_S	I03_O17_S	I02_O17_S	I01_O17_S	I00_O17_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	I28_O17_S	**Controls the path from I28 to O17** 0: Off 1: On
27	I27_O17_S	**Controls the path from I27 to O17** 0: Off 1: On
26	I26_O17_S	**Controls the path from I26 to O17** 0: Off 1: On
25	I25_O17_S	**Controls the path from I25 to O17** 0: Off 1: On
24	I24_O17_S	**Controls the path from I24 to O17** 0: Off 1: On
23	I23_O17_S	**Controls the path from I23 to O17**

Bit(s)	Name	Description
		0: Off 1: On
22	I22_O17_S	**Controls the path from I22 to O17** 0: Off 1: On
21	I21_O17_S	**Controls the path from I21 to O17** 0: Off 1: On
20	I20_O17_S	**Controls the path from I20 to O17** 0: Off 1: On
19	I19_O17_S	**Controls the path from I19 to O17** 0: Off 1: On
18	I18_O17_S	**Controls the path from I18 to O17** 0: Off 1: On
17	I17_O17_S	**Controls the path from I17 to O17** 0: Off 1: On
16	I16_O17_S	**Controls the path from I16 to O17** 0: Off 1: On
15	I15_O17_S	**Controls the path from I15 to O17** 0: Off 1: On
14	I14_O17_S	**Controls the path from I14 to O17** 0: Off 1: On
13	I13_O17_S	**Controls the path from I13 to O17** 0: Off 1: On
12	I12_O17_S	**Controls the path from I12 to O17** 0: Off 1: On
11	I11_O17_S	**Controls the path from I11 to O17** 0: Off 1: On
10	I10_O17_S	**Controls the path from I10 to O17** 0: Off 1: On
9	I09_O17_S	**Controls the path from I09 to O17** 0: Off 1: On
8	I08_O17_S	**Controls the path from I08 to O17** 0: Off 1: On
7	I07_O17_S	**Controls the path from I07 to O17** 0: Off 1: On
6	I06_O17_S	**Controls the path from I06 to O17** 0: Off 1: On
5	I05_O17_S	**Controls the path from I05 to O17** 0: Off 1: On
4	I04_O17_S	**Controls the path from I04 to O17**

Bit(s)	Name	Description
		0: Off 1: On
3	I03_O17_S	**Controls the path from I03 to O17** 0: Off 1: On
2	I02_O17_S	**Controls the path from I02 to O17** 0: Off 1: On
1	I01_O17_S	**Controls the path from I01 to O17** 0: Off 1: On
0	I00_O17_S	**Controls the path from I00 to O17** 0: Off 1: On

11220464 AFE_CONN18 AFE Connection Register 18 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				I28_O18_S	I27_O18_S	I26_O18_S	I25_O18_S	I24_O18_S	I23_O18_S	I22_O18_S	I21_O18_S	I20_O18_S	I19_O18_S	I18_O18_S	I17_O18_S	I16_O18_S
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O18_S	I14_O18_S	I13_O18_S	I12_O18_S	I11_O18_S	I10_O18_S	I09_O18_S	I08_O18_S	I07_O18_S	I06_O18_S	I05_O18_S	I04_O18_S	I03_O18_S	I02_O18_S	I01_O18_S	I00_O18_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	I28_O18_S	**Controls the path from I28 to O18** 0: Off 1: On
27	I27_O18_S	**Controls the path from I27 to O18** 0: Off 1: On
26	I26_O18_S	**Controls the path from I26 to O18** 0: Off 1: On
25	I25_O18_S	**Controls the path from I25 to O18** 0: Off 1: On
24	I24_O18_S	**Controls the path from I24 to O18** 0: Off 1: On
23	I23_O18_S	**Controls the path from I23 to O18** 0: Off 1: On
22	I22_O18_S	**Controls the path from I22 to O18** 0: Off 1: On
21	I21_O18_S	**Controls the path from I21 to O18** 0: Off 1: On

Bit(s)	Name	Description
20	I20_O18_S	**Controls the path from I20 to O18** 0: Off 1: On
19	I19_O18_S	**Controls the path from I19 to O18** 0: Off 1: On
18	I18_O18_S	**Controls the path from I18 to O18** 0: Off 1: On
17	I17_O18_S	**Controls the path from I17 to O18** 0: Off 1: On
16	I16_O18_S	**Controls the path from I16 to O18** 0: Off 1: On
15	I15_O18_S	**Controls the path from I15 to O18** 0: Off 1: On
14	I14_O18_S	**Controls the path from I14 to O18** 0: Off 1: On
13	I13_O18_S	**Controls the path from I13 to O18** 0: Off 1: On
12	I12_O18_S	**Controls the path from I12 to O18** 0: Off 1: On
11	I11_O18_S	**Controls the path from I11 to O18** 0: Off 1: On
10	I10_O18_S	**Controls the path from I10 to O18** 0: Off 1: On
9	I09_O18_S	**Controls the path from I09 to O18** 0: Off 1: On
8	I08_O18_S	**Controls the path from I08 to O18** 0: Off 1: On
7	I07_O18_S	**Controls the path from I07 to O18** 0: Off 1: On
6	I06_O18_S	**Controls the path from I06 to O18** 0: Off 1: On
5	I05_O18_S	**Controls the path from I05 to O18** 0: Off 1: On
4	I04_O18_S	**Controls the path from I04 to O18** 0: Off 1: On
3	I03_O18_S	**Controls the path from I03 to O18** 0: Off 1: On
2	I02_O18_S	**Controls the path from I02 to O18** 0: Off 1: On

Bit(s)	Name	Description
1	I01_O18_S	**Controls the path from I01 to O18** 0: Off 1: On
0	I00_O18_S	**Controls the path from I00 to O18** 0: Off 1: On

11220468 AFE_CONN19 AFE Connection Register 19 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				I28_O19_S	I27_O19_S	I26_O19_S	I25_O19_S	I24_O19_S	I23_O19_S	I22_O19_S	I21_O19_S	I20_O19_S	I19_O19_S	I18_O19_S	I17_O19_S	I16_O19_S
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O19_S	I14_O19_S	I13_O19_S	I12_O19_S	I11_O19_S	I10_O19_S	I09_O19_S	I08_O19_S	I07_O19_S	I06_O19_S	I05_O19_S	I04_O19_S	I03_O19_S	I02_O19_S	I01_O19_S	I00_O19_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	I28_O19_S	**Controls the path from I28 to O19** 0: Off 1: On
27	I27_O19_S	**Controls the path from I27 to O19** 0: Off 1: On
26	I26_O19_S	**Controls the path from I26 to O19** 0: Off 1: On
25	I25_O19_S	**Controls the path from I25 to O19** 0: Off 1: On
24	I24_O19_S	**Controls the path from I24 to O19** 0: Off 1: On
23	I23_O19_S	**Controls the path from I23 to O19** 0: Off 1: On
22	I22_O19_S	**Controls the path from I22 to O19** 0: Off 1: On
21	I21_O19_S	**Controls the path from I21 to O19** 0: Off 1: On
20	I20_O19_S	**Controls the path from I20 to O19** 0: Off 1: On
19	I19_O19_S	**Controls the path from I19 to O19** 0: Off 1: On
18	I18_O19_S	**Controls the path from I18 to O19** 0: Off

Bit(s)	Name	Description
		1: On
17	I17_O19_S	**Controls the path from I17 to O19** 0: Off 1: On
16	I16_O19_S	**Controls the path from I16 to O19** 0: Off 1: On
15	I15_O19_S	**Controls the path from I15 to O19** 0: Off 1: On
14	I14_O19_S	**Controls the path from I14 to O19** 0: Off 1: On
13	I13_O19_S	**Controls the path from I13 to O19** 0: Off 1: On
12	I12_O19_S	**Controls the path from I12 to O19** 0: Off 1: On
11	I11_O19_S	**Controls the path from I11 to O19** 0: Off 1: On
10	I10_O19_S	**Controls the path from I10 to O19** 0: Off 1: On
9	I09_O19_S	**Controls the path from I09 to O19** 0: Off 1: On
8	I08_O19_S	**Controls the path from I08 to O19** 0: Off 1: On
7	I07_O19_S	**Controls the path from I07 to O19** 0: Off 1: On
6	I06_O19_S	**Controls the path from I06 to O19** 0: Off 1: On
5	I05_O19_S	**Controls the path from I05 to O19** 0: Off 1: On
4	I04_O19_S	**Controls the path from I04 to O19** 0: Off 1: On
3	I03_O19_S	**Controls the path from I03 to O19** 0: Off 1: On
2	I02_O19_S	**Controls the path from I02 to O19** 0: Off 1: On
1	I01_O19_S	**Controls the path from I01 to O19** 0: Off 1: On
0	I00_O19_S	**Controls the path from I00 to O19** 0: Off 1: On

1122046C AFE_CONN20 AFE Connection Register 20 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				I28_O20_S	I27_O20_S	I26_O20_S	I25_O20_S	I24_O20_S	I23_O20_S	I22_O20_S	I21_O20_S	I20_O20_S	I19_O20_S	I18_O20_S	I17_O20_S	I16_O20_S
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O20_S	I14_O20_S	I13_O20_S	I12_O20_S	I11_O20_S	I10_O20_S	I09_O20_S	I08_O20_S	I07_O20_S	I06_O20_S	I05_O20_S	I04_O20_S	I03_O20_S	I02_O20_S	I01_O20_S	I00_O20_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	I28_O20_S	**Controls the path from I28 to O20** 0: Off 1: On
27	I27_O20_S	**Controls the path from I27 to O20** 0: Off 1: On
26	I26_O20_S	**Controls the path from I26 to O20** 0: Off 1: On
25	I25_O20_S	**Controls the path from I25 to O20** 0: Off 1: On
24	I24_O20_S	**Controls the path from I24 to O20** 0: Off 1: On
23	I23_O20_S	**Controls the path from I23 to O20** 0: Off 1: On
22	I22_O20_S	**Controls the path from I22 to O20** 0: Off 1: On
21	I21_O20_S	**Controls the path from I21 to O20** 0: Off 1: On
20	I20_O20_S	**Controls the path from I20 to O20** 0: Off 1: On
19	I19_O20_S	**Controls the path from I19 to O20** 0: Off 1: On
18	I18_O20_S	**Controls the path from I18 to O20** 0: Off 1: On
17	I17_O20_S	**Controls the path from I17 to O20** 0: Off 1: On
16	I16_O20_S	**Controls the path from I16 to O20** 0: Off 1: On
15	I15_O20_S	**Controls the path from I15 to O20** 0: Off

Bit(s)	Name	Description
		1: On
14	I14_O20_S	**Controls the path from I14 to O20** 0: Off 1: On
13	I13_O20_S	**Controls the path from I13 to O20** 0: Off 1: On
12	I12_O20_S	**Controls the path from I12 to O20** 0: Off 1: On
11	I11_O20_S	**Controls the path from I11 to O20** 0: Off 1: On
10	I10_O20_S	**Controls the path from I10 to O20** 0: Off 1: On
9	I09_O20_S	**Controls the path from I09 to O20** 0: Off 1: On
8	I08_O20_S	**Controls the path from I08 to O20** 0: Off 1: On
7	I07_O20_S	**Controls the path from I07 to O20** 0: Off 1: On
6	I06_O20_S	**Controls the path from I06 to O20** 0: Off 1: On
5	I05_O20_S	**Controls the path from I05 to O20** 0: Off 1: On
4	I04_O20_S	**Controls the path from I04 to O20** 0: Off 1: On
3	I03_O20_S	**Controls the path from I03 to O20** 0: Off 1: On
2	I02_O20_S	**Controls the path from I02 to O20** 0: Off 1: On
1	I01_O20_S	**Controls the path from I01 to O20** 0: Off 1: On
0	I00_O20_S	**Controls the path from I00 to O20** 0: Off 1: On

11220470 AFE_CONN21 AFE Connection Register 21 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				I28_O21_S	I27_O21_S	I26_O21_S	I25_O21_S	I24_O21_S	I23_O21_S	I22_O21_S	I21_O21_S	I20_O21_S	I19_O21_S	I18_O21_S	I17_O21_S	I16_O21_S
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O21_S	I14_O21_S	I13_O21_S	I12_O21_S	I11_O21_S	I10_O21_S	I09_O21_S	I08_O21_S	I07_O21_S	I06_O21_S	I05_O21_S	I04_O21_S	I03_O21_S	I02_O21_S	I01_O21_S	I00_O21_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	I28_O21_S	**Controls the path from I28 to O21** 0: Off 1: On
27	I27_O21_S	**Controls the path from I27 to O21** 0: Off 1: On
26	I26_O21_S	**Controls the path from I26 to O21** 0: Off 1: On
25	I25_O21_S	**Controls the path from I25 to O21** 0: Off 1: On
24	I24_O21_S	**Controls the path from I24 to O21** 0: Off 1: On
23	I23_O21_S	**Controls the path from I23 to O21** 0: Off 1: On
22	I22_O21_S	**Controls the path from I22 to O21** 0: Off 1: On
21	I21_O21_S	**Controls the path from I21 to O21** 0: Off 1: On
20	I20_O21_S	**Controls the path from I20 to O21** 0: Off 1: On
19	I19_O21_S	**Controls the path from I19 to O21** 0: Off 1: On
18	I18_O21_S	**Controls the path from I18 to O21** 0: Off 1: On
17	I17_O21_S	**Controls the path from I17 to O21** 0: Off 1: On
16	I16_O21_S	**Controls the path from I16 to O21** 0: Off 1: On
15	I15_O21_S	**Controls the path from I15 to O21** 0: Off 1: On
14	I14_O21_S	**Controls the path from I14 to O21** 0: Off 1: On
13	I13_O21_S	**Controls the path from I13 to O21** 0: Off 1: On
12	I12_O21_S	**Controls the path from I12 to O21**

Bit(s)	Name	Description
		0: Off 1: On
11	I11_O21_S	**Controls the path from I11 to O21** 0: Off 1: On
10	I10_O21_S	**Controls the path from I10 to O21** 0: Off 1: On
9	I09_O21_S	**Controls the path from I09 to O21** 0: Off 1: On
8	I08_O21_S	**Controls the path from I08 to O21** 0: Off 1: On
7	I07_O21_S	**Controls the path from I07 to O21** 0: Off 1: On
6	I06_O21_S	**Controls the path from I06 to O21** 0: Off 1: On
5	I05_O21_S	**Controls the path from I05 to O21** 0: Off 1: On
4	I04_O21_S	**Controls the path from I04 to O21** 0: Off 1: On
3	I03_O21_S	**Controls the path from I03 to O21** 0: Off 1: On
2	I02_O21_S	**Controls the path from I02 to O21** 0: Off 1: On
1	I01_O21_S	**Controls the path from I01 to O21** 0: Off 1: On
0	I00_O21_S	**Controls the path from I00 to O21** 0: Off 1: On

11220474 AFE_CONN22 AFE Connection Register 22 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				I28_O22_S	I27_O22_S	I26_O22_S	I25_O22_S	I24_O22_S	I23_O22_S	I22_O22_S	I21_O22_S	I20_O22_S	I19_O22_S	I18_O22_S	I17_O22_S	I16_O22_S
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O22_S	I14_O22_S	I13_O22_S	I12_O22_S	I11_O22_S	I10_O22_S	I09_O22_S	I08_O22_S	I07_O22_S	I06_O22_S	I05_O22_S	I04_O22_S	I03_O22_S	I02_O22_S	I01_O22_S	I00_O22_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
28	I28_O22_S	**Controls the path from I28 to O22** 0: Off 1: On
27	I27_O22_S	**Controls the path from I27 to O22** 0: Off 1: On
26	I26_O22_S	**Controls the path from I26 to O22** 0: Off 1: On
25	I25_O22_S	**Controls the path from I25 to O22** 0: Off 1: On
24	I24_O22_S	**Controls the path from I24 to O22** 0: Off 1: On
23	I23_O22_S	**Controls the path from I23 to O22** 0: Off 1: On
22	I22_O22_S	**Controls the path from I22 to O22** 0: Off 1: On
21	I21_O22_S	**Controls the path from I21 to O22** 0: Off 1: On
20	I20_O22_S	**Controls the path from I20 to O22** 0: Off 1: On
19	I19_O22_S	**Controls the path from I19 to O22** 0: Off 1: On
18	I18_O22_S	**Controls the path from I18 to O22** 0: Off 1: On
17	I17_O22_S	**Controls the path from I17 to O22** 0: Off 1: On
16	I16_O22_S	**Controls the path from I16 to O22** 0: Off 1: On
15	I15_O22_S	**Controls the path from I15 to O22** 0: Off 1: On
14	I14_O22_S	**Controls the path from I14 to O22** 0: Off 1: On
13	I13_O22_S	**Controls the path from I13 to O22** 0: Off 1: On
12	I12_O22_S	**Controls the path from I12 to O22** 0: Off 1: On
11	I11_O22_S	**Controls the path from I11 to O22** 0: Off 1: On
10	I10_O22_S	**Controls the path from I10 to O22** 0: Off 1: On

Bit(s)	Name	Description
9	I09_O22_S	**Controls the path from I09 to O22** 0: Off 1: On
8	I08_O22_S	**Controls the path from I08 to O22** 0: Off 1: On
7	I07_O22_S	**Controls the path from I07 to O22** 0: Off 1: On
6	I06_O22_S	**Controls the path from I06 to O22** 0: Off 1: On
5	I05_O22_S	**Controls the path from I05 to O22** 0: Off 1: On
4	I04_O22_S	**Controls the path from I04 to O22** 0: Off 1: On
3	I03_O22_S	**Controls the path from I03 to O22** 0: Off 1: On
2	I02_O22_S	**Controls the path from I02 to O22** 0: Off 1: On
1	I01_O22_S	**Controls the path from I01 to O22** 0: Off 1: On
0	I00_O22_S	**Controls the path from I00 to O22** 0: Off 1: On

11220478 AFE_CONN23 AFE Connection Register 23 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				I28_O23_S	I27_O23_S	I26_O23_S	I25_O23_S	I24_O23_S	I23_O23_S	I22_O23_S	I21_O23_S	I20_O23_S	I19_O23_S	I18_O23_S	I17_O23_S	I16_O23_S
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O23_S	I14_O23_S	I13_O23_S	I12_O23_S	I11_O23_S	I10_O23_S	I09_O23_S	I08_O23_S	I07_O23_S	I06_O23_S	I05_O23_S	I04_O23_S	I03_O23_S	I02_O23_S	I01_O23_S	I00_O23_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	I28_O23_S	**Controls the path from I28 to O23** 0: Off 1: On
27	I27_O23_S	**Controls the path from I27 to O23** 0: Off 1: On
26	I26_O23_S	**Controls the path from I26 to O23** 0: Off

Bit(s)	Name	Description
		1: On
25	I25_O23_S	**Controls the path from I25 to O23** 0: Off 1: On
24	I24_O23_S	**Controls the path from I24 to O23** 0: Off 1: On
23	I23_O23_S	**Controls the path from I23 to O23** 0: Off 1: On
22	I22_O23_S	**Controls the path from I22 to O23** 0: Off 1: On
21	I21_O23_S	**Controls the path from I21 to O23** 0: Off 1: On
20	I20_O23_S	**Controls the path from I20 to O23** 0: Off 1: On
19	I19_O23_S	**Controls the path from I19 to O23** 0: Off 1: On
18	I18_O23_S	**Controls the path from I18 to O23** 0: Off 1: On
17	I17_O23_S	**Controls the path from I17 to O23** 0: Off 1: On
16	I16_O23_S	**Controls the path from I16 to O23** 0: Off 1: On
15	I15_O23_S	**Controls the path from I15 to O23** 0: Off 1: On
14	I14_O23_S	**Controls the path from I14 to O23** 0: Off 1: On
13	I13_O23_S	**Controls the path from I13 to O23** 0: Off 1: On
12	I12_O23_S	**Controls the path from I12 to O23** 0: Off 1: On
11	I11_O23_S	**Controls the path from I11 to O23** 0: Off 1: On
10	I10_O23_S	**Controls the path from I10 to O23** 0: Off 1: On
9	I09_O23_S	**Controls the path from I09 to O23** 0: Off 1: On
8	I08_O23_S	**Controls the path from I08 to O23** 0: Off 1: On
7	I07_O23_S	**Controls the path from I07 to O23** 0: Off

Bit(s)	Name	Description
		1: On
6	I06_O23_S	**Controls the path from I06 to O23** 0: Off 1: On
5	I05_O23_S	**Controls the path from I05 to O23** 0: Off 1: On
4	I04_O23_S	**Controls the path from I04 to O23** 0: Off 1: On
3	I03_O23_S	**Controls the path from I03 to O23** 0: Off 1: On
2	I02_O23_S	**Controls the path from I02 to O23** 0: Off 1: On
1	I01_O23_S	**Controls the path from I01 to O23** 0: Off 1: On
0	I00_O23_S	**Controls the path from I00 to O23** 0: Off 1: On

1122047C AFE_CONN24 AFE Connection Register 24 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				I28_O24_S	I27_O24_S	I26_O24_S	I25_O24_S	I24_O24_S	I23_O24_S	I22_O24_S	I21_O24_S	I20_O24_S	I19_O24_S	I18_O24_S	I17_O24_S	I16_O24_S
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O24_S	I14_O24_S	I13_O24_S	I12_O24_S	I11_O24_S	I10_O24_S	I09_O24_S	I08_O24_S	I07_O24_S	I06_O24_S	I05_O24_S	I04_O24_S	I03_O24_S	I02_O24_S	I01_O24_S	I00_O24_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	I28_O24_S	**Controls the path from I28 to O24** 0: Off 1: On
27	I27_O24_S	**Controls the path from I27 to O24** 0: Off 1: On
26	I26_O24_S	**Controls the path from I26 to O24** 0: Off 1: On
25	I25_O24_S	**Controls the path from I25 to O24** 0: Off 1: On
24	I24_O24_S	**Controls the path from I24 to O24** 0: Off 1: On
23	I23_O24_S	**Controls the path from I23 to O24**

Bit(s)	Name	Description
		0: Off 1: On
22	I22_O24_S	**Controls the path from I22 to O24** 0: Off 1: On
21	I21_O24_S	**Controls the path from I21 to O24** 0: Off 1: On
20	I20_O24_S	**Controls the path from I20 to O24** 0: Off 1: On
19	I19_O24_S	**Controls the path from I19 to O24** 0: Off 1: On
18	I18_O24_S	**Controls the path from I18 to O24** 0: Off 1: On
17	I17_O24_S	**Controls the path from I17 to O24** 0: Off 1: On
16	I16_O24_S	**Controls the path from I16 to O24** 0: Off 1: On
15	I15_O24_S	**Controls the path from I15 to O24** 0: Off 1: On
14	I14_O24_S	**Controls the path from I14 to O24** 0: Off 1: On
13	I13_O24_S	**Controls the path from I13 to O24** 0: Off 1: On
12	I12_O24_S	**Controls the path from I12 to O24** 0: Off 1: On
11	I11_O24_S	**Controls the path from I11 to O24** 0: Off 1: On
10	I10_O24_S	**Controls the path from I10 to O24** 0: Off 1: On
9	I09_O24_S	**Controls the path from I09 to O24** 0: Off 1: On
8	I08_O24_S	**Controls the path from I08 to O24** 0: Off 1: On
7	I07_O24_S	**Controls the path from I07 to O24** 0: Off 1: On
6	I06_O24_S	**Controls the path from I06 to O24** 0: Off 1: On
5	I05_O24_S	**Controls the path from I05 to O24** 0: Off 1: On
4	I04_O24_S	**Controls the path from I04 to O24**

Bit(s)	Name	Description
		0: Off 1: On
3	I03_O24_S	**Controls the path from I03 to O24** 0: Off 1: On
2	I02_O24_S	**Controls the path from I02 to O24** 0: Off 1: On
1	I01_O24_S	**Controls the path from I01 to O24** 0: Off 1: On
0	I00_O24_S	**Controls the path from I00 to O24** 0: Off 1: On

112204B0 AFE_CONN25 AFE Connection Register 25 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				I28_O25_S	I27_O25_S	I26_O25_S	I25_O25_S	I24_O25_S	I23_O25_S	I22_O25_S	I21_O25_S	I20_O25_S	I19_O25_S	I18_O25_S	I17_O25_S	I16_O25_S
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O25_S	I14_O25_S	I13_O25_S	I12_O25_S	I11_O25_S	I10_O25_S	I09_O25_S	I08_O25_S	I07_O25_S	I06_O25_S	I05_O25_S	I04_O25_S	I03_O25_S	I02_O25_S	I01_O25_S	I00_O25_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	I28_O25_S	**Controls the path from I28 to O25** 0: Off 1: On
27	I27_O25_S	**Controls the path from I27 to O25** 0: Off 1: On
26	I26_O25_S	**Controls the path from I26 to O25** 0: Off 1: On
25	I25_O25_S	**Controls the path from I25 to O25** 0: Off 1: On
24	I24_O25_S	**Controls the path from I24 to O25** 0: Off 1: On
23	I23_O25_S	**Controls the path from I23 to O25** 0: Off 1: On
22	I22_O25_S	**Controls the path from I22 to O25** 0: Off 1: On
21	I21_O25_S	**Controls the path from I21 to O25** 0: Off 1: On

Bit(s)	Name	Description
20	I20_O25_S	**Controls the path from I20 to O25** 0: Off 1: On
19	I19_O25_S	**Controls the path from I19 to O25** 0: Off 1: On
18	I18_O25_S	**Controls the path from I18 to O25** 0: Off 1: On
17	I17_O25_S	**Controls the path from I17 to O25** 0: Off 1: On
16	I16_O25_S	**Controls the path from I16 to O25** 0: Off 1: On
15	I15_O25_S	**Controls the path from I15 to O25** 0: Off 1: On
14	I14_O25_S	**Controls the path from I14 to O25** 0: Off 1: On
13	I13_O25_S	**Controls the path from I13 to O25** 0: Off 1: On
12	I12_O25_S	**Controls the path from I12 to O25** 0: Off 1: On
11	I11_O25_S	**Controls the path from I11 to O25** 0: Off 1: On
10	I10_O25_S	**Controls the path from I10 to O25** 0: Off 1: On
9	I09_O25_S	**Controls the path from I09 to O25** 0: Off 1: On
8	I08_O25_S	**Controls the path from I08 to O25** 0: Off 1: On
7	I07_O25_S	**Controls the path from I07 to O25** 0: Off 1: On
6	I06_O25_S	**Controls the path from I06 to O25** 0: Off 1: On
5	I05_O25_S	**Controls the path from I05 to O25** 0: Off 1: On
4	I04_O25_S	**Controls the path from I04 to O25** 0: Off 1: On
3	I03_O25_S	**Controls the path from I03 to O25** 0: Off 1: On
2	I02_O25_S	**Controls the path from I02 to O25** 0: Off 1: On

Bit(s)	Name	Description
1	I01_O25_S	**Controls the path from I01 to O25** 0: Off 1: On
0	I00_O25_S	**Controls the path from I00 to O25** 0: Off 1: On

112204B4 AFE_CONN26 AFE Connection Register 26 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				I28_O26_S	I27_O26_S	I26_O26_S	I25_O26_S	I24_O26_S	I23_O26_S	I22_O26_S	I21_O26_S	I20_O26_S	I19_O26_S	I18_O26_S	I17_O26_S	I16_O26_S
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O26_S	I14_O26_S	I13_O26_S	I12_O26_S	I11_O26_S	I10_O26_S	I09_O26_S	I08_O26_S	I07_O26_S	I06_O26_S	I05_O26_S	I04_O26_S	I03_O26_S	I02_O26_S	I01_O26_S	I00_O26_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	I28_O26_S	**Controls the path from I28 to O26** 0: Off 1: On
27	I27_O26_S	**Controls the path from I27 to O26** 0: Off 1: On
26	I26_O26_S	**Controls the path from I26 to O26** 0: Off 1: On
25	I25_O26_S	**Controls the path from I25 to O26** 0: Off 1: On
24	I24_O26_S	**Controls the path from I24 to O26** 0: Off 1: On
23	I23_O26_S	**Controls the path from I23 to O26** 0: Off 1: On
22	I22_O26_S	**Controls the path from I22 to O26** 0: Off 1: On
21	I21_O26_S	**Controls the path from I21 to O26** 0: Off 1: On
20	I20_O26_S	**Controls the path from I20 to O26** 0: Off 1: On
19	I19_O26_S	**Controls the path from I19 to O26** 0: Off 1: On
18	I18_O26_S	**Controls the path from I18 to O26** 0: Off

Bit(s)	Name	Description
		1: On
17	I17_O26_S	**Controls the path from I17 to O26** 0: Off 1: On
16	I16_O26_S	**Controls the path from I16 to O26** 0: Off 1: On
15	I15_O26_S	**Controls the path from I15 to O26** 0: Off 1: On
14	I14_O26_S	**Controls the path from I14 to O26** 0: Off 1: On
13	I13_O26_S	**Controls the path from I13 to O26** 0: Off 1: On
12	I12_O26_S	**Controls the path from I12 to O26** 0: Off 1: On
11	I11_O26_S	**Controls the path from I11 to O26** 0: Off 1: On
10	I10_O26_S	**Controls the path from I10 to O26** 0: Off 1: On
9	I09_O26_S	**Controls the path from I09 to O26** 0: Off 1: On
8	I08_O26_S	**Controls the path from I08 to O26** 0: Off 1: On
7	I07_O26_S	**Controls the path from I07 to O26** 0: Off 1: On
6	I06_O26_S	**Controls the path from I06 to O26** 0: Off 1: On
5	I05_O26_S	**Controls the path from I05 to O26** 0: Off 1: On
4	I04_O26_S	**Controls the path from I04 to O26** 0: Off 1: On
3	I03_O26_S	**Controls the path from I03 to O26** 0: Off 1: On
2	I02_O26_S	**Controls the path from I02 to O26** 0: Off 1: On
1	I01_O26_S	**Controls the path from I01 to O26** 0: Off 1: On
0	I00_O26_S	**Controls the path from I00 to O26** 0: Off 1: On

112204B8 AFE_CONN27 AFE Connection Register 27 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				I28_O27_S	I27_O27_S	I26_O27_S	I25_O27_S	I24_O27_S	I23_O27_S	I22_O27_S	I21_O27_S	I20_O27_S	I19_O27_S	I18_O27_S	I17_O27_S	I16_O27_S
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O27_S	I14_O27_S	I13_O27_S	I12_O27_S	I11_O27_S	I10_O27_S	I09_O27_S	I08_O27_S	I07_O27_S	I06_O27_S	I05_O27_S	I04_O27_S	I03_O27_S	I02_O27_S	I01_O27_S	I00_O27_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	I28_O27_S	**Controls the path from I28 to O27** 0: Off 1: On
27	I27_O27_S	**Controls the path from I27 to O27** 0: Off 1: On
26	I26_O27_S	**Controls the path from I26 to O27** 0: Off 1: On
25	I25_O27_S	**Controls the path from I25 to O27** 0: Off 1: On
24	I24_O27_S	**Controls the path from I24 to O27** 0: Off 1: On
23	I23_O27_S	**Controls the path from I23 to O27** 0: Off 1: On
22	I22_O27_S	**Controls the path from I22 to O27** 0: Off 1: On
21	I21_O27_S	**Controls the path from I21 to O27** 0: Off 1: On
20	I20_O27_S	**Controls the path from I20 to O27** 0: Off 1: On
19	I19_O27_S	**Controls the path from I19 to O27** 0: Off 1: On
18	I18_O27_S	**Controls the path from I18 to O27** 0: Off 1: On
17	I17_O27_S	**Controls the path from I17 to O27** 0: Off 1: On
16	I16_O27_S	**Controls the path from I16 to O27** 0: Off 1: On
15	I15_O27_S	**Controls the path from I15 to O27** 0: Off

Bit(s)	Name	Description
		1: On
14	I14_O27_S	**Controls the path from I14 to O27** 0: Off 1: On
13	I13_O27_S	**Controls the path from I13 to O27** 0: Off 1: On
12	I12_O27_S	**Controls the path from I12 to O27** 0: Off 1: On
11	I11_O27_S	**Controls the path from I11 to O27** 0: Off 1: On
10	I10_O27_S	**Controls the path from I10 to O27** 0: Off 1: On
9	I09_O27_S	**Controls the path from I09 to O27** 0: Off 1: On
8	I08_O27_S	**Controls the path from I08 to O27** 0: Off 1: On
7	I07_O27_S	**Controls the path from I07 to O27** 0: Off 1: On
6	I06_O27_S	**Controls the path from I06 to O27** 0: Off 1: On
5	I05_O27_S	**Controls the path from I05 to O27** 0: Off 1: On
4	I04_O27_S	**Controls the path from I04 to O27** 0: Off 1: On
3	I03_O27_S	**Controls the path from I03 to O27** 0: Off 1: On
2	I02_O27_S	**Controls the path from I02 to O27** 0: Off 1: On
1	I01_O27_S	**Controls the path from I01 to O27** 0: Off 1: On
0	I00_O27_S	**Controls the path from I00 to O27** 0: Off 1: On

112204BC AFE_CONN28 AFE Connection Register 28 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				I28_O28_S	I27_O28_S	I26_O28_S	I25_O28_S	I24_O28_S	I23_O28_S	I22_O28_S	I21_O28_S	I20_O28_S	I19_O28_S	I18_O28_S	I17_O28_S	I16_O28_S
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O28_S	I14_O28_S	I13_O28_S	I12_O28_S	I11_O28_S	I10_O28_S	I09_O28_S	I08_O28_S	I07_O28_S	I06_O28_S	I05_O28_S	I04_O28_S	I03_O28_S	I02_O28_S	I01_O28_S	I00_O28_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	I28_O28_S	**Controls the path from I28 to O28** 0: Off 1: On
27	I27_O28_S	**Controls the path from I27 to O28** 0: Off 1: On
26	I26_O28_S	**Controls the path from I26 to O28** 0: Off 1: On
25	I25_O28_S	**Controls the path from I25 to O28** 0: Off 1: On
24	I24_O28_S	**Controls the path from I24 to O28** 0: Off 1: On
23	I23_O28_S	**Controls the path from I23 to O28** 0: Off 1: On
22	I22_O28_S	**Controls the path from I22 to O28** 0: Off 1: On
21	I21_O28_S	**Controls the path from I21 to O28** 0: Off 1: On
20	I20_O28_S	**Controls the path from I20 to O28** 0: Off 1: On
19	I19_O28_S	**Controls the path from I19 to O28** 0: Off 1: On
18	I18_O28_S	**Controls the path from I18 to O28** 0: Off 1: On
17	I17_O28_S	**Controls the path from I17 to O28** 0: Off 1: On
16	I16_O28_S	**Controls the path from I16 to O28** 0: Off 1: On
15	I15_O28_S	**Controls the path from I15 to O28** 0: Off 1: On
14	I14_O28_S	**Controls the path from I14 to O28** 0: Off 1: On
13	I13_O28_S	**Controls the path from I13 to O28** 0: Off 1: On
12	I12_O28_S	**Controls the path from I12 to O28**

Bit(s)	Name	Description
		0: Off 1: On
11	I11_O28_S	**Controls the path from I11 to O28** 0: Off 1: On
10	I10_O28_S	**Controls the path from I10 to O28** 0: Off 1: On
9	I09_O28_S	**Controls the path from I09 to O28** 0: Off 1: On
8	I08_O28_S	**Controls the path from I08 to O28** 0: Off 1: On
7	I07_O28_S	**Controls the path from I07 to O28** 0: Off 1: On
6	I06_O28_S	**Controls the path from I06 to O28** 0: Off 1: On
5	I05_O28_S	**Controls the path from I05 to O28** 0: Off 1: On
4	I04_O28_S	**Controls the path from I04 to O28** 0: Off 1: On
3	I03_O28_S	**Controls the path from I03 to O28** 0: Off 1: On
2	I02_O28_S	**Controls the path from I02 to O28** 0: Off 1: On
1	I01_O28_S	**Controls the path from I01 to O28** 0: Off 1: On
0	I00_O28_S	**Controls the path from I00 to O28** 0: Off 1: On

112204C0 AFE_CONN29 AFE Connection Register 29 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				I28_O29_S	I27_O29_S	I26_O29_S	I25_O29_S	I24_O29_S	I23_O29_S	I22_O29_S	I21_O29_S	I20_O29_S	I19_O29_S	I18_O29_S	I17_O29_S	I16_O29_S
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I15_O29_S	I14_O29_S	I13_O29_S	I12_O29_S	I11_O29_S	I10_O29_S	I09_O29_S	I08_O29_S	I07_O29_S	I06_O29_S	I05_O29_S	I04_O29_S	I03_O29_S	I02_O29_S	I01_O29_S	I00_O29_S
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
28	I28_O29_S	**Controls the path from I28 to O29** 0: Off 1: On
27	I27_O29_S	**Controls the path from I27 to O29** 0: Off 1: On
26	I26_O29_S	**Controls the path from I26 to O29** 0: Off 1: On
25	I25_O29_S	**Controls the path from I25 to O29** 0: Off 1: On
24	I24_O29_S	**Controls the path from I24 to O29** 0: Off 1: On
23	I23_O29_S	**Controls the path from I23 to O29** 0: Off 1: On
22	I22_O29_S	**Controls the path from I22 to O29** 0: Off 1: On
21	I21_O29_S	**Controls the path from I21 to O29** 0: Off 1: On
20	I20_O29_S	**Controls the path from I20 to O29** 0: Off 1: On
19	I19_O29_S	**Controls the path from I19 to O29** 0: Off 1: On
18	I18_O29_S	**Controls the path from I18 to O29** 0: Off 1: On
17	I17_O29_S	**Controls the path from I17 to O29** 0: Off 1: On
16	I16_O29_S	**Controls the path from I16 to O29** 0: Off 1: On
15	I15_O29_S	**Controls the path from I15 to O29** 0: Off 1: On
14	I14_O29_S	**Controls the path from I14 to O29** 0: Off 1: On
13	I13_O29_S	**Controls the path from I13 to O29** 0: Off 1: On
12	I12_O29_S	**Controls the path from I12 to O29** 0: Off 1: On
11	I11_O29_S	**Controls the path from I11 to O29** 0: Off 1: On
10	I10_O29_S	**Controls the path from I10 to O29** 0: Off 1: On

Bit(s)	Name	Description
9	I09_O29_S	**Controls the path from I09 to O29** 0: Off 1: On
8	I08_O29_S	**Controls the path from I08 to O29** 0: Off 1: On
7	I07_O29_S	**Controls the path from I07 to O29** 0: Off 1: On
6	I06_O29_S	**Controls the path from I06 to O29** 0: Off 1: On
5	I05_O29_S	**Controls the path from I05 to O29** 0: Off 1: On
4	I04_O29_S	**Controls the path from I04 to O29** 0: Off 1: On
3	I03_O29_S	**Controls the path from I03 to O29** 0: Off 1: On
2	I02_O29_S	**Controls the path from I02 to O29** 0: Off 1: On
1	I01_O29_S	**Controls the path from I01 to O29** 0: Off 1: On
0	I00_O29_S	**Controls the path from I00 to O29** 0: Off 1: On

11220494 AFE_CONN_RS **AFE Connection Right Shift Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			O29_RS	O28_RS	O27_RS	O26_RS	O25_RS	O24_RS	O23_RS	O22_RS	O21_RS	O20_RS	O19_RS	O18_RS	O17_RS	O16_RS
Type			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	O15_RS	O14_RS	O13_RS	O12_RS	O11_RS	O10_RS	O09_RS	O08_RS	O07_RS	O06_RS	O05_RS	O04_RS	O03_RS	O02_RS	O01_RS	O00_RS
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29	O29_RS	**Controls the enabling of right shift 1 bit of O29** 0: No shift 1: Right shift 1 bit
28	O28_RS	**Controls the enabling of right shift 1 bit of O28** 0: No shift 1: Right shift 1 bit
27	O27_RS	**Controls the enabling of right shift 1 bit of O27** 0: No shift 1: Right shift 1 bit

Bit(s)	Name	Description
26	O26_RS	**Controls the enabling of right shift 1 bit of O26** 0: No shift 1: Right shift 1 bit
25	O25_RS	**Controls the enabling of right shift 1 bit of O25** 0: No shift 1: Right shift 1 bit
24	O24_RS	**Controls the enabling of right shift 1 bit of O24** 0: No shift 1: Right shift 1 bit
23	O23_RS	**Controls the enabling of right shift 1 bit of O23** 0: No shift 1: Right shift 1 bit
22	O22_RS	**Controls the enabling of right shift 1 bit of O22** 0: No shift 1: Right shift 1 bit
21	O21_RS	**Controls the enabling of right shift 1 bit of O21** 0: No shift 1: Right shift 1 bit
20	O20_RS	**Controls the enabling of right shift 1 bit of O20** 0: No shift 1: Right shift 1 bit
19	O19_RS	**Controls the enabling of right shift 1 bit of O19** 0: No shift 1: Right shift 1 bit
18	O18_RS	**Controls the enabling of right shift 1 bit of O18** 0: No shift 1: Right shift 1 bit
17	O17_RS	**Controls the enabling of right shift 1 bit of O17** 0: No shift 1: Right shift 1 bit
16	O16_RS	**Controls the enabling of right shift 1 bit of O16** 0: No shift 1: Right shift 1 bit
15	O15_RS	**Controls the enabling of right shift 1 bit of O15** 0: No shift 1: Right shift 1 bit
14	O14_RS	**Controls the enabling of right shift 1 bit of O14** 0: No shift 1: Right shift 1 bit
13	O13_RS	**Controls the enabling of right shift 1 bit of O13** 0: No shift 1: Right shift 1 bit
12	O12_RS	**Controls the enabling of right shift 1 bit of O12** 0: No shift 1: Right shift 1 bit
11	O11_RS	**Controls the enabling of right shift 1 bit of O11** 0: No shift 1: Right shift 1 bit
10	O10_RS	**Controls the enabling of right shift 1 bit of O10** 0: No shift 1: Right shift 1 bit
9	O09_RS	**Controls the enabling of right shift 1 bit of O9** 0: No shift 1: Right shift 1 bit
8	O08_RS	**Controls the enabling of right shift 1 bit of O8** 0: No shift 1: Right shift 1 bit

Bit(s)	Name	Description
7	O07_RS	**Controls the enabling of right shift 1 bit of O7** 0: No shift 1: Right shift 1 bit
6	O06_RS	**Controls the enabling of right shift 1 bit of O6** 0: No shift 1: Right shift 1 bit
5	O05_RS	**Controls the enabling of right shift 1 bit of O5** 0: No shift 1: Right shift 1 bit
4	O04_RS	**Controls the enabling of right shift 1 bit of O4** 0: No shift 1: Right shift 1 bit
3	O03_RS	**Controls the enabling of right shift 1 bit of O3** 0: No shift 1: Right shift 1 bit
2	O02_RS	**Controls the enabling of right shift 1 bit of O2** 0: No shift 1: Right shift 1 bit
1	O01_RS	**Controls the enabling of right shift 1 bit of O1** 0: No shift 1: Right shift 1 bit
0	O00_RS	**Controls the enabling of right shift 1 bit of O0** 0: No shift 1: Right shift 1 bit

11220498 AFE_CONN_DI **AFE Connection Dithering Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			O29_DI	O28_DI	O27_DI	O26_DI	O25_DI	O24_DI	O23_DI	O22_DI	O21_DI	O20_DI	O19_DI	O18_DI	O17_DI	O16_DI
Type			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	O15_DI	O14_DI	O13_DI	O12_DI	O11_DI	O10_DI	O09_DI	O08_DI	O07_DI	O06_DI	O05_DI	O04_DI	O03_DI	O02_DI	O01_DI	O00_DI
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29	O29_DI	**Controls the enabling of dithering of O29, only valid when O29_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
28	O28_DI	**Controls the enabling of dithering of O28, only valid when O28_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
27	O27_DI	**Controls the enabling of dithering of O27, only valid when O27_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
26	O26_DI	**Controls the enabling of dithering of O26, only valid when O26_24bit = 0** 0: No dithering

Bit(s)	Name	Description
		1: Dithering LSB 8 bits
25	O25_DI	**Controls the enabling of dithering of O25, only valid when O25_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
24	O24_DI	**Controls the enabling of dithering of O24, only valid when O24_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
23	O23_DI	**Controls the enabling of dithering of O23, only valid when O23_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
22	O22_DI	**Controls the enabling of dithering of O22, only valid when O22_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
21	O21_DI	**Controls the enabling of dithering of O21, only valid when O21_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
20	O20_DI	**Controls the enabling of dithering of O20, only valid when O20_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
19	O19_DI	**Controls the enabling of dithering of O19, only valid when O19_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
18	O18_DI	**Controls the enabling of dithering of O18, only valid when O18_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
17	O17_DI	**Controls the enabling of dithering of O17, only valid when O17_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
16	O16_DI	**Controls the enabling of dithering of O16, only valid when O16_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
15	O15_DI	**Controls the enabling of dithering of O15, only valid when O15_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
14	O14_DI	**Controls the enabling of dithering of O14, only valid when O14_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
13	O13_DI	**Controls the enabling of dithering of O13, only valid when O13_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
12	O12_DI	**Controls the enabling of dithering of O12, only valid when O12_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
11	O11_DI	**Controls the enabling of dithering of O11, only valid when**

Bit(s)	Name	Description
		O11_24bit = 0 0: No dithering 1: Dithering LSB 8 bits
10	O10_DI	**Controls the enabling of dithering of O10, only valid when O10_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
9	O09_DI	**Controls the enabling of dithering of O09, only valid when O09_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
8	O08_DI	**Controls the enabling of dithering of O08, only valid when O08_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
7	O07_DI	**Controls the enabling of dithering of O07, only valid when O07_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
6	O06_DI	**Controls the enabling of dithering of O06, only valid when O06_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
5	O05_DI	**Controls the enabling of dithering of O05, only valid when O05_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
4	O04_DI	**Controls the enabling of dithering of O04, only valid when O04_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
3	O03_DI	**Controls the enabling of dithering of O03, only valid when O03_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
2	O02_DI	**Controls the enabling of dithering of O02, only valid when O02_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
1	O01_DI	**Controls the enabling of dithering of O01, only valid when O01_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits
0	O00_DI	**Controls the enabling of dithering of O00, only valid when O00_24bit = 0** 0: No dithering 1: Dithering LSB 8 bits

11220034 AFE_I2S_CON1 **AFE I2S Control Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I2S2_LR_SWAP														I2S_ONOFF_NOT_RESET_	I2S2_SEL_O03_O04

															CK_ENABLE	
Type	RW														RW	RW
Reset	0														0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				I2S2_HD_EN	I2S2_OUT_MODE						INV_LRCK		I2S2_FMT		I2S2_WLEN	I2S2_EN
Type				RW	RW						RW		RW		RW	RW
Reset				0	0	0	0	0			0		0		0	0

Bit(s)	Name	Description
31	I2S2_LR_SWAP	**Only for the flexibility usage** 0: No swapping L and R channel 1: Swap left and right channel
17	I2S_ONOFF_NOT_RESET_CK_ENABLE	**Controls I2S on/off to reset ck_enable or not.** 0: On/off reset ck_enable 1: On/off not reset ck_enable
16	I2S2_SEL_O03_O04	**sel input for I2S1** 0: sel o28 o29 to I2S1 1: sel o03 o04 to I2S1
12	I2S2_HD_EN	**Enables low-jitter bck HD audio** 0: Normal h26m clock 1: Low-jitter clock
11:8	I2S2_OUT_MODE	**Controls the sampling frequency for I2S2 output path** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k
5	INV_LRCK	**Controls the phase of I2S path** 0: Not invert LRCK 1: Invert LRCK for LJ mode
3	I2S2_FMT	**Controls the format for I2S path** 0: EIAJ 1: I2S
1	I2S2_WLEN	**Controls the word length of I2S** 0: 16 bits 1: 32 bits
0	I2S2_EN	**Controls the enbling of I2S path** 0: Disable I2S output 1: Enable I2S output

11220038 AFE_I2S_CON2 AFE I2S Control Register 2 08000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I2S3_LR_SWAP			I2S3 _UPD ATE_ WORD					I2S3_bck_inv	I2S3_fpga_bit_test	I2S3_fpga_bi t	I2S3_LOOPBACK			I2S_ONOFF_NOT_RESET_CK_ENABLE	
Type	RW			RW					RW	RW	RW	RW			RW	
Reset	0			0	1	0	0	0	0	0	0	0			0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				I2S3_HD_EN	I2S3_OUT_MODE								I2S3_FMT		I2S3_WLEN	I2S3_EN
Type				RW	RW								RW		RW	RW
Reset				0	0	0	0	0					0		0	0

Bit(s)	Name	Description
31	I2S3_LR_SWAP	**Only for flexibility usage** 0: Not swap L and R channel 1: Swap left and right channel
28:24	I2S3_UPDATE_WORD	**I2S3 buffer update timing** Valid between 0 ~ 15 for 32fs BCK or 0 ~ 31 for 64fs BCK
23	I2S3_bck_inv	**Inverts bit_ck for EXTADC** 0: Does not invert bit_ck (to EXTADC) 1: Invert bit_ck (to EXTADC)
22	I2S3_fpga_bit_test	**For debugging** 0: sdata depends on bit[20]. 1: sdata depends on bit[21].
21	I2S3_fpga_bit	**Valid when bit[22] = 1** 0: sdata set to 0 1: sdata set to 1
20	I2S3_LOOPBACK	**Controls I2S internal loopback mode** Loopback source is from I2S4 output. 0: Normal I2S in 1: I2S in from internal DAC I2S output
17	I2S_ONOFF_NOT_RESET_CK_ENABLE	**Controls I2S on/off to reset ck_enable or not** 0: On/off reset ck_enable 1: On/off not reset ck_enable
12	I2S3_HD_EN	**Enables low-jitter bck HD audio** 0: Normal h26m clock 1: Low-jitter clock
11:8	I2S3_OUT_MODE	**Controls the sampling frequency for I2S3 output path** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k

Bit(s)	Name	Description
3	I2S3_FMT	0: EIAJ 1: I2S
1	I2S3_WLEN	**Controls the word length of I2S** 0: 16 bits 1: 32 bits
0	I2S3_EN	**Controls the enbling of I2S path** 0: Disable I2S input 1: Enable I2S input

1122003C AFE_MRGIF_CON **AFE Merge Interface Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									MRGIF_I2S_MODE				MRGIF_I2S_LOOPBACK	MRGIF_TX2RX_LOOPBACK		MRGIF_I2S_EN
Type									RW				RW	RW		RW
Reset									0	0	0	0	0	0		0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		MRG_CLK_NO_INV	MRG_I2S_TX_DIS	MRG_CNT_CLR	MRG_SYNC_DLY				MRG_CLK_EDGE_DLY		MRG_CLK_DLY					MRGIF_EN
Type		RW	RW	RW	RW				RW		RW					RW
Reset		0	0	0	0	0	0	0	0	0	0	0				0

Bit(s)	Name	Description
23:20	MRGIF_I2S_MODE	**Merge I2S mode** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k
19	MRGIF_I2S_LOOPBACK	**Merge interface I2S loopback** 0: Off 1: On
18	MRGIF_TX2RX_LOOPBACK	**Merge interface TX to RX loopback** (mrg_rx = mrg_tx) 0: Off 1: On
16	MRGIF_I2S_EN	**Merge interface I2S transmit** 0: Off 1: On
14	MRG_CLK_NO_INV	**Set to 1 to not to invert merge interface I2S clock.** 0: Inverse 1: Non-inverse
13	MRG_I2S_TX_DIS	**Set to 1 to disable merge interface I2S TX.** 0: Enable 1: Disable
12	MRG_CNT_CLR	**When this bit is 1, the I2S and PCM's monitor counter**

Bit(s)	Name	Description
		will be cleared. When monitor is used, this bit should be 0. 0: Off 1: On
11:8	MRG_SYNC_DLY	**Merge interface sync delay number in 26M clock domain**
7:6	MRG_CLK_EDGE_DLY	**Sample and output data's delay number in 26M clock domain**
5:4	MRG_CLK_DLY	**Merge interface clk delay number in 26M clock domain**
0	MRGIF_EN	**Enables merge interface** 0: Off 1: On

11220040 AFE_DL1_BASE AFE DL1 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL1_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL1_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	AFE_DL1_BASE	**Base address of DL1 input in master mode** Always set AFE_DL1_BASE[3:0] = 4'h0 for the convenience of the hardware implementation.

11220044 AFE_DL1_CUR AFE DL1 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL1_CUR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL1_CUR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AFE_DL1_CUR	Indicates the current address of the DL1 input buffer.

11220048 AFE_DL1_END AFE_DL1_END 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL1_END															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL1_END												AFE_DL1_END_LSB			
Type	RW												RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Name	Description
31:4	AFE_DL1_END	**End address of DL1 input in master mode** Always set AFE_DL1_END[3:0] = 4'hf for the convenience of the hardware implementation.
3:0	AFE_DL1_END_LSB	

1122004C AFE_I2S_CON3 AFE I2S Control Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	I2S4_LR_SWAP														I2S_ONOFF_NOT_RESET_CK_ENABLE	
Type	RW														RW	
Reset	0														0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				I2S4_HD_EN	I2S4_OUT_MODE						INV_LRCK		I2S4_FMT		I2S4_WLEN	I2S4_EN
Type				RW	RW						RW		RW		RW	RW
Reset				0	0	0	0	0			0		0		0	0

Bit(s)	Name	Description
31	I2S4_LR_SWAP	**Only for flexibility usage** 0: Not swap L and R channel 1: Swaps left and right channel
17	I2S_ONOFF_NOT_RESET_CK_ENABLE	**Controls I2S on/off to reset ck_enable or not** 0: On/off reset ck_enable 1: On/off not reset ck_enable
12	I2S4_HD_EN	**Enables low-jitter bck HD audio** 0: Normal h26m clock 1: Low-jitter clock
11:8	I2S4_OUT_MODE	**Controls the sampling frequency for I2S4 output path** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k

Bit(s)	Name	Description
		1100b: 96k 1101b: 176.4k 1110b: 192k
5	INV_LRCK	**Controls the phase of I2S4 path** 0: Not invert LRCK 1: Invert LRCK for LJ mode
3	I2S4_FMT	**Controls the format for I2S4 path** 0: EIAJ 1: I2S
1	I2S4_WLEN	**Controls the word length of I2S4 path** 0: 16 bits 1: 32 bits
0	I2S4_EN	**Controls the enbling of I2S path** 0: Disable I2S output 1: Enable I2S output

11220050 AFE_DL2_BASE AFE DL2 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL2_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL2_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	AFE_DL2_BASE	**Base address of DL2 input in master mode** Always set AFE_DL2_BASE[3:0] = 4'h0 for the convenience of the hardware implementation.

11220054 AFE_DL2_CUR AFE DL2 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL2_CUR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL2_CUR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AFE_DL2_CUR	Indicates the current address of the DL2 input buffer

11220058 AFE_DL2_END AFE_DL2_END 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL2_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL2_END												AFE_DL2_END_LSB			
Type	RW												RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Name	Description
31:4	AFE_DL2_END	**End address of DL2 input in master mode** Always set AFE_DL2_END[3:0] = 4'hf for the convenience of the hardware implementation.
3:0	AFE_DL2_END_LSB	

11220360 AFE_DL3_BASE AFE DL3 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL3_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL3_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	AFE_DL3_BASE	**Base address of DL3 input in master mode** Always set AFE_DL3_BASE[3:0] = 4'h0 for the convenience of the hardware implementation.

11220364 AFE_DL3_CUR AFE DL3 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL3_CUR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL3_CUR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AFE_DL3_CUR	Indicates the current address of the DL3 input buffer

11220368 AFE_DL3_END AFE_DL3_END 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	AFE_DL3_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL3_END												AFE_DL3_END_LSB			
Type	RW												RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Name	Description
31:4	AFE_DL3_END	**End address of DL3 input in master mode** Always set AFE_DL3_END[3:0] = 4'hf for the convenience of the hardware implementation.
3:0	AFE_DL3_END_LSB	

1122006C AFE_CONN_24BIT AFE Connection 24-bit Register 0019E018

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			O29_24BIT	O28_24BIT	O27_24BIT	O26_24BIT	O25_24BIT	O24_24BIT	O23_24BIT	O22_24BIT	O21_24BIT	O20_24BIT	O19_24BIT	O18_24BIT	O17_24BIT	O16_24BIT
Type			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0	0	0	0	1	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	O15_24BIT	O14_24BIT	O13_24BIT	O12_24BIT	O11_24BIT	O10_24BIT	O09_24BIT	O08_24BIT	O07_24BIT	O06_24BIT	O05_24BIT	O04_24BIT	O03_24BIT	O02_24BIT	O01_24BIT	O00_24BIT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0

Bit(s)	Name	Description
29	O29_24BIT	**Controls output data format of O25** 0: 16-bit 1: 24-bit
28	O28_24BIT	0: 16-bit 1: 24-bit
27	O27_24BIT	0: 16-bit 1: 24-bit
26	O26_24BIT	0: 16-bit 1: 24-bit
25	O25_24BIT	0: 16-bit 1: 24-bit
24	O24_24BIT	**Controls output data format of O24** 0: 16-bit 1: 24-bit
23	O23_24BIT	**Controls output data format of O23** 0: 16-bit 1: 24-bit
22	O22_24BIT	**Controls output data format of O22** 0: 16-bit 1: 24-bit
21	O21_24BIT	**Controls output data format of O21** 0: 16-bit 1: 24-bit
20	O20_24BIT	**Controls output data format of O20** 0: 16-bit

Bit(s)	Name	Description
		1: 24-bit
19	O19_24BIT	**Controls output data format of O19** 0: 16-bit 1: 24-bit
18	O18_24BIT	**Controls output data format of O18** 0: 16-bit 1: 24-bit
17	O17_24BIT	**Controls output data format of O17** 0: 16-bit 1: 24-bit
16	O16_24BIT	**Controls output data format of O16** 0: 16-bit 1: 24-bit
15	O15_24BIT	**Controls output data format of O15** 0: 16-bit 1: 24-bit
14	O14_24BIT	**Controls output data format of O14** 0: 16-bit 1: 24-bit
13	O13_24BIT	**Controls output data format of O13** 0: 16-bit 1: 24-bit
12	O12_24BIT	**Controls output data format of O12** 0: 16-bit 1: 24-bit
11	O11_24BIT	**Controls output data format of O11** 0: 16-bit 1: 24-bit
10	O10_24BIT	**Controls output data format of O10** 0: 16-bit 1: 24-bit
9	O09_24BIT	**Controls output data format of O09** 0: 16-bit 1: 24-bit
8	O08_24BIT	**Controls output data format of O08** 0: 16-bit 1: 24-bit
7	O07_24BIT	**Controls output data format of O07** 0: 16-bit 1: 24-bit
6	O06_24BIT	**Controls output data format of O06** 0: 16-bit 1: 24-bit
5	O05_24BIT	**Controls output data format of O05** 0: 16-bit 1: 24-bit
4	O04_24BIT	**Controls output data format of O04** 0: 16-bit 1: 24-bit
3	O03_24BIT	**Controls output data format of O03.** 0: 16-bit 1: 24-bit
2	O02_24BIT	**Controls output data format of O02** 0: 16-bit 1: 24-bit
1	O01_24BIT	**Controls output data format of O01** 0: 16-bit

Bit(s)	Name	Description
		1: 24-bit
0	O00_24BIT	**Controls output data format of O00** 0: 16-bit 1: 24-bit

11220070 AFE_AWB_BASE AFE AWB Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_AWB_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_AWB_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	AFE_AWB_BASE	**Base address of AWB input in master mode** Always set AFE_AWB_BASE[2:0] = 3'h0 for the convenience of the hardware implementation.

11220078 AFE_AWB_END AFE AWB End Address Register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_AWB_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_AWB_END													AFE_AWB_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Name	Description
31:3	AFE_AWB_END	**End address of AWB input in master mode** Always set AFE_AWB_END[2:0] = 3'h7 for the convenience of the hardware implementation.
2:0	AFE_AWB_END_LSB	

1122007C AFE_AWB_CUR AFE AWB Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_AWB_CUR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_AWB_CUR															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AFE_AWB_CUR	Indicates the current address of the AWB input buffer

11220080 AFE_VUL_BASE AFE VUL Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_VUL_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_VUL_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	AFE_VUL_BASE	**Base address of VUL input in master mode** Always set AFE_VUL_BASE[2:0] = 3'h0 for the convenience of the hardware implementation.

11220088 AFE_VUL_END AFE VUL End Address Register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_VUL_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_VUL_END													AFE_VUL_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Name	Description
31:3	AFE_VUL_END	**End address of VUL input in master mode** Always set AFE_VUL_END[2:0] = 3'h7 for the convenience of the hardware implementation.
2:0	AFE_VUL_END_LSB	

1122008C AFE_VUL_CUR AFE VUL Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_VUL_CUR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_VUL_CUR															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AFE_VUL_CUR	**Indicates the current address of the VUL input buffer**

11220090 AFE_DAI_BASE AFE DAI Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DAI_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DAI_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	AFE_DAI_BASE	**Base address of DAI input in master mode** Always set AFE_DAI_BASE[2:0] = 3'h0 for the convenience of the hardware implementation.

1122009C AFE_DAI_CUR AFE DAI Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DAI_CUR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DAI_CUR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AFE_DAI_CUR	Indicates the current address of the DAI input buffer

11220098 AFE_DAI_END AFE_DAI_END 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DAI_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DAI_END													AFE_DAI_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Name	Description
31:3	AFE_DAI_END	**End address of DAI input in master mode** Always set AFE_DAI_END[2:0] = 3'h7 for the convenience of the hardware implementation.
2:0	AFE_DAI_END_LSB	

112200CC AFE_MEMIF_MSB **AFE Memory Interface MSB Register** **003F0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CPU_COMPACT_MODE	CPU_HD_ALIGN	VUL_data2_AXI_WR_SIGN	VUL_AXI_WR_SIGN	DAI_AXI_WR_SIGN	MOD_DAI_AXI_WR_SIGN	AWB_MSTR_SIGN	SYSRAM_SIGN
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DL3_MSB	Reserved 1	Reserved	HDMI_MSB	VUL_data2_MSB	VUL_MSB	DAI_MSB	MOD_DAI_MSB	AWB_MSB	DL1_data2_MSB	DL2_MSB	DL1_MSB
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23	CPU_COMPACT_MODE	**Selects valid 24-bit data from 32-bit write data bus** 0: 24bit use normal mode 1: 24bit use compact mode
22	CPU_HD_ALIGN	**Selects valid 24-bit data from 32-bit write data bus** 0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}
21	VUL_data2_AXI_WR_SIGN	**Signed extension 24-bit data to 32-bit for VUL_data2 memory agent** 0: append 0 1: bit[23] signed extension
20	VUL_AXI_WR_SIGN	**Signed extension 24-bit data to 32-bit for VUL memory agent** 0: append 0 1: bit[23] signed extension
19	DAI_AXI_WR_SIGN	**Signed extension 24-bit data to 32-bit for DAI memory agent** 0: append 0 1: bit[23] signed extension
18	MOD_DAI_AXI_WR_SIGN	**Signed extension 24-bit data to 32-bit for MOD_DAI memory agent** 0: append 0 1: bit[23] signed extension
17	AWB_MSTR_SIGN	**Signed extension 24-bit data to 32-bit for AWB memory agent** 0: append 0 1: bit[23] signed extension
16	SYSRAM_SIGN	**Signed extension 24-bit data to 32-bit for bus read SYSRAM** 0: append 0 1: bit[23] signed extension

Bit(s)	Name	Description
11	DL3_MSB	**Indicates MSB (bit 33) of DL3 memory address**
10	Reserved1	**Indicates MSB (bit 33) of SPDIF2 memory address**
9	Reserved	**Indicates MSB (bit 33) of SPDIF memory address**
8	HDMI_MSB	**Indicates MSB (bit 33) of HDMI memory address**
7	VUL_data2_MSB	**Indicates MSB (bit 33) of VUL_data2 memory address**
6	VUL_MSB	**Indicates MSB (bit 33) of VUL memory address**
5	DAI_MSB	**Indicates MSB (bit 33) of DAI memory address**
4	MOD_DAI_MSB	**Indicates MSB (bit 33) of MOD_DAI memory address**
3	AWB_MSB	**Indicates MSB (bit 33) of AWB memory address**
2	DL1_data2_MSB	**Indicates MSB (bit 33) of DL1_2 memory address**
1	DL2_MSB	**Indicates MSB (bit 33) of DL2 memory address**
0	DL1_MSB	**Indicates MSB (bit 33) of DL1 memory address**

112200D0 AFE_MEMIF_MON0 — AFE Memory Interface Monitor Register 0 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DL1_RCH_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DL1_LCH_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DL1_RCH_DATA	Memory interface DL1 right channel data output
15:0	DL1_LCH_DATA	Memory interface DL1 left channel data output

112200D4 AFE_MEMIF_MON1 — AFE Memory Interface Monitor Register 1 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DL2_RCH_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DL2_LCH_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DL2_RCH_DATA	Memory interface DL2 right channel data output
15:0	DL2_LCH_DATA	Memory interface DL2 left channel data output

112200D8 AFE_MEMIF_MON2 — AFE Memory Interface Monitor Register 2 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VUL_RCH_DATA															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAI_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	VUL_RCH_DATA	Memory interface VUL right channel data input
15:0	DAI_DATA	Memory interface DAI data input

112200E0 AFE_MEMIF_MON4 **AFE Memory Interface Monitor Register 4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AWB_RCH_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AWB_LCH_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	AWB_RCH_DATA	Memory interface AWB right channel data input
15:0	AWB_LCH_DATA	Memory interface AWB left channel data input

112201D0 AFE_SIDETONE_DEBUG **Side-Tone Debug** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													STF_PRETEND_AS_I5I6_DL1	STF_SRC_SEL		
Type													RW	RW		
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SLT_CNT_FLAG_RESET		SLT_CNT_THD										
Type				RW		RW										
Reset				0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	STF_PRETEND_AS_I5I6_DL1	**STF output to I_05/I_06 for debugging** 0: Normal I_05/I_06 function 1: STF output pretends as I_05/I_06 sources
18:16	STF_SRC_SEL	**Selects STF input source** 1: Sine generator 2: DL1 L and R from memory

Bit(s)	Name	Description
		3: I_03/I_04 (ADC I2S IN) 4: I_17/I_48 (ADC I2S IN 2) Others: From ADDA VUL channel out
12	SLT_CNT_FLAG_RESET	**Resets SLT_CNT_FLAG when SLT_CNT < SLT_CNT_THD** 0: Does not reset slt_cnt_flag 1: Reset slt_cnt_flag
10:0	SLT_CNT_THD	**slt_cnt_thd threshold** STF state machine slt_cnt threshold

112201D4 AFE_SIDETONE_MON **Side-Tone Debug Monitor** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SLT_CNT_FLAG		SLT_CNT										
Type				RU		RU										
Reset				0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12	SLT_CNT_FLAG	**Resets SLT_CNT_FLAG when SLT_CNT > SLT_CNT_THD** 0: slt_cnt >= SLT_CNT_THD 1: slt_cnt < SLT_CNT_THD
10:0	SLT_CNT	**STF state machine slt_cnt counted by fixed 26MHz between 2 consecutive input timing**

112201E0 AFE_SIDETONE_CON0 **Side-Tone Control Port 0** **02000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		R_RDY	W_RDY				R_W_EN	R_W_SEL	SEL_CH2			SIDE_TONE_COEFFICIENT_ADDR				
Type		RU	RU				RW	RW	RW			RW				
Reset		0	0				1	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIDE_TONE_COEFFICIENT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	R_RDY	**Read ready** If it is different from the value recorded before you assign a read address, read out the side tone coefficient of address specified ahead. 0: Ready/not ready 1: Ready/not ready
29	W_RDY	**Write ready**

Bit(s)	Name	Description
		If it is different from the value recorded before the first written coefficient, write the "next" side tone coefficient. 0: Ready/not ready 1: Ready/not ready
25	R_W_EN	**Enables read/write** 0: Disable 1: Enable
24	R_W_SEL	**Reads or writes coefficients** 0: Read 1: Write
23	SEL_CH2	**Selects STF (side tone filter) input source** 0: Uplink I2S CH1 as STF input 1: Uplink i2s CH2 as STF input
20:16	SIDE_TONE_COEFFICIENT_ADDR	**Coefficient SRAM address access control** For example, if address 0x00 has coefficient 0x1234, this field should be filled 0x00 and [15:0] filled 0x1234.
15:0	SIDE_TONE_COEFFICIENT	**Coefficient of the side tone filter** 2's complement. The Q-format is 1.15.

112201E4 AFE_SIDETONE_COEFF **Side-Tone coefficient Port** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIDE_TONE_COEFF															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SIDE_TONE_COEFF	Reads out side tone coefficients

112201E8 AFE_SIDETONE_CON1 **Side-Tone Control Port 1** **0000001F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STF_BYPASS_MODE	STF_BYPASS_MODE_O28_O29														
Type	RW	RW														
Reset	0	0														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								SIDE_TONE_ON			SIDE_TONE_HALF_TAP_NUM					
Type								RW			RW					
Reset								0			0	1	1	1	1	1

Bit(s)	Name	Description
31	STF_BYPASS_MODE	**STF bypass mode** 0: Use STF result adding into I2S_OUT0 1: Bypass STF result
30	STF_BYPASS_MODE_O28_O29	**STF bypass mode** 0: Use STF result adding into I2S_OUT0 1: Bypass STF result
8	SIDE_TONE_ON	**STF enabling bit** 0: Disable STF 1: Enable STF
5:0	SIDE_TONE_HALF_TAP_NUM	**Number of half Nth taps for every symmetry.** Example: SIDE_TONE_HALF_TAP_NUM[5:0] = 13 if taps number used = 26.

112201EC AFE_SIDETONE_GAIN **Side-Tone Gain Port** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIDE_TONE_GAIN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SIDE_TONE_GAIN	**Gain of side tone filter** 2's complement. The Q-format is 1.15.

112201F0 AFE_SGEN_CON0 **AFE Sine-Wave Gen Config 0** **F0000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INNER_LOOP_BACK_MODE				IN_OUT_SEL	dac_en	mute_sw_ch2	mute_sw_ch1	sine_mode_ch2				amp_div_ch2			freq_div_ch2
Type	RW				RW	RW	RW	RW	RW				RW			RW
Reset	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	freq_div_ch2				sine_mode_ch1				amp_div_ch1				freq_div_ch1			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	INNER_LOOP_BACK_MODE	**Loopback mode testing for audio_conn** Valid if SINE_MODE_CH1 > 8 for sinewave gen ch1 and SINE_MODE_CH2 > 8 for sinewave gen ch2. 0: in_en[00], i_00, i_01 use sin_ch1 and sin_ch2 as input source (when bit[27] is set to 1'b0) 1: in_en[02], i_02 use sin_ch1 input source 2: in_en[03], i_03, i_04 use sin_ch1 and sin_ch2 as input source 3: in_en[05], i_05, i_06 use sin_ch1 and sin_ch2 as input

Bit(s)	Name	Description
		source (if 0x1d0[19]=0) 4: in_en[07], i_07, i_08 use sin_ch1 and sin_ch2 as input source 5: in_en[09], i_09 use sin_ch1 6: in_en[10], i_10, i_11 use sin_ch1 and sin_ch2 as input source 7: in_en[12], i_12, i_13 use sin_ch1 and sin_ch2 as input source 8: in_en[14], i_14 use sin_ch1 9: in_en[15], i_15, i_16 use sin_ch1 and sin_ch2 as input source 10: in_en[17], i_17, i_18 use sin_ch1 and sin_ch2 as input source 11: in_en[19], i_19, i_20 use sin_ch1 and sin_ch2 as input source 12: in_en[21], i_21, i_22 use sin_ch1 and sin_ch2 as input source 14: in_en[25], i_25, i_26 use sin_ch1 and sin_ch2 as input source 0: out_en[00], o_00, o_01 use sin_ch1 and sin_ch2 as input source (when bit[27] is set to 1'b0) 1: out_en[02], o_02 use sin_ch1 as input source 2: out_en[03], o_03, o_04 use sin_ch1 and sin_ch2 as input source 3: out_en[05], o_05, o_06 use sin_ch1 and sin_ch2 as input source 4: out_en[07], o_07, o_08 use sin_ch1 and sin_ch2 5: out_en[09], o_09, o_10 use sin_ch1 and sin_ch2 as input source 6: out_en[11], o_11 use sin_ch1 as input source 7: out_en[12], o_12 use sin_ch1 as input source 8: out_en[13], o_13, o_14 use sin_ch1 and sin_ch2 as input source 9: out_en[15], o_15, o_16 use sin_ch1 and sin_ch2 as input source 10: out_en[17], o_17, o_18 use sin_ch1 and sin_ch2 as input source 11: out_en[19], o_19, o_20 use sin_ch1 and sin_ch2 as input source 12: out_en[21], o_21, o_22 use sin_ch1 and sin_ch2 as input source 13: out_en[23], o_23, o_24 use sin_ch1 and sin_ch2 as input source 14: out_en[25], o_25 use sin_ch1 15: out_en[28], o_28, o_29 use sin_ch1 and sin_ch2 as input source
27	IN_OUT_SEL	**Selects sinewave to input/output** 0: To input 1: To output
26	dac_en	**Enables sinewave generator** 0: Disable sigen 1: Enable sigen
25	mute_sw_ch2	**Sinewave generator mute for ch2** 0: Unmute sigen 1: Mute sigen
24	mute_sw_ch1	**Sinewave generator mute for ch1** 0: Unmute sigen 1: Mute sigen
23:20	sine_mode_ch2	**Enables sinewave generator timing selection for ch2** 0: 8k

Bit(s)	Name	Description
		1: 11.025k 2: 12k 4: 16k 5: 22.05k 6: 24k 8: 32k 9: 44.1k 10: 48k 11: 88.2k 12: 96k 13: 176.4k 14: 192k
19:17	amp_div_ch2	**Selects sinewave generator amplitude for ch2** 0: sinewave_out/128 1: sinewave_out/64 2: sinewave_out/32 3: sinewave_out/16 4: sinewave_out/8 5: sinewave_out/4 6: sinewave_out/2 7: sinewave_out/1
16:12	freq_div_ch2	**Selects sinewave generator frequency for ch2 sampled by signal timing generator selection bit[23:20] (or bit[31:28]) for ch2** 0: DC output 1: 64/1 samples/period 2: 64/2 samples/period 3: 64/3 samples/period 4: 64/4 samples/period 5: 64/5 samples/period 6: 64/6 samples/period x: 64/x samples/period 31: 64/31 samples/period
11:8	sine_mode_ch1	**Enables sinewave generator timing selection for ch1** 0: 8k 1: 11.025k 2: 12k 4: 16k 5: 22.05k 6: 24k 8: 32k 9: 44.1k 10: 48k 11: 88.2k 12: 96k 13: 176.4k 14: 192k
7:5	amp_div_ch1	**Selects sinewave generator amplitude for ch1** 0: sinewave_out/128 1: sinewave_out/64 2: sinewave_out/32 3: sinewave_out/16 4: sinewave_out/8 5: sinewave_out/4 6: sinewave_out/2

Bit(s)	Name	Description
		7: sinewave_out/1
4:0	freq_div_ch1	**Selects sinewave generator frequency for ch2 sampled by signal timing generator selection bit[23:20] (or bit[31:28]) for ch1** 0: DC output 1: 64/1 samples/period 2: 64/2 samples/period 3: 64/3 samples/period 4: 64/4 samples/period 5: 64/5 samples/period 6: 64/6 samples/period x: 64/x samples/period 31: 64/31 samples/period

11220200 AFE_TOP_CON0 AFE Top Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LOOP_BACK_MODE															
Type	RW															
Reset	0	0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31:28	LOOP_BACK_MODE	**Specifies loop back mode** 0: Normal mode 1: Sine tone output of ch1 to i_05, sine tone output of ch2 to i_06 2: Sine tone output of ch1 to i_07, sine tone output of ch2 to i_08 4: Sine tone output of ch1 to src_B ch1, sine tone output of ch2 to src_B ch2 6: Uplink left channel output to src_B ch1, uplink right channel output to src_B ch2

11220330 AFE_MOD_DAI_BASE AFE MOD_DAI Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_MOD_DAI_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_MOD_DAI_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	AFE_MOD_DAI_BASE	**Base address of MOD_DAI input in master mode** Always set AFE_MOD_DAI_BASE[2:0] = 3'h0 for the convenience of the hardware implementation.

Bit(s)	Name	Description

11220338 AFE_MOD_DAI_END AFE_MOD_DAI_END 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_MOD_DAI_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_MOD_DAI_END													AFE_MOD_DAI_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Name	Description
31:3	AFE_MOD_DAI_END	**End address of MOD_DAI input in master mode** Always set AFE_MOD_DAI_END[2:0] = 3'h7 for the convenience of the hardware implementation.
2:0	AFE_MOD_DAI_END_LSB	

1122033C AFE_MOD_DAI_CUR AFE MOD_DAI Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_MOD_DAI_CUR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_MOD_DAI_CUR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AFE_MOD_DAI_CUR	Indicates the current address of MOD_DAI input buffer

11220350 AFE_VUL_D2_BASE AFE VUL_D2 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_VUL_D2_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_VUL_D2_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	AFE_VUL_D2_BASE	**Base address of VUL_D2 input in master mode** Always set AFE_VUL_D2_BASE[2:0] = 3'h0 for the convenience

Bit(s)	Name	Description
		of the hardware implementation.

11220358 AFE_VUL_D2_END AFE VUL_D2 End Address Register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_VUL_D2_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_VUL_D2_END													AFE_VUL_D2_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Name	Description
31:3	AFE_VUL_D2_END	**End address of the VUL_D2 input in master mode** Always set AFE_VUL_D2_END[2:0] = 3'h7 for the convenience of the hardware implementation.
2:0	AFE_VUL_D2_END_LSB	

1122035C AFE_VUL_D2_CUR AFE VUL_D2 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_VUL_D2_CUR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_VUL_D2_CUR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AFE_VUL_D2_CUR	Indicates the current address of the VUL_D2 input buffer

112203A0 AFE_IRQ_MCU_CON AFE IRQ MCU Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					IRQ7_MCU_MODE				IRQ4_MCU_MODE				IRQ3_MCU_MODE			
Type					RW				RW				RW			
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		IRQ7_MCU_ON			IRQ2_MCU_MODE				IRQ1_MCU_MODE				IRQ4_MCU_ON	IRQ3_MCU_ON	IRQ2_MCU_ON	IRQ1_MCU_ON
Type		RW			RW				RW				RW	RW	RW	RW
Reset		0			0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:24	IRQ7_MCU_MODE	**Controls the IRQ7_MCU count unit** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 0111b: 130k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k 0111b: 130k 1111b: 260k
23:20	IRQ4_MCU_MODE	**Controls the IRQ3_MCU count unit** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k 0111b: 130k 1111b: 260k
19:16	IRQ3_MCU_MODE	**Controls the IRQ4_MCU count unit** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k 0111b: 130k 1111b: 260k
14	IRQ7_MCU_ON	**Controls the enbling of IRQ7_MCU** 0: Off 1: On
11:8	IRQ2_MCU_MODE	**Controls the IRQ2_MCU count unit** 0000b: 8k 0001b: 11.025k

Bit(s)	Name	Description
		0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k 0111b: 130k 1111b: 260k
7:4	IRQ1_MCU_MODE	**Controls the IRQ1_MCU count unit** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k 0111b: 130k 1111b: 260k
3	IRQ4_MCU_ON	**Controls the enbling of IRQ4_MCU** 0: Off 1: On
2	IRQ3_MCU_ON	**Controls the enbling of IRQ3_MCU** 0: Off 1: On
1	IRQ2_MCU_ON	**Controls the enbling of IRQ2_MCU** 0: Off 1: On
0	IRQ1_MCU_ON	**Controls the enbling of IRQ1_MCU** 0: Off 1: On

112203A4 AFE_IRQ_MCU_STATUS **AFE IRQ MCU Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**IRQ7_MCU**		**IRQ5_MCU**	**IRQ4_MCU**	**IRQ3_MCU**	**IRQ2_MCU**	**IRQ1_MCU**
Type										RU		RU	RU	RU	RU	RU
Reset										0		0	0	0	0	0

Bit(s)	Name	Description
6	IRQ7_MCU	**Reads the status for IRQ7_MCU (I2S)** 0: No interrupt 1: IRQ7 interrupt
4	IRQ5_MCU	**Reads the status for IRQ5_MCU (TDM)** 0: No interrupt 1: IRQ5 interrupt
3	IRQ4_MCU	**Reads the status for IRQ4_MCU** 0: No interrupt 1: IRQ4 interrupt
2	IRQ3_MCU	**Reads the status for IRQ3_MCU** 0: No interrupt 1: IRQ3 interrupt
1	IRQ2_MCU	**Reads the status for IRQ2_MCU (I2S)** 0: No interrupt 1: IRQ2 interrupt
0	IRQ1_MCU	**Reads the status for IRQ1_MCU (VUL/DL1/DL2/AWB)** 0: No interrupt 1: IRQ1 interrupt

112203A8 AFE_IRQ_MCU_CLR AFE IRQ Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		IRQ7_MCU_MISS_CLR		IRQ5_MCU_MISS_CLR	IRQ4_MCU_MISS_CLR	IRQ3_MCU_MISS_CLR	IRQ2_MCU_MISS_CLR	IRQ1_MCU_MISS_CLR		IRQ7_MCU_CLR		IRQ5_MCU_CLR	IRQ4_MCU_CLR	IRQ3_MCU_CLR	IRQ2_MCU_CLR	IRQ1_MCU_CLR
Type		WO		WO	WO	WO	WO	WO		WO		WO	WO	WO	WO	WO
Reset		0		0	0	0	0	0		0		0	0	0	0	0

Bit(s)	Name	Description
14	IRQ7_MCU_MISS_CLR	**Clears the status of IRQ7 miss flag** 0: No operation 1: Clear IRQ7 miss flag
12	IRQ5_MCU_MISS_CLR	**Clears the status of IRQ5 miss flag** 0: No operation 1: Clear IRQ5 miss flag
11	IRQ4_MCU_MISS_CLR	**Clears the status of IRQ4 miss flag** 0: No operation 1: Clear IRQ4 miss flag
10	IRQ3_MCU_MISS_CLR	**Clears the status of IRQ3 miss flag** 0: No operation 1: Clear IRQ3 miss flag
9	IRQ2_MCU_MISS_CLR	**Clears the status of IRQ2 miss flag** 0: No operation 1: Clear IRQ2 miss flag
8	IRQ1_MCU_MISS_CLR	**Clears the status of IRQ1 miss flag** 0: No operation

Bit(s)	Name	Description
		1: Clear IRQ1 miss flag
6	IRQ7_MCU_CLR	**Clears the status for IRQ7_MCU.** 0: No operation 1: Clear IRQ7 Interrupt
4	IRQ5_MCU_CLR	**Clears the status for IRQ5_MCU.** 0: No operation 1: Clear IRQ5 interrupt
3	IRQ4_MCU_CLR	**Clears the status for IRQ4_MCU.** 0: No operation 1: Clear IRQ4 interrupt
2	IRQ3_MCU_CLR	**Clears the status for IRQ3_MCU.** 0: No operation 1: Clear IRQ3 interrupt
1	IRQ2_MCU_CLR	**Clears the status for IRQ2_MCU.** 0: No operation 1: Clear IRQ2 interrupt
0	IRQ1_MCU_CLR	**Clears the status for IRQ1_MCU.** 0: No operation 1: Clear IRQ1 interrupt

112203AC AFE_IRQ_MCU_CNT1 **AFE IRQ1 MCU Counter Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ_MCU_CNT1	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ_MCU_CNT1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:0	AFE_IRQ_MCU_CNT1	**Sets up the counter value for IRQ1 according to IRQ1_MODE** The IRQ1 counter in AFE will count down from AFE_IRQ_MCU_CNT1 and set up IRQ1 while IRQ1 counter reaches 1. Therefore, the maximum IRQ time for IRQ1 at 48kHz mode is 5s.

112203B0 AFE_IRQ_MCU_CNT2 **AFE IRQ2 MCU Counter Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ_MCU_CNT2	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ_MCU_CNT2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:0	AFE_IRQ_MCU_CNT2	**Sets up the counter value for IRQ2 according to IRQ2_MODE** The IRQ2 counter in AFE will count down from AFE_IRQ_MCU_CNT2 and set up IRQ2 while IRQ2 counter reaches 1. Therefore, the maximum IRQ time for IRQ2 at 48kHz mode is 5s.

112203B4 AFE_IRQ_MCU_EN AFE IRQ MCU Enable Register 00080473

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										AFE_IRQ_CM4_EN						
Type										RW						
Reset										0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		AFE_IRQ_MD32_EN								AFE_IRQ_MCU_EN						
Type		RW								RW						
Reset		0	0	0	0	1	0	0		1	1	1	0	0	1	1

Bit(s)	Name	Description
22:16	AFE_IRQ_CM4_EN	IRQ to CM4 enable control
14:8	AFE_IRQ_MD32_EN	IRQ to MD32 enable control
6:0	AFE_IRQ_MCU_EN	IRQ to MCU enable control

112203B8 AFE_IRQ_MCU_MON2 AFE IRQ MCU MON2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		IRQ7_MISS_FLAG		IRQ5_MISS_FLAG	IRQ4_MISS_FLAG	IRQ3_MISS_FLAG	IRQ2_MISS_FLAG	IRQ1_MISS_FLAG	AFE_IRQ_MCU_CLR_PHASE							
Type		RU		RU	RU	RU	RU	RU	RU							
Reset		0		0	0	0	0	0	0							

Bit(s)	Name	Description
14	IRQ7_MISS_FLAG	**Shows if there is any miss of the IRQ7** Writing 1 to 0x3a8[14] will clear this bit. 0: No miss 1: Miss happened.
12	IRQ5_MISS_FLAG	**Shows if there is any miss of the IRQ5** Writing 1 to 0x3a8[12] will clear this bit. 0: No miss 1: Miss happened.
11	IRQ4_MISS_FLAG	**Shows if there is any miss of the IRQ4**

Bit(s)	Name	Description
		Writing 1 to 0x3a8[11] will clear this bit. 0: No miss 1: Miss happened.
10	IRQ3_MISS_FLAG	**Shows if there is any miss of the IRQ3** Writing 1 to 0x3a8[10] will clear this bit. 0: No miss 1: Miss happened.
9	IRQ2_MISS_FLAG	**Shows if there is any miss of the IRQ2** Writing 1 to 0x3a8[9] will clear this bit. 0: No miss 1: Miss happened.
8	IRQ1_MISS_FLAG	**Shows if there is any miss of the IRQ1** Writing 1 to 0x3a8[8] will clear this bit. 0: No miss 1: Miss happened.
7	AFE_IRQ_MCU_CLR_PHASE	**For debuggingAFE_IRQ_MCU_CLR**

112203C0 AFE_IRQ1_MCU_CNT_MON AFE IRQ1 MCU Count Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ1_CNT_MON	
Type															RU	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ1_CNT_MON															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:0	AFE_IRQ1_CNT_MON	**Monitors the counter value for IRQ1 according toIRQ1_MODE** The IRQ1 counter in AFE will count down from AFE_IRQ_MCU_CNT1.

112203C4 AFE_IRQ2_MCU_CNT_MON AFE IRQ2 MCU Count Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ2_CNT_MON	
Type															RU	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ2_CNT_MON															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:0	AFE_IRQ2_CNT_MON	**Monitors the counter value for IRQ2 according toI2S_MODE** The IRQ1 counter in AFE will count down from

Bit(s)	Name	Description
		AFE_IRQ_MCU_CNT2.

112203C8 AFE_IRQ1_MCU_EN_CNT_MON — AFE IRQ1 MCU Enable Count Monitor Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_IRQ1_MCU_EN_CNT_MON															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ1_MCU_EN_CNT_MON															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AFE_IRQ1_MCU_EN_CNT_MON	Monitors the enable count number of IRQ1 enabling signal

112203D0 AFE_MEMIF_MINLEN — AFE MEMIF Min BLength Register — 33333333

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved2				HDMI_MINLEN				Reserved1				Reserved			
Type	RW				RW				RW				RW			
Reset	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DL3_MINLEN				DL2_MINLEN				DL1_data2_MINLEN				DL1_MINLEN			
Type	RW				RW				RW				RW			
Reset	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1

Bit(s)	Name	Description
31:28	Reserved2	The minimum burst length minus 1.
27:24	HDMI_MINLEN	The minimum burst length minus 1.
23:20	Reserved1	The minimum burst length minus 1.
19:16	Reserved	The minimum burst length minus 1.
15:12	DL3_MINLEN	The minimum burst length minus 1.
11:8	DL2_MINLEN	The minimum burst length minus 1.
7:4	DL1_data2_MINLEN	The minimum burst length minus 1.
3:0	DL1_MINLEN	The minimum burst length minus 1.

112203D4 AFE_MEMIF_MAXLEN — AFE MEMIF Max BLength Register — 11111115

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved				HDMI_MAXLEN				Reserved1							
Type	RW				RW				RW							
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved1				DL3_MAXLEN				DL2_MAXLEN				DL1_data2_MAXLEN		DL1_MAXLEN	
Type	RW				RW				RW				RW		RW	

Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	1	0	1

Bit(s)	Name	Description
31:28	Reserved	
27:24	HDMI_MAXLEN	0: Not support 1: 16 byte burst 2: 32 bytes burst 3: 64 bytes burst
23:12	Reserved1	
11:8	DL3_MAXLEN	0: Not support 1: 16 byte burst 2: 32 bytes burst 3: 64 bytes burst
7:4	DL2_MAXLEN	0: Not support 1: 16 byte burst 2: 32 bytes burst 3: 64 bytes burst
3:2	DL1_data2_MAXLEN	0: Not support 1: 16 byte burst 2: 32 bytes burst 3: 64 bytes burst
1:0	DL1_MAXLEN	0: Not support 1: 16 byte burst 2: 32 bytes burst 3: 64 bytes burst

112203D8 AFE_MEMIF_PBUF_SIZE **AFE MEMIF Prefecth Buffer Size** **00000FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved1														DL1_data2_4ch	VUL_data2_4ch
Type	RW														RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved				DL3_PBUF_SIZE		DL1_data2_PBUF_SIZE		IEC_PBUF_SIZE		HDMI_PBUF_SIZE		DL2_PBUF_SIZE		DL1_PBUF_SIZE	
Type	RW				RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:18	Reserved1	
17	DL1_data2_4ch	0: 2ch 1: 4ch
16	VUL_data2_4ch	0: 2ch 1: 4ch
15:12	Reserved	
11:10	DL3_PBUF_SIZE	00: 16 bytes 01: 32 bytes 10: 64 bytes 11: 128 bytes
9:8	DL1_data2_PBUF_SIZE	00: 16 bytes 01: 32 bytes

Bit(s)	Name	Description
		10: 64 bytes 11: 128 bytes
7:6	IEC_PBUF_SIZE	00: 16 bytes 01: 32 bytes 10: 64 bytes 11: 128 bytes
5:4	HDMI_PBUF_SIZE	00: 16 bytes 01: 32 bytes 10: 64 bytes 11: 128 bytes
3:2	DL2_PBUF_SIZE	00: 16 bytes 01: 32 bytes 10: 64 bytes 11: 128 bytes
1:0	DL1_PBUF_SIZE	00: 16 bytes 01: 32 bytes 10: 64 bytes 11: 128 bytes

112203F8 AFE_MEMIF_HD_MODE AFE MEMIF HD Mode Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved2								Reserved1		HDMI_HD		MOD_DAI_HD		DAI_HD	
Type	RW								RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved		VUL_data2_HD		VUL_HD		AWB_HD		DL3_HD		DL2_HD		DL1_data2_HD		DL1_HD	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Reserved2	
23:22	Reserved1	
21:20	HDMI_HD	0: 16 bits format 1: 24 bits format
19:18	MOD_DAI_HD	0: 16 bits format 1: 24 bits format
17:16	DAI_HD	0: 16 bits format 1: 24 bits format
15:14	Reserved	
13:12	VUL_data2_HD	0: 16 bits format 1: 24 bits format
11:10	VUL_HD	0: 16 bits format 1: 24 bits format
9:8	AWB_HD	0: 16 bits format 1: 24 bits format
7:6	DL3_HD	0: 16 bits format 1: 24 bits format
5:4	DL2_HD	0: 16 bits format 1: 24 bits format
3:2	DL1_data2_HD	0: 16 bits format 1: 24 bits format
1:0	DL1_HD	0: 16 bits format

Bit(s)	Name	Description
		1: 24 bits format

112203FC AFE_MEMIF_HDALIGN AFE MEMIF HD ALIGN Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved3					HDMI_NORMAL_MODE	MOD_DAI_NORMAL_MODE	DAI_NORMAL_MODE	Reserved2	VUL_data2_NORMAL_MODE	VUL_NORMAL_MODE	AWB_NORMAL_MODE	DL3_NORMAL_MODE	DL2_NORMAL_MODE	DL1_data2_NORMAL_MODE	DL1_NORMAL_MODE
Type	RW					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved1				Reserved	HDMI_HD_ALIGN	MOD_DAI_HD_ALIGN	DAI_ALIGN	VUL2_HD_ALIGN	VUL_data2_HD_ALIGN	VUL_HD_ALIGN	AWB_HD_ALIGN	DL3_HD_ALIGN	DL2_HD_ALIGN	DL1_data2_HD_ALIGN	DL1_HD_ALIGN
Type	RW				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:27	Reserved3	
26	HDMI_NORMAL_MODE	0: 24-bit uses compact mode. 1: 24-bit uses normal mode.
25	MOD_DAI_NORMAL_MODE	0: 24-bit uses compact mode. 1: 24-bit uses normal mode.
24	DAI_NORMAL_MODE	0: 24-bit uses compact mode. 1: 24-bit uses normal mode.
23	Reserved2	0: 24-bit uses compact mode. 1: 24-bit uses normal mode.
22	VUL_data2_NORMAL_MODE	0: 24-bit uses compact mode. 1: 24-bit uses normal mode.
21	VUL_NORMAL_MODE	0: 24-bit uses compact mode. 1: 24-bit uses normal mode.
20	AWB_NORMAL_MODE	0: 24-bit uses compact mode. 1: 24-bit uses normal mode.
19	DL3_NORMAL_MODE	0: 24-bit uses compact mode. 1: 24-bit uses normal mode.
18	DL2_NORMAL_MODE	0: 24-bit uses compact mode. 1: 24-bit uses normal mode.
17	DL1_data2_NORMAL_MODE	0: 24-bit uses compact mode. 1: 24-bit uses normal mode.
16	DL1_NORMAL_MODE	0: 24-bit uses compact mode. 1: 24-bit uses normal mode.
15:12	Reserved1	
11	Reserved	
10	HDMI_HD_ALIGN	0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}
9	MOD_DAI_HD_ALIGN	0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}
8	DAI_ALIGN	0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}
7	VUL2_HD_ALIGN	0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}

Bit(s)	Name	Description
6	VUL_data2_HD_ALIGN	0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}
5	VUL_HD_ALIGN	0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}
4	AWB_HD_ALIGN	0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}
3	DL3_HD_ALIGN	0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}
2	DL2_HD_ALIGN	0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}
1	DL1_data2_HD_ALIGN	0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}
0	DL1_HD_ALIGN	0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}

112203DC AFE_IRQ_MCU_CNT7 **AFE IRQ7 MCU Counter Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ_MCU_CNT7	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ_MCU_CNT7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:0	AFE_IRQ_MCU_CNT7	**Sets up the counter value for IRQ7 according to IRQ7_MODE** The IRQ7 counter in AFE will count down from AFE_IRQ_MCU_CNT7 and set up IRQ7 while IRQ7 counter reaches 1.

112203F0 AFE_APLL1_TUNER_CFG **AFE Tuner Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	upper_bound								apll_div					xtal_en_128fs_sel		freq_tuner_en
Type	RW								RW					RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
15:8	upper_bound	**Upper bound setting for changing PCW**
7:4	apll_div	**Divider setting of apll 128fs**

Bit(s)	Name	Description
2:1	xtal_en_128fs_sel	2'b00: 32kHz*128 2'b01: 44.1kHz*128 2'b10: 48kHz*128 2'b11: 0
0	freq_tuner_en	1: Enable apll tuner

112203F4 AFE_APLL2_TUNER_CFG **AFE Tuner 2 Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	upper_bound								apll_div					xtal_en_128fs_sel		freq_tuner_en
Type	RW								RW					RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
15:8	upper_bound	**Upper bound setting for changing PCW**
7:4	apll_div	**Divider setting of apll 128fs**
2:1	xtal_en_128fs_sel	2'b00: 32kHz*128 2'b01: 44.1kHz*128 2'b10: 48kHz*128 2'b11: 0
0	freq_tuner_en	1: Enable apll tuner

11220410 AFE_GAIN1_CON0 **AFE Gain 1 Control Register 0** **0000C800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN1_SAMPLE_PER_STEP								GAIN1_MODE							GAIN1_ON
Type	RW								RW							RW
Reset	1	1	0	0	1	0	0	0	0	0	0	0				0

Bit(s)	Name	Description
15:8	GAIN1_SAMPLE_PER_STEP	**Gain 1 sample per step**
7:4	GAIN1_MODE	**Gain 1 mode** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k

Bit(s)	Name	Description
		1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k
0	GAIN1_ON	**Gain 1 on** 0: Off 1: On

11220414 AFE_GAIN1_CON1 AFE Gain 1 Control Register 1 00080000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GAIN1_TARGET			
Type													RW			
Reset													1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN1_TARGET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	GAIN1_TARGET	Gain 1 target

11220418 AFE_GAIN1_CON2 AFE Gain 1 Control Register 2 0007C5E5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GAIN1_DOWN_STEP			
Type													RW			
Reset													0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN1_DOWN_STEP															
Type	RW															
Reset	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1

Bit(s)	Name	Description
19:0	GAIN1_DOWN_STEP	Gain 1 down step

1122041C AFE_GAIN1_CON3 AFE Gain 1 Control Register 3 00083BCD

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GAIN1_UP_STEP			
Type													RW			
Reset													1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	GAIN1_UP_STEP															
Type	RW															
Reset	0	0	1	1	1	0	1	1	1	1	0	0	1	1	0	1

Bit(s)	Name	Description
19:0	GAIN1_UP_STEP	Gain 1 up step

11220424 AFE_GAIN1_CUR AFE Gain 1 Cursor Register 00080000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													AFE_GAIN1_CUR			
Type													RW			
Reset													1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_GAIN1_CUR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	AFE_GAIN1_CUR	Indicates the current Gain 1

11220428 AFE_GAIN2_CON0 AFE Gain 2 Control Register 0 0000C800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN2_SAMPLE_PER_STEP								GAIN2_MODE							GAIN2_ON
Type	RW								RW							RW
Reset	1	1	0	0	1	0	0	0	0	0	0	0				0

Bit(s)	Name	Description
15:8	GAIN2_SAMPLE_PER_STEP	**Gain 2 sample per step**
7:4	GAIN2_MODE	**Gain 2 mode** 0000b: 8k 0001b: 11.025k 0010b: 12k 0100b: 16k 0101b: 22.05k 0110b: 24k 1000b: 32k 1001b: 44.1k 1010b: 48k 1011b: 88.2k 1100b: 96k 1101b: 176.4k 1110b: 192k
0	GAIN2_ON	**Gain 2 on**

Bit(s)	Name	Description
		0: Off 1: On

1122042C AFE_GAIN2_CON1 AFE Gain 2 Control Register 1 00080000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GAIN2_TARGET			
Type													RW			
Reset													1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN2_TARGET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	GAIN2_TARGET	Gain 2 target

11220430 AFE_GAIN2_CON2 AFE Gain 2 Control Register 2 0007C5E5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GAIN2_DOWN_STEP			
Type													RW			
Reset													0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN2_DOWN_STEP															
Type	RW															
Reset	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1

Bit(s)	Name	Description
19:0	GAIN2_DOWN_STEP	Gain 2 down step

11220434 AFE_GAIN2_CON3 AFE Gain 2 Control Register 3 00083BCD

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GAIN2_UP_STEP			
Type													RW			
Reset													1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN2_UP_STEP															
Type	RW															
Reset	0	0	1	1	1	0	1	1	1	1	0	0	1	1	0	1

Bit(s)	Name	Description
19:0	GAIN2_UP_STEP	Gain 2 up step

1122043C AFE_GAIN2_CUR — AFE Gain 2 Cursor Register — 00080000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													AFE_GAIN2_CUR			
Type													RW			
Reset													1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_GAIN2_CUR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	AFE_GAIN2_CUR	Indicates the current Gain 2

11220500 AFE_ASRC_CON0 — ASRC Config 0 — 80080000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHSET1_O16BIT		CHSET1_CLR_IIR_HISTORY	CHSET1_IS_MONO	CHSET1_OFS_SEL		CHSET1_IFS_SEL		CHSET1_IIR_EN	CHSET1_IIR_STAGE			CHSET0_O16BIT		CHSET0_CLR_IIR_HISTORY	CHSET0_IS_MONO
Type	RW		RW	RW	RW		RW		RW	RW			RW		RW	RW
Reset	1		0	0	0	0	0	0	0	0	0	0	1		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHSET0_OFS_SEL		CHSET0_IFS_SEL		CHSET0_IIR_EN	CHSET0_IIR_STAGE				CHSET_STR_CLR			CHSET_ON		COEFF_SRAM_CTRL	ASM_ON
Type	RW		RW		RW	RW				RW			RU		RW	RW
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	CHSET1_O16BIT	**Selects 16-bit/24-bit output**
29	CHSET1_CLR_IIR_HISTORY	**Set to 1 to clear the current IIR output history buffer for RX.** This register will auto-clear once the histories are cleared.
28	CHSET1_IS_MONO	**Mono/Stereo selection register**
27:26	CHSET1_OFS_SEL	**Selects output sample rate for RX** Set to 01 for OFS fix value.
25:24	CHSET1_IFS_SEL	**Selects input sample rate for RX** Set to 10 for frequency tracking mode.
23	CHSET1_IIR_EN	**Enables anti-alias IIR filter for RX** Set 1 to Turns on anti-alias IIR filter.
22:20	CHSET1_IIR_STAGE	**Anti-alias IIR filter stage for RX** Defines how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 orders are supported.
19	CHSET0_O16BIT	**Selects 16-bit/24-bit output**
17	CHSET0_CLR_IIR_HISTORY	**Set to 1 to clear current IIR output history buffer for TX.** This register will auto-clear once the histories are cleared.
16	CHSET0_IS_MONO	**Mono/Stereo selection register**
15:14	CHSET0_OFS_SEL	**Selects output sample rate for TX**

Bit(s)	Name	Description
		Set to 00 for OFS fix value.
13:12	CHSET0_IFS_SEL	**Selects input sample rate selection for TX** Set to 11 for period tracking mode.
11	CHSET0_IIR_EN	**Enables anti-alias IIR filter for TX** Set 1 to Turns on anti-alias IIR filter.
10:8	CHSET0_IIR_STAGE	**Anti-alias IIR filter stage for TX** Defines how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 orders are supported.
6:4	CHSET_STR_CLR	**Each channel set clear signal** Set bit 0 to 1 to clear the TX history. Set bit 1 to 1 to clear the RX history. Set bit 2 to 1 to clear the I2S history.
3:2	CHSET_ON	**Indicates which channel set is on currently** 01: TX 10: RX
1	COEFF_SRAM_CTRL	**Controls coefficient SRAM access** 0: Disable access 1: Enable access
0	ASM_ON	**ASRC enabling signal** Turn it on after all Configurations are set. 0: Disable ASRC 1: Enable ASRC

11220504 AFE_ASRC_CON1 **ASRC Config 1** **00000CB2**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_0							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_0															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Name	Description
23:0	ASM_FREQ_0	**Frequency palette** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX OFS.

11220508 AFE_ASRC_CON2 **ASRC Config 2** **00400000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_1							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	ASM_FREQ_1	**Frequency palette** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX OFS.

1122050C AFE_ASRC_CON3 **ASRC Config 3** **00400000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_2							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	ASM_FREQ_2	**Frequency palette** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX IFS.

11220510 AFE_ASRC_CON4 **ASRC Config 4** **00000CB2**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_3							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_3															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Name	Description
23:0	ASM_FREQ_3	**Frequency palette** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX IFS.

11220514 AFE_ASRC_CON5 **ASRC Config 5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RESULT_SEL		

Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	RESULT_SEL	**Selects output** 000: ASRC output 001: Data input 010: CMPF output 011: HBF1 output 100: HBF2 output 101: HBF3 output 110: HBF4 output 111: Each IIR stage output in order

11220518 AFE_ASRC_CON6 ASRC Config 6 00010800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FREQ_CALI_CYCLE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			FREQ_CALC_RUNNING	AUTO_TUNE_FREQ3	COMP_FREQ_RES_EN		FREQ_CALI_SEL		FREQ_CALI_BP_DGL	FREQ_CALI_MAX_GWIDTH			AUTO_TUNE_FREQ2	FREQ_CALI_AUTO_RESTART	CALI_USE_FREQ_OUT	CALI_EN
Type			RU	RW	RW		RW		RW	RW			RW	RW	RW	RU
Reset			0	0	1		0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	FREQ_CALI_CYCLE	**Frequency calibrating cycle register** Defines how many input signal cycles the calibrator calibrates are in one round. This register is updated into calibrator once the calibrator enable [0] is turned on.
13	FREQ_CALC_RUNNING	**Shows if frequency calculation is running** For one round running case, wait for this bit and the CALI_EN bit to become low before frequency result is ready.
12	AUTO_TUNE_FREQ3	**Enables asm_freq_3 auto update with the calibrator result once the calibrator completes one round** 0: Disable auto update 1: Enable auto update
11	COMP_FREQ_RES_EN	**Frequency compensation enabling register** 0: Disable compensation 1: Enable compensation
9:8	FREQ_CALI_SEL	**Calibrator input source selection register** Before modifying this register, make sure the calibrator is turned off. 00: Use PCM SYNC word 01: Not connected 10: Not connected 11: Not connected
7	FREQ_CALI_BP_DGL	**Bypasses deglitch circuit for calibrator input** 0: No bypass 1: Bypass

Bit(s)	Name	Description
6:4	FREQ_CALI_MAX_GWIDTH	**Defines the maximum glitch width of the calibrator input signal** Unit: Calibrator reference clock cycles
3	AUTO_TUNE_FREQ2	**Enables asm_freq_2 auto update with the calibrator result once the calibrator completes one round** 0: Disable auto update 1: Enable auto update
2	FREQ_CALI_AUTO_RESTART	**Enables calibrator auto restart new calibration while one run is completed** This value will be updated into calibrator once the enabling signal is turned on from off state. 0: Disable auto restart 1: Enable auto restart
1	CALI_USE_FREQ_OUT	**Selects frequency or period calibration mode** 0: Use period calibration result to update asm_freq_2. Use frequency calibration result to update asm_freq_3 1: Use frequency calibration result to update asm_freq_2. Use period calibration result to update asm_freq_3
0	CALI_EN	**Enables frequency calibrator** If auto restart is 0, this bit will be cleared while one calibration run is completed. If this bit is set to 0, wait until this bit becomes 0 to make the next run start safely. 0: Disable calibrator 1: Enable calibrator

1122051C AFE_ASRC_CON7 ASRC Config 7 00000659

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALC_DENOMINATOR							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALC_DENOMINATOR															
Type	RW															
Reset	0	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1

Bit(s)	Name	Description
23:0	FREQ_CALC_DENOMINATOR	Determines the denominator for performing period-to-frequency calibration result translation

11220520 AFE_ASRC_CON8 ASRC Config 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PRD_CALI_RESULT_RECORD							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRD_CALI_RESULT_RECORD															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	PRD_CALI_RESULT_RECORD	**Period calibration result** Records the calibration result of the previous round. Writing any value to this register will clear the result.

11220524 AFE_ASRC_CON9 ASRC Config 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_RESULT							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_RESULT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	FREQ_CALI_RESULT	**Frequency calibrator result** Records the calibration result of previous round. This value is got from the quotient of (FREQ_CALC_DENOMINATOR/PRD_CALI_RESULT) in 1.23 format.

11220528 AFE_ASRC_CON10 ASRC Config 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									COEFF_SRAM_DATA							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COEFF_SRAM_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	COEFF_SRAM_DATA	**Read/Write data port of coefficient SRAM** Read data have one cycle delay. The coefficients are filled stage by stage: each stage has 6 coefficients. For the 2nd-order IIR filter with transfer function of one stage as: "(2^shift)*a0 + (2^shift)*a1*Z^-1 + (2^shift)*a2*Z^-2/1 + (2^shift)*b1*Z^ -1 + (2^shift)*b2*Z^-2" The coefficient should be filled as (from low address to high address) a2 a1 a0 -b1 -b2 shift

1122052C AFE_ASRC_CON11 ASRC Config 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										COEFF_SRAM_ADR						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	COEFF_SRAM_ADR	**Determines the rd/wr address of IIR coefficient SRAM** Read/Write COEFF_SRAM_DATA will make this register increase by 1.

11220530 PCM_INTF_CON1 PCM Interface Config 1 00000006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIX_VALUE_SEL	BUFFER_LOOPBACK	PARALLEL_LOOPBACK	SERIAL_LOOPBACK	DAI_PCM_LOOPBACK	I2S_PCM_LOOPBACK	SYNC_DELSEL	TX_LR_SWAP	SYNC_OUT_INV	BCLK_OUT_INV	SYNC_IN_INV	BCLK_IN_INV	TX_LCH_RPT	VBT_16K_MODE	EXT_MODEM	PCM_24BIT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PCM_WLEN		SYNC_LENGTH					SYNC_TYPE	BT_MODE	BYP_ASRC	PCM_SLAVE	PCM_MODE		PCM_FMT		PCM_EN
Type	RW		RW					RW	RW	RW	RW	RW		RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bit(s)	Name	Description
31	FIX_VALUE_SEL	**Selects fix register value sent on PCM TX** Fix register value is from 0x0538. 0: Disable fix value on TX 1: Enable fix value on TX
30	BUFFER_LOOPBACK	**PCM RX parallel data in async FIFO are loopback to PCM TX async FIFO** 2-channel TX data receive the same 1-channel RX data. 0: Disable loopback 1: Enable loopback
29	PARALLEL_LOOPBACK	**PCM RX parallel data are looped back to PCM TX directly.** 2-channel TX data receive the same 1-channel RX data. 0: Disable loopback 1: Enable loopback
28	SERIAL_LOOPBACK	**PCM RX serial data are loopback to PCM TX directly** 0: Disable loopback 1: Enable loopback
27	DAI_PCM_LOOPBACK	**Internal loopback with AFE_DAIBT module** 0: Disable loopback 1: Enable loopback
26	I2S_PCM_LOOPBACK	**Internal loopback with AFE_I2S module** 0: Disable loopback 1: Enable loopback
25	SYNC_DELSEL	**Selects synchronizer** 0: Select 2 FFs synchronizer

Bit(s)	Name	Description
		1: Select 1 FF synchronizer
24	TX_LR_SWAP	**TX L/R channels swap** 0: Disable swap 1: Enable swap
23	SYNC_OUT_INV	**Inverts PCM SYNC out** 0: Not invert 1: Invert
22	BCLK_OUT_INV	**Inverts PCM BCLK out** 0: Not invert 1: Invert
21	SYNC_IN_INV	**Inverts PCM SYNC in** 0: Not invert 1: Invert
20	BCLK_IN_INV	**Inverts PCM BCLK in** 0: Not invert 1: Invert
19	TX_LCH_RPT	**TX L-channel repeat twice in one sample period** 0: No repeat 1: Repeat
18	VBT_16K_MODE	**Mode support for 2 samples in once sync** Used in 16K mode only. 0: Disable 1: Enable
17	EXT_MODEM	**Selects internal/external modem PCM interface** 0: Select internal modem 1: Select external modem
16	PCM_24BIT	**Selects data sample bit width** 0: 16-bit sample 1: 24-bit sample
15:14	PCM_WLEN	**Selects BCK cycles in one LRCK period** 00: 32 BCK 01: 64 BCK
13:9	SYNC_LENGTH	**PCM mode B sync length** SYNC_TYPE must be set to 1 to enable extended sync length. 00000: Sync is 1 BCK cycle 00001: Sync is 2 BCK cycles 00010: Sync is 3 BCK cycles 11111: Sync is 32 BCK cycles
8	SYNC_TYPE	**PCM mode B single BCK cycle sync length or multiple BCK cycles sync length** 0: 1 BCK cycle sync length 1: Extended BCK cycles sync length
7	BT_MODE	**In BT mode, only L channel data are sent on PCM TX.** 0: Dual mic on TX 1: Single mic on TX
6	BYP_ASRC	**Set to 0 when source and destination use different crystals.** Set to 1 when the source and destination use same crystal. 0: TX/RX parallel data go through ASRC 1: TX/RX parallel data go through async FIFO
5	PCM_SLAVE	**Selects master/slave mode** 0: Master mode 1: Slave mode
4:3	PCM_MODE	**Selects sampling rate** 00: 8K 01: 16K 10: 32K

Bit(s)	Name	Description
2:1	PCM_FMT	**PCM interface formats** 00: I2S 01: EIAJ 10: PCM mode A 11: PCM mode B
0	PCM_EN	**Enables PCM interface** 0: Disable PCM interface 1: Enable PCM interface

11220538 PCM_INTF_CON2 PCM Interface Config 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PCM1_TX_FIFO_OV	PCM1_RX_FIFO_OV	PCM2_TX_FIFO_OV	PCM2_RX_FIFO_OV	PCM1_SYNC_GLITCH	PCM2_SYNC_GLITCH										
Type	RU	RU	RU	RU	RU	RU										
Reset	0	0	0	0	0	0										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PCM1_PCM2_LOOPBACK		DAI_PCM_LOOPBACK_CH	I2S_PCM_LOOPBACK_CH				PCM_USE_MD3	TX_FIX_VALUE							
Type	RU		RW	RU				RW	RW							
Reset	0		0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PCM1_TX_FIFO_OV	**PCM1 (master/slave PCM) TX async FIFO overflow/underflow flag**
30	PCM1_RX_FIFO_OV	**PCM1 (master/slave PCM) RX async FIFO overflow/underflow flag**
29	PCM2_TX_FIFO_OV	**PCM2 (slave only PCM) TX Async FIFO overflow/underflow flag**
28	PCM2_RX_FIFO_OV	**PCM2 (slave only PCM) RX Async FIFO overflow/underflow flag**
27	PCM1_SYNC_GLITCH	**PCM1 (master/slave PCM) sync glitch flag**
26	PCM2_SYNC_GLITCH	**PCM2 (slave only PCM) sync glitch flag**
15	PCM1_PCM2_LOOPBACK	**Internal loopback with AFE_PCM_SLV_INTF module** 0: Disable loopback 1: Enable loopback
13	DAI_PCM_LOOPBACK_CH	**Selects internal loopback signal with AFE_DAIBT module** 0: TX 1: TX2
12	I2S_PCM_LOOPBACK_CH	**Selects internal loopback signal with AFE_I2S module** 0: TX 1: TX2
8	PCM_USE_MD3	**Selects internal MD2/MD3 PCM interface** 0: Select internal MD2 1: Select internal MD3
7:0	TX_FIX_VALUE	**Fix register value sent on PCM TX**

1122053C PCM2_INTF_CON **PCM2 Interface Config** **00000006**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_FIX_VALUE								FIX_VALUE_SEL	BUFFER_LOOPBACK	PARALLEL_LOOPBACK	SERIAL_LOOPBACK	DAI_PCM_LOOPBACK	I2S_PCM_LOOPBACK	SYNC_DELSEL	TX_LR_SWAP
Type	RW								RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYNC_IN_INV	BCLK_IN_INV	TX_LCH_RPT	VBT_16K_MODE	LOOPBACK_CH_SEL			TX2_BT_MODE	BT_MODE	PCM_AFIFO	PCM_WLEN	PCM_MODE		PCM_FMT		PCM_EN
Type	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW		RW		RW
Reset	0	0	0	0	0	0		0	0	0	0	0	0	1	1	0

Bit(s)	Name	Description
31:24	TX_FIX_VALUE	**Fix register value sent on PCM TX**
23	FIX_VALUE_SEL	**Selects fix register value sent on PCM TX** Fix register value is from bit[31:24]. 0: Disable fix value on TX 1: Enable fix value on TX
22	BUFFER_LOOPBACK	**PCM RX parallel data in async FIFO are looped back to PCM TX async FIFO.** 2-channel TX data receive the same 1-channel RX data. 0: Disable loopback 1: Enable loopback
21	PARALLEL_LOOPBACK	**PCM RX parallel data are looped back to PCM TX directly.** 2-channels TX data receives same 1-channel RX data. 0: Disable loopback 1: Enable loopback
20	SERIAL_LOOPBACK	**PCM RX serial data are looped back to PCM TX directly.** 0: Disable loopback 1: Enable loopback
19	DAI_PCM_LOOPBACK	**Internal loopback with DAIBT module** 0: Disable loopback 1: Enable loopback
18	I2S_PCM_LOOPBACK	**Internal loopback with AFE_I2S module** 0: Disable loopback 1: Enable loopback
17	SYNC_DELSEL	**Selects synchronizer** 0: Select 2 FFs synchronizer 1: Select 1 FF synchronizer
16	TX_LR_SWAP	**Swaps TX L/R channels** 0: Disable swap 1: Enable swap
15	SYNC_IN_INV	**Inverts PCM SYNC in** 0: Not invert 1: Invert
14	BCLK_IN_INV	**Inverts PCM BCLK in** 0: Not invert 1: Invert
13	TX_LCH_RPT	**TX L-channel repeat twice in one sample period** 0: No repeat 1: Repeat
12	VBT_16K_MODE	**Mode support for 2 samples in once sync**

Bit(s)	Name	Description
		Used in 16K mode only. 0: Disable 1: Enable
11:10	LOOPBACK_CH_SEL	**Selects loopback channels for PCM2 to I2S or PCM2 to DAI loopback mode** 00: PCM2_TX for loopback 01: PCM2_TX2 for loopback 10: PCM2_TX3 for loopback
8	TX2_BT_MODE	**In BT mode, only L channel data are sent on PCM TX2.** 0: Dual mic on TX2 1: Single mic on TX2
7	BT_MODE	**In BT mode, only L channel data are sent on PCM TX.** 0: Dual mic on TX 1: Single mic on TX
6	PCM_AFIFO	**Select ASRC if modem is using different clock source.** Select AFIFO if modem is using same clock source. 0: ASRC 1: AFIFO
5	PCM_WLEN	**Selects BCK cycles in one LRCK period** 0: 32 BCK cycles 1: 64 BCK cycles
4:3	PCM_MODE	**Selects sampling rate** 00: 8K 01: 16K 10: 32K
2:1	PCM_FMT	**PCM interface formats** 00: I2S 01: EIAJ 10: PCM mode A 11: PCM mode B
0	PCM_EN	**Enables PCM interface** 0: Disable PCM interface 1: Enable PCM interface

11220550 AFE_ASRC_CON13 ASRC Config 13 00080000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CHSET2_O16BIT		CHSET2_CLR_IIR_HISTORY	CHSET2_IS_MONO
Type													RW		RW	RW
Reset													1		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CHSET2_IIR_EN	CHSET2_IIR_STAGE			CHSET_STR_CLR			CHSET_ON			COEFF_SRAM_CTRL	ASM_ON
Type					RW	RW			RU			RU			RU	RU
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	CHSET2_O16BIT	**Selects 16-bit/24-bit output**

Bit(s)	Name	Description
17	CHSET2_CLR_IIR_HISTORY	**Set to 1 to clear the current IIR output history buffer for RX.** This register will auto-clear once the histories are cleared.
16	CHSET2_IS_MONO	**Mono/Stereo selection register**
11	CHSET2_IIR_EN	**Enables anti-alias IIR filter for I2S IN** Set 1 to turn on anti-alias IIR filter.
10:8	CHSET2_IIR_STAGE	**Anti-alias IIR filter stage for I2S IN** Defines how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 orders are supported.
7:5	CHSET_STR_CLR	**Sets AFE_ASRC_CON0 to clear.** Read-only.
4:2	CHSET_ON	**Indicates which channel set is on currently** 000: PCM TX 010: PCM TX 100: I2S RX
1	COEFF_SRAM_CTRL	**Coefficient SRAM access control** 0: Disable access 1: Enable access
0	ASM_ON	**ASRC enabling signal** Turned on after all Configurations are set. 0: ASRC disable 1: ASRC enable

11220554 AFE_ASRC_CON14 ASRC Config 14 00600000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_4							
Type									RW							
Reset									0	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	ASM_FREQ_4	**Frequency palette** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for I2S RX OFS. 48K: 3250/[(26M/48K)*8] = 0x600000 44.1K: 8125/[(26M/44.1K)*8] = 0xDC8000

11220558 AFE_ASRC_CON15 ASRC Config 15 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_5							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_5															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	ASM_FREQ_5	**Frequency palette** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for I2S RX IFS. 48K: 3250/[(26M/32K)*8] = 0x400000 44.1K: 8125/[(26M/32K)*8] = 0xA00000

1122055C AFE_ASRC_CON16 ASRC Config 16 00010800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FREQ_CALI2_CYCLE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		FREQ_CALI2_AUTORST_EN	FREQ_CALC2_RUNNING	AUTO_TUNE_FREQ4	COMP_FREQ_RES_EN2		FREQ_CALI2_SEL		FREQ_CALI2_BP_DGL	FREQ_CALI2_MAX_GWIDTH			AUTO_TUNE_FREQ5	FREQ_CALI2_AUTO_RESTART	CALI2_USE_FREQ_OUT	CALI2_EN
Type		RW	RU	RW	RW		RW		RW	RW			RW	RW	RW	RW
Reset		0	0	0	1		0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	FREQ_CALI2_CYCLE	**Frequency calibrating 2 cycle Register** Defines how many input signal cycles the calibrator calibrates in one round. This register is updated into calibrator once the calibrator enable [0] is turned on. In OFS 48K or 44.1K, set to 7.
14	FREQ_CALI2_AUTORST_EN	**Enables freq_cali2 auto reset with the calibrator result too large (slow I2S in when FM change)** For I2S in, set it to 1. 0: Disable auto reset 1: Enable auto reset
13	FREQ_CALC2_RUNNING	**Shows if frequency calculation 2 is running** For one round running case, wait for this bit and CALI_EN bit become low before frequency result is ready.
12	AUTO_TUNE_FREQ4	**Enables asm_freq_4 auto update with the calibrator result once the calibrato complete one round** For I2S in, set it to 0. 0: Disable auto update 1: Enable auto update
11	COMP_FREQ_RES_EN2	**Frequency compensation 2 enabling register** 0: Disable compensation 1: Enable compensation
9:8	FREQ_CALI2_SEL	**Calibrator 2 input source selection register** Before modifying this register, make sure the calibrator is turned off. For I2S in, set it to 2'b01. 00: Use PCM SYNC word 01: Not connected 10: Not connected 11: Not connected
7	FREQ_CALI2_BP_DGL	**Bypasses deglitch circuit for calibrator 2 input**

Bit(s)	Name	Description
		0: No bypass 1: Bypass
6:4	FREQ_CALI2_MAX_GWIDTH	**Defines maximum glitch width of the calibrator 2 input signal** Unit: Calibrator reference clock cycles
3	AUTO_TUNE_FREQ5	**Enables asm_freq_5 auto update with the calibrator result once the calibrato complete one round** For I2S in, set it to 1. 0: Disable auto update 1: Enable auto update
2	FREQ_CALI2_AUTO_RESTART	**Enables calibrator 2 auto restart new calibration while one run completes** This value will be updated into calibrator once the enabling signal is turned on from off state. 0: Disable atuo restart 1: Enable auto restart
1	CALI2_USE_FREQ_OUT	**Selects frequency or period calibration mode** For I2S in, set it to 1. 0: Use period calibration result to update asm_freq_2, use frequency calibration result to update asm_freq_3 1: Use frequency calibration result to update asm_freq_2, use period calibration result to update asm_freq_3
0	CALI2_EN	**Enables frequency calibrator 2** If auto restart is 0, this bit will be cleared while one calibration run is completed. If this bit is set to 0, wait until this bit becomes 0 to make the next run start safely. 0: Disable calibrator 1: Enable calibrator

11220560 AFE_ASRC_CON17 ASRC Config 17 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALC2_DENOMINATOR							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALC2_DENOMINATOR															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Name	Description
23:0	FREQ_CALC2_DENOMINATOR	**Determines denominator for performing period-to-frequency calibration result translation** 48K: 3250 (0xCB2) 44.1K: 8125 (0x1FBD)

11220564 AFE_ASRC_CON18 ASRC Config 18 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PRD_CALI2_RESULT_RECORD							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRD_CALI2_RESULT_RECORD															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	PRD_CALI2_RESULT_RECORD	**Period calibration 2 result** Records the calibration result of previous round. Write any value to this register will clear the result.

11220568 AFE_ASRC_CON19 ASRC Config 19 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI2_RESULT							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI2_RESULT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	FREQ_CALI2_RESULT	**Frequency calibrator 2 result** Records the calibration result of previous round. This value is got from the quotient of (FREQ_CALC2_DENOMINATOR/PRD_CALI2_RESULT) in 1.23 format.

1122056C AFE_ASRC_CON20 ASRC Config 20 00001B00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI2_AUTORST_TH_HIGH							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI2_AUTORST_TH_HIGH															
Type	RW															
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	FREQ_CALI2_AUTORST_TH_HIGH	**Frequency calibrator 2 auto reset threshold high bound** When the calibration result is bigger than this value, HW will auto reset freq_cali2/ring2/history status when calibration result returns to normal value.

11220570 AFE_ASRC_CON21 ASRC Config 21 00001800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI2_AUTORST_TH_LOW							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI2_AUTORST_TH_LOW															
Type	RW															
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	FREQ_CALI2_AUTORST_TH_LOW	**Frequency calibrator 2 auto reset threshold low bound** When the calibration result is smaller than this value, HW will auto reset freq_cali2/ring2/history status when calibration result returns to normal value.

11220108 AFE_ADDA_DL_SRC2_CON0 AFE_DL_SRC2 Control Register 0F000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dl_2_input_mode_ctl				dl_2_ch1_saturation_en_ctl	dl_2_ch2_saturation_en_ctl	dl_2_output_sel_ctl								dl_2_fade in_ostart_en	
Type	RW				RW	RW	RW								RW	
Reset	0	0	0	0	1	1	1	1							0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dl_disable_hw_cg_ctl	c_data_en_sel_ctl_pre	dl_2_side_tone_on_ctl_pre	dl_2_mute_ch1_off_ctl_pre	dl_2_mute_ch2_off_ctl_pre	dl2_aramp sp_ctl_pre		dl_2_iirmode_ctl_pre			dl_2_voice_mode_ctl_pre	d2_2_mute_ch1_on_ctl_pre	d2_2_mute_ch2_on_ctl_pre	dl_2_iir_on_ctl_pre	dl_2_gain_on_ctl_pre	dl_2_src_on_tmp_ctl_pre
Type	RW	RW	RW	RW	RW	RW		RW			RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	dl_2_input_mode_ctl	**Selects input sampling rate of down-link** 0: 8k 1: 11.025k 2: 12k 3: 16k 4: 22.05k 5: 24k 6: 32k 7: 44.1k 8: 48k 9: 96k 10: 192k Other : 8k
27	dl_2_ch1_saturation_en_ctl	**Saturates input signal into -1~1-1LSB** (Origin: -8~8-1lsb)
26	dl_2_ch2_saturation_en_ct	**Saturates input signal into -1~1-1LSB**

Bit(s)	Name	Description
	l	(Origin: -8~8-1lsb)
25:24	dl_2_output_sel_ctl	**Selects output mode of down-link** 0: x1 of up-sample rate 1: x2 of up-sample rate 2: x4 of up-sample rate 3: x8 of up-sample rate
17:16	dl_2_fadein_0start_en	**When [12:11]=0 (mute_off=0 means enable mute function), test method should be** 2-1 [12:11]=0 and [4:3]=0 (fade-in), then [17:16]=2'b11 to trigger fade-in start at 0 gain. To trigger, write [17:16]=2'b00 then [17:16]=2'b11. Each on/off of bit[17:16] should be seperated by time interval > 1/FS. 2-2 test 2-1 but setup [4:3]=2'b11 (fade-out) and the fade-out procedure should not be affected. 00: Disable ch1 and ch2 fadein from 0 11: Enable ch1 and ch2 fadein from 0
15	dl_disable_hw_cg_ctl	**Turns on to disable HW CG** 0: Default 1: Disable HW CG
14	c_data_en_sel_ctl_pre	Default: 0 DL output rate: 8x Otherwise, the output rate is decided by AFE_DL_SRC2_CON0_H[9:8]
13	dl_2_side_tone_on_ctl_pre	**Turns on side-tone filter from up-link path** Reserved
12	dl_2_mute_ch1_off_ctl_pre	**Turns off mute function in channel 1** 0: Turn on mute function 1: Turn off mute function
11	dl_2_mute_ch2_off_ctl_pre	**Turns off mute function in channel 2** 0: Turn on mute function 1: Turn off mute function
10:9	dl2_arampsp_ctl_pre	**Speed of mute function to zero out** 0: Gain speed = 0.00025 per sample (total 4,096 samples) 1: Gain speed = 0.0005 per sample (total 2,048 samples) 2: Gain speed = 0.001 per sample (total 1,024 samples) 3: Gain speed = 0.002 per sample (total 512 samples)
8:6	dl_2_iirmode_ctl_pre	**Selects band of IIR DC-removial filter** 0: 4k: 90Hz, 8k: 180Hz 1: 4k: 160Hz, 8k: 320Hz 2: 4k: 200Hz, 8k: 400Hz 3: 4k: 250Hz, 8k: 500Hz 4: 16k: 100Hz
5	dl_2_voice_mode_ctl_pre	**Selects voice input** 0: Audio data 1: Voice data (small group delay and only enable 8k/16kHz)
4	d2_2_mute_ch1_on_ctl_pre	0: Mute up (back to gain = 1) 1: Mute down
3	d2_2_mute_ch2_on_ctl_pre	0: Mute up (back to gain = 1) 1: Mute down
2	dl_2_iir_on_ctl_pre	**Turns on DC_removal function**
1	dl_2_gain_on_ctl_pre	**Turns on degrade gain function**
0	dl_2_src_on_tmp_ctl_pre	**Turns on down-link**

1122010C	**AFE_ADDA_DL_SRC2_CON1**	**AFE_DL_SRC2 Control Register 1 Part**	**00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dl_2_gain_ctl_pre															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																dl_2_gain_mode_ctl
Type																RW
Reset																0

Bit(s)	Name	Description
31:16	dl_2_gain_ctl_pre	**Gain of degrade gain stage [1, 0] = [FFFF, 0]**
0	dl_2_gain_mode_ctl	**Down link gain formatting** 0: gain_to_mac = [2:0:16] (suggested) 1: gain_to_mac = {[1:0:16],1'b0}

11220114 AFE_ADDA_UL_SRC_CON0 AFE Uplink SRC Control Register 0 Part 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	c_comb_out_sin_gen_ctl	c_baseband_sin_gen_ctl	c_digmic_phase_sel_ch1_ctl			c_digmic_phase_sel_ch2_ctl			c_two_digital_mic_ctl	ul_mode_3p25m_ch2_ctl	ul_mode_3p25m_ch1_ctl	ul_src_use_cic_out_ctl	ul_voice_mode_ch1_ch2_ctl			
Type	RW	RW	RW			RW			RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmic_low_power_mode_ctl		dmic_48k_sel_ctl	ul_disable_hw_cg_ctl		ul_iir_on_tmp_ctl	ul_iirmode_ctl				digmic_3p25m_1p625m_sel_ctl	agc_260k_sel_ch2_ctl	agc_260k_sel_ch1_ctl	ul_loop_back_mode_ctl	ul_sdm_3_level_ctl	ul_src_on_tmp_ctl
Type	RW		RW	RW		RW	RW				RW	RW	RW	RW	RW	RW
Reset	0	0	0	0		0	0	0	0		0	0	0	0	0	0

Bit(s)	Name	Description
31	c_comb_out_sin_gen_ctl	**Mux for uplink comb filter output to uDSP** 0: Uplink comb filter data path output 1: Sine table output
30	c_baseband_sin_gen_ctl	**Mux for the uplink SRC output to interconnections.** Reserved 0: Uplink SRC data path output 1: Sine table output
29:27	c_digmic_phase_sel_ch1_ctl	**Selects 8 input phase latch** Reserved
26:24	c_digmic_phase_sel_ch2_ctl	**Selects 8 input phase latch** Reserved
23	c_two_digital_mic_ctl	**Turns on dual digital microphones mode** Reserved 0: Turn off 1: Turn on

Bit(s)	Name	Description
22	ul_mode_3p25m_ch2_ctl	**Turns on digital microphone for channel 2** The input mode is 3.25MHz sampling rate. Reserved. 0: Turn off 1: Turn on
21	ul_mode_3p25m_ch1_ctl	**Turns on digital microphone for channel 1** The input mode is 3.25MHz sampling rate. Reserved. 0: Turn off 1: Turn on
20	ul_src_use_cic_out_ctl	**Selects uplink CIC mode** 0: PMIC output rate is 64k/96k/384k for normal/Hi-res uplink 1: PMIC output rate is 260k/130k/65k/others for ANC/CIC1 uplink
19:17	ul_voice_mode_ch1_ch2_ctl	**Selects voice mode of channel 1 and channel 2** 000b: 8kHz mode 001b: 16kHz mode 010b: 32kHz mode 011b: 48kHz mode 100b: HD96kHz mode 101b: HD192kHz mode 110b: HD48kHz mode
15:14	dmic_low_power_mode_ctl	**Ch1/ch2 digital mic low power mode** 0: Original mode 1: 1.625m 48k mode 2: 812.5k low power mode 3: 406.25k low power mode
13	dmic_48k_sel_ctl	**Ch1/ch2 3.25m 48k support** 0: 3.25m 32k/16k/8k 1: 3.25m 48k
12	ul_disable_hw_cg_ctl	**Turns on to disable HW CG** 0: Default 1: Disable HW CG
10	ul_iir_on_tmp_ctl	**Turns on IIR DC removal filter** 0: Turn off 1: Turn on
9:7	ul_iirmode_ctl	**Selects stop band of IIR DC-removal filter** 000b: 90Hz if 8kHz mode; 180Hz if 16kHz mode 001b: 160Hz if 8kHz mode; 320Hz if 16kHz mode 010b: 200Hz if 8kHz mode; 400Hz if 16kHz mode 011b: 320Hz if 8kHz mode; 640Hz if 16kHz mode 100b: 100Hz if 16kHz mode
5	digmic_3p25m_1p625m_sel_ctl	**Digmic input mode** 0: 325M mode 1: 1625M mode
4	agc_260k_sel_ch2_ctl	**Replaces the original raw data with AGC computed one at 260kHz in channel 2** Reserved 0: Does not replace the original raw data 1: Replace the original raw data
3	agc_260k_sel_ch1_ctl	**Replaces the original raw data with AGC computed one at 260kHz in channel 1** Reserved 0: Does not replace the original raw data 1: Replace the original raw data
2	ul_loop_back_mode_ctl	**Uplink input is from the downlink output** The 2nd-priority choice 0: De-select loopback mode

Bit(s)	Name	Description
		1: Select loopback mode from downlink SDM
1	ul_sdm_3_level_ctl	**Selects SDM 3-level mode (digital MIC data path), first priority choice** 0: De-select SDM 3-level mode 1: Select SDM 3-level mode
0	ul_src_on_tmp_ctl	**Turns on uplink SRC** 0: Turn off 1: Turn on

11220118 AFE_ADDA_UL_SRC_CON1 AFE Uplink SRC Control Register 1 Part 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	c_sdm_reset_ctl	adithon_ctl	adithval_ctl		c_dac_en_ctl	c_mute_sw_ctl	asdm_src_sel_ctl		c_amp_div_ch2_ctl				c_freq_div_ch2_ctl			
Type	RW	RW	RW		RW	RW	RW		RW				RW			
Reset	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c_sine_mode_ch2_ctl				c_amp_div_ch1_ctl			c_freq_div_ch1_ctl					c_sine_mode_ch1_ctl			
Type	RW				RW			RW					RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	c_sdm_reset_ctl	**Software reset of FPGA SDM** Reserved 0: No reset 1: Reset
30	adithon_ctl	**Turns on dither in FPGA SDM** Reserved 0: Turn off 1: Turn on
29:28	adithval_ctl	**Sets up value of dither in FPGA SDM** Reserved
27	c_dac_en_ctl	**Mux for uplink comb filter output to uDSP** 0: Uplink comb filter data path output 1: Sine table output
26	c_mute_sw_ctl	**Mute switch (SGEN)** 0: Turn on the sine wave output in this test mode 1: Mute the sine wave output
25	asdm_src_sel_ctl	**DAC SDM Tri-angular generator testing path (TSGEN)** 0: Normal path 1: Triangular tone
23:21	c_amp_div_ch2_ctl	**Amplitude setting of channel 2 (SGEN)** 000b: 1/128 full scale 001b: 1/64 full scale 010b: 1/32 full scale 011b: 1/16 full scale 100b: 1/8 full scale 101b: 1/4 full scale 110b: 1/2 full scale 111b: full scale
20:16	c_freq_div_ch2_ctl	**Frequency setting of channel 2** 1X ~ 15X for voice, 1X ~ 31X for audio.

Bit(s)	Name	Description
		Frequency = Sampling rate/64*FREQ_DIV (SGEN)
15:12	c_sine_mode_ch2_ctl	**Selects input mode of sine table of channel 2 (SGEN)** 0: 8k 1: 11.025k 2: 12k 3: 16k 4: 22.05k 5: 24k 6: 32k 7: 44.1k 8~15: 48k
11:9	c_amp_div_ch1_ctl	**Amplitude setting of channel 1 (SGEN)** 000b: 1/128 full scale 001b: 1/64 full scale 010b: 1/32 full scale 011b: 1/16 full scale 100b: 1/8 full scale 101b: 1/4 full scale 110b: 1/2 full scale 111b: Full scale
8:4	c_freq_div_ch1_ctl	**Frequency setting of channel 1** 1X ~ 15X for voice, 1X ~ 31X for audio. Frequency = sSampling rate/64*FREQ_DIV (SGEN)
3:0	c_sine_mode_ch1_ctl	**Select the input mode of sine table of channel 1 (SGEN)** 0: 8k 1: 11.025k 2: 12k 3: 16k 4: 22.05k 5: 24k 6: 32k 7: 44.1k 8~15: 48k

11220120 AFE_ADDA_TOP_CON0 AFE Top Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**c_loop_back_mode_ctl**															**c_ext_adc_ctl**
Type	RW															RW
Reset	0	0	0	0												0

Bit(s)	Name	Description
15:12	c_loop_back_mode_ctl	**Built-in loop-back test mode** 0: Normal path from analog input path 2: Built-in sine table for UL-I2S-FIFO input (1st priority) 1: DL-I2S-FIFO output to UL-I2S input (2nd priority) 4: Down-link input from built-in sine table

Bit(s)	Name	Description
0	c_ext_adc_ctl	**I_03/I_04 souce from internal/external ADC** 0: Internal adc output selection 1: External adc output selection

11220124 AFE_ADDA_UL_DL_CON0 Audio UL and DL Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		afe_ul_dl_cono_reserved														adda_afe_on
Type		RW														RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:1	afe_ul_dl_cono_reserved	
0	adda_afe_on	**Enables ADDA total (synced with 26M)** 0: Disable ADDA interface 1: Enable ADDA interface

1122012C AFE_ADDA_SRC_DEBUG AFE UL Debug Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				ul_slt_cnt_flag_reset_ctl		slt_cnt_thd_ctl										
Type				RW		RW										
Reset				0		0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				dl_slt_cnt_flag_reset_ctl	dl_slt_cnt_thd_ctl											
Type				RW	RW											
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	ul_slt_cnt_flag_reset_ctl	**Resets SLT_CNT_FLAG when SLT_CNT < SLT_CNT_THD** 0: Does not reset slt_cnt_flag of UL 1: Reset slt_cnt_flag of UL
26:16	slt_cnt_thd_ctl	**slt_cnt_thd threshold** ul state machine slt_cnt threshold
12	dl_slt_cnt_flag_reset_ctl	**Resets SLT_CNT_FLAG when SLT_CNT <**

Bit(s)	Name	Description
		SLT_CNT_THD 0: Does not reset slt_cnt_flag of DL 1: Reset slt_cnt_flag of DL
11:0	dl_slt_cnt_thd_ctl	**slt_cnt_thd threshold** dl state machine slt_cnt threshold

11220130 AFE_ADDA_SRC_DEBUG_MON0 **AFE Uplink SRC Monitor Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				slt_cnt_flag_ctl		slt_counter_ctl										
Type				RU		RU										
Reset				0		0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dl_slt_cnt_flag_ctl			dl_ini_sram_finish_ctl		dl_slt_counter_ctl										
Type	RU			RU		RU										
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	slt_cnt_flag_ctl	
26:16	slt_counter_ctl	
15	dl_slt_cnt_flag_ctl	
12	dl_ini_sram_finish_ctl	
11:0	dl_slt_counter_ctl	

11220134 AFE_ADDA_SRC_DEBUG_MON1 **AFE Downlink SRC Monitor Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				slt_cnt_flag_hires_ctl		slt_ counter_ hires_ctl										
Type				RU		RU										
Reset				0		0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													dlsatflag			
Type													RU			
Reset													0	0	0	0

Bit(s)	Name	Description
28	slt_cnt_flag_hires_ctl	

Bit(s)	Name	Description
26:16	slt_counter_hires_ctl	
3:0	dlsatflag	[3] pos_sat_ch1 [2] neg_sat_ch1 [1] pos_sat_ch2 [0] neg_sat_ch2

11220138 AFE_ADDA_NEWIF_CFG0 AFE MTK ADDA NEWIF Control Register 0 03F87200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dlsatflag_clr				up8x_rxif_clkinv_adc	up8x_rxif_fifo_rsp_adc			up8x_sync_word							
Type	RW				RW	RW			RW							
Reset	0				0	0	1	1	1	1	1	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	up8x_sync_word										up8x_if_hires_fmt	up8x_if_loopback1			up8x_txif_clkinv	up8x_txif_sat_en
Type	RW										RW	RW			RW	RW
Reset	0	1	1	1	0	0	1	0			0	0			0	0

Bit(s)	Name	Description
31	dlsatflag_clr	0: Write 0 to enable SAT flag detection. 1: Write 1 to clear dlsatflag[3:0]
27	up8x_rxif_clkinv_adc	0: Does not invert 1: SCK inverts in ADC NEWIF (at top first latch circuit).
26:24	up8x_rxif_fifo_rsp_adc	**NEWIF ADC FIFO read start point**
23:8	up8x_sync_word	**up8x interface sync word definition**
5	up8x_if_hires_fmt	0: Original format [1 4 19] 1: Hires format [1 0 23]
4	up8x_if_loopback1	**Tests ADDA loopback from up8x_txif (DAC) to up8x_rxif_adc (ADC) to check AP side up-sample/decimation filter.** *Note:* *1. For DAC sample rate FS, only FS = 8K/12K can conduct the loopback test. When FS = 8K, the ADC sample rate is operating at 64kHz (ul_voice_mode_ch1_ctl = ul_voice_mode_ch2_ctl = 0/1/2). When FS = 12K, the ADC sample rate is operating at 96kHz (ul_voice_mode_ch1_ctl = ul_voice_mode_ch2_ctl = 3).* *2. Because the bitwidth between DAC and ADC is not the same, the DAC gain function must be turned on (dl_2_gain_on_ctl_pre = 1) and the maximum dl_2_gain_ctl_pre should be constrained (for ul_voice_mode_ch1_ctl = ul_voice_mode_ch2_ctl = 0/1/2, the recommended maximum gain is 0xF625, for ul_voice_mode_ch1_ctl = ul_voice_mode_ch2_ctl = 3, the maximum gain is 0x3FFF), if you would like to receive the un-saturated sinewave. If you do not mind the saturated sinewave, be sure to set up up8x_txif_sat_en = 1 for wrapping around in the Rx domain.* 0: No loopback (normal path) 1: Loopback test 1
1	up8x_txif_clkinv	**Reserved**

Bit(s)	Name	Description
0	up8x_txif_sat_en	0: Does not invert 1: Invert 0: Not saturated ([1 4 19]) 1: Saturated ([1 4 19]--> [1 0 19])

1122013C AFE_ADDA_NEWIF_CFG1 AFE MTK ADDA NEWIF Control Register 1 03117180

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					up8x_rxif_adc_invalid_sync_check_round				up8x_rxif_adc_sync_check_round							up8x_rxif_adc_sync_search_table
Type					RW				RW							RW
Reset					0	0	1	1	0	0	0	1				1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	up8x_rxif_adc_sync_search_table				up8x_rxif_adc_voice_mode			up8x_rxif_adc_sync_cnt_table_adc								
Type	RW				RW			RW								
Reset	0	1	1	1	0	0		1	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:24	up8x_rxif_adc_invalid_sync_check_round	**up8x rxif: Invalid sync word after not consecutively searching for the same sync; will output fail flag at bit[31]**
23:20	up8x_rxif_adc_sync_check_round	**up8x rxif: Valid sync word after consecutively searching for the same sync word successfully**
16:12	up8x_rxif_adc_sync_search_table	**up8x rxif: Time slot 2 (sync found window) calculated by 26MHz after passing time slot 1**
11:10	up8x_rxif_adc_voice_mode	**This value should be identical to ul_voice_mode_ch1_ctl(=ul_voice_mode_ch2_ctl) but can be set to 0 for user-defined value (up8x_rxif_adc_sync_cnt_table[8:0])** 0: Time slot 1 = up8x_rxif_adc_sync_cnt_table[8:0], time slot 2 = up8x_rxif_adc_sync_search_table[4:0] 1: Time slot 1 = 384, time slot 2 = 23 @ 64K interval 2: Time slot 1= 384, time slot 2 = 23 @ 64K interval 3: Time slot 1 = 246, time slot 2 = 27 @ 96K interval
8:0	up8x_rxif_adc_sync_cnt_table_adc	**up8x rxif: Time slot 1 (lower bound) between 2 valid sync word calculated by 26MHz**

11220140 AFE_ADDA_NEWIF_CFG2 AFE MTK ADDA NEWIF Control Register 2 03117180

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	anc_up8x_rxif_adc_voice_mode				anc_up8x_rxif_adc_invalid_sync_check_round				anc_up8x_rxif_adc_sync_check_round							anc_up8x_rxif_adc_sync_search_table
Type	RW				RW				RW							RW

Reset	0	0	0	0	0	0	1	1	0	0	0	1				1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	anc_up8x_rxif_adc_sync_search_table				anc_if_zd_mode	anc_up8x_rxif_adc_sync_cnt_table_adc										
Type	RW				RW	RW										
Reset	0	1	1	1	0	0	0	1	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	anc_up8x_rxif_adc_voice_mode	**up8x rxif: Invalid sync word after not consecutively searching for the same sync; will output fail flag at bit[31]** 0: Time slot 1 = up8x_rxif_adc_sync_cnt_table[8:0], time slot 2 = up8x_rxif_adc_sync_search_table[4:0] 1: Time slot 1 = 384, time slot 2 = 23 @ 64K interval 2: Time slot 1= 384, time slot 2 = 23 @ 64K interval 4: Time slot 1 = 49, time slot 2 = 24 @ 384K interval 5: Time slot 1 = 49, time slot 2 = 24 @ 384K interval 6: Time slot 1 = 49, time slot 2 = 24 @ 384K interval 8: Time slot1 = 78, time slot 2 = 24 @ 260K interval 9: Time slot 1 = 178, time slot 2 = 24 @ 130K interval 10: Time slot 1 = 378, time slot 2 = 24 @ 65K interval 11: Time slot 1 = 778, time slot 2 = 24 @ 32.5K interval 12: Time slot 1 =1578, time slot 2 = 24 @ 16.25K interval
27:24	anc_up8x_rxif_adc_invalid_sync_check_round	**up8x rxif: Invalid sync word after not consecutively searching for the same sync; will output fail flag at bit[31]**
23:20	anc_up8x_rxif_adc_sync_check_round	**up8x rxif: Valid sync word after consecutively searching for the same sync word successfully**
16:12	anc_up8x_rxif_adc_sync_search_table	**up8x rxif: Time slot 2 (sync found window) calculated by 26MHz after passing time slot 1**
11	anc_if_zd_mode	**Sets up zero delay mode**
10:0	anc_up8x_rxif_adc_sync_cnt_table_adc	**up8x rxif: Time slot 1 (lower bound) between 2 valid sync word calculated by 26MHz**

11220600 AFE_ADDA2_TOP_CON0 **EVEREST HPANC control register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																io2io3_data_loss_status
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				0506_anc_data_select	021022_anc_data_select	hpanc_io2_loss_clear	anc_dl_dat_from_fifo	anc_dl_fifo_en	ul_dn25_sel	adda2_anc_dl_input_mode			adda2_dl_src_on	anc_loop_back_sine_ch2	anc_loop_back_sine_ch1	anc_mtkif_loop_back1
Type				RW	RW	RW	RW	RW	RW	RW			RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	io2io3_data_loss_status	**io2, io3 data loss flag status**
12	o506_anc_data_select	**o506 select anc data**
11	o21022_anc_data_select	**o21 022 select anc data**
10	hpanc_io2_loss_clear	**Clears hp anc io2,3 data loss flag**
9	anc_dl_dat_from_fifo	**Selects anc dl data from FIFO**
8	anc_dl_fifo_en	**Enables anc dl FIFO**
7	ul_dn25_sel	**UL source from PMIC is down 25x**
6:4	adda2_anc_dl_input_mode	**Selects anc dl path data rate** Default: 260k; others for debugging
3	adda2_dl_src_on	**Enables anc dl path**
2	anc_loop_back_sine_ch2	**anc dl mtk tx source select sine tone**
1	anc_loop_back_sine_ch1	**anc dl mtk tx source select sine tone**
0	anc_mtkif_loop_back1	**anc dl mtk rx sdata select anc dl mtk tx out**

11220260 AFE_ADDA_PREDIS_CON0 AFE Pre-distortion Control Port 0 High Part 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	predis_on_ch1_ctl				predis_a2_ch1_ctl											
Type	RW				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					predis_a3_ch1_ctl											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	predis_on_ch1_ctl	Down-link pre-distortion on for ch1
27:16	predis_a2_ch1_ctl	pre-distortion coefficient a2 for ch1
11:0	predis_a3_ch1_ctl	pre-distortion coefficient a3 for ch1

11220264 AFE_ADDA_PREDIS_CON1 AFE Pre-distortion Control Port 1 High Part 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	predis_on_ch2_ctl				predis_a2_ch2_ctl											
Type	RW				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					predis_a3_ch2_ctl											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	predis_on_ch2_ctl	Down-link pre-distortion on for ch2
27:16	predis_a2_ch2_ctl	pre-distortion coefficient a2 for ch2
11:0	predis_a3_ch2_ctl	pre-distortion coefficient a3 for ch2

Bit(s)	Name	Description

11220270 AFE_MRGIF_MON0 AFE Merge Interface Monitor Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MRGIF_I2S_RCH_CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	MRGIF_I2S_RCH_CNT	Indicates PCM Rx FIFO is overflow

11220274 AFE_MRGIF_MON1 AFE Merge Interface Monitor Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MRGIF_I2S_LCH_CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	MRGIF_I2S_LCH_CNT	**Receive data's monitor counter of I2S's right channel** When data 0 is recieved, this counter will be not increased.

11220278 AFE_MRGIF_MON2 AFE Merge Interface Monitor Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															MRGIF_PCM_RX_OVF	MRGIF_PCM_RX_UNF
Type															RU	RU
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MRGIF_PCM_CNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	MRGIF_PCM_RX_OVF	**Indicates PCM Rx FIFO is underflow**
16	MRGIF_PCM_RX_UNF	**Receive data's monitor counter of PCM**

Bit(s)	Name	Description
15:0	MRGIF_PCM_CNT	When data 0 is recieved, this counter will be not increased. **MRGIF_PCM_CNT**

1122027C AFE_I2S_MON **EVEREST FM Connsys Debug Signal** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				i2s_src				valid_check				i2s_in_ws				e_ws_neg
Type				RU				RU				RU				RU
Reset				0				0				0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				e_ws_pos				rcv_cnt								sync_glitch
Type				RU				RU								RU
Reset				0				0	0	0	0	0				0

Bit(s)	Name	Description
28	i2s_src	i2s src signal
24	valid_check	enable for check rcv_cnt
20	i2s_in_ws	i2s_in_ws
16	e_ws_neg	e_ws_neg
12	e_ws_pos	e_ws_pos
8:4	rcv_cnt	rcv_cnt
0	sync_glitch	sync_glitch

112206C0 AFE_ASRC4_CON0 **ASRC4 Config 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			CHSET1_CLR_IIR_HISTORY	CHSET1_IS_MONO	CHSET1_OFS_SEL		CHSET1_IFS_SEL		CHSET1_IIR_EN	CHSET1_IIR_STAGE					CHSETo_CLR_IIR_HISTORY	CHSETo_IS_MONO
Type			RW	RW	RW		RW		RW	RW					RW	RW
Reset			0	0	0	0	0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHSETo_OFS_SEL		CHSETo_IFS_SEL		CHSETo_IIR_EN	CHSETo_IIR_STAGE					CHSET_STR_CLR		CHSET_ON		COEF_SRAM_CTRL	ASM_ON
Type	RW		RW		RW	RW					RW		RU		RW	RW
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
29	CHSET1_CLR_IIR_HISTORY	**Set to 1 to clear the current IIR output history buffer for RX.** This register will auto-clear once the histories are cleared.
28	CHSET1_IS_MONO	**Mono/Stereo selection register**
27:26	CHSET1_OFS_SEL	**Selects output sample rate for RX** Set to 01 for OFS fix value.

Bit(s)	Name	Description
25:24	CHSET1_IFS_SEL	**Selects input sample rate for RX** Set to 10 for frequency tracking mode.
23	CHSET1_IIR_EN	**Enables anti-alias IIR filter for RX** Set 1 to Turns on anti-alias IIR filter.
22:20	CHSET1_IIR_STAGE	**Anti-alias IIR filter stage for RX** Defines how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 orders are supported.
17	CHSET0_CLR_IIR_HISTORY	**Set to 1 to clear current IIR output history buffer for TX.** This register will auto-clear once the histories are cleared.
16	CHSET0_IS_MONO	**Mono/Stereo selection register**
15:14	CHSET0_OFS_SEL	**Selects output sample rate for TX** Set to 00 for OFS fix value.
13:12	CHSET0_IFS_SEL	**Selects input sample rate selection for TX** Set to 11 for period tracking mode.
11	CHSET0_IIR_EN	**Enables anti-alias IIR filter for TX** Set 1 to Turns on anti-alias IIR filter.
10:8	CHSET0_IIR_STAGE	**Anti-alias IIR filter stage for TX** Defines how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 orders are supported.
5:4	CHSET_STR_CLR	**Each channel set clear signal** Set bit 0 to 1 to clear the TX history. Set bit 1 to 1 to clear the RX history. Set bit 2 to 1 to clear the I2S history.
3:2	CHSET_ON	**Indicates which channel set is on currently** 01: TX 10: RX
1	COEFF_SRAM_CTRL	**Controls coefficient SRAM access** 0: Disable access 1: Enable access
0	ASM_ON	**ASRC enabling signal** Turn it on after all Configurations are set. 0: Disable ASRC 1: Enable ASRC

112206C4 AFE_ASRC4_CON1 ASRC4 Config 1 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_0							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_0															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Name	Description
23:0	ASM_FREQ_0	**Frequency palette** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX OFS.

112206C8 AFE_ASRC4_CON2 **ASRC4 Config 2** **00400000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_1							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	ASM_FREQ_1	**Frequency palette** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX OFS.

112206CC AFE_ASRC4_CON3 **ASRC4 Config 3** **00400000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_2							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	ASM_FREQ_2	**Frequency palette** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX IFS.

112206D0 AFE_ASRC4_CON4 **ASRC4 Config 4** **00000CB2**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_3							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_3															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Name	Description
23:0	ASM_FREQ_3	**Frequency palette** The frequency palette for each channel set to define its input frequency and output frequency.

Bit(s)	Name	Description
		Default is set for TX IFS.

112206D4 AFE_ASRC4_CON5 **ASRC4 Config 5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RESULT_SEL		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	RESULT_SEL	**Selects output** 000: ASRC output 001: Data input 010: CMPF output 011: HBF1 output 100: HBF2 output 101: HBF3 output 110: HBF4 output 111: Each IIR stage output in order

112206D8 AFE_ASRC4_CON6 **ASRC4 Config 6** **00010800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FREQ_CALI_CYCLE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_EN		FREQ_CALC_RUNNING	AUTO_TUNE_FREQ3	COMP_FREQ_RES_EN		FREQ_CALI_SEL		FREQ_CALI_BP_DGL	FREQ_CALI_MAX_GWIDTH			AUTO_TUNE_FREQ2	FREQ_CALI_AUTO_RESTART	CALI_USE_FREQ_OUT	CALI_EN
Type	RW		RU	RW	RW		RW		RW	RW			RW	RW	RW	RU
Reset	0		0	0	1		0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	FREQ_CALI_CYCLE	**Frequency calibrating cycle register** Defines how many input signal cycles the calibrator calibrates are in one round. This register is updated into calibrator once the calibrator enable [0] is turned on.
15	FREQ_CALI_AUTORST_EN	**Enables period calibration auto-reset** Priod calibration bigger than 0x734 or smaller than 0x738 will trigger ASRC reset.
13	FREQ_CALC_RUNNING	**Shows if frequency calculation is running** For one round running case, wait for this bit and the CALI_EN bit to become low before frequency result is ready.

Bit(s)	Name	Description
12	AUTO_TUNE_FREQ3	**Enables asm_freq_3 auto update with the calibrator result once the calibrator completes one round** 0: Disable auto update 1: Enable auto update
11	COMP_FREQ_RES_EN	**Frequency compensation enabling register** 0: Disable compensation 1: Enable compensation
9:8	FREQ_CALI_SEL	**Calibrator input source selection register** Before modifying this register, make sure the calibrator is turned off. 00: Use PCM SYNC word 01: Not connected 10: Not connected 11: Not connected
7	FREQ_CALI_BP_DGL	**Bypasses deglitch circuit for calibrator input** 0: No bypass 1: Bypass
6:4	FREQ_CALI_MAX_GWIDTH	**Defines the maximum glitch width of the calibrator input signal** Unit: Calibrator reference clock cycles
3	AUTO_TUNE_FREQ2	**Enables asm_freq_2 auto update with the calibrator result once the calibrator completes one round** 0: Disable auto update 1: Enable auto update
2	FREQ_CALI_AUTO_RESTART	**Enables calibrator auto restart new calibration while one run is completed** This value will be updated into calibrator once the enabling signal is turned on from off state. 0: Disable auto restart 1: Enable auto restart
1	CALI_USE_FREQ_OUT	**Selects frequency or period calibration mode** 0: Use period calibration result to update asm_freq_2. Use frequency calibration result to update asm_freq_3 1: Use frequency calibration result to update asm_freq_2. Use period calibration result to update asm_freq_3
0	CALI_EN	**Enables frequency calibrator** If auto restart is 0, this bit will be cleared while one calibration run is completed. If this bit is set to 0, wait until this bit becomes 0 to make the next run start safely. 0: Disable calibrator 1: Enable calibrator

112206DC AFE_ASRC4_CON7 ASRC4 Config 7 00000659

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALC_DENOMINATOR							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALC_DENOMINATOR															
Type	RW															
Reset	0	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1

Bit(s)	Name	Description

Bit(s)	Name	Description
23:0	FREQ_CALC_DENOMINATOR	Determines the denominator for performing period-to-frequency calibration result translation

112206E0 AFE_ASRC4_CON8 **ASRC4 Config 8** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PRD_CALI_RESULT_RECORD							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRD_CALI_RESULT_RECORD															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	PRD_CALI_RESULT_RECORD	**Period calibration result** Records the calibration result of the previous round. Writing any value to this register will clear the result.

112206E4 AFE_ASRC4_CON9 **ASRC4 Config 9** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_RESULT							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_RESULT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	FREQ_CALI_RESULT	**Frequency calibrator result** Records the calibration result of previous round. This value is got from the quotient of (FREQ_CALC_DENOMINATOR/PRD_CALI_RESULT) in 1.23 format.

112206E8 AFE_ASRC4_CON10 **ASRC4 Config 10** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									COEFF_SRAM_DATA							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COEFF_SRAM_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	COEFF_SRAM_DATA	**Read/Write data port of coefficient SRAM** Read data have one cycle delay. The coefficients are filled stage by stage: each stage has 6 coefficients. For the 2nd-order IIR filter with transfer function of one stage as: "(2^shift)*a0 + (2^shift)*a1*Z^-1 + (2^shift)*a2*Z^-2/1 + (2^shift)*b1*Z^ -1 + (2^shift)*b2*Z^-2" The coefficient should be filled as (from low address to high address) a2 a1 a0 -b1 -b2 shift

112206EC AFE_ASRC4_CON11 **ASRC4 Config 11** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										COEFF_SRAM_ADR						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	COEFF_SRAM_ADR	**Determines the rd/wr address of IIR coefficient SRAM** Read/Write COEFF_SRAM_DATA will make this register increase by 1.

112206F0 AFE_ASRC4_CON12 **ASRC4 Config 12** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									RING1_PALSE_READ_RECORD	RING1_PALSE_WRITE_RECORD	RING1_READ_PTR_PHASE	RING1_WRITE_PTR_PHASE	RING1_READ_PTR			
Type									RU	RU	RU	RU	RU			
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING1_WRITE_PTR				RINGo_PALSE_READ_RECORD	RINGo_PALSE_WRITE_RECORD	RINGo_READ_PTR_PHASE	RINGo_WRITE_PTR_PHASE	RINGo_READ_PTR				RINGo_WRITE_PTR			
Type	RU				RU	RU	RU	RU	RU				RU			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23	RING1_PALSE_READ_RECORD	
22	RING1_PALSE_WRITE_RECORD	
21	RING1_READ_PTR_PHASE	

Bit(s)	Name	Description
20	RING1_WRITE_PTR_PHASE	
19:16	RING1_READ_PTR	
15:12	RING1_WRITE_PTR	
11	RING0_PALSE_READ_RECORD	
10	RING0_PALSE_WRITE_RECORD	
9	RING0_READ_PTR_PHASE	
8	RING0_WRITE_PTR_PHASE	
7:4	RING0_READ_PTR	
3:0	RING0_WRITE_PTR	

112206F4 AFE_ASRC4_CON13 ASRC4 Config 13 00001B00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_HIGH							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_HIGH															
Type	RW															
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	FREQ_CALI_AUTORST_TH_HIGH	**High period calibration threshold to trigger autoreset** Need to enable 0x718[15].

112206F8 AFE_ASRC4_CON14 ASRC4 Config 14 00001800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_LOW							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_LOW															
Type	RW															
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	FREQ_CALI_AUTORST_TH_LOW	**Low period calibration threshold to trigger autoreset** Need to enable 0x718[15].

11220700 AFE_ASRC2_CON0 ASRC2 Config 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			CHSET1_CLR_IIR_H	CHSET1_IS_MONO	CHSET1_OFS_SEL		CHSET1_IFS_SEL		CHSET1_IIR_EN	CHSET1_IIR_STAGE					CHSET0_CLR_IIR_H	CHSET0_IS_MONO

			ISTORY												ISTORY	
Type			RW	RW	RW		RW		RW	RW					RW	RW
Reset			0	0	0	0	0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHSETo_OFS_SEL		CHSETo_IFS_SEL		CHSETo_IIR_EN	CHSETo_IIR_STAGE					CHSET_STR_CLR		CHSET_ON		COEFF_SRAM_CTRL	ASM_ON
Type	RW		RW		RW	RW					RW		RU		RW	RW
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
29	CHSET1_CLR_IIR_HISTORY	**Set to 1 to clear the current IIR output history buffer for RX. This register will auto-clear once the histories are cleared.**
28	CHSET1_IS_MONO	**Mono/Stereo selection register**
27:26	CHSET1_OFS_SEL	**Selects output sample rate for RX.** Set to 01 for OFS fix value.
25:24	CHSET1_IFS_SEL	**Selects input sample rate for RX.** Set to 10 for frequency tracking mode.
23	CHSET1_IIR_EN	**Enables anti-alias IIR filter for RX.** Set 1 to Turns on anti-alias IIR filter.
22:20	CHSET1_IIR_STAGE	**Anti-alias IIR filter stage for RX.** Defines how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 orders are supported.
17	CHSETo_CLR_IIR_HISTORY	**Set to 1 to clear current IIR output history buffer for TX. This register will auto-clear once the histories are cleared.**
16	CHSETo_IS_MONO	**Mono/Stereo selection register**
15:14	CHSETo_OFS_SEL	**Selects output sample rate for TX.** Set to 00 for OFS fix value.
13:12	CHSETo_IFS_SEL	**Selects input sample rate selection for TX.** Set to 11 for period tracking mode.
11	CHSETo_IIR_EN	**Enables anti-alias IIR filter for TX.** Set 1 to Turns on anti-alias IIR filter.
10:8	CHSETo_IIR_STAGE	**Anti-alias IIR filter stage for TX.** Defines how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 orders are supported.
5:4	CHSET_STR_CLR	**Each channel set clear signal. Set bit 0 to 1 to clear the TX history. Set bit 1 to 1 to clear the RX history. Set bit 2 to 1 to clear the I2S history.**
3:2	CHSET_ON	**Indicates which channel set is on currently. 01 means TX. 10 means RX.**
1	COEFF_SRAM_CTRL	**Controls coefficient SRAM access** 0: Disable access 1: Enable access
0	ASM_ON	**ASRC enabling signal. Turn it on after all Configurations are set.** 0: Disable ASRC 1: Enable ASRC

11220704 AFE_ASRC2_CON1 ASRC2 Config 1 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name									ASM_FREQ_0							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_0															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Name	Description
23:0	ASM_FREQ_0	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX OFS.

11220708 AFE_ASRC2_CON2 ASRC2 Config 2 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_1							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	ASM_FREQ_1	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX OFS.

1122070C AFE_ASRC2_CON3 ASRC2 Config 3 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_2							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	ASM_FREQ_2	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX IFS.

11220710 AFE_ASRC2_CON4 ASRC2 Config 4 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_3							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_3															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Name	Description
23:0	ASM_FREQ_3	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX IFS.

11220714 AFE_ASRC2_CON5 ASRC2 Config 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RESULT_SEL		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	RESULT_SEL	**Output selection** 000: ASRC output 001: Data input 010: CMPF output 011: HBF1 output 100: HBF2 output 101: HBF3 output 110: HBF4 output 111: Each IIR stage output in order

11220718 AFE_ASRC2_CON6 ASRC2 Config 6 00010800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FREQ_CALI_CYCLE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORS		FREQ_CALC_RUNNIN	AUTO_TUNE_FREQ3	COMP_FREQ_RES_EN		FREQ_CALI_SEL		FREQ_CALI_BP_DGL	FREQ_CALI_MAX_GWIDTH			AUTO_TUNE_FREQ2	FREQ_CALI_AUTO_R	CALI_USE_FREQ_OU	CALI_EN

	T_EN		G										ESTART	T	
Type	RW		RU	RW	RW		RW		RW	RW			RW	RW	RU
Reset	0		0	0	1		0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	FREQ_CALI_CYCLE	**Frequency calibrating cycle register.** Defines how many input signal cycles the calibrator calibrates are in one round. This register is updated into calibrator once the calibrator enable [0] is turned on.
15	FREQ_CALI_AUTORST_EN	**Period calibration auto-reset enable. Period calibration larger than 0x734 or smaller than 0x738 will trigger ASRC reset.**
13	FREQ_CALC_RUNNING	**Shows if frequency calculation is running.** For one round running case, wait for this bit and the CALI_EN bit to become low before frequency result is ready.
12	AUTO_TUNE_FREQ3	**Enables asm_freq_3 auto update with the calibrator result once the calibrator completes one round.** 0: Disable auto update 1: Enable auto update
11	COMP_FREQ_RES_EN	**Frequency compensation enabling register.** 0: Disable compensation 1: Enable compensation
9:8	FREQ_CALI_SEL	**Calibrator input source selection register. Before modifying this register, make sure the calibrator is turned off.** 00: Use PCM SYNC word 01: Not connected 10: Not connected 11: Not connected
7	FREQ_CALI_BP_DGL	**Bypass the deglitch circuit for calibrator input.** 0: No bypass 1: Bypass
6:4	FREQ_CALI_MAX_GWIDTH	**Defines the maximum glitch width of the calibrator input signal. Unit: Calibrator reference clock cycles.**
3	AUTO_TUNE_FREQ2	**Enables asm_freq_2 auto update with the calibrator result once the calibrator completes one round.** 0: Disable auto update 1: Enable auto update
2	FREQ_CALI_AUTO_RESTART	**Enables calibrator auto restart new calibration while one run is completed. This value will be updated into calibrator once the enabling signal is turned on from off state.** 0: Disable auto restart 1: Enable auto restart
1	CALI_USE_FREQ_OUT	**Selects frequency or period calibration mode** 0: Use period calibration result to update asm_freq_2. Use frequency calibration result to update asm_freq_3 1: Use frequency calibration result to update asm_freq_2. Use period calibration result to update asm_freq_3
0	CALI_EN	**Enable frequency calibrator. If auto restart is 0, this bit will be cleared while one calibration run is completed. If this bit is set to 0, wait until this bit becomes 0 to make the next run start safely.** 0: Disable calibrator 1: Enable calibrator

1122071C AFE_ASRC2_CON7 ASRC2 Config 7 00000659

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALC_DENOMINATOR							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALC_DENOMINATOR															
Type	RW															
Reset	0	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1

Bit(s)	Name	Description
23:0	FREQ_CALC_DENOMINATOR	Determines the denominator for performing period-to-frequency calibration result translation.

11220720 AFE_ASRC2_CON8 ASRC2 Config 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PRD_CALI_RESULT_RECORD							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRD_CALI_RESULT_RECORD															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	PRD_CALI_RESULT_RECORD	**Period calibration result.** Records the calibration result of the previous round. Writing any value to this register will clear the result.

11220724 AFE_ASRC2_CON9 ASRC2 Config 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_RESULT							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_RESULT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	FREQ_CALI_RESULT	**Frequency calibrator result.** Records the calibration result of previous round. This value is got from the quotient of (FREQ_CALC_DENOMINATOR / PRD_CALI_RESULT) in 1.23 format.

11220728 AFE_ASRC2_CON10 ASRC2 Config 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									COEFF_SRAM_DATA							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COEFF_SRAM_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	COEFF_SRAM_DATA	**Read/Write data port of coefficient SRAM.** Read data have one cycle delay. The coefficients are filled stage by stage: each stage has 6 coefficients. For the 2nd-order IIR filter with transfer function of one stage as: "(2^shift)*a0 + (2^shift)*a1*Z^-1 + (2^shift)*a2*Z^-2/1 + (2^shift)*b1*Z^ -1 + (2^shift)*b2*Z^-2" The coefficient should be filled as (from low address to high address) a2 a1 a0 -b1 -b2 shift

1122072C AFE_ASRC2_CON11 ASRC2 Config 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										COEFF_SRAM_ADR						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	COEFF_SRAM_ADR	**Determines the rd/wr address of IIR coefficient SRAM.** Read/Write COEFF_SRAM_DATA will make this register increase by 1.

11220730 AFE_ASRC2_CON12 ASRC2 Config 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									RING1_PALSE_READ_RECORD	RING1_PALSE_WRITE_RECORD	RING1_READ_PTR_PHASE	RING1_WRITE_PTR_PHASE	RING1_READ_PTR			
Type									RU	RU	RU	RU	RU			
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RING1_WRITE_PTR				RINGo_PALSE_READ_RECORD	RINGo_PALSE_WRITE_RECORD	RINGo_READ_PTR_PHASE	RINGo_WRITE_PTR_PHASE	RINGo_READ_PTR				RINGo_WRITE_PTR			
Type	RU				RU	RU	RU	RU	RU				RU			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23	RING1_PALSE_READ_RECORD	
22	RING1_PALSE_WRITE_RECORD	
21	RING1_READ_PTR_PHASE	
20	RING1_WRITE_PTR_PHASE	
19:16	RING1_READ_PTR	
15:12	RING1_WRITE_PTR	
11	RINGo_PALSE_READ_RECORD	
10	RINGo_PALSE_WRITE_RECORD	
9	RINGo_READ_PTR_PHASE	
8	RINGo_WRITE_PTR_PHASE	
7:4	RINGo_READ_PTR	
3:0	RINGo_WRITE_PTR	

11220734 AFE_ASRC2_CON13 ASRC2 Config 13 00001B00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_HIGH							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_HIGH															
Type	RW															
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	FREQ_CALI_AUTORST_TH_HIGH	**High period calibration threshold to trigger autoreset** Enable 0x718[15].

11220738 AFE_ASRC2_CON14 ASRC2 Config 14 00001800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_LOW							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_LOW															
Type	RW															
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	FREQ_CALI_AUTORST_TH_LOW	**Low period calibration threshold to trigger**

Bit(s)	Name	Description
		autoreset Enable 0x718[15].

11220740 AFE_ASRC3_CON0 ASRC3 Config 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			CHSET1_CLR_IIR_HISTORY	CHSET1_IS_MONO	CHSET1_OFS_SEL		CHSET1_IFS_SEL		CHSET1_IIR_EN	CHSET1_IIR_STAGE					CHSETo_CLR_IIR_HISTORY	CHSETo_IS_MONO
Type			RW	RW	RW		RW		RW	RW					RW	RW
Reset			0	0	0	0	0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHSETo_OFS_SEL		CHSETo_IFS_SEL		CHSETo_IIR_EN	CHSETo_IIR_STAGE					CHSET_STR_CLR		CHSET_ON		COEFF_SRAM_CTRL	ASM_ON
Type	RW		RW		RW	RW					RW		RU		RW	RW
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
29	CHSET1_CLR_IIR_HISTORY	**Set to 1 to clear the current IIR output history buffer for RX** This register will auto-clear once the histories are cleared.
28	CHSET1_IS_MONO	**Mono/Stereo selection register**
27:26	CHSET1_OFS_SEL	**Selects output sample rate for RX** Set to 01 for OFS fix value.
25:24	CHSET1_IFS_SEL	**Selects input sample rate for RX** Set to 10 for frequency tracking mode.
23	CHSET1_IIR_EN	**Enables anti-alias IIR filter for RX** Set 1 to Turns on anti-alias IIR filter.
22:20	CHSET1_IIR_STAGE	**Anti-alias IIR filter stage for RX** Defines how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 orders are supported.
17	CHSETo_CLR_IIR_HISTORY	**Set to 1 to clear current IIR output history buffer for TX.** This register will auto-clear once the histories are cleared.
16	CHSETo_IS_MONO	**Mono/Stereo selection register**
15:14	CHSETo_OFS_SEL	**Selects output sample rate for TX** Set to 00 for OFS fix value.
13:12	CHSETo_IFS_SEL	**Selects input sample rate selection for TX** Set to 11 for period tracking mode.
11	CHSETo_IIR_EN	**Enables anti-alias IIR filter for TX** Set 1 to Turns on anti-alias IIR filter.
10:8	CHSETo_IIR_STAGE	**Anti-alias IIR filter stage for TX** Defines how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 orders are supported.
5:4	CHSET_STR_CLR	**Each channel set clear signal** Set bit 0 to 1 to clear the TX history. Set bit 1 to 1 to clear the RX history. Set bit 2 to 1 to clear the I2S history.
3:2	CHSET_ON	**Indicates which channel set is on currently** 01: TX 10: RX

Bit(s)	Name	Description
1	COEFF_SRAM_CTRL	**Controls coefficient SRAM access** 0: Disable access 1: Enable access
0	ASM_ON	**ASRC enabling signal** Turn it on after all Configurations are set. 0: Disable ASRC 1: Enable ASRC

11220744 AFE_ASRC3_CON1 ASRC3 Config 1 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_0							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_0															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Name	Description
23:0	ASM_FREQ_0	**Frequency palette** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX OFS.

11220748 AFE_ASRC3_CON2 ASRC3 Config 2 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_1							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	ASM_FREQ_1	**Frequency palette** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX OFS.

1122074C AFE_ASRC3_CON3 ASRC3 Config 3 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_2							
Type									RW							

Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	ASM_FREQ_2	**Frequency palette** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX IFS.

11220750 AFE_ASRC3_CON4 ASRC3 Config 4 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_3							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_3															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Name	Description
23:0	ASM_FREQ_3	**Frequency palette** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX IFS.

11220754 AFE_ASRC3_CON5 ASRC3 Config 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RESULT_SEL		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	RESULT_SEL	**Selects output** 000: ASRC output 001: Data input 010: CMPF output 011: HBF1 output 100: HBF2 output 101: HBF3 output 110: HBF4 output

Bit(s)	Name	Description
		111: Each IIR stage output in order

11220758 AFE_ASRC3_CON6 ASRC3 Config 6 00010800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FREQ_CALI_CYCLE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_EN		FREQ_CALC_RUNNING	AUTO_TUNE_FREQ3	COMP_FREQ_RES_EN		FREQ_CALI_SEL		FREQ_CALI_BP_DGL	FREQ_CALI_MAX_GWIDTH			AUTO_TUNE_FREQ2	FREQ_CALI_AUTO_RESTART	CALI_USE_FREQ_OUT	CALI_EN
Type	RW		RU	RW	RW		RW		RW	RW			RW	RW	RW	RU
Reset	0		0	0	1		0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	FREQ_CALI_CYCLE	**Frequency calibrating cycle register** Defines how many input signal cycles the calibrator calibrates are in one round. This register is updated into calibrator once the calibrator enable [0] is turned on.
15	FREQ_CALI_AUTORST_EN	**Enables period calibration auto-reset** Period calibration bigger than 0x774 or smaller than 0x778 will trigger ASRC reset.
13	FREQ_CALC_RUNNING	**Shows if frequency calculation is running** For one round running case, wait for this bit and the CALI_EN bit to become low before frequency result is ready.
12	AUTO_TUNE_FREQ3	**Enables asm_freq_3 auto update with the calibrator result once the calibrator completes one round** 0: Disable auto update 1: Enable auto update
11	COMP_FREQ_RES_EN	**Frequency compensation enabling register** 0: Disable compensation 1: Enable compensation
9:8	FREQ_CALI_SEL	**Calibrator input source selection register** Before modifying this register, make sure the calibrator is turned off. 00: Use PCM SYNC word 01: Not connected 10: Not connected 11: Not connected
7	FREQ_CALI_BP_DGL	**Bypasses deglitch circuit for calibrator input** 0: No bypass 1: Bypass
6:4	FREQ_CALI_MAX_GWIDTH	**Defines the maximum glitch width of the calibrator input signal** Unit: Calibrator reference clock cycles
3	AUTO_TUNE_FREQ2	**Enables asm_freq_2 auto update with the calibrator result once the calibrator completes one round** 0: Disable auto update 1: Enable auto update
2	FREQ_CALI_AUTO_RESTART	**Enables calibrator auto restart new calibration while one run is completed**

Bit(s)	Name	Description
		This value will be updated into calibrator once the enabling signal is turned on from off state. 0: Disable auto restart 1: Enable auto restart
1	CALI_USE_FREQ_OUT	**Selects frequency or period calibration mode** 0: Use period calibration result to update asm_freq_2. Use frequency calibration result to update asm_freq_3 1: Use frequency calibration result to update asm_freq_2. Use period calibration result to update asm_freq_3
0	CALI_EN	**Enables frequency calibrator** If auto restart is 0, this bit will be cleared while one calibration run is completed. If this bit is set to 0, wait until this bit becomes 0 to make the next run start safely. 0: Disable calibrator 1: Enable calibrator

1122075C AFE_ASRC3_CON7 ASRC3 Config 7 00000659

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALC_DENOMINATOR							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALC_DENOMINATOR															
Type	RW															
Reset	0	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1

Bit(s)	Name	Description
23:0	FREQ_CALC_DENOMINATOR	Determines the denominator for performing period-to-frequency calibration result translation

11220760 AFE_ASRC3_CON8 ASRC3 Config 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PRD_CALI_RESULT_RECORD							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRD_CALI_RESULT_RECORD															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	PRD_CALI_RESULT_RECORD	**Period calibration result** Records the calibration result of the previous round. Writing any value to this register will clear the result.

11220764 AFE_ASRC3_ ASRC3 Config 9 00000000

CON9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_RESULT							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_RESULT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	FREQ_CALI_RESULT	**Frequency calibrator result** Records the calibration result of previous round. This value is got from the quotient of (FREQ_CALC_DENOMINATOR / PRD_CALI_RESULT) in 1.23 format.

11220768 AFE_ASRC3_CON10 ASRC3 Config 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									COEFF_SRAM_DATA							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COEFF_SRAM_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	COEFF_SRAM_DATA	**Read/Write data port of coefficient SRAM** Read data have one cycle delay. The coefficients are filled stage by stage: each stage has 6 coefficients. For the 2nd-order IIR filter with transfer function of one stage as: "(2^shift)*a0 + (2^shift)*a1*Z^-1 + (2^shift)*a2*Z^-2/1 + (2^shift)*b1*Z^ -1 + (2^shift)*b2*Z^-2" The coefficient should be filled as (from low address to high address) a2 a1 a0 -b1 -b2 shift

1122076C AFE_ASRC3_CON11 ASRC3 Config 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										COEFF_SRAM_ADR						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	COEFF_SRAM_ADR	**Determines the rd/wr address of IIR coefficient SRAM** Read/Write COEFF_SRAM_DATA will make this register increase by 1.

11220770 AFE_ASRC3_CON12 ASRC3 Config 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									RING1_PALSE_READ_RECORD	RING1_PALSE_WRITE_RECORD	RING1_READ_PTR_PHASE	RING1_WRITE_PTR_PHASE	RING1_READ_PTR			
Type									RU	RU	RU	RU	RU			
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING1_WRITE_PTR				RINGo_PALSE_READ_RECORD	RINGo_PALSE_WRITE_RECORD	RINGo_READ_PTR_PHASE	RINGo_WRITE_PTR_PHASE	RINGo_READ_PTR				RINGo_WRITE_PTR			
Type	RU				RU	RU	RU	RU	RU				RU			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23	RING1_PALSE_READ_RECORD	
22	RING1_PALSE_WRITE_RECORD	
21	RING1_READ_PTR_PHASE	
20	RING1_WRITE_PTR_PHASE	
19:16	RING1_READ_PTR	
15:12	RING1_WRITE_PTR	
11	RINGo_PALSE_READ_RECORD	
10	RINGo_PALSE_WRITE_RECORD	
9	RINGo_READ_PTR_PHASE	
8	RINGo_WRITE_PTR_PHASE	
7:4	RINGo_READ_PTR	
3:0	RINGo_WRITE_PTR	

11220774 AFE_ASRC3_CON13 ASRC2 Config 13 00001B00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_HIGH							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_HIGH															
Type	RW															
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	FREQ_CALI_AUTORST_TH_HIGH	**High period calibration threshold to trigger**

Bit(s)	Name	Description
		autoreset Enable 0x758[15].

11220778 AFE_ASRC3_CON14 ASRC2 Config 14 00001800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_LOW							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_LOW															
Type	RW															
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	FREQ_CALI_AUTORST_TH_LOW	**Low period calibration threshold to trigger autoreset** Enable 0x758[15].

112205A0 CLK_AUDDIV_0 Audio Clock Selection Register 0 770000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	apll2_ck_div0				apll1_ck_div0				apll12_divb_inv	apll12_div4_inv	apll12_div3_inv	apll12_div2_inv	apll12_div1_inv	apll12_div0_inv	apll2_div0_inv	apll1_div0_inv
Type	RW				RW				RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				apll_i2s4_mck_sel	apll_i2s3_mck_sel	apll_i2s2_mck_sel	apll_i2s1_mck_sel	apll_i2s0_mck_sel	apll12_divb_pdn	apll12_div4_pdn	apll12_div3_pdn	apll12_div2_pdn	apll12_div1_pdn	apll12_div0_pdn	apll2_div0_pdn	apll1_div0_pdn
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:28	apll2_ck_div0	**Divider setting of f_faud_engen2_ck, n = [2:0]** f_faud_engen2_ck = Clock source*[1/(n+1)]
27:24	apll1_ck_div0	**Divider setting of f_faud_engen1_ck, n = [2:0]** f_faud_engen1_ck = Clock source*[1/(n+1)]
23	apll12_divb_inv	**Inverts f_faud_i2s_bck clock phase** 1: Enable phase inversion
22	apll12_div4_inv	**Inverts f_faud_i2s4_mck clock phase** 1: Enable phase inversion
21	apll12_div3_inv	**Inverts f_faud_i2s3_mck clock phase** 1: Enable phase inversion
20	apll12_div2_inv	**Inverts f_faud_i2s2_mck clock phase** 1: Enable phase inversion
19	apll12_div1_inv	**Inverts f_faud_i2s1_mck clock phase** 1: Enable phase inversion
18	apll12_div0_inv	**Inverts f_faud_i2s0_mck clock phase**

Bit(s)	Name	Description
		1: Enable phase inversion
17	apll2_div0_inv	**Inverts f_faud_engen2_ck clock phase** 1: Enable phase inversion
16	apll1_div0_inv	**Inverts f_faud_engen1_ck clock phase** 1: Enable phase inversion
12	apll_i2s4_mck_sel	**Selects hf_faud_i2s4_mck clock mux** 0: From hf_faud_1_ck 1: From hf_faud_2_ck
11	apll_i2s3_mck_sel	**Selects hf_faud_i2s3_mck clock mux** 0: From hf_faud_1_ck 1: From hf_faud_2_ck
10	apll_i2s2_mck_sel	**Selects hf_faud_i2s2_mck clock mux** 0: From hf_faud_1_ck 1: From hf_faud_2_ck
9	apll_i2s1_mck_sel	**Selects hf_faud_i2s1_mck clock mux** 0: From hf_faud_1_ck 1: From hf_faud_2_ck
8	apll_i2s0_mck_sel	**Selects hf_faud_i2s0_mck clock mux** 0: From hf_faud_1_ck 1: From hf_faud_2_ck
7	apll12_divb_pdn	**Powers down apll12_divb divider** 1: Enable power-down
6	apll12_div4_pdn	**Powers down apll12_div4 divider** 1: Enable power-down
5	apll12_div3_pdn	**Powers down apll12_div3 divider** 1: Enable power-down
4	apll12_div2_pdn	**Powers down apll12_div2 divider** 1: Enable power-down
3	apll12_div1_pdn	**Powers down apll12_div1 divider** 1: Enable power-down
2	apll12_div0_pdn	**Powers down apll12_div0 divider** 1: Enable power-down
1	apll2_div0_pdn	**Powers down apll2_div0 divider** 1: Enable power-down
0	apll1_div0_pdn	**Powers down apll1_div0 divider** 1: Enable power-down

112205A4 CLK_AUDDIV_1 Audio Clock Selection Register 1 07070707

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	apll12_ck_div3								apll12_ck_div2							
Type	RW								RW							
Reset	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	apll12_ck_div1								apll12_ck_div0							
Type	RW								RW							
Reset	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1

Bit(s)	Name	Description
31:24	apll12_ck_div3	**Divider setting of f_faud_i2s3_mck, n = [6:0]** f_faud_i2s3_mck = Clock source*[1/(n+1)]
23:16	apll12_ck_div2	**Divider setting of f_faud_i2s2_mck, n = [6:0]** f_faud_i2s2_mck = Clock source*[1/(n+1)]
15:8	apll12_ck_div1	**Divider setting of f_faud_i2s1_mck, n = [6:0]**

Bit(s)	Name	Description
7:0	apll12_ck_div0	f_faud_i2s1_mck = Clock source*[1/(n+1)] **Divider setting of f_faud_i2s0_mck, n = [6:0]** f_faud_i2s0_mck = Clock source*[1/(n+1)]

112205A8 CLK_AUDDIV_2 **Audio Clock Selection Register 2** **00000707**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	apll12_ck_divb								apll12_ck_div4							
Type	RW								RW							
Reset	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1

Bit(s)	Name	Description
31:16	Reserved	**Reserved**
15:8	apll12_ck_divb	**Divider setting of f_faud_i2s_bck, n = [6:0]** f_faud_i2s_bck = Clock source*[1/(n+1)]
7:0	apll12_ck_div4	**Divider setting of f_faud_i2s4_mck, n = [6:0]** f_faud_i2s4_mck = Clock source*[1/(n+1)]

112205AC CLK_AUDDIV_3 **Audio Clock Selection Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	Reserved	Reserved

11220150 AFE_DMA_CTL **AFE DMA Selection Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						AFE_DMA_SEL	AFE_DMA_SIZE									AFE_DMA_ON
Type						RW	RW									RW
Reset						0	0	0								0

Bit(s)	Name	Description
10	AFE_DMA_SEL	0: DL1 1: DL2
9:8	AFE_DMA_SIZE	0: 8x4 bytes 1: 16x4 bytes 2: 32x4 bytes 3: 64x4 bytes
0	AFE_DMA_ON	0: Off 1: On

11220154 AFE_DMA_MON0 AFE DMA Monitor 0 Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REQ_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACK_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:16	REQ_CNT	
15:0	ACK_CNT	

11220158 AFE_DMA_MON1 AFE DMA Monitor 1 Regsiter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DMA_WPTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL_CUR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	AFE_DMA_WPTR	
15:0	AFE_DL_CUR	

112203E0 AFE_IRQ7_MCU_CNT_MON AFE IRQ7 MCU Count Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ7_CNT_MON	
Type															RU	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	AFE_IRQ7_CNT_MON															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:0	AFE_IRQ7_CNT_MON	**Monitors the counter value for IRQ7 according toIRQ7_MODE** The IRQ7 counter in AFE will count down from AFE_IRQ_MCU_CNT7.

112203E4 AFE_IRQ_MCU_CNT3 — AFE IRQ3 MCU Counter Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ_MCU_CNT3	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ_MCU_CNT3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:0	AFE_IRQ_MCU_CNT3	**Sets up the counter value for IRQ1 according to IRQ1_MODE** The IRQ3 counter in AFE will count down from AFE_IRQ_MCU_CNT3 and set up IRQ3 while IRQ3 counter reaches 1. Therefore, the maximum IRQ time for IRQ3 at 48kHz mode is 5s.

112203E8 AFE_IRQ_MCU_CNT4 — AFE IRQ4 MCU Counter Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ_MCU_CNT4	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ_MCU_CNT4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:0	AFE_IRQ_MCU_CNT4	**Sets up the counter value for IRQ4 according to IRQ4_MODE** The IRQ4 counter in AFE will count down from AFE_IRQ_MCU_CNT4 and set up IRQ4 while IRQ4 counter reaches 1. Therefore, the maximum IRQ time for IRQ4 at 48kHz mode is 5s.

11220398 AFE_IRQ3_MCU_CNT_MON AFE IRQ3 MCU Count Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ3_CNT_MON	
Type															RU	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ3_CNT_MON															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:0	AFE_IRQ3_CNT_MON	**Monitors the counter value for IRQ3 according toIRQ3_MODE** The IRQ3 counter in AFE will count down from AFE_IRQ_MCU_CNT3.

1122039C AFE_IRQ4_MCU_CNT_MON AFE IRQ4 MCU Count Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ4_CNT_MON	
Type															RU	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ4_CNT_MON															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:0	AFE_IRQ4_CNT_MON	**Monitors the counter value for IRQ4 according toIRQ4_MODE** The IRQ4 counter in AFE will count down from AFE_IRQ_MCU_CNT4.

112205C8 AUDIO_TOP_DBG_CON Audio Top IP Debug Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															ahb_slv_mux_err_flag_en	md32_apb_err_flag_en
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	ahb_slv_mux_err_flag_en	Enables AHB slave mux debug outputs
0	md32_apb_err_flag_en	Enables MD32 APB freq bridge debug outputs

112205CC AUDIO_TOP_DBG_MON0 **Audio Top IP Debug Monitor 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ahb_slv_mux_err_decerr	ahb_slv_mux_err_rw	ahb_slv_mux_idle	md32_bridge_idle_s	md32_bridge_idle_m	md32_apb_err_timeout
Type											RU	RU	RU	RU	RU	RU
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5	ahb_slv_mux_err_decerr	AHB slave mux decoding error
4	ahb_slv_mux_err_rw	AHB slave mux read or write error
3	ahb_slv_mux_idle	AHB slave mux idle
2	md32_bridge_idle_s	MD32 AHB freq bridge slave idle
1	md32_bridge_idle_m	MD32 AHB freq bridge master idle
0	md32_apb_err_timeout	MD32 APB freq bridge timeout error

112205D0 AUDIO_TOP_DBG_MON1 **Audio Top IP Debug Monitor 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ahb_slv_mux_err_addr															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ahb_slv_mux_err_addr															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ahb_slv_mux_err_addr	AHB slave mux error address

112205D4 AUDIO_TOP_DBG_MON2 **Audio Top IP Debug Monitor 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	md32_apb_err_addr															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	md32_apb_err_addr															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	md32_apb_err_addr	MD32 APB freq bridge error address

11220800 AFE_GENERAL_REG0 Audio General Purpose Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_general_rego															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_general_rego															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_general_rego	General purpose register 0

11220804 AFE_GENERAL_REG1 Audio General Purpose Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_general_reg1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_general_reg1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_general_reg1	General purpose register 1

11220808 AFE_GENERAL_REG2 Audio General Purpose Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_general_reg2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_general_reg2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_general_reg2	General purpose register 2

1122080C AFE_GENERAL_REG3 Audio General Purpose Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_general_reg3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_general_reg3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_general_reg3	General purpose register 3

11220810 AFE_GENERAL_REG4 Audio General Purpose Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_general_reg4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_general_reg4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_general_reg4	General purpose register 4

11220814 AFE_GENERAL_REG5 Audio General Purpose Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_general_reg5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_general_reg5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_general_reg5	General purpose register 5

11220818 AFE_GENERA Audio General Purpose Register 00000000

L_REG6 **6**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_general_reg6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_general_reg6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_general_reg6	General purpose register 6

1122081C **AFE_GENERAL_REG7** **Audio General Purpose Register 7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_general_reg7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_general_reg7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_general_reg7	General purpose register 7

11220820 **AFE_GENERAL_REG8** **Audio General Purpose Register 8** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_general_reg8															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_general_reg8															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_general_reg8	General purpose register 8

11220824 **AFE_GENERAL_REG9** **Audio General Purpose Register 9** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_general_reg9															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_general_reg9															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_general_reg9	General purpose register 9

11220828 AFE_GENERAL_REG10 Audio General Purpose Register 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_general_reg10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_general_reg10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_general_reg10	General purpose register 10

1122082C AFE_GENERAL_REG11 Audio General Purpose Register 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_general_reg11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_general_reg11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_general_reg11	General purpose register 11

11220830 AFE_GENERAL_REG12 Audio General Purpose Register 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_general_reg12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_general_reg12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_general_reg12	General purpose register 12

11220834 AFE_GENERAL_REG13 Audio General Purpose Register 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_general_reg13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_general_reg13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_general_reg13	General purpose register 13

11220838 AFE_GENERAL_REG14 Audio General Purpose Register 14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_general_reg14															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_general_reg14															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_general_reg14	General purpose register 14

1122083C AFE_GENERAL_REG15 Audio General Purpose Register 15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_general_reg15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_general_reg15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_general_reg15	General purpose register 15

112203BC AFE_IRQ_MC AFE IRQ5 MCU Counter 00000000

U_CNT5 **Register**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ_MCU_CNT5	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ_MCU_CNT5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:0	AFE_IRQ_MCU_CNT5	**Sets up the counter value for IRQ5 according to IRQ5_MODE** The IRQ5 counter in AFE will count down from AFE_IRQ_MCU_CNT5 and set up IRQ5 while IRQ5 counter reaches 1. Therefore, the maximum IRQ time for IRQ5 at 48kHz mode is 5s.

112203CC **AFE_IRQ5_MCU_CNT_MON** **AFE IRQ5 MCU Count Monitor Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ5_CNT_MON	
Type															RU	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ5_CNT_MON															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:0	AFE_IRQ5_CNT_MON	**Monitors the counter value for IRQ5 according toIRQ5_MODE** The IRQ5 counter in AFE will count down from AFE_IRQ_MCU_CNT5.

11220548 **AFE_TDM_CON1** **AFE TDM Config 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LRCK_TDM_WIDTH											DAC_BIT_NUM				
Type	RW											RW				
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			CHANNEL_BCK_CYCLES		CHANNEL_NUM		WLEN					LEFT_ALIGN	DELAY_DATA	LRCK_INVERSE	BCK_INVERSE	TDM_EN
Type			RW		RW		RW					RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
31:24	LRCK_TDM_WIDTH	**Sets up LRCK width as number of BCK cycles** 0: LRCK is 1 BCK cycle 1: LRCK is 2 BCK cycles 2: LRCK is 3 BCK cycles 254: LRCK is 255 BCK cycles
20:16	DAC_BIT_NUM	**Specifies sample bit width for RJ format** This format is not available for TDM.
13:12	CHANNEL_BCK_CYCLES	**Selects number of BCK cycles for each channel** 0: 16 BCK cycles 1: 24 BCK cycles 2: 32 BCK cycles
11:10	CHANNEL_NUM	**Selects number of channels for each sdata** 0: 2 channels 1: 4 channels 2: 8 channels
9:8	WLEN	**Data word length** 1: 16 bits 2: 32 bits
4	LEFT_ALIGN	**Set up this bit for EIAJ & I2S mode** 0: Sample is not aligned to MSB bit. 1: Sample is aligned to MSB bit.
3	DELAY_DATA	**Set up this bit for I2S mode** 0: MSB bit data are 0 BCK cycle behind LRCK trigger edge. Set for EIAJ mode. 1: MSB bit data are 1 BCK cycle behind LRCK trigger edge. Set for I2S mode.
2	LRCK_INVERSE	**Inverts TDM LRCK** 0: Does not invert LRCK 1: Invert LRCK
1	BCK_INVERSE	**Inverts TDM BCK** 0: Does not invert BCK 1: Invert BCK
0	TDM_EN	**Enables TDM** Enable this bit when all other Configurations are set, including sampling rate. 0: Disable TDM 1: Enable TDM

1122054C AFE_TDM_CON2 **AFE TDM Config 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDM_ FIX_ VALU E									TDM_I2S_L OOPBACK_C H		TDM_ I2S_ LOOP BACK				TDM_ FIX_ VALU E_SE L
Type	RW									RW		RW				RW
Reset	0	0	0	0	0	0	0	0		0	0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ST_CH_PAIR_SO UT3				ST_CH_PAIR_SO UT2				ST_CH_PAIR_SO UT1				ST_CH_PAIR_SO UT0		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
31:24	TDM_FIX_VALUE	**Sets up fix value sent on TDM TX**
22:21	TDM_I2S_LOOPBACK_CH	**Selects HDMI sdatax for loopback test** 00: Select hdmi_sdata0 for loopback test 01: Select hdmi_sdata1 for loopback test 10: Select hdmi_sdata2 for loopback test 11: Select hdmi_sdata3 for loopback test
20	TDM_I2S_LOOPBACK	**Sets TDM to I2S path** 0: Disable TDM to I2S path 1: Enable TDM to I2S path
16	TDM_FIX_VALUE_SEL	**TDM enable sends fix value on TX.** 0: Disable fix value on TX 1: Enable fix value on TX
14:12	ST_CH_PAIR_SOUT3	**Sets up start channels for SOUT3** The remaining channels are sent in assending order. 0: Channels sent are O30, O31, O32, O33, O34, O35, O36, O37. 1: Channels sent are O32, O33, O34, O35, O36, O37, 0. 2. Channels sent are O34, O35, O36, O37, 0. 3: Channels sent are O36, O37, 0. 4: Channel sent is 0. 0: Channel starts from O30/O31. 1: Channel starts from O32/O33. 2: Channel starts from O34/O35. 3: Channel starts from O36/O37. 4: Channel data is 0. 5: Channel data is 0. 6: Channel data is 0. 7: Channel data is 0.
10:8	ST_CH_PAIR_SOUT2	**Sets up start channels for SOUT2** The remaining channels are sent in assending order. 0: Channels sent are O30, O31, O32, O33, O34, O35, O36, O37. 1: Channels sent are O32, O33, O34, O35, O36, O37, 0. 2. Channels sent are O34, O35, O36, O37, 0. 3: Channels sent are O36, O37, 0. 4: Channel sent is 0. 0: Channel starts from O30/O31. 1: Channel starts from O32/O33. 2: Channel starts from O34/O35. 3: Channel starts from O36/O37. 4: Channel data is 0. 5: Channel data is 0. 6: Channel data is 0. 7: Channel data is 0.
6:4	ST_CH_PAIR_SOUT1	**Sets up start channels for SOUT1** The remaining channels are sent in assending order. 0: Channels sent are O30, O31, O32, O33, O34, O35, O36, O37. 1: Channels sent are O32, O33, O34, O35, O36, O37, 0. 2. Channels sent are O34, O35, O36, O37, 0. 3: Channels sent are O36, O37, 0. 4: Channel sent is 0. 0: Channel starts from O30/O31. 1: Channel starts from O32/O33. 2: Channel starts from O34/O35. 3: Channel starts from O36/O37. 4: Channel data is 0. 5: Channel data is 0. 6: Channel data is 0. 7: Channel data is 0.

Bit(s)	Name	Description
2:0	ST_CH_PAIR_SOUT0	**Sets up start channels for SOUT0** The remaining channels are sent in assending order. 0: Channels sent are O30, O31, O32, O33, O34, O35, O36, O37. 1: Channels sent are O32, O33, O34, O35, O36, O37, 0. 2. Channels sent are O34, O35, O36, O37, 0. 3: Channels sent are O36, O37, 0. 4: Channel sent is 0. 0: Channel starts from O30/O31. 1: Channel starts from O32/O33. 2: Channel starts from O34/O35. 3: Channel starts from O36/O37. 4: Channel data is 0. 5: Channel data is 0. 6: Channel data is 0. 7: Channel data is 0.

11220370 AFE_HDMI_OUT_CON0 AFE HDMI_OUT Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								AFE_HDMI_OUT_ON_RETM	AFE_HDMI_OUT_CH_NUM						AFE_HDMI_OUT_BIT_WIDTH	AFE_HDMI_OUT_ON
Type								RO	RW						RW	RW
Reset								0	0	0	0	0			0	0

Bit(s)	Name	Description
8	AFE_HDMI_OUT_ON_RETM	
7:4	AFE_HDMI_OUT_CH_NUM	**Specifies number of output channels to be enabled on I30~I37** Range: 1 ~ 8 0000: Enable I30 0001: Enable I30 0010: Enable I30~I31 0011: Enable I30~I32 0100: Enable I30~I33 0101: Enable I30~I34 0110: Enable I30~I35 0111: Enable I30~I36 1000: Enable I30~I37
1	AFE_HDMI_OUT_BIT_WIDTH	**Controls input data bit-width** 0: 16-bit 1: 32-bit
0	AFE_HDMI_OUT_ON	**Enables HDMI output**

11220374 AFE_HDMI_B AFE HDMI Base Address 00000000

ASE **Register**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_HDMI_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_HDMI_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	AFE_HDMI_BASE	**Base address of HDMI input in master mode** Always set AFE_HDMI_BASE[2:0] = 3'h0 for the convenience of hardware implementation.

11220378 **AFE_HDMI_CUR** **AFE HDMI Cursor Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_HDMI_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_HDMI_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AFE_HDMI_CUR	Indicates the current address of HDMI input buffer

1122037C **AFE_HDMI_END** **AFE HDMI End Address Register** **00000007**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_HDMI_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_HDMI_END													AFE_HDMI_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Name	Description
31:3	AFE_HDMI_END	**End address of HDMI input in master mode** Always set AFE_HDMI_END[2:0] = 3'h7 for the convenience of hardware implementation.
2:0	AFE_HDMI_END_LSB	

11220390 **AFE_HDMI_C** **AFE HDMI Output Connection** **00000000**

ONNO Control Register 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved 1	Reserved	O_39_CFG			O_38_CFG			O37_CFG			O36_CFG			O35_CFG	
Type	RW	RW	RW			RW			RW			RW			RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	O35_CFG	O34_CFG			O33_CFG			O32_CFG			O31_CFG			O30_CFG		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	Reserved1	
30	Reserved	
29:27	O_39_CFG	**These bits control the o_39 data.** 000: Select I30 001: Select I31 010: Select I32 011: Select I33 100: Select I34 101: Select I35 110: Select I36 111: Select I37
26:24	O_38_CFG	**These bits control the o_38 data.** 000: Select I30 001: Select I31 010: Select I32 011: Select I33 100: Select I34 101: Select I35 110: Select I36 111: Select I37
23:21	O37_CFG	**Selects input source to O37** I30 ~ I37 000: Select I30 001: Select I31 010: Select I32 011: Select I33 100: Select I34 101: Select I35 110: Select I36 111: Select I37
20:18	O36_CFG	**Selects input source to O36** I30 ~ I37 000: Select I30 001: Select I31 010: Select I32 011: Select I33 100: Select I34 101: Select I35 110: Select I36 111: Select I37
17:15	O35_CFG	**Selects input source to O35** I30 ~ I37 000: Select I30

Bit(s)	Name	Description
		001: Select I31 010: Select I32 011: Select I33 100: Select I34 101: Select I35 110: Select I36 111: Select I37
14:12	O34_CFG	**Selects input source to O34** I30 ~ I37 000: Select I30 001: Select I31 010: Select I32 011: Select I33 100: Select I34 101: Select I35 110: Select I36 111: Select I37
11:9	O33_CFG	**Selects input source to O33** I30 ~ I37 000: Select I30 001: Select I31 010: Select I32 011: Select I33 100: Select I34 101: Select I35 110: Select I36 111: Select I37
8:6	O32_CFG	**Selects input source to O32** I30 ~ I37 000: Select I30 001: Select I31 010: Select I32 011: Select I33 100: Select I34 101: Select I35 110: Select I36 111: Select I37
5:3	O31_CFG	**Selects input source to O31** I30 ~ I37 000: Select I30 001: Select I31 010: Select I32 011: Select I33 100: Select I34 101: Select I35 110: Select I36 111: Select I37
2:0	O30_CFG	**Selects input source to O30** I30 ~ I37 000: Select I30 001: Select I31 010: Select I32 011: Select I33 100: Select I34 101: Select I35 110: Select I36

Bit(s)	Name	Description
		111: Select I37

11220840 AFE_CBIP_CFG0 **00000037**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CBIP_ASYNC_MST_RG_FIFO_THRE		CBIP_ASYNC_MST_postwrite_dis		CBIP_ASYNC_SLV_RG_FIFO_THRE		CBIP_ASYNC_SLV_postwrite_dis		CBIP_SLV_DECODER_error_flag_en	CBIP_SLV_DECODER_reg_slave_way_en		CBIP_SLV_MUX_error_flag_en	CBIP_SLV_MUX_reg_slave_way_en	CBIP_SLV_MUX_reg_layer_way_en	
Type		RW		RW		RW		RW		RW	RW		RW	RW	RW	
Reset		0	0	0		0	0	0		0	1	1	0	1	1	1

Bit(s)	Name	Description
14:13	CBIP_ASYNC_MST_RG_FIFO_THRE	
12	CBIP_ASYNC_MST_postwrite_dis	
10:9	CBIP_ASYNC_SLV_RG_FIFO_THRE	
8	CBIP_ASYNC_SLV_postwrite_dis	
6	CBIP_SLV_DECODER_error_flag_en	
5:4	CBIP_SLV_DECODER_reg_slave_way_en	
3	CBIP_SLV_MUX_error_flag_en	
2	CBIP_SLV_MUX_reg_slave_way_en	
1:0	CBIP_SLV_MUX_reg_layer_way_en	

11220844 AFE_CBIP_MON0 **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CBIP_SLV_DECODER_err_domain	CBIP_SLV_DECODER_err_id	CBIP_SLV_DECODER_err_rw	CBIP_SLV_DECODER_err_decerr	CBIP_SLV_DECODER_ctrl_update			CBIP_SLV_MUX_err_domain	CBIP_SLV_MUX_err_id	CBIP_SLV_MUX_err_rw	CBIP_SLV_MUX_err_decerr	CBIP_SLV_MUX_ctrl_update_status	

								_status								
Type				RO	RO	RO	RO	RO			RO	RO	RO	RO	RO	
Reset				0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
12	CBIP_SLV_DECODER_err_domain	
11	CBIP_SLV_DECODER_err_id	
10	CBIP_SLV_DECODER_err_rw	
9	CBIP_SLV_DECODER_err_decerr	
8	CBIP_SLV_DECODER_ctrl_update_status	
5	CBIP_SLV_MUX_err_domain	
4	CBIP_SLV_MUX_err_id	
3	CBIP_SLV_MUX_err_rw	
2	CBIP_SLV_MUX_err_decerr	
1:0	CBIP_SLV_MUX_ctrl_update_status	

11220848 AFE_CBIP_SLV_MUX_MON **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CBIP_SLV_MUX_err_addr															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CBIP_SLV_MUX_err_addr															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CBIP_SLV_MUX_err_addr	

1122084C AFE_CBIP_SLV_DECODER_MON0 **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CBIP_SLV_DECODER_err_addr															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CBIP_SLV_DECODER_err_addr															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CBIP_SLV_DECODER_err_addr	

112204F0 AFE_SRAM_DELSEL_CON0 **Memory DELSEL Control 0** **AAAAAAAA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_src_4ch_mbist_delsel_1				afe_src_4ch_mbist_delsel_0				afe_src_mbist_del sel_1				afe_src_mbist_del sel_0			
Type	RW				RW				RW				RW			
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_side_tone_coeff_mbist_delsel				afe_side_tone_mbist_delsel				afe_dl_buf_mbist_delsel				afe_ul_buf_mbist_delsel			
Type	RW				RW				RW				RW			
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Name	Description
31:28	afe_src_4ch_mbist_delsel_1	Controls DELSEL for SRC 4ch IIR coefficient memory
27:24	afe_src_4ch_mbist_delsel_	Controls DELSEL for SRC 4ch history memory
23:20	afe_src_mbist_delsel_1	Controls DELSEL for SRC IIR coefficient memory
19:16	afe_src_mbist_delsel_0	Controls DELSEL for SRC history memory
15:12	afe_side_tone_coeff_mbist_delsel	Controls DELSEL for sidetone coefficient memory
11:8	afe_side_tone_mbist_delsel	Controls DELSEL for sidetone memory
7:4	afe_dl_buf_mbist_delsel	Controls DELSEL for DL memory
3:0	afe_ul_buf_mbist_delsel	Controls DELSEL for UL coefficient memory

112204F4 AFE_SRAM_DELSEL_CON1 **Memory DELSEL Control 1** **00000AAA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					afe_ul_hires_buf_mbist_delsel				afe_memif_mbist_delsel_0				afe_memif_mbist_delsel_1			
Type					RW				RW				RW			
Reset					1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Name	Description
11:8	afe_ul_hires_buf_mbist_delsel	Controls DELSEL for UL high resolution coefficient memory
7:4	afe_memif_mbist_delsel_0	Controls DELSEL for MEMIF sysram memory
3:0	afe_memif_mbist_delsel_1	Controls DELSEL for MEMIF prefetch buffer memory

112201FC AFE_SINEGEN_CON_TDM **TDM SGEN control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				sgen_tdm_input_en				c_dac_en_tdm				sine_mode_tdm2	amp_div_tdm2			freq_div_tdm2

Type				RW				RW				RW	RW			RW
Reset				0				0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	freq_div_tdm2							sine_mode_tdm1	amp_div_tdm1			freq_div_tdm1				
Type	RW							RW	RW			RW				
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	sgen_tdm_input_en	**Selects afe_con_hdmi input** 0: From mem 1: From sgen
24	c_dac_en_tdm	**Enables singen** 0: Sigen off 1: Sigen on
20	sine_mode_tdm2	**Sinewave generator mute for TDM** 0: Unmute sigen 1: Mute sigen
19:17	amp_div_tdm2	**Selects sinewave generator amplitude for TDM** 0: sinewave_out/128 1: sinewave_out/64 2: sinewave_out/32 3: sinewave_out/16 4: sinewave_out/8 5: sinewave_out/4 6: sinewave_out/2 7: sinewave_out/1
16:12	freq_div_tdm2	**Selects sinewave generator frequency for TDM sampled by signal timing generator selection** 0: DC output 1: 64/1 samples/period 2: 64/2 samples/period 3: 64/3 samples/period 4: 64/4 samples/period 5: 64/5 samples/period 6: 64/6 samples/period x: 64/x samples/period 31: 64/31 samples/period
8	sine_mode_tdm1	**Sinewave generator mute for TDM** 0: Unmute sigen 1: Mute sigen
7:5	amp_div_tdm1	**Selects sinewave generator amplitude for TDM** 0: sinewave_out/128 1: sinewave_out/64 2: sinewave_out/32 3: sinewave_out/16 4: sinewave_out/8 5: sinewave_out/4 6: sinewave_out/2 7: sinewave_out/1
4:0	freq_div_tdm1	**Selects sinewave generator frequency for TDM sampled by signal timing generator selection** 0: DC output 1: 64/1 samples/period

Bit(s)	Name	Description
		2: 64/2 samples/period 3: 64/3 samples/period 4: 64/4 samples/period 5: 64/5 samples/period 6: 64/6 samples/period x: 64/x samples/period 31: 64/31 samples/period

3.14 BTIF

Module name: btif Base address: (+1100c000h)

Address	Name	Width	Register Function
1100C000	BTIF_RBR_OR_BTIF_THR	8	RX/TX Buffer Register
1100C004	BTIF_IER	8	Interrupt Enable Register
1100C008	BTIF_IIR_OR_BTIF_FIFOCTRL	8	Interrupt Identification Register or FIFO Control Register
1100C00C	BTIF_FAKELCR	8	Fake Control Register
1100C014	BTIF_LSR	8	Line Status Register
1100C048	BTIF_SLEEP_EN	8	Sleep Enable Register
1100C04C	BTIF_DMA_EN	8	DMA Enable Register
1100C054	BTIF_RTOCNT	8	RX Timeout Count
1100C060	BTIF_TRI_LVL	8	TRX FIFO Trigger Level Register
1100C064	BTIF_WAK	8	Wake-up Register
1100C068	BTIF_WAT_TIME	8	Asynchorous Timer Register
1100C06C	BTIF_HANDSHAKE	8	New Handshake Control Register
1100C070	BTIF_DEBUG_TX_FIFO_0	8	TX FIFO Address 0 Debug Register
1100C074	BTIF_DEBUG_TX_FIFO_1	8	TX FIFO Address 1 Debug Register
1100C078	BTIF_DEBUG_TX_FIFO_2	8	TX FIFO Address 2 Debug Register
1100C07C	BTIF_DEBUG_TX_FIFO_3	8	TX FIFO Address 3 Debug Register
1100C080	BTIF_DEBUG_TX_FIFO_4	8	TX FIFO Address 4 Debug Register
1100C084	BTIF_DEBUG_TX_FIFO_5	8	TX FIFO Address 5 Debug Register
1100C058	BTIF_DEBUG_TX_FIFO_6	8	TX FIFO Address 6 Debug Register
1100C08C	BTIF_DEBUG_TX_FIFO_7	8	TX FIFO Address 7 Debug Register
1100C090	BTIF_DEBUG_TX_FIFO_8	8	TX FIFO Address 8 Debug Register
1100C094	BTIF_DEBUG_TX_FIFO_9	8	TX FIFO Address 9 Debug Register
1100C098	BTIF_DEBUG_TX_FIFO_a	8	TX FIFO Address 10 Debug Register
1100C09C	BTIF_DEBUG_TX_FIFO_b	8	TX FIFO Address 11 Debug Register
1100C0A0	BTIF_DEBUG_TX_FIFO_c	8	TX FIFO Address 12 Debug Register
1100C0A4	BTIF_DEBUG_TX_FIFO_d	8	TX FIFO Address 13 Debug Register
1100C0A8	BTIF_DEBUG_TX_FIFO_e	8	TX FIFO Address 14 Debug Register
1100C0AC	BTIF_DEBUG_TX_FIFO_f	8	TX FIFO Address 15 Debug Register
1100C0B0	BTIF_DEBUG_RX_FIFO_0	8	RX FIFO Address 0 Debug Register
1100C0B4	BTIF_DEBUG_RX_	8	RX FIFO Address 1 Debug Register

Address	Name	Width	Register Function
	FIFO_1		
1100C0B8	BTIF_DEBUG_RX_FIFO_2	8	RX FIFO Address 2 Debug Register
1100C0BC	BTIF_DEBUG_RX_FIFO_3	8	RX FIFO Address 3 Debug Register
1100C0C0	BTIF_DEBUG_RX_FIFO_4	8	RX FIFO Address 4 Debug Register
1100C0C4	BTIF_DEBUG_RX_FIFO_5	8	RX FIFO Address 5 Debug Register
1100C0C8	BTIF_DEBUG_RX_FIFO_6	8	RX FIFO Address 6 Debug Register
1100C0CC	BTIF_DEBUG_RX_FIFO_7	8	RX FIFO Address 7 Debug Register
1100C0D0	BTIF_DEBUG_TX_PTR	8	TX FIFO Pointer Debug Register
1100C0D4	BTIF_DEBUG_RX_PTR	8	RX FIFO Pointer Debug Register

1100C000 BTIF_RBR_OR_BTIF_THR RX/TX Buffer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_RBR_OR_BTIF_THR							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	BTIF_RBR_OR_BTIF_THR	BTIF_RBR_OR_BTIF_THR	**The received data can be read by accessing this register.** The data to be transmitted is written to this register and sent to the PC via serial communication. This register will be valid only when BTIF_FAKELCR[7] (0x0C) = 0.

1100C004 BTIF_IER Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RXFEN	TXEEN
Type															RU	RU
Reset															0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
1	**RXFEN**	RXFEN	**Enables RX full and timeout interrupt** This register will be valid only when BTIF_FAKELCR[7] = 0. 0: No interrupt will be generated if the RX buffer contains data or timeout. 1: An interrupt will be generated if the RX buffer contains data or timeout.
0	**TXEEN**	TXEEN	**Enables TX empty interrupt** This register will be valid only when BTIF_FAKELCR[7] = 0. 0: No interrupt will be generated if the TX holding register is empty. 1: An interrupt will bes generated if the TX holding register is empty.

1100C008 BTIF_IIR_OR_BTIF_FIFOCTRL **Interrupt Identification Register or FIFO Control Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BTIF_IIR_OR_BTIF_FIFOCTRL			
Type													RW			
Reset													0	0	0	1

Bit(s)	Mnemonic	Name	Description
3:0	**BTIF_IIR_OR_BTIF_FIFOCTRL**	BTIF_IIR_OR_BTIF_FIFOCTRL	**Interrupt identification** This register will be valid only when BTIF_FAKELCR (0x0C) = 0xBF. Bit 1: Clear Transmit FIFO Bit 2: Clear Receive FIFO This register will be valid only when BTIF_FAKELCR (0x0C) is not equal to 0xBF. 4'h1: No interrupt pending 4'h4: RX data received 4'hc: RX data timeout 4'h2 :TX holding register empty CLRT: 0: Leave TX FIFO intact 1: Clear all bytes in TX FIFO CLRR: 0: Leave RX FIFO intact 1: Clear all bytes in RX FIFO

1100C00C BTIF_FAKELCR **Fake Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_FAKELCR							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_FAKELCR**	BTIF_FAKELCR	**Synchronizes SW control method of UART** When FAKELCR[7] = 1, RBR(0x00), THR(0x00) and IER(0x04) will not be readable/writable. When FAKELCR = 0xBF, RBR(0x00), THR(0x00), IER(0x04), IIR(0x08) and LSR(0x14) will not be readable/writable.

1100C014 BTIF_LSR **Line Status Register** **00000060**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										TEMT	THRE					DR
Type										RU	RU					RU
Reset										1	1					0

Bit(s)	Mnemonic	Name	Description
6	**TEMT**	TEMT	**TX holding register is empty** Readable when LCR != 0xBF. 0: Empty conditions are not met. 1: This bit is set when TX holding register are empty.
5	**THRE**	THRE	**Indicates if TX FIFO is reduced to its trigger level** Readable when LCR != 0xBF. 0: Reset whenever the contents of TX FIFO are more than its trigger level (FIFOs are enabled) 1: Set whenever the contents of TX FIFO are reduced to its trigger level (FIFOs are enabled)
0	**DR**	DR	**Data ready** Readable when LCR != 0xBF. 0: Cleared by reading RX buffer 1: Set by RX buffer becoming full

1100C048 BTIF_SLEEP_EN **Sleep Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BTIF_SLEEP_EN

Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**BTIF_SLEEP_EN**	BTIF_SLEEP_EN	**For sleep mode issue** 0: Does not deal with sleep mode indication signal 1: Activate flow control according to software initial setting when chip enters sleep mode. Release hardware flow when chip wakes up.

1100C04C BTIF_DMA_EN **DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														TO_CNT_AUTORST	TX_DMA_EN	RX_DMA_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	**TO_CNT_AUTORST**	TO_CNT_AUTORST	**Timeout counter auto reset register** 0: After RX timeout happens, SW should reset the interrupt by reading BTIF 0x4C. 1: The timeout counter will be auto reset.
1	**TX_DMA_EN**	TX_DMA_EN	**TX_DMA mechanism enable signal** 0: Does not use DMA in TX 1: Use DMA in TX. When this register is enabled, the flow control will be based on the DMA threshold and generate a timeout interrupt for DMA.
0	**RX_DMA_EN**	RX_DMA_EN	**RX_DMA mechanism enable signal** 0: Does not use DMA in RX 1: Use DMA in RX. When this register is enabled, the flow control will be based on the DMA threshold and generate a timeout interrupt.

1100C054 BTIF_RTOCNT **RX Timeout Count** **00000040**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_RTOCNT							
Type									RW							
Reset									0	1	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_RTOCNT**	BTIF_RTOCNT	**Used for RX timeout interrupt** The RX timeout interrupt will be generated when: 1. RXRTOEN (0x04[0]) is set to 1. 2. RX buffer is empty. 3. The most recent character was received longer than (RTOCNT*bclk period*4).

1100C060 BTIF_TRI_LVL TRX FIFO Trigger Level Register 0000005A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_LOOP	RX_TRI_LVL			TX_TRI_LVL			
Type									RW	RW			RW			
Reset									0	1	0	1	1	0	1	0

Bit(s)	Mnemonic	Name	Description
7	**BTIF_LOOP**	BTIF_LOOP	**Enables BTIF loop back mode** The data output from TX will be received by RX.
6:4	**RX_TRI_LVL**	RX_TRI_LVL	**Used for RX FIFO trigger threshold** An RX trigger interrupt (IIR(0x08]) = 4) might be set if the data in the RXFIFO are more than RX_TRI_LVL. The output flow control signal will be set if the data in the RXFIFO are more than RX_TRI_LVL.
3:0	**TX_TRI_LVL**	TX_TRI_LVL	**Used for TX FIFO trigger threshold** THRE(0x14[5]) will be set if the data in TXFIFO are less than TX_TRI_LVL.

1100C064 BTIF_WAK Wake-up Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BTIF_WAK
Type																RW
Reset																1

Bit(s)	Mnemonic	Name	Description
0	**BTIF_WAK**	BTIF_WAK	Wakes up BTIF module

1100C068 BTIF_WAT_TIME Asynchorous Timer Register 00000012

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											WAT_TIME_2			WAT_TIME_1		
Type											RW			RW		
Reset											0	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
5:3	**WAT_TIME_2**	WAT_TIME_2	**Scond level of wait time** WAT_TIME_2 cannot be smaller than 0x2.
2:0	**WAT_TIME_1**	WAT_TIME_1	**First level of wait time** WAT_TIME_1 cannot be smaller than 0x2.

1100C06C BTIF_HANDSHAKE **New Handshake Control Register** **00000003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RTO_EXT	HIGH_SPEED_EN	HANDSHAKE_EN
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Mnemonic	Name	Description
2	**RTO_EXT**	RTO_EXT	Extends value of RX timeout counter (16*rto_time)
1	**HIGH_SPEED_EN**	HIGH_SPEED_EN	Enables high speed mode
0	**HANDSHAKE_EN**	HANDSHAKE_EN	Enables handshake mode

1100C070 BTIF_DEBUG_TX_FIFO_0 **TX FIFO Address 0 Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_TX_FIFO_0							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_TX_FIFO_0**	BTIF_DEBUG_TX_FIFO_0	Debug TX FIFO address 0

1100C074 BTIF_DEBUG_TX_FIFO_1 TX FIFO Address 1 Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_TX_FIFO_1							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_TX_FIFO_1**	BTIF_DEBUG_TX_FIFO_1	Debug TX FIFO address 1

1100C078 BTIF_DEBUG_TX_FIFO_2 TX FIFO Address 2 Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_TX_FIFO_2							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_TX_FIFO_2**	BTIF_DEBUG_TX_FIFO_2	Debug TX FIFO address 2

1100C07C BTIF_DEBUG_TX_FIFO_3 TX FIFO Address 3 Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_TX_FIFO_3							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_TX_FIFO_3**	BTIF_DEBUG_TX_FIFO_3	Debug TX FIFO address 3

1100C080 BTIF_DEBUG_TX_FIFO_4 — TX FIFO Address 4 Debug Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_TX_FIFO_4							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_TX_FIFO_4**	BTIF_DEBUG_TX_FIFO_4	Debug TX FIFO address 4

1100C084 BTIF_DEBUG_TX_FIFO_5 — TX FIFO Address 5 Debug Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_TX_FIFO_5							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_TX_FIFO_5**	BTIF_DEBUG_TX_FIFO_5	Debug TX FIFO address 5

1100C058 BTIF_DEBUG_TX_FIFO_6 — TX FIFO Address 6 Debug Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_TX_FIFO_6							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_TX_FIFO_6**	BTIF_DEBUG_TX_FIFO_6	Debug TX FIFO address 6

1100C08C BTIF_DEBUG — TX FIFO Address 7 Debug — 00000000

_TX_FIFO_7 Register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_TX_FIFO_7							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	BTIF_DEBUG_TX_FIFO_7	BTIF_DEBUG_TX_FIFO_7	Debug TX FIFO address 7

1100C090 BTIF_DEBUG_TX_FIFO_8 TX FIFO Address 8 Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_TX_FIFO_8							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	BTIF_DEBUG_TX_FIFO_8	BTIF_DEBUG_TX_FIFO_8	Debug TX FIFO address 8

1100C094 BTIF_DEBUG_TX_FIFO_9 TX FIFO Address 9 Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_TX_FIFO_9							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	BTIF_DEBUG_TX_FIFO_9	BTIF_DEBUG_TX_FIFO_9	Debug TX FIFO address 9

1100C098 BTIF_DEBUG_TX_FIFO_a TX FIFO Address 10 Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_TX_FIFO_a							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_TX_FIFO_a**	BTIF_DEBUG_TX_FIFO_a	Debug TX FIFO address 10

1100C09C BTIF_DEBUG_TX_FIFO_b **TX FIFO Address 11 Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_TX_FIFO_b							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_TX_FIFO_b**	BTIF_DEBUG_TX_FIFO_b	Debug TX FIFO address 11

1100C0A0 BTIF_DEBUG_TX_FIFO_c **TX FIFO Address 12 Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_TX_FIFO_c							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_TX_FIFO_c**	BTIF_DEBUG_TX_FIFO_c	Debug TX FIFO address 12

1100C0A4 BTIF_DEBUG_TX_FIFO_d **TX FIFO Address 13 Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_TX_FIFO_d							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_TX_FIFO_d**	BTIF_DEBUG_TX_FIFO_d	Debug TX FIFO address 13

1100C0A8 BTIF_DEBUG_TX_FIFO_e **TX FIFO Address 14 Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_TX_FIFO_e							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_TX_FIFO_e**	BTIF_DEBUG_TX_FIFO_e	Debug TX FIFO address 14

1100C0AC BTIF_DEBUG_TX_FIFO_f **TX FIFO Address 15 Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_TX_FIFO_f							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_TX_FIFO_f**	BTIF_DEBUG_TX_FIFO_f	Debug TX FIFO address 15

1100C0B0 BTIF_DEBUG_RX_FIFO_0 **RX FIFO Address 0 Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_RX_FIFO_0							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_RX_FIFO_0**	BTIF_DEBUG_RX_FIFO_0	Debug RX FIFO address 0

1100C0B4 BTIF_DEBUG_RX_FIFO_1 — RX FIFO Address 1 Debug Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_RX_FIFO_1							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_RX_FIFO_1**	BTIF_DEBUG_RX_FIFO_1	Debug RX FIFO address 1

1100C0B8 BTIF_DEBUG_RX_FIFO_2 — RX FIFO Address 2 Debug Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_RX_FIFO_2							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_RX_FIFO_2**	BTIF_DEBUG_RX_FIFO_2	Debug RX FIFO address 2

1100C0BC BTIF_DEBUG_RX_FIFO_3 — RX FIFO Address 3 Debug Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_RX_FIFO_3							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_RX_FIFO_3**	BTIF_DEBUG_RX_FIFO_3	Debug RX FIFO address 3

1100C0C0 BTIF_DEBUG_RX_FIFO_4 **RX FIFO Address 4 Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_RX_FIFO_4							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_RX_FIFO_4**	BTIF_DEBUG_RX_FIFO_4	Debug RX FIFO address 4

1100C0C4 BTIF_DEBUG_RX_FIFO_5 **RX FIFO Address 5 Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_RX_FIFO_5							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_RX_FIFO_5**	BTIF_DEBUG_RX_FIFO_5	Debug RX FIFO address 5

1100C0C8 BTIF_DEBUG_RX_FIFO_6 **RX FIFO Address 6 Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_RX_FIFO_6							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_RX_FIFO_6**	BTIF_DEBUG_RX_FIFO_6	Debug RX FIFO address 6

1100C0CC BTIF_DEBUG_RX_FIFO_7 **RX FIFO Address 7 Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_RX_FIFO_7							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_RX_FIFO_7**	BTIF_DEBUG_RX_FIFO_7	Debug RX FIFO address 7

1100C0D0 BTIF_DEBUG_TX_PTR **TX FIFO Pointer Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BTIF_DEBUG_TX_PTR							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_TX_PTR**	BTIF_DEBUG_TX_PTR	**Debug TX FIFO pointer** bit 0~3 are read poiners; bit 4~7 are writer pointers.

1100C0D4 BTIF_DEBUG_RX_PTR **RX FIFO Pointer Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name									BTIF_DEBUG_RX_PTR							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**BTIF_DEBUG_RX_PTR**	BTIF_DEBUG_RX_PTR	**Debug RX FIFO pointer** bit 0~3 are read poiners; bti 4~7 are writer pointers.

3.15 USIM

Module name: usim Base address: (+80040000h)

Address	Name	Width	Register Function
80040000	USIM_CODA_VERSION	32	USIM Version Control Register
80040010	USIM_CTRL	32	USIM Control Register
80040014	USIM_CONF	32	USIM Configuration Register
80040018	USIM_CONFSTA	32	USIM Configuration Status Register
8004001C	USIM_BRR	32	USIM Baud Rate Register
80040020	USIM_IRQEN	32	USIM Interrupt Enable Register
80040024	USIM_STS	32	USIM Interrupt Event Status Register
80040030	USIM_RETRY	32	USIM Retry Limit Register
80040034	USIM_TIDE	32	USIM FIFO Tide Mark Register
80040040	USIM_DATA	32	Data Register Used as TX/RX Data Register
80040044	USIM_COUNT	32	USIM FIFO Count Register
80040050	USIM_ATIME	32	USIM Activation Time Register
80040054	USIM_DTIME	32	USIM Deactivation Time Register
80040058	USIM_TOUT	32	Character to Character Waiting Time Register
8004005C	USIM_GTIME	32	Command Block to Block Guard Time Register
80040060	USIM_ETIME	32	TX Error Detection Wait Time Register
80040064	USIM_EXT_TIME	32	USIM Extended Output Enable Control Register
80040068	USIM_CGTIME	32	Character to Character Guard Time Register
80040070	USIM_COMDCTRL	32	USIM Command Control Register
80040074	USIM_COMDLEN	32	USIM Command Data Length Register
80040078	USIM_LEFTLEN	32	USIM Command Left Length Register
8004007C	USIM_LATCH1	32	USIM Latched Data 1 Register
80040080	USIM_LATCH2	32	USIM Latched Data 2 Register
80040090	USIM_ATRSTA	32	USIM Activation Controller State Register
80040094	USIM_ToPTLSTA	32	USIM Protocol Controller State Register
80040098	USIM_DBG	32	USIM Debug Register
8004009C	USIM_DBGDATA	32	USIM FIFO Data Debug Register
800400A0	USIM_DMADATA	32	Data Register Used as HDMA TX/RX Data Register

80040000 USIM_CODA_VERSION USIM Version Control Register 20110920

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CODA_VERSION															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CODA_VERSION															
Type	RO															
Reset	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	CODA_VERSION	CODA_VERSION	

Bit(s)	Mnemonic	Name	Description

80040010 USIM_CTRL **USIM Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											IFCLR	RSTCTRL	RSTLV	WRST	CSTOP	SIMON
Type											WP	RW	RW	WP	RW	RW
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5	**IFCLR**	IFCLR	1: Clear USIM interface for the next command transfer
4	**RSTCTRL**	RSTCTRL	0: Disable SIMRST direct control mode 1: Enable SIMRST direct control mode 0: Disable SIMRST direct control mode 1: Enable SIMRST direct control mode
3	**RSTLV**	RSTLV	0: Parking at LOW level 1: Parking at HIGH level 0: Parking at LOW level 1: Parking at HIGH level
2	**WRST**	WRST	1: Trigger warm reset (AL card) 1: Trigger warm reset (AL card)
1	**CSTOP**	CSTOP	0: Enable SIMCLK output 1: Disable SIMCLK output 0: Enable SIMCLK output 1: Disable SIMCLK output
0	**SIMON**	SIMON	0: 1-to-0 change will start the card deactivation sequence 1: 0-to-1 change will start the card activation sequence 0: 1-to-0 change will start the card deactivation sequence 1: 0-to-1 change will start the card activation sequence

80040014 USIM_CONF **USIM Configuration Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					T1TX2RXEN	TXRDIS	RXRDIS	HFEN	ToEN	T1EN	TOUTEN	SIMSEL	CONV	CPOL	TXACK	RXACK
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11	**T1TX2RXEN**	T1TX2RXEN	0: DMA type auto switch function is not enabled. 1: DMA type auto switch function is enabled.
10	**TXRDIS**	TXRDIS	0: Enable TX DMA request (default) 1: Disable TX DMA request

Bit(s)	Mnemonic	Name	Description
9	**RXRDIS**	RXRDIS	0: Enable RX DMA request (default) 1: Disable RX DMA request
8	**HFEN**	HFEN	0: Disable hardware flow control 1: Enable hardware flow control
7	**T0EN**	T0EN	0: Disable T=0 protocol controller 1: Enable T=0 protocol controller
6	**T1EN**	T1EN	0: Disable T=1 protocol controller 1: Enable T=1 protocol controller
5	**TOUTEN**	TOUTEN	0: Disable timeout counter 1: Enable timeout counter
4	**SIMSEL**	SIMSEL	0: SIMSEL pin is set to LOW level. 1: SIMSEL pin is set to HIGH level.
3	**CONV**	CONV	0: Direct convention 1: Inverse convention
2	**CPOL**	CPOL	0: SIMCLK stop in LOW level 1: SIMCLK stop in HIGH level
1	**TXACK**	TXACK	0: Disable character transmission handshaking 1: Enable character transmission handshaking
0	**RXACK**	RXACK	0: Disable character reception handshaking 1: Enable character reception handshaking

80040018 USIM_CONFSTA **USIM Configuration Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						TXRDIS_S										SIM_CLR
Type						RU										RU
Reset						0										0

Bit(s)	Mnemonic	Name	Description
10	**TXRDIS_S**	TXRDIS_S	0: TX DMA request is enabled. 1: TX DMA request is disabled.
0	**SIM_CLR**	SIM_CLR	

8004001C USIM_BRR **USIM Baud Rate Register** **000005D1**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						ETU									SIMCLK	
Type						RW									RW	
Reset						1	0	1	1	1	0	1	0	0	0	1

Bit(s)	Mnemonic	Name	Description
10:2	**ETU**	ETU	
1:0	**SIMCLK**	SIMCLK	0: Reserved

Bit(s)	Mnemonic	Name	Description
			1: 13/4MHz 2: 13/8MHz 3: 13/12MHz

80040020 USIM_IRQEN **USIM Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					UDRUN	EDCERR	T1END	RXERR	ToEND	SIMOFF	ATRERR	TXERR	TOUT	OVRUN	RXTIDE_EN	TXTIDE_EN
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11	**UDRUN**	UDRUN	0: Disable interrupt 1: Enable interrupt
10	**EDCERR**	EDCERR	0: Disable interrupt 1: Enable interrupt
9	**T1END**	T1END	0: Disable interrupt 1: Enable interrupt
8	**RXERR**	RXERR	0: Disable interrupt 1: Enable interrupt
7	**ToEND**	ToEND	0: Disable interrupt 1: Enable interrupt
6	**SIMOFF**	SIMOFF	0: Disable interrupt 1: Enable interrupt
5	**ATRERR**	ATRERR	0: Disable interrupt 1: Enable interrupt
4	**TXERR**	TXERR	0: Disable interrupt 1: Enable interrupt
3	**TOUT**	TOUT	0: Disable interrupt 1: Enable interrupt
2	**OVRUN**	OVRUN	0: Disable interrupt 1: Enable interrupt
1	**RXTIDE_EN**	RXTIDE_EN	0: Disable interrupt 1: Enable interrupt
0	**TXTIDE_EN**	TXTIDE_EN	0: Disable interrupt 1: Enable interrupt

80040024 USIM_STS **USIM Interrupt Event Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					UDRUN_S	EDCERR_S	T1END_S	RXERR_S	ToEND_S	SIMOFF_S	ATRERR_S	TXERR_S	TOUT_S	OVRUN_S	RXTIDE_S	TXTIDE_S
Type					W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	RU	RU
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11	**UDRUN_S**	UDRUN_S	0: No event occurs. 1: Event occurred and not yet cleared.
10	**EDCERR_S**	EDCERR_S	0: No event occurs. 1: Event occurred and not yet cleared.
9	**T1END_S**	T1END_S	0: No event occurs. 1: Event occurred and not yet cleared.
8	**RXERR_S**	RXERR_S	0: No event occurs. 1: Event occurred and not yet cleared.
7	**T0END_S**	T0END_S	0: No event occurs. 1: Event occurred and not yet cleared.
6	**SIMOFF_S**	SIMOFF_S	0: No event occurs. 1: Event occurred and not yet cleared.
5	**ATRERR_S**	ATRERR_S	0: No event occurs. 1: Event occurred and not yet cleared.
4	**TXERR_S**	TXERR_S	0: No event occurs. 1: Event occurred and not yet cleared.
3	**TOUT_S**	TOUT_S	0: No event occurs. 1: Event occurred and not yet cleared.
2	**OVRUN_S**	OVRUN_S	0: No event occurs. 1: Event occurred and not yet cleared.
1	**RXTIDE_S**	RXTIDE_S	0: The amount of bytes in FIFO is not larger than RX tide. 1: The amount of bytes in FIFO is larger than RX tide.
0	**TXTIDE_S**	TXTIDE_S	0: The amount of bytes in FIFO is not smaller than TX tide. 1: The amount of bytes in FIFO is smaller than TX tide.

80040030 USIM_RETRY **USIM Retry Limit Register** **00000303**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						TXRE TRY								RXRETRY		
Type						RW								RW		
Reset						0	1	1						0	1	1

Bit(s)	Mnemonic	Name	Description
10:8	**TXRETRY**	TXRETRY	
2:0	**RXRETRY**	RXRETRY	

80040034 USIM_TIDE **USIM FIFO Tide Mark Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TXTI DE								RXTIDE			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:8	**TXTIDE**	TXTIDE	
3:0	**RXTIDE**	RXTIDE	

80040040 USIM_DATA **Data Register Used as TX/RX Data Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DATA							
Type									OTHER							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**DATA**	DATA	

80040044 USIM_COUNT **USIM FIFO Count Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												COUNT				
Type												RU				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0	**COUNT**	COUNT	

80040050 USIM_ATIME **USIM Activation Time Register** **000002BE**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							ATIME									
Type							RW									
Reset							1	0	1	0	1	1	1	1	1	0

Bit(s)	Mnemonic	Name	Description
9:0	**ATIME**	ATIME	

80040054 USIM_DTIME — USIM Deactivation Time Register — 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DTIME					
Type											RW					
Reset											0	0	1	1	1	1

Bit(s)	Mnemonic	Name	Description
5:0	DTIME	DTIME	

80040058 USIM_TOUT — Character to Character Waiting Time Register — 00000260

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											WTIME					
Type											RW					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WTIME															
Type	RW															
Reset	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:0	WTIME	WTIME	

8004005C USIM_GTIME — Command Block to Block Guard Time Register — 0000000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													GTIME			
Type													RW			
Reset													1	0	1	0

Bit(s)	Mnemonic	Name	Description
3:0	GTIME	GTIME	

80040060 USIM_ETIME — TX Error Detection Wait Time Register — 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ETIME					
Type											RW					
Reset											0	0	1	1	1	1

Bit(s)	Mnemonic	Name	Description
5:0	ETIME	ETIME	

80040064 USIM_EXT_TIME — USIM Extended Output Enable Control Register — 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													EXT_TIME			
Type													RW			
Reset													0	0	0	1

Bit(s)	Mnemonic	Name	Description
3:0	EXT_TIME	EXT_TIME	

80040068 USIM_CGTIME — Character to Character Guard Time Register — 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CGTIME							
Type									RW							
Reset									0	0	0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0	CGTIME	CGTIME	

80040070 USIM_COMDCTRL — USIM Command Control Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	START							INSD	SIMINS							

Type	WP							RW	RW							
Reset	0							0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**START**	START	1: Start to transfer a T=0 or T=1 command
8	**INSD**	INSD	0: T=0 instruction is for receiving a command from the USIM card. 1: T=0 instruction is for sending a command to the USIM card.
7:0	**SIMINS**	SIMINS	

80040074 USIM_COMDLEN **USIM Command Data Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LEN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**LEN**	LEN	

80040078 USIM_LEFTLEN **USIM Command Left Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								LEFT								
Type								RU								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0	**LEFT**	LEFT	

8004007C USIM_LATCH1 **USIM Latched Data 1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LATCH1							
Type									RU							

Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**LATCH1**	LATCH1	

80040080 USIM_LATCH2 USIM Latched Data 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**LATCH2**							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**LATCH2**	LATCH2	

80040090 USIM_ATRSTA USIM Activation Controller State Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**AL**	**IR**							**OFF**
Type								RU	RU							RU
Reset								0	0							1

Bit(s)	Mnemonic	Name	Description
8	**AL**	AL	
7	**IR**	IR	
0	**OFF**	OFF	0: USIM card is on. 1: USIM card is off.

80040094 USIM_ToPTLSTA USIM Protocol Controller State Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**EDC**	**ALL**	**ONE**	**SW2**	**PROC**	**HEAD**	**IDLE**
Type										RU	RU	RU	RU	RU	RU	RU
Reset										0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
6	**EDC**	EDC	
5	**ALL**	ALL	
4	**ONE**	ONE	
3	**SW2**	SW2	
2	**PROC**	PROC	
1	**HEAD**	HEAD	
0	**IDLE**	IDLE	0: The controller is active. 1: The controller is idle.

80040098 USIM_DBG **USIM Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DBG7	DBG6	DBG5	DBG4				DBG3				
Type					RU	RU	RU	RU				RU				
Reset					0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DBG2								DBG1				
Type				RU								RU				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27	**DBG7**	DBG7	
26	**DBG6**	DBG6	
25	**DBG5**	DBG5	
24	**DBG4**	DBG4	0: FIFO RX mode 1: FIFO TX mode
20:16	**DBG3**	DBG3	
12:8	**DBG2**	DBG2	
4:0	**DBG1**	DBG1	

8004009C USIM_DBGDATA **USIM FIFO Data Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DBGPTR				DBGDATA							
Type					RU				RU							
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:8	**DBGPTR**	DBGPTR	
7:0	**DBGDATA**	DBGDATA	

800400A0 USIM_DMADATA **Data Register Used as HDMA TX/RX Data Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DMADATA							
Type									OTHER							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**DMADATA**	DMADATA	

3.16 WIFI-HIF

Module name: WIF_HIF_SDCTL_TOP_DMA Base address: (+0h)

Address	Name	Width	Register Function
00000000	WCIR	32	WLAN Chip ID Register
00000004	WHLPCR	32	WLAN HIF Low Power Control Register
00000008	WSDIOCSR	32	WLAN SDIO Control Status Register (SDIO Only)
0000000C	WHCR	32	WLAN HIF Control Register
00000010	WHISR	32	WLAN HIF Interrupt Status Register
00000014	WHIER	32	WLAN HIF Interrupt Enable Register
00000020	WASR	32	WLAN Abnormal Status Register
00000024	WSICR	32	WLAN Software Interrupt Control Register
00000034	WTDR1	32	WLAN TX Data Register 1
00000050	WRDR0	32	WLAN RX Data Register 0
00000054	WRDR1	32	WLAN RX Data Register 1
00000070	H2DSM0R	32	Host to Device Send Mailbox 0 Register
00000074	H2DSM1R	32	Host to Device Send Mailbox 1 Register
00000078	D2HRM0R	32	Device to Host Receive Mailbox 0 Register
0000007C	D2HRM1R	32	Device to Host Receive Mailbox 1 Register
00000090	WRPLR	32	WLAN RX Packet Length Register
000000D4	WPLRCR	32	WLAN Packet Length Report Control Register
000000D8	WSR	32	WLAN Snapshot Register
000000E0	WASR2	32	WLAN Debug Register
00000130	WTQCR0	32	WLAN TXQ Count Register 0
00000134	WTQCR1	32	WLAN TXQ Count Register 1
00000138	WTQCR2	32	WLAN TXQ Count Register 2
0000013C	WTQCR3	32	WLAN TXQ Count Register 3
00000140	WTQCR4	32	WLAN TXQ Count Register 4
00000144	WTQCR5	32	WLAN TXQ Count Register 5
00000148	WTQCR6	32	WLAN TXQ Count Register 6
0000014C	WTQCR7	32	WLAN TXQ Count Register 7

00000000 WCIR **WLAN Chip ID Register** **00100279**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEVICE_STATUS										W_FUNC_RDY	POR_INDICATOR	REVISION_ID			
Type	RO										RO	W1C	RO			
Reset	0	0	0	0	0	0	0	0			0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHIP_ID															
Type	RO															
Reset	0	0	0	0	0	0	1	0	0	1	1	1	1	0	0	1

Bit(s)	Name	Description
31:24	DEVICE_STATUS	**These status bits are defined by users and can be read by the host driver via SDIO bus interface. For example,**

Bit(s)	Name	Description
		watchdog reset status can be read by the host driver even when there is no AHB clock in SDIO controller.
21	W_FUNC_RDY	**Indicate that WLAN functional block has finished its initial procedure and is ready for normal operation** This is a sticky bit of HWFCR.W_FUNC_RDY. The driver will keep polling this bit during initialization. After FW is ready and sets up the corresponding bit in FW, the driver can do following control to FW. 0: WLAN functional block is not ready for normal operation. 1: WLAN functional block is ready for normal operation.
20	POR_INDICATOR	**Indicates reset occurs including external pin reset, power detect reset, power on reset, SDIO CCCR(0x06).Bit[3] reset (only in SDIO).** Write 1 to clear this bit. Writing 0 is meaningless.
19:16	REVISION_ID	**Revision ID**
15:0	CHIP_ID	**Chip ID**

00000004 WHLPCR **WLAN HIF Low Power Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							W_FW_OWN_REQ_CLR	W_FW_OWN_REQ_SET							W_INT_EN_CLR	W_INT_EN_SET
Type							W1S	W1S							W1S	W1S
Reset							0	0							0	0

Bit(s)	Name	Description
9	W_FW_OWN_REQ_CLR	**Write 1 to this bit to request firmware to return the ownership of chip WLAN function to host driver. Writing 0 has no meaning. (Refer to "Power Management" section for details).** Read always returns 0. This bit will be set during initialization or by firmware writing 1 to HWFICR. FW_OWN_BACK_INT_SET or any driver-domain WLAN interrupts.
8	W_FW_OWN_REQ_SET	**Write 1 to this bit to transfer ownership of chip WLAN function to firmware. Writing 0 has no meaning. (Refer to "Power Management" section for details). The host driver should set up this bit to give ownership to firmware only when the host driver has ownership.** Read will get the status of WLAN_DRV_OWN. WLAN_DRV_OWN indicates that software driver has the ownership of chip WLAN sub-system. 0: WLAN driver does not have ownership. 1: WLAN driver has ownership.
1	W_INT_EN_CLR	**Writing 0 has no meaning. Write 1 to clear WLAN interrupt enable signal.** Read always returns 0.
0	W_INT_EN_SET	**Writing 0 has no meaning. Write 1 to set up WLAN interrupt enable signal.** Read will get the status of W_INT_EN.

Bit(s)	Name	Description
		W_INT_EN indicates the current value of WLAN interrupt enable signal. This enable signal is used for controlling the output of WLAN interrupt signal. 0: WLAN interrupt cannot output to host. 1: WLAN interrupt can output to host.

00000008 WSDIOCSR **WLAN SDIO Control Status Register (SDIO Only)** **0000000C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DB_WR_BUSY_EN	DB_RD_BUSY_EN		
Type													RW	RW		
Reset													1	1		

Bit(s)	Name	Description
3	DB_WR_BUSY_EN	**Write busy function control bit** If the available space of internal TX FIFO is smaller than the pre-defined max. block size, write busy will be asserted. The write busy function can only be used when the block size set is smaller than pre-defined fifo size (i.e. max. block size). 0: Disable DMA write busy function 1: Enable DMA write busy function
2	DB_RD_BUSY_EN	**Read busy function control bit** If the usage of internal RX FIFO is smaller than the pre-defiend max. block size, the read busy will be triggered except that the data are the last part of this transaction. The read busy function can only be used when the block size set is smaller than pre-defined fifo size (i.e. max. block size). 0: Disable DMA read busy function 1: Enable DMA read busy function

0000000C WHCR **WLAN HIF Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_ENHANCE_MODE
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MAX_HIF_RX_LEN_NUM										RPT_OWN_RX_PACKET_LEN	RECV_MAILBOX_RD_CLR_EN	W_INT_CLR_CTRL	
Type			RW										RW	RW	RW	

Reset			0	0	0	0	0	0					0	0	0	

Bit(s)	Name	Description
16	RX_ENHANCE_MODE	**Enable the read of RX data packet, TX count status, RX length, and mailbox information in RX packet enhance mode.** 0: disable RX packet enhance mode 1: Enable the read of RX data packet, TX count status, RX length, and mailbox information in RX packet enhance mode. Design limitation: If RX_ENHANCE_MODE are enable, host should read both RX packet and interrupt enhance data at the same time.
13:8	MAX_HIF_RX_LEN_NUM	**Maximum number of SDIO controller to report the per-queue RX packets length via INT/ RX enhance mode** 0: Report entire 16 RX packets length in the same RX queue without limitation. Others (N): Report at most N RX packet lengths for each RX queue
3	RPT_OWN_RX_PACKET_LEN	**Controls RX packet report length and structure in enhance mode** If this bit is set to 1, each RX queue can report its own length according to the setting in WPLRCR. The total report length will be changed if this bit is set. The host driver should parse the enhance mode status according to the length setting in WPLRCR to get correct information. 0: Disable the function that each RX queue can report its own packet length and the maximal report length is constrained by max_hif_rx_len_num field in WHCR 1: Enable the function that each RX queue can report its own packet length and the maximal report length can be different by each queue according to the setting in WPLRCR
2	RECV_MAILBOX_RD_CLR_EN	**Controls whether the received mail-box (D2HRM0R, D2HRM1R) will be read-clear or not (including read from enhance mode structure)**
1	W_INT_CLR_CTRL	**Selects the clear mechanism of WLAN interrupt statue (WHISR)** It only supports SW_INT and FW_OWN_BACK_INT. 0: Read clear 1: Write 1 clear

00000010 WHISR — WLAN HIF Interrupt Status Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D2H_SW_INT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D2H_SW_INT								FW_OWN_BACK_INT	ABNORMAL_INT				RX1_DONE_INT	RX0_DONE_INT	TX_DONE_INT
Type	RC								RC	RO				RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0				0	0	0

Bit(s)	Name	Description
31:8	D2H_SW_INT	**Used for software interrupt for WLAN function in FW to**

Bit(s)	Name	Description
		host driver direction WLAN firmware writing 1s to HWFICR.Bit[31:8] will set up the corresponding bit field.
7	FW_OWN_BACK_INT	**Firmware has returned the ownership to host driver.** This field is set with driver own-back only. Firmware writing 1 to HWFICR. Bit[4] will set up this bit.
6	ABNORMAL_INT	**Abnormal event interrupt** The abnormal status will be shown in WASR, including: Data overflow of WLAN TX0 and TX1 port; Data underflow of WLAN RX0 and RX1 port; FW_OWN_INVALID_ACCESS.
2	RX1_DONE_INT	**When any of the RX length data of RX1 exists in HIF RX length FIFO, this bit will be asserted.**
1	RX0_DONE_INT	**When any of the RX length data of RX0 exists in HIF RX length FIFO, this bit will be asserted.**
0	TX_DONE_INT	**If any WTQCR0 ~ WTQCR7 is not 0, this bit will be set.** 0: WTQCR0 ~ WTQCR7 are all 0. 1: Any of WTQCR0 ~ WTQCR7 is not 0. WTQCR0 ~ WTQCR7 are read clear. TX_DONE_INT will be cleared after WTQCR0 ~ WTQCR7 are all read out.

00000014 WHIER — WLAN HIF Interrupt Enable Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D2H_SW_INT_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D2H_SW_INT_EN								FW_OWN_BACK_INT_EN	ABNORMAL_INT_EN				RX1_DONE_INT_EN	RX0_DONE_INT_EN	TX_DONE_INT_EN
Type	RW								RW	RW				RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0				0	0	0

Bit(s)	Name	Description
31:8	D2H_SW_INT_EN	**WLAN host interrupt output control bits** 0: Mask the WLAN related bit interrupt output; the corresponding bits will still be written to WHISR without triggering interrupt. 1: Enable WLAN related bit interrupt output
7	FW_OWN_BACK_INT_EN	**WLAN host interrupt output control bits** 0: Mask the WLAN related bit interrupt output; the corresponding bits will still be written to WHISR without triggering interrupt. 1: Enable WLAN related bit interrupt output
6	ABNORMAL_INT_EN	**WLAN host interrupt output control bits** 0: Mask the WLAN related bit interrupt output; the corresponding bits will still be written to WHISR without triggering interrupt. 1: Enable WLAN related bit interrupt output
2	RX1_DONE_INT_EN	**WLAN host interrupt output control bits** 0: Mask the WLAN related bit interrupt output; the corresponding bits will still be written to WHISR without triggering interrupt. 1: Enable WLAN related bit interrupt output

Bit(s)	Name	Description
1	RX0_DONE_INT_EN	**WLAN host interrupt output control bits** 0: Mask the WLAN related bit interrupt output; the corresponding bits will still be written to WHISR without triggering interrupt. 1: Enable WLAN related bit interrupt output
0	TX_DONE_INT_EN	**WLAN host interrupt output control bits** 0: Mask the WLAN related bit interrupt output; the corresponding bits will still be written to WHISR without triggering interrupt. 1: Enable WLAN related bit interrupt output

00000020 WASR **WLAN Abnormal Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																WASR2
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RX1_UNDERFLOW	RX0_UNDERFLOW							TX1_OVERFLOW	
Type							RC	RC							RC	
Reset							0	0							0	

Bit(s)	Name	Description
16	WASR2	**It is abnormal interrupt.** See WASR2 for abnormal status table 2.
9	RX1_UNDERFLOW	**Data underflow of WLAN RX1 port**
8	RX0_UNDERFLOW	**Data underflow of WLAN RX0 port**
1	TX1_OVERFLOW	**Data overflow of WLAN TX1 port**

00000024 WSICR **WLAN Software Interrupt Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	H2D_SW_INT_SET															
Type	W1S															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31:16	H2D_SW_INT_SET	**Host driver writing 1 will set HWFISR. HOST_DRIVER_INT. Writing 0 is meaningless.** Read always returns 0. This is used as a communication between driver and firmware, with interrupt functionality to SDIO controller.

00000034 WTDR1 **WLAN TX Data Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX1_DATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX1_DATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX1_DATA	**TX1 write data port** Read always return 0. Data must be padded to multiples of block when the data to write is more than the size of a single block. Writing data with multiple blocks in one transaction and the remaining in another with byte mode is prohibited.

00000050 WRDR0 **WLAN RX Data Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX0_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX0_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX0_DATA	**RX0 read data port** Writing has no effect. The RX0 data port supports data aggregation. The driver should read the entire RX packets by the last SDIO controller indicated information. The number of total RX aggregation packets is restricted by WHCR. MAX_HIF_RX_LEN_NUM. The length to read must be extended to multiples of block when the data to read are more than the size of a single block. Reading data with multiple blocks in one transaction and the remaining in another with byte mode is prohibited. As long as the host driver knows the total available packet number and length via enhanced interrupt response and/or RX packet enhanced mode, it must read all RX packets in a single transaction. Reading for partial packets is also prohibited.

00000054 WRDR1 **WLAN RX Data Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX1_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX1_DATA															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX1_DATA	**RX1 read data port** Writing has no effect. The RX1 data port supports data aggregation. The driver should read the entire RX packets by the last SDIO controller indicated information. The number of total RX aggregation packets is restricted by WHCR. MAX_HIF_RX_LEN_NUM. The data length to read must be extended to multiples of block when the data to read are more than the size of a single block. Reading data with multiple blocks in one transaction and the remaining in another with byte mode is prohibited. As long as the host driver knows the total available packet number and length via enhanced interrupt response and/or RX packet enhanced mode, it must read all RX packets in a single transaction. Reading for partial packets is also prohibited.

00000070 H2DSM0R — Host to Device Send Mailbox 0 Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	H2D_SM0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	H2D_SM0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	H2D_SM0	Used by host driver to transmit data to SDIO controller which will be updated to H2DRM0R and read by FW

00000074 H2DSM1R — Host to Device Send Mailbox 1 Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	H2D_SM1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	H2D_SM1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	H2D_SM1	Used by host driver to transmit data to SDIO controller which will be updated to H2DRM1R and read by FW

00000078 D2HRM0R — Device to Host Receive Mailbox — 00000000

0 Register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D2H_RM0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D2H_RM0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	D2H_RM0	**Used by host driver to receive data from SDIO controller which is updated through D2HSM0R by FW.** The property of RO/ RC is by control of WHCR. RECV_MAILBOX_RD_CLR_EN bit.

0000007C D2HRM1R **Device to Host Receive Mailbox 1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D2H_RM1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D2H_RM1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	D2H_RM1	**Used by host driver to receive data from SDIO controller which is updated through D2HSM1R by FW.** The property of RO/ RC is by control of WHCR. RECV_MAILBOX_RD_CLR_EN bit.

00000090 WRPLR **WLAN RX Packet Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX1_PACKET_LENGTH															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX0_PACKET_LENGTH															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RX1_PACKET_LENGTH	**Used to get the next RX packet length in the RX1 length FIFO which is updated by FW HWRQ1CR.** When this field is read, it will report only 1 RX packet length in this RX queue, and at most 1 packet will return by the next RX port read.
15:0	RX0_PACKET_LENGTH	**Used to get the next RX packet length in RX0 length**

Bit(s)	Name	Description
		FIFO which is updated by FW HWRQ0CR. When this field is read, it will report only 1 RX packet length in this RX queue, and at most 1 packet will return by the next RX port read.

000000D4 WPLRCR WLAN Packet Length Report Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RX1_RPT_PKT_LEN								RX0_RPT_PKT_LEN					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
13:8	RX1_RPT_PKT_LEN	**If the RPT_OWN_RX_PACKET_LEN bit in WHCR is set, the host driver can set up this field to decide the maximal report length for RX queue 1 in enhance mode.** The default value 0 is to report maximal packet number 16. The host driver can set up the required length from 0 to 15. It is not allowed to set up this field with value bigger than the maximal packet number.
5:0	RX0_RPT_PKT_LEN	**If the RPT_OWN_RX_PACKET_LEN bit in WHCR is set, the host driver can set up this field to decide the maximal report length for RX queue 0 in enhance mode.** The default value 0 is to report maximal packet number 16. The host driver can set up the required length from 0 to 15. It is not allowed to set up this field with value bigger than the maximal packet number.

000000D8 WSR WLAN Snapshot Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SNAPSHOT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SNAPSHOT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SNAPSHOT	**32-bits register which can copy the content of AHB clock domain register read** For register with RC property, if there is CRC error during the read access, the host driver should keep reading this snapshot register until there is no CRC error to avoid information loss. SW should not read other registers first; it is atomic operation. For register without RC property, if there is CRC error during the read access, the host can only read the original register again.

Bit(s)	Name	Description
		The value in this register will be undefined if the previous read is reading register without RC property.

000000E0 WASR2 **WLAN Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							CMD53_ERR_CNT									
Type							RC									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								CMD53_ERR						RD_Timeout	WR_Timeout	FW_OWN_INVALID_ACCESS
Type								RC						RC	RC	RC
Reset								0						0	0	0

Bit(s)	Name	Description
25:16	CMD53_ERR_CNT	**Number of CMD53_ERR occurs** It is read-clear.
8	CMD53_ERR	**CMD53 byte count error** It means CMD53 read/write counter is not equivalent to CMD_BASE_SETUP. It is read-clear.
2	RD_Timeout	**If the host reads data and device cannot prepare the data well in pre-defined period, the timeout interrupt will be triggered. It is read-clear.**
1	WR_Timeout	**If the host writes data and device cannot receive the data well in pre-defined period, the write timeout interrupt will be triggered. It is read-clear.**
0	FW_OWN_INVALID_ACCESS	**Will be asserted when registers other than WCIR, WHLPCR and WSDIOCSR are accessed when FW own = 1.** Will be cleared when the host reads WASR2.

00000130 WTQCR0 **WLAN TXQ Count Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXQ1_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXQ0_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TXQ1_CNT	**Indicates the released count of TXQ1 during WTQCR0 read access** The unit can be defined by the driver. This field is cleared by read operation. Writing has no meaning.
15:0	TXQ0_CNT	**Indicates the released count of TXQ0 during WTQCR0 read access**

Bit(s)	Name	Description
		The unit can be defined by the driver. This field is cleared by read operation. Writing has no meaning.

00000134 WTQCR1 **WLAN TXQ Count Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXQ3_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXQ2_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TXQ3_CNT	**Indicates the released count of TXQ3 during WTQCR1 read access** The unit can be defined by the driver. This field is cleared by read operation. Writing has no meaning.
15:0	TXQ2_CNT	**Indicates the released count of TXQ2 during WTQCR1 read access** The unit can be defined by the driver. This field is cleared by read operation. Writing has no meaning.

00000138 WTQCR2 **WLAN TXQ Count Register 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXQ5_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXQ4_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TXQ5_CNT	**Indicates the released count of TXQ5 during WTQCR2 read access** The unit can be defined by the driver. This field is cleared by read operation. Writing has no meaning.
15:0	TXQ4_CNT	**Indicates the released count of TXQ4 during WTQCR2 read access** The unit can be defined by the driver. This field is cleared by read operation. Writing has no meaning.

0000013C WTQCR3 **WLAN TXQ Count Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXQ7_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	TXQ6_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TXQ7_CNT	**Indicates the released count of TXQ7 during WTQCR3 read access** The unit can be defined by the driver. This field is cleared by read operation. Writing has no meaning.
15:0	TXQ6_CNT	**Indicates the released count of TXQ6 during WTQCR3 read access** The unit can be defined by the driver. This field is cleared by read operation. Writing has no meaning.

00000140 WTQCR4 WLAN TXQ Count Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXQ9_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXQ8_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TXQ9_CNT	**Indicates the released count of TXQ9 during WTQCR4 read access** The unit can be defined by the driver. This field is cleared by read operation. Writing has no meaning.
15:0	TXQ8_CNT	**Indicates the released count of TXQ8 during WTQCR4 read access** The unit can be defined by the driver. This field is cleared by read operation. Writing has no meaning.

00000144 WTQCR5 WLAN TXQ Count Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXQ11_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXQ10_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TXQ11_CNT	**Indicates the released count of TXQ11 during WTQCR5 read access** The unit can be defined by the driver. This field is cleared by read operation. Writing has no meaning.
15:0	TXQ10_CNT	**Indicates the released count of TXQ10 during WTQCR5 read access** The unit can be defined by the driver. This field is cleared by read

Bit(s)	Name	Description
		operation. Writing has no meaning.

00000148 WTQCR6 **WLAN TXQ Count Register 6** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXQ13_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXQ12_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TXQ13_CNT	**Indicates the released count of TXQ13 during WTQCR6 read access** The unit can be defined by the driver. This field is cleared by read operation. Writing has no meaning.
15:0	TXQ12_CNT	**Indicates the released count of TXQ12 during WTQCR6 read access** The unit can be defined by the driver. This field is cleared by read operation. Writing has no meaning.

0000014C WTQCR7 **WLAN TXQ Count Register 7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXQ15_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXQ14_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TXQ15_CNT	**Indicates the released count of TXQ15 during WTQCR7 read access** The unit can be defined by the driver. This field is cleared by read operation. Writing has no meaning.
15:0	TXQ14_CNT	**Indicates the released count of TXQ14 during WTQCR7 read access** The unit can be defined by the driver. This field is cleared by read operation. Writing has no meaning.

Module name: WIF_HIF_SDCTL_TOP_FW Base address: (+50030000h)

Address	Name	Width	Register Function
50030000	**HGFCR**	32	HIF Global Firmware Configuration Register
50030004	**HGFISR**	32	HIF Global Firmware Interrupt Status Register
50030008	**HGFIER**	32	HIF Global Firmware Interrupt Enable Register
50030018	**HCSDCR**	32	HIF Clock Stop Detection register

Address	Name	Width	Register Function
5003001C	HGH2DR	32	HIF Global Host to Device Register
50030020	HDBGCR	32	HIF Debug Control Register
50030100	HWFISR	32	HIF WLAN Firmware Interrupt Status Register
50030104	HWFIER	32	HIF WLAN Firmware Interrupt Enable Register
50030110	HWFTE0SR	32	HIF WLAN Firmware TX Event 0 Status Register
50030120	HWFTE0ER	32	HIF WLAN Firmware TX Event 0 Enable Register
50030130	HWFRE0SR	32	HIF WLAN Firmware RX Event 0 Status Register
50030134	HWFRE1SR	32	HIF WLAN Firmware RX Event 1 Status Register
50030140	HWFRE0ER	32	HIF WLAN Firmware RX Event 0 Enable Register
50030144	HWFRE1ER	32	HIF WLAN Firmware RX Event 1 Enable Register
50030150	HWFICR	32	HIF WLAN Firmware Interrupt Control Register
50030154	HWFCR	32	HIF WLAN Firmware Control Register
50030158	HWTDCR	32	HIF WLAN TX DMA Control Register
500301A0	H2DRM0R	32	Host to Device Receive Mailbox 0 Register
500301A4	H2DRM1R	32	Host to Device Receive Mailbox 1 Register
500301A8	D2HSM0R	32	Device to Host Send Mailbox 0 Register
500301AC	D2HSM1R	32	Device to Host Send Mailbox 1 Register
500301C0	HWRQ0CR	32	HIF WLAN RX Queue 0 Control Register
500301C4	HWRQ1CR	32	HIF WLAN RX Queue 1 Control Register
500301E0	HWRLFACR	32	HIF WLAN RX Length FIFO Available Count Register
500301E8	HWDMACR	32	HIF WLAN DMA Control Register
500301F0	HSDIOTOCR	32	HIF SDIO Timeout Control Register
50030210	HWDBGCR	32	HIF WLAN Debug Control Register
50030214	HWDBGPLR	32	HIF WLAN Debug Packet Length Register

50030000 HGFCR — HIF Global Firmware Configuration Register — 40020001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		SW_SEL_CLKBLC	SW_SET_CLK_NONBLC	PAD_CR_SET_BY_FW	PB_HCLK_DIS	EHPI_HCLK_DIS	SPI_HCLK_DIS	SDIO_HCLK_DIS						FORCE_SD_HS	HCLK_NO_GATED	INT_TER_CYC_MASK
Type		RW	RW	RW	RW	RW	RW	RW						RW	RW	RW
Reset		1	0	0	0	0	0	0						0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SDCTL_BUSY	CARD_IS_18V	HINT_AS_FW_OB		SDIO_PIO_SEL	EHPI_MODE	SPI_MODE		DB_HIF_SEL		
Type						RW	RW	RW		RO	RO	RO		RO		
Reset						0	0	0		0	0	0		0	0	1

Bit(s)	Name	Description
30	SW_SEL_CLKBLC	**SW enables this bit to take over the control of balance and non-balance SD clock for pad macro.** The need for non-balance SD clock for pad macro is due to tight output timing specification. The default setting is controlled by the hardware to decide the clock balance. However, the flexibility

Bit(s)	Name	Description
		is kept for SW to decide the balance or nonbalance clock tree for the SDIO pad macro. 0: The balance/non-balance SD clock for pad macro is controlled by HW. 1: The balance/non-balance SD clock for pad macro is controlled by SW.
29	SW_SET_CLK_NONBLC	**SW enables this bit to use balance and non-balance SD clock for pad macro.** 0: Use balance sd clock for pad macro 1: Use non-balance sd clock for pad macro
28	PAD_CR_SET_BY_FW	**Enables pad macro control register test mode** Firmware writes this bit then gets the ownership to access these pad macro control registers. 0: Pad macro control register set by host driver (normal mode) 1: Pad macro control register set by firmware (test mode)
27	PB_HCLK_DIS	**Disables AHB clock for PIO-based funciton design** Will be set when PIO-based function is not used in some specific Configurations. Otherwise, PIO-based function cannot work normally. 0: AHB clock is not disabled. 1: Disable AHB clock.
26	EHPI_HCLK_DIS	**Disables AHB clock for EHPI interface** Will be set when EHPI is not used in some specific Configurations. Otherwise, EHPI cannot work normally. 0: AHB clock is not disabled. 1: Disable AHB clock.
25	SPI_HCLK_DIS	**Disables AHB clock for SPI interface** Will be set when SPI is not used in some specific Configurations. Otherwise, SPI cannot work normally. 0: AHB clock is not disabled. 1: Disable AHB clock.
24	SDIO_HCLK_DIS	**Disables AHB clock for SDIO1 interface** Will be set when SDIO is not used in some specific Configurations. Otherwise, SDIO cannot work normally. 0: AHB clock is not disabled. 1: Disable AHB clock.
18	FORCE_SD_HS	**Card capability setting method is provided to force high speed. Use external effuse or R/W interface to enable this function according to IP Configuration.** 0: SDIO is in the operation mode specified in EHS of CCCR. 1: FORCE SDIO to operate in high speed despite the value of EHS of CCCR.
17	HCLK_NO_GATED	**0: SDIO controller will gate some parts of AHB clock inside automatically for the unused period.** 1: AHB clock inside SDIO controller will always be turned on.
16	INT_TER_CYC_MASK	**Determines if SDIO should be driven high to bus bit1 during the interrupt termination cycle** 0: Always drive high during the termination cycle 1: Drive high during the termination cycle only when it is in interrupt period.
10	SDCTL_BUSY	**Indicates SDIO controller is busy or not** 0: SDIO controller is not busy. 1: SDIO controller is still busy.
9	CARD_IS_18V	**Firmware writes 1 to this field to show the voltage switch process is done and the card is in 1.8v state.** 0: Card is not in 1.8v state. 1: Card is in 1.8v state (UHS mode).
8	HINT_AS_FW_OB	**Uses interrupt to host as a firmware own back control** 0: Host interrupt to host will not trigger firmware own back. 1: Host interrupt to host will trigger firmware own back.
6	SDIO_PIO_SEL	**Host interface for SDIO PIO-based function in used**

Bit(s)	Name	Description
		0: SDIO PIO mode is not used. 1: SDIO PIO mode is used.
5	EHPI_MODE	**Indicates if EHPI8-mode or EHPI16-mode is used** 0: EHPI16-mode of EHPI is used. 1: EHPI8-mode of EHPI is used.
4	SPI_MODE	**Indicates if TI-mode or Motor-mode is used**
2:0	DB_HIF_SEL	**Host interface for DMA-based function in use** 0x1: SDIO 0x2: SPI 0x4: EHPI

50030004 HGFISR **HIF Global Firmware Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SD1_SET_DS_INT	SD1_SET_XTAL_UPD_INT	CHG_TO_18V_REQ_INT	CMD53_ERROR_INT	PB_INT	DB_INT	SDIO_SET_ABT	SDIO_SET_RES	DRV_SET_PB_IOE	DRV_SET_DB_IOE	DRV_CLR_PB_IOE	DRV_CLR_DB_IOE
Type					W1C	W1C	W1C	W1C	RO	RO	W1C	W1C	W1C	W1C	W1C	W1C
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	SD1_SET_DS_INT	**(For SDIO interface only) If the host sets up the CCCR deep sleep register, this bit will be set.** After firmware detects this event, it can know the information that the host wants the device to enter deep sleep mode. Firmware can clear this bit by writing 1. Writing 0 is meaningless.
10	SD1_SET_XTAL_UPD_INT	**(For SDIO interface only) If the host sets up the CCCR xtal frequency update register, this bit will be set.** After firmware detects this event, it can know the information that the host has updated the xtal frequency. Firmware can then read HGH2DR to know the updated frequency value. Firmware can clear this bit by writing 1. Writing 0 is meaningless.
9	CHG_TO_18V_REQ_INT	**Host sends command 11 to request device to change voltage to 1.8v.** Firmware receives the interrupt or polls the status to start the voltage switch. After the voltage switch is done, firmware will write the card is in 1.8v status to HGFCR.
8	CMD53_ERROR_INT	**CMD53 byte count error** CMD53 read/write counter is not equivalent to CMD_BASE_SETUP. It is write 1 clear.
7	PB_INT	**Status bit of PIO-based function firmware interrupt**
6	DB_INT	**Status bit of DMA-based function firmware interrupt**
5	SDIO_SET_ABT	**SDIO writes 1 to SDIO CCCR.ABORT to abort transaction.** After firmware detects this event, the TX and RX queue should be stopped by firmware, and the data in buffer should be discarded. Firmware can clear this bit by writing 1. Writing 0 is

Bit(s)	Name	Description
		meaningless.
4	SDIO_SET_RES	**SDIO writes 1 to SDIO CCCR.RES to assert software reset.** After firmware detects this event, it should disable the sub-systems on SDIO interface. Firmware can clear this bit by writing 1. Writing 0 is meaningless.
3	DRV_SET_PB_IOE	**(For SDIO interface only) If host the sets up the CCCR.IOE bit of PIO-based functional block, this bit will be set.** After firmware detects this event, it should enable sub-system which uses PIO-based function. Firmware can clear this bit by writing 1. Writing 0 is meaningless.
2	DRV_SET_DB_IOE	**(For SDIO interface only) If the host sets up the CCCR.IOE bit of DMA-based functional block, this bit will be set.** After firmware detects this event, it should enable sub-system which uses DMA-Based function. Firmware can clear this bit by writing 1. Writing 0 is meaningless.
1	DRV_CLR_PB_IOE	**(For SDIO interface only) If the host clears the CCCR.IOE bit of PIO-based functional block, this bit will be set.** After firmware detects this event, it should disable sub-system which uses PIO-based function. Firmware can clear this bit by writing 1. Writing 0 is meaningless.
0	DRV_CLR_DB_IOE	**(For SDIO interface only) If the host clears the CCCR.IOE bit of DMA-based functional block, this bit will be set.** After firmware detects this event, it should disable sub-system which uses DMA-based function. Firmware can clear this bit by writing 1. Writing 0 is meaningless.

50030008 HGFIER **HIF Global Firmware Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SD1_SET_DS_INT_EN	SD1_SET_XTAL_UPD_INT_EN	CHG_TO_18V_REQ_INT_EN	CRC_ERROR_INT_EN	PB_INT_EN	DB_INT_EN	SDIO_SET_ABT_INT_EN	SDIO_SET_RES_INT_EN	DRV_SET_PB_IOE_INT_EN	DRV_SET_DB_IOE_INT_EN	DRV_CLR_PB_IOE_INT_EN	DRV_CLR_DB_IOE_INT_EN
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	SD1_SET_DS_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR** 0: Disable the related bit interrupt output

Bit(s)	Name	Description
		1: Enable the related bit interrupt output
10	SD1_SET_XTAL_UPD_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
9	CHG_TO_18V_REQ_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
8	CRC_ERROR_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
7	PB_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
6	DB_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
5	SDIO_SET_ABT_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
4	SDIO_SET_RES_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
3	DRV_SET_PB_IOE_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
2	DRV_SET_DB_IOE_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
1	DRV_CLR_PB_IOE_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
0	DRV_CLR_DB_IOE_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output

50030018 HCSDCR **HIF Clock Stop Detection register** **00017318**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SDCLK_STOP_NUM			
Type													RW			
Reset													0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SDCLK_STOP_NUM															
Type	RW															
Reset	0	1	1	1	0	0	1	1	0	0	0	1	1	0	0	0

Bit(s)	Name	Description
19:0	SDCLK_STOP_NUM	**For SDIO 3.0 design, host driver needs to issue CMD11 to switch voltage to 1.8v to enter UHS mode.** This field is to set the hardware timer threshold for SDIO hardware to judge if the SD clock has been stopped or not. According to SDIO 3.0 specification, the host should stop the clock at least 5ms for device to switch voltage from 3.3V to 1.8V. The unit of this field is based on the AHB clock cycle number.

5003001C HGH2DR — **HIF Global Host to Device Register** — **00000003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														XTAL_FREQ		
Type														RO		
Reset														0	1	1

Bit(s)	Name	Description
2:0	XTAL_FREQ	**Host can write this CCCR vender unique register to update the xtal frequency information for FW to read.** When the host writes 1 to this field, hardware will send an interrupt to firmware to notice that the xtal frequency has been updated by the host. Firmware can read the firmware domain HGH2DR register to derive the updated xtal frequency.

50030020 HDBGCR — **HIF Debug Control Register** — **10100000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_MONH								DEBUG_MONL							
Type	RO								RO							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FLAG_HSEL								FLAG_LSEL							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DEBUG_MONH	**Debug flag monitor for high byte** Shows the flag value specified in FLAG_HSEL.
23:16	DEBUG_MONL	**Debug flag monitor for low byte** Shows the flag value specified in FLAG_LSEL
15:8	FLAG_HSEL	**Flag number of high byte for debugging** Selects which flag for debugging in high byte.
7:0	FLAG_LSEL	**Flag number of low byte for debugging** Selects which flag for debugging in low byte.

50030100 HWFISR — **HIF WLAN Firmware Interrupt Status Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	H2D_SW_INT															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RX_EVENT_1	RX_EVENT_0				TX_EVENT_0				WR_TIMEOUT_INT	RD_TIMEOUT_INT		DRV_CLR_FW_OWN	DRV_SET_FW_OWN
Type			RO	RO				RO				W1C	W1C		W1C	W1C
Reset			0	0				0				0	0		0	0

Bit(s)	Name	Description
31:16	H2D_SW_INT	**For software interrupt for WLAN function.** The host driver writing 1s to WSICR [31:16] will set up the corresponding bit field.
13	RX_EVENT_1	**If there is any interrupt asserted in HWFRE1SR, this bit will be asserted.** The bit will be de-asserted after software driver clears the interrupt event in HWFRE1SR.
12	RX_EVENT_0	**If there is any interrupt asserted in HWFRE0SR, this bit will be asserted.** The bit will be de-asserted after software driver clears the interrupt event in HWFRE0SR.
8	TX_EVENT_0	**If there is any interrupt asserted in HWFTE0SR, this bit will be asserted.** The bit will be de-asserted after software driver clears the interrupt event in HWFTE0SR.
4	WR_TIMEOUT_INT	**If the host writes data and device cannot receive the data well in pre-defined period, the write timeout interrupt will be triggered.** Firmware should receive the write timeout interrupt and tx_overflow interrupt simultaneously.
3	RD_TIMEOUT_INT	**If the host reads data and device cannot prepare the data well in pre-defined period, the timeout interrupt will be triggered.** Firmware should receive the timeout interrupt and rx_underflow interrupt simultaneously.
1	DRV_CLR_FW_OWN	**If software driver writes 1 to "WHLPCR.FW_OWN_REQ_CLR", this bit will be set to 1, and it means software driver wants firmware to return the ownership of WLAN sub-system.** Firmware must wake up WLAN sub-system from sleep mode and write 1 to HWFICR.FW_OWN_BACK_INT_SET. Firmware can clear this bit by writing 1. Writing 0 is meaningless.
0	DRV_SET_FW_OWN	**If software driver writes 1 to "WHLPCR.FW_OWN_REQ_SET", this bit will be set to 1, and it means software driver transfers the ownership of WLAN sub-system to firmware.** Firmware can force WLAN sub-system into sleep mode. Firmware can clear this bit by writing 1. Writing 0 is meaningless.

50030104 HWFIER — HIF WLAN Firmware Interrupt Enable Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	H2D_SW_INT_EN															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RX_EVENT_1_INT_EN	RX_EVENT_0_INT_EN				TX_EVENT_0_INT_EN				WR_TIMEOUT_INT_EN	RD_TIMEOUT_INT_EN		DRV_CLR_FW_OWN_INT_EN	DRV_SET_FW_OWN_INT_EN
Type			RW	RW				RW				RW	RW		RW	RW
Reset			0	0				0				0	0		0	0

Bit(s)	Name	Description
31:16	H2D_SW_INT_EN	**WLAN firmware interrupt output control for each bit** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
13	RX_EVENT_1_INT_EN	**WLAN firmware interrupt output control for each bit** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
12	RX_EVENT_0_INT_EN	**WLAN firmware interrupt output control for each bit** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
8	TX_EVENT_0_INT_EN	**WLAN firmware interrupt output control for each bit** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
4	WR_TIMEOUT_INT_EN	**WLAN firmware interrupt output control for each bit** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
3	RD_TIMEOUT_INT_EN	**WLAN firmware interrupt output control for each bit** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
1	DRV_CLR_FW_OWN_INT_EN	**WLAN firmware interrupt output control for each bit** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
0	DRV_SET_FW_OWN_INT_EN	**WLAN firmware interrupt output control for each bit** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output

50030110 HWFTE0SR **HIF WLAN Firmware TX Event 0 Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							TX1_OVERFLOW								TX1_RDY	
Type							W1C								W1C	
Reset							0								0	

Bit(s)	Name	Description
9	TX1_OVERFLOW	**Data overflow of WLAN TX1 port** Firmware can clear this bit by writing 1. Writing 0 is meaningless.
1	TX1_RDY	**If a complete frame has been moved to WLAN TX1 queue form host and the ownership bit of the buffer descriptor is cleared, this bit will be set.**

Bit(s)	Name	Description
		Firmware can clear this bit by writing 1. Writing 0 is meaningless.

50030120 HWFTE0ER **HIF WLAN Firmware TX Event 0 Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							TX1_OVERFLOW_INT_EN								TX1_RDY_INT_EN	
Type							RW								RW	
Reset							0								0	

Bit(s)	Name	Description
9	TX1_OVERFLOW_INT_EN	**WLAN firmware interrupt output control for each bit** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
1	TX1_RDY_INT_EN	**WLAN firmware interrupt output control for each bit** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output

50030130 HWFRE0SR **HIF WLAN Firmware RX Event 0 Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							RX_LEN_FIFO1_OVERFLOW	RX_LEN_FIFO0_OVERFLOW								
Type							W1C	W1C								
Reset							0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RX1_UNDERFLOW	RX0_UNDERFLOW							RX1_DONE	RX0_DONE
Type							W1C	W1C							W1C	W1C
Reset							0	0							0	0

Bit(s)	Name	Description
25	RX_LEN_FIFO1_OVERFLOW	**RX length FIFO 1 over-flow** This interrupt will be generated whenever FW attempts to set up RX length FIFO by HWRQ1CR when the packet length FIFO is already full leading to FIFO overflow. The entry in packet length FIFO will be pushed in by FW and popped out when the corresponding RX length is read by the host driver.

Bit(s)	Name	Description
24	RX_LEN_FIFO0_OVERFLOW	**RX length FIFO 0 over-flow** This interrupt will be generated whenever FW attempts to set up RX length FIFO by HWRQ0CR when the packet length FIFO is already full leading to FIFO overflow. The entry in packet length FIFO will be pushed in by FW and popped out when the corresponding RX length is read by the host driver.
9	RX1_UNDERFLOW	**Data underflow of WLAN RX1 port** Firmware can clear this bit by writing 1. Writing 0 is meaningless.
8	RX0_UNDERFLOW	**Data underflow of WLAN RX0 port** Firmware can clear this bit by writing 1. Writing 0 is meaningless.
1	RX1_DONE	**If a complete frame has been moved to the host from WLAN RX1 queue (which also implies the corresponding entry is popped out from RX1 length FIFO), this bit will be set.** Firmware can clear this bit by writing 1. Writing 0 is meaningless.
0	RX0_DONE	**If a complete frame has been moved to the host from WLAN RX0 queue (which also implies the corresponding entry is popped out from RX0 length FIFO), this bit will be set.** Firmware can clear this bit by writing 1. Writing 0 is meaningless.

50030134 HWFRE1SR **HIF WLAN Firmware RX Event 1 Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RX1_OWN_CLEAR_DONE	RX0_OWN_CLEAR_DONE
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	RX1_OWN_CLEAR_DONE	**If a complete frame has been moved to internal FIFO from WLAN RX1 queue and the ownership bit of the buffer descriptor is cleared, this bit will be set.** Firmware can clear this bit by writing 1. Writing 0 is meaningless.
0	RX0_OWN_CLEAR_DONE	**If a complete frame has been moved to internal FIFO from WLAN RX0 queue and the ownership bit of the buffer descriptor is cleared, this bit will be set.** Firmware can clear this bit by writing 1. Writing 0 is meaningless.

50030140 HWFRE0ER **HIF WLAN Firmware RX Event** **00000000**

0 Enable Register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							RX_LEN_FIFO1_OVERFLOW_INT_EN	RX_LEN_FIFO0_OVERFLOW_INT_EN								
Type							RW	RW								
Reset							0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RX1_UNDERFLOW_INT_EN	RX0_UNDERFLOW_INT_EN							RX1_DONE_INT_EN	RX0_DONE_INT_EN
Type							RW	RW							RW	RW
Reset							0	0							0	0

Bit(s)	Name	Description
25	RX_LEN_FIFO1_OVERFLOW_INT_EN	**WLAN firmware interrupt output control for each bit** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
24	RX_LEN_FIFO0_OVERFLOW_INT_EN	**WLAN firmware interrupt output control for each bit** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
9	RX1_UNDERFLOW_INT_EN	**WLAN firmware interrupt output control for each bit** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
8	RX0_UNDERFLOW_INT_EN	**WLAN firmware interrupt output control for each bit** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
1	RX1_DONE_INT_EN	**WLAN firmware interrupt output control for each bit** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
0	RX0_DONE_INT_EN	**WLAN firmware interrupt output control for each bit** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output

50030144 HWFRE1ER HIF WLAN Firmware RX Event 1 Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RX1_OWN_CLEAR_DONE_I	RX0_OWN_CLEAR_DONE_I

															NT_EN	NT_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RX1_OWN_CLEAR_DONE_INT_EN	**WLAN firmware interrupt output control for each bit** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output
0	RX0_OWN_CLEAR_DONE_INT_EN	**WLAN firmware interrupt output control for each bit** 0: Disable the related bit interrupt output 1: Enable the related bit interrupt output

50030150 HWFICR **HIF WLAN Firmware Interrupt Control Register** **00000010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D2H_SW_INT_SET															
Type	W1S															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D2H_SW_INT_SET											FW_OWN_BACK_INT_SET				
Type	W1S											W1S				
Reset	0	0	0	0	0	0	0	0				1				

Bit(s)	Name	Description
31:8	D2H_SW_INT_SET	**Firmware writing 1s will set up WHISR.D2H_SW_INT. Writing 0 is meaningless.** Read always returns 0. This is used as a communication between FW to driver, with interrupt functionality to host driver HIF.
4	FW_OWN_BACK_INT_SET	**Firmware writing 1 will set up WHISR.FW_OWN_BACK_INT. Writing 0 is meaningless. It will also clear WLAN_FW_OWN bit and set up WHLPCR.WLAN_DRV_OWN bit.** If driver requests firmware to return the ownership or firmware wants to wake up the driver, firmware can set up this bit. Read will get the status of WLAN_FW_OWN bit. WLAN_FW_OWN indicates that WLAN firmware has the ownership of chip WLAN sub-system. This bit will be cleared by firmware writing 1 to HWFICR.FW_OWN_BACK_INT_SET or any WLAN driver-domain interrupt. 0: WLAN firmware does not have ownership. 1: WLAN firmware has ownership.

50030154 HWFCR **HIF WLAN Firmware Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																W_FUNC_RDY
Type																RW
Reset																0

Bit(s)	Name	Description
0	W_FUNC_RDY	**Indicates WLAN functional block's current status** If WLAN functional block has finished its initial procedure and it is ready for normal operation, firmware should set up this bit. If WLAN functional block is disabled, this bit should be cleared. This is a sticky bit of WCIR.W_FUNC_RDY. 0: WLAN functional block is not ready for normal operation. 1: WLAN functional block is ready for normal operation.

50030158 HWTDCR **HIF WLAN TX DMA Control Register** **02000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							TXQ1_DMA_STATUS								TXQ1_DMA_RUM	
Type							RO								W1S	
Reset							1								0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							TXQ1_DMA_START								TXQ1_DMA_STOP	
Type							W1S								W1S	
Reset							0								0	

Bit(s)	Name	Description
25	TXQ1_DMA_STATUS	**Read for TX1 queue DMA status** When the HIF controller is reset, the queue will be in the inactive state by default. After receiving a START or RESUME command and executing it without error, the queue will enter active state. When the queue is empty or stopped by a STOP command, it will return to the inactive state. 0: Inactive 1: Active
17	TXQ1_DMA_RUM	**Resumes TX1 queue DMA to operate** The DMA will reload the chain descriptor from the current address. Firmware writes 1 to enable the DMA. Writing 0 is meaningless. Read always returns 0.
9	TXQ1_DMA_START	**Starts TX1 queue DMA operation** The DMA will load the chain descriptor from the address assigned by HWFTQ1SAR. SW must check if TXQ1_DMA_STATUS is inactive before it starts. Writing 0 is meaningless. Read always returns 0.
1	TXQ1_DMA_STOP	**Stops TX1 queue DMA operation** It will not clear the result of TX count set by HWTPCCR(WTSR0/

Bit(s)	Name	Description
		WTSR1). Firmware writes 1 to stop the DMA. Writing 0 is meaningless. Read always returns the current DMA activity. 0: Stopped 1: Stopped command is on-going. If one data port to multiple queues design is configured, any one of these queues stopped will lead to these queues stopping at the same time (e.g. If TX queue 1 stops, TX queue 2, 3, 4, 5, 6, 7 will also stop by HW since they share the same data port).

500301A0 H2DRM0R Host to Device Receive Mailbox 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	H2D_RM0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	H2D_RM0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	H2D_RM0	Used by firmware to receive data from SDIO controller which is updated through H2DSM0R by host driver

500301A4 H2DRM1R Host to Device Receive Mailbox 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	H2D_RM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	H2D_RM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	H2D_RM1	Used by firmware to receive data from SDIO controller which is updated through H2DSM1R by host driver

500301A8 D2HSM0R Device to Host Send Mailbox 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D2H_SM0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D2H_SM0															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	D2H_SM0	Used by firmware to transmit data to SDIO controller which is updated to D2HRM0R and read by host driver

500301AC D2HSM1R **Device to Host Send Mailbox 1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D2H_SM1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D2H_SM1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	D2H_SM1	Used by firmware to transmit data to SDIO controller which is updated to D2HRM1R and read by host driver

500301C0 HWRQ0CR **HIF WLAN RX Queue 0 Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													RXQ0_DMA_STATUS	RXQ0_DMA_RUM	RXQ0_DMA_START	RXQ0_DMA_STOP
Type													RO	W1S	W1S	W1S
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXQ0_PACKET_LENGTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	RXQ0_DMA_STATUS	**Read for RX0 queue DMA status** When the SDIO controller is reset, the queue will be in the inactive state by default. After receiving a START or RESUME command and executing it without error, the queue will enter active state. When the queue is empty or stopped by a STOP command, it will return to the inactive state. 0: Inactive 1: Active
18	RXQ0_DMA_RUM	**Resumes RX0 queue DMA to operate** The DMA will reload the chain descriptor from the current address. Firmware writes 1 to enable the DMA. Writing 0 is meaningless. Read always returns 0.
17	RXQ0_DMA_START	**Starts RX0 queue DMA operation** The DMA will load the chain descriptor from the address

Bit(s)	Name	Description
		assigned by HWFRQ0SAR. SW must check if RXQ0_DMA_STATUS is inactive before it starts. Writing 0 is meaningless. Read always returns 0.
16	RXQ0_DMA_STOP	**Stops RX0 queue DMA operation** The content in RXQ0 FIFO and RXQ0 length FIFO will be cleared. Firmware writes 1 to stop the DMA. Writing 0 is meaningless. Read returns the current RXQ0 operation state. 0: Stop operation is finished. 1: Stop operation is on-going.
15:0	RXQ0_PACKET_LENGTH	**When write:** Indicates HIF that 1 RX packet in this packet length is queued into this RX queue. When read: Read the 1st RX packet length indicated from this queue and will be 0 when queue is empty. FW will write this FIFO-like port (at most 64 entries depending on the hardware Configuration for each project) together with RXQ0_DMA_RUM bit set after RX packet is queued into descriptor chain. RX packet with length set by this field can be read by the host driver which is through reading WRPLR, INT enhance mode or RX enhance mode. Non-empty entry will generate RX done interrupt, and the corresponding entry will be cleared by HW after this packet length is read by the host driver. Writing 0 is meaningless.

500301C4 HWRQ1CR **HIF WLAN RX Queue 1 Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													RXQ1_DMA_STATUS	RXQ1_DMA_RUM	RXQ1_DMA_START	RXQ1_DMA_STOP
Type													RO	W1S	W1S	W1S
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX1_PACKET_LENGTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	RXQ1_DMA_STATUS	**Read for RXQ1 DMA status** When the SDIO controller is reset, the queue will be in the inactive state by default. After receiving a START or RESUME command and executing it without error, the queue will enter active state. When the queue is empty or stopped by a STOP command, it will return to the inactive state. 0: Inactive 1: Active
18	RXQ1_DMA_RUM	**Resumes RX1 queue DMA to operate** The DMA will reload the chain descriptor from the current address. Firmware writes 1 to enable the DMA. Writing 0 is meaningless. Read always returns 0.

Bit(s)	Name	Description
17	RXQ1_DMA_START	**Starts RX1 queue DMA operation** The DMA will load the chain descriptor from the address assigned by HWFRQ1SAR. SW must check if RXQ1_DMA_STATUS is inactive before it starts. Writing 0 is meaningless. Read always returns 0.
16	RXQ1_DMA_STOP	**Stops RX1 queue DMA operation** The content in RXQ1 FIFO and RXQ1 length FIFO will be cleared. Firmware writes 1 to stop the DMA. Writing 0 is meaningless. Read returns the current RXQ1 operation state. 0: Stopped 1: Active
15:0	RX1_PACKET_LENGTH	**When write:** Indicates HIF that 1 RX packet in this packet length is queued into this RX queue. When read: Read the 1st RX packet length indicated from this queue, and will be 0 when queue is empty. FW will write this FIFO-like port (at most 64 entries depending on the hardware Configuration for each project) together with RXQ1_DMA_RUM bit set after RX packet is queued into descriptor chain. RX packet with length been set by this field can be read by the host driver which is through reading WRPLR, INT enhance mode or RX enhance mode. Non-empty entry will generate RX done interrupt, and the corresponding entry will be cleared by HW after this packet length is read by the host driver. Writing 0 is meaningless.

500301E0 HWRLFACR **HIF WLAN RX Length FIFO Available Count Register** **00001010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RX1_LEN_FIFO_AVAIL_CNT								RX0_LEN_FIFO_AVAIL_CNT						
Type		RO								RO						
Reset		0	0	1	0	0	0	0		0	0	1	0	0	0	0

Bit(s)	Name	Description
14:8	RX1_LEN_FIFO_AVAIL_CNT	**Indicates RX1 length FIFO available count** SW should prevent push extra entries into FIFO. If under the definition of SDCTL_RXD_PACKET_LEN_16, the maximum is 16.
6:0	RX0_LEN_FIFO_AVAIL_CNT	**Indicates RX0 length FIFO available count** SW should prevent pushing extra entries into FIFO. If under the definition of SDCTL_RXE_PACKET_LEN_16, the maximum is 16.

500301E8 HWDMACR **HIF WLAN DMA Control Register** **0000004E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AHB_BURST_SIZE		AHB_PROT2_CTL		ARBITER_MODE	DMA_BST_SIZE	DEST_BST_TYP	AHB_1KBNDRY_PRTCT
Type									RW		RW		RW	RW	RW	RW
Reset									0	1	0	0	1	1	1	0

Bit(s)	Name	Description
7:6	AHB_BURST_SIZE	**WDMA burst size** 0x1: Burst 8
5:4	AHB_PROT2_CTL	**Controls AHB bus Protection 2 function**
3	ARBITER_MODE	**For normal mode, the arbitration algorithm is more preferred for TX direction (from host to FW), which is good for reducing the duration time of write busy in SDIO interface.** For reserve mode, it is more aggressive than normal mode, which means RX will not be executed unless TX is completed.
2	DMA_BST_SIZE	**Determines DMA burst size** 0: 4 DW 1: 8 DW
1	DEST_BST_TYP	**Specifies AHB burst type for HWO write back**
0	AHB_1KBNDRY_PRTCT	**Specifies protection of 1K boundary or not**

500301F0 HSDIOTOCR **HIF SDIO Timeout Control Register** **00032000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															REG_WR_TIMEOUT_EN	REG_RD_TIMEOUT_EN
Type															RW	RW
Reset															1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REG_TIMEOUT_NUM															
Type	RW															
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	REG_WR_TIMEOUT_EN	**Firmware can write 0 to this field to disable SDIO write timeout function and wirte 1 to enable the function.** 0: Disable SDIO timeout function 1: Enable SDIO timeout function
16	REG_RD_TIMEOUT_EN	**Firmware can write 0 to this field to disable SDIO read timeout function and wirte 1 to enable the function.** 0: Disable SDIO timeout function 1: Enable SDIO timeout function
15:0	REG_TIMEOUT_NUM	**Firmware can write this field to decide the timeout threshold** Unit: SDIO clock cycle number

Bit(s)	Name	Description

50030210 HWDBGCR **HIF WLAN Debug Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													TX1_RECORD_EN	RX1_RECORD_EN	RX0_RECORD_EN	NO_DMU_DBG_MODE
Type													RW	RW	RW	RW
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_PKTLEN_OFFSET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	TX1_RECORD_EN	**Firmware can write 1 to this field to enable TX1 data port record in debug mode.**
18	RX1_RECORD_EN	**Firmware can write 1 to this field to enable RX1 data port record in debug mode.**
17	RX0_RECORD_EN	**Firmware can write 1 to this field to enable RX0 data port record in debug mode.**
16	NO_DMU_DBG_MODE	**Firmware can write 1 to this field to enable virtual direct DMA debug mode.** When this mode is enabled, the data transfer between SDIO controller and SDIO wrapper will also be written to SDIO internal memory in PIO mode for debugging. Firmware can enable the data port to be recorded by writing 1 to the corresponding field in this register. Only one data port can be recorded at a time for debug mode so that the recording condition can be applied to that port correctly. The recording condition is packet size and packet length offset. Packets that meet both two criteria will be recorded.
15:0	DBG_PKTLEN_OFFSET	**Since the memory used for debugging is only roughly 2KB and might not be enough to record one full packet size, firmware can set up this field to indicate the offset of one packet size to be recorded.** This field is limited by DW alignment size. e.g. firmware writing 20 to this field means that the data from byte 21 will be recorded.

50030214 HWDBGPLR **HIF WLAN Debug Packet Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBG_LEN_UP_BOUND															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_LEN_LOW_BOUND															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
31:16	DBG_LEN_UP_BOUND	**Firmware can write this field to decide the upper bound packet size to record.** Packets that meet both the upper and lower bound criteria will be recorded.
15:0	DBG_LEN_LOW_BOUND	**Firmware can write this field to decide the lower bound packet size to record.** Packets that meet both the upper and lower bound criteria will be recorded.

Module name: WIF_HIF_Connsys_HIF Base address: (+180f0000h)

Address	Name	Width	Register Function
180F0000	SDIO_CMD_BASE	32	CMD52/CMD53 Command Information
180F0004	CMD52	32	CMD52 Port (Read/Write SDIO on Func0)
180F0008	CMD3	32	CMD3 Port (Read only: R6 response)
180F000C	CMD5	32	CMD5 Port (Read only: R4 response)
180F0010	CMD7	32	CMD7 Port (Read only: R1 response)
180F0014	CMD11	32	CMD11 Port (Read only: R1 response)
180F1000	CMD53	32	CMD53 Port (General read/write SDIO)
180F0200	CONN_HIF_REG00	32	CONN_HIF_REG00
180F0204	CONN_HIF_REG01	32	CONN_HIF_REG01
180F0208	CONN_HIF_REG02	32	CONN_HIF_REG02
180F0300	CONN_HIF_DBGCR00	32	WIF-HIF Debug Register
180F0304	CONN_HIF_DBGCR01	32	WIF-HIF Debug Register
180F0308	CONN_HIF_DBGCR02	32	WIF-HIF Debug Register
180F030C	CONN_HIF_DBGCR03	32	WIF-HIF Debug Register
180F0310	CONN_HIF_DBGCR04	32	WIF-HIF Debug Register
180F0314	CONN_HIF_DBGCR05	32	WIF-HIF Debug Register
180F0318	CONN_HIF_DBGCR06	32	WIF-HIF Debug Register
180F031C	CONN_HIF_DBGCR07	32	WIF-HIF Debug Register
180F0320	CONN_HIF_DBGCR08	32	WIF-HIF Debug Register
180F0324	CONN_HIF_DBGCR09	32	WIF-HIF Debug Register
180F0328	CONN_HIF_DBGCR10	32	WIF-HIF Debug Register
180F032C	CONN_HIF_DBGCR11	32	WIF-HIF Debug Register
180F0330	CONN_HIF_DBGCR12	32	WIF-HIF Debug Register

180F0000 SDIO_CMD_B CMD52/CMD53 Command 00000000

ASE **Information**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SDIO_CMD_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SDIO_CMD_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SDIO_CMD_BASE	**CMD52/CMD53 command information** For CMD53, CR[31]: R/W flag CR[30:28]: Function number CR[27]: Block mode CR[26]: OP CR[25:9]: Register address CR[8:0]: Byte/Block count For CMD52, CR[31]: R/W flag CR[30:28]: Function number CR[27]: RAW flag CR[26]: Stuff (reserved) CR[25:9]: Register address CR[8:0]: Write data or stuff bits

180F0004 CMD52 **CMD52 Port (Read/Write SDIO on Func0)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CMD52															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CMD52															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CMD52	Read CMD52 port will return 8 bits of data. Write CMD52 port will write 8 bits of data specified in command information.

180F0008 CMD3 **CMD3 Port (Read only: R6 response)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CMD3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CMD3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CMD3	Read CMD3 port will turn SDIO R6 response.

180F000C CMD5 CMD5 Port (Read only: R4 response) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CMD5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CMD5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CMD5	Read CMD3 port will turn SDIO R4 response.

180F0010 CMD7 CMD7 Port (Read only: R1 response) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CMD7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CMD7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CMD7	Read CMD3 port will turn SDIO R1 response.

180F0014 CMD11 CMD11 Port (Read only: R1 response) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CMD11															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CMD11															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CMD11	Read CMD11 will request device switch to 1.8V and return SDIO R1 response.

180F1000 CMD53 — CMD53 Port (General read/write SDIO) — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CMD53															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CMD53															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CMD53	**Read CMD53 port will return 32 bits of data from address specified in command information.** Write CMD53 port will write 32 bits of data into address specified in command information.

180F0200 CONN_HIF_REG00 — CONN_HIF_REG00 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															conn_hif_int_disable
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:1	Reserved	**Reserved**
0	conn_hif_int_disable	**Connsys HIF interrupt control** 1'b0: Enable connsys interrupt 1'b1: Disable connsys interrupt

180F0204 CONN_HIF_REG01 — CONN_HIF_REG01 — 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved												conn_hif_dma_burst_size			
Type	RW												RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
31:4	Reserved	**Reserved**
3:0	conn_hif_dma_burst_size	**Connsys HIF option for DMA request** (For debugging only. Do not set up this register.) Default setting for APDMA burst size is 4. Set also connsys HIF DMA request to size 4.

180F0208 CONN_HIF_REG02 CONN_HIF_REG02 00010009

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																tran_cnt_opt_set
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									tran_cnt_opt							
Type									RW							
Reset									0	0	0	0	1	0	0	1

Bit(s)	Name	Description
16	tran_cnt_opt_set	**Connsys HIF option for internal FIFO control** (For debugging only. Do not set up this register.)
7:0	tran_cnt_opt	**Connsys HIF option for internal FIFO control** (For debugging only. Do not set up this register.) This option controls TX/RX busy FIFO length. The default setting for APDMA burst size is 4. Set also connsys HIF DMA request to size 4.

180F0300 CONN_HIF_DBGCR00 WIF-HIF Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SDIO_CMD_BASE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SDIO_CMD_BASE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SDIO_CMD_BASE	Information for SDIO_CMD_BASE set by APMCU

180F0304 CONN_HIF_DBGCR01 WIF-HIF Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								Xfer_byte_counter								
Type								RO								

Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Xfer_block_counter															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	Xfer_byte_counter	Transfer byte counter on cmd53 byte mode; transfer block counter on cmd53 block mode
15:0	Xfer_block_counter	Transfer byte counter on block mode

180F0308 CONN_HIF_DBGCR02 WIF-HIF Debug Register 00000060

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		fn1_tx_busy	fn2_tx_busy	tx_busy_chk_flag	rx_busy_chk_flag	sd1_clk_wakeupt_host	db_drv_own	db_int_glb_en	db_int_ctl	db_wr_busy_en	db_rd_busy_en	db_fw_own_inv_acc	pb_drv_own	pb_int_glb_en	pb_wr_busy_en	pb_int_ctl
Type		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset		0	0	0	0	0	0	0	0	1	1	0	0	0	0	0

Bit(s)	Name	Description
14	fn1_tx_busy	SDIO function1 tx_busy sinagl
13	fn2_tx_busy	SDIO function2 tx_busy sinagl
12	tx_busy_chk_flag	tx_busy_chk_flag
11	rx_busy_chk_flag	rx_busy_chk_flag
10	sd1_clk_wakeupt_host	sd1_clk_wakeupt_host
9	db_drv_own	db_drv_own
8	db_int_glb_en	db_int_glb_en
7	db_int_ctl	db_int_ctl
6	db_wr_busy_en	db_wr_busy_en
5	db_rd_busy_en	db_rd_busy_en
4	db_fw_own_inv_acc	db_fw_own_inv_acc
3	pb_drv_own	pb_drv_own
2	pb_int_glb_en	pb_int_glb_en
1	pb_wr_busy_en	pb_wr_busy_en
0	pb_int_ctl	pb_int_ctl

180F030C CONN_HIF_DBGCR03 WIF-HIF Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Cmd53_rdata_fifo_csm_data_lat															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Cmd53_rdata_fifo_csm_data_lat															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	Cmd53_rdata_fifo_csm_data_lat	Cmd53_rdata_fifo_csm_data_lat

180F0310 CONN_HIF_DBGCR04 WIF-HIF Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Cmd53_xfer_blk_total															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Cmd53_xfer_blk_total															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	Cmd53_xfer_blk_total	Cmd53_xfer_blk_total

180F0314 CONN_HIF_DBGCR05 WIF-HIF Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Cmd53_info_rw	Cmd53_info_func_num			Cmd53_info_addr											
Type	RO	RO			RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Cmd53_info_addr					Cmd53_info_blk_mode	Cmd53_info_byte_cnt									Cmd53_info_rx_port
Type	RO					RO	RO									RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	Cmd53_info_rw	Cmd53_info_rw
30:28	Cmd53_info_func_num	Cmd53_info_func_num
27:11	Cmd53_info_addr	Cmd53_info_addr
10	Cmd53_info_blk_mode	Cmd53_ info _blk_mode
9:1	Cmd53_info_byte_cnt	Cmd53_ info _byte_cnt
0	Cmd53_info_rx_port	Cmd53_ info _rx_port

180F0318 CONN_HIF_DBGCR06 WIF-HIF Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								Cmd53_info_xfer_byte_cnt								

Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Cmd53_info_xfer_blk_cnt															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	Cmd53_info_xfer_byte_cnt	Cmd53_info_xfer_byte_cnt
15:0	Cmd53_info_xfer_blk_cnt	Cmd53 _info xfer_blk_cnt

180F031C CONN_HIF_DBGCR07 WIF-HIF Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				Fifo_popend_wait_period	Fifo_full_wait_period	Cmd53_xfer_hs_wr_period	Cmd53_xfer_hs_rd_period	Cmd53_xfer_hs_byte_cnt								
Type				RO	RO	RO	RO	RO								
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Cmd53_xfer_hs_blk_cnt															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	Fifo_popend_wait_period	Fifo_popend_wait_period
27	Fifo_full_wait_period	Fifo_full_wait_period
26	Cmd53_xfer_hs_wr_period	Cmd53_xfer_hs_wr_period
25	Cmd53_xfer_hs_rd_period	Cmd53_xfer_hs_rd_period
24:16	Cmd53_xfer_hs_byte_cnt	Cmd53_xfer_hs_byte_cnt
15:0	Cmd53_xfer_hs_blk_cnt	Cmd53_xfer_hs_blk_cnt

180F0320 CONN_HIF_DBGCR08 WIF-HIF Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		h2d_fifo_full	h2d_fifo_empty	h2d_wfifo_cnt								h2d_rfifo_cnt				
Type		RO	RO	RO								RO				
Reset		0	0	0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		d2h_fifo_full	d2h_fifo_empty	d2h_wfifo_cnt								d2h_rfifo_cnt				
Type		RO	RO	RO								RO				
Reset		0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
30	h2d_fifo_full	CMD53 Write data fifo full signal
29	h2d_fifo_empty	CMD53 Write data fifo empty signal
28:24	h2d_wfifo_cnt	CMD53 Write data fifo write counter
20:16	h2d_rfifo_cnt	CMD53 Write data fifo read counter
14	d2h_fifo_full	CMD53 Read data fifo full signal
13	d2h_fifo_empty	CMD53 Read data fifo empty signal
12:8	d2h_wfifo_cnt	CMD53 Read data fifo write counter
4:0	d2h_rfifo_cnt	CMD53 Read data fifo read counter

180F0324 CONN_HIF_DBGCR09 WIF-HIF Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	tqcnt_eq0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sdctl_dbg_prb															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	tqcnt_eq0	tqcnt_eq0
15:0	sdctl_dbg_prb	sdctl_dbg_prb

180F0328 CONN_HIF_DBGCR10 WIF-HIF Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	whisr															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	whisr															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	whisr	whisr

180F032C CONN_HIF_DBGCR11 WIF-HIF Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	wasr															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wasr															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	wasr	**wasr**

180F0330 CONN_HIF_DBGCR12 **WIF-HIF Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						txo_wr_access	rxo_rd_access	rx1_rd_access								
Type						RO	RO	RO								
Reset						0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
26	txo_wr_access	txo_wr_access
25	rxo_rd_access	rxo_rd_access
24	rx1_rd_access	rx1_rd_access

3.17 SSUSB

Module name: ssusb_usb3_sys_csr Base address: (+11272400h)

Address	Name	Width	Register Function
11272600	LINK_HP_TIMER	32	
11272604	LINK_CMD_TIMER	32	
11272608	LINK_PM_TIMER	32	
1127260C	LINK_UX_INACT_TIMER	32	
11272610	LINK_POWER_CONTROL	32	
11272614	LINK_ERR_COUNT	32	
11272618	LTSSM_TRANSITION	32	
11272620	LINK_RETRY_CTR L	32	
11272624	SYS_FAST_SIMULATIION	32	
11272628	LINK_CAPABILITY_CTRL	32	
1127262C	LINK_DEBUG_INF O	32	
11272640	USB3_U1_REJECT	32	
11272644	USB3_U2_REJECT	32	
11272690	DEV_NOTIF_0	32	
11272694	DEV_NOTIF_1	32	
11272698	VENDOR_DEV_TEST	32	
1127269C	VENDOR_DEF_DATA_LOW	32	
112726A0	VENDOR_DEF_DATA_HIGH	32	
112726A4	HOST_SET_PORT_CTRL	32	
112726AC	LINK_CAP_CONTROL	32	
112726B0	PORT_CONF_TIMEOUT	32	
112726B4	TIMING_PULSE_CTRL	32	
112726B8	ISO_TIMESTAMP	32	
112726C0	RECEIVE_PKT_INTR_EN	32	
112726C4	RECEIVE_PKT_INTR	32	
112726C8	CRC_ERR_INTR_E N	32	
112726CC	CRC_ERR_INTR	32	
112726D0	PORT_STATUS_INTR_EN	32	
112726D4	PORT_STATUS_INTR	32	
112726D8	RECOVERY_COUNT	32	
112726DC	T2R_LOOPBACK_TEST	32	

11272600 LINK_HP_TIMER 00003208

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		chp_timeout_v alue											php_timeout_value			
Type		RW											RW			
Reset		0	1	1	0	0	1	0					1	0	0	0

Bit(s)	Mnemonic	Name	Description
14:8		chp_timeout_va lue	**Timeout value for CREDIT_HP_TIMER of USB3 SPEC** Unit: 100us. Default: 5000us
3:0		php_timeout_va lue	**Timeout value for PENDING_HP_TIMER of USB3 SPEC** Unit: 0.5us. Default: 4us

11272604 LINK_CMD_TIMER 00000A99

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					no_lc_timeout_val ue				ldn_timeout_value				lup_timeout_value			
Type					RW				RW				RW			
Reset					1	0	1	0	1	0	0	1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
11:8		no_lc_timeout_ value	**Timeout value for USB3 MAC to meature time interval between two consecutive link commands (tU0RecoveryTimeout)** Unit: 100us. Default: 1000us
7:4		ldn_timeout_va lue	**Timeout value for host to send LDN link command** Unit: 1us. Default: 9us
3:0		lup_timeout_va lue	**Timeout value for device to send LUP link command** Unit: 1us. Default: 9us

11272608 LINK_PM_TIMER 000A0708

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													lpma _sen t_cn t_va lue			
Type													RW			

Reset													1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					pm_entry_timeout_ value								pm_lc_timeout_val ue			
Type					RW								RW			
Reset					0	1	1	1					1	0	0	0

Bit(s)	Mnemonic	Name	Description
19:16		lpma_sent_cnt_ value	**When USB3 MAC sends LPMA link command, USB3 MAC will wait for the count value of sys_ck until LPMA is sent to USB3 PHY.** Default: 10 clock cycles of sys_ck
11:8		pm_entry_timeo ut_value	**Timeout value for PM_ENTRY_TIMER of USB3 SPEC** Unit: 1us. Default: 7us
3:0		pm_lc_timeout_ value	**Timeout value for PM_LC_TIMER of USB3 SPEC** Unit: 0.5us. Default: 4us

1127260C LINK_UX_IN ACT_TIMER **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									dev_u2_inact_timeout_value							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	u2_inact_timeout_value								u1_inact_timeout_value							
Type	RU								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:16		dev_u2_inact_t imeout_value	**(Device only)** Valid value: 0x01~0xFE Unit: 256us SW can set up dev_u2_inact_timer and HW will send lgo_u2 automatically when timer is timeout. The timer is used to U0 -> U2 in device mode.
15:8		u2_inact_timeo ut_value	**Valid value: 0x01~0xFE** Unit: 256us Host: HW will set up the register through xHCI port ctrl module. The timer is used to both U0 -> U2 and U1 -> U2 in host mode. Device: HW will set up the register atuomatically when receive u2_inact_timeout lmp from host. The timer is used to U1 -> U2 in device mode.
7:0		u1_inact_timeo ut_value	**Valid value: 0x01~0xFE** Unit: 1us Host: HW will set up the register through xHCI port ctrl module. The timer is used to U0 -> U1. Device: SW can set up U1 timer and HW will send lgo_u1 automatically when u1_inact_timer is timeout. The timer is used to U0 -> U1.

11272610 LINK_POWER_CONTROL **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							sw_u2_accept_enable	sw_u1_accept_enable			ux_exit	lgo_u3	lgo_u2	lgo_u1	sw_u2_request_enable	sw_u1_request_enable
Type							RW	RW			WO	WO	WO	WO	WO	WO
Reset							0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
9		sw_u2_accept_e nable	**(Device only) Enables capability for device to accept LGO_U2 link command from host**
8		sw_u1_accept_e nable	**(Device only) Enables capability for device to accept LGO_U1 link command from host**
5		ux_exit	**Software can set up the register to ask USB3 MAC to initialize UX_EXIT_LFPS when LTSSM is in U1/U2/U3.** When USB3 MAC returns to U0 state, HW will clear the register.
4		lgo_u3	**(Host only) Software can set up the register to ask USB3 MAC to send LGO_U3 link command.** When USB3 MAC sends out LGO_U3, HW will clear the register.
3		lgo_u2	**Software can set the register to ask USB3 MAC send LGO_U2 link command.** When USB3 MAC send out LGO_U2 and hardware would clear the register.
2		lgo_u1	**Software can set the register to ask USB3 MAC send LGO_U1 link command.** When USB3 MAC send out LGO_U1 and hardware would clear the register.
1		sw_u2_request_ enable	**(Device only) Enables capability for device to send LGO_U2 link command** When device receives setup command (set feature U2_ENABLE), SW can set up the register. Note: The register will be cleared when ltssm is in hot reset/polling.
0		sw_u1_request_ enable	**(Device only) Enables capability for device to send LGO_U1 link command** When device receives setup command (set feature U1_ENABLE), SW can set up the register. Note: The register will be cleared when ltssm is in hot reset/polling.

11272614 LINK_ERR_COUNT **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																clr_link_err_cnt

Type																W1C
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	link_error_count															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		clr_link_err_c nt	**Software can write 1 to clear link error counter.**
15:0		link_error_cou nt	**USB3 MAC will calculate the link error count when the link has error and enters recovery state.** The counter will be cleared when: 1. USB3 MAC receives warm reset or hot reset. 2. Software sets up clr_link_err_cnt.

11272618 LTSSM_TRANSITION **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													go_hot_reset	go_warm_reset	go_rxdetect	go_ss_disable
Type													WO	WO	WO	WO
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3		go_hot_reset	**(Host only) Software can set up the register to ask USB3 MAC to send hot reset.** The register will be cleared when USB3 MAC starts to send hot reset.
2		go_warm_reset	**(Host only) Software can set the register to ask LTSSM from any state to Rx.Detect.Reset state and send warm reset.** The register will be cleared when USB3 MAC starts to send warm reset.
1		go_rxdetect	**(Host only) Software can set up the register to ask LTSSM from SS.Disable state to Rx.Detect state.** When LTSSM enters Rx.Detect state, HW will clear the register.
0		go_ss_disable	**(Host only) SW can set up the register to ask LTSSM from any state to SS.Disable state.** When LTSSM enters SS.Disable state, HW will clear the register.

11272620 LINK_RETRY_CTRL **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																tx_lrty_dpp_en
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		tx_lrty_dpp_en	**Enables capability of TX retry DPH with DPP** 0: TX retry DPH without DPP 1: TX retry DPH with DPP

11272624 SYS_FAST_SIMULATIION **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																sys_speed_ms_to_us
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		sys_speed_ms_t o_us	**(Simulation only) SW can set up the register to speed up ms timing value to us timing value.** The register can change 1ms unit to 1us unit.

11272628 LINK_CAPABILITY_CTRL **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									insert_crc32_err_dp_num							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								insert_crc32_err_en								zlp_crc32_chk_dis
Type								WO								RW
Reset								0								0

Bit(s)	Mnemonic	Name	Description
23:16		insert_crc32_e rr_dp_num	**(Test only) Indicates dp number will be inserted crc32 error.** Valid value: 1~255
8		insert_crc32_e rr_en	**(Test only) After one crc32 error is inserted, the bit will be auto cleared to 0.** 0: Disable inserting crc32 error 1: Enable inserting crc32 error
0		zlp_crc32_chk_ dis	

1127262C LINK_DEBUG_INFO **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															clr_tx_datalen_over_1024	tx_datalen_over_1024
Type															W1C	RU
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1		clr_tx_datalen _over_1024	**Write 1 to clear tx_datalen_over_1024.**
0		tx_datalen_ove r_1024	**USB3 MAC will record if TX datalen is longer than 1024.** The register will be cleared by set clr_tx_datalen_over_1024.

11272640 USB3_U1_REJECT **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																clr_usb3_u1_reject_cnt
Type																W1C
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	usb3_u1_reject_cnt															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		clr_usb3_u1_re ject_cnt	**SW writes 1 to clear USB3 U1 reject counter in USB3 MAC**

Bit(s)	Mnemonic	Name	Description
15:0		usb3_u1_reject _cnt	**Calculates number of times USB3 MAC rejects LGO_U1 from link partner** The counter will stop at 16'hFFFF.

11272644 USB3_U2_REJECT **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																clr_usb3_u2_reject_cnt
Type																W1C
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	usb3_u2_reject_cnt															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		clr_usb3_u2_reject_cnt	**SW writes 1 to clear USB3 U2 reject counter in USB3 MAC.**
15:0		usb3_u2_reject _cnt	**Calculates number of times USB3 MAC rejects LGO_U2 from link partner** The counter will stop at 16'hFFFF.

11272690 DEV_NOTIF_ **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dev_notif_type_specific_low															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dev_notif_type_specific_low								dev_notif_type							send_dev_notif
Type	RW								RW							WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0				0

Bit(s)	Mnemonic	Name	Description
31:8		dev_notif_type _specific_low	**(Device only) Decides device notification type specific value** SW should set up the register first before setting up send_dev_notif. Function_wake: Use bit[15:8] to be interface value and [31:16] should be 0. Latency_tolerance_message: Use bit[19:8] to be BELT value and [31:20] should be 0. Bus_interval_adjustment_message: Use [31:16] to be bus interval adjustment value and [15:8] should be 0.
7:4		dev_notif_type	**(Device only) Decides device notification type** SW should set up the register first before setting up

Bit(s)	Mnemonic	Name	Description
0		send_dev_notif	send_dev_notif. **(Device only) Write 1 to request USB3 MAC to send device notification packet.** When device notification packet is sent to host, this bit will be set to 0 by USB3 MAC.

11272694 DEV_NOTIF_1 **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dev_notif_type_specific_high															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dev_notif_type_specific_high															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		dev_notif_type_specific_high	**(Device only) Decides device notification type specific value** SW should set up the register first before setting up send_dev_notif.

11272698 VENDOR_DEV_TEST **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									vendor_dev_test_value							
Type									WO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																send_vendor_dev_test
Type																WO
Reset																0

Bit(s)	Mnemonic	Name	Description
23:16		vendor_dev_test_value	**(Device only) Venter test value field in vendor device test LMP** SW should set up the register first before setting up send_vendor_dev_test.
0		send_vendor_dev_test	**(Device only) Set up the register to request USB3 MAC to send vendor device test LMP.**

1127269C VENDOR_DEF_DATA_LOW **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	vendor_def_data_low															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vendor_def_data_low															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		vendor_def_dat a_low	**(Device only) Low double word of venter defined data field in vendor device test LMP** SW should set up the register first before setting up send_vendor_dev_test.

112726A0 VENDOR_DEF_DATA_HIGH 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	vendor_def_data_high															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vendor_def_data_high															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		vendor_def_dat a_high	**(Device only) High double word of venter defined data field in vendor device test LMP** SW should set up the register first before setting up send_vendor_dev_test.

112726A4 HOST_SET_PORT_CTRL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**send_u2_inact_timeout**	**force_link_pm_acpt**	**send_set_link_func**
Type														RU	RU	RU
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2		send_u2_inact_ timeout	(Host only) xHCI can ask USB3 MAC to send U2_INACT_TIMEOUT LMP through port ctrl module.
1		force_link_pm_ acpt	(Device only) HW will set up the register when receiving

Bit(s)	Mnemonic	Name	Description
0		send_set_link_ func	SET_LINK_FUNC LMP from host and the bit "force_link_pm_accept" is set in the header packet. (Host only) xHCI can ask USB3 MAC to send SET_LINK_FUNC LMP through port ctrl module.

112726AC LINK_CAP_CONTROL **00000401**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													tiebreaker			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	num_hp_buf								link_speed							
Type	RW								RW							
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
19:16		tiebreaker	"Tiebreaker" field in port capability LMP
15:8		num_hp_buf	"Num HP Buffers" field in port capability LMP
7:0		link_speed	"Link Speed" field in port capability LMP and port configuration LMP

112726B0 PORT_CONF_TIMEOUT **00000014**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												tport_conf_timeout_va lue				
Type												RW				
Reset												1	0	1	0	0

Bit(s)	Mnemonic	Name	Description
4:0		tport_conf_tim eout_value	**Timeout value for tPortConfig timer of USB3 SPEC** Unit: 1us

112726B4 TIMING_PULSE_CTRL **AAA0007D**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	cnt_ 1ms_ valu e				cnt_ 100u s_va lue				cnt_ 10us _val ue							
Type	RW				RW				RW							
Reset	1	0	1	0	1	0	1	0	1	0	1	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									cnt_1us_value							

Type									RW							
Reset									0	1	1	1	1	1	0	1

Bit(s)	Mnemonic	Name	Description
31:28		cnt_1ms_value	**For 1ms counter to calculate the timing interval of 100us**
27:24		cnt_100us_valu e	**For 100us counter to calculate the timing interval of 10us**
23:20		cnt_10us_value	**For 10us counter to calculate the timing interval of 1us**
7:0		cnt_1us_value	**For 1us counter to calculate cycle of sys_ck to reach 1us.** Default value: For sys_ck = 120MHz Sys_ck range: 62.5~125MHz Example: 62.5MHz: 63 70MHz: 70 80MHz: 80 100MHz: 100 120MHz: 120 125MHz: 125

112726B8 ISO_TIMESTAMP 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						iso_timestamp										
Type						RU										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	iso_timestamp															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26:0		iso_timestamp	(Device only) HW will update the register when receiving ITP from host.

112726C0 RECEIVE_PKT_INTR_EN 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														recv_set_link_func_intr_en	recv_u2_inact_intr_en	recv_itp_intr_en
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2		recv_set_link_ func_intr_en	Enables recv_set_link_func_intr
1		recv_u2_inact_ intr_en	Enables recv_u2_inact_intr
0		recv_itp_intr_ en	Enables recv_itp_intr

112726C4 RECEIVE_PKT_INTR **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														recv_set_link_func_intr	recv_u2_inact_intr	recv_itp_intr
Type														W1C	W1C	W1C
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2		recv_set_link_ func_intr	(Device only) When USB3 MAC receives SET_LINK_FUNCTION LMP, HW will set up the interrupt.
1		recv_u2_inact_ intr	(Device only) When USB3 MAC receives U2_INACT_TIMEOUT LMP, HW will set up the interrupt.
0		recv_itp_intr	(Device only) When USB3 MAC receives ITP, HW will set up the interrupt.

112726C8 CRC_ERR_INTR_EN **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														crc16_err_intr_en	crc5_err_intr_en	crc32_err_intr_en
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2		crc16_err_intr _en	(Device only) Enables crc16_err_intr
1		crc5_err_intr_ en	(Device only) Enables crc5_err_intr

Bit(s)	Mnemonic	Name	Description
0		crc32_err_intr _en	(Device only) Enables crc32_err_intr

112726CC CRC_ERR_INTR **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														crc16_err_intr	crc5_err_intr	crc32_err_intr
Type														W1C	W1C	W1C
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2		crc16_err_intr	(Device only) When USB3 MAC detects crc16 error in header packet, HW will set up the interrupt.
1		crc5_err_intr	(Device only) When USB3 MAC detects crc5 error in link command or header packet, HW will set up the interrupt.
0		crc32_err_intr	(Device only) When USB3 MAC detects crc32 error in DPP, HW will set up the interrupt.

112726D0 PORT_STATUS_INTR_EN **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														lmp_adv_err_intr_en	lmp_adv_done_intr_en	link_adv_done_intr_en
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2		lmp_adv_err_in tr_en	(Device only) Enables lmp_adv_err_intr
1		lmp_adv_done_intr_en	(Device only) Enables lmp_adv_done_intr
0		link_adv_done_intr_en	(Device only) Enables link_adv_done_intr

112726D4 PORT_STATU **00000000**

S_INTR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														lmp_adv_err_intr	lmp_adv_done_int r	link_adv_done_intr
Type														W1C	W1C	W1C
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2		lmp_adv_err_in tr	(Device only) HW will set up the interrupt when LMP advertisement (port capability and port configuration exchange) fails.
1		lmp_adv_done_i ntr	(Device only) HW will set up the interrupt when LMP advertisement (port capability and port configuration exchange) is completed.
0		link_adv_done_ intr	(Device only) HW will set up the interrupt when link advertisement (LGOOD and LCRD exchange) is completed.

112726D8 RECOVERY_COUNT **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																clr_recov_cnt
Type																W1C
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	recov_cnt															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		clr_recov_cnt	Software can write 1 to clear recov_cnt.
15:0		recov_cnt	USB3 MAC will calculate the recovery count when LTSSM enters recovery state.

112726DC T2R_LOOPBACK_TEST **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name																t2r_loopback
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		t2r_loopback	Set up the register to ingore LPM advertisement when MAC is in T2R loopback throught PHY serial port.

Module name: ssusb_usb3_mac_csr Base address: (+11272400h)

Address	Name	Width	Register Function
11272400	TS_CONFIG	32	
11272404	PIPE	32	
1127240C	LTSSM_PARAMETER	32	
11272410	LTSSM_CTRL	32	
11272414	LTSSM_INFO	32	
1127241C	USB3_CONFIG	32	
11272450	USB3_U1_STATE_INFO	32	
11272454	USB3_U2_STATE_INFO	32	
1127247C	UX_LFPS_TIMING_PARAMETER	32	
11272480	U1_LFPS_TIMING_PARAMETER_2	32	
11272484	U2_LB_LFPS_TIMING_PARAMETER_1	32	
11272488	U2_LB_LFPS_TIMING_PARAMETER_2	32	
1127248C	U3_LFPS_TIMING_PARAMETER_1	32	
11272490	U3_LFPS_TIMING_PARAMETER_2	32	
11272494	PING_LFPS_TIMING_PARAMETER	32	
11272498	POLLING_LFPS_TIMING_PARAMETER_1	32	
1127249C	POLLING_LFPS_TIMING_PARAMETER_2	32	
112724A0	UX_EXIT_LFPS_TIMING_PARAMETER	32	
112724A4	P3_TIMING_PARAMETER	32	
112724A8	WARM_RESET_TIMING_PARAMETER	32	
112724AC	UX_EXIT_TIMING_PARAMETER	32	
112724B0	REF_CK_PARAMET	32	

Address	Name	Width	Register Function
	ER		
1127250C	LTSSM_TIMING_PARAMETER_1	32	
11272510	LTSSM_TIMING_PARAMETER_2	32	
11272514	LTSSM_TIMING_PARAMETER_3	32	
11272518	LTSSM_TIMING_PARAMETER_4	32	
1127251C	LTSSM_TIMING_PARAMETER_5	32	
11272520	LTSSM_RXDETECT_CTRL	32	
11272528	PIPE_RXDATA_ERR_INTR_ENABLE	32	
1127252C	PIPE_RXDATA_ERR_INTR	32	
11272530	PIPE_LATCH_SELECT	32	
11272534	LINK_STATE_MACHINE	32	
11272538	MAC_FAST_SIMULATION	32	
1127253C	LTSSM_INTR_ENABLE	32	
11272540	LTSSM_INTR	32	
11272548	SKP_CNT	32	

11272400 TS_CONFIG **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ts_config_disable_scrambling
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		ts_config_disable_scrambling	**Disables scrambling bit in TS1 and TS2** USB3 MAC TX TS1 or TS2 with disable scramble bit asserted when the register is set to 1.

11272404 PIPE **00000095**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									cp_txdeemph_withou t		cp_txdeemph_with		cp_txdeemph		pipe_txdeemph	
Type									RW		RW		RW		RW	
Reset									1	0	0	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
7:6		cp_txdeemph_wi thout	**Txdeemph of PIPE interface for compliance mode when TX compliance pattern CP6 CP8.** 2'b00: -6dB de-emphasis 2'b01: -3.5dB de-emphasis 2'b10: No de-dmphasis 2'b11: Reserved
5:4		cp_txdeemph_wi th	**Txdeemph of PIPE interface for compliance mode when TX compliance pattern CP5 CP7** 2'b00: -6dB de-emphasis 2'b01: -3.5dB de-emphasis 2'b10: No de-dmphasis 2'b11: Reserved
3:2		cp_txdeemph	**Txdeemph of PIPE interface for compliance mode when TX compliance pattern CP0 CP1 CP2 CP3 CP4** 2'b00: -6dB de-emphasis 2'b01: -3.5dB de-emphasis 2'b10: No de-dmphasis 2'b11: Reserved
1:0		pipe_txdeemph	**Txdeemph of PIPE interface for normal mode** 2'b00: -6dB de-emphasis 2'b01: -3.5dB de-emphasis 2'b10: No de-dmphasis 2'b11: Reserved

1127240C LTSSM_PARAMETER **0308FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					disable_num							rxdetect_num				
Type					RW							RW				
Reset					0	0	1	1				0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_tseq_num															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
27:24		disable_num	**(Device only) Defines number of time to enter SS.Disable before switching from USB3 to USB2** The value cannot be 0.
20:16		rxdetect_num	**(Device only) Defines number of trials before rxdetect fails and enters SS.Disable**

Bit(s)	Mnemonic	Name	Description
15:0		tx_tseq_num	The value cannot be 0. **Defines TSEQ times USB3 MAC will be sent before entering Polling.Active** The value cannot be 0.

11272410 LTSSM_CTRL **00000007**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												force_polling_fail	force_rxdetect_fail	soft_u3_exit_en	compliance_en	u1_go_u2_en
Type												RW	RW	RW	RW	RW
Reset												0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
4		force_polling_ fail	**(Test only) SW should set up the register before USB3 is initialized.** 0: Normal function 1: Polling will fail purposely in polling.active state.
3		force_rxdetect _fail	**(Test only) SW should set up the register before USB3 is initialized.** 0: Normal function 1: Rxdetect will fail purposely in rxdetect.active state.
2		soft_u3_exit_e n	**SW should set up the register before USB3 is initialized.** 0: MAC will respond u3 exit lfps automatically when receiving u3 exit lfps from link parner. LTSSM state: U3_STATE -> U3_EXIT. 1: MAC will not respond u3 exit lfps until software set ux_exit (0x0210) register. LTSSM state: U3_STATE -> U3_RESUME --> U3_EXIT
1		compliance_en	**(Test only) Set the register to 1 to test compliance pattern.** If the register is set to 0, ltssm will not enter compliance when 360ms timeout and will not receive any LFPS. Host: Enter rxdetect Device: Enter SS.Disable 0: LTSSM will not enter compliance state. 1: Normal function
0		u1_go_u2_en	**(Test only) Enables U1 -> U2 state transition when LTSSM is in U1** 0: Disable U1 -> U2 state transition 1: Enable U1 -> U2 state transition

11272414 LTSSM_INFO **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						clr_pwr_	clr_disa	clr_rxde								pwr_chg_

						chg_tmout_flag	ble_cnt	tect_cnt								tmout_flag
Type						W1C	W1C	W1C								RU
Reset						0	0	0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					disable_cnt							rxdetect_cnt				
Type					RU							RU				
Reset					0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26		clr_pwr_chg_tmout_flag	**SW writes 1 to clear pwr_chg_tmout_flag in USB3 MAC.**
25		clr_disable_cnt	**SW writes 1 to clear disable counter in USB3 MAC.**
24		clr_rxdetect_cnt	**SW writes 1 to clear rxdetect counter in USB3 MAC.**
16		pwr_chg_tmout_flag	**Timeout in power mode change** It means there is abnormal behavior in pipe interface.
11:8		disable_cnt	**LTSSM disable counter value in USB3 MAC**
4:0		rxdetect_cnt	**LTSSM rxdetect counter value in USB3 MAC**

1127241C USB3_CONFIG **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																usb3_en
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		usb3_en	**(Device only) Enables super speed function** If usb3_en=0, LTSSM will enter ss.disable state.

11272450 USB3_U1_STATE_INFO **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																clr_usb3_u1_cnt
Type																W1C
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	usb3_u1_cnt															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		clr_usb3_u1_cn t	**SW writes 1 to clear USB3 U1 counter in USB3 MAC**
15:0		usb3_u1_cnt	**Calculates the number of times LTSSM enters U1 state** The counter will stop at 16'hFFFF.

11272454 USB3_U2_STATE_INFO **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																clr_usb3_u2_cnt
Type																W1C
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	usb3_u2_cnt															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		clr_usb3_u2_cn t	**SW writes 1 to clear USB3 U2 counter in USB3 MAC.**
15:0		usb3_u2_cnt	**Calculates the number of times LTSSM enters U2 state** The counter will stop at 16'hFFFF.

1127247C UX_LFPS_TIMING_PARAMETER **00000026**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ux_exit_t12_t11_minus_300ns							
Type									RW							
Reset									0	0	1	0	0	1	1	0

Bit(s)	Mnemonic	Name	Description
7:0		ux_exit_t12_t1 1_minus_300ns	**UX_EXIT_LFPS t12_t11 timing minus 300ns in USB3 SPEC (because HW uses 300ns to detect ux exit LFPS)** Unit: 8ns. Default: 304ns

11272480 U1_LFPS_TIMING_PARAM **07D05858**

ETER_2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					u1_exit_no_lfps_tmout											
Type					RW											
Reset					0	1	1	1	1	1	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	u1_exit_t13_t11								u1_exit_t12_t10							
Type	RW								RW							
Reset	0	1	0	1	1	0	0	0	0	1	0	1	1	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16		u1_exit_no_lfp s_tmout	**U1_EXIT_LFPS no response timeout in USB3 SPEC** Unit: 1us. Default: 2000us
15:8		u1_exit_t13_t1 1	**U1_EXIT_LFPS t13_t11 timing in USB3 SPEC** Unit: 8ns. Default: 704ns
7:0		u1_exit_t12_t1 0	**U1_EXIT_LFPS t12_t10 timing in USB3 SPEC** Unit: 8ns. Default: 704ns

11272484 U2_LB_LFPS_TIMING_PARAMETER_1 **00500050**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					u2_lb_exit_t13_t11											
Type					RW											
Reset					0	0	0	0	0	1	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					u2_lb_exit_t12_t10											
Type					RW											
Reset					0	0	0	0	0	1	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16		u2_lb_exit_t13 _t11	**U2_LB_EXIT_LFPS t13_t11 timing in USB3 SPEC** Unit: 1us. Default: 80us
11:0		u2_lb_exit_t12 _t10	**U2_LB_EXIT_LFPS t12_t10 timing in USB3 SPEC** Unit: 1us. Default: 80us

11272488 U2_LB_LFPS_TIMING_PARAMETER_2 **000007D0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					u2_lb_exit_no_lfps_tmout											
Type					RW											

Reset					0	1	1	1	1	1	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0		u2_lb_exit_no_lfps_tmout	**U2_LB_EXIT_LFPS no response timeout in USB3 SPEC** Unit: 1us. Default: 2000us

1127248C U3_LFPS_TIMING_PARAMETER_1 **00500050**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			u3_exit_t13_t11													
Type			RW													
Reset			0	0	0	0	0	0	0	1	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			u3_exit_t12_t10													
Type			RW													
Reset			0	0	0	0	0	0	0	1	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:16		u3_exit_t13_t1 1	**U3_EXIT_LFPS t13_t11 timing in USB3 SPEC** Unit: 1us. Default: 80us
13:0		u3_exit_t12_t1 0	**U3_EXIT_LFPS t12_t10 timing in USB3 SPEC** Unit: 1us. Default: 80us

11272490 U3_LFPS_TIMING_PARAMETER_2 **00322710**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									send_u3_exit_lfps_wait_cy cle							
Type									RW							
Reset									0	0	1	1	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			u3_exit_no_lfps_tmout													
Type			RW													
Reset			1	0	0	1	1	1	0	0	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:16		send_u3_exit_lfps_wait_cycle	**The time LTSSM will wait for before sending U3 EXIT LFPS** Unit: 8ns. Default: 400ns
13:0		u3_exit_no_lfps_tmout	**U3_EXIT_LFPS no response timeout in USB3 SPEC** Unit: 1us. Default: 10000us

11272494 PING_LFPS_TIMING_PAR **000F2505**

AMETER

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											tx_p ing_ lfps _tbu rst					
Type											RW					
Reset											0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			rx_ping_lfps_tburst_max										rx_ping_lfps_tbur st_min			
Type			RW										RW			
Reset			1	0	0	1	0	1					0	1	0	1

Bit(s)	Mnemonic	Name	Description
21:16		tx_ping_lfps_t burst	**Timing value for USB3 MAC to send Ping.LFPS** Unit: 8ns. Default: 120ns
13:8		rx_ping_lfps_t burst_max	**Max. value for USB3 MAC to detect Ping.LFPS** Unit: 8ns. Default: 296ns
3:0		rx_ping_lfps_t burst_min	**Min. value for USB3 MAC to detect Ping.LFPS** Unit: 8ns. Default: 40ns

11272498 **POLLING_LFPS_TIMING_PARAMETER_1** **0000C83E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_polling_lfps_tburst_max									rx_polling_lfps_tburst_min						
Type	RW									RW						
Reset	1	1	0	0	1	0	0	0		0	1	1	1	1	1	0

Bit(s)	Mnemonic	Name	Description
15:8		rx_polling_lfp s_tburst_max	**Max. value for USB3 MAC to detect Polling.LFPS** Unit: 8ns. Default: 1600ns
6:0		rx_polling_lfp s_tburst_min	**Min. value for USB3 MAC to detect Polling.LFPS** Unit: 8ns. Default: 496ns

1127249C **POLLING_LFPS_TIMING_PARAMETER_2** **00100A7D**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												tx_p olli ng_l fps_ num				
Type												RW				
Reset												1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					tx_polling_lfps_t repeat				tx_polling_lfps_tburst							
Type					RW				RW							

Reset					1	0	1	0	0	1	1	1	1	1	0	1

Bit(s)	Mnemonic	Name	Description
20:16		tx_polling_lfp s_num	**Number of TX Polling.LFPS when LTSSM is in Polling.LFPS state**
11:8		tx_polling_lfp s_trepeat	**Timing value for USB3 MAC to send tRepeat of Polling.LFPS** Unit: 1us. Default: 10us
7:0		tx_polling_lfp s_tburst	**Timing value for USB3 MAC to send tBurst of Polling.LFPS** Unit: 8ns. Default: 1000ns

112724A0 UX_EXIT_LFPS_TIMING_PARAMETER **00000826**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_ux_exit_lfps_ref								rx_ux_exit_lfps_pipe							
Type	RW								RW							
Reset	0	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0

Bit(s)	Mnemonic	Name	Description
15:8		rx_ux_exit_lfp s_ref	**Timing value for USB3 MAC to detect UX_EXIT_LFPS when LTSSM is in U3 state and clock source is ref_ck** UX_EXIT_LFPS will be valid if LFPS is longer than 300ns. Unit: Depends on ref_ck period. Default: 320ns for ref_ck is 25MHz ref clk range: 10~100MHz 10MHz (100ns): 3 20MHz (50ns): 6 25MHz (40ns): 8 27 MHz (37ns): 9 50MHz (20ns): 15 100MHz (10ns): 30
7:0		rx_ux_exit_lfp s_pipe	**Timing value for USB3 MAC to detect UX_EXIT_LFPS when MAC operates in pipe_ck** UX_EXIT_LFPS will be valid if LFPS is longer than 300ns. Unit: 8ns. Default: 304ns

112724A4 P3_TIMING_PARAMETER **00F70000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									p3_enter_cycle				p3_exit_cycle			
Type									RW				RW			
Reset									1	1	1	1	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
23:20		p3_enter_cycle	**The clock cycle which ltssm must stay in P3 state to ensure the clock source is switched to ref_ck.** Default: 15 clock cycles of ref_ck
19:16		p3_exit_cycle	**The clock cycle which ltssm must stay in P3 exit state to ensure the clock source is switched to pipe_ck.** Default: 7 clock cycles of pipe_ck

112724A8 WARM_RESET_TIMING_PARAMETER 00006412

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	treset_tburst										tresetdelay					
Type	RW										RW					
Reset	0	1	1	0	0	1	0	0			0	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
15:8		treset_tburst	**Timing value for host to send warm reset LFPS to device** Unit: 1ms. Default: 100ms
5:0		tresetdelay	**Timing value for device detect warm reset LFPS from host** Unit: 1ms. Default: 18ms

112724AC UX_EXIT_TIMING_PARAMETER 000B71B0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													ux_exit_timer			
Type													RW			
Reset													1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ux_exit_timer															
Type	RW															
Reset	0	1	1	1	0	0	0	1	1	0	1	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:0		ux_exit_timer	**Timeout value from U1/U2 to U0 in USB3_MAC SPEC** Unit: 8ns. Default: 6ms

Bit(s)	Mnemonic	Name	Description

112724B0 REF_CK_PARAMETER **0000001A**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ref_1000ns							
Type									RW							
Reset									0	0	0	1	1	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0		ref_1000ns	**Defines how many ref_ck cycles are equal to 1000ns** Default: For 24MHz ref clk range: 10~100MHz Example: 10MHz: 10 20MHz: 20 24MHz: 24 25MHz: 25 27MHz: 27 50MHz: 50 100MHz: 100

1127250C LTSSM_TIMING_PARAMETER_1 **00060002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													mac_ 6ms			
Type													RW			
Reset													0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									mac_2ms							
Type									RW							
Reset									0	0	0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
19:16		mac_6ms	**Timeout value for Recovery.Configuration to enter SS.Inactive** Unit: 1ms. Default: 6ms
7:0		mac_2ms	**Timeout value for Polling.Idle, Recovery.Idle and Hot_RESET.Exit to enter SS.Inactive** Unit: 1ms. Default: 2ms

11272510 LTSSM_TIMING_PARAMET **0064000C**

ER_2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									mac_100ms							
Type									RW							
Reset									0	1	1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												mac_12ms				
Type												RW				
Reset												0	1	1	0	0

Bit(s)	Mnemonic	Name	Description
23:16		mac_100ms	**Timeout value for host to detect temination periodically in U2 or U3 state** Unit: 1ms. Default: 100ms
4:0		mac_12ms	**Timeout value** For: 1. Polling.Active, Polling.Configuration, Recovery.Active, HOT_RESET.Active to enter SS.Inactive. 2. Rx.Detect.Quite to enter Rx.Detect.Active. 3. SS.Inactive.Quite to enter SS.Inactive.Disconnect.Detect Unit: 1ms. Default: 12ms

11272514 LTSSM_TIMING_PARAMETER_3 **0168012C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							mac_360ms									
Type							RW									
Reset							0	1	0	1	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							mac_300ms									
Type							RW									
Reset							0	1	0	0	1	0	1	1	0	0

Bit(s)	Mnemonic	Name	Description
25:16		mac_360ms	**Timeout value for Polling.LFPS to enter compliance mode** Unit: 1ms. Default: 360ms
9:0		mac_300ms	**Timeout value for host to detect PING.LFPS from device in U1 state** Unit: 1ms. Default: 300ms

11272518 LTSSM_TIMING_PARAMETER_4 **000000BE**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									mac_200ms							
Type									RW							
Reset									1	0	1	1	1	1	1	0

Bit(s)	Mnemonic	Name	Description
7:0		mac_200ms	**Timeout value for device TX PING.LFPS periodically in U1 state** Unit: 1ms. Default: 190ms

1127251C **LTSSM_TIMING_PARAMETER_5** **03E803E8**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							power_change_time out_value									
Type							RW									
Reset							1	1	1	1	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							rxdetect_timeout_value									
Type							RW									
Reset							1	1	1	1	1	0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
25:16		power_change_timeout_value	**Timeout value for USB3 MAC to do power change but cannot sample phystatus** Unit: 1ms. Default: 1000ms
9:0		rxdetect_timeout_value	**Timeout value for USB3 MAC to do rxdetect but cannot sample phystatus** Unit: 1us. Default: 1000us

11272520 **LTSSM_RXDETECT_CTRL** **00003200**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxdetect_wait_time															rxdetect_wait_en
Type	RW															RW
Reset	0	0	1	1	0	0	1	0								0

Bit(s)	Mnemonic	Name	Description
15:8		rxdetect_wait_ time	**The idle time USB3 MAC will wait in Rxdetect.Active state before doing TX detect RX.** Unit: 1us. Default: 50us
0		rxdetect_wait_ en	**Defines if USB3 MAC waits for idle time in Rxdetect.Active state before doing TX detect RX**

Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable

11272528 PIPE_RXDATA_ERR_INTR_ENABLE **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														dec_8b10b_err_intr_en	disparity_err_intr_en	ebuf_err_intr_en
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2		dec_8b10b_err_ intr_en	(Device only) Enables dec_8b10b_err_intr
1		disparity_err_ intr_en	(Device only) Enables disparity_err_intr
0		ebuf_err_intr_ en	(Device only) Enables ebuf_err_intr

1127252C PIPE_RXDATA_ERR_INTR **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														dec_8b10b_err_intr	disparity_err_intr	ebuf_err_intr
Type														W1C	W1C	W1C
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2		dec_8b10b_err_ intr	(Device only) Sets up interrupt when detecting 8B/10B decoding error
1		disparity_err_ intr	(Device only) Sets up interrupt when detecting disparity error
0		ebuf_err_intr	(Device only) Sets up interrupt when detecting PHYD ebuf overflow or underflow

11272530 PIPE_LATCH **00000000**

_SELECT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													tx_signal_sel		rx_signal_sel	
Type													WO		WO	
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:2		tx_signal_sel	**For FPGA only** 00: Posedge pipe_ck latch pipe TX signal 01: Negedge pipe_ck latch pipe TX signal 10, 11: Reserved
1:0		rx_signal_sel	**For FPGA only** 00: Posedge pipe_ck latch pipe RX signal 01: Negedge pipe_ck latch pipe RX signal 10, 11: Reserved

11272534 LINK_STATE_MACHINE **3FFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	vbus_dbc_cycle															
Type	RW															
Reset	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								vbus_valid				ltssm				
Type								RU				RU				
Reset								0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		vbus_dbc_cycle	**VBUS dobunce cycle to set up vbus_valid signal**
8		vbus_valid	**VBUS signal after debouncing**
4:0		ltssm	**LTSSM state** 5'h00: ST_RESET 5'h01: ST_DISABLE 5'h02: ST_SS_INACTIVE_QUITE 5'h03: ST_SS_INACTIVE_DISC_DETECT 5'h04: ST_RX_DETECT_RESET 5'h05: ST_RX_DETECT_ACTIVE 5'h06: ST_RX_DETECT_QUITE 5'h07: ST_RX_DETECT_EXIT 5'h08: ST_POLLING_LFPS 5'h09: ST_POLLING_RXEQ 5'h0A: ST_POLLING_ACTIVE 5'h0B: ST_POLLING_CONFIGURATION 5'h0C: ST_POLLING_IDLE 5'h0D: ST_U0_STATE

Bit(s)	Mnemonic	Name	Description
			5'h0E: ST_U1_STATE 5'h0F: ST_U1_TX_PING 5'h10: ST_U1_EXIT 5'h11: ST_U2_STATE 5'h12: ST_U2_DETECT 5'h13: ST_U2_EXIT 5'h14: ST_U3_STATE 5'h15: ST_U3_DETECT 5'h16: ST_U3_EXIT 5'h17: ST_COMPLIANCE 5'h18: ST_RECOVERY_ACTIVE 5'h19: ST_RECOVERY_CONFIGURATION 5'h1A: ST_RECOVERY_IDLE 5'h1B: ST_LOOPBACK_ACTIVE_MASTER 5'h1C: ST_LOOPBACK_ACTIVE_SLAVE 5'h1D: ST_LOOPBACK_EXIT 5'h1E: ST_HOT_RESET_ACTIVE 5'h1F: ST_HOT_RESET_EXIT

11272538 MAC_FAST_SIMULATION **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											force_u0_to_u3	force_u0_to_u2	force_u0_to_u1	mac_speed_ms_to_us	bypass_warm_reset	
Type											RW	RW	RW	RW	RW	
Reset											0	0	0	0	0	

Bit(s)	Mnemonic	Name	Description
5		force_u0_to_u3	**(Simulation only) Forces LTSSM from U0 to U3**
4		force_u0_to_u2	**(Simulation only) Forces LTSSM from U0 to U2**
3		force_u0_to_u1	**(Simulation only) Forces LTSSM from U0 to U1**
2		mac_speed_ms_t o_us	**(Simulation only) SW can set up the register to speed up all ms timing vlaues to us timing value in mac clock domain.** Example: 300ms => 300us 12ms => 12us
1		bypass_warm_re set	**(Simulation only) Enters Rx.Detect.Reset and exits quickly to speed up simulation**

1127253C LTSSM_INTR_ENABLE **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														u3_resum	u3_lfps_	vbus_fal

														e_intr_en	tmout_intr_en	l_intr_en
Type														RW	RW	RW
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vbus_rise_intr_en	rxdet_success_intr_en	exit_u3_intr_en	exit_u2_intr_en	exit_u1_intr_en	enter_u3_intr_en	enter_u2_intr_en	enter_u1_intr_en	enter_u0_intr_en	recovery_intr_en	warm_rst_intr_en	hot_rst_intr_en	loopback_intr_en	compliance_intr_en	ss_disable_intr_en	ss_inactive_intr_en
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
18		u3_resume_intr _en	(Device only) Enables u3_resume_intr
17		u3_lfps_tmout_ intr_en	(Device only) Enables u3_lfps_tmout_intr
16		vbus_fall_intr _en	(Device only) Enables vbus_fall_intr
15		vbus_rise_intr _en	(Device only) Enables vbus_rise_intr
14		rxdet_success_ intr_en	(Device only) Enables rxdet_success_intr
13		exit_u3_intr_e n	(Device only) Enables exit_u3_intr
12		exit_u2_intr_e n	(Device only) Enables exit_u2_intr
11		exit_u1_intr_e n	(Device only) Enables exit_u1_intr
10		enter_u3_intr_ en	(Device only) Enables enter_u3_intr
9		enter_u2_intr_ en	(Device only) Enables enter_u2_intr
8		enter_u1_intr_ en	(Device only) Enables enter_u1_intr
7		enter_u0_intr_ en	(Device only) Enables enter_u0_intr
6		recovery_intr_ en	(Device only) Enables recovery_intr
5		warm_rst_intr_ en	(Device only) Enables warm_rst_intr
4		hot_rst_intr_e n	(Device only) Enables hot_rst_intr
3		loopback_intr_ en	(Device only) Enables loopback_intr
2		compliance_int r_en	(Device only) Enables compliance_intr
1		ss_disable_int r_en	(Device only) Enables ss_disable_intr
0		ss_inactive_in tr_en	(Device only) Enables ss_inactive_intr

11272540 LTSSM_INTR **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														u3_resume_intr	u3_lfps_tmout_intr	vbus_fall_intr
Type														W1C	W1C	W1C
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vbus_rise_intr	rxdet_success_intr	exit_u3_intr	exit_u2_intr	exit_u1_intr	enter_u3_int r	enter_u2_int r	enter_u1_int r	enter_u0_int r	recovery_int r	warm_rst_int r	hot_rst_intr	loopback_int r	compliance_intr	ss_disable_intr	ss_inactive_intr
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
18		u3_resume_intr	(Device only) Sets up interrupt when LTSSM enters U3 RESUME state
17		u3_lfps_tmout_ intr	(Device only) Sets up interrupt when TX U3 exits lfps timeout
16		vbus_fall_intr	(Device only) Sets up interrupt when vbus is not valid
15		vbus_rise_intr	(Device only) Sets up interrupt when vbus is valid
14		rxdet_success_ intr	(Device only) Sets up interrupt when USB3 termination is detected successfully
13		exit_u3_intr	(Device only) Sets up interrupt when LTSSM exits U3 state
12		exit_u2_intr	(Device only) Sets up interrupt when LTSSM exits U2 state
11		exit_u1_intr	(Device only) Sets up interrupt when LTSSM exits U1 state
10		enter_u3_intr	(Device only) Sets up interrupt when LTSSM enters U3 state
9		enter_u2_intr	(Device only) Sets up interrupt when LTSSM enters U2 state
8		enter_u1_intr	(Device only) Sets up interrupt when LTSSM enters U1 state
7		enter_u0_intr	(Device only) Sets up interrupt when LTSSM enters U0 state
6		recovery_intr	(Device only) Sets up interrupt when LTSSM enters Recovery state
5		warm_rst_intr	(Device only) Sets up interrupt when LTSSM enters Rx.Detect.Reset state (receive warm reset)
4		hot_rst_intr	(Device only) Sets up interrupt when LTSSM enters Hot.Reset state
3		loopback_intr	(Device only) Sets up interrupt when LTSSM enters Loopback state
2		compliance_int r	(Device only) Sets up interrupt when LTSSM enters Compliance state
1		ss_disable_int r	(Device only) Sets up interrupt when LTSSM enters SS.Disable state
0		ss_inactive_in tr	(Device only) Sets up interrupt when LTSSM enters SS.Inactive state

11272548 SKP_CNT **00000057**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										skp_symbol_num						
Type										RW						
Reset										1	0	1	0	1	1	1

Bit(s)	Mnemonic	Name	Description
6:0		skp_symbol_num	**Symbol number for USB3 MAC to send skp order set** Unit: 4 symbols. Default: (87+1)*4=352 symbols Each 354 symbols send one SKP OS.

Module name: ssusb_sifslv_u3phyd_t20soc_tphy Base address: (+11290900h)

Address	Name	Width	Register Function
11290900	PHYD_MIX0	32	SSUSB PHYD Mix 0 Register
11290904	PHYD_MIX1	32	SSUSB PHYD Mix 1 Register
11290908	PHYD_LFPS0	32	SSUSB PHYD LFPS 0 Register
1129090C	PHYD_LFPS1	32	SSUSB PHYD LFPS 1 Register
11290910	PHYD_IMPCAL0	32	SSUSB PHYD Impedance Calibration 0 Register
11290914	PHYD_IMPCAL1	32	SSUSB PHYD Impedance Calibration 1 Register
11290918	PHYD_TXPLL0	32	SSUSB PHYD Tx PLL 0 Register
1129091C	PHYD_TXPLL1	32	SSUSB PHYD Tx PLL 1 Register
11290920	PHYD_TXPLL2	32	SSUSB PHYD Tx PLL 2 Register
11290924	PHYD_FL0	32	SSUSB PHYD Frequency Lock Detection 0 Register
11290928	PHYD_MIX2	32	SSUSB PHYD Mix 2 Register
1129092C	PHYD_RX0	32	SSUSB PHYD Rx Register
11290930	PHYD_T2RLB	32	SSUSB PHYD T2R Loopback Register
11290934	PHYD_CPPAT	32	SSUSB PHYD CP Pattern Gen Register
11290938	PHYD_MIX3	32	SSUSB PHYD Mix 3 Register
1129093C	PHYD_EBUFCTL	32	SSUSB PHYD Ebuf Control Register
11290940	PHYD_PIPE0	32	SSUSB PHYD PIPE Control 0 Register
11290944	PHYD_PIPE1	32	SSUSB PHYD PIPE Control 1 Register
11290948	PHYD_MIX4	32	SSUSB PHYD Mix 4 Register
1129094C	PHYD_CKGEN0	32	SSUSB PHYD CKGEN Control 0 Register
11290950	PHYD_MIX5	32	
11290954	PHYD_RESERVED	32	SSUSB PHYD Reserved Register
11290958	PHYD_CDR0	32	SSUSB PHYD CDR Control 0 Register
1129095C	PHYD_CDR1	32	SSUSB PHYD CDR Control 1 Register
11290960	PHYD_PLL_0	32	SSUSB PHYD PLL Control 0 Register
11290964	PHYD_PLL_1	32	SSUSB PHYD PLL Control 1 Register
11290968	PHYD_BCN_DET_1	32	SSUSB PHYD BCN DET 1 Register
1129096C	PHYD_BCN_DET_2	32	SSUSB PHYD BCN DET 2 Register
11290970	EQ0	32	SSUSB PHYA EQ 0 Register
11290974	EQ1	32	SSUSB PHYA EQ 1 Register
11290978	EQ2	32	SSUSB PHYA EQ 2 Register
1129097C	EQ3	32	SSUSB PHYA EQ 3 Register
11290980	EQ_EYE0	32	SSUSB PHYA EYE 0 Register
11290984	EQ_EYE1	32	SSUSB PHYA EYE 1 Register
11290988	EQ_EYE2	32	SSUSB PHYA EYE 2 Register
1129098C	EQ_DFE0	32	
11290990	EQ_DFE1	32	
11290994	EQ_DFE2	32	
11290998	EQ_DFE3	32	
112909A0	PHYD_MON0	32	SSUSB PHYD Monitor 0 Register
112909A4	PHYD_MON1	32	SSUSB PHYD Monitor 1 Register
112909A8	PHYD_MON2	32	SSUSB PHYD Monitor 2 Register
112909AC	PHYD_MON3	32	SSUSB PHYD Monitor 3 Register
112909B0	PHYD_MON4	32	SSUSB PHYD Monitor 4 Register

Address	Name	Width	Register Function
112909B4	PHYD_MON5	32	SSUSB PHYD Monitor 5 Register
112909B8	PHYD_MON6	32	SSUSB PHYD Monitor 6 Register
112909BC	PHYD_MON7	32	SSUSB PHYD Monitor 7 Register
112909C0	PHYA_RX_MON0	32	SSUSB PHYA RX Monitor 0 Register
112909C4	PHYA_RX_MON1	32	SSUSB PHYA RX Monitor 1 Register
112909C8	PHYA_RX_MON2	32	SSUSB PHYA RX Monitor 2 Register
112909CC	PHYA_RX_MON3	32	SSUSB PHYA RX Monitor 3 Register
112909D0	PHYA_RX_MON4	32	SSUSB PHYA RX Monitor 4 Register
112909D4	PHYA_RX_MON5	32	SSUSB PHYA RX Monitor 5 Register
112909D8	PHYD_CPPAT2	32	SSUSB PHYD CP Pattern Gen Register2
112909DC	EQ_EYE3	32	SSUSB PHYA EYE 3 Register
112909E0	KBAND_OUT	32	KBAND_OUT
112909E4	KBAND_OUT1	32	KBAND_OUT1

11290900 PHYD_MIX0 SSUSB PHYD Mix 0 Register 00080210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_p_p3_tx_ng	rg_ssusb_tseq_en	rg_ssusb_tseq_polen	rg_ssusb_tseq_pol	rg_ssusb_p_p3_pclk_ng	rg_ssusb_tseq_th			rg_ssusb_prbs_berth							
Type	RW	RW	RW	RW	RW	RW			RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_disable_phy_u2_on	rg_ssusb_disable_phy_u2_off	rg_ssusb_prbs_en	rg_ssusb_bpslock	rg_ssusb_rtcomcnt				rg_ssusb_comcnt				rg_ssusb_prbsel_calib			
Type	RW	RW	RW	RW	RW				RW				RW			
Reset	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**p_p3_tx_ng**	rg_ssusb_p_p3_ tx_ng	**PCIe Host mode only** 1'b0: Gate TX clock at P2 1'b1: Not gate TX clock at P2
30	**tseq_en**	rg_ssusb_tseq_ en	**Enables TSEQ decoder** 0: Disable 1: Enable
29	**tseq_polen**	rg_ssusb_tseq_ polen	**Enables TSEQ polarity check** 0: Disable 1: Enable
28	**tseq_pol**	rg_ssusb_tseq_ pol	**Default TSEQ polarity check value** 0: Default 0 1: Default 1
27	**p_p3_pclk_ng**	rg_ssusb_p_p3_ pclk_ng	**PCIe host mode only** 1'b0: Gate PCLK clock at P2 1'b1: Does not gate PCLK clock at P2
26:24	**tseq_th**	rg_ssusb_tseq_ th	**TSEQ lock detect threshold**

Bit(s)	Mnemonic	Name	Description
23:16	**prbs_berth**	rg_ssusb_prbs_ berth	**PRBS bit error threshold** If bit error count is bigger than the threshold, rg_ssusb_prbs_passth will be deasserted.
15	**disable_phy_u2 _on**	rg_ssusb_disab le_phy_u2_on	**Disables PHY with USB2 PHY on** 1'b0: Enable PHY 1'b1: Disable PHY. PHY is at low power station.
14	**disable_phy_u2 _off**	rg_ssusb_disab le_phy_u2_off	**Disable PHY with USB2 PHY off** 1'b0: Enable PHY 1'b1: Disable PHY. PHY is at low power station.
13	**prbs_en**	rg_ssusb_prbs_ en	**Enables PRBS decoder** 0: Disable 1: Enable
12	**bpslock**	rg_ssusb_bpslo ck	**Bypasses symbol lock** 0: Disable 1: Enable
11:8	**rtcomcnt**	rg_ssusb_rtcom cnt	**com symbol retrack threshold**
7:4	**comcnt**	rg_ssusb_comcn t	**com symbol lock threshold**
3:0	**prbsel_calib**	rg_ssusb_prbse l_calib	**Selects prb_out_calib probe out signals** 4'b0000: prb_out_pllcal 4'b0001: prb_out_tx_impcal 4'b0010: prb_out_rx_impcal 4'b0011: prb_out_sigdet_cal 4'b0100: prb_out_rx_fldet 4'b0101: prb_out_ana2cal 4'b0110: prb_out_tximpsel 4'b0111: prb_out_rximpsel 4'b1000: prb_out_txband_cal

11290904 PHYD_MIX1 SSUSB PHYD Mix 1 Register 88B71300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**rg_ssusb_sleep_en**	**rg_ssusb_prbsel_pcs**			**rg_ssusb_txlfps_p rd**				**rg_ssusb_p_rx_pos_ck**	**rg_ssusb_p_tx_pos_ck**	**rg_ssusb_pdnctl**					
Type	RW	RW			RW				RW	RW	RW					
Reset	1	0	0	0	1	0	0	0	1	0	1	1	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**rg_ssusb_tx_drv_en**	**rg_ssusb_tx_drv_sel**	**rg_ssusb_tx_drv_dly**						**rg_ssusb_bert_en**	**rg_ssusb_scp_ th**			**rg_ssusb_scp_en**	**rg_ssusb_rxandsidec_test**		
Type	RW	RW	RW						RW	RW			RW	RW		
Reset	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**sleep_en**	rg_ssusb_sleep _en	**"ssusb_sleep" enable control** 0: Disable 1: Enable
30:28	**prbsel_pcs**	rg_ssusb_prbse l_pcs	**PCS probe select control** 0: ebuf 1: ansi decoder 2: train decoder 3: bert loopback 4: ansi encoder

Bit(s)	Mnemonic	Name	Description
			5: cp pattern 6: Reserved 7: Reserved
27:24	**txlfps_prd**	rg_ssusb_txlfp s_prd	**Tx LFPS period control** 1~16 (x 4nsec)
23	**p_rx_pos_ck**	rg_ssusb_p_rx_ pos_ck	**PCIe mode only** 0: Enable RX clock when Pos 1: Disable RX clock when Pos
22	**p_tx_pos_ck**	rg_ssusb_p_tx_ pos_ck	**PCIe mode only** 0: Enable TX clock when Pos 1: Disable TX clock when Pos
21:16	**pdnctl**	rg_ssusb_pdnct l	**[0]: TX pll p1 gating control** [1]: TX pll p2 gating control [2]: TX pll p3 powerdown control [3]: RX pll p1 powerdown control [4]: RX pll p2 powerdown control [5]: RX pll p3 powerdown control TX/RX pll will not be turned off if control is disabled respectively. 0: Disable 1: Enable
15	**tx_drv_en**	rg_ssusb_tx_dr v_en	**D/A register mode for da_ssusb_tx_drv_en**
14	**tx_drv_sel**	rg_ssusb_tx_dr v_sel	**Selects D/A "da_ssusb_tx_drv_en" mode** 0: Normal 1: D/A register mode
13:8	**tx_drv_dly**	rg_ssusb_tx_dr v_dly	**TX drive stable delay time** 1~64 (32*Tref_ck, for 25MHz~1.28usec)
7	**bert_en**	rg_ssusb_bert_ en	**Enables bert loop back register** 0: Disable 1: Enable
6:4	**scp_th**	rg_ssusb_scp_t h	**Single pattern detected threshold**
3	**scp_en**	rg_ssusb_scp_e n	**Enables single pattern detect** 0: Disable 1: Enable
2:0	**rxansidec_test**	rg_ssusb_rxans idec_test	**Option of testing ansi-decoder**

11290908 PHYD_LFPS0 SSUSB PHYD LFPS 0 Register 1E048219

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		rg_ssusb_lfps_pwd	rg_ssusb_force_lfps_pwd	rg_ssusb_rxlfps_ovf					rg_ssusb_p3_entry_sel	rg_ssusb_p3_entry	rg_ssusb_rxlfps_cdrsel		rg_ssusb_rxlfps_cdrth			
Type		RW	RW	RW					RW	RW	RW		RW			
Reset		0	0	1	1	1	1	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_lock5g_bloc k	rg_ssusb_tfifo_ext_d_sel	rg_ssusb_tfifo_no_extend	rg_ssusb_rxlfps_lob					rg_ssusb_txlfps_en	rg_ssusb_txlfps_sel	rg_ssusb_rxlfps_cdrlock	rg_ssusb_rxlfps_upb				
Type	RW	RW	RW	RW					RW	RW	RW	RW				
Reset	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
30	**lfps_pwd**	rg_ssusb_lfps_ pwd	**da_ssusb_lfps_pwd force mode register**
29	**force_lfps_pwd**	rg_ssusb_force _lfps_pwd	**da_ssusb_lfps_pwd force mode enable**
28:24	**rxlfps_ovf**	rg_ssusb_rxlfp s_ovf	**Rx LFPS detect period overflow threshold** If the received LFPS period is longer than the threshold, will not be treated as Rx LFPS anymore. 1~31 (x 4nsec)
23	**p3_entry_sel**	rg_ssusb_p3_en try_sel	**Selects D/A "da_ssusb_p3_entry" mode** 0: Normal 1: D/A register mode
22	**p3_entry**	rg_ssusb_p3_en try	**D/A register mode for da_ssusb_p3_entry**
21:20	**rxlfps_cdrsel**	rg_ssusb_rxlfp s_cdrsel	**CDR lock to 5G control modes** 0: Normal 1: p0 2: Sigal detect output 3: Register mode
19:16	**rxlfps_cdrth**	rg_ssusb_rxlfp s_cdrth	**Rx LFPS detect thresold for CDR control**
15	**lock5g_block**	rg_ssusb_lock5 g_block	**da_ssusb_cdr_lck2ref de-asserted condition option** 0: Non-block by txlfps_en 1: Block by txlfps_en
14	**tfifo_ext_d_se l**	rg_ssusb_tfifo _ext_d_sel	**Selects TFIFO TX data when rg_ssusb_tfifo_no_extend = 1'b0** 1'b0: 20'd0 1'b1: Last cycle data
13	**tfifo_no_exten d**	rg_ssusb_tfifo _no_extend	**TFIFO extend 1 clock cycle** 1'b0: Enable for PCIe mode 1'b1: Disable
12:8	**rxlfps_lob**	rg_ssusb_rxlfp s_lob	**Rx LFPS detect period upper bond** If the received LFPS period is shorter than the threshold, Rx LFPS will not be triggered. 1~31 (x 4nsec)
7	**txlfps_en**	rg_ssusb_txlfp s_en	**D/A register mode for da_ssusb_txlfps_en**
6	**txlfps_sel**	rg_ssusb_txlfp s_sel	**Selects D/A "da_ssusb_txlfps_en" mode** 0: Normal 1: D/A register mode
5	**rxlfps_cdrlock**	rg_ssusb_rxlfp s_cdrlock	**D/A register mode for da_ssusb_cdr_lck2ref**
4:0	**rxlfps_upb**	rg_ssusb_rxlfp s_upb	**Rx LFPS detect period upper bond** If the received LFPS period is longer than the threshold, Rx LFPS will not be triggered. 1~31 (x 4nsec)

1129090C PHYD_LFPS1 **SSUSB PHYD LFPS 1 Register** **00000150**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_s susb _rx_ imp_ bias				rg_ssusb_tx_imp_b ias						rg_ssusb_fwake_th					
Type	RW				RW						RW					
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		rg_s susb _p1_ entr y_se l	rg_s susb _p1_ entr y	rg_ssusb_rxlfps_udf					rg_ssusb_rxlfps_poidleth							
Type		RW	RW	RW					RW							
Reset		0	0	0	0	0	0	1	0	1	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**rx_imp_bias**	rg_ssusb_rx_imp_bias	**rg_ssusb_rx_imp_bias[2:0]: TX impsel offset, da_ssusb_rx_imp_sel +/-** **rg_ssusb_rx_imp_bias[2:0]: After impedance calibration done** rg_ssusb_rx_imp_bias[3]: 0 is plus, 1 is minus
27:24	**tx_imp_bias**	rg_ssusb_tx_imp_bias	**rg_ssusb_tx_imp_bias[2:0]: TX impsel offset, da_ssusb_tx_imp_sel +/-** **rg_ssusb_tx_imp_bias[2:0]: After impedance calibration done** rg_ssusb_tx_imp_bias[3]: 0 is plus, 1 is minus
21:16	**fwake_th**	rg_ssusb_fwake_th	**Fake wakeup detection threshold** For sleep wakeup triggered, if there is no real activity in the threshold time, enter sleep again. 1~64 (16*Tref_ck, for 25MHz ~0.64usec)
14	**p1_entry_sel**	rg_ssusb_p1_entry_sel	**Selects D/A "da_ssusb_p1_entry" mode** 0: Normal 1: D/A register mode
13	**p1_entry**	rg_ssusb_p1_entry	**D/A register mode for da_ssusb_p1_entry**
12:8	**rxlfps_udf**	rg_ssusb_rxlfps_udf	**Rx LFPS detect period underflow threshold** If the received LFPS period is shorter than the threshold, will not be treated as Rx LFPS anymore. 1~31 (x 4nsec)
7:0	**rxlfps_poidleth**	rg_ssusb_rxlfps_poidleth	**CDR po switch control idle delay** CDR switch will wait for the thresold before switching to 5G. 1~64 (256x4nsec ~1usec)

11290910 PHYD_IMPCAL0 SSUSB PHYD Impedance Calibration 0 Register 003F0E20

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**rg_ssusb_force_tx_impsel**	**rg_ssusb_tx_impcal_en**	**rg_ssusb_force_tx_impcal_en**	**rg_ssusb_tx_impsel**							**rg_ssusb_tx_impcal_calcyc**					
Type	RW	RW	RW	RW							RW					
Reset	0	0	0	0	0	0	0	0			1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**rg_ssusb_tx_impcal_stbcyc**					**rg_ssusb_tx_impcal_cyccnt**									
Type		RW					RW									
Reset		0	0	0	1	1	1	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**force_tx_impsel**	rg_ssusb_force_tx_impsel	**Enables forcing da_ssusb_tx_impsel** 0: Disable 1: Enable
30	**tx_impcal_en**	rg_ssusb_tx_impcal_en	**da_ssusb_tx_impcalib_en force mode register** When rg_ssusb_force_tx_impcal_en = 1, da_ssusb_tx_impcalib_en = rg_ssusb_tx_impcal_en.
29	**force_tx_impcal_en**	rg_ssusb_force_tx_impcal_en	**Enables DA_SSUSB_TX_IMPCALIB_EN force mode** 0: Disable 1: Enable
28:24	**tx_impsel**	rg_ssusb_tx_impsel	**For force da_ssusb_tx_imp_sel[4:0]** When rg_ssusb_force_tx_impsel = 1, da_ssusb_tx_imp_sel = rg_ssusb_tx_impsel.

Bit(s)	Mnemonic	Name	Description
21:16	**tximpcal_calcyc**	rg_ssusb_tx_impcal_calcyc	**TX impedance calibration cycle times**
14:10	**tx_impcal_stbcyc**	rg_ssusb_tx_impcal_stbcyc	**TX impedance calibration stable cycle times**
9:0	**tx_impcal_cyccnt**	rg_ssusb_tx_impcal_cyccnt	**TX impedance calibration cycle count/time**

11290914 PHYD_IMPCAL1 **SSUSB PHYD Impedance Calibration 1 Register** **003F0E20**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_force_rx_impsel	rg_ssusb_rx_impcal_en	rg_ssusb_force_rx_impcal_en	rg_ssusb_rx_impsel							rg_ssusb_rx_impcal_calcyc					
Type	RW	RW	RW	RW							RW					
Reset	0	0	0	0	0	0	0	0			1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		rg_ssusb_rx_impcal_stbcyc					rg_ssusb_rx_impcal_cyccnt									
Type		RW					RW									
Reset		0	0	0	1	1	1	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**force_rx_impsel**	rg_ssusb_force_rx_impsel	**Enables forcing da_ssusb_rx_impsel** 0: Disable 1: Enable
30	**rx_impcal_en**	rg_ssusb_rx_impcal_en	**da_ssusb_rx_impcalib_en force mode register** When rg_ssusb_force_rx_impcal_en = 1, da_ssusb_rx_impcalib_en = rg_ssusb_rx_impcal_en.
29	**force_rx_impcal_en**	rg_ssusb_force_rx_impcal_en	**Enables DA_SSUSB_RX_IMPCALIB_EN force mode** 0: Disable 1: Enable
28:24	**rx_impsel**	rg_ssusb_rx_im psel	**da_ssusb_tx_imp_sel[4:0] force mode register** When rg_ssusb_force_rx_impsel = 1, da_ssusb_rx_imp_sel = rg_ssusb_rx_impsel.
21:16	**rx_impcal_calcyc**	rg_ssusb_rx_impcal_calcyc	**RX impedance calibration cycle times**
14:10	**rx_impcal_stbcyc**	rg_ssusb_rx_impcal_stbcyc	**RX impedance calibration stable cycle times**
9:0	**rx_impcal_cyccnt**	rg_ssusb_rx_impcal_cyccnt	**RX impedance calibration cycle count/time**

11290918 PHYD_TXPLL **SSUSB PHYD Tx PLL 0 Register** **F030C801**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_txpll_dsen_cyc					rg_ssusb_txpll_on	rg_ssusb_force_txpll_on	rg_ssusb_txpll_stbcyc								
Type	RW					RW	RW	RW								

Reset	1	1	1	1	0	0	0	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_txpll_ncpochg_cyc				rg_ssusb_txpll_ncpoen_cyc									rg_ssusb_txpll_ddsrstb_cyc		
Type	RW				RW									RW		
Reset	1	1	0	0	1	0								0	0	1

Bit(s)	Mnemonic	Name	Description
31:27	**txpll_ddsen_cy c**	rg_ssusb_txpll _ddsen_cyc	**da_ssusb_pll_ddsen stable cycle counts** After da_ssusb_pll_ncpo_en is asserted, count rg_ssusb_txpll_ddsen_cyc, and da_ssusb_pll_ddsen will be asserted.
26	**txpll_on**	rg_ssusb_txpll _on	**Forces txpll on** When rg_ssusb_force_txpllon =1, da_ssusb_pll_pwd = ~rg_ssusb_txpll_on.
25	**force_txpllon**	rg_ssusb_force _txpllon	**Enables forcing txpll on** 0: Disable 1: Enable
24:16	**txpll_stbcyc**	rg_ssusb_txpll _stbcyc	**txpll_stable stable cycle counts** After da_ssusb_pll_ddsen is asserted, count rg_ssusb_txpll_stbcyc, and txpll_stable will be asserted
15:12	**txpll_ncpochg_ cyc**	rg_ssusb_txpll _ncpochg_cyc	**da_ssusb_pll_ncpo_chg stable cycle counts** After da_ssusb_pll_ddsrstb is asseted, count rg_ssusb_txpll_ncpochg_cyc, and da_ssusb_pll_ncpo_chg will be asserted.
11:10	**txpll_ncpoen_c yc**	rg_ssusb_txpll _ncpoen_cyc	**da_ssusb_pll_ncpo_en stable cycle counts** After da_ssusb_pll_pcw_ncp_chg is asserted, count rg_ssusb_txpll_ncpoen_cyc, and da_ssusb_pll_ncpo_en will be asserted.
2:0	**txpll_ddsrstb_ cyc**	rg_ssusb_txpll _ddsrstb_cyc	**da_ssusb_pll_dds_rstb stable cycles counts** After both da_ssusb_pll_dds_pwd and ad_ssusb_pll_vcocal_cplt are asserted, count rg_ssusb_txpll_ddsrstb_cyc, and da_ssusb_pll_dds_rstb will be asserted.

1129091C PHYD_TXPLL_1 SSUSB PHYD Tx PLL 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_pll_ncpo_en	rg_ssusb_pll_fifo_start_man		rg_ssusb_pll_ncpo_chg	rg_ssusb_pll_ddsrst b	rg_ssusb_pll_ddspwdb	rg_ssusb_pll_ddsen	rg_ssusb_pll_autok_vco	rg_ssusb_pll_pwd	rg_ssusb_rx_afe_pwd	rg_ssusb_pll_tcadj					
Type	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW					
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_force_cdr_tcadj	rg_ssusb_force_cdr_autok_vco	rg_ssusb_force_cdr_pwd	rg_ssusb_force_pll_ncpo_en	rg_ssusb_force_pll_fifo_start_man		rg_ssusb_force_pll_ncpo_chg	rg_ssusb_force_pll_dds_rstb	rg_ssusb_force_pll_dds_pwdb	rg_ssusb_force_pll_ddsen	rg_ssusb_force_pll_tcadj	rg_ssusb_force_pll_autok_vco	rg_ssusb_force_pll_pwd	rg_ssusb_flt_1_dispeerr_b		
Type	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW		

Reset	0	0	0	0	0		0	0	0	0	0	0	0	0		

Bit(s)	Mnemonic	Name	Description
31	**pll_ncpo_en**	rg_ssusb_pll_ncpo_en	**da_ssusb_pll_ncpo_en force mode register**
30	**pll_fifo_start _man**	rg_ssusb_pll_fifo_start_man	**da_ssusb_pll_fifo_start_man force mode register**
28	**pll_ncpo_chg**	rg_ssusb_pll_ncpo_chg	**da_ssusb_pll_pcw_ncpo_chg force mode register**
27	**pll_dds_rstb**	rg_ssusb_pll_dds_rstb	**da_ssusb_pll_dds_rstb force mode register**
26	**pll_dds_pwdb**	rg_ssusb_pll_dds_pwdb	**da_ssusb_pll_dds_pwdb force mode register**
25	**pll_ddsen**	rg_ssusb_pll_d dsen	**da_ssusb_pll_ddsen force mode register**
24	**pll_autok_vco**	rg_ssusb_pll_autok_vco	**da_ssusb_pll_autok_vco force mode register**
23	**pll_pwd**	rg_ssusb_pll_p wd	**da_ssusb_pll_pwd force mode register**
22	**rx_afe_pwd**	rg_ssusb_rx_af e_pwd	**da_ssusb_rx_afe_pwd force mode register**
21:16	**pll_tcadj**	rg_ssusb_pll_t cadj	**da_ssusb_pll_tcadj force mode register**
15	**force_cdr_tcad j**	rg_ssusb_force_cdr_tcadj	**Enables da_ssusb_cdr_tcadj force mode** 0: Disable 1: Enable
14	**force_cdr_auto k_vco**	rg_ssusb_force_cdr_autok_vco	**Enables da_ssusb_cdr_autok_vco force mode** 0: Disable 1: Enable
13	**force_cdr_pwd**	rg_ssusb_force_cdr_pwd	**Enables da_ssusb_cdr_pwd force mode** 0: Disable 1: Enable
12	**force_pll_ncpo _en**	rg_ssusb_force_pll_ncpo_en	**Enables da_ssusb_pll_ncpo_en force mode** 0: Disable 1: Enable
11	**force_pll_fifo _start_man**	rg_ssusb_force_pll_fifo_star t_man	**Enables da_ssusb_pll_fifo_start_man force mode** 0: Disable 1: Enable
9	**force_pll_ncpo _chg**	rg_ssusb_force_pll_ncpo_chg	**Enables da_ssusb_pll_pcw_ncpo_chg force mode** 0: Disable 1: Enable
8	**force_pll_dds_ rstb**	rg_ssusb_force_pll_dds_rstb	**Enables da_ssusb_pll_pcw_ncpo_chg force mode** 0: Disable 1: Enable
7	**force_pll_dds_ pwdb**	rg_ssusb_force_pll_dds_pwdb	**Enables da_ssusb_pll_dds_pwdb force mode** 0: Disable 1: Enable
6	**force_pll_ddse n**	rg_ssusb_force_pll_ddsen	**Enables da_ssusb_pll_ddsen force mode** 0: Disable 1: Enable
5	**force_pll_tcad j**	rg_ssusb_force_pll_tcadj	**Enables da_ssusb_pll_tcadj force mode** 0: Disable 1: Enable
4	**force_pll_auto k_vco**	rg_ssusb_force_pll_autok_vco	**Enables da_ssusb_pll_autok_vco force mode** 0: Disable 1: Enable
3	**force_pll_pwd**	rg_ssusb_force_pll_pwd	**Enables da_ssusb_pll_pwd force mode** 0: Disable 1: Enable
2	**flt_1_disperr_ b**	rg_ssusb_flt_1_disperr_b	

Bit(s)	Mnemonic	Name	Description

11290920 PHYD_TXPLL_2 SSUSB PHYD Tx PLL 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_tx_lfps_en	rg_ssusb_force_tx_lfps_en	rg_ssusb_tx_lfps	rg_ssusb_force_tx_lfps	rg_ssusb_rxpll_stb	rg_ssusb_txpll_stb	rg_ssusb_force_rxpll_stb	rg_ssusb_force_txpll_stb								rg_ssusb_rxpll_refcksel
Type	RW	RW	RW	RW	RW	RW	RW	RW								RW
Reset	0	0	0	0	0	0	0	0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					rg_ssusb_rxpll_stbmode	rg_ssusb_rxpll_on	rg_ssusb_force_rxpllon	rg_ssusb_force_rx_afe_pwd	rg_ssusb_cdr_autok_vco	rg_ssusb_cdr_pwd	rg_ssusb_cdr_tcadj					
Type					RW	RW	RW	RW	RW	RW	RW					
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**tx_lfps_en**	rg_ssusb_tx_lf ps_en	**da_ssusb_tx_lfps_en force mode register**
30	**rg_ssusb_force _tx_lfps_en**	rg_ssusb_force _tx_lfps_en	**Enables da_ssusb_tx_lfps_en force mode**
29	**tx_lfps**	rg_ssusb_tx_lf ps	**da_ssusb_tx_lfps force mode register**
28	**force_tx_lfps**	rg_ssusb_force _tx_lfps	**Enables da_ssusb_tx_lfps force mode**
27	**rxpll_stb**	rg_ssusb_rxpll _stb	**rxpll_stb force mode register**
26	**txpll_stb**	rg_ssusb_txpll _stb	**txpll_stb force mode register**
25	**force_rxpll_st b**	rg_ssusb_force _rxpll_stb	**Enables rxpll_stb force mode**
24	**force_txpll_st b**	rg_ssusb_force _txpll_stb	**Enables txpll_stb force mode**
16	**rxpll_refcksel**	rg_ssusb_rxpll _refcksel	**rxpll on base on xtalbias_stable or syspll_stable** 0: syspll_stable 1: xtalbias_stable
11	**rxpll_stbmode**	rg_ssusb_rxpll _stbmode	**rxpll_stable mode** 0: rxpll_stable indicates rxpll lock and rxpll stable time out after rxpll is turned on. 1: rxpll_stable indicates rxpll_lock.
10	**rxpll_on**	rg_ssusb_rxpll _on	**Forces rxpll on** When rg_ssusb_force_rxpllon =1, da_ssusb_cdr_pwd = ~rg_ssusb_rxpll_on.
9	**force_rxpllon**	rg_ssusb_force _rxpllon	**Enables forcing rxpll on**
8	**force_rx_afe_p wd**	rg_ssusb_force _rx_afe_pwd	**Enables da_ssusb_rx_afe_pwd force mode** 0: Disable 1: Enable
7	**cdr_autok_vco**	rg_ssusb_cdr_a utok_vco	**da_ssusb_cdr_autok_vco force mode register** 0: Disable 1: Enable
6	**cdr_pwd**	rg_ssusb_cdr_p wd	**da_ssusb_cdr_pwd force mode register**
5:0	**cdr_tcadj**	rg_ssusb_cdr_t cadj	**da_ssusb_cdr_tcadj force mode register**

Bit(s)	Mnemonic	Name	Description

11290924 PHYD_FL0 SSUSB PHYD Frequency Lock Detection 0 Register 00640064

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_rx_fl_target															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_rx_fl_cyclecnt															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

Bit(s)	Mnemonic	Name	Description
31:16	**rx_fl_target**	rg_ssusb_rx_fl _target	RX frequency lock detection - ref counter detection cycle counts target
15:0	**rx_fl_cyclecnt**	rg_ssusb_rx_fl _cyclecnt	RX frequency lock detection - fb counter detection cycle counts

11290928 PHYD_MIX2 SSUSB PHYD Mix 2 Register 00040204

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_rx_eq_rst	rg_ssusb_rx_eq_rst_sel	rg_ssusb_rxval_rst	rg_s susb _rxv al_c nt										rg_ssusb_cdros_en	rg_ssusb_cdr_lckop	
Type	RW	RW	RW	RW										RW	RW	
Reset	0	0	0	0	0	0	0	0						1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					rg_ssusb_rx_fl_lo ckth				rg_ssusb_rx_fl_offset							
Type					RW				RW							
Reset					0	0	1	0	0	0	0	0	0	1	0	0

Bit(s)	Mnemonic	Name	Description
31	**rx_eq_rst**	rg_ssusb_rx_eq _rst	**D/A register mode for da_ssusb_eq_rst**
30	**rx_eq_rst_sel**	rg_ssusb_rx_eq _rst_sel	**Selects D/A "da_ssusb_eq_rst" mode**
29	**rxval_rst**	rg_ssusb_rxval _rst	**Resets RX path valid register** 0: Disable 1: Enable
28:24	**rxval_cnt**	rg_ssusb_rxval _cnt	**Enables RX path delay from CDR lock to data** 1~32 x (256*4nsec)
18	**cdros_en**	rg_ssusb_cdros _en	**Enables CDR offset calibration** 0: Disable 1: Enable
17:16	**cdr_lckop**	rg_ssusb_cdr_l ckop	**[0]: RX pll ready force mode** 1: Force RX pll ready high [1]: RX pll ready selection control
11:8	**rx_fl_lockth**	rg_ssusb_rx_fl _lockth	**RX frequency lock detection lock threshold**
7:0	**rx_fl_offset**	rg_ssusb_rx_fl _offset	**RX frequency lock detection - detection cycle offset tolerance counts**

1129092C PHYD_RX0 SSUSB PHYD Rx Register 00000043

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_t2rlb_berth								rg_ssusb_t2rlb_pat							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_t2rlb_en	rg_ssusb_t2rlb_bpscramb	rg_ssusb_t2rlb_serial	rg_ssusb_t2rlb_mode		rg_ssusb_rx_saosc_en	rg_ssusb_rx_saosc_en_sel	rg_ssusb_rx_dfe_option	rg_ssusb_rx_dfe_en	rg_ssusb_rx_dfe_en_sel	rg_ssusb_rx_eq_en	rg_ssusb_rx_eq_en_sel	rg_ssusb_rx_saosc_rst	rg_ssusb_rx_saosc_rst_sel	rg_ssusb_rx_dfe_rst	rg_ssusb_rx_dfe_rst_sel
Type	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:24	**t2rlb_berth**	rg_ssusb_t2rlb _berth	**T2R loop back bit error threshold**
23:16	**t2rlb_pat**	rg_ssusb_t2rlb _pat	**T2R loop back pattern**
15	**t2rlb_en**	rg_ssusb_t2rlb _en	**Enables T2R loop back** 0: Disable 1: Enable
14	**t2rlb_bpscramb**	rg_ssusb_t2rlb _bpscramb	**T2R loop back bypass scrambler**
13	**t2rlb_serial**	rg_ssusb_t2rlb _serial	**T2R loop back serial mode**
12:11	**t2rlb_mode**	rg_ssusb_t2rlb _mode	**[0]: Enable T2R loop back mode** [1]: T2R loop back parallel mode 0: Disable 1: Enable
10	**rx_saosc_en**	rg_ssusb_rx_saosc_en	**D/A register mode for da_ssusb_saosc_en**
9	**rx_saosc_en_sel**	rg_ssusb_rx_saosc_en_sel	**Selects D/A "da_ssusb_saosc_en" mode**
8	**rx_dfe_option**	rg_ssusb_rx_dfe_option	**Option control for da_ssusb_dfe_en**
7	**rx_dfe_en**	rg_ssusb_rx_dfe_en	**D/A register mode for da_ssusb_dfe_en**
6	**rx_dfe_en_sel**	rg_ssusb_rx_dfe_en_sel	**Selects D/A "da_ssusb_dfe_en" mode**
5	**rx_eq_en**	rg_ssusb_rx_eq_en	**D/A register mode for da_ssusb_eq_en**
4	**rx_eq_en_sel**	rg_ssusb_rx_eq_en_sel	**Selects D/A "da_ssusb_eq_en" mode**
3	**rx_saosc_rst**	rg_ssusb_rx_saosc_rst	**D/A register mode for da_ssusb_saosc_rst**
2	**rx_saosc_rst_sel**	rg_ssusb_rx_saosc_rst_sel	**Selects D/A "da_ssusb_saosc_rst" mode**
1	**rx_dfe_rst**	rg_ssusb_rx_dfe_rst	**D/A register mode for da_ssusb_dfe_rst**
0	**rx_dfe_rst_sel**	rg_ssusb_rx_dfe_rst_sel	**Selects D/A "da_ssusb_dfe_rst" mode**

11290930 PHYD_T2RLB SSUSB PHYD T2R Loopback Register 006A0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ip_u3_port_power	force_ip_u3_port_pow	rg_u3_phyd_rst_b_dis	rg_ssusb_eqtrain_ch_	rg_ssusb_prb_out_cpp	rg_ssusb_bpansienc	rg_ssusb_valid_en	rg_ssusb_ebuf_srst	rg_ssusb_k_emp				rg_ssusb_k_ful			

		er		mode	at											
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW				RW			
Reset	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_t2rlb_bd atrst					rg_ssusb_p_t2rlb_skp_en	rg_ssusb_t2rlb_pat mode		rg_ssusb_t2rlb_tseqcnt							
Type	RW					RW	RW		RW							
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		rg_ip_u3_port_ power	
30		force_ip_u3_po rt_power	
29		rg_u3_phyd_rst _b_dis	
28	**eqtrain_ch_mod e**	rg_ssusb_eqtra in_ch_mode	**Changes criteria of half-full decision in eqtraining mode** 0: Normal mode 1: Change mode
27	**prb_out_cppat**	rg_ssusb_prb_o ut_cppat	**Probe selection control** 0: cp pattern 1: PRBS pattern
26	**bpansienc**	rg_ssusb_bpans ienc	**Bypasses signal through ansi encoder** 0: Does not bypass 1: Bypass
25	**valid_en**	rg_ssusb_valid _en	**Option of valid enable** 0: Disable 1: Enable
24	**ebuf_srst**	rg_ssusb_ebuf_ srst	**Reset of rgs_ssusb_ebuf_ovf and rgs_ssusb_ebuf_udf** 0: No reset 1: Reset
23:20	**ssusb_k_emp**	rg_ssusb_k_emp	**Parameter for determining the half-empty level in read domain**
19:16	**ssusb_k_ful**	rg_ssusb_k_ful	**Parameter for determining the half-full level in write domain**
15:12	**t2rlb_bdatrst**	rg_ssusb_t2rlb _bdatrst	**T2R loop back BDAT reset period control**
10	**p_t2rlb_skp_en**	rg_ssusb_p_t2r lb_skp_en	**PCIe mode only, t2rlb pattern with SKP-OS** 1'b0: Disable 1'b1: Enable
9:8	**t2rlb_patmode**	rg_ssusb_t2rlb _patmode	**T2R loop back pattern modes** 0: Increase 1: Decrease 2: From rg_ssusb_t2rlb_pat 3: All 0
7:0	**t2rlb_tseqcnt**	rg_ssusb_t2rlb _tseqcnt	**T2R loop back TSEQ length control**

11290934 PHYD_CPPAT SSUSB PHYD CP Pattern Gen Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name								rg_ssusb_cppat_program_en		rg_ssusb_cppat_toz		rg_ssusb_cppat_prbs_en	rg_ssusb_cppat_out_tmp2			
Type								RW		RW		RW	RW			
Reset								0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_cppat_out_tmp1								rg_ssusb_cppat_out_tmp0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24	**cppat_program_ en**	rg_ssusb_cppat _program_en	**Enables progrmmable pattern output** 0: Disable 1: Enable
22:21	**cppat_toz**	rg_ssusb_cppat _toz	**Decides number of successive 0's and 1's in compliance mode** 0: 60 1: 120 2: 180 3: 240
20	**cppat_prbs_en**	rg_ssusb_cppat _prbs_en	**Compliance pattern change to PRBS** 0: Compliance pattern 1: PRBS pattern
19:16	**cppat_out_tmp2**	rg_ssusb_cppat _out_tmp2	**Programmable pattern (tx_40b_cppat_program[19:16]) for compliance debugging, bit 19~0** For bit 39~20, refer to rg_ssusb_cppat_out_h_tmp*.
15:8	**cppat_out_tmp1**	rg_ssusb_cppat _out_tmp1	**Programmable pattern (tx_40b_cppat_program[15:8]) for compliance debugging, bit 19~0** For bit 39~20, refer to rg_ssusb_cppat_out_h_tmp*.
7:0	**cppat_out_tmp0**	rg_ssusb_cppat _out_tmp0	**Programmable pattern (tx_40b_cppat_program[7:0]) for compliance debugging, bit 19~0** For bit 39~20, refer to rg_ssusb_cppat_out_h_tmp*.

11290938 PHYD_MIX3 SSUSB PHYD Mix 3 Register 400000D0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_cdr_tcadj_minus	rg_ssusb_p_cdros_en		rg_ssusb_p_p2_tx_drv_dis		rg_ssusb_cdr_tcadj_offset			rg_ssusb_pll_tcadj_minus			rg_ssusb_force_pll_bias_lpf_en	rg_ssusb_pll_bias_lpf_en	rg_ssusb_pll_tcadj_offset		
Type	RW	RW		RW		RW			RW			RW	RW	RW		
Reset	0	1		0		0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_force_pll_s	rg_ssusb_pll_sscen	rg_ssusb_force_cdr_p	rg_ssusb_cdr_pi_pwd	rg_ssusb_cdr_pi_mode		rg_ssusb_txpll_sscen_cyc									

	scen		i_pwd													
Type	RW	RW	RW	RW	RW		RW									
Reset	0	0	0	0	0		0	0	1	1	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**cdr_tcadj_minus**	rg_ssusb_cdr_tcadj_minus	**da_ssusb_cdr_tcadj = da_ssusb_tx_impsel +/- rg_ssusb_cdr_tcadj_offset** +/- depends on rg_ssusb_cdr_tcadj_minus. 0: - 1: +
30	**p_cdros_en**	rg_ssusb_p_cdros_en	**(PCIe mode only) Enables cdros calibration when rate operated at 5G** 1'b0: Disable 1'b1: Enable
28	**p_p2_tx_drv_dis**	rg_ssusb_p_p2_tx_drv_dis	**(PCIe mode only) Disables DA_SSUSB_TX_DRV_EN when powerdown=2'b10** 1'b0: Enable DA_SSUSB_TX_DRV_EN 1'b1: Disable DA_SSUSB_TX_DRV_EN
26:24	**cdr_tcadj_offset**	rg_ssusb_cdr_tcadj_offset	**da_ssusb_cdr_tcadj = da_ssusb_tx_impsel +/- rg_ssusb_cdr_tcadj_offset** +/- depends on rg_ssusb_cdr_tcadj_minus. rg_ssusb_cdr_tcadj_minus=1: - rg_ssusb_cdr_tcadj_minus=0: +
23	**pll_tcadj_minus**	rg_ssusb_pll_tcadj_minus	**da_ssusb_pll_tcadj = da_ssusb_tx_impsel +/- rg_ssusb_pll_tcadj_offset** +/- depends on rg_ssusb_pll_tcadj_minus. 0: - 1: +
20	**force_pll_bias_lpe_en**	rg_ssusb_force_pll_bias_lpf_en	**Enables da_ssusb_pll_bias_lpe_en force mode**
19	**pll_bias_lpe_en**	rg_ssusb_pll_bias_lpf_en	**da_ssusb_pll_bias_lpe_en force mode register**
18:16	**pll_tcadj_offset**	rg_ssusb_pll_tcadj_offset	**da_ssusb_pll_tcadj = da_ssusb_tx_impsel +/- rg_ssusb_pll_tcadj_offset** +/- depend on rg_ssusb_pll_tcadj_minus. rg_ssusb_pll_tcadj_minus= 1: - rg_ssusb_pll_tcadj_minus= 0: +
15	**force_pll_sscen**	rg_ssusb_force_pll_sscen	**Enables da_ssusb_pll_ssc_en force mode**
14	**pll_sscen**	rg_ssusb_pll_sscen	**da_ssusb_pll_ssc_en force mode register**
13	**force_cdr_pi_pwd**	rg_ssusb_force_cdr_pi_pwd	**Enables da_ssusb_cdr_pi_pwd force mode**
12	**cdr_pi_pwd**	rg_ssusb_cdr_pi_pwd	**da_ssusb_cdr_pi_pwd force mode register**
11	**cdr_pi_mode**	rg_ssusb_cdr_pi_mode	**PI mode control** 1'b0: CLK0/CLK90 with PI mode 1'b1: CLK0/CLK90 without PI mode
9:0	**txpll_sscen_cyc**	rg_ssusb_txpll_sscen_cyc	**da_ssusb_pll_ssc_en stable cycle counts** After da_ssusb_pll_ddsen asserted, count rg_ssusb_txpll_sscen_cyc, and da_ssusb_pll_ssc_en will be asserted.

1129093C PHYD_EBUFCTL **SSUSB PHYD Ebuf Control Register** **0044AA00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_ebufctl															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_ebufctl															
Type	RW															
Reset	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ebufctl**	rg_ssusb_ebufc tl	**Parameters for control function** [0]: Reset wrfull_start [2:1]: Probe output control [11:8]: mid_ful_start [15:12]: mid_ful_rxeq [19:16]: mid_emp_start [23:20]: mid_emp_rxeq

11290940 PHYD_PIPE0 SSUSB PHYD PIPE Control 0 Register 00000060

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		rg_ssusb_rxtermination	rg_ssusb_rxeqtraining	rg_ssusb_rxpolarity	rg_ssusb_txdeemph		rg_ssusb_powerdown		rg_ssusb_txonezeros	rg_ssusb_txelecidle	rg_ssusb_txdetectrx	rg_ssusb_pipe_sel	rg_ssusb_txdatak			
Type		RW	RW	RW	RW		RW		RW	RW	RW	RW	RW			
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_cdr_stable_sel	rg_ssusb_cdr_stable	rg_ssusb_cdr_rstb_sel	rg_ssusb_cdr_rstb	rg_ssusb_frc_pipe_powerdown					rg_ssusb_p_txbcn_dis	rg_ssusb_p_error_sel		rg_ssusb_txmargin			rg_ssusb_txcompliance
Type	RW	RW	RW	RW	RW					RW	RW		RW			RW
Reset	0	0	0	0	0					1	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30	**rxtermination**	rg_ssusb_rxter mination	**Register control for PIPE bypass mode**
29	**rxeqtraining**	rg_ssusb_rxeqt raining	**Register control for PIPE bypass mode**
28	**rxpolarity**	rg_ssusb_rxpol arity	**Register control for PIPE bypass mode**
27:26	**txdeemph**	rg_ssusb_txdee mph	**Register control for PIPE bypass mode**
25:24	**powerdown**	rg_ssusb_power down	**Register control for PIPE bypass mode**
23	**txonezseros**	rg_ssusb_txone szeros	**Register control for PIPE bypass mode**
22	**txelecidle**	rg_ssusb_txele cidle	**Register control for PIPE bypass mode**
21	**txdetectrx**	rg_ssusb_txdet ectrx	**Register control for PIPE bypass mode**
20	**pipe_sel**	rg_ssusb_pipe_ sel	**Register control enable for PIPE bypass mode** 0: Disable 1: Enable
19:16	**txdatak**	rg_ssusb_txdat ak	**Register control for PIPE bypass mode**
15	**cdr_stable_sel**	rg_ssusb_cdr_s table_sel	**Selects D/A "da_ssusb_cdr_stable" mode**
14	**cdr_stable**	rg_ssusb_cdr_s table	**D/A register mode for da_ssusb_cdr_stable**
13	**cdr_rstb_sel**	rg_ssusb_cdr_r stb_sel	**Selects D/A "da_ssusb_cdr_rstb" mode**

Bit(s)	Mnemonic	Name	Description
12	**cdr_rstb**	rg_ssusb_cdr_r stb	**D/A register mode for da_ssusb_cdr_rstb**
11		rg_ssusb_frc_p ipe_powerdown	
6	**p_txbcn_dis**	rg_ssusb_p_txb cn_dis	**Disables PCIe beacon**
5:4	**p_error_sel**	rg_ssusb_p_err or_sel	**Continuous RX error occur sel for judging RX end** 2'b00: Continuous 7 symbols as RX end 2'b01: Continuous 15 symbols as RX end 2'b10: Continuous 31 symbols as RX end 2'b11: Continuous 63 symbols as RX end
3:1	**txmargin**	rg_ssusb_txmar gin	**Register control for PIPE bypass mode**
0	**txcompliance**	rg_ssusb_txcom pliance	**Register control for PIPE bypass mode**

11290944 PHYD_PIPE1 SSUSB PHYD PIPE Control 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_txdata															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_txdata															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**txdata**	rg_ssusb_txdat a	Register control for PIPE bypass mode

11290948 PHYD_MIX4 SSUSB PHYD Mix 4 Register 27000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			rg_s susb _cdr os_c nt													rg_s susb _t2r lb_b er_e n
Type			RW													RW
Reset			1	0	0	1	1	1								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_t2rlb_ber_rate															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:24	**cdros_cnt**	rg_ssusb_cdros _cnt	CDR offset calibration latency control
16	**t2rlb_ber_en**	rg_ssusb_t2rlb _ber_en	Enables T2R loop back bit error insertion
15:0	**t2rlb_ber_rate**	rg_ssusb_t2rlb _ber_rate	T2R loop back bit error rate control

1129094C PHYD_CKGEN — SSUSB PHYD CKGEN Control 0 Register — 08000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					rg_ssusb_rfifo_implat	rg_ssusb_tfifo_psel										
Type					RW	RW										
Reset					1	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							rg_ssusb_ckgen_psel									rg_ssusb_rxck_inv
Type							RW									RW
Reset							0	0								0

Bit(s)	Mnemonic	Name	Description
27	**rfifo_implat**	rg_ssusb_rfifo _implat	Improves rfifo latency
26:24	**tfifo_psel**	rg_ssusb_tfifo _psel	Selects tfifo probe out
9:8	**ckgen_psel**	rg_ssusb_ckgen _psel	Selects ssusb_ckgen_top probe out
0	**rxck_inv**	rg_ssusb_rxck_ inv	Enables rx250m clock inversion

11290950 PHYD_MIX5 — 00000030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_prb_sel															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						rg_ssusb_rxpll_stbcyc										
Type						RW										
Reset						0	0	0	0	0	1	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	**prb_sel**	rg_ssusb_prb_s el	**Probe selection control**
10:0	**rxpll_stbcyc**	rg_ssusb_rxpll _stbcyc	**rxpll stable cycles counts** After da_ssusb_cdr_pwd = 0 and ad_ssusb_cdr_vcocal_cplt = 1, count rg_ssusb_rxpll_stbcyc, and rxpll_stable will be asserted.

11290954 PHYD_RESERVED — SSUSB PHYD Reserved Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_phyd_reserve															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	rg_ssusb_phyd_reserve															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**phyd_reserve**	rg_ssusb_phyd_ reserve	**[0]: Select Gen2 1 EIOS detection** 1b0: Continuous EIOS 1b1: Non-continuous EIOS

11290958 PHYD_CDR0 SSUSB PHYD CDR Control 0 Register F80E0E0E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_s susb _cdr _bic _ltr				rg_s susb _cdr _bic _ltd o							rg_ssusb_cdr_bc_ltd1				
Type	RW				RW							RW				
Reset	1	1	1	1	1	0	0	0				0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				rg_ssusb_cdr_bc_ltr								rg_ssusb_cdr_bc_ltdo				
Type				RW								RW				
Reset				0	1	1	1	0				0	1	1	1	0

Bit(s)	Mnemonic	Name	Description
31:28	**cdr_bic_ltr**	rg_ssusb_cdr_b ic_ltr	Register control for CDR bic ltr
27:24	**cdr_bic_ltdo**	rg_ssusb_cdr_b ic_ltdo	Register control for CDR bic ltd
20:16	**cdr_bc_ltd1**	rg_ssusb_cdr_b c_ltd1	Register control for CDR bc ltd
12:8	**cdr_bc_ltr**	rg_ssusb_cdr_b c_ltr	Register control for CDR bc ltr
4:0	**cdr_bc_ltdo**	rg_ssusb_cdr_b c_ltdo	Register control for CDR bc ltd

1129095C PHYD_CDR1 SSUSB PHYD CDR Control 1 Register 020A0802

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				rg_s susb _cdr _bir _ltd 1								rg_ssusb_cdr_bir_ltr				
Type				RW								RW				
Reset				0	0	0	1	0				0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				rg_ssusb_cdr_bir_ltdo					rg_ssusb_ cdr_bw_se l				rg_ssusb_cdr_bic_ ltd1			
Type				RW					RW				RW			
Reset				0	1	0	0	0	0	0			0	0	1	0

Bit(s)	Mnemonic	Name	Description
28:24	**cdr_bir_ltd1**	rg_ssusb_cdr_b ir_ltd1	**Register control for CDR bir ltd**
20:16	**cdr_bir_ltr**	rg_ssusb_cdr_b ir_ltr	**Register control for CDR bir ltr**
12:8	**cdr_bir_ltdo**	rg_ssusb_cdr_b ir_ltdo	**Register control for CDR bir ltd**
7:6	**cdr_bwsel_dly**	rg_ssusb_cdr_b w_sel	**ssusb_cdr_bw_sel delay time control** 2'b00: 2us 2'b01: 4us 2'b10: 6us

Bit(s)	Mnemonic	Name	Description
			2'b11: 8us
3:0	**cdr_bic_ltd1**	rg_ssusb_cdr_bic_ltd1	**Register control for CDR bic ltd**

11290960 PHYD_PLL_0 SSUSB PHYD PLL Control 0 Register 00328040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				rg_ssusb_force_cdr_band_5g	rg_ssusb_force_cdr_band_2p5g	rg_ssusb_force_pll_band_5g	rg_ssusb_force_pll_band_2p5g	rg_ssusb_p_eq_t_sel								
Type				RW	RW	RW	RW	RW								
Reset				0	0	0	0	0	0	0	1	1	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_p_eq_t_sel	rg_ssusb_pll_iso_en_cyc										rg_ssusb_pllband_recal	rg_ssusb_pll_dds_iso_en	rg_ssusb_force_pll_dds_iso_en	rg_ssusb_pll_dds_pwr_on	rg_ssusb_force_pll_dds_pwr_on
Type	RW	RW										RW	RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28	**force_cdr_band_5g**	rg_ssusb_force_cdr_band_5g	**Forces 5G cdr band**
27	**force_cdr_band_2p5g**	rg_ssusb_force_cdr_band_2p5g	**Forces 2.5G cdr band**
26	**force_pll_band_5g**	rg_ssusb_force_pll_band_5g	**Forces 5G pll band**
25	**force_pll_band_2p5g**	rg_ssusb_force_pll_band_2p5g	**Forces 2.5G pll band**
24:15	**p_eq_t_sel**	rg_ssusb_p_eq_t_sel	**(PCIe mode only) Selects rxeq training time when rate operates at 5G** 1 represents 64 ref_ck cycles.
14:5	**pll_iso_en_cyc**	rg_ssusb_pll_iso_en_cyc	**da_ssusb_pll_iso_en stable cycle counts** After da_ssusb_pll_pwdb is asserted, count rg_ssusb_pll_iso_en_cyc, and da_ssusb_pll_iso_en will be asserted.
4	**pllband_recal**	rg_ssusb_pllband_recal	**Recalibrates txpll/cdrpll band after exiting ssusb_sleep**
3	**pll_dds_iso_en**	rg_ssusb_pll_dds_iso_en	**pll_dds_iso_en force mode register**
2	**force_pll_dds_iso_en**	rg_ssusb_force_pll_dds_iso_en	**Enables pll_dds_iso_en force mode**
1	**pll_dds_pwr_on**	rg_ssusb_pll_dds_pwr_on	**pll_dds_pwr_on force mode register**
0	**force_pll_dds_pwr_on**	rg_ssusb_force_pll_dds_pwr_on	**Enables pll_dds_pwr_on force mode**

11290964 PHYD_PLL_1 SSUSB PHYD PLL Control 1 00000000

Register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_cdr_band_5g								rg_ssusb_cdr_band_2p5g							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_pll_band_5g								rg_ssusb_pll_band_2p5g							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**cdr_band_5g**	rg_ssusb_cdr_band_5g	5G cdr band register
23:16	**cdr_band_2p5g**	rg_ssusb_cdr_band_2p5g	2.5G cdr band register
15:8	**pll_band_5g**	rg_ssusb_pll_band_5g	5G pll band register
7:0	**pll_band_2p5g**	rg_ssusb_pll_band_2p5g	2.5G pll band register

11290968 PHYD_BCN_DET_1 SSUSB PHYD BCN DET 1 Register 271003E8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_p_bcn_obs_prd															
Type	RW															
Reset	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_u_bcn_obs_prd															
Type	RW															
Reset	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	**p_bcn_obs_prd**	rg_ssusb_p_bcn_obs_prd	PCIe Host beacon detection observation period
15:0	**u_bcn_obs_prd**	rg_ssusb_u_bcn_obs_prd	USB3 noise observation period

1129096C PHYD_BCN_DET_2 SSUSB PHYD BCN DET 2 Register 0007112C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					rg_ssusb_p_bcn_obs_sel											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				rg_ssusb_bcn_det_dis	rg_ssusb_u_bcn_obs_sel											
Type				RW	RW											
Reset				1	0	0	0	1	0	0	1	0	1	1	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**p_bcn_obs_sel**	rg_ssusb_p_bcn_obs_sel	**PCIe host beacon det threshold** Beacon: Toggle > rg_ssusb_p_bcn_obs_sel Noise: Toggle < rg_ssusb_p_bcn_obs_sel
12	**bcn_det_dis**	rg_ssusb_bcn_det_dis	**Enables/Disables beacon detection (noise Filter)** For PCIe mode: 1'b0: Enable beacon detection 1'b1: Disable beacon detection For USB3 mode, when P3, selects wakeup condition: 1'b0: Enable noise Filter 1'b1: Disable noise Filter
11:0	**u_bcn_obs_sel**	rg_ssusb_u_bcn_obs_sel	**USB3 LFPS threshold** LFPS: Toggle > rg_ssusb_u_bcn_obs_sel Noise: Toggle < rg_ssusb_u_bcn_obs_sel

11290970 EQ0 SSUSB PHYA EQ 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_SSUSB_EQ_DLHL_ LFI								RG_SSUSB_EQ_DHHL_LFI						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_SSUSB_EQ_DDoHOS_LFI								RG_SSUSB_EQ_DDoLOS_LFI						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:24	**EQ_DLHL_LFI**	RG_SSUSB_EQ_DLHL_LFI	Filter count: DFE, LHL
22:16	**EQ_DHHL_LFI**	RG_SSUSB_EQ_DHHL_LFI	Filter count: DFE, HHL
14:8	**EQ_DDoHOS_LFI**	RG_SSUSB_EQ_DDoHOS_LFI	Filter count: CDR offset calibration for DoH latch
6:0	**EQ_DDoLOS_LFI**	RG_SSUSB_EQ_DDoLOS_LFI	Filter count: CDR offset calibration for DoL latch

11290974 EQ1 SSUSB PHYA EQ 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_SSUSB_EQ_DD1HO S_LFI								RG_SSUSB_EQ_DD1LOS_LFI						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_SSUSB_EQ_DEoOS_LFI								RG_SSUSB_EQ_DE1OS_LFI						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:24	**EQ_DD1HOS_LFI**	RG_SSUSB_EQ_DD1HOS_LFI	Filter count: CDR offset calibration for D1H latch
22:16	**EQ_DD1LOS_LFI**	RG_SSUSB_EQ_DD	Filter count: CDR offset calibration for D1L latch

Bit(s)	Mnemonic	Name	Description
14:8	**EQ_DE0OS_LFI**	1LOS_LFI RG_SSUSB_EQ_DE0OS_LFI	Filter count: CDR offset calibration for DE0 latch
6:0	**EQ_DE1OS_LFI**	RG_SSUSB_EQ_DE1OS_LFI	Filter count: CDR offset calibration for DE1 latch

11290978 EQ2 **SSUSB PHYA EQ 2 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_SSUSB_EQ_DLHLOS_LF I								RG_SSUSB_EQ_DHHLOS_LFI						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_SSUSB_EQ_STOPTIME	RG_SSUSB_EQ_DHHL_LF_SEL			RG_SSUSB_EQ_DSAOS_LF_SEL			RG_SSUSB_EQ_STARTTIME		RG_SSUSB_EQ_DLEQ_LF_SEL			RG_SSUSB_EQ_DLHL_LF_SEL		
Type		RW	RW			RW			RW		RW			RW		
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:24	**EQ_DLHLOS_LFI**	RG_SSUSB_EQ_DLHLOS_LFI	**Filter count: CDR offset calibration for DLHL latch**
22:16	**EQ_DHHLOS_LFI**	RG_SSUSB_EQ_DHHLOS_LFI	**Filter count: CDR offset calibration for DHHL latch**
14	**EQ_STOPTIME**	RG_SSUSB_EQ_STOPTIME	**EQ counter statistial polling stop time** 0: 16u 1: 32u
13:11	**EQ_DHHL_LF_SEL**	RG_SSUSB_EQ_DHHL_LF_SEL	**Selects DFE, HHL loop Filter**
10:8	**EQ_DSAOS_LF_SEL**	RG_SSUSB_EQ_DSAOS_LF_SEL	**Selects Sense-Amp. DFF offset loop Filter**
7:6	**EQ_STARTTIME**	RG_SSUSB_EQ_STARTTIME	**EQ counter statistic polling start time** 2'b00: 0.5u 2'b01: 1u 2'b10: 1.5u
5:3	**EQ_DLEQ_LF_SEL**	RG_SSUSB_EQ_DLEQ_LF_SEL	**Selects LEQ loop Filter**
2:0	**EQ_DLHL_LF_SEL**	RG_SSUSB_EQ_DLHL_LF_SEL	**Selects DFE, LHL loop Filter**

1129097C EQ3 **SSUSB PHYA EQ 3 Register** **83000098**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_SSUSB_EQ_DLEQ_LFI_GEN2				RG_SSUSB_EQ_DLEQ_LFI_GEN1					RG_SSUSB_EQ_DEYE0OS_LFI						
Type	RW				RW					RW						
Reset	1	0	0	0	0	0	1	1		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_SSUSB_EQ_DEYE1OS_LFI							RG_SSUSB_EQ_TRI_DET_EN	RG_SSUSB_EQ_TRI_DET_TH						

Type		RW							RW	RW						
Reset		0	0	0	0	0	0	0	1	0	0	1	1	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**EQ_DLEQ_LFI_GEN2**	RG_SSUSB_EQ_DLEQ_LFI_GEN2	gen2 Filter count: LEQ, peaking
27:24	**EQ_DLEQ_LFI_GEN1**	RG_SSUSB_EQ_DLEQ_LFI_GEN1	gen1 Filter count: LEQ, peaking
22:16	**EQ_DEYE0OS_LFI**	RG_SSUSB_EQ_DEYE0OS_LFI	Filter count: CDR offset calibration for EYE0 latch
14:8	**EQ_DEYE1OS_LFI**	RG_SSUSB_EQ_DEYE1OS_LFI	Filter count: CDR offset calibration for EYE1 latch
7	**EQ_TRI_DET_EN**	RG_SSUSB_EQ_TRI_DET_EN	Enables signal detection PI code wandering
6:0	**EQ_TRI_DET_TH**	RG_SSUSB_EQ_TRI_DET_TH	Signal detection PI code wandering range

11290980 EQ_EYE0 SSUSB PHYA EYE 0 Register 00000040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_SSUSB_ EQ_EYE_XO FFSET							RG_SSUSB_EQ_EYE_MON_EN		RG_SSUSB_EQ_EYE0_Y						
Type	RW							RW		RW						
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_SSUSB_EQ_EYE1_Y							RG_SSUSB_EQ_PILPO_ROUT	RG_SSUSB_EQ_PI_KPGAIN			RG_SSUSB_EQ_EYE_CNT_EN			
Type		RW							RW	RW			RW			
Reset		0	0	0	0	0	0	0	0	1	0	0	0			

Bit(s)	Mnemonic	Name	Description
31:25	**EQ_EYE_XOFFSET**	RG_SSUSB_EQ_EYE_XOFFSET	**PI code offset for eye monitor**
24	**EQ_EYE_MON_EN**	RG_SSUSB_EQ_EYE_MON_EN	**Enables eye monitor** 0: Disable 1: Enable
22:16	**EQ_EYE0_Y**	RG_SSUSB_EQ_EYE0_Y	**Horizontal PI code control for EYE0**
14:8	**EQ_EYE1_Y**	RG_SSUSB_EQ_EYE1_Y	**Horizontal PI code control for EYE0**
7	**EQ_PILPO_ROUT**	RG_SSUSB_EQ_PILPO_ROUT	**PI code mointor switch** 0: Real-time toggling 1: Snap shot
6:4	**EQ_PI_KPGAIN**	RG_SSUSB_EQ_PI_KPGAIN	**PI phase calibration loop control**
3	**EQ_EYE_CNT_EN**	RG_SSUSB_EQ_EYE_CNT_EN	**Eye monitor, error count recount**

11290984 EQ_EYE1 **SSUSB PHYA EYE 1 Register** **05000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_SSUSB_EQ_SIGDET														RG_SSUSB_EQ_EYE_MASK
Type		RW														RW
Reset		0	0	0	0	1	0	1								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SSUSB_EQ_EYE_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0							

Bit(s)	Mnemonic	Name	Description
30:24	**EQ_SIGDET**	RG_SSUSB_EQ_SIGDET	Voltage threshold voltage for signal detection
16:7	**EQ_EYE_MASK**	RG_SSUSB_EQ_EYE_MASK	Data Filter for eye monitor

11290988 EQ_EYE2 **SSUSB PHYA EYE 2 Register** **03030000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_SSUSB_EQ_RX500M_CK_SEL		RG_SSUSB_EQ_SD_CNT1						RG_SSUSB_EQ_ISIFLAG_SEL		RG_SSUSB_EQ_SD_CNT0					
Type	RW		RW						RW		RW					
Reset	0		0	0	0	0	1	1	0	0	0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
31	**RX500M_CK_SEL**	RG_SSUSB_EQ_RX500M_CK_SEL	Signal detection count value
29:24	**EQ_SD_CNT1**	RG_SSUSB_EQ_SD_CNT1	
23:22	**EQ_ISIFLAG_SEL**	RG_SSUSB_EQ_ISIFLAG_SEL	
21:16	**EQ_SD_CNT0**	RG_SSUSB_EQ_SD_CNT0	Signal detection count value

1129098C EQ_DFE0 **F0202000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_SSUSB_EQ_LEQMAX				RG_SSUSB_EQ_DFEX_EN	RG_SSUSB_EQ_DFEX_LF_SEL			RG_SSUSB_EQ_CHK_EYE_H	RG_SSUSB_EQ_PIEYE_INI						

Type	RW				RW	RW			RW	RW						
Reset	1	1	1	1	0	0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_SSUSB_EQ_PI90_INI								RG_SSUSB_EQ_PI0_INI						
Type		RW								RW						
Reset		0	1	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**EQ_LEQMAX**	RG_SSUSB_EQ_LEQMAX	**LEQ upper bound**
27	**EQ_DFEX_EN**	RG_SSUSB_EQ_DFEX_EN	**Forces DFEX enable** 0: HW control 1: Force DFEX enable
26:24	**EQ_DFEX_LF_SEL**	RG_SSUSB_EQ_DFEX_LF_SEL	**Selects DFEX loop Filter**
23	**EQ_CHK_EYE_H**	RG_SSUSB_EQ_CHK_EYE_H	**Forces DFEX check EYE_H**
22:16	**EQ_PIEYE_INI**	RG_SSUSB_EQ_PIEYE_INI	**EQ_PIEYE initial value**
14:8	**EQ_PI90_INI**	RG_SSUSB_EQ_PI90_INI	**EQ PI90 initial value**
6:0	**EQ_PI0_INI**	RG_SSUSB_EQ_PI0_INI	**EQ PI0 initial value**

11290990 EQ_DFE1 **78000044**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_SSUSB_EQ_REV															
Type	RW															
Reset	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_SSUSB_EQ_DFEYEN_DUR				RG_SSUSB_EQ_DFEXEN_DUR			RG_SSUSB_EQ_DFEX_RST	RG_SSUSB_EQ_GATED_RXD_B	RG_SSUSB_EQ_PI90CK_SEL			RG_SSUSB_EQ_DFEX_DIS	RG_SSUSB_EQ_DFEYEN_STOP_DIS	RG_SSUSB_EQ_DFEXEN_SEL
Type		RW				RW			RW	RW	RW			RW	RW	RW
Reset		0	0	0		0	0	0	0	1	0	0		1	0	0

Bit(s)	Mnemonic	Name	Description
31:16	**EQ_REV**	RG_SSUSB_EQ_REV	**EQ reserved register**
14:12	**EQ_DFEYEN_DUR**	RG_SSUSB_EQ_DFEYEN_DUR	**EQ DFEY_EN delay duration** 16/32/48/64/80/96/112/128 us
10:8	**EQ_DFEXEN_DUR**	RG_SSUSB_EQ_DFEXEN_DUR	**EQ DFEX_EN delay duration** 32/64/96/128/160/192/224/256 us
7	**EQ_DFEX_RST**	RG_SSUSB_EQ_DFEX_RST	**Forces EQ_DFEX reset**
6	**EQ_GATED_RXD_B**	RG_SSUSB_EQ_GATED_RXD_B	**Forces gated RX data**
5:4	**EQ_PI90CK_SEL**	RG_SSUSB_EQ_PI90CK_SEL	**Selects PI90 count-down clock**
2	**EQ_DFEX_DIS**	RG_SSUSB_EQ_DF	**Disables DFEX function**

Bit(s)	Mnemonic	Name	Description
		EX_DIS	
1	**EQ_DFEYEN_STOP_DIS**	RG_SSUSB_EQ_DFEYEN_STOP_DIS	**Disables DFEYEN deassertion**
0	**EQ_DFEXEN_SEL**	RG_SSUSB_EQ_DFEXEN_SEL	**Selects DFEX_EN** 0: Original DFEX_EN control 1: DFEY_EN

11290994 EQ_DFE2 **00020000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_SSUSB_EQ_MON_SEL										RG_SSUSB_EQ_LEQOSC_DLYCNT		
Type				RW										RW		
Reset				0	0	0	0	0						0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_SSUSB_EQ_DLEQOS_LFI										RG_SSUSB_EQ_DFE_TOG	RG_SSUSB_EQ_LEQ_STOP_TO	
Type				RW										RW	RW	
Reset				0	0	0	0	0						0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**EQ_MON_SEL**	RG_SSUSB_EQ_MON_SEL	**Selects monitor**
18:16	**LEQOSC_DLYCNT**	RG_SSUSB_EQ_LEQOSC_DLYCNT	**leq os calibration enable delay time (after saosc_en is enabled)** Confirm rg_ssusb_cdros_cnt setting. 4'h0: 1*8 us 4'h1: 2*8 us 4'hf: 16*8 us
12:8	**EQ_DELEQOS_LFI**	RG_SSUSB_EQ_DLEQOS_LFI	**Filter count: CDR offset calibration for DCLEQOS latch**
2		RG_SSUSB_EQ_DFE_TOG	**DFE toggle mode**
1:0	**EQ_LEQ_STOP_TO**	RG_SSUSB_EQ_LEQ_STOP_TO	**LEQ_STOP timeout time** 32/64/96/128/160/192/224/256 us

11290998 EQ_DFE3 **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_SSUSB_EQ_RESERVED															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SSUSB_EQ_RESERVED															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**EQ_RESERVED**	RG_SSUSB_EQ_RESERVED	[0]: RG_SSUSB_EQ_STOP_FLAG_BPS

Bit(s)	Mnemonic	Name	Description

112909A0 PHYD_MON0 SSUSB PHYD Monitor 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rgs_ssusb_bert_berc															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgs_ssusb_lfps					rgs_ssusb_traindec			rgs_ssusb_scp_pat							
Type	RO					RO			RO							
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	**rgs_bert_berc**	rgs_ssusb_bert _berc	Debug signals
15:12	**rgs_lfps**	rgs_ssusb_lfps	Debug signals for LFPS
10:8	**rgs_traindec**	rgs_ssusb_trai ndec	Debug signals
7:0	**rgs_scp_pat**	rgs_ssusb_scp_ pat	Debug signals

112909A4 PHYD_MON1 SSUSB PHYD Monitor 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgs_ssusb_rx_fl_out															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**rgs_rx_fl_out**	rgs_ssusb_rx_f l_out	Debug signals

112909A8 PHYD_MON2 SSUSB PHYD Monitor 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rgs_ssusb_t2rlb_errcnt															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgs_ssusb_retrack					rgs_ssusb_rx_pll_lock	rgs_ssusb_cdr_vcocal_cplt_d	rgs_ssusb_pll_vcocal_cplt_d	rgs_ssusb_pdnctl							
Type	RO					RO	RO	RO	RO							

Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	**rgs_t2rlb_errc nt**	rgs_ssusb_t2rl b_errcnt	Debug signals for T2RLB error count
15:12	**rgs_retrack**	rgs_ssusb_retr ack	Debug signals
10	**rgs_rxpll_lock**	rgs_ssusb_rxpl l_lock	rxpll_lock signal
9	**rgs_cdr_vcocal _cplt_d**	rgs_ssusb_cdr_ vcocal_cplt_d	ad_ssusb_cdr_vcocal_cplt signal
8	**rgs_pll_vcocal _cplt_d**	rgs_ssusb_pll_ vcocal_cplt_d	ad_ssusb_pll_vcocal_cplt signal
7:0	**rgs_pdnctl**	rgs_ssusb_pdnc tl	Debug signals for PDNCTL

112909AC PHYD_MON3 SSUSB PHYD Monitor 3 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rgs_ssusb_tseq_errcnt															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgs_ssusb_prbs_errcnt															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	**rgs_tseq_errcn t**	rgs_ssusb_tseq _errcnt	Debug signals
15:0	**rgs_prbs_errcn t**	rgs_ssusb_prbs _errcnt	Debug signals

112909B0 PHYD_MON4 SSUSB PHYD Monitor 4 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					rgs_ssusb_rx_lslock_cnt				rgs_ssusb_scp_detcnt							
Type					RO				RO							
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgs_ssusb_tseq_detcnt															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24	**rgs_rx_lslock_ cnt**	rgs_ssusb_rx_l slock_cnt	Debug signals
23:16	**rgs_scp_detcnt**	rgs_ssusb_scp_ detcnt	Debug signals
15:0	**rgs_tseq_detcn t**	rgs_ssusb_tseq _detcnt	Debug signals

112909B4 PHYD_MON5 SSUSB PHYD Monitor 5 00000000

Register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rgs_ssusb_ebufmsg															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgs_ssusb_bert_lock	rgs_ssusb_scp_det	rgs_ssusb_tseq_det	rgs_ssusb_ebuf_udf	rgs_ssusb_ebuf_ovf	rgs_ssusb_prbs_passth	rgs_ssusb_prbs_pass	rgs_ssusb_prbs_lock		rgs_ssusb_t2rlb_err	rgs_ssusb_t2rlb_passth	rgs_ssusb_t2rlb_pass	rgs_ssusb_t2rlb_lock	rgs_ssusb_rx_impcal_done	rgs_ssusb_tx_impcal_done	rgs_ssusb_rxdetected
Type	RO	RO	RO	RO	RO	RO	RO	RO		RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	**rgs_ebufmsg**	rgs_ssusb_ebuf msg	Debug signals
15	**rgs_bert_lock**	rgs_ssusb_bert _lock	Debug signals
14	**rgs_scp_det**	rgs_ssusb_scp_ det	Debug signals
13	**rgs_tseq_det**	rgs_ssusb_tseq _det	Debug signals
12	**rgs_ebuf_udf**	rgs_ssusb_ebuf _udf	Debug signals
11	**rgs_ebuf_ovf**	rgs_ssusb_ebuf _ovf	Debug signals
10	**rgs_prbs_passt h**	rgs_ssusb_prbs _passth	Debug signals
9	**rgs_prbs_pass**	rgs_ssusb_prbs _pass	Debug signals
8	**rgs_prbs_lock**	rgs_ssusb_prbs _lock	Debug signals
6	**rgs_t2rlb_err**	rgs_ssusb_t2rl b_err	Debug signals
5	**rgs_t2rlb_pass th**	rgs_ssusb_t2rl b_passth	Debug signals
4	**rgs_t2rlb_pass**	rgs_ssusb_t2rl b_pass	Debug signals
3	**rgs_t2rlb_lock**	rgs_ssusb_t2rl b_lock	Debug signals
2	**rgs_rx_impcal_ done**	rgs_ssusb_rx_i mpcal_done	Debug signals
1	**rgs_tx_impcal_ done**	rgs_ssusb_tx_i mpcal_done	Debug signals
0	**rgs_rxdetected**	rgs_ssusb_rxde tected	Debug signals

112909B8 PHYD_MON6 SSUSB PHYD Monitor 6 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		rgs_ssusb_sigcal_done	rgs_ssusb_sigcal_cal_out	rgs_ssusb_sigcal_offset								rgs_ssusb_rx_imp_sel				
Type		RO	RO	RO								RO				
Reset		0	0	0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				rgs_ssusb_tx_imp_sel					rgs_ssusb_tfifo_msg				rgs_ssusb_rfifo_msg			
Type				RO					RO				RO			
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30	**sigcal_done**	rgs_ssusb_sigc al_done	Debug signals

Bit(s)	Mnemonic	Name	Description
29	**sigcal_cal_out**	rgs_ssusb_sigcal_cal_out	Debug signals
28:24	**sigcal_offset**	rgs_ssusb_sigcal_offset	Debug signals
20:16	**rgs_rx_imp_sel**	rgs_ssusb_rx_imp_sel	Debug signals
12:8	**rgs_tx_imp_sel**	rgs_ssusb_tx_imp_sel	Debug signals
7:4	**rgs_tfifo_msg**	rgs_ssusb_tfifo_msg	Debug signals
3:0	**rgs_rfifo_msg**	rgs_ssusb_rfifo_msg	Debug signals

112909BC PHYD_MON7 SSUSB PHYD Monitor 7 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgs_ssusb_ft_out								rgs_ssusb_prb_out							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**rgs_t2rlb_lock**	rgs_ssusb_ft_out	Debug signals
7:0	**rgs_prb_out**	rgs_ssusb_prb_out	Debug signals

112909C0 PHYA_RX_MON0 SSUSB PHYA RX Monitor 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RGS_SSUSB_EQ_DCLEQ					RGS_SSUSB_EQ_DCD0H						
Type					RO					RO						
Reset					0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RGS_SSUSB_EQ_DCD0L								RGS_SSUSB_EQ_DCD1H						
Type		RO								RO						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24	**RGS_EQ_DCLEQ**	RGS_SSUSB_EQ_DCLEQ	Linear EQ control code
22:16	**RGS_EQ_DCD0H**	RGS_SSUSB_EQ_DCD0H	Data 0 H control code
14:8	**RGS_EQ_DCD0L**	RGS_SSUSB_EQ_DCD0L	Data 0 L control code
6:0	**RGS_EQ_DCD1H**	RGS_SSUSB_EQ_DCD1H	Data 1 H control code

112909C4 PHYA_RX_MON1 SSUSB PHYA RX Monitor 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RGS_SSUSB_EQ_DCD1 L								RGS_SSUSB_EQ_DCEo						
Type		RO								RO						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RGS_SSUSB_EQ_DCE1								RGS_SSUSB_EQ_DCHHL						
Type		RO								RO						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:24	**RGS_EQ_DCD1L**	RGS_SSUSB_EQ_DCD1L	Data 1 L control code
22:16	**RGS_EQ_DCEo**	RGS_SSUSB_EQ_DCEo	Edge o control code
14:8	**RGS_EQ_DCE1**	RGS_SSUSB_EQ_DCE1	Edge 1 control code
6:0	**RGS_EQ_DCHHL**	RGS_SSUSB_EQ_DCHHL	Data HHL control code

112909C8 PHYA_RX_MON2 SSUSB PHYA RX Monitor 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RGS_SSUSB_EQ_LEQ_STOP	RGS_SSUSB_EQ_DCLHL							RGS_SSUSB_EQ_STATUS							
Type	RO	RO							RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RGS_SSUSB_EQ_DCEYEo								RGS_SSUSB_EQ_DCEYE1						
Type		RO								RO						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**RGS_EQ_LEQ_STOP**	RGS_SSUSB_EQ_LEQ_STOP	Linear EQ stop flag
30:24	**RGS_EQ_DCLHL**	RGS_SSUSB_EQ_DCLHL	Data LHL control code
23:16	**RGS_EQ_STATUS**	RGS_SSUSB_EQ_STATUS	EQ status output
14:8	**RGS_RX_DCEYEo**	RGS_SSUSB_EQ_DCEYEo	EYEo control code
6:0	**RGS_RX_DCEYE1**	RGS_SSUSB_EQ_DCEYE1	EYE1 control code

112909CC PHYA_RX_MON3 SSUSB PHYA RX Monitor 3 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													RGS_SSUSB_EQ_EYE_MONITOR_ERRCNT_o			

Type													RO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RGS_SSUSB_EQ_EYE_MONITOR_ERRCNT_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:0	**RGS_RX_EYE_MONITOR_ERRCNT_0**	RGS_SSUSB_EQ_EYE_MONITOR_ERRCNT_0	PI code minitor

112909D0 PHYA_RX_MON4 **SSUSB PHYA RX Monitor 4 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													RGS_SSUSB_EQ_EYE_MONITOR_ERRCNT_1			
Type													RO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RGS_SSUSB_EQ_EYE_MONITOR_ERRCNT_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:0	**RGS_RX_EYE_MONITOR_ERRCNT_1**	RGS_SSUSB_EQ_EYE_MONITOR_ERRCNT_1	Error count for EYE0

112909D4 PHYA_RX_MON5 **SSUSB PHYA RX Monitor 5 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RGS_SSUSB_EQ_DCLEQOS					RGS_SSUSB_EQ_EYE_CNT_RDY	RGS_SSUSB_EQ_PILPO						
Type				RO					RO	RO						
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:8	**RGS_EQ_DCLEQOS**	RGS_SSUSB_EQ_DCLEQOS	LEQ offset control code
7	**RGS_RX_EYE_CNT_RDY**	RGS_SSUSB_EQ_EYE_CNT_RDY	Error count for EYE1
6:0	**RGS_RX_PILPO**	RGS_SSUSB_EQ_P	Error count ready flag

Bit(s)	Mnemonic	Name	Description
		ILPO	

112909D8 PHYD_CPPAT2 SSUSB PHYD CP Pattern Gen Register2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													rg_ssusb_cppat_out_h_tmp2			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_cppat_out_h_tmp1								rg_ssusb_cppat_out_h_tmpo							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:16	cppat_out_h_tm p2	rg_ssusb_cppat _out_h_tmp2	Programmable pattern (tx_40b_cppat_program[19:16]) for compliance debugging, bit 39~20
15:8	cppat_out_h_tm p1	rg_ssusb_cppat _out_h_tmp1	Programmable pattern (tx_40b_cppat_program[15:8]) for compliance debugging, bit 39~20
7:0	cppat_out_h_tm po	rg_ssusb_cppat _out_h_tmp0	Programmable pattern (tx_40b_cppat_program[7:0]) for compliance debugging, bit 39~20

112909DC EQ_EYE3 SSUSB PHYA EYE 3 Register 00000080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						RG_S SUSB _EQ_ LEQ_ SHIF T							RG_SSUSB_EQ_EYE_C NT			
Type						RW							RW			
Reset						0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SSUSB_EQ_EYE_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26:24	LEQ_SHIFT	RG_SSUSB_EQ_LE Q_SHIFT	leq shift
19:0	EQ_EYE_CNT	RG_SSUSB_EQ_EY E_CNT	Eye minitor error count value

112909E0 KBAND_OUT KBAND_OUT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rgs_ssusb_cdr_band_5g								rgs_ssusb_cdr_band_2p5g							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgs_ssusb_pll_band_5g								rgs_ssusb_pll_band_2p5g							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**cdr_band_5g**	rgs_ssusb_cdr_band_5g	rgs_ssusb_cdr_band_5g
23:16	**cdr_band_2p5g**	rgs_ssusb_cdr_band_2p5g	rgs_ssusb_cdr_band_2p5g
15:8	**pll_band_5g**	rgs_ssusb_pll_band_5g	rgs_ssusb_pll_band_5g
7:0	**pll_band_2p5g**	rgs_ssusb_pll_band_2p5g	rgs_ssusb_pll_band_2p5g

112909E4 KBAND_OUT1 KBAND_OUT1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								rgs_ssusb_cdr_vcocal_fail	rgs_ssusb_cdr_vcocal_state							
Type								RO	RO							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								rgs_ssusb_pll_vcocal_fail	rgs_ssusb_pll_vcocal_state							
Type								RO	RO							
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24	**rgs_cdr_vcocal_fail**	rgs_ssusb_cdr_vcocal_fail	Debug signals
23:16	**rgs_cdr_vcocal_state**	rgs_ssusb_cdr_vcocal_state	Debug signals
8	**rgs_pll_vcocal_fail**	rgs_ssusb_pll_vcocal_fail	Debug signals
7:0	**rgs_pll_vcocal_state**	rgs_ssusb_pll_vcocal_state	Debug signals

Module name: ssusb_sifslv_u3phya_da_t20soc_tphy Base address: (+11290c00h)

Address	Name	Width	Register Function
11290C00	**ssusb_usb30_phya_da_reg0**	32	DA_SSUSB_CDR_REFCK_SEL
11290C04	**ssusb_usb30_phya_da_reg1**	32	DA_PCIE_MODE
11290C08	**ssusb_usb30_phya_da_reg4**	32	DA_SSUSB_PLL_BC
11290C0C	**ssusb_usb30_phya_da_reg5**	32	DA_SSUSB_PLL_IC
11290C10	**ssusb_usb30_phya_da_reg6**	32	DA_SSUSB_PLL_IR
11290C14	**ssusb_usb30_ph**	32	DA_SSUSB_PLL_BP

Address	Name	Width	Register Function
	ya_da_reg7		
11290C18	ssusb_usb30_phya_da_reg8	32	DA_SSUSB_PLL_FBKSEL
11290C1C	ssusb_usb30_phya_da_reg9	32	DA_SSUSB_PLL_FBKDIV
11290C20	ssusb_usb30_phya_da_reg10	32	
11290C38	ssusb_usb30_phya_da_reg19	32	DA_SSUSB_PLL_SSC_DELTA1
11290C3C	ssusb_usb30_phya_da_reg20	32	
11290C40	ssusb_usb30_phya_da_reg21	32	
11290C44	ssusb_usb30_phya_da_reg23	32	
11290C48	ssusb_usb30_phya_da_reg25	32	
11290C4C	ssusb_usb30_phya_da_reg26	32	DA_SSUSB_PLL_REFCKDIV
11290C50	ssusb_usb30_phya_da_reg28	32	DA_SSUSB_CDR_BPA
11290C54	ssusb_usb30_phya_da_reg29	32	DA_SSUSB_CDR_BPB
11290C58	ssusb_usb30_phya_da_reg30	32	DA_SSUSB_CDR_BR
11290C5C	ssusb_usb30_phya_da_reg31	32	DA_SSUSB_CDR_FBDIV
11290C60	ssusb_usb30_phya_da_reg32	32	
11290C64	ssusb_usb30_phya_da_reg33	32	DA_SSUSB_EQ_RSTEP2

11290C00 ssusb_usb30_phya_da_rego DA_SSUSB_CDR_REFCK_SEL 01844845

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								RG_PCIE_SPEED_PE2D	RG_PCIE_SPEED_PE2H	RG_PCIE_SPEED_PE1D	RG_PCIE_SPEED_PE1H	RG_PCIE_SPEED_U3	RG_SSUSB_XTAL_EXT_EN_PE2D		RG_SSUSB_XTAL_EXT_EN_PE2H	
Type								RW	RW	RW	RW	RW	RW		RW	
Reset								1	1	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SSUSB_XTAL_EXT_EN_PE1D		RG_SSUSB_XTAL_EXT_EN_PE1H		RG_SSUSB_XTAL_EXT_EN_U3		RG_SSUSB_CDR_REFCK_SEL_PE2D		RG_SSUSB_CDR_REFCK_SEL_PE2H		RG_SSUSB_CDR_REFCK_SEL_PE1D		RG_SSUSB_CDR_REFCK_SEL_PE1H		RG_SSUSB_CDR_REFCK_SEL_U3	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	1	0	0	1	0	0	0	0	1	0	0	0	1	0	1

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
24		RG_PCIE_SPEED_PE2D	
23		RG_PCIE_SPEED_PE2H	
22		RG_PCIE_SPEED_PE1D	
21		RG_PCIE_SPEED_PE1H	
20		RG_PCIE_SPEED_U3	BG
19:18		RG_SSUSB_XTAL_EXT_EN_PE2D	
17:16		RG_SSUSB_XTAL_EXT_EN_PE2H	
15:14		RG_SSUSB_XTAL_EXT_EN_PE1D	
13:12		RG_SSUSB_XTAL_EXT_EN_PE1H	
11:10		RG_SSUSB_XTAL_EXT_EN_U3	BG
9:8		RG_SSUSB_CDR_REFCK_SEL_PE2D	
7:6		RG_SSUSB_CDR_REFCK_SEL_PE2H	
5:4		RG_SSUSB_CDR_REFCK_SEL_PE1D	
3:2		RG_SSUSB_CDR_REFCK_SEL_PE1H	
1:0		RG_SSUSB_CDR_REFCK_SEL_U3	BG

11290C04 ssusb_usb30_phya_da_reg1 DA_PCIE_MODE 0103010E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							RG_PCIE_REFCK_DIV4_PE2D	RG_PCIE_REFCK_DIV4_PE2H						RG_PCIE_REFCK_DIV4_PE1D	RG_PCIE_REFCK_DIV4_PE1H	RG_PCIE_REFCK_DIV4_U3
Type							RW	RW						RW	RW	RW
Reset							0	1						0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_PCIE_MODE_PE2D					RG_PCIE_MODE_PE2H	RG_PCIE_MODE_PE1D	RG_PCIE_MODE_PE1H	RG_PCIE_MODE_U3
Type								RW					RW	RW	RW	RW
Reset								1					1	1	1	0

Bit(s)	Mnemonic	Name	Description
25		RG_PCIE_REFCK_DIV4_PE2D	
24		RG_PCIE_REFCK_DIV4_PE2H	
18		RG_PCIE_REFCK_	

Bit(s)	Mnemonic	Name	Description
		DIV4_PE1D	
17		RG_PCIE_REFCK_DIV4_PE1H	
16		RG_PCIE_REFCK_DIV4_U3	BG
8		RG_PCIE_MODE_PE2D	
3		RG_PCIE_MODE_PE2H	
2		RG_PCIE_MODE_PE1D	
1		RG_PCIE_MODE_PE1H	
0		RG_PCIE_MODE_U3	BG

11290C08 ssusb_usb30_phya_dareg4 DA_SSUSB_PLL_BC 00000047

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								RG_SSUSB_PLL_DIVEN_PE2D			RG_SSUSB_PLL_DIVEN_PE2H			RG_SSUSB_PLL_DIVEN_PE1D		
Type								RW			RW			RW		
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SSUSB_PLL_DIVEN_PE1H			RG_SSUSB_PLL_DIVEN_U3			RG_SSUSB_PLL_BC_PE2D		RG_SSUSB_PLL_BC_PE2H		RG_SSUSB_PLL_BC_PE1D			RG_SSUSB_PLL_BC_PE1H		RG_SSUSB_PLL_BC_U3
Type	RW			RW			RW		RW		RW			RW		
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
24:22		RG_SSUSB_PLL_DIVEN_PE2D	
21:19		RG_SSUSB_PLL_DIVEN_PE2H	
18:16		RG_SSUSB_PLL_DIVEN_PE1D	
15:13		RG_SSUSB_PLL_DIVEN_PE1H	
12:10		RG_SSUSB_PLL_DIVEN_U3	TX
9:8		RG_SSUSB_PLL_BC_PE2D	
7:6		RG_SSUSB_PLL_BC_PE2H	
5:4		RG_SSUSB_PLL_BC_PE1D	
3:2		RG_SSUSB_PLL_BC_PE1H	
1:0		RG_SSUSB_PLL_BC_U3	TX

11290C0C ssusb_usb30_phya_da DA_SSUSB_PLL_IC 004CDCD1

reg5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_SSUSB_PLL_BR_PE2D		RG_SSUSB_PLL_BR_PE2H		RG_SSUSB_PLL_BR_PE1D		RG_SSUSB_PLL_BR_PE1H		RG_SSUSB_PLL_BR_U3				RG_SSUSB_PLL_IC_PE2D			
Type	RW		RW		RW		RW		RW				RW			
Reset	0	0	0	0	0	0	0	0	0	1			1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SSUSB_PLL_IC_PE2H				RG_SSUSB_PLL_IC_PE1D				RG_SSUSB_PLL_IC_PE1H				RG_SSUSB_PLL_IC_U3			
Type	RW				RW				RW				RW			
Reset	1	1	0	1	1	1	0	0	1	1	0	1	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:30		RG_SSUSB_PLL_BR_PE2D	
29:28		RG_SSUSB_PLL_BR_PE2H	
27:26		RG_SSUSB_PLL_BR_PE1D	
25:24		RG_SSUSB_PLL_BR_PE1H	
23:22		RG_SSUSB_PLL_BR_U3	TX
19:16		RG_SSUSB_PLL_IC_PE2D	
15:12		RG_SSUSB_PLL_IC_PE2H	
11:8		RG_SSUSB_PLL_IC_PE1D	
7:4		RG_SSUSB_PLL_IC_PE1H	
3:0		RG_SSUSB_PLL_IC_U3	TX

11290C10 ssusb_usb30_phya_da_reg6 DA_SSUSB_PLL_IR 0C0C0CC2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RG_SSUSB_PLL_IR_PE2D								RG_SSUSB_PLL_IR_PE2H			
Type					RW								RW			
Reset					1	1	0	0					1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_SSUSB_PLL_IR_PE1D				RG_SSUSB_PLL_IR_PE1H				RG_SSUSB_PLL_IR_U3			
Type					RW				RW				RW			
Reset					1	1	0	0	1	1	0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
27:24		RG_SSUSB_PLL_IR_PE2D	
19:16		RG_SSUSB_PLL_IR_PE2H	
11:8		RG_SSUSB_PLL_I	

Bit(s)	Mnemonic	Name	Description
		R_PE1D	
7:4		RG_SSUSB_PLL_IR_PE1H	
3:0		RG_SSUSB_PLL_IR_U3	

11290C14 **ssusb_usb30_phya_dareg7** **DA_SSUSB_PLL_BP** **0002002E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RG_SSUSB_PLL_BP_PE2D								RG_SSUSB_PLL_BP_PE2H			
Type					RW								RW			
Reset					0	0	0	0					0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_SSUSB_PLL_BP_PE1D				RG_SSUSB_PLL_BP_PE1H				RG_SSUSB_PLL_BP_U3			
Type					RW				RW				RW			
Reset					0	0	0	0	0	0	1	0	1	1	1	0

Bit(s)	Mnemonic	Name	Description
27:24		RG_SSUSB_PLL_BP_PE2D	
19:16		RG_SSUSB_PLL_BP_PE2H	
11:8		RG_SSUSB_PLL_BP_PE1D	
7:4		RG_SSUSB_PLL_BP_PE1H	
3:0		RG_SSUSB_PLL_BP_U3	

11290C18 **ssusb_usb30_phya_dareg8** **DA_SSUSB_PLL_FBKSEL** **0202020A**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							RG_SSUSB_PLL_FBKSEL_PE2D								RG_SSUSB_PLL_FBKSEL_PE2H	
Type							RW								RW	
Reset							1	0							1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_SSUSB_PLL_FBKSEL_PE1D						RG_SSUSB_PLL_FBKSEL_PE1H		RG_SSUSB_PLL_FBKSEL_U3	
Type							RW						RW		RW	
Reset							1	0					1	0	1	0

Bit(s)	Mnemonic	Name	Description
25:24		RG_SSUSB_PLL_FBKSEL_PE2D	

Bit(s)	Mnemonic	Name	Description
17:16		RG_SSUSB_PLL_FBKSEL_PE2H	
9:8		RG_SSUSB_PLL_FBKSEL_PE1D	
3:2		RG_SSUSB_PLL_FBKSEL_PE1H	
1:0		RG_SSUSB_PLL_FBKSEL_U3	

11290C1C **ssusb_usb30_phya_dareg9** **DA_SSUSB_PLL_FBKDIV** **18181818**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_SSUSB_PLL_FBKDIV_PE2H								RG_SSUSB_PLL_FBKDIV_PE1D						
Type		RW								RW						
Reset		0	0	1	1	0	0	0		0	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_SSUSB_PLL_FBKDIV_PE1H								RG_SSUSB_PLL_FBKDIV_U3						
Type		RW								RW						
Reset		0	0	1	1	0	0	0		0	0	1	1	0	0	0

Bit(s)	Mnemonic	Name	Description
30:24		RG_SSUSB_PLL_FBKDIV_PE2H	
22:16		RG_SSUSB_PLL_FBKDIV_PE1D	
14:8		RG_SSUSB_PLL_FBKDIV_PE1H	
6:0		RG_SSUSB_PLL_FBKDIV_U3	

11290C20 **ssusb_usb30_phya_dareg10** **00000018**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RG_SSUSB_PLL_PREDIV_PE2D		RG_SSUSB_PLL_PREDIV_PE2H						RG_SSUSB_PLL_PREDIV_PE1D		RG_SSUSB_PLL_PREDIV_PE1H	
Type					RW		RW						RW		RW	
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_SSUSB_PLL_PREDIV_U3			RG_SSUSB_PLL_FBKDIV_PE2D						
Type							RW			RW						
Reset							0	0		0	0	1	1	0	0	0

Bit(s)	Mnemonic	Name	Description
27:26		RG_SSUSB_PLL_PREDIV_PE2D	
25:24		RG_SSUSB_PLL_P	

Bit(s)	Mnemonic	Name	Description
		REDIV_PE2H	
19:18		RG_SSUSB_PLL_P	
		REDIV_PE1D	
17:16		RG_SSUSB_PLL_P	
		REDIV_PE1H	
9:8		RG_SSUSB_PLL_P	
		REDIV_U3	
6:0		RG_SSUSB_PLL_F	
		BKDIV_PE2D	

11290C38 **ssusb_usb30_phya_dareg19** **DA_SSUSB_PLL_SSC_DELTA1** **00470042**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_SSUSB_PLL_SSC_DELTA1_PE1H															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SSUSB_PLL_SSC_DELTA1_U3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
31:16		RG_SSUSB_PLL_S	
		SC_DELTA1_PE1H	
15:0		RG_SSUSB_PLL_S	
		SC_DELTA1_U3	

11290C3C **ssusb_usb30_phya_dareg20** **00470047**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_SSUSB_PLL_SSC_DELTA1_PE2H															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SSUSB_PLL_SSC_DELTA1_PE1D															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:16		RG_SSUSB_PLL_S	
		SC_DELTA1_PE2H	
15:0		RG_SSUSB_PLL_S	
		SC_DELTA1_PE1D	

11290C40 **ssusb_usb30_phya_dareg21** **003E0047**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_SSUSB_PLL_SSC_DELTA_U3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SSUSB_PLL_SSC_DELTA1_PE2D															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:16		RG_SSUSB_PLL_SSC_DELTA_U3	
15:0		RG_SSUSB_PLL_SSC_DELTA1_PE2D	

11290C44 ssusb_usb30_phya_da_reg23 **00430043**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_SSUSB_PLL_SSC_DELTA_PE1D															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SSUSB_PLL_SSC_DELTA_PE1H															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:16		RG_SSUSB_PLL_SSC_DELTA_PE1D	
15:0		RG_SSUSB_PLL_SSC_DELTA_PE1H	

11290C48 ssusb_usb30_phya_da_reg25 **00430043**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_SSUSB_PLL_SSC_DELTA_PE2D															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SSUSB_PLL_SSC_DELTA_PE2H															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:16		RG_SSUSB_PLL_SSC_DELTA_PE2D	
15:0		RG_SSUSB_PLL_SSC_DELTA_PE2H	

11290C4C **ssusb_usb30_phya_da_reg26** **DA_SSUSB_PLL_REFCKDIV** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							RG_SSUSB_PLL_REFCKDIV_PE2D	RG_SSUSB_PLL_REFCKDIV_PE2H								RG_SSUSB_PLL_REFCKDIV_PE1D
Type							RW	RW								RW
Reset							0	0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_SSUSB_PLL_REFCKDIV_PE1H								RG_SSUSB_PLL_REFCKDIV_U3
Type								RW								RW
Reset								0								0

Bit(s)	Mnemonic	Name	Description
25		RG_SSUSB_PLL_REFCKDIV_PE2D	
24		RG_SSUSB_PLL_REFCKDIV_PE2H	
16		RG_SSUSB_PLL_REFCKDIV_PE1D	
8		RG_SSUSB_PLL_REFCKDIV_PE1H	
0		RG_SSUSB_PLL_REFCKDIV_U3	

11290C50 **ssusb_usb30_phya_da_reg28** **DA_SSUSB_CDR_BPA** **03030F01**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							RG_SSUSB_CDR_BPA_PE2D								RG_SSUSB_CDR_BPA_PE2H	
Type							RW								RW	
Reset							1	1							1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_SSUSB_CDR_BPA_PE1D		RG_SSUSB_CDR_BPA_PE1H								RG_SSUSB_CDR_BPA_U3	
Type					RW		RW								RW	
Reset					1	1	1	1							0	1

Bit(s)	Mnemonic	Name	Description
25:24		RG_SSUSB_CDR_BPA_PE2D	

Bit(s)	Mnemonic	Name	Description
17:16		RG_SSUSB_CDR_BPA_PE2H	
11:10		RG_SSUSB_CDR_BPA_PE1D	
9:8		RG_SSUSB_CDR_BPA_PE1H	
1:0		RG_SSUSB_CDR_BPA_U3	

11290C54 **ssusb_usb30_phya_da_reg29** **DA_SSUSB_CDR_BPB** **030300DB**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						RG_SSUSB_CDR_BPB_PE2D								RG_SSUSB_CDR_BPB_PE2H		
Type						RW								RW		
Reset						0	1	1						0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_SSUSB_CDR_BPB_PE1D			RG_SSUSB_CDR_BPB_PE1H			RG_SSUSB_CDR_BPB_U3		
Type								RW			RW			RW		
Reset								0	1	1	0	1	1	0	1	1

Bit(s)	Mnemonic	Name	Description
26:24		RG_SSUSB_CDR_BPB_PE2D	
18:16		RG_SSUSB_CDR_BPB_PE2H	
8:6		RG_SSUSB_CDR_BPB_PE1D	
5:3		RG_SSUSB_CDR_BPB_PE1H	
2:0		RG_SSUSB_CDR_BPB_U3	

11290C58 **ssusb_usb30_phya_da_reg30** **DA_SSUSB_CDR_BR** **070701FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						RG_SSUSB_CDR_BR_PE2D								RG_SSUSB_CDR_BR_PE2H		
Type						RW								RW		
Reset						1	1	1						1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_SSUSB_CDR_BR_PE1D			RG_SSUSB_CDR_BR_PE1H			RG_SSUSB_CDR_BR_U3		
Type								RW			RW			RW		
Reset								1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
26:24		RG_SSUSB_CDR_BR_PE2D	

Bit(s)	Mnemonic	Name	Description
18:16		RG_SSUSB_CDR_BR_PE2H	
8:6		RG_SSUSB_CDR_BR_PE1D	
5:3		RG_SSUSB_CDR_BR_PE1H	
2:0		RG_SSUSB_CDR_BR_U3	

11290C5C **ssusb_usb30_phya_da_reg31** **DA_SSUSB_CDR_FBDIV** **18181818**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_SSUSB_CDR_FBDIV_PE2H								RG_SSUSB_CDR_FBDIV_PE1D						
Type		RW								RW						
Reset		0	0	1	1	0	0	0		0	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_SSUSB_CDR_FBDIV_PE1H								RG_SSUSB_CDR_FBDIV_U3						
Type		RW								RW						
Reset		0	0	1	1	0	0	0		0	0	1	1	0	0	0

Bit(s)	Mnemonic	Name	Description
30:24		RG_SSUSB_CDR_FBDIV_PE2H	
22:16		RG_SSUSB_CDR_FBDIV_PE1D	
14:8		RG_SSUSB_CDR_FBDIV_PE1H	
6:0		RG_SSUSB_CDR_FBDIV_U3	

11290C60 **ssusb_usb30_phya_da_reg32** **AA802018**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_SSUSB_EQ_RSTEP1_PE2D		RG_SSUSB_EQ_RSTEP1_PE2H		RG_SSUSB_EQ_RSTEP1_PE1D		RG_SSUSB_EQ_RSTEP1_PE1H		RG_SSUSB_EQ_RSTEP1_U3		RG_SSUSB_LFPS_DEGLITCH_PE2D		RG_SSUSB_LFPS_DEGLITCH_PE2H		RG_SSUSB_LFPS_DEGLITCH_PE1D	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SSUSB_LFPS_DEGLITCH_PE1H		RG_SSUSB_LFPS_DEGLITCH_U3		RG_SSUSB_CDR_KVSEL_PE2D	RG_SSUSB_CDR_KVSEL_PE2H	RG_SSUSB_CDR_KVSEL_PE1D	RG_SSUSB_CDR_KVSEL_PE1H	RG_SSUSB_CDR_KVSEL_U3	RG_SSUSB_CDR_FBDIV_PE2D						
Type	RW		RW		RW	RW	RW	RW	RW	RW						
Reset	0	0	1	0	0	0	0	0	0	0	0	1	1	0	0	0

Bit(s)	Mnemonic	Name	Description
31:30		RG_SSUSB_EQ_RS	

Bit(s)	Mnemonic	Name	Description
		TEP1_PE2D	
29:28		RG_SSUSB_EQ_RS	
		TEP1_PE2H	
27:26		RG_SSUSB_EQ_RS	
		TEP1_PE1D	
25:24		RG_SSUSB_EQ_RS	
		TEP1_PE1H	
23:22		RG_SSUSB_EQ_RS	
		TEP1_U3	
21:20		RG_SSUSB_LFPS_	
		DEGLITCH_PE2D	
19:18		RG_SSUSB_LFPS_	
		DEGLITCH_PE2H	
17:16		RG_SSUSB_LFPS_	
		DEGLITCH_PE1D	
15:14		RG_SSUSB_LFPS_	
		DEGLITCH_PE1H	
13:12		RG_SSUSB_LFPS_	
		DEGLITCH_U3	
11		RG_SSUSB_CDR_K	
		VSEL_PE2D	
10		RG_SSUSB_CDR_K	
		VSEL_PE2H	
9		RG_SSUSB_CDR_K	
		VSEL_PE1D	
8		RG_SSUSB_CDR_K	
		VSEL_PE1H	
7		RG_SSUSB_CDR_K	
		VSEL_U3	
6:0		RG_SSUSB_CDR_F	
		BDIV_PE2D	

11290C64 ssusb_usb30_phya_da_reg33 DA_SSUSB_EQ_RSTEP2 00000155

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						RG_SSUSB_RX_CMPWD_PE2D	RG_SSUSB_RX_CMPWD_PE2H	RG_SSUSB_RX_CMPWD_PE1D	RG_SSUSB_RX_CMPWD_PE1H							RG_SSUSB_RX_CMPWD_U3
Type						RW	RW	RW	RW							RW
Reset						0	0	0	0							0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_SSUSB_EQ_RSTEP2_PE2D		RG_SSUSB_EQ_RSTEP2_PE2H		RG_SSUSB_EQ_RSTEP2_PE1D		RG_SSUSB_EQ_RSTEP2_PE1H		RG_SSUSB_EQ_RSTEP2_U3	
Type							RW		RW		RW		RW		RW	
Reset							0	1	0	1	0	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
26		RG_SSUSB_RX_CM	
		PWD_PE2D	
25		RG_SSUSB_RX_CM	
		PWD_PE2H	

Bit(s)	Mnemonic	Name	Description
24		RG_SSUSB_RX_CMPWD_PE1D	
23		RG_SSUSB_RX_CMPWD_PE1H	
16		RG_SSUSB_RX_CMPWD_U3	
9:8		RG_SSUSB_EQ_RSTEP2_PE2D	
7:6		RG_SSUSB_EQ_RSTEP2_PE2H	
5:4		RG_SSUSB_EQ_RSTEP2_PE1D	
3:2		RG_SSUSB_EQ_RSTEP2_PE1H	
1:0		RG_SSUSB_EQ_RSTEP2_U3	

Module name: ssusb_sifslv_u3phyd_bank2_t20soc_tphy Base address: (+11290a00h)

Address	Name	Width	Register Function
11290A00	**B2_PHYD_TOP1**	32	Bank 2 SSUSB PHYD TOP1
11290A04	**B2_PHYD_TOP2**	32	Bank 2 SSUSB PHYD TOP2
11290A08	**B2_PHYD_TOP3**	32	Bank 2 SSUSB PHYD TOP3
11290A0C	**B2_PHYD_TOP4**	32	Bank 2 SSUSB PHYD TOP4
11290A10	**B2_PHYD_TOP5**	32	Bank 2 SSUSB PHYD TOP5
11290A14	**B2_PHYD_TOP6**	32	Bank 2 SSUSB PHYD TOP6
11290A18	**B2_PHYD_TOP7**	32	Bank 2 SSUSB PHYD TOP7
11290A1C	**B2_PHYD_P_SIGDET1**	32	Bank 2 SSUSB PHYD_P_SIGDET1
11290A20	**B2_PHYD_P_SIGDET2**	32	Bank 2 SSUSB PHYD_P_SIGDET2
11290A24	**B2_PHYD_P_SIGDET_CAL1**	32	Bank 2 SSUSB PHYD_P_SIGDET_CAL1
11290A28	**B2_PHYD_RXDET1**	32	Bank 2 SSUSB PHYD_RXDET1
11290A2C	**B2_PHYD_RXDET2**	32	Bank 2 SSUSB PHYD_RXDET2
11290A30	**B2_PHYD_MISC0**	32	B2_PHYD_MISC0
11290A34	**B2_PHYD_MISC2**	32	B2_PHYD_MISC2
11290A38	**B2_PHYD_MISC3**	32	B2_PHYD_MISC3
11290A3C	**B2_PHYD_L1SS**	32	B2_PHYD_L1SS
11290A40	**B2_ROSC_0**	32	B2_ROSC_0
11290A44	**B2_ROSC_1**	32	B2_ROSC_1
11290A48	**B2_ROSC_2**	32	B2_ROSC_2
11290A4C	**B2_ROSC_3**	32	B2_ROSC_3
11290A50	**B2_ROSC_4**	32	B2_ROSC_4
11290A54	**B2_ROSC_5**	32	B2_ROSC_5
11290A58	**B2_ROSC_6**	32	B2_ROSC_6
11290A5C	**B2_ROSC_7**	32	B2_ROSC_7
11290A60	**B2_ROSC_8**	32	B2_ROSC_8
11290A64	**B2_ROSC_9**	32	B2_ROSC_9
11290A68	**B2_ROSC_A**	32	B2_ROSC_A
11290A70	**B2_2step_sigdet**	32	B2_2step_sigdet

Address	Name	Width	Register Function
11290A74	**B2_2step_sigdet_1**	32	B2_2step_sigdet_1
11290AE0	**PHYD_VERSION**	32	PHYD_VERSION
11290AE4	**PHYD_MODEL**	32	PHYD_MODEL

11290A00 B2_PHYD_TOP1 **Bank 2 SSUSB PHYD TOP1** **4B000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_pcie2_k_emp				rg_ssusb_pcie2_k_ful										rg_ssusb_tx_eidle_lp_en	rg_ssusb_force_tx_eidle_lp_en
Type	RW				RW										RW	RW
Reset	0	1	0	0	1	0	1	1							0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_sigdet_en	rg_ssusb_force_sigdet_en	rg_ssusb_clkrx_en	rg_ssusb_force_clkrx_en	rg_ssusb_clktx_en	rg_ssusb_force_clktx_en	rg_ssusb_clk_req_n_i	rg_ssusb_force_clk_req_n_i		rg_ssusb_rate	rg_ssusb_force_rate	rg_ssusb_pcie_mode_sel	rg_ssusb_force_pcie_mode_sel	rg_ssusb_phy_mode		rg_ssusb_force_phy_mode
Type	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW		RW
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		rg_ssusb_pcie2_k_emp	Parameter for determining half-empty level in read domain
27:24		rg_ssusb_pcie2_k_ful	Parameter for determining half-full level in write domain
17		rg_ssusb_tx_eidle_lp_en	da_ssusb_tx_eidle_lp_en force mode register
16		rg_ssusb_force_tx_eidle_lp_en	Enables da_ssusb_tx_eidle_lp_en force mode
15		rg_ssusb_sigdet_en	da_pcie_sigdet_en force mode register
14		rg_ssusb_force_sigdet_en	Enables da_pcie_sigdet_en force mode
13		rg_ssusb_clkrx_en	da_pcie_clkrx_en force mode register
12		rg_ssusb_force_clkrx_en	Enables da_pcie_clkrx_en force mode
11		rg_ssusb_clktx_en	da_pcie_clktx_en force mode register
10		rg_ssusb_force_clktx_en	Enables da_pcie_clktx_en force mode
9		rg_ssusb_clk_req_n_i	ssusb_clk_req_n_i force mode register
8		rg_ssusb_force_clk_req_n_i	Enables ssusb_clk_req_n_i force mode
6		rg_ssusb_rate	ssusb_rate force mode register
5		rg_ssusb_force_rate	Enables ssusb_rate force mode
4		rg_ssusb_pcie_mode_sel	ssusb_pcie_mode force mode register
3		rg_ssusb_force_pcie_mode_sel	Enables ssusb_pcie_mode force mode
2:1		rg_ssusb_phy_mode	ssusb_phy_mode force mode register

Bit(s)	Mnemonic	Name	Description
0		rg_ssusb_force _phy_mode	Enables ssusb_phy_mode force mode

11290A04 B2_PHYD_TOP2 **Bank 2 SSUSB PHYD TOP2** **25112A32**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		rg_ssusb_force_idrv_6db	rg_ssusb_idrv_6db							rg_ssusb_force_idem_3p5db	rg_ssusb_idem_3p5db					
Type		RW	RW							RW	RW					
Reset		0	1	0	0	1	0	1		0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		rg_ssusb_force_idrv_3p5db	rg_ssusb_idrv_3p5db							rg_ssusb_force_idrv_odb	rg_ssusb_idrv_odb					
Type		RW	RW							RW	RW					
Reset		0	1	0	1	0	1	0		0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
30		rg_ssusb_force _idrv_6db	**Forces da_ssusb_idrv_6db to rg_ssusb_idrv_6db**
29:24		rg_ssusb_idrv_ 6db	**TX driver tail current control for 6dB de-empahsis mode** 000000: 0mA 000001: 0.4mA 000010: 0.8mA 111111: 25.2mA
22		rg_ssusb_force _idem_3p5db	**Forces da_ssusb_idem_3p5db to rg_ssusb_idem_3p5db**
21:16		rg_ssusb_idem_ 3p5db	**TX driver de-emphasis current control for 3.5dB de-empahsis mode** 000000: 0mA 000001: 0.2mA 000010: 0.4mA 111111: 12.6mA
14		rg_ssusb_force _idrv_3p5db	**Forces da_ssusb_idrv_3p5db to rg_ssusb_idrv_3p5db**
13:8		rg_ssusb_idrv_ 3p5db	**TX driver tail current control for 3.5dB de-empahsis mode** 000000: 0mA 000001: 0.4mA 000010: 0.8mA 111111: 25.2mA
6		rg_ssusb_force _idrv_odb	**Forces da_ssusb_idrv_odb to rg_ssusb_idrv_odb**
5:0		rg_ssusb_idrv_ odb	**TX driver tail current control for 0dB de-empahsis mode** 000000: 0mA

Bit(s)	Mnemonic	Name	Description
			000001: 0.4mA 000010: 0.8mA 111111: 25.2mA

11290A08 B2_PHYD_TOP3 Bank 2 SSUSB PHYD TOP3 0A010019

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					rg_ssusb_tx_bias_i			rg_ssusb_force_tx_biasi_en								rg_ssusb_tx_biasi_en
Type					RW			RW								RW
Reset					1	0	1	0								1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			rg_ssusb_force_tx_biasi					rg_ssusb_force_idem_6db			rg_ssusb_idem_6db					
Type			RW					RW			RW					
Reset			0					0			0	1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
27:25		rg_ssusb_tx_bi asi	**TX driver bias I control** 000: 3mA 001: 4mA 010: 5mA 011: 6mA 100: 4mA 101: 5mA 110: 6mA 111: 7mA
24		rg_ssusb_force _tx_biasi_en	**Forces da_ssusb_tx_biasi_en to rg_ssusb_tx_biasi_en**
16		rg_ssusb_tx_bi asi_en	**Enables TX driver bias I from 3.3V** 0: Disable 1: Enable
13		rg_ssusb_force _tx_biasi	**Forces da_ssusb_tx_biasi to rg_ssusb_tx_biasi**
8		rg_ssusb_force _idem_6db	**Forces da_ssusb_idem_6db to rg_ssusb_idem_6db**
5:0		rg_ssusb_idem_ 6db	**TX driver de-emphasis current control for 6dB de-empahsis mode** 000000: 0mA 000001: 0.2mA 000010: 0.4mA 111111: 12.6mA

11290A0C B2_PHYD_TOP4 Bank 2 SSUSB PHYD TOP4 FF0E0E0E

P4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_s susb _g1_ cdr_ bic_ ltr				rg_ssusb_g1_c dr_bic_ltdo							rg_ssusb_g1_cdr_bc_lt d1				
Type	RW				RW							RW				
Reset	1	1	1	1	1	1	1	1				0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		rg_ssusb_ g1_l1ss_c dr_bw_sel		rg_ssusb_g1_cdr_bc_lt r						rg_ssusb_ g1_cdr_bw _sel		rg_ssusb_g1_cdr_bc_lt do				
Type		RW		RW						RW		RW				
Reset		0	0	0	1	1	1	0		0	0	0	1	1	1	0

Bit(s)	Mnemonic	Name	Description
31:28	**g1_cdr_bic_ltr**	rg_ssusb_g1_cd r_bic_ltr	Register control for PCIe G1 CDR bic ltr
27:24	**g1_cdr_bic_ltd 0**	rg_ssusb_g1_cd r_bic_ltdo	Register control for PCIe G1 CDR bic ltd
20:16	**g1_cdr_bc_ltd1**	rg_ssusb_g1_cd r_bc_ltd1	Register control for PCIe G1 CDR bc ltd
14:13		rg_ssusb_g1_l1 ss_cdr_bw_sel	
12:8	**g1_cdr_bc_ltr**	rg_ssusb_g1_cd r_bc_ltr	Register control for PCIe G1 CDR bc ltr
6:5		rg_ssusb_g1_cd r_bw_sel	
4:0	**g1_cdr_bc_ltdo**	rg_ssusb_g1_cd r_bc_ltdo	Register control for PCIe G1 CDR bc ltd

11290A10 B2_PHYD_TOP5 Bank 2 SSUSB PHYD TOP5 040A1004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				rg_s susb _g1_ cdr_ bir_ ltd1								rg_ssusb_g1_c dr_bir_ltr				
Type				RW								RW				
Reset				0	0	1	0	0				0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				rg_ssusb_g1_cdr_bir_l tdo									rg_ssusb_g1_cdr_b ic_ltd1			
Type				RW									RW			
Reset				1	0	0	0	0					0	1	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**g1_cdr_bir_ltd 1**	rg_ssusb_g1_cd r_bir_ltd1	Register control for PCIe G1 CDR bir ltd
20:16	**g1_cdr_bir_ltr**	rg_ssusb_g1_cd r_bir_ltr	Register control for PCIe G1 CDR bir ltr
12:8	**g1_cdr_bir_ltd 0**	rg_ssusb_g1_cd r_bir_ltdo	Register control for PCIe G1 CDR bir ltd
3:0	**g1_cdr_bic_ltd 1**	rg_ssusb_g1_cd r_bic_ltd1	Register control for PCIe G1 CDR bic ltd

11290A14 B2_PHYD_TOP6 Bank 2 SSUSB PHYD TOP6 F80E0E0E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_s susb _g2_ cdr_ bic_ ltr				rg_ssusb_g2_c dr_bic_ltdo							rg_ssusb_g2_cdr_bc_lt d1				
Type	RW				RW							RW				
Reset	1	1	1	1	1	0	0	0				0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		rg_ssusb_ g2_l1ss_c dr_bw_sel		rg_ssusb_g2_cdr_bc_lt r						rg_ssusb_ g2_cdr_bw _sel		rg_ssusb_g2_cdr_bc_lt do				
Type		RW		RW						RW		RW				
Reset		0	0	0	1	1	1	0		0	0	0	1	1	1	0

Bit(s)	Mnemonic	Name	Description
31:28	**g2_cdr_bic_ltr**	rg_ssusb_g2_cd r_bic_ltr	Register control for PCIe G2 CDR bic ltr
27:24	**g2_cdr_bic_ltd o**	rg_ssusb_g2_cd r_bic_ltdo	Register control for PCIe G2 CDR bic ltd
20:16	**g2_cdr_bc_ltd1**	rg_ssusb_g2_cd r_bc_ltd1	Register control for PCIe G2 CDR bc ltd
14:13		rg_ssusb_g2_l1 ss_cdr_bw_sel	
12:8	**g2_cdr_bc_ltr**	rg_ssusb_g2_cd r_bc_ltr	Register control for PCIe G2 CDR bc ltr
6:5		rg_ssusb_g2_cd r_bw_sel	
4:0	**g2_cdr_bc_ltdo**	rg_ssusb_g2_cd r_bc_ltdo	Register control for PCIe G2 CDR bc ltd

11290A18 **B2_PHYD_TOP7** **Bank 2 SSUSB PHYD TOP7** **020A0802**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				rg_s susb _g2_ cdr_ bir_ ltd1								rg_ssusb_g2_c dr_bir_ltr				
Type				RW								RW				
Reset				0	0	0	1	0				0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				rg_ssusb_g2_cdr_bir_l tdo									rg_ssusb_g2_cdr_b ic_ltd1			
Type				RW									RW			
Reset				0	1	0	0	0					0	0	1	0

Bit(s)	Mnemonic	Name	Description
28:24	**g2_cdr_bir_ltd 1**	rg_ssusb_g2_cd r_bir_ltd1	Register control for PCIe G2 CDR bir ltd
20:16	**g2_cdr_bir_ltr**	rg_ssusb_g2_cd r_bir_ltr	Register control for PCIe G2 CDR bir ltr
12:8	**g2_cdr_bir_ltd 0**	rg_ssusb_g2_cd r_bir_ltdo	Register control for PCIe G2 CDR bir ltd
3:0	**g2_cdr_bic_ltd 1**	rg_ssusb_g2_cd r_bic_ltd1	Register control for PCIe G2 CDR bic ltd

11290A1C **B2_PHYD_P_SIGDET1** **Bank 2 SSUSB PHYD_P_SIGDET1** **07070302**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_p_sigdet_flt_dis	rg_ssusb_p_sigdet_flt_g2_deast_sel								rg_ssusb_p_sigdet_flt_g1_deast_sel						
Type	RW	RW								RW						
Reset	0	0	0	0	0	1	1	1		0	0	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		rg_ssusb_p_sigdet_flt_p2_ast_sel								rg_ssusb_p_sigdet_flt_px_ast_sel						
Type		RW								RW						
Reset		0	0	0	0	0	1	1		0	0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
31	**p_sigdet_flt_dis**	rg_ssusb_p_sigdet_flt_dis	**Sigdet filter control** 1'b0: Enable filter 1'b1: Disable filter
30:24	**p_sigdet_flt_g2_deast_sel**	rg_ssusb_p_sigdet_flt_g2_deast_sel	**Selects sigdet kick out** Continuous sigdet is deasserted when OP at G2; 1 scale represents 2 ref_ck cycles.
22:16	**p_sigdet_flt_g1_deast_sel**	rg_ssusb_p_sigdet_flt_g1_deast_sel	**Selects sigdet kick out** Continuous sigdet is deasserted when OP at G1; 1 scale represents 2 ref_ck cycles.
14:8	**p_sigdet_flt_p2_ast_sel**	rg_ssusb_p_sigdet_flt_p2_ast_sel	**Selects sigdet kick in** Continuous sigdet is assert at P2; 1 scale represents 2 ref_ck cycles.
6:0	**p_sigdet_flt_px_ast_sel**	rg_ssusb_p_sigdet_flt_px_ast_sel	**Selects sigdet kick in** Continuous sigdet is asserted at P0/P0s/P1; 1 scale represents 2 ref_ck cycles.

11290A20 B2_PHYD_P_SIGDET2 **Bank 2 SSUSB PHYD_P_SIGDET2** **0200011A**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			rg_ssusb_p_sigdet_rx_val_s	rg_ssusb_p_sigdet_los_deas_sel	rg_ssusb_p_sigdet_los_exit_s	rg_ssusb_p_sigdet_los_exit_s		rg_ssusb_p_sigdet_los_exit_s								rg_ssusb_p_sigdet_los_entry_s
Type			RW	RW	RW	RW		RW								RW
Reset			0	0	0	0	1	0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						rg_ssusb_p_sigdet_prb_sel	rg_ssusb_p_sigdet_bk_sig_t			rg_ssusb_p_sigdet_p2_rxlfps	rg_ssusb_p_sigdet_non_bk_ad	rg_ssusb_p_sigdet_bk_b_rxeq	rg_ssusb_p_sigdet_g2_ko_sel		rg_ssusb_p_sigdet_g1_ko_sel	
Type						RW	RW			RW	RW	RW	RW		RW	
Reset						0	0	1		0	0	1	1	0	1	0

Bit(s)	Mnemonic	Name	Description
29	**p_sigdet_rx_val_s**	rg_ssusb_p_sigdet	**Selects deassert sigdet when at Los moment**

Bit(s)	Mnemonic	Name	Description
		det_rx_val_s	1'b0: rx_val_pcie will be deasserted when p1/p2. 1'b1: rx_val_pcie deassertion does not depend on p1/p2.
28	**p_sigdet_los_deas_sel**	rg_ssusb_p_sigdet_los_deas_sel	**Selects deassert sigdet when at Los moment** 1'b0: Normal 1'b1: Deassert when to_los moment
27	**p_sigdet_lo_exit_s**	rg_ssusb_p_sigdet_lo_exit_s	**kick_out option when ssusbpower_down[1]=1** 1'b0: Nornal 1'b1: Kick out when ssusb_powerdown[1] = 1
26:25	**p_sigdet_los_exit_t_s**	rg_ssusb_p_sigdet_los_exit_t _s	**Selects Los exit, kick in time** 2'd0: 1 ref_ck cycles 2'd1: 25 ref_ck cycles 2'd2: 37 ref_ck cycles 2'd3: 50 ref_ck cycles
24	**p_sigdet_los_exit_s**	rg_ssusb_p_sigdet_los_exit_s	**Selects Los exit, kick in condition**
16	**p_sigdet_los_entry_s**	rg_ssusb_p_sigdet_los_entry_ s	**Selects Los entry, kick out condition**
10	**p_sigdet_prb_s el**	rg_ssusb_p_sigdet_prb_sel	**ssusb_p_sigdet_prb_select**
9:8	**p_sigdet_bk_si g_t**	rg_ssusb_p_sigdet_bk_sig_t	**Temporarily disable sigdet flt control when kick off** 2'd0: 3 ref_ck cycles 2'd1: 7 ref_ck cycles 2'd2: 15 ref_ck cycles 2'd3: 31 ref_ck cycles
6	**p_sigdet_p2_rx lfps**	rg_ssusb_p_sigdet_p2_rxlfps	**RxElecIdle function at P2** 1'b0: RxElecIdle is !sigdet_fit. 1'b1: RxElecIdle is !ad_ssusb_rx_lfps.
5	**p_sigdet_non_bk_ad**	rg_ssusb_p_sigdet_non_bk_ad	
4	**p_sigdet_bk_b_rxeq**	rg_ssusb_p_sigdet_bk_b_rxeq	**rx_val_pcie block by rxeqtraining_pdnctl** 1'b0: RX valid does not care rxeqtraining_pdnctll. 1'b1: RX valid when rxeqtraining_pdnctl is deasserted.
3:2	**p_sigdet_g2_ko_sel**	rg_ssusb_p_sigdet_g2_ko_sel	**Selects G2 sigdet kick out condition** 2d0: ~rxpll_lock 2d1: ~rxpll_lock or ~sigdet_flt 2d2: ~rxpll_lock or eios_det_ppctl 2d3: ~rxpll_lock or error_det_ppctl
1:0	**p_sigdet_g1_ko _sel**	rg_ssusb_p_sigdet_g1_ko_sel	**Selects G1 sigdet kick out condition** 2d0: ~rxpll_lock 2d1: ~rxpll_lock or ~sigdet_flt 2d2: ~rxpll_lock or ~sigdet_flt or eios_det_ppctl 2d3: ~rxpll_lock or ~sigdet_flt or error_det_ppctl

11290A24 **B2_PHYD_P_SIGDET_CAL1** **Bank 2 SSUSB PHYD_P_SIGDET_CAL1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			rg_ssusb_g2_2eios_det_en	rg_ssusb_p_sigdet_cal_offset												rg_ssusb_p_force_sigdet_cal_offset
Type			RW	RW												RW

Reset			0	0	0	0	0	0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								rg_ssusb_p_sigdet_cal_en					rg_ssusb_p_force_sigdet_cal_en	rg_ssusb_p_sigdet_flt_en	rg_ssusb_p_sigdet_sample_prd	rg_ssusb_p_sigdet_rek
Type								RW					RW	RW	RW	RW
Reset								0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
29		rg_ssusb_g2_2eios_det_en	**Selects PCIe Gen2 EIOS detector** 1'b0: 1 EIOS complete RX EIOS detection 1'b1: 2 EIOS complete RX EIOS detection
28:24		rg_ssusb_p_sigdet_cal_offset	**da_pcie_sigdet_cal_offset force mode register**
16		rg_ssusb_p_force_sigdet_cal_ offset	**Enables da_pcie_sigdet_cal_offset force mode**
8		rg_ssusb_p_sigdet_cal_en	**da_pcie_sigdet_cal_en force mode register**
3		rg_ssusb_p_force_sigdet_cal_ en	**Enables da_pcie_sigdet_cal_en force mode**
2		rg_ssusb_p_sigdet_flt_en	**Filter of ad_pcie_sigdet_cal_out control** 1'b0: Disable 1'b1: Enable
1		rg_ssusb_p_sigdet_sample_prd	**Selects waiting cycles for sample ad_pcie_sigdet_cal_out** 1'b0: 2 ref_ck cycles 1'b1: 5 ref_ck cycles
0		rg_ssusb_p_sigdet_rek	**Redoes signal detection calibration** 1'b0: Disable 1'b1: Redo sigdet calibration

11290A28 B2_PHYD_RXDET1 **Bank 2 SSUSB PHYD_RXDET1** **00A0203C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_rxdet_prb_sel	rg_ssusb_force_cmdet	rg_ssusb_rxdet_en	rg_ssusb_force_rxdet_en	rg_ssusb_rxdet_k_twice	rg_ssusb_rxdet_stb3_set									rg_ssusb_rxdet_stb2_set	
Type	RW	RW	RW	RW	RW	RW									RW	
Reset	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_rxdet_stb2_set							rg_ssusb_rxdet_stb1_set								
Type	RW							RW								
Reset	0	0	1	0	0	0	0	0	0	0	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
31		rg_ssusb_rxdet_prb_sel	**Selects ssusb_rxdet probe out**
30		rg_ssusb_force_cmdet	

Bit(s)	Mnemonic	Name	Description
29		rg_ssusb_rxdet _en	**da_ssusb_rxdet_en force mode register**
28		rg_ssusb_force _rxdet_en	**Enables da_ssusb_rxdet_en force mode**
27		rg_ssusb_rxdet _k_twice	**Calibration time** 1'b0: Once 1'b1: Twice
26:18		rg_ssusb_rxdet _stb3_set	**Selects RX detection stable time when ssusb_powerdown=2b10** 1 scale represents 64 reference cycles. Covers reference clock from 1M~100MHz, 63us~327us.
17:9		rg_ssusb_rxdet _stb2_set	**Selects RX detection stable time when ssusb_powerdown=2b10** 1 scale represents 8 reference cycles. Covers reference clock from 1M~100MHz, 7us~40us.
8:0		rg_ssusb_rxdet _stb1_set	**Selects TX discharge stable time** 1 scale represents 64 reference cycles. Covers reference clock from 1M~100MHz, 63us~327us.

11290A2C B2_PHYD_RXDET2 **Bank 2 SSUSB PHYD_RXDET2** **18805020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_phyd_traindec_force_cgen	rg_ssusb_phyd_bertlb_force_cgen	rg_ssusb_phyd_t2rlb_force_cgen	rg_ssusb_lck2ref_ext_en	rg_ssusb_g2_lck2ref_ext_sel				rg_ssusb_lck2ref_ext_sel				rg_ssusb_pdn_t_sel		rg_ssusb_rxdet_stb3_set_p3	
Type	RW	RW	RW	RW	RW				RW				RW		RW	
Reset	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_rxdet_stb3_set_p3								rg_ssusb_rxdet_stb2_set_p3							
Type	RW								RW							
Reset	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		rg_ssusb_phyd_ traindec_force _cgen	
30		rg_ssusb_phyd_ bertlb_force_c gen	
29		rg_ssusb_phyd_ t2rlb_force_cg en	
28		rg_ssusb_lck2r ef_ext_en	
27:24		rg_ssusb_g2_lc k2ref_ext_sel	
23:20		rg_ssusb_lck2r ef_ext_sel	
19:18		rg_ssusb_pdn_t _sel	**Selects rate switch, txpll/rxpll power-down time** 2'd0: 2us 2'd1: 4us 2'd2: 8us 2'd3: 16us
17:9		rg_ssusb_rxdet _stb3_set_p3	**Selects RX detection stable time when ssusb_powerdown=2b11**

Bit(s)	Mnemonic	Name	Description
8:0		rg_ssusb_rxdet_stb2_set_p3	1 scale represents 64 reference cycles. Covers reference clock from 1M~100MHz, 63us~327us. **Selects RX detection stable time when ssusb_powerdown=2b11** 1 scale represents 8 reference cycles. Covers reference clock from 1M~100MHz, 7us~40us.

11290A30 B2_PHYD_MISC0 B2_PHYD_MISC0 14000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_tx_eidle_lp_podlycyc						rg_ssusb_tx_ser_en	rg_ssusb_force_tx_ser_en	rg_ssusb_txpll_refcksel	rg_ssusb_force_pll_dds_hf_en	rg_ssusb_pll_dds_hf_en_man	rg_ssusb_rxlfps_entxdrv	rg_ssusb_rx_fl_unlockth			
Type	RW						RW	RW	RW	RW	RW	RW	RW			
Reset	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_lfps_psel	rg_ssusb_rx_sigdet_en	rg_ssusb_rx_sigdet_en_sel	rg_ssusb_rx_pi_cal_en	rg_ssusb_rx_pi_cal_en_sel	rg_ssusb_p3_cls_ck_sel	rg_ssusb_t2rlb_psel		rg_ssusb_ppctl_psel			rg_ssusb_phyd_tx_data_inv	rg_ssusb_bertlb_psel		rg_ssusb_retrack_dis	rg_ssusb_pperrcnt_clr
Type	RW	RW	RW	RW	RW	RW	RW		RW			RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:26		rg_ssusb_tx_eidle_lp_podlycyc	rg_ssusb_tx_eidle_lp_podlycyc
25		rg_ssusb_tx_ser_en	rg_ssusb_force_tx_ser_en
24		rg_ssusb_force_tx_ser_en	rg_ssusb_force_tx_ser_en
23	**0 txpll power on after xtalb ias stable 1 t xpll power on after syspll s table**	rg_ssusb_txpll_refcksel	rg_ssusb_txpll_refcksel
22		rg_ssusb_force_pll_dds_hf_en	rg_ssusb_force_pll_dds_hf_en
21		rg_ssusb_pll_dds_hf_en_man	rg_ssusb_pll_dds_hf_en_man
20	**performance option, when rx lfps, enable t x drive**	rg_ssusb_rxlfps_entxdrv	rg_ssusb_rxlfps_entxdrrrv
19:16		rg_ssusb_rx_fl_unlockth	rg_ssusb_rx_fl_unlockth
15		rg_ssusb_lfps_psel	rg_ssusb_lfps_psel
14		rg_ssusb_rx_sigdet_en	rg_ssusb_rx_sigdet_en
13		rg_ssusb_rx_sigdet_en_sel	rg_ssusb_rx_sigdet_en_sel
12		rg_ssusb_rx_pi_cal_en	rg_ssusb_rx_pi_cal_en
11		rg_ssusb_rx_pi_cal_en_sel	rg_ssusb_rx_pi_cal_en_sel

Bit(s)	Mnemonic	Name	Description
10		rg_ssusb_p3_cl s_ck_sel	rg_ssusb_p3_cls_ck_sel
9:8		rg_ssusb_t2rlb _psel	Selects t2rlb probe
7:5		rg_ssusb_ppctl _psel	Selects ppctl probe
4		rg_ssusb_phyd_ tx_data_inv	Inverts TX data
3:2		rg_ssusb_bertl b_psel	Selects bertlb probe
1		rg_ssusb_retra ck_dis	rg_ssusb_retrack_dis
0	**rg_ssusb_pperr cnt_clr**	rg_ssusb_pperr cnt_clr	Clears pipe error counter

11290A34 B2_PHYD_MI SC2 **B2_PHYD_MISC2** **46426C8B**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_frc_pll_dds_prediv2	rg_ssusb_frc_pll_dds_iadj				rg_ssusb_p_sigdet_125filter	rg_ssusb_p_sigdet_rst_filter	rg_ssusb_p_sigdet_eid_use_raw	rg_ssusb_p_sigdet_ltd_use_raw	rg_ssusb_eidle_bf_rxdet	rg_ssusb_eidle_lp_stbcyc					
Type	RW	RW				RW	RW	RW	RW	RW	RW					
Reset	0	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_eidle_lp_stbcyc			rg_ssusb_tx_eidle_lp_postdly						rg_ssusb_tx_eidle_lp_predly						rg_ssusb_tx_eidle_lp_en_adv
Type	RW			RW						RW						RW
Reset	0	1	1	0	1	1	0	0	1	0	0	0	1	0	1	1

Bit(s)	Mnemonic	Name	Description
31	**rg_ssusb_pll_d ds_prediv2**	rg_ssusb_frc_p ll_dds_prediv2	rg_ssusb_pll_dds_prediv2
30:27	**rg_ssusb_pll_d ds_iadj**	rg_ssusb_frc_p ll_dds_iadj	rg_ssusb_pll_dds_iadj
26	**rg_ssusb_p_sig det_125filter**	rg_ssusb_p_sig det_125filter	rg_ssusb_p_sigdet_125filter
25	**rg_ssusb_p_sig det_rst_filter**	rg_ssusb_p_sig det_rst_filter	rg_ssusb_p_sigdet_rst_filter
24	**rg_ssusb_p_sig det_eid_use_ra w**	rg_ssusb_p_sig det_eid_use_ra w	rg_ssusb_p_sigdet_eid_use_raw
23	**rg_ssusb_p_sig det_ltd_use_ra w**	rg_ssusb_p_sig det_ltd_use_ra w	rg_ssusb_p_sigdet_ltd_use_raw
22	**rg_ssusb_eidle _bf_rxdet**	rg_ssusb_eidle _bf_rxdet	rg_ssusb_eidle_bf_rxdet
21:13	**rg_ssusb_eidle _lp_stbcyc**	rg_ssusb_eidle _lp_stbcyc	rg_ssusb_eidle_lp_stbcyc
12:7	**rg_ssusb_tx_ei dle_lp_postdly**	rg_ssusb_tx_ei dle_lp_postdly	rg_ssusb_tx_eidle_lp_postdly
6:1	**rg_ssusb_tx_ei dle_lp_predly**	rg_ssusb_tx_ei dle_lp_predly	rg_ssusb_tx_eidle_lp_predly
0		rg_ssusb_tx_ei dle_lp_en_adv	rx_ssusb_tx_eidle_lp_en_adv

Bit(s)	Mnemonic	Name	Description

11290A38 B2_PHYD_MISC3 B2_PHYD_MISC3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														rgs_ssusb_dds_calib_c_state		
Type														RO		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgs_ssusb_pperrcnt															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
18:16	**rgs_ssusb_dds_calib_c_state**	rgs_ssusb_dds_calib_c_state	rgs_ssusb_dds_calib_c_state
15:0	**rgs_ssusb_pperrcnt**	rgs_ssusb_pperrcnt	Pipe error counter

11290A3C B2_PHYD_L1SS B2_PHYD_L1SS 00000080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_l1ss_rev1								rg_ssusb_l1ss_revo							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					rg_ssusb_p_ltd1_slock_dis	rg_ssusb_pll_cnt_clean_dis	rg_ssusb_p_pll_rek_sel	rg_ssusb_txdrv_maskdly	rg_ssusb_rxsts_val	rg_pcie_phy_clkreq_n_en	rg_pcie_force_phy_clkreq_n_en	rg_pcie_phy_clkreq_n_out	rg_pcie_force_phy_clkreq_n_out	rg_ssusb_rxpll_stb_pxo	rg_pcie_l1ss_en	rg_pcie_force_l1ss_en
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**rg_ssusb_l1ss_rev1**	rg_ssusb_l1ss_rev1	rg_ssusb_l1ss_rev1
23:16	**rg_ssusb_l1ss_revo**	rg_ssusb_l1ss_revo	rg_ssusb_l1ss_revo
11	**rg_ssusb_p_ltd1_slock_dis**	rg_ssusb_p_ltd1_slock_dis	
10	**rg_ssusb_pll_cnt_clean_dis**	rg_ssusb_pll_cnt_clean_dis	rg_ssusb_pll_cnt_clean_dis
9	**rg_ssusb_p_pll_rek_sel**	rg_ssusb_p_pll_rek_sel	rg_ssusb_p_pll_rek_sel
8	**rg_ssusb_txdrv_maskdly**	rg_ssusb_txdrv_maskdly	rg_ssusb_txdrv_maskdly
7	**rg_ssusb_rxsts_val**	rg_ssusb_rxsts_val	rg_ssusb_rxsts_val
6	**rg_pcie_phy_clkreq_n_en**	rg_pcie_phy_clkreq_n_en	rg_pcie_phy_clkreq_n_en
5	**rg_pcie_force_phy_clkreq_n_en**	rg_pcie_force_phy_clkreq_n_en	rg_pcie_force_phy_clkreq_n_en

Bit(s)	Mnemonic	Name	Description
4	**rg_pcie_phy_clkreq_n_out**	rg_pcie_phy_clkreq_n_out	rg_pcie_phy_clkreq_n_out
3	**rg_pcie_force_phy_clkreq_n_out**	rg_pcie_force_phy_clkreq_n_out	rg_pcie_force_phy_clkreq_n_out
2	**rg_ssusb_rxpll_stb_pxo**	rg_ssusb_rxpll_stb_pxo	rg_ssusb_rxpll_stb_pxo
1	**rg_pcie_l1ss_en**	rg_pcie_l1ss_en	rg_pcie_l1ss_en
0	**rg_pcie_force_l1ss_en**	rg_pcie_force_l1ss_en	rg_pcie_force_l1ss_en

11290A40 B2_ROSC_0 **B2_ROSC_0** **ED7F0001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_ring_osc_cntend									rg_ssusb_xtal_osc_cntend						
Type	RW									RW						
Reset	1	1	1	0	1	1	0	1	0	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													rg_ssusb_ring_osc_en	rg_ssusb_ring_osc_force_en	rg_ssusb_frc_ring_bypass_det	rg_ssusb_ring_bypass_det
Type													RW	RW	RW	RW
Reset													0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:23	**rg_ssusb_ring_osc_cntend**	rg_ssusb_ring_osc_cntend	rg_ssusb_ring_osc_cntend
22:16	**rg_ssusb_xtal_osc_cntend**	rg_ssusb_xtal_osc_cntend	rg_ssusb_xtal_osc_cntend
3	**rg_ssusb_ring_osc_en**	rg_ssusb_ring_osc_en	rg_ssusb_ring_osc_en
2	**rg_ssusb_ring_osc_force_en**	rg_ssusb_ring_osc_force_en	rg_ssusb_ring_osc_force_en
1	**rg_ssusb_frc_ring_bypass_det**	rg_ssusb_frc_ring_bypass_det	rg_ssusb_frc_ring_bypass_det
0	**rg_ssusb_ring_bypass_det**	rg_ssusb_ring_bypass_det	rg_ssusb_ring_bypass_det

11290A44 B2_ROSC_1 **B2_ROSC_1** **00060001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												rg_ssusb_ring_osc_frc_p3	rg_ssusb_ring_osc_p3	rg_ssusb_ring_osc_frc_recal		rg_ssusb_ring_osc_recal
Type												RW	RW	RW		RW
Reset												0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_ring_osc_sel															rg_ssusb_ring_osc_fr

																c_sel
Type	RW															RW
Reset	0	0	0	0	0	0	0	0								1

Bit(s)	Mnemonic	Name	Description
20	rg_ssusb_ring_osc_frc_p3	rg_ssusb_ring_osc_frc_p3	rg_ssusb_ring_osc_frc_p3
19	rg_ssusb_ring_osc_p3	rg_ssusb_ring_osc_p3	rg_ssusb_ring_osc_p3
18:17	rg_ssusb_ring_osc_frc_recal	rg_ssusb_ring_osc_frc_recal	rg_ssusb_ring_osc_frc_recal
16	rg_ssusb_ring_osc_recal	rg_ssusb_ring_osc_recal	rg_ssusb_ring_osc_recal
15:8	rg_ssusb_ring_osc_sel	rg_ssusb_ring_osc_sel	rg_ssusb_ring_osc_sel
0	rg_ssusb_ring_osc_frc_sel	rg_ssusb_ring_osc_frc_sel	rg_ssusb_ring_osc_frc_sel

11290A48 B2_ROSC_2 **B2_ROSC_2** **00800020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_ring_det_strcyc2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_ring_det_strcyc1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	rg_ssusb_ring_det_strcyc2	rg_ssusb_ring_det_strcyc2	rg_ssusb_ring_det_strcyc2
15:0	rg_ssusb_ring_det_strcyc1	rg_ssusb_ring_det_strcyc1	rg_ssusb_ring_det_strcyc1

11290A4C B2_ROSC_3 **B2_ROSC_3** **01500090**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_ring_det_detwin1															
Type	RW															
Reset	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_ring_det_strcyc3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	rg_ssusb_ring_det_detwin1	rg_ssusb_ring_det_detwin1	rg_ssusb_ring_det_detwin1
15:0	rg_ssusb_ring_det_strcyc3	rg_ssusb_ring_det_strcyc3	rg_ssusb_ring_det_strcyc3

11290A50 B2_ROSC_4 **B2_ROSC_4** **02200160**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_ring_det_detwin3															
Type	RW															
Reset	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_ring_det_detwin2															
Type	RW															
Reset	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	**rg_ssusb_ring_det_detwin3**	rg_ssusb_ring_det_detwin3	rg_ssusb_ring_det_detwin3
15:0	**rg_ssusb_ring_det_detwin2**	rg_ssusb_ring_det_detwin2	rg_ssusb_ring_det_detwin2

11290A54 B2_ROSC_5 **B2_ROSC_5** **00030000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_ring_det_lbond1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_ring_det_ubond1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	**rg_ssusb_ring_det_lbond1**	rg_ssusb_ring_det_lbond1	rg_ssusb_ring_det_lbond1
15:0	**rg_ssusb_ring_det_ubond1**	rg_ssusb_ring_det_ubond1	rg_ssusb_ring_det_ubond1

11290A58 B2_ROSC_6 **B2_ROSC_6** **00050000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_ring_det_lbond2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_ring_det_ubond2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	**rg_ssusb_ring_det_lbond2**	rg_ssusb_ring_det_lbond2	rg_ssusb_ring_det_lbond2
15:0	**rg_ssusb_ring_det_ubond2**	rg_ssusb_ring_det_ubond2	rg_ssusb_ring_det_ubond2

11290A5C B2_ROSC_7 **B2_ROSC_7** **00070000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_ring_det_lbond3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_ssusb_ring_det_ubond3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	**rg_ssusb_ring_det_lbond3**	rg_ssusb_ring_det_lbond3	rg_ssusb_ring_det_lbond3
15:0	**rg_ssusb_ring_det_ubond3**	rg_ssusb_ring_det_ubond3	rg_ssusb_ring_det_ubond3

11290A60 B2_ROSC_8 **B2_ROSC_8** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ssusb_ring_reserve															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											rg_ssusb_rosc_prob_sel				rg_ssusb_ring_freqmeter_en	rg_ssusb_ring_det_bps_ubond
Type											RW				RW	RW
Reset											0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:16	**rg_ssusb_ring_reserve**	rg_ssusb_ring_reserve	rg_ssusb_ring_reserve
5:2	**rg_ssusb_rosc_prob_sel**	rg_ssusb_rosc_prob_sel	rg_ssusb_rosc_prob_sel
1	**rg_ssusb_ring_freqmeter_en**	rg_ssusb_ring_freqmeter_en	rg_ssusb_ring_freqmeter_en
0	**rg_ssusb_ring_det_bps_ubond**	rg_ssusb_ring_det_bps_ubond	rg_ssusb_ring_det_bps_ubond

11290A64 B2_ROSC_9 **B2_ROSC_9** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rgs_fm_ring_cnt															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					rgs_ssusb_ring_osc_state		rgs_ssusb_ring_osc_stable	rgs_ssusb_ring_osc_cal_fail	rgs_ssusb_ring_osc_cal							

Type					RO		RO	RO	RO							
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16	**rgs_fm_ring_cn t**	rgs_fm_ring_cn t	rgs_fm_ring_cnt
11:10	**rgs_ssusb_ring _osc_state**	rgs_ssusb_ring _osc_state	rgs_ssusb_ring_osc_state
9	**rgs_ssusb_ring _osc_stable**	rgs_ssusb_ring _osc_stable	rgs_ssusb_ring_osc_stable
8	**rgs_ssusb_ring _osc_cal_fail**	rgs_ssusb_ring _osc_cal_fail	rgs_ssusb_ring_osc_cal_fail
7:0	**rgs_ssusb_ring _osc_cal**	rgs_ssusb_ring _osc_cal	rgs_ssusb_ring_osc_cal

11290A68 B2_ROSC_A **B2_ROSC_A** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									rgs_ssusb_rosc_prob_out							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**rgs_ssusb_rosc _prob_out**	rgs_ssusb_rosc _prob_out	rgs_ssusb_rosc_prob_out

11290A70 B2_2step_sigdet **B2_2step_sigdet** **08100001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					rg_s susb _p_c _sig det_ cal_ offs et				rg_ssusb_pcie_2step_fth							
Type					RW				RW							
Reset					1	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						rg_s susb _p_c _for ce_s igde t_ca l_of fset	rg_s susb _p_c _sig det_ cal_ en	rg_s susb _p_c _for ce_s igde t_ca l_en	rg_s susb _p_c _sig det_ flt_ en	rg_s susb _p_c _sig det_ samp le_p rd	rg_s susb _p_c _sig det_ rek	rg_s susb _pci e_cr sdet _rst b	rg_s susb _frc _pci e_cr sdet _rst b	rg_s susb _pci e_cr sdet _en	rg_s susb _frc _pci e_cr sdet _en	rg_s susb _pci e_2s tep_ en
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
27:24	**rg_ssisn_p_c_s igdet_cal_offs et**	rg_ssusb_p_c_s igdet_cal_offs et	rg_ssisn_p_c_sigdet_cal_offset
23:16	**rg_ssusb_pcie_**	rg_ssusb_pcie_	rg_ssusb_pcie_2step_fth

Bit(s)	Mnemonic	Name	Description
	2step_fth	2step_fth	
10	**rg_ssisn_p_c_force_sigdet_cal_offset**	rg_ssusb_p_c_force_sigdet_cal_offset	rg_ssisn_p_c_force_sigdet_cal_offset
9	**rg_ssusb_p_c_sigdet_cal_en**	rg_ssusb_p_c_sigdet_cal_en	rg_ssusb_p_c_sigdet_cal_en
8	**rg_ssusb_p_c_force_sigdet_cal_en**	rg_ssusb_p_c_force_sigdet_cal_en	rg_ssusb_p_c_force_sigdet_cal_en
7	**rg_ssusb_p_c_sigdet_flt_en**	rg_ssusb_p_c_sigdet_flt_en	rg_ssusb_p_c_sigdet_flt_en
6	**rg_ssusb_p_c_sigdet_sample_prd**	rg_ssusb_p_c_sigdet_sample_prd	rg_ssusb_p_c_sigdet_sample_prd
5	**rg_ssusb_p_c_sigdet_rek**	rg_ssusb_p_c_sigdet_rek	rg_ssusb_p_c_sigdet_rek
4	**rg_ssusb_pcie_crsdet_rstb**	rg_ssusb_pcie_crsdet_rstb	rg_ssusb_pcie_crsdet_rstb
3	**rg_ssusb_frc_pcie_crsdet_rstb**	rg_ssusb_frc_pcie_crsdet_rstb	rg_ssusb_frc_pcie_crsdet_rstb
2	**rg_ssusb_pcie_crsdet_en**	rg_ssusb_pcie_crsdet_en	rg_ssusb_pcie_crsdet_en
1	**rg_ssusb_frc_pcie_crsdet_en**	rg_ssusb_frc_pcie_crsdet_en	rg_ssusb_frc_pcie_crsdet_en
0	**rg_ssusb_pcie_2step_en**	rg_ssusb_pcie_2step_en	rg_ssusb_pcie_2step_en

11290A74 **B2_2step_sigdet_1** **B2_2step_sigdet_1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**rgs_ssusb_c_sigcal_done**	**rgs_ssusb_c_sigcal_offset**				**rgs_ssusb_c_sigcal_cal_out**
Type											RO	RO				RO
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5		rgs_ssusb_c_sigcal_done	
4:1		rgs_ssusb_c_sigcal_offset	
0		rgs_ssusb_c_sigcal_cal_out	

11290AE0 **PHYD_VERSION** **PHYD_VERSION** **130506A0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**rgs_ssusb_phyd_version**															

Type	RO															
Reset	0	0	0	1	0	0	1	1	0	0	0	0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgs_ssusb_phyd_version															
Type	RO															
Reset	0	0	0	0	0	1	1	0	1	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	.	.rgs_ssusb_phyd_version	**PHYD version code** [31:8] Release date [7:0] ECO version

11290AE4 PHYD_MODEL PHYD_MODEL 0A60909A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rgs_ssusb_phyd_model															
Type	RO															
Reset	0	0	0	0	1	0	1	0	0	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgs_ssusb_phyd_model															
Type	RO															
Reset	1	0	0	1	0	0	0	0	1	0	0	1	1	0	1	0

Bit(s)	Mnemonic	Name	Description
31:0		rgs_ssusb_phyd_model	Project name string

3.18 MSDC

Module name: MSDC0 Base address: (+11230000h)

Address	Name	Width	Register Function
11230000	MSDC_CFG	32	MSDC Configuration Register
11230004	MSDC_IOCON	32	MSDC IO Configuration Register
11230008	MSDC_PS	32	MSDC Pin Status Register
1123000C	MSDC_INT	32	MSDC Interrupt Register
11230010	MSDC_INTEN	32	MSDC Interrupt Enable Register
11230014	MSDC_FIFOCS	32	MSDC FIFO Control and Status Register
11230018	MSDC_TXDATA	32	MSDC TX Data Port Register
1123001C	MSDC_RXDATA	32	MSDC RX Data Port Register
11230030	SDC_CFG	32	SD Configuration Register
11230034	SDC_CMD	32	SD Command Register
11230038	SDC_ARG	32	SD Argument Register
1123003C	SDC_STS	32	SD Status Register
11230040	SDC_RESP0	32	SD Response Register 0
11230044	SDC_RESP1	32	SD Response Register 1
11230048	SDC_RESP2	32	SD Response Register 2
1123004C	SDC_RESP3	32	SD Response Register 3
11230050	SDC_BLK_NUM	32	SD Block Number Register
11230054	SDC_VOL_CHG	32	SD Voltage Change Wait Time Register
11230058	SDC_CSTS	32	SD Card Status Register
1123005C	SDC_CSTS_EN	32	SD Card Status Enable Register
11230060	SDC_DATCRC_STS	32	SD Card Data CRC Status Register
11230070	EMMC_CFG0	32	EMMC Configuration Register 0
11230074	EMMC_CFG1	32	EMMC Configuration Register 1
11230078	EMMC_STS	32	EMMC Status Register
1123007C	EMMC_IOCON	32	EMMC IO Control Register
11230080	SD_ACMD_RESP	32	SD ACMD Response Register
11230084	SD_ACMD19_TRG	32	SD ACMD19 Target Register
11230088	SD_ACMD19_STS	32	SD ACMD19 Status Register
1123008C	DMA_SA_HIGH4BIT	32	DMA Current Address Resgiter of High 4 Bits
11230090	DMA_SA	32	DMA Start Address Register
11230094	DMA_CA	32	DMA Current Address Register
11230098	DMA_CTRL	32	DMA Control Register
1123009C	DMA_CFG	32	DMA Configuration Register
112300A0	SW_DBG_SEL	32	MSDC S/W Debug Selection Register
112300A4	SW_DBG_OUT	32	MSDC S/W Debug Output Register
112300A8	DMA_LENGTH	32	DMA Length Register
112300B0	PATCH_BIT0	32	MSDC Patch Bit Register 0
112300B4	PATCH_BIT1	32	MSDC Patch Bit Register 1
112300B8	PATCH_BIT2	32	MSDC Patch Bit Register 2
112300F0	DAT_RD_DLY0	32	MSDC Data Delay Line Register 0
112300F4	DAT_RD_DLY1	32	MSDC Data Delay Line Register 1
112300F8	HW_DBG_SEL	32	MSDC H/W Debug Selection Register
11230100	MAIN_VER	32	MSDC Main Version Register

Address	Name	Width	Register Function
11230104	ECO_VER	32	MSDC ECO Version Register
11230180	EMMC50_PAD_CTL0	32	MSDC eMMC5.0 CLK PAD Control Register 0
11230184	EMMC50_PAD_DS_CTL0	32	MSDC eMMC5.0 DS PAD Control Register 0
11230188	EMMC50_PAD_DS_TUNE	32	MSDC eMMC5.0 DS Pad Tuning Register
1123018C	EMMC50_PAD_CMD_TUNE	32	MSDC eMMC5.0 CMD Pad Tuning Register
11230190	EMMC50_PAD_DAT01_TUNE	32	MSDC eMMC5.0 DAT0/1 Pad Tuning Register
11230194	EMMC50_PAD_DAT23_TUNE	32	MSDC eMMC5.0 DAT2/3 Pad Tuning Register
11230198	EMMC50_PAD_DAT45_TUNE	32	MSDC eMMC5.0 DAT4/5 Pad Tuning Register
1123019C	EMMC50_PAD_DAT67_TUNE	32	MSDC eMMC5.0 DAT6/7 Pad Tuning Register
11230204	EMMC51_CFG0	32	eMMC51 Configuration Register 0
11230208	EMMC50_CFG0	32	eMMC50 Configuration Register 0
1123020C	EMMC50_CFG1	32	eMMC50 Configuration Register 1
1123021C	EMMC50_CFG2	32	AHB2AXI Wrapper Control Register
11230220	EMMC50_CFG3	32	
11230224	EMMC50_CFG4	32	
11230228	EMMC50_BLOCK_LENGTH	32	

11230000 MSDC_CFG MSDC Configuration Register 02400099

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RAL1							CFG_START_BIT					CARD_CK_DIV			
Type	RO							RW					RW			
Reset	0	0	0	0	0	0		0	0				0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CARD_CK_DIV								CARD_CK_STABLE			CARD_CK_DRV_EN	PIO_MODE	RST	CARD_CK_PWDN	MSDC
Type	RW								RU			RW	RW	A0	RW	RW
Reset	0	0	0	0	0	0	0	0	1			1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
31:26		RAL1	
24:23		CFG_START_BIT	
19:8	CCKDIV	CARD_CK_DIV	**MS/SD card clock divider** Controls clock frequency of serial clock on MS/SD bus. Refer to "Data Line Latching Timing Diagram" and "Response Latching Timing Diagram". For non-DDR mode, msdc_ck equals SD bus clock. (Example: For SDR25 or HS, msdc_ck and SD bus clock will be 50MHz.) For DDR mode, msdc_ck denotes the MSDC internal clock which will be dobuled to SD bus clock. (Example: For DDR50, msdc_ck should be set to

Bit(s)	Mnemonic	Name	Description
			100MHz, and bus clock will be 50MHz.) 8'b00000000: msdc_ck = (1/2)*msdc_src_ck 8'b00000001: msdc_ck = [1/(4*1)]*msdc_src_ck 8'b00000010: msdc_ck = [1/(4*2)]*msdc_src_ck 8'b00000011: msdc_ck = [1/(4*3)]*msdc_src_ck 8'b00010000: msdc_ck = [1/(4*16)]*msdc_src_ck 8'b11111111: msdc_ck = [1/(4*255)]*msdc_src_ck
7	**CCKSB**	CARD_CK_STABLE	**MS/SD card clock is stable or not** After programming CARD_CK_MODE or CARD_CK_DIV, this bit will immediately become 0 and return to 1 if stable. Poll this register to ensure safety control of MSDC. 1'b0: Clock output is not stable. 1'b1: Clock output is stable.
4	**CCKDRVE**	CARD_CK_DRV_EN	**SD/MS card bus clock drive enable bit** Set this bit to 1 to enable MSDC bus clock driver. The default bus state depends on MSDC_CFG][1] CARD_CK_PWDN bit. If MSDC_CFG[1] CARD_CK_PWDN= 1, the default clock state will be free running. If MSDC_CFG[1] CARD_CK_PWDN = 0, the default clock state will be gated to 0. Set this bit to 0 to put the bus state into "tri-state". Default: 1 1'b0: Put the clock pad into tri-state 1'b1: Enable MSDC to drive clock pad; the state of CLK depends on MSDC_CFG[1] CARD_CK_PWDN.
3	**PIO**	PIO_MODE	**MS/SD PIO mode** Selects PIO mode Default: PIO mode 1'b0: DMA mode 1'b1: PIO mode
2	**RST**	RST	**Software reset** Writing 1 to this register will cause internal synchronous reset of MS/SD controller, and it will not reset register settings and DMA controller. The reset sequence is done when this bit becomes 0. SW should wait this bit to return to 0 after writing 1. 1'b0: MS/SD controller is not in reset state. 1'b1: MS/SD controller is in reset state.
1	**CCKPD**	CARD_CK_PWDN	**MSDC bus clock power-down mode** Controls card clock power-down mode. 1'b0: Clock is gated to 0 if no command or data is transmitted. 1'b1: Clock is free running even if no command or data is transmitted. (The clock may still be stopped when MSDC write data are not enough or no space for the next read data.)
0	**MSDC**	MSDC	**Selects MS/SD mode** Configures the controller as the host of memory stick or as the host of SD/MMC memory card. The default value is configuring the controller as the host of memory stick. 1'b0: Configure the controller as the host of memory stick 1'b1: Configure the controller as the host of SD/MMC memory card

11230004 MSDC_IOCON MSDC IO Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									R_D7_SMPL	R_D6_SMPL	R_D5_SMPL	R_D4_SMPL	R_D3_SMPL	R_D2_SMPL	R_D1_SMPL	R_D0_SMPL
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			W_D3_SMPL	W_D2_SMPL	W_D1_SMPL	W_D0_SMPL	W_D_SMPL_SEL	W_D_SMPL			R_D_SMPL_SEL		D_DLYLINE_SEL	R_D_SMPL	R_SMPL	SDR104_CLK_SEL
Type			RW	RW	RW	RW	RW	RW			RW		RW	RW	RW	RW
Reset			0	0	0	0	0	0			0		0	0	0	0

Bit(s)	Mnemonic	Name	Description
23	**RD7SPL**	R_D7_SMPL	**Selects read data 7 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
22	**RD6SPL**	R_D6_SMPL	**Selects read data 6 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
21	**RD5SPL**	R_D5_SMPL	**Selects read data 5 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
20	**RD4SPL**	R_D4_SMPL	**Selects read data 4 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
19	**RD3SPL**	R_D3_SMPL	**Selects read data 3 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
18	**RD2SPL**	R_D2_SMPL	**Selects read data 2 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
17	**RD1SPL**	R_D1_SMPL	**Selects read data 1 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
16	**RD0SPL**	R_D0_SMPL	**Selects read data 0 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
13	**WD3SPL**	W_D3_SMPL	**Selects SDIO interrupt sample** This bit is only valid when bit 9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
12	**WD2SPL**	W_D2_SMPL	**Selects SDIO interrupt sample** This bit is only valid when bit 9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge

Bit(s)	Mnemonic	Name	Description
			1'b1: Sample SDIO interrupt by external bus clock falling edge
11	**WD1SPL**	W_D1_SMPL	**Selects SDIO interrupt sample** This bit is only valid when bit 9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
10	**WD0SPL**	W_D0_SMPL	**Selects CRC status and SDIO interrupt sample** This bit is only valid when bit 9 is on. 1'b0: Sample CRC Status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC Status and SDIO interrupt by external bus clock falling edge
9	**WDSPLSEL**	W_D_SMPL_SEL	**Selects data line rising/falling latch fine-tuning in write transaction** 1'b0: All data line share one value indicated by MSDC_IOCON.W_D_SMPL 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.W_D0_SMPL Data line 1: MSDC_IOCON.W_D1_SMPL Data line 2: MSDC_IOCON.W_D2_SMPL Data line 3: MSDC_IOCON.W_D3_SMPL
8	**WDSPL**	W_D_SMPL	**Selects CRC status and SDIO interrupt sample** 1'b0: Sample CRC status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC status and SDIO interrupt by external bus clock falling edge
5	**RDSPLSEL**	R_D_SMPL_SEL	**Selects data line rising/falling latch fine-tuning in read transaction** 1'b0: All data line share one value indicated by MSDC_IOCON.R_D_SMPL 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.R_D0_SMPL Data line 1: MSDC_IOCON.R_D1_SMPL Data line 2: MSDC_IOCON.R_D2_SMPL Data line 3: MSDC_IOCON.R_D3_SMPL Data line 4: MSDC_IOCON.R_D4_SMPL Data line 5: MSDC_IOCON.R_D5_SMPL Data line 6: MSDC_IOCON.R_D6_SMPL Data line 7: MSDC_IOCON.R_D7_SMPL
3	**DDLSEL**	D_DLYLINE_SEL	**Selects data line delay line fine-tuning** 1'b0: All data line share one delay selection value indicated by PAD_TUNE.PAD_DAT_RD_RXDLY 1'b1: Each data line has its own delay selection value indicated by Data line 0: DAT_RD_DLY0.DAT0_RD_DLY Data line 1: DAT_RD_DLY0.DAT1_RD_DLY Data line 2: DAT_RD_DLY0.DAT2_RD_DLY Data line 3: DAT_RD_DLY0.DAT3_RD_DLY Data line 4: DAT_RD_DLY1.DAT4_RD_DLY Data line 5: DAT_RD_DLY1.DAT5_RD_DLY Data line 6: DAT_RD_DLY1.DAT6_RD_DLY Data line 7: DAT_RD_DLY1.DAT7_RD_DLY
2	**RDSPL**	R_D_SMPL	**Selects read data sample** 1'b0: Sample read data by external bus clock rising edge

Bit(s)	Mnemonic	Name	Description
			1'b1: Sample read data by external bus clock falling edge
1	**RSPL**	R_SMPL	**Selects command response sample** 1'b0: Sample response by external bus clock rising edge 1'b1: Sample response by external bus clock falling edge
0	**SDR104CKS**	SDR104_CLK_SEL	**SDR104 SCLK output clock control** Only used when MSDC_CFG[17:16] CARD_CK_MODE is 2'b01. 1'b0: Bus clock output equals inverted msdc_src_ck 1'b1: Bus clock output equals msdc_src_ck

11230008 MSDC_PS **MSDC Pin Status Register** **81FF0002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SD_WP							CMD	DAT							
Type	RU							RU	RU							
Reset	1							1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDDEBOUNCE														CDSTS	CDEN
Type	RW														RU	RW
Reset	0	0	0	0											1	0

Bit(s)	Mnemonic	Name	Description
31	**SDWP**	SD_WP	**Write Protection switch status on SD memory card** Shows the status of Write Protection switch on SD memory card. There is no default reset value. The pin WP (Write Protection) is only useful when the controller is configured for SD memory card. 1'b0: Write Protection switch on. Memory card is desired to be write-protected. 1'b1: Write Protection switch off. Memory card is writable.
24	**CMD**	CMD	**Command line status** Reflects the command line value of MSDC bus.
23:16	**DAT**	DAT	**Data line status** Reflects the data line value of MSDC bus (8-bit).
15:12	**CDDBCE**	CDDEBOUNCE	**Card detection de-bounce timer** Specifies time interval for card detection de-bounce. Default value: 0, meaning the de-bounce interval is one 32kHz cycle. The interval will extend one cycle time of 32kHz by increasing the counter by 1.
1	**CDSTS**	CDSTS	**Card detection status** 1'b1: Card detection pin status is logic high.
0	**CDEN**	CDEN	**Enables card detection** Controls card detection circuit. 1'b0: Disable card detection 1'b1: Enable card detection

1123000C MSDC_INT **MSDC Interrupt Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													DMA_PROT	GPD_CS_E	BD_CS_ER	

													ECT	RR	R	
Type													W1C	W1C	W1C	
Reset													0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SD_DATA_CRCERR	SD_DATTO	DMA_XFER_DONE	SD_XFER_COMPLETE	SD_CSTS	SD_RESP_CRCERR	SD_CMDTO	SD_CMDRDY		DMA_Q_EMPTY	SD_AUTOCMD_RESP_CRCERR	SD_AUTOCMD_CMDTO	SD_AUTOCMD_CMDRDY		MSDC_CDSC	MMC_IRQ
Type	W1C	W1C	W1C	W1C	RU	W1C	W1C	W1C		W1C	W1C	W1C	W1C		W1C	W1C
Reset	0	0	0	0	0	0	0	0		0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
19	**DMAPROTECT**	DMA_PROTECT	**There is write operation to DMA start address, length, start bit or the last buf bit.**
18	**GPDCSERR**	GPD_CS_ERR	**GPD checksum error detected**
17	**BDCSERR**	BD_CS_ERR	**BD checksum error detected**
15	**SDDCRCERR**	SD_DATA_CRCERR	**SD data CRC error interrupt** Indicates MS/SD controller detects a CRC error after reading a block of data from the DAT line or SD/MMC signals a CRC error after writing a block of data to the DAT line. 1'b0: Otherwise 1'b1: MS/SD controller detects a CRC error after reading a block of data from the DAT line or SD/MMC signals a CRC error after writing a block of data to the DAT line.
14	**SDDTO**	SD_DATTO	**SD data timeout interrupt** Indicates SD/MMC controller detects a timeout condition while waiting for data token on the DAT line. This bit is for both data read and data write. For SD data read, timeout will occur when the read data are not presented. For SD data write, timeout will occur when the write data CRC status is not presented if PATCH_BIT[30] DETECT_WR_CRC_TIMEOUT = 1. 1'b0: Otherwise 1'b1: SD/MMC controller detects a timeout condition while waiting for data token on the DAT line.
13	**DMAXFDNE**	DMA_XFER_DONE	**DMA transfer done interrupt** Indicates status of data block transfer. 1'b0: Otherwise 1'b1: A data block is successfully transferred.
12	**SDXFCPL**	SD_XFER_COMPLETE	**SD data transfer completed interrupt** Indicates transaction which contains data that are completed. While performing tuning procedure (Execute Tuning is set to 1), SD_XFER_COMPLETE is not set to 1.
11	**SDCSTS**	SD_CSTS	**SD CSTA update interrupt** Indicates any bit in register SDC_CSTA is active. The register bit will be set to 1. SW should clear SDC_CSTA, and this bit will be de-asserted automatically. 1'b0: No SD memory card interrupt 1'b1: SD memory card interrupt exists.
10	**SDRCRCER**	SD_RESP_CRCERR	**SD command CRC error interrupt** Indicates SD/MMC controller detects a CRC error after reading a response from the CMD line. 1'b0: Otherwise 1'b1: SD/MMC controller detects a CRC error after

Bit(s)	Mnemonic	Name	Description
			reading a response from the CMD line.
9	**SDCTO**	SD_CMDTO	**SD command timeout interrupt** Indicates SD/MMC controller detects a timeout condition while waiting for a response on the CMD line. 1'b0: Otherwise 1'b1: SD/MMC controller detects a timeout condition while waiting for a response on the CMD line.
8	**SDCRDY**	SD_CMDRDY	**SD command ready interrupt** For the command without response, the register bit will be 1 once the command is completed on SD/MMC bus. For command with response without busy, the register bit will be 1 whenever the command is issued onto SD/MMC bus and its corresponding response is received without CRC error. For command with response with busy in DAT0, the register bit will be 1 whenever the command is issued onto SD/MMC bus and its corresponding response is received without CRC error and the DAT0 transited from busy to idle. 1'b0: Otherwise 1'b1: Command finished successfully without a CRC error
6	**DMAQEPTY**	DMA_Q_EMPTY	**DMA queue empty interrupt** Indicates the current DMA queue is empty. Only for descriptor mode and enhance mode.
5	**SDACDRCRCER**	SD_AUTOCMD_RESP_CRCERR	**SD auto command CRC error interrupt** Set when detecting a CRC error in the auto command response.
4	**SDACDCTO**	SD_AUTOCMD_CMDTO	**SD auto command timeout interrupt** Set if no response is returned within a specified cycles (64T in spec) from the end bit of auto command.
3	**SDACDCRDY**	SD_AUTOCMD_CMDRDY	**SD auto command ready interrupt** Set if auto command is executed without CRC error or timeout.
1	**MSDCCDSC**	MSDC_CDSC	**MSDC card detection status change interrupt** Indicates if any interrupt for memory card insertion/removal exists. Whenever memory card is inserted or removed and card detection circuit is enabled, i.e. register bit CDEN in register MSDC_PS is set to 1, the register bit will be set to 1. It will be reset when the register is read. 1'b0: Otherwise 1'b1: Card is inserted or removed.
0	**MMCIRQ**	MMC_IRQ	**MMC card interrupt** 1'b0: Otherwise 1'b1: MMC card interrupt event occurs.

11230010 MSDC_INTEN MSDC Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													EN_DMA_PROTECT	EN_GPD_CS_ERR	EN_BD_CS_ERR	
Type													RW	RW	RW	
Reset													0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	EN_SD_DATA_CRCERR	EN_SD_DATTO	EN_SD_DMA_XFER_DONE	EN_SD_XFER_COMPL ETE	EN_SD_CSTA	EN_SD_RESP_CRCERR	EN_SD_CMDTO	EN_SD_CMDRDY	EN_SD_SDIOIRQ	EN_DMA_Q_EMPTY	EN_SD_AUTOCMD_RESP_CRCERR	EN_SD_AUTOCMD_CMDTO	EN_AUTOCMD_CMDRDY		EN_MSDC_CDSC	EN_MMC_IRQ
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
19	**ENDMAPROTECT**	EN_DMA_PROTECT	**Enables DMA protection interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
18	**ENGPDCSERR**	EN_GPD_CS_ERR	**Enables GPD checksum error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
17	**ENBDCSERR**	EN_BD_CS_ERR	**Enables BD checksum error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
15	**ENSDDCRCERR**	EN_SD_DATA_CRC ERR	**Enables SD data CRC error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
14	**ENSDDTO**	EN_SD_DATTO	**Enables SD data timeout interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
13	**ENDMAXFDNE**	EN_SD_DMA_XFER _DONE	**Enables DMA transfer done interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
12	**ENSDXFCPL**	EN_SD_XFER_COM PLETE	**Enables SD data transfer completed interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
11	**ENSDCSTA**	EN_SD_CSTA	**Enables SD CSTA update interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
10	**ENSDRCRCER**	EN_SD_RESP_CRC ERR	**Enables SD command CRC error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
9	**ENSDCTO**	EN_SD_CMDTO	**Enables SD command timeout interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
8	**ENSDCRDY**	EN_SD_CMDRDY	**Enables SD command ready interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
7	**ENSDIOIRQ**	EN_SD_SDIOIRQ	**Enables SD SDIO interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
6	**ENDMAQEPTY**	EN_DMA_Q_EMPTY	**Enables DMA queue empty interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
5	**ENSDACDRCRCER**	EN_SD_AUTOCMD_ RESP_CRCERR	**Enables SD auto command CRC error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
4	**ENSDACDCTO**	EN_SD_AUTOCMD_ CMDTO	**Enables SD auto command timeout interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt

Bit(s)	Mnemonic	Name	Description
3	**ENSDACDCRDY**	EN_AUTOCMD_CMDRDY	**Enables SD auto command ready interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
1	**ENMSDCCDSC**	EN_MSDC_CDSC	**Enables MSDC card detection status change interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
0	**ENMMCIRQ**	EN_MMC_IRQ	**Enables MMC card interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt

11230014 MSDC_FIFOCS **MSDC FIFO Control and Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFOCLR								TXFIFOCNT							
Type	A0								RU							
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RXFIFOCNT							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**FIFOCLR**	FIFOCLR	**Clears embedded FIFO** Write 1 to this bit to clear FIFO. It will become 0 when FIFO is cleared. SW needs to check this bit to make sure clearing FIFO sequence is done. This bit can be used when the data read/write sequence has error and needs to clear HW FIFO.
23:16	**TXFIFOCNT**	TXFIFOCNT	**TX FIFO count for MSDC write** 8'd0: No data in FIFO 8'd1: 1-byte data in FIFO 8'd2: 2-byte data in FIFO 8'd131: Max. 131-byte data in FIFO Others: Reserved
7:0	**RXFIFOCNT**	RXFIFOCNT	**RX FIFO count for MSDC read** 8'd0: No data in FIFO 8'd1: 1-byte data in FIFO 8'd2: 2-byte data in FIFO 8'd131: Max. 131-byte data in FIFO Others: Reserved

11230018 MSDC_TXDATA **MSDC TX Data Port Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PIO_TXDATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	PIO_TXDATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PIOTXDATA**	PIO_TXDATA	**PIO mode TXDATA port** This register can be accessed by byte, half-word or word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

1123001C MSDC_RXDATA MSDC RX Data Port Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PIO_RXDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIO_RXDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PIORXDATA**	PIO_RXDATA	**PIO mode RXDATA port** This register can be accessed by byte, half-word or word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

11230030 SDC_CFG SD Configuration Register 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DTOC										INT_AT_BLOCK_GAP	SDIO_INT_DET_EN	SDIO		BUSW IDTH	
Type	RW										RW	RW	RW		RW	
Reset	0	0	0	0	0	0	0	0			0	1	0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															WAKEUP_INS_EN	WAKEUP_SDIOINT_EN
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DTOC**	DTOC	**Data timeout counter** The period from the end of the initial host read command or the last read data block in a multiple block read operation to the start bit of the next read data block requires at least two serial clock cycles. The counter is used to extend the period (Read Data Access Time) in unit of 1,048,576 serial clocks.

Bit(s)	Mnemonic	Name	Description
			8'b00000000: Extend 1,048,576 more serial clock cycles 8'b00000001: Extend 1,048,576*2 more serial clock cycles 8'b00000010: Extend 1,048,576*3 more serial clock cycles 8'b11111111: Extend 1,048,576*256 more serial clock cycles
21	**INTBGP**	INT_AT_BLOCK_G AP	**Interrupt at block gap** This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Set to 1 to enable interrupt detection at the block gap for a multiple block transfer. Set to 0 to disable interrupt detection during a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the host driver detects an SD card insertion, it will set up this bit according to the CCCR of the SDIO card. 1'b0: Disable interrupt detection at block gap 1'b1: Enable interrupt detection at block gap
20	**SDIOIDE**	SDIO_INT_DET_E N	**Enables SDIO interrupt detection** Informs SD controller to sense the SDIO interrupt. 1'b0: Disable SDIO interrupt detection 1'b1: Enable SDIO interrupt detection if the SDIO bit is also on
19	**SDIO**	SDIO	**SDIO mode enable bit** Enables support to sense the SDIO interrupt and disables R4 response CRC check for SDIO card. 1'b0: Disable SDIO mode 1'b1: Enable SDIO mode
17:16	**BUSWD**	BUSWIDTH	**Configures bus width** Defines SD/MMC bus width. 2'b00: 1 bit mode 2'b01: 4 bit mode 2'b10: 8 bit mode 2'b11: Reserved
1	**ENWKUPINS**	WAKEUP_INS_EN	**Card status change wakeup event enable bit** 1'b0: Disable wakeup event for card status change 1'b1: Enable wakeup event for card status change
0	**ENWKUPSDIOINT**	WAKEUP_SDIOINT _EN	**SDIO card interrupt wakeup event enable bit** 1'b0: Disable wakeup event for SDIO card interrupt 1'b1: Enable wakeup event for SDIO card interrupt

11230034 SDC_CMD **SD Command Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VOL_SWTH1				LEN											
Type	RO				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GO_IRQ	STOP	RW	DTYPE		RSPTYP1	RSPTYP			BREAK	CMD					
Type	RW	RW	RW	RW		RO	RW			RW	RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		VOL_SWTH1	
27:16	**LEN**	LEN	**Length** Defines the length of one block (unit: byte) in a data transaction of block mode or the data length (unit: byte) in data transaction of byte mode. The maximal value of block length is 2,048 bytes. 12'b000000000000: Reserved 12'b000000000001: Block length is 1 byte 12'b000000000010: Block length is 2 bytes. 12'b011111111111: Block length is 2047 bytes. 12'b100000000000: Block length is 2048 bytes.
15	**GOIRQ**	GO_IRQ	**GO_IRQ command** Indicates if the command is GO_IRQ_STATE (CMD40) and used only for MMC protocol. If the command is GO_IRQ_STATE, the period between command token and response token will not be limited. 1'b0: The command is not GO_IRQ_STATE. 1'b1: The command is GO_IRQ_STATE.
14	**STOP**	STOP	**Stop command** Indicates if the command is a stop transmission command. It should be set to 1 when CMD12 (SD/MMC) or CMD52 with I/O abort (SDIO) is to be issued. 1'b0: The command is not a stop transmission command. 1'b1: The command is a stop transmission command.
13	**RW**	RW	**Selects command read write** Defines the command is a read command or write command. The register bit is valid only when the command causes a transaction with data token. 1'b0: The command is a read command. 1'b1: The command is a write command.
12:11	**DTYPE**	DTYPE	**Selects data block** Defines data token type for the command. 2'b00: No data token for the command 2'b01: Single block transaction (only available in block mode) 2'b10: Multiple block transaction (only available in block mode) 2'b11: Stream operation. Should only be used in MMC protocol (only available in block mode).
10		RSPTYP1	
9:7	**RSPTYP**	RSPTYP	**Command response type** 3'b000: This command has no response. 3'b001: The command has R1/R5/R6/R7 response. The response token is 48-bit with CRC check (for SD/MMC/SDIO)(excluding SDIO abort command) 3'b010: The command has R2 response. The response token is 136-bit (for SD/MMC). 3'b011: The command has R3 response. The response token is 48-bit response, no CRC check (for SD/MMC). 3'b100: The command has R4 response. The response token is 48-bit without CRC check (for SDIO); the response token is 48-bit with CRC check (for MMC). 3'b111: The command has R1b response. The response token is 48-bit (for SD/MMC/SDIO).
6	**BREAK**	BREAK	**Aborts pending MMC GO_IRQ command** Only valid for a pending GO_IRQ_MODE command waiting for MMC interrupt response. 1'b0: Not a beak command

Bit(s)	Mnemonic	Name	Description
			1'b1: Break a pending MMC GO_IRQ_MODE command in the controller
5:0	**CMD**	CMD	**SD memory card command**

11230038 SDC_ARG **SD Argument Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ARG**	ARG	Memory card controller argument register

1123003C SDC_STS **SD Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMC_STREAM_WR_COMPL															CMD_WR_BUSY
Type	RU															W1C
Reset	0															0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CMDBUSY	SDCBUSY
Type															RU	RU
Reset															0	0

Bit(s)	Mnemonic	Name	Description
31	**MMCSWRCPL**	MMC_STREAM_WR_COMPL	**MMC stream mode write data are all flushed to MMC card** SW can use this bit to confirm the last write data are flushed to MMC then issue STOP command. This bit is only valid when the command SDC_CMD.DTYPE=2'b11. 1'b0: Last data are partially inside MSDC. 1'b1: Flush last data to MMC card
16		CMD_WR_BUSY	
1	**CMDBSY**	CMDBUSY	**SD command line busy status** SW should always read this bit to make sure the command line is not busy before sending the next command. If the command is R1B or data read/write command, SW should check the SDCBUSY bit too. Note: When auto command 12 is enabled, this bit will be asserted immediately after SDC_CMD is written and de-asserted after auto-command 12 is finished. 1'b0: No transmission is going on CMD line on SD bus.

Bit(s)	Mnemonic	Name	Description
0	**SDCBSY**	SDCBUSY	1'b1: There is transmission going on CMD line on SD bus. **SD controller busy status** 1'b0: SD controller is idle. 1'b1: SD controller is busy.

11230040 SDC_RESP0 SD Response Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP0**	RESP0	Memory card controller response register 0

11230044 SDC_RESP1 SD Response Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP1**	RESP1	Memory card controller response register 1

11230048 SDC_RESP2 SD Response Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP2**	RESP2	Memory card controller response register 2

1123004C SDC_RESP3 SD Response Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP3**	RESP3	Memory card controller response register 3

11230050 SDC_BLK_NUM SD Block Number Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BLOCK_NUMBER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLOCK_NUMBER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:0	**BLKNUM**	BLOCK_NUMBER	**Memory card controller block number** Indicates block number of data transaction. 32'd0: Reserved 32'd1: 1 data block 32'd2: 2 data block 32'd3: 3 data block 32'hffffffff: 4GB-1 data block

11230054 SDC_VOL_CHG SD Voltage Change Wait Time Register 00000145

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11230058 SDC_CSTS SD Card Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CSTS**	CSTS	**CSTS** The card status field in the response R1 or R1b field. Each bit can be written 1 to clear individually.

1123005C SDC_CSTS_EN SD Card Status Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTS_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CSTS_EN**	CSTS_EN	**CSTS_EN** Controls which bit of CSTA will generate MSDC_INT.SDCSTA.

11230060 SDC_DATCRC_STS SD Card Data CRC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DAT_CRCSTS_POS							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**DCSSP**	DAT_CRCSTS_POS	**MSDC read DATA CRC status** Reflects CRC status of data line[7:0]. Only for MSDC read. 1'b0: No CRC error 1'b1: CRC error

11230070 EMMC_CFG0 EMMC Configuration Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11230074 EMMC_CFG1 EMMC Configuration Register 1 00200003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11230078 EMMC_STS EMMC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1123007C EMMC_IOCON EMMC IO Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11230080 SD_ACMD_RESP SD ACMD Response Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AUTOCMD_RESP															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOCMD_RESP															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ACMDRESP**	AUTOCMD_RESP	**SD auto command response register** Stores the response[39:8] of ACMD12/ACMD23/ACMD19.

11230084 SD_ACMD19_TRG SD ACMD19 Target Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11230088 SD_ACMD19_STS SD ACMD19 Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1123008C DMA_SA_HIGH4BIT **DMA Current Address Resgiter of High 4 Bits** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMA_SURR_ADDR_HIGH4BIT			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DMASAHIGH4BIT**	DMA_SURR_ADDR_HIGH4BIT	Sets up high 4-bit address of start address because 64G DRAM needs 36-bit address

11230090 DMA_SA **DMA Start Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_STR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_STR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DMASA**	DMA_STR_ADDR	**Start address of the DMA address** Sets up the start address of the DMA. In DMA basic mode, this field indicates the source or destination address of the data transfer which depends on the command. In descriptor base DMA, this is the descriptor chain start address.

11230094 DMA_CA **DMA Current Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_CURR_ADDR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_CURR_ADDR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DMACA**	DMA_CURR_ADDR	**Current address of the DMA address** Reads the current address of the DMA descriptor chain.

11230098 DMA_CTRL **DMA Control Register** **00006008**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		BURST_SIZE			DMA_SPLIT_1K	LAST_BUF	DMA_ALIGN	DMA_MODE					AHB_READYM	DMA_RESUME	DMA_STOP	DMA_START
Type		RW			RW	RW	RW	RW					RO	WO	Ao	WO
Reset		1	1	0	0	0	0	0					1	0	0	0

Bit(s)	Mnemonic	Name	Description
14:12	**BSTSZ**	BURST_SIZE	**DMA burst size** Specifies the maximum transfer bytes allowed at the device per DMA burst. This field cannot be modified when the DMA status is 1. 3'd3: 8 bytes 3'd4: 16 bytes 3'd5: 32 bytes 3'd6: 64 bytes Other: Reserved
11	**SPLIT1K**	DMA_SPLIT_1K	**Specifies split burst when crossing 1K boundry address** 1'b0: 1K boundary is not split. 1'b1: 1K boundary is split.
10	**LASTBF**	LAST_BUF	**Last buffer of the basic DMA mode** Indicates the last buffer in the basic DMA mode.
9	**DMAALIGN**	DMA_ALIGN	**Specifies address aligment burst size** 1'b0: Not DAM burst size alignment 1'b1: DAM burst size alignment
8	**DMAMOD**	DMA_MODE	**DMA operation mode** Indicates operation mode of DMA. 1'b0: Basic DMA mode 1'b1: Descriptor base DMA mode
3	**READYM**	AHB_READYM	**Only for debugging when DMA hangs** SW checks if AHB bus is ok when GDMA hangs.
2	**DMARSM**	DMA_RESUME	**DMA resume control register** Resumes DMA transaction. Read always returns 0.
1	**DMASTOP**	DMA_STOP	**DMA stop control register** Stops DMA transaction. When SW issues STOP command, SW must wait for this bit to be de-asserted or DMA inactive to guarantee stop is done.
0	**DMASTART**	DMA_START	**DMA start control register** Starts DMA transaction. Read always returns 0.

1123009C DMA_CFG **DMA Configuration Register** **00000004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																DMA_CHK_SUM_12B
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name			MSDC _ACTIVE_ EN				AHB_ HPROT_2_ EN							LOCK_DISABLE	DMA_DSCP_CS_EN	DMA_STATUS
Type			RW				RW							RW	RW	RU
Reset			0	0			0	0						1	0	0

Bit(s)	Mnemonic	Name	Description
16	**DMACHKSUM12B**	DMA_CHK_SUM_12 B	**Indicates GPD/BD checksum covers 16 bytes or 12 bytes** 1'b0: GPD/BD checksum covers 16 bytes. 1'b1: GPD/BD checksum only covers 12 bytes.
13:12	**MSDCACTIVEEN**	MSDC_ACTIVE_EN	**Indicates how to control msdc_active** 2'b00: Dynamic control msdc_active 2'b01: msdc_active = 0 2'b10: msdc_active = 1 2'b11: Reserved
9:8	**AHBHPROT2EN**	AHB_HPROT_2_EN	**Determines how to control hprot_2 pin of AHB bus** AHB_HPROT_2_EN = 2'b00 and basic DMA mode All the write transfers of a burst will be accessed by bufferable mode except for the last burst of DMA. AHB_HPROT2_2_EN=2'b00 and descriptor DMA mode All the write transfers of a burst will be accessed by bufferable mode except for HW own update transfer. 2'b00: Dynamic control hprot_2 2'b01: hprot_2 = 0 2'b10: hprot_2 = 1
2	**LOCKDISABLE**	LOCK_DISABLE	**Disables lock to improve EMI efficiency** 1'b0: Enable AHB lock 1'b1: Disable AHB lock
1	**DSCPCSEN**	DMA_DSCP_CS_EN	**Enables DMA descriptor checksum** This bit is used to enable or disable the descriptor checksum validation function for the descriptor. This field cannot be modified when the DMA status is 1.
0	**DMASTS**	DMA_STATUS	**DMA status** Indicates the status of DMA. 1'b0: DMA engine is inactive. 1'b1: DMA engine is active.

112300A0 SW_DBG_SEL MSDC S/W Debug Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_SEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**SWDBGSEL**	DBG_SEL	**Selects MSDC debugging** Reserved.

Bit(s)	Mnemonic	Name	Description

112300A4 SW_DBG_OUT **MSDC S/W Debug Output Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SWDBGO**	DBG_OUT	**MSDC debug output** 32-bit output selected by SW_DBG_SEL register

112300A8 DMA_LENGTH **DMA Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	XFER_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XFER_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**XFSZ**	XFER_SIZE	**DMA total transfer size** Specifies the number of DMA transfer byte required for the movement of source data through DMA. This field is only valid in basic DMA mode.

112300B0 PATCH_BIT0 **MSDC Patch Bit Register 0** **403C000F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_MMC_DRV_RESP	DETECT_WR_CRC_TIMEOUT	SPC_ALWAYS_PUSH	SDIO_INT_DLY_SEL	SDC_CMD_CMDFAIL_SEL	SDC_CMD_IDRT_SEL	SDC_CFG_WDOD				SDC_CFG_BSYDLY				SDIO_CFG_INTC_SEL	MSDC_BLKNUM_SEL
Type	RW	RW	RW	RW	RW	RW	RW				RW				RW	RW
Reset	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC_FIFO_RD_DIS						INT_DAT_LATCH_CK_SEL				DESC_UP_SEL1			DIS_REFLECT_CMDWR_WHEN_BSY	EN_SDC_OD_8BIT_SUP	

Type	RW						RW				RW			RW	RW	
Reset	0						0	0	0		0	0		1	1	1

Bit(s)	Mnemonic	Name	Description
31	**PTCH31**	EN_MMC_DRV_RES P	**Enables MSDC always drives bus when outputting wake-up response (BREAK)** 1'b0: Disable 1'b1: Enable
30	**PTCH30**	DETECT_WR_CRC_ TIMEOUT	**Detects MSDC write data CRC phase timeout** 1'b0: Does not detect CRC phase timeout 1'b1: Detect CRC phase timeout
29	**PTCH29**	SPC_ALWAYS_PUS H	**SPC buffer push mechanism** 1'b0: Push the buffer only when read transfer is on-going 1'b1: Always push the buffer
28	**PTCH28**	SDIO_INT_DLY_S EL	**Selects SDIO interrupt latch time** 1'b0: Latch the data line value in internal SDIO interrupt period 1'b1: Latch the data line value in 1 clock delay of internal SDIO interrupt period
27	**PTCH27**	SDC_CMD_CMDFAI L_SEL	**Selects SDIO interrupt period recovery** 1'b0: SDIO interrupt period will re-start after a CMD12 or CMD52 command is issued. 1'b1: SDIO interrupt period whenever DAT line is not busy.
26	**PTCH26**	SDC_CMD_IDRT_S EL	**Selects SD identification response time** The register bit indicates if the command has a response with NID (i.e. 5 serial clock cycles as defined in SD memory card Specification Part 1 Physical Layer Specification version 1.0) response time. The register bit is valid only when the command has a response token. Thus, the register bit must be set to 1 for CMD2 (ALL_SEND_CID) and ACMD41 (SD_APP_OP_CMD). 1'b0: Otherwise 1'b1: The command has a response with NID response time.
25:22	**PTCH22**	SDC_CFG_WDOD	**SD write data output delay** The period from finish of the response for the initial host write command or the last write data block in a multiple block write operation to the start bit of the next write data block requires at least two serial clock cycles. The register field is used to extend the period (Write Data Output Delay) in unit of one serial clock. 4'b0000: No extension 4'b0001: Extend 1 more serial clock cycle 4'b0010: Extend 2 more serial clock cycles 4'b1111: Extend 15 more serial clock cycles
21:18	**PTCH18**	SDC_CFG_BSYDLY	**SD R1B busy detection mode** The register field is only valid for the commands with R1b response. If the command has a response of R1b type, MS/SD controller must monitor the data line 0 for card busy status from the bit time that is two serial clock cycles after the command end bit to check if operations in SD/MMC Memory Card have finished. The register field is used to expand the time between the command end bit and end of detection period to detect card busy status. If time is up and there is no card busy status on data line 0, then the controller will abandon the detection. 4'b0000: No extension

Bit(s)	Mnemonic	Name	Description
			4'b0001: Extend 1 more serial clock cycle 4'b0010: Extend 2 more serial clock cycles 4'b1111: Extend 15 more serial clock cycles
17	**PTCH17**	SDIO_CFG_INTC_ SEL	**Selects SDIO interrupt mode** 1'b0: Only when data line [1] = 0 and then trigger SDIO interurpt event 1'b1: Only when data line [3:0] = 4'b1101 and then trigger SDIO interurpt event
16	**PTCH16**	MSDC_BLKNUM_SE L	**Supports ACMD23 reliable/force prog feature** 1'b0: Support ACMD23 reliable/force prog feature 1'b1: Does not support ACMD23 reliable/force prog feature
15	**PTCH15**	MSDC_FIFO_RD_D IS	**Disables MSDC RXFIFO read** 1'b0: Disable FIFO read permission to RXFIFO in PIO mode 1'b1: Enable FIFO read permission to RXFIFO in PIO mode
9:7	**INTCKS**	INT_DAT_LATCH_ CK_SEL	**Selects internal MSDC clock phase** Total 8 stages, each stage can delay 1 clock period of msdc_src_ck.
5:4		DESC_UP_SEL1	
2	**PTCH02**	DIS_REFLECT_CM DWR_WHEN_BSY	**Enables SD command register write monitor** 1'b0: Enable monitor function 1'b1: Disable monitor function
1:0	**PTCH01**	EN_SDC_ODD_8BI T_SUP	**Enables SD odd number support for 8-bit data bus** 1'b0: Disable 1'b1: Enable

112300B4 PATCH_BIT1 MSDC Patch Bit Register 1 FFFE0009

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MSDC_CK_SHBFF_CK EN	MSDC_CK_RCTL_CKEN	MSDC_CK_WCTL_CKEN	MSDC_CK_SD_CKEN	MSDC_CK_ACMD_CKEN	MSDC_CK_VOLDET_CKEN	MSDC_CK_PSC_CKEN	MSDC_CK_SPC_CKEN	AHB_CK_GDMA_CKEN							ENABLE_SINGLE_BURST
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW							RW
Reset	1	1	1	1	1	1	1	1	1							0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESET_GDMA	RALo	BIAS_EXTBIAS_28NM	BIAS_EN18IO_28NM	BIAS_TUNE_28NM				GET_CRC_MARG IN	GET_BUSY_MARG IN	CMD_RSP_TA_CN TR			WRDAT_CRCS_TA _CNTR		
Type	RW	RW	RW	RW	RW				RW	RW	RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
31	**MSHBFCKEN**	MSDC_CK_SHBFF_ CKEN	**msdc_src_ck clock enable bit for SHBFF** 1'b0: Disable 1'b1: Enable
30	**MRCTLCKEN**	MSDC_CK_RCTL_C KEN	**msdc_src_ck clock enable bit for RCTL** 1'b0: Disable 1'b1: Enable

Bit(s)	Mnemonic	Name	Description
29	**MWCTLCKEN**	MSDC_CK_WCTL_CKEN	**msdc_src_ck clock enable bit for WCTL** 1'b0: Disable 1'b1: Enable
28	**MSDCKEN**	MSDC_CK_SD_CKE N	**msdc_src_ck clock enable bit for SD** 1'b0: Disable 1'b1: Enable
27	**MACMDCKEN**	MSDC_CK_ACMD_CKEN	**msdc_src_ck clock enable bit for ACMD** 1'b0: Disable 1'b1: Enable
26	**MVOLDTCKEN**	MSDC_CK_VOLDET_CKEN	**msdc_src_ck clock enable bit for VOLDET** 1'b0: Disable 1'b1: Enable
25	**MPSCCKEN**	MSDC_CK_PSC_CKEN	**msdc_src_ck clock enable bit for PSC** 1'b0: Disable 1'b1: Enable
24	**MSPCCKEN**	MSDC_CK_SPC_CKEN	**msdc_src_ck clock enable bit forSPC** 1'b0: Disable 1'b1: Enable
23	**HGDMACKEN**	AHB_CK_GDMA_CKEN	**hclk_ck clock enable bit for GDMA** 1'b0: Disable 1'b1: Enable
16	**SINGLEBURST**	ENABLE_SINGLE_BURST	**AHB bus will not support incr1 burst type in the future. This will only affect AHB bus MSDC design, not AXI bus design.** 1'b0: HW will send incr1 burst type. 1'b1: HW will send single burst type instead of incr1 type.
15	**RESETGDMA**	RESET_GDMA	**SW can reset GDMA when design hangs.** 1'b1: Reset GDMA 1'b0: Does not reset GDMA
14		RAL0	
13	**BIAS28R0**	BIAS_EXTBIAS_28NM	**28NM BIAS controller register 0**
12	**BIAS28R1**	BIAS_EN18IO_28 NM	**28NM BIAS controller register 1**
11:8	**BIAS28R2**	BIAS_TUNE_28NM	**28NM BIAS controller register 2**
7	**GETCRCMARGIN**	GET_CRC_MARGIN	**Adds margin to get CRC status when card resp CRC does not match spec 2 cycle from endbit** 1'b0: 8 cycles reserved to get CRC status from write data CRC endbit 1'b1: 16 cycles reserved to get CRC status from write data CRC endbit
6	**GETBUSYMARGIN**	GET_BUSY_MARGI N	**Adds margin to get busy state of data0** 1'b0: 1 cycle reserved to get busy state from SRC status endbit 1'b1: 3 cycles reserved to get busy state from SRC status endbit
5:3	**CMDTA**	CMD_RSP_TA_CNT R	**CMD response turn around period** Turn around cycle = CMD_RSP_TA_CNTR + 2 In USH104 mode, this register should be set to 1. In non-UHS104 mode, this register should be set to 0.
2:0	**WRTA**	WRDAT_CRCS_TA_CNTR	**Write data and CRC status turn around period** Turn around cycle = WRDAT_CRCS_TA_CNTR + 2 In USH104 mode, this register should be set to 1. In non-UHS104 mode,this register should be set to 0.

112300B8 PATCH_BIT2 MSDC Patch Bit Register 2 14801803

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	CRCS TS_L ATCH _EN_ SEL			CFG_ CRCS TS	CFG_CRCST S_CNT		CFG_ CRCS TS_E DGE	CFG_ CRCS TS_S EL	POP_EN_CNT					RESP_LATCH_EN _SEL		
Type	RW			RW	RW		RW	RW	RW					RW		
Reset	0	0	0	1	0	1	0	0	1	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG_ RESP	CFG_RESP_CNT			INTC _RES P_SE L		CFG_ RDAT	CFG_RDAT_CNT					RESP_WAIT _CNT		SUPP ORT_ 64G	ENHA NCE_ WAIT _GPD
Type	RW	RW			RW		RW	RW					RW		RW	RW
Reset	0	0	0	1	1		0	0	0	0	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:29	**CRCSTSENSEL**	CRCSTS_LATCH_E N_SEL	**Configures latch CRC status enable signal for async FIFO in eMMC45** 3'b000: Latch CRC status enable signal does not delay. 3'b001: Latch CRC status enable signal delays 1T msdc_ck. 3'b010: Latch CRC status enable signal delays 2T msdc_ck. 3'b011: Latch CRC status enable signal delays 3T msdc_ck. 3'b111: Latch CRC status enable signal delays 7T msdc_ck.
28	**CFGCRCSTS**	CFG_CRCSTS	**Configures CRC status path selection** This setting only uses eMMC4.5 feature. 1'b0: Latch CRC status select delay-line path 1'b1: Latch CRC status select async FIFO path
27:26	**CFGCRCSTSCNT**	CFG_CRCSTS_CNT	**Configures the number of data pushed in async FIFO until starting to pop out data from async FIFO** Min. setting: 1. Do not set it to 0. This setting only uses eMMC4.5 feature. 2'b00: Push 0 data in async FIFO when starting to pop out data from async FIFO 2'b01: Push 1 data in async FIFO when starting to pop out data from async FIFO 2'b10: Push 2 data in async FIFO when starting to pop out data from async FIFO 2'b11: Push 3 data in async FIFO when starting to pop out data from async FIFO
25	**CFGCRCSTSEDGE**	CFG_CRCSTS_EDG E	**Configures to use rising async FIFO or falling async FIFO** 1'b0: Async FIFO latch CRC status uses rising async FIFO. 1'b1: Async FIFO latch CRC status uses falling async FIFO.
24		CFG_CRCSTS_SEL	**Configures async FIFO path selection** 1'b0: Use normal path in async FIFO 1'b1: Use 2DFF path in async FIFO
23:20	**POPENCNT**	POP_EN_CNT	**Pop enable counter** Defines how many write pointer and the read pointer margins begin to pop data transfer
18:16	**RESPSTSENSEL**	RESP_LATCH_EN_ SEL	**Configures latch CMD response enable signal for async FIFO in eMMC45** 3'b000: Latch CMD response enable signal does not delay. 3'b001: Latch CMD response enable signal delays 1T

Bit(s)	Mnemonic	Name	Description
			msdc_ck. 3'b010: Latch CMD response enable signal delays 2T msdc_ck. 3'b011: Latch CMD response enable signal delays 3T msdc_ck. 3'b111: Latch CMD response enable signal delays 7T msdc_ck.
15	**CFGRESP**	CFG_RESP	**Configures CMD response path selection** This setting only uses eMMC4.5 feature. 1'b0: Latch CMD response select async FIFO path 1'b1: Latch CMD response select delay-line path
14:12	**CFGRESPCNT**	CFG_RESP_CNT	**Configures the number of data pushed in async FIFO until starting to pop out data from async FIFO** Min. setting: 1. Do not set it to 0. This setting only uses eMMC4.5 feature. 3'b000: Push 0 data in async FIFO when starting to pop out data from async FIFO 3'b001: Push 1 data in async FIFO when starting to pop out data from async FIFO 3'b111: Push 7 data in async FIFO when starting to pop out data from async FIFO
11	**INTCRESPSEL**	INTC_RESP_SEL	**Configures BREAK command async FIFO path** 1'b0: Use normal path in async FIFO 1'b1: Use 2DFF path in async FIFO
9	**CFGRDAT**	CFG_RDAT	**Configures read data path** 1'b0: Read data path bypasses delay line 1'b1: Read data path through delay line
8:4	**CFGRDATCNT**	CFG_RDAT_CNT	**Configures read data path delay line**
3:2	**RESPWAITCNT**	RESP_WAIT_CNT	**Configures CMD response timeout** Timeout cycle = 65T + 16*RESP_WAIT_CNT 2'b00: CMD response timeout is 65T. 2'b01: CMD response timeout is 65T+16*1T. 2'b01: CMD response timeout is 65T+16*2T. 2'b01: CMD response timeout is 65T+16*3T.
1	**SUPPORT64G**	SUPPORT_64G	**Supports high 64G DRAM space access or not** 1'b1: Support 64G DRAM access 1'b0: Does not support 64G DRAM access
0	**ENHANCEGPD**	ENHANCE_WAIT_GPD	**If SW clears int when GPD update is not finished, design will hang.** Set this bit to 1 to avoid this issue in enhance write mode. 1'b1: Use new HW code for updating GPD in enhance mode 1'b0: Use old HW code

112300F0 DAT_RD_DLY MSDC Data Delay Line Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT0_RD_DLY								DAT1_RD_DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT2_RD_DLY								DAT3_RD_DLY				
Type				RW								RW				

Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT0RDDLY**	DAT0_RD_DLY	**Controls DAT0 pad RX delay line (for MSDC RD)** Total 32 stages.
20:16	**DAT1RDDLY**	DAT1_RD_DLY	**Controls DAT1 pad RX delay line (for MSDC RD)** Total 32 stages.
12:8	**DAT2RDDLY**	DAT2_RD_DLY	**Controls DAT2 pad RX delay line (for MSDC RD)** Total 32 stages.
4:0	**DAT3RDDLY**	DAT3_RD_DLY	**Controls DAT3 pad RX delay line (for MSDC RD)** Total 32 stages.

112300F4 DAT_RD_DLY1 **MSDC Data Delay Line Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT4_RD_DLY										RAL0	DAT5_RD_DLY				
Type	RO										RW	RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RAL1		RAL2	DAT6_RD_DLY					DAT7_RD_DLY							
Type	RO		RW	RW					RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:22	**DAT4RDDLY**	DAT4_RD_DLY	**Controls DAT4 pad RX delay line (for MSDC RD)** Total 32 stages.
21		RAL0	
20:16	**DAT5RDDLY**	DAT5_RD_DLY	**Controls DAT5 pad RX delay line (for MSDC RD)** Total 32 stages.
15:14		RAL1	
13		RAL2	
12:8	**DAT6RDDLY**	DAT6_RD_DLY	**Controls DAT6 pad RX delay line (for MSDC RD)** Total 32 stages.
7:0	**DAT7RDDLY**	DAT7_RD_DLY	**Controls DAT7 pad RX delay line (for MSDC RD)** Total 32 stages.

112300F8 HW_DBG_SEL **MSDC H/W Debug Selection Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RAL0			HW_DBG3_SEL					RAL1			HW_DBG2_SEL				
Type	RO			RW					RO			RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RAL2			HW_DBG1_SEL					RAL3			HW_DBG0_SEL				
Type	RO			RW					RO			RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:29	**DBGWSEL**	RAL0	**Selects HW debug output for wrapper** 0: Original debug pins 1: Wrapper debug pins
28:24 23:21	**DBG3SEL**	HW_DBG3_SEL RAL1	**Selects HW debug output**
20:16 15:13	**DBG2SEL**	HW_DBG2_SEL RAL2	**Selects HW debug output**
12:8 7:5	**DBG1SEL**	HW_DBG1_SEL RAL3	**Selects HW debug output**
4:0	**DBG0SEL**	HW_DBG0_SEL	**Selects HW debug output**

11230100 MAIN_VER MSDC Main Version Register 20140512

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAIN_VER															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAIN_VER															
Type	RO															
Reset	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
31:0	**MAINVER**	MAIN_VER	Main version

11230104 ECO_VER MSDC ECO Version Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ECO_VER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ECO_VER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ECOVER**	ECO_VER	ECO version

11230180 EMMC50_PAD_CTL0 MSDC eMMC5.0 CLK PAD Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name																
Type																
Reset																

Bit(s)	Name	Description

11230184 EMMC50_PAD_DS_CTL0 MSDC eMMC5.0 DS PAD Control Register 0 0000001C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11230188 EMMC50_PAD_DS_TUNE MSDC eMMC5.0 DS Pad Tuning Register 00014015

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1123018C EMMC50_PAD_CMD_TUNE MSDC eMMC5.0 CMD Pad Tuning Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

Bit(s)	Name	Description

11230190 EMMC50_PAD_DAT01_TUNE **MSDC eMMC5.0 DAT0/1 Pad Tuning Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11230194 EMMC50_PAD_DAT23_TUNE **MSDC eMMC5.0 DAT2/3 Pad Tuning Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11230198 EMMC50_PAD_DAT45_TUNE **MSDC eMMC5.0 DAT4/5 Pad Tuning Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1123019C EMMC50_PAD_DAT67_TUNE **MSDC eMMC5.0 DAT6/7 Pad Tuning Register** **00000000**

E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11230204 EMMC51_CFG eMMC51 Configuration Register 0 1A86A000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CMDQ_CMD_ENABLE										RDAT_CNT					
Type	RW										RW					
Reset	0	0	0	1	1	0	1	0	1	0	0	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDAT_CNT				RAL0		RAL1		WDAT_CNT							CMDQ_EN
Type	RW				RW		RW		RW							RW
Reset	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:22	**CMDQCMDEN**	CMDQ_CMD_ENABLE	**Configures CMD queue enable type** 1'b0: Enable CMD queue for cmd13, cmd44, cmd45 1'b1: Enable CMD queue for all cmd
21:12	**RDATCNT**	RDAT_CNT	**Read data counter threshold for CMD queue**
11:10		RAL0	
9:7		RAL1	
6:1	**WDATCNT**	WDAT_CNT	**Write data counter threshold for CMD queue**
0	**CMDQEN**	CMDQ_EN	**Enables CMD queue**

11230208 EMMC50_CFG eMMC50 Configuration Register 0 02E889E2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MSDC_RD_VALID_SEL	MSDC_WR_VALID_SEL	MSDC_RD_VALID	MSDC_WR_VALID	EMMC50_MON_SEL	READ_DAT_CNT			ENDBIT_CNT				
Type				RW	RW	RU	RU	RW	RW			RW				
Reset				0	0	0	1	0	1	1	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENDBIT_CNT					CMD_EDGE_SEL	CMD_RESP_SEL	END_BIT_CHK_CNT				CRC_STS_SEL	CRC_STS_EDGE	CRC_STS_CNT		PAD_CMD_LATCH_CK
Type	RW					RW	RW	RW				RW	RW	RW		RW
Reset	1	0	0	0	1	0	0	1	1	1	1	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
28	**RDVALIDSEL**	MSDC_RD_VALID_ SEL	
27	**WRVALIDSEL**	MSDC_WR_VALID_ SEL	
26	**MSDCRDVALID**	MSDC_RD_VALID	**For eMMC50 spec, the host cannot stop pad CLK in one block transfer, so the host should have the whole block len data in FIFO when the host is to transfer data to device.** 1'b0: SD FIFO is not valid to read for writing device. 1'b1: SD FIFO is valid to read for writing device.
25	**MSDCWRVALID**	MSDC_WR_VALID	**For eMMC50 spec, the host cannot stop pad CLK in one block transfer, so the host should have enough space for storing a block len data read from device.** 0: SD FIFO is not valid for reading data from device. 1: SD FIFO is valid for reading data from device.
24	**EMMC50MONSEL**	EMMC50_MON_SEL	**Set this bit to 1 to debug eMMC50 signals.** 0: Select eMMC50 debug signals to debug pin 1: Does not select eMMC50 debug signals to debug pins
23:21	**READDATCNT**	READ_DAT_CNT	**Decides to latch how many data in RCLK domain switch pop condition**
20:11	**ENDBITCNT**	ENDBIT_CNT	**Sets up endbit check value in RCLK domain**
10	**CMDEDGESEL**	CMD_EDGE_SEL	**Selects CMD response edge** 1'b0: CMD response from RCLK rising edge latch 1'b1: CMD response from RCLK falling edge latch
9	**CMDRESPSEL**	CMD_RESP_SEL	**Selects CMD response output** 1'b0: CMD response from delay line; same as eMMC4.5 spec design 1'b1: CMD response from FIFO; this is design for eMMC5.0 spec
8:5	**END_BITCHKCNT**	END_BIT_CHK_CN T	**Decides how many cycles to check device busy status after CRC status**
4	**CRCSTSSEL**	CRC_STS_SEL	**Selects CRC status output** 1'b0: CRC status data from 2-DFF, before eMMC5.0 is used 1'b1: CRC status data from FIFO. eMMC5.0 is used.
3	**CRCSTSEDGE**	CRC_STS_EDGE	**In HS400 mode, selects CRC status data psh** 1'b0: In HS400 mode, select rising edge CRC status data psh 1'b1: In HS400 mode, select falling edge CRC status data psh
2:1	**CRCSTSCNT**	CRC_STS_CNT	
0	**PADLATCK**	PAD_CMD_LATCH_ CK	**In HS400 modes, selects pad CMD latch clock** 1'b0: Select internal clock as pad CMD latch clock in HS400 mode 1'b1: Select DS (RCLK) as pad CMD latch clock in HS400 mode

1123020C EMMC50_CFG1 **eMMC50 Configuration Register** **0100070C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserveo			DS_CFG	PSH_PS_SEL	PSH_CNT			EMMC50_DEBUG_SEL							
Type	RW			RW	RW	RW			RW							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAIT_8_CLK_CNT				RD_DAT_STOP	LATCH_CK_SWITCH_CNT			WR_PTR_MARGIN							
Type	RW				RW	RW			RW							
Reset	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	0

Bit(s)	Mnemonic	Name	Description
31:29		reserve0	**Reserved for backup2**
28	**DSCFG**	DS_CFG	**Defines whether to mask redundant DS clock** 1'b0: Mask redundant DS clock 1'b1: Does not mask redundant DS clock
27	**PSHPSSEL**	PSH_PS_SEL	**Defines using rising or falling edge push pulse** 1'b0: Rising edge pulse 1'b1: Falling edge pulse
26:24	**PSHCNT**	PSH_CNT	**Defines how many push cnt start sync pop pulse to pop data**
23:16	**EMMC50DEBUGSEL**	EMMC50_DEBUG_SEL	**Selects eMMC50 debug signal out**
15:12	**WAIT8CLKCNT**	WAIT_8_CLK_CNT	**Configures 8 clock counter**
11	**RDATSTOP**	RD_DAT_STOP	**Selects eMMC50 read data stop signals** 1'b0: Select rising signal 1'b1: Select falling signal
10:8	**CKSWITCHCNT**	LATCH_CK_SWITCH_CNT	**After CRC status sets up latchclock switch counter**
7:0	**WRPTRMARGIN**	WR_PTR_MARGIN	**Write pointer marign**

1123021C EMMC50_CFG_2 **AHB2AXI Wrapper Control Register** **0F0C0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11230220 EMMC50_CFG_3 **0F28A3C1**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11230224 EMMC50_CFG_4 **0001001E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11230228 EMMC50_BLOCK_LENGTH **00000080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

Module name: MSDC1 Base address: (+11240000h)

Address	Name	Width	Register Function
11240000	MSDC_CFG	32	MSDC Configuration Register
11240004	MSDC_IOCON	32	MSDC IO Configuration Register
11240008	MSDC_PS	32	MSDC Pin Status Register
1124000C	MSDC_INT	32	MSDC Interrupt Register
11240010	MSDC_INTEN	32	MSDC Interrupt Enable Register
11240014	MSDC_FIFOCS	32	MSDC FIFO Control and Status Register
11240018	MSDC_TXDATA	32	MSDC TX Data Port Register
1124001C	MSDC_RXDATA	32	MSDC RX Data Port Register
11240030	SDC_CFG	32	SD Configuration Register
11240034	SDC_CMD	32	SD Command Register
11240038	SDC_ARG	32	SD Argument Register
1124003C	SDC_STS	32	SD Status Register
11240040	SDC_RESP0	32	SD Response Register 0

Address	Name	Width	Register Function
11240044	SDC_RESP1	32	SD Response Register 1
11240048	SDC_RESP2	32	SD Response Register 2
1124004C	SDC_RESP3	32	SD Response Register 3
11240050	SDC_BLK_NUM	32	SD Block Number Register
11240054	SDC_VOL_CHG	32	SD Voltage Change Wait Time Register
11240058	SDC_CSTS	32	SD Card Status Register
1124005C	SDC_CSTS_EN	32	SD Card Status Enable Register
11240060	SDC_DATCRC_STS	32	SD Card Data CRC Status Register
11240070	EMMC_CFG0	32	EMMC Configuration Register 0
11240074	EMMC_CFG1	32	EMMC Configuration Register 1
11240078	EMMC_STS	32	EMMC Status Register
1124007C	EMMC_IOCON	32	EMMC IO Control Register
11240080	SD_ACMD_RESP	32	SD ACMD Response Register
11240084	SD_ACMD19_TRG	32	SD ACMD19 Target Register
11240088	SD_ACMD19_STS	32	SD ACMD19 Status Register
1124008C	DMA_SA_HIGH4BIT	32	DMA Current Address Resgiter of High 4 Bits
11240090	DMA_SA	32	DMA Start Address Register
11240094	DMA_CA	32	DMA Current Address Register
11240098	DMA_CTRL	32	DMA Control Register
1124009C	DMA_CFG	32	DMA Configuration Register
112400A0	SW_DBG_SEL	32	MSDC S/W Debug Selection Register
112400A4	SW_DBG_OUT	32	MSDC S/W Debug Output Register
112400A8	DMA_LENGTH	32	DMA Length Register
112400B0	PATCH_BIT0	32	MSDC Patch Bit Register 0
112400B4	PATCH_BIT1	32	MSDC Patch Bit Register 1
112400B8	PATCH_BIT2	32	MSDC Patch Bit Register 2
112400C0	DAT0_TUNE_CRC	32	DAT0 Tune Result Register
112400C4	DAT1_TUNE_CRC	32	DAT1 Tune Result Register
112400C8	DAT2_TUNE_CRC	32	DAT2 Tune Result Register
112400CC	DAT3_TUNE_CRC	32	DAT3 Tune Result Register
112400D0	CMD_TUNE_CRC	32	CMD Tune Result Register
112400D4	SDIO_TUNE_WIND	32	SDIO Tune Window Register 0
112400F0	DAT_RD_DLY0	32	MSDC Data Delay Line Register 0
112400F4	DAT_RD_DLY1	32	MSDC Data Delay Line Register 1
112400F8	HW_DBG_SEL	32	MSDC H/W Debug Selection Register
11240100	MAIN_VER	32	MSDC Main Version Register
11240104	ECO_VER	32	MSDC ECO Version Register

11240000 MSDC_CFG MSDC Configuration Register 02000099

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CARD_CK_DIV			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	CARD_CK_DIV								CARD_CK_STABLE			CARD_CK_DRV_EN	PIO_MODE	RST	CARD_CK_PWDN	MSDC
Type	RW								RU			RW	RW	Ao	RW	RW
Reset	0	0	0	0	0	0	0	0	1			1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
19:8	**CCKDIV**	CARD_CK_DIV	**MS/SD card clock divider** Controls clock frequency of serial clock on MS/SD bus. Refer to "Data Line Latching Timing Diagram" and "Response Latching Timing Diagram". For non-DDR mode, msdc_ck equals SD bus clock. (Example: For SDR25 or HS, msdc_ck and SD bus clock will be 50MHz.) For DDR mode, msdc_ck denotes the MSDC internal clock which will be dobuled to SD bus clock. (Example: For DDR50, msdc_ck should be set to 100MHz, and bus clock will be 50MHz.) 8'b00000000: msdc_ck = (1/2)*msdc_src_ck 8'b00000001: msdc_ck = [1/(4*1)]*msdc_src_ck 8'b00000010: msdc_ck = [1/(4*2)]*msdc_src_ck 8'b00000011: msdc_ck = [1/(4*3)]*msdc_src_ck 8'b00010000: msdc_ck = [1/(4*16)]*msdc_src_ck 8'b11111111: msdc_ck = [1/(4*255)]*msdc_src_ck
7	**CCKSB**	CARD_CK_STABLE	**MS/SD card clock is stable or not** After programming CARD_CK_MODE or CARD_CK_DIV, this bit will immediately become 0 and return to 1 if stable. Poll this register to ensure safety control of MSDC. 1'b0: Clock output is not stable. 1'b1: Clock output is stable.
4	**CCKDRVE**	CARD_CK_DRV_EN	**SD/MS card bus clock drive enable bit** Set this bit to 1 to enable MSDC bus clock driver. The default bus state depends on MSDC_CFG][1] CARD_CK_PWDN bit. If MSDC_CFG[1] CARD_CK_PWDN= 1, the default clock state will be free running. If MSDC_CFG[1] CARD_CK_PWDN = 0, the default clock state will be gated to 0. Set this bit to 0 to put the bus state into "tri-state". Default: 1 1'b0: Put the clock pad into tri-state 1'b1: Enable MSDC to drive clock pad; the state of CLK depends on MSDC_CFG[1] CARD_CK_PWDN.
3	**PIO**	PIO_MODE	**MS/SD PIO mode** Selects PIO mode Default: PIO mode 1'b0: DMA mode 1'b1: PIO mode
2	**RST**	RST	**Software reset** Writing 1 to this register will cause internal synchronous reset of MS/SD controller, and it will not reset register settings and DMA controller. The reset sequence is done when this bit becomes 0. SW should wait this bit to return to 0 after writing 1. 1'b0: MS/SD controller is not in reset state. 1'b1: MS/SD controller is in reset state.
1	**CCKPD**	CARD_CK_PWDN	**MSDC bus clock power-down mode** Controls card clock power-down mode.

Bit(s)	Mnemonic	Name	Description
			1'b0: Clock is gated to 0 if no command or data is transmitted. 1'b1: Clock is free running even if no command or data is transmitted. (The clock may still be stopped when MSDC write data are not enough or no space for the next read data.)
0	**MSDC**	MSDC	**Selects MS/SD mode** Configures the controller as the host of memory stick or as the host of SD/MMC memory card. The default value is configuring the controller as the host of memory stick. 1'b0: Configure the controller as the host of memory stick 1'b1: Configure the controller as the host of SD/MMC memory card

11240004 MSDC_IOCON MSDC IO Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									R_D7_SMPL	R_D6_SMPL	R_D5_SMPL	R_D4_SMPL	R_D3_SMPL	R_D2_SMPL	R_D1_SMPL	R_D0_SMPL
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			W_D3_SMPL	W_D2_SMPL	W_D1_SMPL	W_D0_SMPL	W_D_SMPL_SEL	W_D_SMPL			R_D_SMPL_SEL		D_DLYLINE_SEL	R_D_SMPL	R_SMPL	SDR104_CLK_SEL
Type			RW	RW	RW	RW	RW	RW			RW		RW	RW	RW	RW
Reset			0	0	0	0	0	0			0		0	0	0	0

Bit(s)	Mnemonic	Name	Description
23	**RD7SPL**	R_D7_SMPL	**Selects read data 7 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
22	**RD6SPL**	R_D6_SMPL	**Selects read data 6 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
21	**RD5SPL**	R_D5_SMPL	**Selects read data 5 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
20	**RD4SPL**	R_D4_SMPL	**Selects read data 4 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
19	**RD3SPL**	R_D3_SMPL	**Selects read data 3 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
18	**RD2SPL**	R_D2_SMPL	**Selects read data 2 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge

Bit(s)	Mnemonic	Name	Description
17	**RD1SPL**	R_D1_SMPL	**Selects read data 1 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
16	**RD0SPL**	R_D0_SMPL	**Selects read data 0 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
13	**WD3SPL**	W_D3_SMPL	**Selects SDIO interrupt sample** This bit is only valid when bit 9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
12	**WD2SPL**	W_D2_SMPL	**Selects SDIO interrupt sample** This bit is only valid when bit 9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
11	**WD1SPL**	W_D1_SMPL	**Selects SDIO interrupt sample** This bit is only valid when bit 9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
10	**WD0SPL**	W_D0_SMPL	**Selects CRC status and SDIO interrupt sample** This bit is only valid when bit 9 is on. 1'b0: Sample CRC Status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC Status and SDIO interrupt by external bus clock falling edge
9	**WDSPLSEL**	W_D_SMPL_SEL	**Selects data line rising/falling latch fine-tuning in write transaction** 1'b0: All data line share one value indicated by MSDC_IOCON.W_D_SMPL 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.W_D0_SMPL Data line 1: MSDC_IOCON.W_D1_SMPL Data line 2: MSDC_IOCON.W_D2_SMPL Data line 3: MSDC_IOCON.W_D3_SMPL
8	**WDSPL**	W_D_SMPL	**Selects CRC status and SDIO interrupt sample** 1'b0: Sample CRC status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC status and SDIO interrupt by external bus clock falling edge
5	**RDSPLSEL**	R_D_SMPL_SEL	**Selects data line rising/falling latch fine-tuning in read transaction** 1'b0: All data line share one value indicated by MSDC_IOCON.R_D_SMPL 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.R_D0_SMPL Data line 1: MSDC_IOCON.R_D1_SMPL Data line 2: MSDC_IOCON.R_D2_SMPL Data line 3: MSDC_IOCON.R_D3_SMPL Data line 4: MSDC_IOCON.R_D4_SMPL Data line 5: MSDC_IOCON.R_D5_SMPL

Bit(s)	Mnemonic	Name	Description
			Data line 6: MSDC_IOCON.R_D6_SMPL Data line 7: MSDC_IOCON.R_D7_SMPL
3	**DDLSEL**	D_DLYLINE_SEL	**Selects data line delay line fine-tuning** 1'b0: All data line share one delay selection value indicated by PAD_TUNE.PAD_DAT_RD_RXDLY 1'b1: Each data line has its own delay selection value indicated by Data line 0: DAT_RD_DLY0.DAT0_RD_DLY Data line 1: DAT_RD_DLY0.DAT1_RD_DLY Data line 2: DAT_RD_DLY0.DAT2_RD_DLY Data line 3: DAT_RD_DLY0.DAT3_RD_DLY Data line 4: DAT_RD_DLY1.DAT4_RD_DLY Data line 5: DAT_RD_DLY1.DAT5_RD_DLY Data line 6: DAT_RD_DLY1.DAT6_RD_DLY Data line 7: DAT_RD_DLY1.DAT7_RD_DLY
2	**RDSPL**	R_D_SMPL	**Selects read data sample** 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
1	**RSPL**	R_SMPL	**Selects command response sample** 1'b0: Sample response by external bus clock rising edge 1'b1: Sample response by external bus clock falling edge
0	**SDR104CKS**	SDR104_CLK_SEL	**SDR104 SCLK output clock control** Only used when MSDC_CFG[17:16] CARD_CK_MODE is 2'b01. 1'b0: Bus clock output equals inverted msdc_src_ck 1'b1: Bus clock output equals msdc_src_ck

11240008 MSDC_PS **MSDC Pin Status Register** **81FF0002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SD_WP							CMD	DAT							
Type	RU							RU	RU							
Reset	1							1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDDEBOUNCE														CDSTS	CDEN
Type	RW														RU	RW
Reset	0	0	0	0											1	0

Bit(s)	Mnemonic	Name	Description
31	**SDWP**	SD_WP	**Write Protection switch status on SD memory card** Shows the status of Write Protection switch on SD memory card. There is no default reset value. The pin WP (Write Protection) is only useful when the controller is configured for SD memory card. 1'b0: Write Protection switch on. Memory card is desired to be write-protected. 1'b1: Write Protection switch off. Memory card is writable.
24	**CMD**	CMD	**Command line status** Reflects the command line value of MSDC bus.
23:16	**DAT**	DAT	**Data line status** Reflects the data line value of MSDC bus (8-bit).

Bit(s)	Mnemonic	Name	Description
15:12	**CDDBCE**	CDDEBOUNCE	**Card detection de-bounce timer** Specifies time interval for card detection de-bounce. Default value: 0, meaning the de-bounce interval is one 32kHz cycle. The interval will extend one cycle time of 32kHz by increasing the counter by 1.
1	**CDSTS**	CDSTS	**Card detection status** 1'b1: Card detection pin status is logic high.
0	**CDEN**	CDEN	**Enables card detection** Controls card detection circuit. 1'b0: Disable card detection 1'b1: Enable card detection

1124000C MSDC_INT MSDC Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													DMA_PROTECT	GPD_CS_ERR	BD_CS_ERR	
Type													W1C	W1C	W1C	
Reset													0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SD_DATA_CRCERR	SD_DATTO	DMA_XFER_DONE	SD_XFER_COMPLETE	SD_CSTS	SD_RESP_CRCERR	SD_CMDTO	SD_CMDRDY		DMA_Q_EMPTY	SD_AUTOCMD_RESP_CRCERR	SD_AUTOCMD_CMDTO	SD_AUTOCMD_CMDRDY		MSDC_CDSC	MMC_IRQ
Type	W1C	W1C	W1C	W1C	RU	W1C	W1C	W1C		W1C	W1C	W1C	W1C		W1C	W1C
Reset	0	0	0	0	0	0	0	0		0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
19	**DMAPROTECT**	DMA_PROTECT	**There is write operation to DMA start address, length, start bit or the last buf bit.**
18	**GPDCSERR**	GPD_CS_ERR	**GPD checksum error detected**
17	**BDCSERR**	BD_CS_ERR	**BD checksum error detected**
15	**SDDCRCERR**	SD_DATA_CRCERR	**SD data CRC error interrupt** Indicates MS/SD controller detects a CRC error after reading a block of data from the DAT line or SD/MMC signals a CRC error after writing a block of data to the DAT line. 1'b0: Otherwise 1'b1: MS/SD controller detects a CRC error after reading a block of data from the DAT line or SD/MMC signals a CRC error after writing a block of data to the DAT line.
14	**SDDTO**	SD_DATTO	**SD data timeout interrupt** Indicates SD/MMC controller detects a timeout condition while waiting for data token on the DAT line. This bit is for both data read and data write. For SD data read, timeout will occur when the read data are not presented. For SD data write, timeout will occur when the write data CRC status is not presented if PATCH_BIT[30] DETECT_WR_CRC_TIMEOUT = 1. 1'b0: Otherwise 1'b1: SD/MMC controller detects a timeout condition while waiting for data token on the DAT line.
13	**DMAXFDNE**	DMA_XFER_DONE	**DMA transfer done interrupt**

Bit(s)	Mnemonic	Name	Description
			Indicates status of data block transfer. 1'b0: Otherwise 1'b1: A data block is successfully transferred.
12	**SDXFCPL**	SD_XFER_COMPLETE	**SD data transfer completed interrupt** Indicates transaction which contains data that are completed. While performing tuning procedure (Execute Tuning is set to 1), SD_XFER_COMPLETE is not set to 1.
11	**SDCSTS**	SD_CSTS	**SD CSTA update interrupt** Indicates any bit in register SDC_CSTA is active. The register bit will be set to 1. SW should clear SDC_CSTA, and this bit will be de-asserted automatically. 1'b0: No SD memory card interrupt 1'b1: SD memory card interrupt exists.
10	**SDRCRCER**	SD_RESP_CRCERR	**SD command CRC error interrupt** Indicates SD/MMC controller detects a CRC error after reading a response from the CMD line. 1'b0: Otherwise 1'b1: SD/MMC controller detects a CRC error after reading a response from the CMD line.
9	**SDCTO**	SD_CMDTO	**SD command timeout interrupt** Indicates SD/MMC controller detects a timeout condition while waiting for a response on the CMD line. 1'b0: Otherwise 1'b1: SD/MMC controller detects a timeout condition while waiting for a response on the CMD line.
8	**SDCRDY**	SD_CMDRDY	**SD command ready interrupt** For the command without response, the register bit will be 1 once the command is completed on SD/MMC bus. For command with response without busy, the register bit will be 1 whenever the command is issued onto SD/MMC bus and its corresponding response is received without CRC error. For command with response with busy in DAT0, the register bit will be 1 whenever the command is issued onto SD/MMC bus and its corresponding response is received without CRC error and the DAT0 transited from busy to idle. 1'b0: Otherwise 1'b1: Command finished successfully without a CRC error
6	**DMAQEPTY**	DMA_Q_EMPTY	**DMA queue empty interrupt** Indicates the current DMA queue is empty. Only for descriptor mode and enhance mode.
5	**SDACDRCRCER**	SD_AUTOCMD_RESP_CRCERR	**SD auto command CRC error interrupt** Set when detecting a CRC error in the auto command response.
4	**SDACDCTO**	SD_AUTOCMD_CMDTO	**SD auto command timeout interrupt** Set if no response is returned within a specified cycles (64T in spec) from the end bit of auto command.
3	**SDACDCRDY**	SD_AUTOCMD_CMDRDY	**SD auto command ready interrupt** Set if auto command is executed without CRC error or timeout.
1	**MSDCCDSC**	MSDC_CDSC	**MSDC card detection status change interrupt** Indicates if any interrupt for memory card insertion/removal exists. Whenever memory card is inserted or removed and card detection circuit is enabled, i.e. register bit CDEN in register MSDC_PS is set to 1, the register bit will be set to 1. It will be reset when the register is read. 1'b0: Otherwise

Bit(s)	Mnemonic	Name	Description
0	**MMCIRQ**	MMC_IRQ	1'b1: Card is inserted or removed. **MMC card interrupt** 1'b0: Otherwise 1'b1: MMC card interrupt event occurs.

11240010 MSDC_INTEN MSDC Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													EN_DMA_PROTECT	EN_GPD_CS_ERR	EN_BD_CS_ERR	
Type													RW	RW	RW	
Reset													0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SD_DATA_CRCERR	EN_SD_DATTO	EN_SD_DMA_XFER_DONE	EN_SD_XFER_COMPL ETE	EN_SD_CSTA	EN_SD_RESP_CRCERR	EN_SD_CMDTO	EN_SD_CMDRDY	EN_SD_SDIOIRQ	EN_DMA_Q_EMPTY	EN_SD_AUTOCMD_RESP_CRCERR	EN_SD_AUTOCMD_CMDTO	EN_AUTOCMD_CMDRDY		EN_MSDC_CDSC	EN_MMC_IRQ
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
19	**ENDMAPROTECT**	EN_DMA_PROTECT	**Enables DMA protection interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
18	**ENGPDCSERR**	EN_GPD_CS_ERR	**Enables GPD checksum error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
17	**ENBDCSERR**	EN_BD_CS_ERR	**Enables BD checksum error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
15	**ENSDDCRCERR**	EN_SD_DATA_CRC ERR	**Enables SD data CRC error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
14	**ENSDDTO**	EN_SD_DATTO	**Enables SD data timeout interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
13	**ENDMAXFDNE**	EN_SD_DMA_XFER _DONE	**Enables DMA transfer done interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
12	**ENSDXFCPL**	EN_SD_XFER_COM PLETE	**Enables SD data transfer completed interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
11	**ENSDCSTA**	EN_SD_CSTA	**Enables SD CSTA update interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
10	**ENSDRCRCER**	EN_SD_RESP_CRC ERR	**Enables SD command CRC error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
9	**ENSDCTO**	EN_SD_CMDTO	**Enables SD command timeout interrupt** 1'b0: Disable interrupt

Bit(s)	Mnemonic	Name	Description
			1'b1: Enable interrupt
8	**ENSDCRDY**	EN_SD_CMDRDY	**Enables SD command ready interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
7	**ENSDIOIRQ**	EN_SD_SDIOIRQ	**Enables SD SDIO interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
6	**ENDMAQEPTY**	EN_DMA_Q_EMPTY	**Enables DMA queue empty interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
5	**ENSDACDRCRCER**	EN_SD_AUTOCMD_RESP_CRCERR	**Enables SD auto command CRC error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
4	**ENSDACDCTO**	EN_SD_AUTOCMD_CMDTO	**Enables SD auto command timeout interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
3	**ENSDACDCRDY**	EN_AUTOCMD_CMDRDY	**Enables SD auto command ready interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
1	**ENMSDCCDSC**	EN_MSDC_CDSC	**Enables MSDC card detection status change interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
0	**ENMMCIRQ**	EN_MMC_IRQ	**Enables MMC card interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt

11240014 MSDC_FIFOCS **MSDC FIFO Control and Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFOCLR								TXFIFOCNT							
Type	A0								RU							
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RXFIFOCNT							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**FIFOCLR**	FIFOCLR	**Clears embedded FIFO** Write 1 to this bit to clear FIFO. It will become 0 when FIFO is cleared. SW needs to check this bit to make sure clearing FIFO sequence is done. This bit can be used when the data read/write sequence has error and needs to clear HW FIFO.
23:16	**TXFIFOCNT**	TXFIFOCNT	**TX FIFO count for MSDC write** 8'd0: No data in FIFO 8'd1: 1-byte data in FIFO 8'd2: 2-byte data in FIFO 8'd131: Max. 131-byte data in FIFO Others: Reserved

Bit(s)	Mnemonic	Name	Description
7:0	**RXFIFOCNT**	RXFIFOCNT	**RX FIFO count for MSDC read** 8'd0: No data in FIFO 8'd1: 1-byte data in FIFO 8'd2: 2-byte data in FIFO 8'd131: Max. 131-byte data in FIFO Others: Reserved

11240018 MSDC_TXDATA MSDC TX Data Port Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PIO_TXDATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIO_TXDATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PIOTXDATA**	PIO_TXDATA	**PIO mode TXDATA port** This register can be accessed by byte, half-word or word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

1124001C MSDC_RXDATA MSDC RX Data Port Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PIO_RXDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIO_RXDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PIORXDATA**	PIO_RXDATA	**PIO mode RXDATA port** This register can be accessed by byte, half-word or word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

11240030 SDC_CFG SD Configuration Register 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DTOC										INT_AT_BLOCK_GAP	SDIO_INT_DET_EN	SDIO		BUSW IDTH	
Type	RW										RW	RW	RW		RW	
Reset	0	0	0	0	0	0	0	0			0	1	0		0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															WAKEUP_INS_EN	WAKEUP_SDIOINT_EN
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DTOC**	DTOC	**Data timeout counter** The period from the end of the initial host read command or the last read data block in a multiple block read operation to the start bit of the next read data block requires at least two serial clock cycles. The counter is used to extend the period (Read Data Access Time) in unit of 1,048,576 serial clocks. 8'b00000000: Extend 1,048,576 more serial clock cycles 8'b00000001: Extend 1,048,576*2 more serial clock cycles 8'b00000010: Extend 1,048,576*3 more serial clock cycles 8'b11111111: Extend 1,048,576*256 more serial clock cycles
21	**INTBGP**	INT_AT_BLOCK_G AP	**Interrupt at block gap** This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Set to 1 to enable interrupt detection at the block gap for a multiple block transfer. Set to 0 to disable interrupt detection during a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the host driver detects an SD card insertion, it will set up this bit according to the CCCR of the SDIO card. 1'b0: Disable interrupt detection at block gap 1'b1: Enable interrupt detection at block gap
20	**SDIOIDE**	SDIO_INT_DET_E N	**Enables SDIO interrupt detection** Informs SD controller to sense the SDIO interrupt. 1'b0: Disable SDIO interrupt detection 1'b1: Enable SDIO interrupt detection if the SDIO bit is also on
19	**SDIO**	SDIO	**SDIO mode enable bit** Enables support to sense the SDIO interrupt and disables R4 response CRC check for SDIO card. 1'b0: Disable SDIO mode 1'b1: Enable SDIO mode
17:16	**BUSWD**	BUSWIDTH	**Configures bus width** Defines SD/MMC bus width. 2'b00: 1 bit mode 2'b01: 4 bit mode 2'b10: 8 bit mode 2'b11: Reserved
1	**ENWKUPINS**	WAKEUP_INS_EN	**Card status change wakeup event enable bit** 1'b0: Disable wakeup event for card status change 1'b1: Enable wakeup event for card status change
0	**ENWKUPSDIOINT**	WAKEUP_SDIOINT _EN	**SDIO card interrupt wakeup event enable bit** 1'b0: Disable wakeup event for SDIO card interrupt 1'b1: Enable wakeup event for SDIO card interrupt

Bit(s)	Mnemonic	Name	Description

11240034 SDC_CMD **SD Command Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LEN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GO_IRQ	STOP	RW	DTYPE			RSPTYP			BREAK	CMD					
Type	RW	RW	RW	RW			RW			RW	RW					
Reset	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**LEN**	LEN	**Length** Defines the length of one block (unit: byte) in a data transaction of block mode or the data length (unit: byte) in data transaction of byte mode. The maximal value of block length is 2,048 bytes. 12'b000000000000: Reserved 12'b000000000001: Block length is 1 byte 12'b000000000010: Block length is 2 bytes. 12'b011111111111: Block length is 2047 bytes. 12'b100000000000: Block length is 2048 bytes.
15	**GOIRQ**	GO_IRQ	**GO_IRQ command** Indicates if the command is GO_IRQ_STATE (CMD40) and used only for MMC protocol. If the command is GO_IRQ_STATE, the period between command token and response token will not be limited. 1'b0: The command is not GO_IRQ_STATE. 1'b1: The command is GO_IRQ_STATE.
14	**STOP**	STOP	**Stop command** Indicates if the command is a stop transmission command. It should be set to 1 when CMD12 (SD/MMC) or CMD52 with I/O abort (SDIO) is to be issued. 1'b0: The command is not a stop transmission command. 1'b1: The command is a stop transmission command.
13	**RW**	RW	**Selects command read write** Defines the command is a read command or write command. The register bit is valid only when the command causes a transaction with data token. 1'b0: The command is a read command. 1'b1: The command is a write command.
12:11	**DTYPE**	DTYPE	**Selects data block** Defines data token type for the command. 2'b00: No data token for the command 2'b01: Single block transaction (only available in block mode) 2'b10: Multiple block transaction (only available in block mode) 2'b11: Stream operation. Should only be used in MMC protocol (only available in block mode).
9:7	**RSPTYP**	RSPTYP	**Command response type** 3'b000: This command has no response. 3'b001: The command has R1/R5/R6/R7 response. The response token is 48-bit with CRC check (for

Bit(s)	Mnemonic	Name	Description
			SD/MMC/SDIO)(excluding SDIO abort command) 3'b010: The command has R2 response. The response token is 136-bit (for SD/MMC). 3'b011: The command has R3 response. The response token is 48-bit response, no CRC check (for SD/MMC). 3'b100: The command has R4 response. The response token is 48-bit without CRC check (for SDIO); the response token is 48-bit with CRC check (for MMC). 3'b111: The command has R1b response. The response token is 48-bit (for SD/MMC/SDIO).
6	**BREAK**	BREAK	**Aborts pending MMC GO_IRQ command** Only valid for a pending GO_IRQ_MODE command waiting for MMC interrupt response. 1'b0: Not a beak command 1'b1: Break a pending MMC GO_IRQ_MODE command in the controller
5:0	**CMD**	CMD	**SD memory card command**

11240038 SDC_ARG **SD Argument Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ARG**	ARG	Memory card controller argument register

1124003C SDC_STS **SD Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMC_STREAM_WR_COMPL															CMD_WR_BUSY
Type	RU															W1C
Reset	0															0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CMDBUSY	SDCBUSY
Type															RU	RU
Reset															0	0

Bit(s)	Mnemonic	Name	Description
31	**MMCSWRCPL**	MMC_STREAM_WR_COMPL	**MMC stream mode write data are all flushed to MMC card** SW can use this bit to confirm the last write data are flushed to MMC then issue STOP command. This bit is only valid when the command SDC_CMD.DTYPE=2'b11.

Bit(s)	Mnemonic	Name	Description
			1'b0: Last data are partially inside MSDC. 1'b1: Flush last data to MMC card
16		CMD_WR_BUSY	
1	**CMDBSY**	CMDBUSY	**SD command line busy status** SW should always read this bit to make sure the command line is not busy before sending the next command. If the command is R1B or data read/write command, SW should check the SDCBUSY bit too. Note: When auto command 12 is enabled, this bit will be asserted immediately after SDC_CMD is written and de-asserted after auto-command 12 is finished. 1'b0: No transmission is going on CMD line on SD bus. 1'b1: There is transmission going on CMD line on SD bus.
0	**SDCBSY**	SDCBUSY	**SD controller busy status** 1'b0: SD controller is idle. 1'b1: SD controller is busy.

11240040 SDC_RESP0 SD Response Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP0**	RESP0	Memory card controller response register 0

11240044 SDC_RESP1 SD Response Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP1**	RESP1	Memory card controller response register 1

11240048 SDC_RESP2 SD Response Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP2															

Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP2**	RESP2	Memory card controller response register 2

1124004C SDC_RESP3 SD Response Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP3**	RESP3	Memory card controller response register 3

11240050 SDC_BLK_NUM SD Block Number Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BLOCK_NUMBER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLOCK_NUMBER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:0	**BLKNUM**	BLOCK_NUMBER	**Memory card controller block number** Indicates block number of data transaction. 32'd0: Reserved 32'd1: 1 data block 32'd2: 2 data block 32'd3: 3 data block 32'hffffffff: 4GB-1 data block

11240054 SDC_VOL_CHG SD Voltage Change Wait Time Register 00000145

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11240058 SDC_CSTS SD Card Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CSTS**	CSTS	**CSTS** The card status field in the response R1 or R1b field. Each bit can be written 1 to clear individually.

1124005C SDC_CSTS_EN SD Card Status Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTS_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CSTS_EN**	CSTS_EN	**CSTS_EN** Controls which bit of CSTA will generate MSDC_INT.SDCSTA.

11240060 SDC_DATCRC_STS SD Card Data CRC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DAT_CRCSTS_POS							

Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**DCSSP**	DAT_CRCSTS_POS	**MSDC read DATA CRC status** Reflects CRC status of data line[7:0]. Only for MSDC read. 1'b0: No CRC error 1'b1: CRC error

11240070 EMMC_CFG0 EMMC Configuration Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11240074 EMMC_CFG1 EMMC Configuration Register 1 00200003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11240078 EMMC_STS EMMC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1124007C EMMC_IOCON — EMMC IO Control Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11240080 SD_ACMD_RESP — SD ACMD Response Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AUTOCMD_RESP															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOCMD_RESP															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ACMDRESP**	AUTOCMD_RESP	**SD auto command response register** Stores the response[39:8] of ACMD12/ACMD23/ACMD19.

11240084 SD_ACMD19_TRG — SD ACMD19 Target Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11240088 SD_ACMD19_STS — SD ACMD19 Status Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1124008C DMA_SA_HIGH4BIT **DMA Current Address Resgiter of High 4 Bits** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMA_SURR_ADDR_HIGH4BIT			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DMASAHIGH4BIT**	DMA_SURR_ADDR_HIGH4BIT	Sets up high 4-bit address of start address because 64G DRAM needs 36-bit address

11240090 DMA_SA **DMA Start Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_STR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_STR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DMASA**	DMA_STR_ADDR	**Start address of the DMA address** Sets up the start address of the DMA. In DMA basic mode, this field indicates the source or destination address of the data transfer which depends on the command. In descriptor base DMA, this is the descriptor chain start address.

11240094 DMA_CA **DMA Current Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_CURR_ADDR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_CURR_ADDR															

Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DMACA**	DMA_CURR_ADDR	**Current address of the DMA address** Reads the current address of the DMA descriptor chain.

11240098 DMA_CTRL DMA Control Register 00006008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		BURST_SIZE			DMA_SPLIT_1K	LAST_BUF	DMA_ALIGN	DMA_MODE					AHB_READYM	DMA_RESUME	DMA_STOP	DMA_START
Type		RW			RW	RW	RW	RW					RO	WO	Ao	WO
Reset		1	1	0	0	0	0	0					1	0	0	0

Bit(s)	Mnemonic	Name	Description
14:12	**BSTSZ**	BURST_SIZE	**DMA burst size** Specifies the maximum transfer bytes allowed at the device per DMA burst. This field cannot be modified when the DMA status is 1. 3'd3: 8 bytes 3'd4: 16 bytes 3'd5: 32 bytes 3'd6: 64 bytes Other: Reserved
11	**SPLIT1K**	DMA_SPLIT_1K	**Specifies split burst when crossing 1K boundry address** 1'b0: 1K boundary is not split. 1'b1: 1K boundary is split.
10	**LASTBF**	LAST_BUF	**Last buffer of the basic DMA mode** Indicates the last buffer in the basic DMA mode.
9	**DMAALIGN**	DMA_ALIGN	**Specifies address aligment burst size** 1'b0: Not DAM burst size alignment 1'b1: DAM burst size alignment
8	**DMAMOD**	DMA_MODE	**DMA operation mode** Indicates operation mode of DMA. 1'b0: Basic DMA mode 1'b1: Descriptor base DMA mode
3	**READYM**	AHB_READYM	**Only for debugging when DMA hangs** SW checks if AHB bus is ok when GDMA hangs.
2	**DMARSM**	DMA_RESUME	**DMA resume control register** Resumes DMA transaction. Read always returns 0.
1	**DMASTOP**	DMA_STOP	**DMA stop control register** Stops DMA transaction. When SW issues STOP command, SW must wait for this bit to be de-asserted or DMA inactive to guarantee stop is done.
0	**DMASTART**	DMA_START	**DMA start control register** Starts DMA transaction. Read always returns 0.

1124009C DMA_CFG **DMA Configuration Register** **00000004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																DMA_CHK_SUM_12B
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MSDC_ACTIVE_EN				AHB_HPROT_2_EN							LOCK_DISABLE	DMA_DSCP_CS_EN	DMA_STATUS
Type			RW				RW							RW	RW	RU
Reset			0	0			0	0						1	0	0

Bit(s)	Mnemonic	Name	Description
16	**DMACHKSUM12B**	DMA_CHK_SUM_12 B	**Indicates GPD/BD checksum covers 16 bytes or 12 bytes** 1'b0: GPD/BD checksum covers 16 bytes. 1'b1: GPD/BD checksum only covers 12 bytes.
13:12	**MSDCACTIVEEN**	MSDC_ACTIVE_EN	**Indicates how to control msdc_active** 2'b00: Dynamic control msdc_active 2'b01: msdc_active = 0 2'b10: msdc_active = 1 2'b11: Reserved
9:8	**AHBHPROT2EN**	AHB_HPROT_2_EN	**Determines how to control hprot_2 pin of AHB bus** AHB_HPROT_2_EN = 2'b00 and basic DMA mode All the write transfers of a burst will be accessed by bufferable mode except for the last burst of DMA. AHB_HPROT2_2_EN=2'b00 and descriptor DMA mode All the write transfers of a burst will be accessed by bufferable mode except for HW own update transfer. 2'b00: Dynamic control hprot_2 2'b01: hprot_2 = 0 2'b10: hprot_2 = 1
2	**LOCKDISABLE**	LOCK_DISABLE	**Disables lock to improve EMI efficiency** 1'b0: Enable AHB lock 1'b1: Disable AHB lock
1	**DSCPCSEN**	DMA_DSCP_CS_EN	**Enables DMA descriptor checksum** This bit is used to enable or disable the descriptor checksum validation function for the descriptor. This field cannot be modified when the DMA status is 1.
0	**DMASTS**	DMA_STATUS	**DMA status** Indicates the status of DMA. 1'b0: DMA engine is inactive. 1'b1: DMA engine is active.

112400A0 SW_DBG_SEL **MSDC S/W Debug Selection Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_SEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**SWDBGSEL**	DBG_SEL	**Selects MSDC debugging** Reserved.

112400A4 SW_DBG_OUT — MSDC S/W Debug Output Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SWDBGO**	DBG_OUT	**MSDC debug output** 32-bit output selected by SW_DBG_SEL register

112400A8 DMA_LENGTH — DMA Length Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	XFER_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XFER_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**XFSZ**	XFER_SIZE	**DMA total transfer size** Specifies the number of DMA transfer byte required for the movement of source data through DMA. This field is only valid in basic DMA mode.

112400B0 PATCH_BIT0 — MSDC Patch Bit Register 0 — 403C0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_MMC_DRV_RESP	DETECT_WR_CRC_TIMEOUT	SPC_ALWAYS_PUSH	SDIO_INT_DLY_SEL	SDC_CMD_CMDFAIL_SEL	SDC_CMD_IDRT_SEL	SDC_CFG_WDOD				SDC_CFG_BSYDLY				SDIO_CFG_INTC_SEL	MSDC_BLKNUM_SEL

Type	RW	RW	RW	RW	RW	RW	RW				RW				RW	RW
Reset	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC_FIFO_RD_DIS						INT_DAT_LATCH_CK_SEL							DIS_REFLECT_CMDWR_WHEN_BSY	EN_SDC_ODD_8BIT_SUP	RALo
Type	RW						RW							RW	RW	RW
Reset	0						0	0	0					1	1	1

Bit(s)	Mnemonic	Name	Description
31	**PTCH31**	EN_MMC_DRV_RES P	**Enables MSDC always drives bus when outputting wake-up response (BREAK)** 1'b0: Disable 1'b1: Enable
30	**PTCH30**	DETECT_WR_CRC_ TIMEOUT	**Detects MSDC write data CRC phase timeout** 1'b0: Does not detect CRC phase timeout 1'b1: Detect CRC phase timeout
29	**PTCH29**	SPC_ALWAYS_PUS H	**SPC buffer push mechanism** 1'b0: Push the buffer only when read transfer is on-going 1'b1: Always push the buffer
28	**PTCH28**	SDIO_INT_DLY_S EL	**Selects SDIO interrupt latch time** 1'b0: Latch the data line value in internal SDIO interrupt period 1'b1: Latch the data line value in 1 clock delay of internal SDIO interrupt period
27	**PTCH27**	SDC_CMD_CMDFAI L_SEL	**Selects SDIO interrupt period recovery** 1'b0: SDIO interrupt period will re-start after a CMD12 or CMD52 command is issued. 1'b1: SDIO interrupt period whenever DAT line is not busy.
26	**PTCH26**	SDC_CMD_IDRT_S EL	**Selects SD identification response time** The register bit indicates if the command has a response with NID (i.e. 5 serial clock cycles as defined in SD memory card Specification Part 1 Physical Layer Specification version 1.0) response time. The register bit is valid only when the command has a response token. Thus, the register bit must be set to 1 for CMD2 (ALL_SEND_CID) and ACMD41 (SD_APP_OP_CMD). 1'b0: Otherwise 1'b1: The command has a response with NID response time.
25:22	**PTCH22**	SDC_CFG_WDOD	**SD write data output delay** The period from finish of the response for the initial host write command or the last write data block in a multiple block write operation to the start bit of the next write data block requires at least two serial clock cycles. The register field is used to extend the period (Write Data Output Delay) in unit of one serial clock. 4'b0000: No extension 4'b0001: Extend 1 more serial clock cycle 4'b0010: Extend 2 more serial clock cycles 4'b1111: Extend 15 more serial clock cycles
21:18	**PTCH18**	SDC_CFG_BSYDLY	**SD R1B busy detection mode** The register field is only valid for the commands with R1b response. If the command has a response of R1b

Bit(s)	Mnemonic	Name	Description
			type, MS/SD controller must monitor the data line 0 for card busy status from the bit time that is two serial clock cycles after the command end bit to check if operations in SD/MMC Memory Card have finished. The register field is used to expand the time between the command end bit and end of detection period to detect card busy status. If time is up and there is no card busy status on data line 0, then the controller will abandon the detection. 4'b0000: No extension 4'b0001: Extend 1 more serial clock cycle 4'b0010: Extend 2 more serial clock cycles 4'b1111: Extend 15 more serial clock cycles
17	**PTCH17**	SDIO_CFG_INTC_ SEL	**Selects SDIO interrupt mode** 1'b0: Only when data line [1] = 0 and then trigger SDIO interurpt event 1'b1: Only when data line [3:0] = 4'b1101 and then trigger SDIO interurpt event
16	**PTCH16**	MSDC_BLKNUM_SE L	**Supports ACMD23 reliable/force prog feature** 1'b0: Support ACMD23 reliable/force prog feature 1'b1: Does not support ACMD23 reliable/force prog feature
15	**PTCH15**	MSDC_FIFO_RD_D IS	**Disables MSDC RXFIFO read** 1'b0: Disable FIFO read permission to RXFIFO in PIO mode 1'b1: Enable FIFO read permission to RXFIFO in PIO mode
9:7	**INTCKS**	INT_DAT_LATCH_ CK_SEL	**Selects internal MSDC clock phase** Total 8 stages, each stage can delay 1 clock period of msdc_src_ck.
2	**PTCH02**	DIS_REFLECT_CM DWR_WHEN_BSY	**Enables SD command register write monitor** 1'b0: Enable monitor function 1'b1: Disable monitor function
1	**PTCH01**	EN_SDC_ODD_8BI T_SUP	**Enables SD odd number support for 8-bit data bus** 1'b0: Disable 1'b1: Enable
0		RAL0	

112400B4 PATCH_BIT1 **MSDC Patch Bit Register 1** **FFFE0009**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MSDC_CK_SHBFF_CKEN	MSDC_CK_RCTL_CKEN	MSDC_CK_WCTL_CKEN	MSDC_CK_SD_CKEN	MSDC_CK_ACMD_CKEN	MSDC_CK_VOLDET_CKEN	MSDC_CK_PSC_CKEN	MSDC_CK_SPC_CKEN	AHB_CK_GDMA_CKEN	RAL0			RAL1			ENABLE_SINGLE_BURST
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			RW			RW
Reset	1	1	1	1	1	1	1	1	1	1			1	1		0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESET_GDMA	RAL2	BIAS_EXTBIAS_28NM	BIAS_EN18IO_28NM	BIAS_TUNE_28NM				GET_CRC_MARG IN	GET_BUSY_MARGIN	CMD_RSP_TA_CN TR		WRDAT_CRCS_TA _CNTR			

Type	RW	RW	RW	RW	RW				RW	RW	RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
31	**MSHBFCKEN**	MSDC_CK_SHBFF_CKEN	**msdc_src_ck clock enable bit for SHBFF** 1'b0: Disable 1'b1: Enable
30	**MRCTLCKEN**	MSDC_CK_RCTL_CKEN	**msdc_src_ck clock enable bit for RCTL** 1'b0: Disable 1'b1: Enable
29	**MWCTLCKEN**	MSDC_CK_WCTL_CKEN	**msdc_src_ck clock enable bit for WCTL** 1'b0: Disable 1'b1: Enable
28	**MSDCKEN**	MSDC_CK_SD_CKE N	**msdc_src_ck clock enable bit for SD** 1'b0: Disable 1'b1: Enable
27	**MACMDCKEN**	MSDC_CK_ACMD_CKEN	**msdc_src_ck clock enable bit for ACMD** 1'b0: Disable 1'b1: Enable
26	**MVOLDTCKEN**	MSDC_CK_VOLDET_CKEN	**msdc_src_ck clock enable bit for VOLDET** 1'b0: Disable 1'b1: Enable
25	**MPSCCKEN**	MSDC_CK_PSC_CKEN	**msdc_src_ck clock enable bit for PSC** 1'b0: Disable 1'b1: Enable
24	**MSPCCKEN**	MSDC_CK_SPC_CKEN	**msdc_src_ck clock enable bit forSPC** 1'b0: Disable 1'b1: Enable
23	**HGDMACKEN**	AHB_CK_GDMA_CKEN	**hclk_ck clock enable bit for GDMA** 1'b0: Disable 1'b1: Enable
22		RAL0	
19:18		RAL1	
16	**SINGLEBURST**	ENABLE_SINGLE_BURST	**AHB bus will not support incr1 burst type in the future. This will only affect AHB bus MSDC design, not AXI bus design.** 1'b0: HW will send incr1 burst type. 1'b1: HW will send single burst type instead of incr1 type.
15	**RESETGDMA**	RESET_GDMA	**SW can reset GDMA when design hangs.** 1'b1: Reset GDMA 1'b0: Does not reset GDMA
14		RAL2	
13	**BIAS28R0**	BIAS_EXTBIAS_28NM	**28NM BIAS controller register 0**
12	**BIAS28R1**	BIAS_EN18IO_28 NM	**28NM BIAS controller register 1**
11:8	**BIAS28R2**	BIAS_TUNE_28NM	**28NM BIAS controller register 2**
7	**GETCRCMARGIN**	GET_CRC_MARGIN	**Adds margin to get CRC status when card resp CRC does not match spec 2 cycle from endbit** 1'b0: 8 cycles reserved to get CRC status from write data CRC endbit 1'b1: 16 cycles reserved to get CRC status from write data CRC endbit
6	**GETBUSYMARGIN**	GET_BUSY_MARGI N	**Adds margin to get busy state of data0** 1'b0: 1 cycle reserved to get busy state from SRC status endbit 1'b1: 3 cycles reserved to get busy state from SRC status endbit
5:3	**CMDTA**	CMD_RSP_TA_CNT R	**CMD response turn around period**

Bit(s)	Mnemonic	Name	Description
2:0	**WRTA**	WRDAT_CRCS_TA_CNTR	Turn around cycle = CMD_RSP_TA_CNTR + 2 In USH104 mode, this register should be set to 1. In non-UHS104 mode, this register should be set to 0. **Write data and CRC status turn around period** Turn around cycle = WRDAT_CRCS_TA_CNTR + 2 In USH104 mode, this register should be set to 1. In non-UHS104 mode,this register should be set to 0.

112400B8 PATCH_BIT2 **MSDC Patch Bit Register 2** **14801801**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRCSTS_LATCH_EN_SEL			CFG_CRCSTS	CFG_CRCSTS_CNT		CFG_CRCSTS_EDGE	CFG_CRCSTS_SEL	POP_EN_CNT				RALo	RESP_LATCH_EN_SEL		
Type	RW			RW	RW		RW	RW	RW				RW	RW		
Reset	0	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG_RESP	CFG_RESP_CNT			INTC_RESP_SEL	RAL1	CFG_RDAT	CFG_RDAT_CNT					RESP_WAIT_CNT		SUPPORT_64G	ENHANCE_WAIT_GPD
Type	RW	RW			RW	RW	RW	RW					RW		RW	RW
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:29	**CRCSTSENSEL**	CRCSTS_LATCH_EN_SEL	**Configures latch CRC status enable signal for async FIFO in eMMC45** 3'b000: Latch CRC status enable signal does not delay. 3'b001: Latch CRC status enable signal delays 1T msdc_ck. 3'b010: Latch CRC status enable signal delays 2T msdc_ck. 3'b011: Latch CRC status enable signal delays 3T msdc_ck. 3'b111: Latch CRC status enable signal delays 7T msdc_ck.
28	**CFGCRCSTS**	CFG_CRCSTS	**Configures CRC status path selection** This setting only uses eMMC4.5 feature. 1'b0: Latch CRC status select delay-line path 1'b1: Latch CRC status select async FIFO path
27:26	**CFGCRCSTSCNT**	CFG_CRCSTS_CNT	**Configures the number of data pushed in async FIFO until starting to pop out data from async FIFO** Min. setting: 1. Do not set it to 0. This setting only uses eMMC4.5 feature. 2'b00: Push 0 data in async FIFO when starting to pop out data from async FIFO 2'b01: Push 1 data in async FIFO when starting to pop out data from async FIFO 2'b10: Push 2 data in async FIFO when starting to pop out data from async FIFO 2'b11: Push 3 data in async FIFO when starting to pop out data from async FIFO
25	**CFGCRCSTSEDGE**	CFG_CRCSTS_EDG E	**Configures to use rising async FIFO or falling async FIFO** 1'b0: Async FIFO latch CRC status uses rising async FIFO. 1'b1: Async FIFO latch CRC status uses falling async

Bit(s)	Mnemonic	Name	Description
			FIFO.
24		CFG_CRCSTS_SEL	**Configures async FIFO path selection** 1'b0: Use normal path in async FIFO 1'b1: Use 2DFF path in async FIFO
23:20	**POPENCNT**	POP_EN_CNT	**Pop enable counter** Defines how many write pointer and the read pointer margins begin to pop data transfer
19		RAL0	
18:16	**RESPSTSENSEL**	RESP_LATCH_EN_SEL	**Configures latch CMD response enable signal for async FIFO in eMMC45** 3'b000: Latch CMD response enable signal does not delay. 3'b001: Latch CMD response enable signal delays 1T msdc_ck. 3'b010: Latch CMD response enable signal delays 2T msdc_ck. 3'b011: Latch CMD response enable signal delays 3T msdc_ck. 3'b111: Latch CMD response enable signal delays 7T msdc_ck.
15	**CFGRESP**	CFG_RESP	**Configures CMD response path selection** This setting only uses eMMC4.5 feature. 1'b0: Latch CMD response select async FIFO path 1'b1: Latch CMD response select delay-line path
14:12	**CFGRESPCNT**	CFG_RESP_CNT	**Configures the number of data pushed in async FIFO until starting to pop out data from async FIFO** Min. setting: 1. Do not set it to 0. This setting only uses eMMC4.5 feature. 3'b000: Push 0 data in async FIFO when starting to pop out data from async FIFO 3'b001: Push 1 data in async FIFO when starting to pop out data from async FIFO 3'b111: Push 7 data in async FIFO when starting to pop out data from async FIFO
11	**INTCRESPSEL**	INTC_RESP_SEL	**Configures BREAK command async FIFO path** 1'b0: Use normal path in async FIFO 1'b1: Use 2DFF path in async FIFO
10		RAL1	
9	**CFGRDAT**	CFG_RDAT	**Configures read data path** 1'b0: Read data path bypasses delay line 1'b1: Read data path through delay line
8:4	**CFGRDATCNT**	CFG_RDAT_CNT	**Configures read data path delay line**
3:2	**RESPWAITCNT**	RESP_WAIT_CNT	**Configures CMD response timeout** Timeout cycle = 65T + 16*RESP_WAIT_CNT 2'b00: CMD response timeout is 65T. 2'b01: CMD response timeout is 65T+16*1T. 2'b01: CMD response timeout is 65T+16*2T. 2'b01: CMD response timeout is 65T+16*3T.
1	**SUPPORT64G**	SUPPORT_64G	**Supports high 64G DRAM space access or not** 1'b1: Support 64G DRAM access 1'b0: Does not support 64G DRAM access
0	**ENHANCEGPD**	ENHANCE_WAIT_GPD	**If SW clears int when GPD update is not finished, design will hang.** Set this bit to 1 to avoid this issue in enhance write mode. 1'b1: Use new HW code for updating GPD in enhance mode 1'b0: Use old HW code

Bit(s)	Mnemonic	Name	Description

112400C0 DAT0_TUNE_CRC **DAT0 Tune Result Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112400C4 DAT1_TUNE_CRC **DAT1 Tune Result Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112400C8 DAT2_TUNE_CRC **DAT2 Tune Result Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112400CC DAT3_TUNE_CRC **DAT3 Tune Result Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112400D0 CMD_TUNE_CRC — **CMD Tune Result Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112400D4 SDIO_TUNE_WIND — **SDIO Tune Window Register 0** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112400F0 DAT_RD_DLY — **MSDC Data Delay Line Register 0** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT0_RD_DLY								DAT1_RD_DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT2_RD_DLY								DAT3_RD_DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT0RDDLY**	DAT0_RD_DLY	**Controls DAT0 pad RX delay line (for MSDC RD)** Total 32 stages.
20:16	**DAT1RDDLY**	DAT1_RD_DLY	**Controls DAT1 pad RX delay line (for MSDC RD)** Total 32 stages.
12:8	**DAT2RDDLY**	DAT2_RD_DLY	**Controls DAT2 pad RX delay line (for MSDC RD)** Total 32 stages.
4:0	**DAT3RDDLY**	DAT3_RD_DLY	**Controls DAT3 pad RX delay line (for MSDC RD)** Total 32 stages.

112400F4 DAT_RD_DLY1 **MSDC Data Delay Line Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT4_RD_DLY										RAL0	DAT6_RD_DLY				
Type	RO										RW	RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RAL1		RAL2	DAT7_RD_DLY					RAL3							
Type	RO		RW	RW					RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:22	**DAT4RDDLY**	DAT4_RD_DLY	**Controls DAT4 pad RX delay line (for MSDC RD)** Total 32 stages.
21	**DAT5RDDLY**	RAL0	**Controls DAT5 pad RX delay line (for MSDC RD)** Total 32 stages.
20:16	**DAT6RDDLY**	DAT6_RD_DLY	**Controls DAT6 pad RX delay line (for MSDC RD)** Total 32 stages.
15:14		RAL1	
13		RAL2	
12:8	**DAT7RDDLY**	DAT7_RD_DLY	**Controls DAT7 pad RX delay line (for MSDC RD)** Total 32 stages.
7:0		RAL3	

112400F8 HW_DBG_SEL **MSDC H/W Debug Selection Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RAL0			HW_DBG3_SEL					RAL1			HW_DBG2_SEL				
Type	RO			RW					RO			RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RAL2			HW_DBG1_SEL					RAL3			HW_DBG0_SEL				
Type	RO			RW					RO			RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
31:29	**DBGWSEL**	RAL0	**Selects HW debug output for wrapper** 0: Original debug pins 1: Wrapper debug pins
28:24 23:21	**DBG3SEL**	HW_DBG3_SEL RAL1	**Selects HW debug output**
20:16 15:13	**DBG2SEL**	HW_DBG2_SEL RAL2	**Selects HW debug output**
12:8 7:5	**DBG1SEL**	HW_DBG1_SEL RAL3	**Selects HW debug output**
4:0	**DBG0SEL**	HW_DBG0_SEL	**Selects HW debug output**

11240100 MAIN_VER MSDC Main Version Register 20140512

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAIN_VER															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAIN_VER															
Type	RO															
Reset	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
31:0	**MAINVER**	MAIN_VER	Main version

11240104 ECO_VER MSDC ECO Version Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ECO_VER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ECO_VER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ECOVER**	ECO_VER	ECO version

Module name: MSDC2 Base address: (+11250000h)

Address	Name	Width	Register Function
11250000	**MSDC_CFG**	32	MSDC Configuration Register
11250004	**MSDC_IOCON**	32	MSDC IO Configuration Register
11250008	**MSDC_PS**	32	MSDC Pin Status Register
1125000C	**MSDC_INT**	32	MSDC Interrupt Register
11250010	**MSDC_INTEN**	32	MSDC Interrupt Enable Register
11250014	**MSDC_FIFOCS**	32	MSDC FIFO Control and Status Register
11250018	**MSDC_TXDATA**	32	MSDC TX Data Port Register

Address	Name	Width	Register Function
1125001C	MSDC_RXDATA	32	MSDC RX Data Port Register
11250030	SDC_CFG	32	SD Configuration Register
11250034	SDC_CMD	32	SD Command Register
11250038	SDC_ARG	32	SD Argument Register
1125003C	SDC_STS	32	SD Status Register
11250040	SDC_RESP0	32	SD Response Register 0
11250044	SDC_RESP1	32	SD Response Register 1
11250048	SDC_RESP2	32	SD Response Register 2
1125004C	SDC_RESP3	32	SD Response Register 3
11250050	SDC_BLK_NUM	32	SD Block Number Register
11250054	SDC_VOL_CHG	32	SD Voltage Change Wait Time Register
11250058	SDC_CSTS	32	SD Card Status Register
1125005C	SDC_CSTS_EN	32	SD Card Status Enable Register
11250060	SDC_DATCRC_STS	32	SD Card Data CRC Status Register
11250080	SD_ACMD_RESP	32	SD ACMD Response Register
11250084	SD_ACMD19_TRG	32	SD ACMD19 Target Register
11250088	SD_ACMD19_STS	32	SD ACMD19 Status Register
1125008C	DMA_SA_HIGH4BIT	32	DMA Current Address Resgiter of High 4 Bits
11250090	DMA_SA	32	DMA Start Address Register
11250094	DMA_CA	32	DMA Current Address Register
11250098	DMA_CTRL	32	DMA Control Register
1125009C	DMA_CFG	32	DMA Configuration Register
112500A0	SW_DBG_SEL	32	MSDC S/W Debug Selection Register
112500A4	SW_DBG_OUT	32	MSDC S/W Debug Output Register
112500A8	DMA_LENGTH	32	DMA Length Register
112500B0	PATCH_BIT0	32	MSDC Patch Bit Register 0
112500B4	PATCH_BIT1	32	MSDC Patch Bit Register 1
112500B8	PATCH_BIT2	32	MSDC Patch Bit Register 2
112500C0	DAT0_TUNE_CRC	32	DAT0 Tune Result Register
112500C4	DAT1_TUNE_CRC	32	DAT1 Tune Result Register
112500C8	DAT2_TUNE_CRC	32	DAT2 Tune Result Register
112500CC	DAT3_TUNE_CRC	32	DAT3 Tune Result Register
112500D0	CMD_TUNE_CRC	32	CMD Tune Result Register
112500D4	SDIO_TUNE_WIND	32	SDIO Tune Window Register 0
112500F0	DAT_RD_DLY0	32	MSDC Data Delay Line Register 0
112500F4	DAT_RD_DLY1	32	MSDC Data Delay Line Register 1
112500F8	HW_DBG_SEL	32	MSDC H/W Debug Selection Register
11250100	MAIN_VER	32	MSDC Main Version Register
11250104	ECO_VER	32	**MSDC ECO Version Register**

11250000 MSDC_CFG MSDC Configuration Register 02000099

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CARD_CK_D IV			
Type													RW			

Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CARD_CK_DIV								CARD_CK_STABLE			CARD_CK_DRV_EN	PIO_MODE	RST	CARD_CK_PWDN	MSDC
Type	RW								RU			RW	RW	A0	RW	RW
Reset	0	0	0	0	0	0	0	0	1			1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
19:8	**CCKDIV**	CARD_CK_DIV	**MS/SD card clock divider** Controls clock frequency of serial clock on MS/SD bus. Refer to "Data Line Latching Timing Diagram" and "Response Latching Timing Diagram". For non-DDR mode, msdc_ck equals SD bus clock. (Example: For SDR25 or HS, msdc_ck and SD bus clock will be 50MHz.) For DDR mode, msdc_ck denotes the MSDC internal clock which will be dobuled to SD bus clock. (Example: For DDR50, msdc_ck should be set to 100MHz, and bus clock will be 50MHz.) 8'b00000000: msdc_ck = (1/2)*msdc_src_ck 8'b00000001: msdc_ck = [1/(4*1)]*msdc_src_ck 8'b00000010: msdc_ck = [1/(4*2)]*msdc_src_ck 8'b00000011: msdc_ck = [1/(4*3)]*msdc_src_ck 8'b00010000: msdc_ck = [1/(4*16)]*msdc_src_ck 8'b11111111: msdc_ck = [1/(4*255)]*msdc_src_ck
7	**CCKSB**	CARD_CK_STABLE	**MS/SD card clock is stable or not** After programming CARD_CK_MODE or CARD_CK_DIV, this bit will immediately become 0 and return to 1 if stable. Poll this register to ensure safety control of MSDC. 1'b0: Clock output is not stable. 1'b1: Clock output is stable.
4	**CCKDRVE**	CARD_CK_DRV_EN	**SD/MS card bus clock drive enable bit** Set this bit to 1 to enable MSDC bus clock driver. The default bus state depends on MSDC_CFG][1] CARD_CK_PWDN bit. If MSDC_CFG[1] CARD_CK_PWDN= 1, the default clock state will be free running. If MSDC_CFG[1] CARD_CK_PWDN = 0, the default clock state will be gated to 0. Set this bit to 0 to put the bus state into "tri-state". Default: 1 1'b0: Put the clock pad into tri-state 1'b1: Enable MSDC to drive clock pad; the state of CLK depends on MSDC_CFG[1] CARD_CK_PWDN.
3	**PIO**	PIO_MODE	**MS/SD PIO mode** Selects PIO mode Default: PIO mode 1'b0: DMA mode 1'b1: PIO mode
2	**RST**	RST	**Software reset** Writing 1 to this register will cause internal synchronous reset of MS/SD controller, and it will not reset register settings and DMA controller. The reset sequence is done when this bit becomes 0. SW should wait this bit to return to 0 after writing 1. 1'b0: MS/SD controller is not in reset state. 1'b1: MS/SD controller is in reset state.

Bit(s)	Mnemonic	Name	Description
1	**CCKPD**	CARD_CK_PWDN	**MSDC bus clock power-down mode** Controls card clock power-down mode. 1'b0: Clock is gated to 0 if no command or data is transmitted. 1'b1: Clock is free running even if no command or data is transmitted. (The clock may still be stopped when MSDC write data are not enough or no space for the next read data.)
0	**MSDC**	MSDC	**Selects MS/SD mode** Configures the controller as the host of memory stick or as the host of SD/MMC memory card. The default value is configuring the controller as the host of memory stick. 1'b0: Configure the controller as the host of memory stick 1'b1: Configure the controller as the host of SD/MMC memory card

11250004 MSDC_IOCON MSDC IO Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									R_D7_SMPL	R_D6_SMPL	R_D5_SMPL	R_D4_SMPL	R_D3_SMPL	R_D2_SMPL	R_D1_SMPL	R_D0_SMPL
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			W_D3_SMPL	W_D2_SMPL	W_D1_SMPL	W_D0_SMPL	W_D_SMPL_SEL	W_D_SMPL			R_D_SMPL_SEL		D_DLYLINE_SEL	R_D_SMPL	R_SMPL	SDR104_CLK_SEL
Type			RW	RW	RW	RW	RW	RW			RW		RW	RW	RW	RW
Reset			0	0	0	0	0	0			0		0	0	0	0

Bit(s)	Mnemonic	Name	Description
23	**RD7SPL**	R_D7_SMPL	**Selects read data 7 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
22	**RD6SPL**	R_D6_SMPL	**Selects read data 6 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
21	**RD5SPL**	R_D5_SMPL	**Selects read data 5 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
20	**RD4SPL**	R_D4_SMPL	**Selects read data 4 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
19	**RD3SPL**	R_D3_SMPL	**Selects read data 3 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
18	**RD2SPL**	R_D2_SMPL	**Selects read data 2 sample** This bit is only valid when bit 5 is on.

Bit(s)	Mnemonic	Name	Description
			1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
17	**RD1SPL**	R_D1_SMPL	**Selects read data 1 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
16	**RD0SPL**	R_D0_SMPL	**Selects read data 0 sample** This bit is only valid when bit 5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
13	**WD3SPL**	W_D3_SMPL	**Selects SDIO interrupt sample** This bit is only valid when bit 9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
12	**WD2SPL**	W_D2_SMPL	**Selects SDIO interrupt sample** This bit is only valid when bit 9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
11	**WD1SPL**	W_D1_SMPL	**Selects SDIO interrupt sample** This bit is only valid when bit 9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
10	**WD0SPL**	W_D0_SMPL	**Selects CRC status and SDIO interrupt sample** This bit is only valid when bit 9 is on. 1'b0: Sample CRC Status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC Status and SDIO interrupt by external bus clock falling edge
9	**WDSPLSEL**	W_D_SMPL_SEL	**Selects data line rising/falling latch fine-tuning in write transaction** 1'b0: All data line share one value indicated by MSDC_IOCON.W_D_SMPL 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.W_D0_SMPL Data line 1: MSDC_IOCON.W_D1_SMPL Data line 2: MSDC_IOCON.W_D2_SMPL Data line 3: MSDC_IOCON.W_D3_SMPL
8	**WDSPL**	W_D_SMPL	**Selects CRC status and SDIO interrupt sample** 1'b0: Sample CRC Status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC Status and SDIO interrupt by external bus clock falling edge
5	**RDSPLSEL**	R_D_SMPL_SEL	**Selects data line rising/falling latch fine-tuning in read transaction** 1'b0: All data line share one value indicated by MSDC_IOCON.R_D_SMPL 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.R_D0_SMPL Data line 1: MSDC_IOCON.R_D1_SMPL Data line 2: MSDC_IOCON.R_D2_SMPL Data line 3: MSDC_IOCON.R_D3_SMPL

Bit(s)	Mnemonic	Name	Description
			Data line 4: MSDC_IOCON.R_D4_SMPL Data line 5: MSDC_IOCON.R_D5_SMPL Data line 6: MSDC_IOCON.R_D6_SMPL Data line 7: MSDC_IOCON.R_D7_SMPL
3	**DDLSEL**	D_DLYLINE_SEL	**Selects data line delay line fine-tuning** 1'b0: All data line share one delay selection value indicated by PAD_TUNE.PAD_DAT_RD_RXDLY 1'b1: Each data line has its own delay selection value indicated by Data line 0: DAT_RD_DLY0.DAT0_RD_DLY Data line 1: DAT_RD_DLY0.DAT1_RD_DLY Data line 2: DAT_RD_DLY0.DAT2_RD_DLY Data line 3: DAT_RD_DLY0.DAT3_RD_DLY Data line 4: DAT_RD_DLY1.DAT4_RD_DLY Data line 5: DAT_RD_DLY1.DAT5_RD_DLY Data line 6: DAT_RD_DLY1.DAT6_RD_DLY Data line 7: DAT_RD_DLY1.DAT7_RD_DLY
2	**RDSPL**	R_D_SMPL	**Selects read data sample** 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
1	**RSPL**	R_SMPL	**Selects command response sample** 1'b0: Sample response by external bus clock rising edge 1'b1: Sample response by external bus clock falling edge
0	**SDR104CKS**	SDR104_CLK_SEL	**SDR104 SCLK output clock control** Only used when MSDC_CFG[17:16] CARD_CK_MODE is 2'b01. 1'b0: Bus clock output equals inverted msdc_src_ck 1'b1: Bus clock output equals msdc_src_ck

11250008 MSDC_PS MSDC Pin Status Register 81FF0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SD_WP							CMD	DAT							
Type	RU							RU	RU							
Reset	1							1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDDEBOUNCE														CDSTS	CDEN
Type	RW														RU	RW
Reset	0	0	0	0											1	0

Bit(s)	Mnemonic	Name	Description
31	**SDWP**	SD_WP	**Write Protection switch status on SD memory card** Shows the status of Write Protection switch on SD memory card. There is no default reset value. The pin WP (Write Protection) is only useful when the controller is configured for SD memory card. 1'b0: Write Protection switch on. Memory card is desired to be write-protected. 1'b1: Write Protection switch off. Memory card is writable.
24	**CMD**	CMD	**Command line status** Reflects the command line value of MSDC bus.

Bit(s)	Mnemonic	Name	Description
23:16	**DAT**	DAT	**Data line status** Reflects the data line value of MSDC bus (8-bit).
15:12	**CDDBCE**	CDDEBOUNCE	**Card detection de-bounce timer** Specifies time interval for card detection de-bounce. Default value: 0, meaning the de-bounce interval is one 32kHz cycle. The interval will extend one cycle time of 32kHz by increasing the counter by 1.
1	**CDSTS**	CDSTS	**Card detection status** 1'b1: Card detection pin status is logic high.
0	**CDEN**	CDEN	**Enables card detection** Controls card detection circuit. 1'b0: Disable card detection 1'b1: Enable card detection

1125000C MSDC_INT **MSDC Interrupt Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													DMA_PROTECT	GPD_CS_ERR	BD_CS_ERR	
Type													W1C	W1C	W1C	
Reset													0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SD_DATA_CRCERR	SD_DATTO	DMA_XFER_DONE	SD_XFER_COMPLETE	SD_CSTS	SD_RESP_CRCERR	SD_CMDTO	SD_CMDRDY		DMA_Q_EMPTY	SD_AUTOCMD_RESP_CRCERR	SD_AUTOCMD_CMDTO	SD_AUTOCMD_CMDRDY		MSDC_CDSC	MMC_IRQ
Type	W1C	W1C	W1C	W1C	RU	W1C	W1C	W1C		W1C	W1C	W1C	W1C		W1C	W1C
Reset	0	0	0	0	0	0	0	0		0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
19	**DMAPROTECT**	DMA_PROTECT	**There is write operation to DMA start address, length, start bit or the last buf bit.**
18	**GPDCSERR**	GPD_CS_ERR	**GPD checksum error detected**
17	**BDCSERR**	BD_CS_ERR	**BD checksum error detected**
15	**SDDCRCERR**	SD_DATA_CRCERR	**SD data CRC error interrupt** Indicates MS/SD controller detects a CRC error after reading a block of data from the DAT line or SD/MMC signals a CRC error after writing a block of data to the DAT line. 1'b0: Otherwise 1'b1: MS/SD controller detects a CRC error after reading a block of data from the DAT line or SD/MMC signals a CRC error after writing a block of data to the DAT line.
14	**SDDTO**	SD_DATTO	**SD data timeout interrupt** Indicates SD/MMC controller detects a timeout condition while waiting for data token on the DAT line. This bit is for both data read and data write. For SD data read, timeout will occur when the read data are not presented. For SD data write, timeout will occur when the write data CRC status is not presented if PATCH_BIT[30] DETECT_WR_CRC_TIMEOUT = 1.

Bit(s)	Mnemonic	Name	Description
			1'b0: Otherwise 1'b1: SD/MMC controller detects a timeout condition while waiting for data token on the DAT line.
13	**DMAXFDNE**	DMA_XFER_DONE	**DMA transfer done interrupt** Indicates status of data block transfer. 1'b0: Otherwise 1'b1: A data block is successfully transferred.
12	**SDXFCPL**	SD_XFER_COMPLETE	**SD data transfer completed interrupt** Indicates transaction which contains data that are completed. While performing tuning procedure (Execute Tuning is set to 1), SD_XFER_COMPLETE is not set to 1.
11	**SDCSTS**	SD_CSTS	**SD CSTA update interrupt** Indicates any bit in register SDC_CSTA is active. The register bit will be set to 1. SW should clear SDC_CSTA, and this bit will be de-asserted automatically. 1'b0: No SD memory card interrupt 1'b1: SD memory card interrupt exists.
10	**SDRCRCER**	SD_RESP_CRCERR	**SD command CRC error interrupt** Indicates SD/MMC controller detects a CRC error after reading a response from the CMD line. 1'b0: Otherwise 1'b1: SD/MMC controller detects a CRC error after reading a response from the CMD line.
9	**SDCTO**	SD_CMDTO	**SD command timeout interrupt** Indicates SD/MMC controller detects a timeout condition while waiting for a response on the CMD line. 1'b0: Otherwise 1'b1: SD/MMC controller detects a timeout condition while waiting for a response on the CMD line.
8	**SDCRDY**	SD_CMDRDY	**SD command ready interrupt** For the command without response, the register bit will be 1 once the command is completed on SD/MMC bus. For command with response without busy, the register bit will be 1 whenever the command is issued onto SD/MMC bus and its corresponding response is received without CRC error. For command with response with busy in DAT0, the register bit will be 1 whenever the command is issued onto SD/MMC bus and its corresponding response is received without CRC error and the DAT0 transited from busy to idle. 1'b0: Otherwise 1'b1: Command finished successfully without a CRC error
6	**DMAQEPTY**	DMA_Q_EMPTY	**DMA queue empty interrupt** Indicates the current DMA queue is empty. Only for descriptor mode and enhance mode.
5	**SDACDRCRCER**	SD_AUTOCMD_RESP_CRCERR	**SD auto command CRC error interrupt** Set when detecting a CRC error in the auto command response.
4	**SDACDCTO**	SD_AUTOCMD_CMDTO	**SD auto command timeout interrupt** Set if no response is returned within a specified cycles (64T in spec) from the end bit of auto command.
3	**SDACDCRDY**	SD_AUTOCMD_CMDRDY	**SD auto command ready interrupt** Set if auto command is executed without CRC error or timeout.
1	**MSDCCDSC**	MSDC_CDSC	**MSDC card detection status change interrupt** Indicates if any interrupt for memory card insertion/removal exists. Whenever memory card is

Bit(s)	Mnemonic	Name	Description
			inserted or removed and card detection circuit is enabled, i.e. register bit CDEN in register MSDC_PS is set to 1, the register bit will be set to 1. It will be reset when the register is read. 1'b0: Otherwise 1'b1: Card is inserted or removed.
0	**MMCIRQ**	MMC_IRQ	**MMC card interrupt** 1'b0: Otherwise 1'b1: MMC card interrupt event occurs.

11250010 MSDC_INTEN MSDC Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													ENDMAPROTECT	ENGPDCSERR	ENBDCSERR	
Type													RW	RW	RW	
Reset													0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENSDDATACRCERR	ENSDDATTO	ENSDDMA_XFER_DONE	ENSDXFER_COMPL ETE	ENSDCSTA	ENSDRESP_CRCERR	ENSDCMDTO	ENSDCMDRDY	ENSDSDIOIRQ	ENDMAQ_EMPTY	ENSDAUTOCMD_RESP_CRCERR	ENSDAUTOCMD_CMDTO	ENAUTOCMD_CMDRD Y		ENMSDC_CDSC	ENMMC_IRQ
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
19	**ENDMAPROTECT**	EN_DMA_PROTECT	**Enables DMA protection interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
18	**ENGPDCSERR**	EN_GPD_CS_ERR	**Enables GPD checksum error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
17	**ENBDCSERR**	EN_BD_CS_ERR	**Enables BD checksum error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
15	**ENSDDCRCERR**	EN_SD_DATA_CRC ERR	**Enables SD data CRC error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
14	**ENSDDTO**	EN_SD_DATTO	**Enables SD data timeout interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
13	**ENDMAXFDNE**	EN_SD_DMA_XFER _DONE	**Enables DMA transfer done interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
12	**ENSDXFCPL**	EN_SD_XFER_COM PLETE	**Enables SD data transfer completed interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
11	**ENSDCSTA**	EN_SD_CSTA	**Enables SD CSTA update interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt

Bit(s)	Mnemonic	Name	Description
10	**ENSDRCRCER**	EN_SD_RESP_CRC ERR	**Enables SD command CRC error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
9	**ENSDCTO**	EN_SD_CMDTO	**Enables SD command timeout interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
8	**ENSDCRDY**	EN_SD_CMDRDY	**Enables SD command ready interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
7	**ENSDIOIRQ**	EN_SD_SDIOIRQ	**Enables SD SDIO interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
6	**ENDMAQEPTY**	EN_DMA_Q_EMPTY	**Enables DMA queue empty interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
5	**ENSDACDRCRCER**	EN_SD_AUTOCMD_ RESP_CRCERR	**Enables SD auto command CRC error interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
4	**ENSDACDCTO**	EN_SD_AUTOCMD_ CMDTO	**Enables SD auto command timeout interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
3	**ENSDACDCRDY**	EN_AUTOCMD_CMD RDY	**Enables SD auto command ready interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
1	**ENMSDCCDSC**	EN_MSDC_CDSC	**Enables MSDC card detection status change interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt
0	**ENMMCIRQ**	EN_MMC_IRQ	**Enables MMC card interrupt** 1'b0: Disable interrupt 1'b1: Enable interrupt

11250014 MSDC_FIFOCS MSDC FIFO Control and Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFOCLR								TXFIFOCNT							
Type	A0								RU							
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RXFIFOCNT							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**FIFOCLR**	FIFOCLR	**Clears embedded FIFO** Write 1 to this bit to clear FIFO. It will become 0 when FIFO is cleared. SW needs to check this bit to make sure clearing FIFO sequence is done. This bit can be used when the data read/write sequence has error and needs to clear HW FIFO.
23:16	**TXFIFOCNT**	TXFIFOCNT	**TX FIFO count for MSDC write**

Bit(s)	Mnemonic	Name	Description
			8'd0: No data in FIFO 8'd1: 1-byte data in FIFO 8'd2: 2-byte data in FIFO 8'd131: Max. 131-byte data in FIFO Others: Reserved
7:0	**RXFIFOCNT**	RXFIFOCNT	**RX FIFO count for MSDC read** 8'd0: No data in FIFO 8'd1: 1-byte data in FIFO 8'd2: 2-byte data in FIFO 8'd131: Max. 131-byte data in FIFO Others: Reserved

11250018 MSDC_TXDATA MSDC TX Data Port Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PIO_TXDATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIO_TXDATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PIOTXDATA**	PIO_TXDATA	**PIO mode TXDATA port** This register can be accessed by byte, half-word or word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

1125001C MSDC_RXDATA MSDC RX Data Port Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PIO_RXDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIO_RXDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PIORXDATA**	PIO_RXDATA	**PIO mode RXDATA port** This register can be accessed by byte, half-word or word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

11250030 SDC_CFG SD Configuration Register 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	DTOC										INT_AT_BLOCK_GAP	SDIO_INT_DET_EN	SDIO		BUSWIDTH	
Type	RW										RW	RW	RW		RW	
Reset	0	0	0	0	0	0	0	0			0	1	0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															WAKEUP_INS_EN	WAKEUP_SDIOINT_EN
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DTOC**	DTOC	**Data timeout counter** The period from the end of the initial host read command or the last read data block in a multiple block read operation to the start bit of the next read data block requires at least two serial clock cycles. The counter is used to extend the period (Read Data Access Time) in unit of 1,048,576 serial clocks. 8'b00000000: Extend 1,048,576 more serial clock cycles 8'b00000001: Extend 1,048,576*2 more serial clock cycles 8'b00000010: Extend 1,048,576*3 more serial clock cycles 8'b11111111: Extend 1,048,576*256 more serial clock cycles
21	**INTBGP**	INT_AT_BLOCK_G AP	**Interrupt at block gap** This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Set to 1 to enable interrupt detection at the block gap for a multiple block transfer. Set to 0 to disable interrupt detection during a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the host driver detects an SD card insertion, it will set up this bit according to the CCCR of the SDIO card. 1'b0: Disable interrupt detection at block gap 1'b1: Enable interrupt detection at block gap
20	**SDIOIDE**	SDIO_INT_DET_E N	**Enables SDIO interrupt detection** Informs SD controller to sense the SDIO interrupt. 1'b0: Disable SDIO interrupt detection 1'b1: Enable SDIO interrupt detection if the SDIO bit is also on
19	**SDIO**	SDIO	**SDIO mode enable bit** Enables support to sense the SDIO interrupt and disables R4 response CRC check for SDIO card. 1'b0: Disable SDIO mode 1'b1: Enable SDIO mode
17:16	**BUSWD**	BUSWIDTH	**Configures bus width** Defines SD/MMC bus width. 2'b00: 1 bit mode 2'b01: 4 bit mode 2'b10: 8 bit mode 2'b11: Reserved
1	**ENWKUPINS**	WAKEUP_INS_EN	**Card status change wakeup event enable bit**

Bit(s)	Mnemonic	Name	Description
0	**ENWKUPSDIOINT**	WAKEUP_SDIOINT_EN	1'b0: Disable wakeup event for card status change 1'b1: Enable wakeup event for card status change **SDIO card interrupt wakeup event enable bit** 1'b0: Disable wakeup event for SDIO card interrupt 1'b1: Enable wakeup event for SDIO card interrupt

11250034 SDC_CMD SD Command Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LEN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GO_IRQ	STOP	RW	DTYPE			RSPTYP			BREAK	CMD					
Type	RW	RW	RW	RW			RW			RW	RW					
Reset	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**LEN**	LEN	**Length** Defines the length of one block (unit: byte) in a data transaction of block mode or the data length (unit: byte) in data transaction of byte mode. The maximal value of block length is 2,048 bytes. 12'b000000000000: Reserved 12'b000000000001: Block length is 1 byte 12'b000000000010: Block length is 2 bytes. 12'b011111111111: Block length is 2047 bytes. 12'b100000000000: Block length is 2048 bytes.
15	**GOIRQ**	GO_IRQ	**GO_IRQ command** Indicates if the command is GO_IRQ_STATE (CMD40) and used only for MMC protocol. If the command is GO_IRQ_STATE, the period between command token and response token will not be limited. 1'b0: The command is not GO_IRQ_STATE. 1'b1: The command is GO_IRQ_STATE.
14	**STOP**	STOP	**Stop command** Indicates if the command is a stop transmission command. It should be set to 1 when CMD12 (SD/MMC) or CMD52 with I/O abort (SDIO) is to be issued. 1'b0: The command is not a stop transmission command. 1'b1: The command is a stop transmission command.
13	**RW**	RW	**Selects command read write** Defines the command is a read command or write command. The register bit is valid only when the command causes a transaction with data token. 1'b0: The command is a read command. 1'b1: The command is a write command.
12:11	**DTYPE**	DTYPE	**Selects data block** Defines data token type for the command. 2'b00: No data token for the command 2'b01: Single block transaction (only available in block mode) 2'b10: Multiple block transaction (only available in block mode)

Bit(s)	Mnemonic	Name	Description
			2'b11: Stream operation. Should only be used in MMC protocol (only available in block mode).
9:7	**RSPTYP**	RSPTYP	**Command response type** 3'b000: This command has no response. 3'b001: The command has R1/R5/R6/R7 response. The response token is 48-bit with CRC check (for SD/MMC/SDIO)(excluding SDIO abort command) 3'b010: The command has R2 response. The response token is 136-bit (for SD/MMC). 3'b011: The command has R3 response. The response token is 48-bit response, no CRC check (for SD/MMC). 3'b100: The command has R4 response. The response token is 48-bit without CRC check (for SDIO); the response token is 48-bit with CRC check (for MMC). 3'b111: The command has R1b response. The response token is 48-bit (for SD/MMC/SDIO).
6	**BREAK**	BREAK	**Aborts pending MMC GO_IRQ command** Only valid for a pending GO_IRQ_MODE command waiting for MMC interrupt response. 1'b0: Not a beak command 1'b1: Break a pending MMC GO_IRQ_MODE command in the controller
5:0	**CMD**	CMD	**SD memory card command**

11250038 SDC_ARG **SD Argument Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ARG**	ARG	Memory card controller argument register

1125003C SDC_STS **SD Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMC_STREAM_WR_COMPL															CMD_WR_BUSY
Type	RU															W1C
Reset	0															0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CMDBUSY	SDCBUSY
Type															RU	RU
Reset															0	0

Bit(s)	Mnemonic	Name	Description
31	**MMCSWRCPL**	MMC_STREAM_WR_COMPL	**MMC stream mode write data are all flushed to MMC card** SW can use this bit to confirm the last write data are flushed to MMC then issue STOP command. This bit is only valid when the command SDC_CMD.DTYPE=2'b11. 1'b0: Last data are partially inside MSDC. 1'b1: Flush last data to MMC card
16		CMD_WR_BUSY	
1	**CMDBSY**	CMDBUSY	**SD command line busy status** SW should always read this bit to make sure the command line is not busy before sending the next command. If the command is R1B or data read/write command, SW should check the SDCBUSY bit too. Note: When auto command 12 is enabled, this bit will be asserted immediately after SDC_CMD is written and de-asserted after auto-command 12 is finished. 1'b0: No transmission is going on CMD line on SD bus. 1'b1: There is transmission going on CMD line on SD bus.
0	**SDCBSY**	SDCBUSY	**SD controller busy status** 1'b0: SD controller is idle. 1'b1: SD controller is busy.

11250040 SDC_RESP0 SD Response Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP0**	RESP0	Memory card controller response register 0

11250044 SDC_RESP1 SD Response Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP1**	RESP1	Memory card controller response register 1

11250048 SDC_RESP2 SD Response Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP2**	RESP2	Memory card controller response register 2

1125004C SDC_RESP3 SD Response Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP3**	RESP3	Memory card controller response register 3

11250050 SDC_BLK_NUM SD Block Number Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BLOCK_NUMBER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLOCK_NUMBER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:0	**BLKNUM**	BLOCK_NUMBER	**Memory card controller block number** Indicates block number of data transaction. 32'd0: Reserved 32'd1: 1 data block 32'd2: 2 data block 32'd3: 3 data block 32'hffffffff: 4GB-1 data block

11250054 SDC_VOL_CH SD Voltage Change Wait Time 00000145

G **Register**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11250058 SDC_CSTS SD Card Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CSTS**	CSTS	**CSTS** The card status field in the response R1 or R1b field. Each bit can be written 1 to clear individually.

1125005C SDC_CSTS_EN SD Card Status Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTS_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CSTS_EN**	CSTS_EN	**CSTS_EN** Controls which bit of CSTA will generate MSDC_INT.SDCSTA.

11250060 SDC_DATCRC_STS SD Card Data CRC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DAT_CRCSTS_POS							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**DCSSP**	DAT_CRCSTS_POS	**MSDC read DATA CRC status** Reflects CRC status of data line[7:0]. Only for MSDC read. 1'b0: No CRC error 1'b1: CRC error

11250080 SD_ACMD_RESP SD ACMD Response Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AUTOCMD_RESP															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOCMD_RESP															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ACMDRESP**	AUTOCMD_RESP	**SD auto command response register** Stores the response[39:8] of ACMD12/ACMD23/ACMD19.

11250084 SD_ACMD19_TRG SD ACMD19 Target Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11250088 SD_ACMD19_STS SD ACMD19 Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1125008C DMA_SA_HIGH4BIT **DMA Current Address Resgiter of High 4 Bits** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMA_SURR_ADDR_HIGH4BIT			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DMASAHIGH4BIT**	DMA_SURR_ADDR_HIGH4BIT	Sets up high 4-bit address of start address because 64G DRAM needs 36-bit address

11250090 DMA_SA **DMA Start Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_STR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_STR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DMASA**	DMA_STR_ADDR	**Start address of the DMA address** Sets up the start address of the DMA. In DMA basic mode, this field indicates the source or destination address of the data transfer which depends on the command. In descriptor base DMA, this is the descriptor chain start address.

11250094 DMA_CA **DMA Current Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_CURR_ADDR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_CURR_ADDR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DMACA**	DMA_CURR_ADDR	**Current address of the DMA address** Reads the current address of the DMA descriptor chain.

11250098 DMA_CTRL DMA Control Register 00006008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		BURST_SIZE			DMA_SPLIT_1K	LAST_BUF	DMA_ALIGN	DMA_MODE					AHB_READYM	DMA_RESUME	DMA_STOP	DMA_START
Type		RW			RW	RW	RW	RW					RO	WO	Ao	WO
Reset		1	1	0	0	0	0	0					1	0	0	0

Bit(s)	Mnemonic	Name	Description
14:12	**BSTSZ**	BURST_SIZE	**DMA burst size** Specifies the maximum transfer bytes allowed at the device per DMA burst. This field cannot be modified when the DMA status is 1. 3'd3: 8 bytes 3'd4: 16 bytes 3'd5: 32 bytes 3'd6: 64 bytes Other: Reserved
11	**SPLIT1K**	DMA_SPLIT_1K	**Specifies split burst when crossing 1K boundry address** 1'b0: 1K boundary is not split. 1'b1: 1K boundary is split.
10	**LASTBF**	LAST_BUF	**Last buffer of the basic DMA mode** Indicates the last buffer in the basic DMA mode.
9	**DMAALIGN**	DMA_ALIGN	**Specifies address aligment burst size** 1'b0: Not DAM burst size alignment 1'b1: DAM burst size alignment
8	**DMAMOD**	DMA_MODE	**DMA operation mode** Indicates operation mode of DMA. 1'b0: Basic DMA mode 1'b1: Descriptor base DMA mode
3	**READYM**	AHB_READYM	**Only for debugging when DMA hangs** SW checks if AHB bus is ok when GDMA hangs.
2	**DMARSM**	DMA_RESUME	**DMA resume control register** Resumes DMA transaction. Read always returns 0.
1	**DMASTOP**	DMA_STOP	**DMA stop control register** Stops DMA transaction. When SW issues STOP command, SW must wait for this bit to be de-asserted or DMA inactive to guarantee stop is done.
0	**DMASTART**	DMA_START	**DMA start control register** Starts DMA transaction. Read always returns 0.

Bit(s)	Mnemonic	Name	Description

1125009C DMA_CFG **DMA Configuration Register** **00000004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																DMA_CHK_SUM_12B
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MSDC_ACTIVE_EN				AHB_HPROT_2_EN							LOCK_DISABLE	DMA_DSCP_CS_EN	DMA_STATUS
Type			RW				RW							RW	RW	RU
Reset			0	0			0	0						1	0	0

Bit(s)	Mnemonic	Name	Description
16	**DMACHKSUM12B**	DMA_CHK_SUM_12 B	**Indicates GPD/BD checksum covers 16 bytes or 12 bytes** 1'b0: GPD/BD checksum covers 16 bytes. 1'b1: GPD/BD checksum only covers 12 bytes.
13:12	**MSDCACTIVEEN**	MSDC_ACTIVE_EN	**Indicates how to control msdc_active** 2'b00: Dynamic control msdc_active 2'b01: msdc_active = 0 2'b10: msdc_active = 1 2'b11: Reserved
9:8	**AHBHPROT2EN**	AHB_HPROT_2_EN	**Determines how to control hprot_2 pin of AHB bus** AHB_HPROT_2_EN = 2'b00 and basic DMA mode All the write transfers of a burst will be accessed by bufferable mode except for the last burst of DMA. AHB_HPROT2_2_EN=2'b00 and descriptor DMA mode All the write transfers of a burst will be accessed by bufferable mode except for HW own update transfer. 2'b00: Dynamic control hprot_2 2'b01: hprot_2 = 0 2'b10: hprot_2 = 1
2	**LOCKDISABLE**	LOCK_DISABLE	**Disables lock to improve EMI efficiency** 1'b0: Enable AHB lock 1'b1: Disable AHB lock
1	**DSCPCSEN**	DMA_DSCP_CS_EN	**Enables DMA descriptor checksum** This bit is used to enable or disable the descriptor checksum validation function for the descriptor. This field cannot be modified when the DMA status is 1.
0	**DMASTS**	DMA_STATUS	**DMA status** Indicates the status of DMA. 1'b0: DMA engine is inactive. 1'b1: DMA engine is active.

112500A0 SW_DBG_SEL **MSDC S/W Debug Selection Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_SEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**SWDBGSEL**	DBG_SEL	**Selects MSDC debugging** Reserved.

112500A4 SW_DBG_OUT MSDC S/W Debug Output Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SWDBGO**	DBG_OUT	**MSDC debug output** 32-bit output selected by SW_DBG_SEL register

112500A8 DMA_LENGTH DMA Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	XFER_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XFER_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**XFSZ**	XFER_SIZE	**DMA total transfer size** Specifies the number of DMA transfer byte required for the movement of source data through DMA. This field is only valid in basic DMA mode.

112500B0 PATCH_BIT0 MSDC Patch Bit Register 0 403C0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_MMC_DRV_R	DETECT_WR_CR	SPC_ALWAYS_P	SDIO_INT_DLY	SDC_CMD_CMDF	SDC_CMD_IDRT	SDC_ CFG_ WDOD				SDC_CFG_BSYDLY				SDIO_CFG_INT	MSDC_BLKNUM_

	ESP	C_TIMEOUT	USH	_SEL	AIL_SEL	_SEL									C_SEL	SEL
Type	RW	RW	RW	RW	RW	RW	RW				RW				RW	RW
Reset	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC_FIFO_RD_DIS						INT_DAT_LATCH_CK_SEL							DIS_REFLECT_CMDWR_WHEN_BSY	EN_SDC_ODD_8BIT_SUP	RALo
Type	RW						RW							RW	RW	RW
Reset	0						0	0	0					1	1	1

Bit(s)	Mnemonic	Name	Description
31	**PTCH31**	EN_MMC_DRV_RES P	**Enables MSDC always drives bus when outputting wake-up response (BREAK)** 1'b0: Disable 1'b1: Enable
30	**PTCH30**	DETECT_WR_CRC_ TIMEOUT	**Detects MSDC write data CRC phase timeout** 1'b0: Does not detect CRC phase timeout 1'b1: Detect CRC phase timeout
29	**PTCH29**	SPC_ALWAYS_PUS H	**SPC buffer push mechanism** 1'b0: Push the buffer only when read transfer is on-going 1'b1: Always push the buffer
28	**PTCH28**	SDIO_INT_DLY_S EL	**Selects SDIO interrupt latch time** 1'b0: Latch the data line value in internal SDIO interrupt period 1'b1: Latch the data line value in 1 clock delay of internal SDIO interrupt period
27	**PTCH27**	SDC_CMD_CMDFAI L_SEL	**Selects SDIO interrupt period recovery** 1'b0: SDIO interrupt period will re-start after a CMD12 or CMD52 command is issued. 1'b1: SDIO interrupt period whenever DAT line is not busy.
26	**PTCH26**	SDC_CMD_IDRT_S EL	**Selects SD identification response time** The register bit indicates if the command has a response with NID (i.e. 5 serial clock cycles as defined in SD memory card Specification Part 1 Physical Layer Specification version 1.0) response time. The register bit is valid only when the command has a response token. Thus, the register bit must be set to 1 for CMD2 (ALL_SEND_CID) and ACMD41 (SD_APP_OP_CMD). 1'b0: Otherwise 1'b1: The command has a response with NID response time.
25:22	**PTCH22**	SDC_CFG_WDOD	**SD write data output delay** The period from finish of the response for the initial host write command or the last write data block in a multiple block write operation to the start bit of the next write data block requires at least two serial clock cycles. The register field is used to extend the period (Write Data Output Delay) in unit of one serial clock. 4'b0000: No extension 4'b0001: Extend 1 more serial clock cycle 4'b0010: Extend 2 more serial clock cycles 4'b1111: Extend 15 more serial clock cycles

Bit(s)	Mnemonic	Name	Description
21:18	**PTCH18**	SDC_CFG_BSYDLY	**SD R1B busy detection mode** The register field is only valid for the commands with R1b response. If the command has a response of R1b type, MS/SD controller must monitor the data line 0 for card busy status from the bit time that is two serial clock cycles after the command end bit to check if operations in SD/MMC Memory Card have finished. The register field is used to expand the time between the command end bit and end of detection period to detect card busy status. If time is up and there is no card busy status on data line 0, then the controller will abandon the detection. 4'b0000: No extension 4'b0001: Extend 1 more serial clock cycle 4'b0010: Extend 2 more serial clock cycles 4'b1111: Extend 15 more serial clock cycles
17	**PTCH17**	SDIO_CFG_INTC_ SEL	**Selects SDIO interrupt mode** 1'b0: Only when data line [1] = 0 and then trigger SDIO interurpt event 1'b1: Only when data line [3:0] = 4'b1101 and then trigger SDIO interurpt event
16	**PTCH16**	MSDC_BLKNUM_SE L	**Supports ACMD23 reliable/force prog feature** 1'b0: Support ACMD23 reliable/force prog feature 1'b1: Does not support ACMD23 reliable/force prog feature
15	**PTCH15**	MSDC_FIFO_RD_D IS	**Disables MSDC RXFIFO read** 1'b0: Disable FIFO read permission to RXFIFO in PIO mode 1'b1: Enable FIFO read permission to RXFIFO in PIO mode
9:7	**INTCKS**	INT_DAT_LATCH_ CK_SEL	**Selects internal MSDC clock phase** Total 8 stages, each stage can delay 1 clock period of msdc_src_ck.
2	**PTCH02**	DIS_REFLECT_CM DWR_WHEN_BSY	**Enables SD command register write monitor** 1'b0: Enable monitor function 1'b1: Disable monitor function
1	**PTCH01**	EN_SDC_ODD_8BI T_SUP	**Enables SD odd number support for 8-bit data bus** 1'b0: Disable 1'b1: Enable
0		RAL0	

112500B4 PATCH_BIT1 **MSDC Patch Bit Register 1** **FFFF0009**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MSDC_CK_SHBFF_CK EN	MSDC_CK_RCTL_CKEN	MSDC_CK_WCTL_CKEN	MSDC_CK_SD_CKEN	MSDC_CK_ACMD_CKEN	MSDC_CK_VOLDET_CKEN	MSDC_CK_PSC_CKEN	MSDC_CK_SPC_CKEN	AHB_CK_GDMA_CKEN	RAL0			RAL1			ENABLE_SINGLE_BURST
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			RW			RW
Reset	1	1	1	1	1	1	1	1	1	1			1	1		1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESE	RAL2	BIAS_EXT	BIAS_EN1	BIAS_TUNE_28NM				GET_CRC_	GET_BUSY	CMD_RSP_TA_CN TR		WRDAT_CRCS_TA _CNTR			

	T_GDMA		BIAS_28NM	8IO_28NM					MARG IN	_MARGIN						
Type	RW	RW	RW	RW	RW				RW	RW	RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
31	**MSHBFCKEN**	MSDC_CK_SHBFF_CKEN	**msdc_src_ck clock enable bit for SHBFF** 1'b0: Disable 1'b1: Enable
30	**MRCTLCKEN**	MSDC_CK_RCTL_CKEN	**msdc_src_ck clock enable bit for RCTL** 1'b0: Disable 1'b1: Enable
29	**MWCTLCKEN**	MSDC_CK_WCTL_CKEN	**msdc_src_ck clock enable bit for WCTL** 1'b0: Disable 1'b1: Enable
28	**MSDCKEN**	MSDC_CK_SD_CKE N	**msdc_src_ck clock enable bit for SD** 1'b0: Disable 1'b1: Enable
27	**MACMDCKEN**	MSDC_CK_ACMD_CKEN	**msdc_src_ck clock enable bit for ACMD** 1'b0: Disable 1'b1: Enable
26	**MVOLDTCKEN**	MSDC_CK_VOLDET_CKEN	**msdc_src_ck clock enable bit for VOLDET** 1'b0: Disable 1'b1: Enable
25	**MPSCCKEN**	MSDC_CK_PSC_CKEN	**msdc_src_ck clock enable bit for PSC** 1'b0: Disable 1'b1: Enable
24	**MSPCCKEN**	MSDC_CK_SPC_CKEN	**msdc_src_ck clock enable bit forSPC** 1'b0: Disable 1'b1: Enable
23	**HGDMACKEN**	AHB_CK_GDMA_CKEN	**hclk_ck clock enable bit for GDMA** 1'b0: Disable 1'b1: Enable
22		RAL0	
19:18		RAL1	
16	**SINGLEBURST**	ENABLE_SINGLE_BURST	**AHB bus will not support incr1 burst type in the future. This will only affect AHB bus MSDC design, not AXI bus design.** 1'b0: HW will send incr1 burst type. 1'b1: HW will send single burst type instead of incr1 type.
15	**RESETGDMA**	RESET_GDMA	**SW can reset GDMA when design hangs.** 1'b1: Reset GDMA 1'b0: Does not reset GDMA
14		RAL2	
13	**BIAS28R0**	BIAS_EXTBIAS_28NM	**28NM BIAS controller register 0**
12	**BIAS28R1**	BIAS_EN18IO_28 NM	**28NM BIAS controller register 1**
11:8	**BIAS28R2**	BIAS_TUNE_28NM	**28NM BIAS controller register 2**
7	**GETCRCMARGIN**	GET_CRC_MARGIN	**Adds margin to get CRC status when card resp CRC does not match spec 2 cycle from endbit** 1'b0: 8 cycles reserved to get CRC status from write data CRC endbit 1'b1: 16 cycles reserved to get CRC status from write data CRC endbit
6	**GETBUSYMARGIN**	GET_BUSY_MARGI N	**Adds margin to get busy state of data0** 1'b0: 1 cycle reserved to get busy state from SRC status endbit 1'b1: 3 cycles reserved to get busy state from SRC status

Bit(s)	Mnemonic	Name	Description
			endbit
5:3	**CMDTA**	CMD_RSP_TA_CNT R	**CMD response turn around period** Turn around cycle = CMD_RSP_TA_CNTR + 2 In USH104 mode, this register should be set to 1. In non-UHS104 mode, this register should be set to 0.
2:0	**WRTA**	WRDAT_CRCS_TA_ CNTR	**Write data and CRC status turn around period** Turn around cycle = WRDAT_CRCS_TA_CNTR + 2 In USH104 mode, this register should be set to 1. In non-UHS104 mode,this register should be set to 0.

112500B8 PATCH_BIT2 **MSDC Patch Bit Register 2** **14801803**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRCSTS_LATCH_EN_SEL			CFG_CRCSTS	CFG_CRCSTS_CNT		CFG_CRCSTS_EDGE	CFG_CRCSTS_SEL	POP_EN_CNT				RALo	RESP_LATCH_EN_SEL		
Type	RW			RW	RW		RW	RW	RW				RW	RW		
Reset	0	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG_RESP	CFG_RESP_CNT			INTC_RESP_SEL	RAL1	CFG_RDAT	CFG_RDAT_CNT					RESP_WAIT_CNT		SUPPORT_64G	ENHANCE_WAIT_GPD
Type	RW	RW			RW	RW	RW	RW					RW		RW	RW
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:29	**CRCSTSENSEL**	CRCSTS_LATCH_EN_SEL	**Configures latch CRC status enable signal for async FIFO in eMMC45** 3'b000: Latch CRC status enable signal does not delay. 3'b001: Latch CRC status enable signal delays 1T msdc_ck. 3'b010: Latch CRC status enable signal delays 2T msdc_ck. 3'b011: Latch CRC status enable signal delays 3T msdc_ck. 3'b111: Latch CRC status enable signal delays 7T msdc_ck.
28	**CFGCRCSTS**	CFG_CRCSTS	**Configures CRC status path selection** This setting only uses eMMC4.5 feature. 1'b0: Latch CRC status select delay-line path 1'b1: Latch CRC status select async FIFO path
27:26	**CFGCRCSTSCNT**	CFG_CRCSTS_CNT	**Configures the number of data pushed in async FIFO until starting to pop out data from async FIFO** Min. setting: 1. Do not set it to 0. This setting only uses eMMC4.5 feature. 2'b00: Push 0 data in async FIFO when starting to pop out data from async FIFO 2'b01: Push 1 data in async FIFO when starting to pop out data from async FIFO 2'b10: Push 2 data in async FIFO when starting to pop out data from async FIFO 2'b11: Push 3 data in async FIFO when starting to pop out data from async FIFO
25	**CFGCRCSTSEDGE**	CFG_CRCSTS_EDG E	**Configures to use rising async FIFO or falling async FIFO**

Bit(s)	Mnemonic	Name	Description
			1'b0: Async FIFO latch CRC status uses rising async FIFO. 1'b1: Async FIFO latch CRC status uses falling async FIFO.
24		CFG_CRCSTS_SEL	**Configures async FIFO path selection** 1'b0: Use normal path in async FIFO 1'b1: Use 2DFF path in async FIFO
23:20	**POPENCNT**	POP_EN_CNT	**Pop enable counter** Defines how many write pointer and the read pointer margins begin to pop data transfer
19		RAL0	
18:16	**RESPSTSENSEL**	RESP_LATCH_EN_SEL	**Configures latch CMD response enable signal for async FIFO in eMMC45** 3'b000: Latch CMD response enable signal does not delay. 3'b001: Latch CMD response enable signal delays 1T msdc_ck. 3'b010: Latch CMD response enable signal delays 2T msdc_ck. 3'b011: Latch CMD response enable signal delays 3T msdc_ck. 3'b111: Latch CMD response enable signal delays 7T msdc_ck.
15	**CFGRESP**	CFG_RESP	**Configures CMD response path selection** This setting only uses eMMC4.5 feature. 1'b0: Latch CMD response select async FIFO path 1'b1: Latch CMD response select delay-line path
14:12	**CFGRESPCNT**	CFG_RESP_CNT	**Configures the number of data pushed in async FIFO until starting to pop out data from async FIFO** Min. setting: 1. Do not set it to 0. This setting only uses eMMC4.5 feature. 3'b000: Push 0 data in async FIFO when starting to pop out data from async FIFO 3'b001: Push 1 data in async FIFO when starting to pop out data from async FIFO 3'b111: Push 7 data in async FIFO when starting to pop out data from async FIFO
11	**INTCRESPSEL**	INTC_RESP_SEL	**Configures BREAK command async FIFO path** 1'b0: Use normal path in async FIFO 1'b1: Use 2DFF path in async FIFO
10		RAL1	
9	**CFGRDAT**	CFG_RDAT	**Configures read data path** 1'b0: Read data path bypasses delay line 1'b1: Read data path through delay line
8:4	**CFGRDATCNT**	CFG_RDAT_CNT	**Configures read data path delay line**
3:2	**RESPWAITCNT**	RESP_WAIT_CNT	**Configures CMD response timeout** Timeout cycle = 65T + 16*RESP_WAIT_CNT 2'b00: CMD response timeout is 65T. 2'b01: CMD response timeout is 65T+16*1T. 2'b01: CMD response timeout is 65T+16*2T. 2'b01: CMD response timeout is 65T+16*3T.
1	**SUPPORT64G**	SUPPORT_64G	**Supports high 64G DRAM space access or not** 1'b1: Support 64G DRAM access 1'b0: Does not support 64G DRAM access
0	**ENHANCEGPD**	ENHANCE_WAIT_GPD	**If SW clears int when GPD update is not finished, design will hang.** Set this bit to 1 to avoid this issue in enhance write

Bit(s)	Mnemonic	Name	Description
			mode. 1'b1: Use new HW code for updating GPD in enhance mode 1'b0: Use old HW code

112500C0 DAT0_TUNE_CRC **DAT0 Tune Result Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112500C4 DAT1_TUNE_CRC **DAT1 Tune Result Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112500C8 DAT2_TUNE_CRC **DAT2 Tune Result Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112500CC DAT3_TUNE **DAT3 Tune Result Register** **00000000**

CRC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112500D0 CMD_TUNE_CRC **CMD Tune Result Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112500D4 SDIO_TUNE_WIND **SDIO Tune Window Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112500F0 DAT_RD_DLY **MSDC Data Delay Line Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT0_RD_DLY								DAT1_RD_DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT2_RD_DLY								DAT3_RD_DLY				
Type				RW								RW				

Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT0RDDLY**	DAT0_RD_DLY	**Controls DAT0 pad RX delay line (for MSDC RD)** Total 32 stages.
20:16	**DAT1RDDLY**	DAT1_RD_DLY	**Controls DAT1 pad RX delay line (for MSDC RD)** Total 32 stages.
12:8	**DAT2RDDLY**	DAT2_RD_DLY	**Controls DAT2 pad RX delay line (for MSDC RD)** Total 32 stages.
4:0	**DAT3RDDLY**	DAT3_RD_DLY	**Controls DAT3 pad RX delay line (for MSDC RD)** Total 32 stages.

112500F4 DAT_RD_DLY1 **MSDC Data Delay Line Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT4_RD_DLY										RAL0	DAT6_RD_DLY				
Type	RO										RW	RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RAL1		RAL2	DAT7_RD_DLY					RAL3							
Type	RO		RW	RW					RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:22	**DAT4RDDLY**	DAT4_RD_DLY	**Controls DAT4 pad RX delay line (for MSDC RD)** Total 32 stages.
21	**DAT5RDDLY**	RAL0	**Controls DAT5 pad RX delay line (for MSDC RD)** Total 32 stages.
20:16	**DAT6RDDLY**	DAT6_RD_DLY	**Controls DAT6 pad RX delay line (for MSDC RD)** Total 32 stages.
15:14		RAL1	
13		RAL2	
12:8	**DAT7RDDLY**	DAT7_RD_DLY	**Controls DAT7 pad RX delay line (for MSDC RD)** Total 32 stages.
7:0		RAL3	

112500F8 HW_DBG_SEL **MSDC H/W Debug Selection Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RAL0			HW_DBG3_SEL					RAL1			HW_DBG2_SEL				
Type	RO			RW					RO			RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RAL2			HW_DBG1_SEL					RAL3			HW_DBG0_SEL				
Type	RO			RW					RO			RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:29	**DBGWSEL**	RAL0	**Selects HW debug output for wrapper** 0: Original debug pins 1: Wrapper debug pins
28:24 23:21	**DBG3SEL**	HW_DBG3_SEL RAL1	**Selects HW debug output**
20:16 15:13	**DBG2SEL**	HW_DBG2_SEL RAL2	**Selects HW debug output**
12:8 7:5	**DBG1SEL**	HW_DBG1_SEL RAL3	**Selects HW debug output**
4:0	**DBG0SEL**	HW_DBG0_SEL	**Selects HW debug output**

11250100 MAIN_VER MSDC Main Version Register 20140512

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAIN_VER															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAIN_VER															
Type	RO															
Reset	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
31:0	**MAINVER**	MAIN_VER	Main version

11250104 ECO_VER MSDC ECO Version Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ECO_VER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ECO_VER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ECOVER**	ECO_VER	ECO version