MT6797 LTE-A Smartphone Application Processor Register Table for Development Board (Part II)

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Specifications are subject to change without notice.

Table of Contents

4 Multimedia

4.1 Display Controller

Module name: MMSYS_CONFIG Base address: (+14000000h)

Address	Name	Width	Register Function
14000000	MMSYS_INTEN	32	MMSYS Interrupt Enable
14000004	MMSYS_INTSTA	32	MMSYS Interrupt Status
1400000C	MJC_APB_TX_CON	32	MMSYS to MJC APB TX Control
1400001C	ISP_MOUT_EN	16	ISP_MDP Multiple Output Enable
14000020	MDP_RDMA0_MOUT_EN	16	MDP_RDMA0 Multiple Output Enable
14000024	MDP_PRZ0_MOUT_EN	16	MDP Resize0 Multiple Output Enable
14000028	MDP_PRZ1_MOUT_EN	16	MDP Resize1 Multiple Output Enable
1400002C	MDP_PRZ2_MOUT_EN	16	MDP Resize2 Multiple Output Enable
14000030	MDP_COLOR_MOUT_EN	16	MDP Color Engine Multiple Output Enable
14000034	DISP_OVL0_MOUT_EN	16	Display Overlay0 Multiple Output Enable
14000038	DISP_OVL1_MOUT_EN	16	Display Overlay1 Multiple Output Enable
1400003C	DISP_DITHER_MOUT_EN	16	Display Dither Multiple Output Enable
14000040	DISP_UFOE_MOUT_EN	16	Display UFOE Multiple Output Enable
14000044	DISP_DSC_MOUT_EN	16	Display DSC_Wrap Multiple Output Enable
14000048	MMSYS_MOUT_RST	16	MMSYS Multiple Output Reset
1400004C	MDP_PRZ0_SEL_IN	16	MDP PRZ0 Input Selection
14000050	MDP_PRZ1_SEL_IN	16	MDP PRZ1 Input Selection
14000054	MDP_PRZ2_SEL_IN	16	MDP PRZ2 Input Selection
14000058	MDP_TDSHP_SEL_IN	16	MDP TDSHP Input Selection
1400005C	MDP_WDMA_SEL_IN	16	MDP WDMA Input Selection
14000060	MDP_WROT0_SEL_IN	16	MDP WROT0 Input Selection
14000064	MDP_WROT1_SEL_IN	16	MDP WROT1 Input Selection
14000068	DISP_COLOR_SEL_IN	16	DISP_COLOR Input Selection
1400006C	DISP_WDMA0_SEL_IN	16	DISP_WDMA0 Input Selection
14000070	DISP_WDMA1_SEL_IN	16	DISP_WDMA1 Input Selection
14000074	DISP_UFOE_SEL_IN	16	DISP_UFOE Input Selection
14000078	DISP_DSC_SEL_IN	16	DISP_DSC_Wrap Input Selection
1400007C	DSI0_SEL_IN	16	DSI0 Input Selection

Address	Name	Width	Register Function
14000080	DSI1_SEL_IN	16	DSI1 Input Selection
14000084	DPI0_SEL_IN	16	DPI0 Input Selection
14000088	DISP_PATH0_SEL_IN	16	DISP_PATH0 Input Selection
1400008C	DISP_PATH0_SOUT_SEL_IN	16	DISP_PATH0 Output Select
14000090	DISP_RDMA0_SOUT_SEL_IN	16	DISP_RDMA0 Output Select
14000094	DISP_RDMA1_SOUT_SEL_IN	16	DISP_RDMA1 Output Select
14000098	DISP_OVL0_SOUT_SEL_IN	16	DISP_OVL0 Output Select
1400009C	DISP_OVL0_SEL_IN	16	DISP_OVL0_MOUT Input Selection
140000A0	DISP_OVL1_SOUT_SEL_IN	16	DISP_OVL1_2L Output Select
140000F0	MMSYS_MISC	16	MMSYS_MISC
140000F4	MMSYS_SMI_LARB_SEL	32	MMSYS_SMI_LARB_SEL
140000F8	MMSYS_SODI_REQ_MASK	32	MMSYS_SODI_REQ_MASK
14000100	MMSYS_CG_CON0	32	MMSYS Clock Gating Config 0
14000104	MMSYS_CG_SET0	32	MMSYS Clock Gating Set 0
14000108	MMSYS_CG_CLR0	32	MMSYS Clock Gating Clear 0
14000110	MMSYS_CG_CON1	32	MMSYS Clock Gating Config 1
14000114	MMSYS_CG_SET1	32	MMSYS Clock Gating Set 1
14000118	MMSYS_CG_CLR1	32	MMSYS Clock Gating Clr 1
14000120	MMSYS_HW_DCM_DIS0	32	MMSYS Hardware DCM Disable 0
14000124	MMSYS_HW_DCM_DIS_SET0	32	MMSYS Hardware DCM Disable Set 0
14000128	MMSYS_HW_DCM_DIS_CLR0	32	MMSYS Hardware DCM Disable Clear 0
14000130	MMSYS_HW_DCM_DIS1	32	MMSYS Hardware DCM Disable 1
14000134	MMSYS_HW_DCM_DIS_SET1	32	MMSYS Hardware DCM Disable Set 1
14000138	MMSYS_HW_DCM_DIS_CLR1	32	MMSYS Hardware DCM Disable Clear 1
14000140	MMSYS_SW0_RST_B	32	MMSYS Software Reset
14000144	MMSYS_SW1_RST_B	32	MMSYS Software Reset
14000150	MMSYS_LCM_RST_B	32	LCM Reset
14000168	SMI_N21MUX_CFG_WR	32	SMI_N21MUX_CFG_WR
1400016C	SMI_N21MUX_CFG_RD	32	SMI_N21MUX_CFG_RD
14000170	ELA2GMC_BASE_ADDR	32	ELA2GMC_BASE_ADDR
14000174	ELA2GMC_BASE_ADDR_END	32	ELA2GMC_BASE_ADDR_END
14000178	ELA2GMC_FINAL_ADDR	32	ELA2GMC_FINAL_ADDR
1400017C	ELA2GMC_STATUS	32	ELA2GMC_STATUS

Address	Name	Width	Register Function
14000180	LARB4_AXI_ASIF_CFG_WD	32	LARB4_AXI_ASIF_CFG_WD
14000184	LARB4_AXI_ASIF_CFG_RD	32	LARB4_AXI_ASIF_CFG_RD
14000190	PROC_TRACK_EMI_BUSY_CON	32	Proc_Track EMI Busy Control
14000200	DISP_FAKE_ENG_EN	32	DISP Fake Engine Enable
14000204	DISP_FAKE_ENG_RST	32	DISP Fake Engine Reset
14000208	DISP_FAKE_ENG_CON0	32	DISP Fake Engine Control 0
1400020C	DISP_FAKE_ENG_CON1	32	DISP Fake Engine Control 1
14000210	DISP_FAKE_ENG_RD_ADDR	32	DISP Fake Engine Read Address
14000214	DISP_FAKE_ENG_WR_ADDR	32	DISP Fake Engine Write Address
14000218	DISP_FAKE_ENG_STATE	32	DISP Fake Engine Status
14000220	DISP_FAKE_ENG2_EN	32	DISP Fake Engine 2 Enable
14000224	DISP_FAKE_ENG2_RST	32	DISP Fake Engine 2 Reset
14000228	DISP_FAKE_ENG2_CON0	32	DISP Fake Engine 2 Control 0
1400022C	DISP_FAKE_ENG2_CON1	32	DISP Fake Engine 2 Control 1
14000230	DISP_FAKE_ENG2_RD_ADDR	32	DISP Fake Engine 2 Read Address
14000234	DISP_FAKE_ENG2_WR_ADDR	32	DISP Fake Engine 2 Write Address
14000238	DISP_FAKE_ENG2_STATE	32	DISP Fake Engine 2 Status
14000800	MMSYS_MBIST_CO N	32	MMSYS MBIST Control
14000804	MMSYS_MBIST_DO NE	32	MMSYS MBIST Done
14000808	MMSYS_MBIST_HO LDB	32	MMSYS MBIST holdb
1400080C	MMSYS_MBIST_MO DE	32	MMSYS MBIST Mode
14000810	MMSYS_MBIST_FA IL0	32	MMSYS MBIST Fail 0
14000814	MMSYS_MBIST_FA IL1	32	MMSYS MBIST Fail 1
14000818	MMSYS_MBIST_FA IL2	32	MMSYS MBIST Fail 2
1400081C	MMSYS_MBIST_FA IL3	32	MMSYS MBIST Fail 3
14000820	MMSYS_MBIST_BS EL0	32	MMSYS MBIST BSEL 0
14000824	MMSYS_MBIST_BS EL1	32	MMSYS MBIST BSEL 1
14000828	MMSYS_MBIST_BS EL2	32	MMSYS MBIST BSEL 2

Address	Name	Width	Register Function
1400082C	MMSYS_MBIST_BSEL3	32	MMSYS MBIST BSEL 3
14000840	MDP_RDMA_MEM_DELSEL	32	MDP_RDMA Memory Delay Select
14000844	MDP_RSZ_MEM_DELSEL	32	MDP_RSZ Memory Delay Select
14000848	MDP_TDSHP_MEM_DELSEL	32	MDP_TDSHP Memory Delay Select
1400084C	MDP_WDMA_MEM_DELSEL	32	MDP_WDMA Memory Delay Select
14000850	MDP_WROT_MEM_DELSEL	32	MDP_WROT Memory Delay Select
14000854	DISP_OVL_MEM_DELSEL	32	DISP_OVL Memory Delay Select
14000858	DISP_OVL_2L_MEM_DELSEL	32	DISP_OVL_2L Memory Delay Select
1400085C	DISP_RDMA_MEM_DELSEL	32	DISP_RDMA Memory Delay Select
14000860	DISP_WDMA0_MEM_DELSEL	32	DISP_WDMA0 Memory Delay Select
14000864	DISP_WDMA1_MEM_DELSEL	32	DISP_WDMA1 Memory Delay Select
14000868	DISP_GAMMA_MEM_DELSEL	32	DISP_GAMMA Memory Delay Select
1400086C	DSI_MEM_DELSEL	32	DSI Memory Delay Select
14000870	DISP_UFOE_MEM_DELSEL	32	DISP_UFOE Memory Delay Select
14000874	DISP_DSC_MEM_DELSEL	32	DISP_DSC Memory Delay Select
14000878	DISP_OD_MEM_DELSEL0	32	DISP_OD Memory Delay Select 0
1400087C	DISP_OD_MEM_DELSEL1	32	DISP_OD Memory Delay Select 1
14000880	MMSYS_DEBUG_OUT_SEL	32	MMSYS Debug Output Select
14000884	MMSYS_MBIST_RP_RST_B	32	MMSYS MBIST Repair Reset
14000888	MMSYS_MBIST_RP_FAIL	32	MMSYS MBIST Repair Fail
1400088C	MMSYS_MBIST_RP_OK	32	MMSYS MBIST Repair OK
14000890	MMSYS_DUMMY0	32	MMSYS Dummy Register 0
14000894	MMSYS_DUMMY1	32	MMSYS Dummy Register 1
14000898	MMSYS_DUMMY2	32	MMSYS Dummy Register 2
1400089C	MMSYS_DUMMY3	32	MMSYS Dummy Register 3
140008A0	DISP_DL_VALID_0	32	DISP Direct Link Valid Status 0
140008A4	DISP_DL_VALID_1	32	DISP Direct Link Valid Status 1
140008A8	DISP_DL_READY_0	32	DISP Direct Link READY Status 0
140008AC	DISP_DL_READY_1	32	DISP Direct Link READY Status 1
140008B0	MDP_DL_VALID_0	32	MDP Direct Link Valid Status 0
140008B4	MDP_DL_VALID_1	32	MDP Direct Link Valid Status 1
140008B8	MDP_DL_READY_0	32	MDP Direct Link READY Status 0

Address	Name	Width	Register Function
140008BC	MDP_DL_READY_1	32	MDP Direct Link READY Status 1
140008C0	SMI_LARB0_GREQ	32	SMI LARB0 Request
140008D0	DISP_MOUT_MASK	32	DISP Multiple Output Mask Status
140008D4	MDP_MOUT_MASK	32	MDP Multiple Output Mask Status

14000000 MMSYS_INTEN **MMSYS Interrupt Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MMSYS_INTEN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**MMSYS_INTEN**	MMSYS_INTEN	**Enables MMSYS interrupt** 0: Disable interrupt source 1: Enable interrupt source Bit 0: MMSYS to MJC APB TX Error Others: Reserved

14000004 MMSYS_INTSTA **MMSYS Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MMSYS_INTSTA
Type																A1
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**MMSYS_INTSTA**	MMSYS_INTSTA	**MMSYS interrupt status** 0: No interrupt occurs. 1: Interrupt occurs. Bit 0: MMSYS to MJC APB TX Error Others: Reserved

1400000C MJC_APB_TX_CON **MMSYS to MJC APB TX Control** **80000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	MJC_APB_COUNTER_EN															
Type	RW															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MJC_APB_ERR_ADDR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**MJC_APB_COUNTER_EN**	MJC_APB_COUNTER_EN	**Enables MMSYS to MJC APB erroc counter** 0: Disable MMSYS to MJC APB TX error counter 1: Enable MMSYS to MJC APB TX error counter
15:0	**MJC_APB_ERR_ADDR**	MJC_APB_ERR_ADDR	**Address to make MMSYS to MJC APB TX error**

1400001C ISP_MOUT_EN — **ISP_MDP Multiple Output Enable** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ISP_MOUT_EN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**ISP_MOUT_EN**	ISP_MOUT_EN	**Enables ISP_MDP multiple output** 0: Disable output port 1: Enable output port Bit 0: Output to PRZ0 Bit 1: Output to PRZ1 Bit 2: Output to PRZ2 Others: Reserved

14000020 MDP_RDMA0_MOUT_EN — **MDP_RDMA0 Multiple Output Enable** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MDP_RDMA0_MOUT_EN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**MDP_RDMA0_MOUT_EN**	MDP_RDMA0_MOUT_EN	**Enables MDP_RDMA0 multiple output** 0: Disable output port 1: Enable output port Bit 0: Output to PRZ0 Bit 1: Output to PRZ1 Bit 2: Output to PRZ2 Others: Reserved

14000024 MDP_PRZ0_MOUT_EN **MDP Resize0 Multiple Output Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MDP_PRZ0_MOUT_EN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**MDP_PRZ0_MOUT_EN**	MDP_PRZ0_MOUT_EN	**Enables MDP Resize0 multiple output** 0: Disable output port 1: Enable output port Bit 0: Output to MDP_WDMA Bit 1: Output to MDP_WROT0 Bit 2: Output to MDP_TDSHP Bit 3: Output to MDP_RSZ1 Others: Reserved

14000028 MDP_PRZ1_MOUT_EN **MDP Resize1 Multiple Output Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MDP_PRZ1_MOUT_EN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**MDP_PRZ1_MOUT_EN**	MDP_PRZ1_MOUT_EN	**Enables MDP Resize1 multiple output** 0: Disable output port 1: Enable output port Bit 0: Output to MDP_WDMA Bit 1: Output to MDP_WROT0 Bit 2: Output to MDP_TDSHP Bit 3: Output to MDP_WROT1 Others: Reserved

Bit(s)	Mnemonic	Name	Description

1400002C MDP_PRZ2_MOUT_EN — **MDP Resize2 Multiple Output Enable** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MDP_PRZ2_MOUT_EN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**MDP_PRZ2_MOUT_EN**	MDP_PRZ2_MOUT_EN	**Enables MDP Resize2 multiple output** 0: Disable output port 1: Enable output port Bit 0: Output to MDP_WDMA Bit 1: Output to MDP_WROT1 Bit 2: Output to MDP_TDSHP Others: Reserved

14000030 MDP_COLOR_MOUT_EN — **MDP Color Engine Multiple Output Enable** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MDP_COLOR_MOUT_EN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**MDP_COLOR_MOUT_EN**	MDP_COLOR_MOUT_EN	**Enables MDP color engine multiple output** 0: Disable output port 1: Enable output port Bit 0: Output to MDP_WDMA Bit 1: Output to MDP_WROT0 Bit 2: Output to MDP_WROT1 Others: Reserved

14000034 DISP_OVL0_MOUT_EN — **Display Overlay0 Multiple Output Enable** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DISP_OVL0_MOUT_EN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**DISP_OVL0_MOUT_EN**	DISP_OVL0_MOUT_EN	**Enables display overlay0 multiple output** 0: Disable output port 1: Enable output port Bit 0: Output to DISP_COLOR Bit 1: Output to DISP_WDMA0 Others: Reserved

14000038 DISP_OVL1_MOUT_EN **Display Overlay1 Multiple Output Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DISP_OVL1_MOUT_EN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**DISP_OVL1_MOUT_EN**	DISP_OVL1_MOUT_EN	**Enables display overlay1 multiple output** 0: Disable output port 1: Enable output port Bit 0: Output to DISP_RDMA1 Bit 1: Output to DISP_WDMA1 Bit 2: Output to DISP_OVL0_MOUT Others: Reserved

1400003C DISP_DITHER_MOUT_EN **Display Dither Multiple Output Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DISP_DITHER_MOUT_EN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**DISP_DITHER_MOUT_EN**	DISP_DITHER_MOUT_EN	**Enables display dither multiple output** 0: Disable output port

Bit(s)	Mnemonic	Name	Description
			1: Enable output port Bit 0: Output to DISP_RDMA0 Bit 1: Output to DISP_PATH0 Bit 2: Output to DISP_WDMA0 Others: Reserved

14000040 DISP_UFOE_MOUT_EN **Display UFOE Multiple Output Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DISP_UFOE_MOUT_EN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**DISP_UFOE_MOUT_EN**	DISP_UFOE_MOUT_EN	**Enables display UFOE multiple output** 0: Disable output port 1: Enable output port Bit 0: Output to DSI0 Bit 1: Output to DISP_SPLIT Bit 2: Output to DPI Bit 3: Output to DISP_WDMA0 Bit 4: Output to DSI1 Others: Reserved

14000044 DISP_DSC_MOUT_EN **Display DSC_Wrap Multiple Output Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DISP_DSC_MOUT_EN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**DISP_DSC_MOUT_EN**	DISP_DSC_MOUT_EN	**Enables display DSC_Wrap multiple output** 0: Disable output port 1: Enable output port Bit 0: Output to DSI0 Bit 1: Output to DSI1 Bit 2: Output to DPI Bit 3: Output to DISP_WDMA1 Others: Reserved

Bit(s)	Mnemonic	Name	Description

14000048 MMSYS_MOUT_RST **MMSYS Multiple Output Reset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMSYS_MOUT_RST															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**MMSYS_MOUT_RST**	MMSYS_MOUT_RST	**Resets MMSYS multiple output** 0: Does not reset 1: Reset Bit 0: ISP_MDP mutiple outupt reset Bit 1: MDP_RDMA0 mutiple outupt reset Bit 2: MDP_PRZ0 mutiple outupt reset Bit 3: MDP_PRZ1 mutiple outupt reset Bit 4: MDP_PRZ2 mutiple outupt reset Bit 5: MDP_COLOR mutiple outupt reset Bit 6: DISP_OVL0 mutiple outupt reset Bit 7: DISP_OVL1 mutiple outupt reset Bit 8: DISP_DITHER mutiple outupt reset Bit 9: DISP_UFOE mutiple outupt reset Bit 10: DISP_DSC mutiple outupt reset Others: Reserved

1400004C MDP_PRZ0_SEL_IN **MDP PRZ0 Input Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													MDP_PRZ0_SEL_IN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**MDP_PRZ0_SEL_IN**	MDP_PRZ0_SEL_IN	**Selects MDP PRZ0 input** 0: From ISP_MDP 1: From MDP_RDMA0 Others: Reserved

14000050 MDP_PRZ1_SEL_IN **MDP PRZ1 Input Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													MDP_PRZ1_SEL_IN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**MDP_PRZ1_SEL_IN**	MDP_PRZ1_SEL_IN	**Selects MDP PRZ1 input** 0: From ISP_MDP 1: From MDP_RDMA0 2: From MDP_PRZ0 Others: Reserved

14000054 MDP_PRZ2_SEL_IN **MDP PRZ2 Input Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													MDP_PRZ2_SEL_IN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**MDP_PRZ2_SEL_IN**	MDP_PRZ2_SEL_IN	**Selects MDP PRZ2 input** 0: From ISP_MDP 1: From MDP_RDMA0 2: From MDP_RDMA1 Others: Reserved

14000058 MDP_TDSHP_SEL_IN **MDP TDSHP Input Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													MDP_TDSHP_SEL_IN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**MDP_TDSHP_SEL_IN**	MDP_TDSHP_SEL_ IN	**Selects MDP TDSHP input** 0: From MDP_PRZ0 1: From MDP_PRZ1 2: From MDP_PRZ2 Others: Reserved

1400005C MDP_WDMA_SEL_IN **MDP WDMA Input Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													MDP_WDMA_SEL_IN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**MDP_WDMA_SEL_IN**	MDP_WDMA_SEL_I N	**Selects MDP WDMA input** 0: From MDP_PRZ0 1: From MDP_PRZ1 2: From MDP_COLOR 3: From MDP_PRZ2 Others: Reserved

14000060 MDP_WROT0_SEL_IN **MDP WROT0 Input Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													MDP_WROT0_SEL_IN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**MDP_WROT0_SEL_IN**	MDP_WROT0_SEL_ IN	**Selects MDP WROT0 input** 0: From MDP_PRZ0 1: From MDP_PRZ1 2: From MDP_COLOR Others: Reserved

14000064 MDP_WROT1_SEL_IN **MDP WROT1 Input Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													MDP_WROT1_SEL_IN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**MDP_WROT1_SEL_IN**	MDP_WROT1_SEL_IN	**Selects MDP WROT1 input** 0: From MDP_PRZ1 1: From MDP_PRZ2 2: From MDP_COLOR Others: Reserved

14000068 DISP_COLOR_SEL_IN DISP_COLOR Input Selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DISP_COLOR_SEL_IN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DISP_COLOR_SEL_IN**	DISP_COLOR_SEL_IN	**Selects DISP_COLOR input** 0: From DISP_RDMA0 1: From DISP_OVL0 Others: Reserved

1400006C DISP_WDMA0_SEL_IN DISP_WDMA0 Input Selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DISP_WDMA0_SEL_IN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DISP_WDMA0_SEL_IN**	DISP_WDMA0_SEL_IN	**Selects DISP_WDMA0 input** 0: From DISP_OVL0 1: From DISP_DITHER 2: From DISP_UFOE

Bit(s)	Mnemonic	Name	Description
			Others: Reserved

14000070 DISP_WDMA1_SEL_IN **DISP_WDMA1 Input Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DISP_WDMA1_SEL_IN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DISP_WDMA1_SEL_IN**	DISP_WDMA1_SEL_IN	**Selects DISP_WDMA1 input** 0: From DISP_OVL1 1: From DISP_DSC Others: Reserved

14000074 DISP_UFOE_SEL_IN **DISP_UFOE Input Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DISP_UFOE_SEL_IN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DISP_UFOE_SEL_IN**	DISP_UFOE_SEL_ IN	**Selects DISP_UFOE input** 0: From DISP_PATH0 1: From DISP_RDMA1 Others: Reserved

14000078 DISP_DSC_SEL_IN **DISP_DSC_Wrap Input Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DISP_DSC_SEL_IN			
Type													RW			

Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DISP_DSC_SEL_I N**	DISP_DSC_SEL_I N	**Selects DISP_DSC_Wrap input** 0: From DISP_PATH0 1: From DISP_RDMA1 Others: Reserved

1400007C DSI0_SEL_IN **DSI0 Input Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DSI0_SEL_IN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DSI0_SEL_IN**	DSI0_SEL_IN	**Selects DSI0 input** 0: From DISP_UFOE 1: From DISP_SPLIT 2: From DISP_RDMA0 3: From DISP_DSC Others: Reserved

14000080 DSI1_SEL_IN **DSI1 Input Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DSI1_SEL_IN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DSI1_SEL_IN**	DSI1_SEL_IN	**Selects DSI1 input** 0: From DISP_SPLIT 1: From DISP_RDMA0 2: From DISP_DSC 3: From DISP_UFOE Others: Reserved

14000084 DPIo_SEL_IN **DPIo Input Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DPIo_SEL_IN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DPIo_SEL_IN**	DPIo_SEL_IN	**Selects DPIo input** 0: From DISP_UFOE 1: From DISP_RDMA0 2: From DISP_DSC Others: Reserved

14000088 DISP_PATH0_SEL_IN **DISP_PATH0 Input Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DISP_PATH0_SEL_IN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DISP_PATH0_SEL_IN**	DISP_PATH0_SEL_IN	**Selects DISP_PATH0 input** 0: From DISP_RDMA0 1: From DISP_DITHER Others: Reserved

1400008C DISP_PATH0_SOUT_SEL_IN **DISP_PATH0 Output Select** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DISP_PATH0_SOUT_SEL_IN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DISP_PATH0_SOUT_SEL_IN**	DISP_PATH0_SOUT_SEL_IN	**Selects DISP_PATH0 output** 0: Output to DISP_UFOE 1: Output to DISP_DSC Others: Reserved

14000090 DISP_RDMA0_SOUT_SEL_IN **DISP_RDMA0 Output Select** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DISP_RDMA0_SOUT_SEL_IN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DISP_RDMA0_SOUT_SEL_IN**	DISP_RDMA0_SOUT_SEL_IN	**Selects DISP_RDMA0 output** 0: Output to DISP_PATH0 1: Output to DISP_COLOR 2: Output to DSI0 3: Output to DSI1 4: Output to DPI0 Others: Reserved

14000094 DISP_RDMA1_SOUT_SEL_IN **DISP_RDMA1 Output Select** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DISP_RDMA1_SOUT_SEL_IN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DISP_RDMA1_SOUT_SEL_IN**	DISP_RDMA1_SOUT_SEL_IN	**Selects DISP_RDMA1 output** 0: Output to DISP_UFOE 1: Output to DISP_DSC Others: Reserved

14000098 DISP_OVL0 **DISP_OVL0 Output Select** **00000000**

SOUT_SEL_IN

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DISP_OVL0_SOUT_SEL_IN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DISP_OVL0_SOUT_SEL_IN**	DISP_OVL0_SOUT_SEL_IN	**Selects DISP_OVL0 output** 0: Output to DISP_OVL0_MOUT 1: Output to DISP_OVL1_2L Others: Reserved

1400009C DISP_OVL0_SEL_IN — **DISP_OVL0_MOUT Input Selection** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DISP_OVL0_SEL_IN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DISP_OVL0_SEL_IN**	DISP_OVL0_SEL_ IN	**Selects DISP_OVL0_MOUT input** 0: From DISP_OVL0 1: From DISP_OVL1 2: From DISP_OVL1_2L Others: Reserved

140000A0 DISP_OVL1_SOUT_SEL_IN — **DISP_OVL1_2L Output Select** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DISP_OVL1_SOUT_SEL_IN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DISP_OVL1_SOUT_SEL_IN**	DISP_OVL1_SOUT_SEL_IN	**Selects DISP_OVL1_2L output** 0: Output to DISP_OVL1 1: Output to DISP_OVL0_MOUT Others: Reserved

140000F0 MMSYS_MISC **MMSYS_MISC** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RDMA_VDE_IGNORE_UFOE_EMPTY	DSI1_TE_SEL	SMI_LARB0_TEST_MODE
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	**RDMA_VDE_IGNORE_UFOE_EMPTY**	RDMA_VDE_IGNORE_UFOE_EMPTY	**Decides whether RDMA_VDE will be influenced by DISP_UFOE empty flag** 0: RDMA_VDE will be influenced by DISP_UFOE empty flag 1: RDMA_VDE will ignore DISP_UFOE empty flag
1	**DSI1_TE_SEL**	DSI1_TE_SEL	**Selects DSI1 external TE** 0: Select DSI0_TE 1: Select DSI1_TE
0	**SMI_LARB0_TEST_MODE**	SMI_LARB0_TEST_MODE	**SMI_LARB0 test mode** 0: Normal mode 1: SMI_LARB0 test mode. All RDMA's output ready is tied to 1; all WDMA's input valid is tied to 1.

140000F4 MMSYS_SMI_LARB_SEL **MMSYS_SMI_LARB_SEL** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															DISP_WDMA0_LARB_SEL	DISP_OVL0_2L_LARB_SEL
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
1	**DISP_WDMA0_LARB_SEL**	DISP_WDMA0_LARB_SEL	**Selects which LARB for DISP_WDMA0 to hook to** 0: Hook DISP_WDMA0 SMI port to LARB0 1: Hook DISP_WDMA0 SMI port to LARB5
0	**DISP_OVL0_2L_LARB_SEL**	DISP_OVL0_2L_LARB_SEL	**Selects which LARB for DISP_OVL0_2L to hook to** 0: Hook DISP_OVL0_2L SMI port to LARB5 1: Hook DISP_OVL0_2L SMI port to LARB0

140000F8 MMSYS_SODI_REQ_MASK **MMSYS_SODI_REQ_MASK** **0000000F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													MMSYS_SODI_REQ_MASK			
Type													RW			
Reset													1	1	1	1

Bit(s)	Mnemonic	Name	Description
3:0	**MMSYS_SODI_REQ_MASK**	MMSYS_SODI_REQ_MASK	**SMI request mask for SODI** 0: Mask SMI request for SODI 1: Not to mask SMI request for SODI Bit 0: DISP_RDMA0 SMI request Bit 1: DISP_RDMA1 SMI request Bit 2: DISP_OD read SMI request Bit 3: DISP_OD write SMI request

14000100 MMSYS_CG_CON0 **MMSYS Clock Gating Config 0** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CG0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CG0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	**CG_CON0**	CG0	**Free run clock gating** 0: Enable clock or disable HW DCM 1: Clock gating or enable HW DCM Bit 0: SMI COMMON (CG) Bit 1: SMI LARB0 (CG) Bit 2: SMI LARB5 (CG) Bit 3: CAM_MDP (DCM) Bit 4: MDP_RDMA0 (DCM)

Bit(s)	Mnemonic	Name	Description
			Bit 5: MDP_RDMA1 (DCM) Bit 6: MDP_RSZ0 (DCM) Bit 7: MDP_RSZ1 (DCM) Bit 8: MDP_RSZ2 (DCM) Bit 9: MDP_TDSHP (DCM) Bit 10: MDP_COLOR (DCM) Bit 11: MDP_WDMA (DCM) Bit 12: MDP_WROT0 (DCM) Bit 13: MDP_WROT1 (DCM) Bit 14: FAKE_ENG (CG) Bit 15: DISP_OVL0 (DCM) Bit 16: DISP_OVL1 (DCM) Bit 17: DISP_OVL0_2L (DCM) Bit 18: DISP_OVL1_2L (DCM) Bit 19: DISP_RDMA0 (DCM) Bit 20: DISP_RDMA1 (DCM) Bit 21: DISP_WDMA0 (DCM) Bit 22: DISP_WDMA1 (DCM) Bit 23: DISP_COLOR (DCM) Bit 24: DISP_CCORR (DCM) Bit 25: DISP_AAL (DCM) Bit 26: DISP_GAMMA (DCM) Bit 27: DISP_OD (DCM) Bit 28: DISP_DITHER (DCM) Bit 29: DISP_UFOE (DCM) Bit 30: DISP_DSC (DCM) Bit 31: DISP_SPLIT (DCM)

14000104 MMSYS_CG_SET0 MMSYS Clock Gating Set 0 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CG0															
Type	WO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CG0															
Type	WO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	CG_SET0	CG0	**Sets up free run clock gating** 0: No effect 1: Clock gating or enable HW DCM Bit 0: SMI COMMON (CG) Bit 1: SMI LARB0 (CG) Bit 2: SMI LARB5 (CG) Bit 3: CAM_MDP (DCM) Bit 4: MDP_RDMA0 (DCM) Bit 5: MDP_RDMA1 (DCM) Bit 6: MDP_RSZ0 (DCM) Bit 7: MDP_RSZ1 (DCM) Bit 8: MDP_RSZ2 (DCM)

Bit(s)	Mnemonic	Name	Description
			Bit 9: MDP_TDSHP (DCM) Bit 10: MDP_COLOR (DCM) Bit 11: MDP_WDMA (DCM) Bit 12: MDP_WROT0 (DCM) Bit 13: MDP_WROT1 (DCM) Bit 14: FAKE_ENG (CG) Bit 15: DISP_OVL0 (DCM) Bit 16: DISP_OVL1 (DCM) Bit 17: DISP_OVL0_2L (DCM) Bit 18: DISP_OVL1_2L (DCM) Bit 19: DISP_RDMA0 (DCM) Bit 20: DISP_RDMA1 (DCM) Bit 21: DISP_WDMA0 (DCM) Bit 22: DISP_WDMA1 (DCM) Bit 23: DISP_COLOR (DCM) Bit 24: DISP_CCORR (DCM) Bit 25: DISP_AAL (DCM) Bit 26: DISP_GAMMA (DCM) Bit 27: DISP_OD (DCM) Bit 28: DISP_DITHER (DCM) Bit 29: DISP_UFOE (DCM) Bit 30: DISP_DSC (DCM) Bit 31: DISP_SPLIT (DCM)

14000108 MMSYS_CG_CLR0 MMSYS Clock Gating Clear 0 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CG0															
Type	WO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CG0															
Type	WO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	CG_CLR0	CG0	**Clears free run clock gating clear** 0: No effect 1: Enable clock or disable HW DCM Bit 0: SMI COMMON (CG) Bit 1: SMI LARB0 (CG) Bit 2: SMI LARB5 (CG) Bit 3: CAM_MDP (DCM) Bit 4: MDP_RDMA0 (DCM) Bit 5: MDP_RDMA1 (DCM) Bit 6: MDP_RSZ0 (DCM) Bit 7: MDP_RSZ1 (DCM) Bit 8: MDP_RSZ2 (DCM) Bit 9: MDP_TDSHP (DCM) Bit 10: MDP_COLOR (DCM) Bit 11: MDP_WDMA (DCM) Bit 12: MDP_WROT0 (DCM)

Bit(s)	Mnemonic	Name	Description
			Bit 13: MDP_WROT1 (DCM) Bit 14: FAKE_ENG (CG) Bit 15: DISP_OVL0 (DCM) Bit 16: DISP_OVL1 (DCM) Bit 17: DISP_OVL0_2L (DCM) Bit 18: DISP_OVL1_2L (DCM) Bit 19: DISP_RDMA0 (DCM) Bit 20: DISP_RDMA1 (DCM) Bit 21: DISP_WDMA0 (DCM) Bit 22: DISP_WDMA1 (DCM) Bit 23: DISP_COLOR (DCM) Bit 24: DISP_CCORR (DCM) Bit 25: DISP_AAL (DCM) Bit 26: DISP_GAMMA (DCM) Bit 27: DISP_OD (DCM) Bit 28: DISP_DITHER (DCM) Bit 29: DISP_UFOE (DCM) Bit 30: DISP_DSC (DCM) Bit 31: DISP_SPLIT (DCM)

14000110 MMSYS_CG_CON1 MMSYS Clock Gating Config 1 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CG1															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CG1															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	CG_CON1	CG1	**Free run clock gating** 0: Enable clock or disable HW DCM 1: Clock gating or enable HW DCM Bit 0: DSI0 MM clock (CG) Bit 1: DSI0 interface clock (CG) Bit 2: DSI1 MM clock (CG) Bit 3: DSI1 interface clock (CG) Bit 4: DPI MM clock (CG) Bit 5: DPI interface clock (DCM) Bit 6: LARB4_AXI_ASIF MM clock (CG) Bit 7: LARB4_AXI_ASIF MJC clock (CG) Bit 8: DISP_OVL0_MOUT clock (DCM) Bit 9: FAKE_ENG2 (CG) Others: Reserved

14000114 MMSYS_CG_SET1 MMSYS Clock Gating Set 1 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	CG1															
Type	WO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CG1															
Type	WO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	**CG_SET1**	CG1	**Sets up free run clock gating** 0: No effect 1: Clock gating or enable HW DCM Bit 0: DSI0 MM clock (CG) Bit 1: DSI0 interface clock (CG) Bit 2: DSI1 MM clock (CG) Bit 3: DSI1 interface clock (CG) Bit 4: DPI MM clock (CG) Bit 5: DPI interface clock (DCM) Bit 6: LARB4_AXI_ASIF MM clock (CG) Bit 7: LARB4_AXI_ASIF MJC clock (CG) Bit 8: DISP_OVL0_MOUT clock (DCM) Bit 9: FAKE_ENG2 (CG) Others: Reserved

14000118 MMSYS_CG_CLR1 MMSYS Clock Gating Clr 1 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CG1															
Type	WO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CG1															
Type	WO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	**CG_CLR1**	CG1	**Clears free run clock gating** 0: No effect 1: Enable clock or disable HW DCM Bit 0: DSI0 MM clock (CG) Bit 1: DSI0 interface clock (CG) Bit 2: DSI1 MM clock (CG) Bit 3: DSI1 interface clock (CG) Bit 4: DPI MM clock (CG) Bit 5: DPI interface clock (DCM) Bit 6: LARB4_AXI_ASIF MM clock (CG) Bit 7: LARB4_AXI_ASIF MJC clock (CG) Bit 8: DISP_OVL0_MOUT clock (DCM) Bit 9: FAKE_ENG2 (CG) Others: Reserved

14000120 MMSYS_HW_DCM_DIS0 MMSYS Hardware DCM Disable 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DCM_DIS0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCM_DIS0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	HW_DCM_DIS0	DCM_DIS0	**Disables hardware DCM 0** 0: Enable HW DCM 1: Disable HW DCM Bit 0: MDP_RDMA0 Bit 1: MDP_RDMA1 Bit 2: MDP_RSZ0 Bit 3: MDP_RSZ1 Bit 4: MDP_RSZ2 Bit 5: MDP_TDSHP Bit 6: MDP_COLOR Bit 7: MDP_WDMA Bit 8: MDP_WROT0 Bit 9: MDP_WROT1 Bit 10: DISP_OVL0 Bit 11: DISP_OVL1 Bit 12: DISP_OVL0_2L Bit 13: DISP_OVL1_2L Bit 14: DISP_RDMA0 Bit 15: DISP_RDMA1 Bit 16: DISP_WDMA0 Bit 17: DISP_WDMA1 Bit 18: DISP_COLOR Bit 19: DISP_CCORR Bit 20: DISP_AAL Bit 21: DISP_GAMMA Bit 22: DISP_OD Bit 23: DISP_DITHER Bit 24: DISP_UFOE Bit 25: DISP_DSC Bit 26: DISP_DSI0 FIFO Bit 27: DISP_DSI1 FIFO Bit 28: DISP_DPI Others: Reserved

14000124 MMSYS_HW_DCM_DIS_SET MMSYS Hardware DCM Disable Set 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DCM_DIS0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	DCM_DIS0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**HW_DCM_DIS_SET0**	DCM_DIS0	**Sets up hardware DCM 0 disable** 0: No effect 1: Disable HW DCM Bit 0: MDP_RDMA0 Bit 1: MDP_RDMA1 Bit 2: MDP_RSZ0 Bit 3: MDP_RSZ1 Bit 4: MDP_RSZ2 Bit 5: MDP_TDSHP Bit 6: MDP_COLOR Bit 7: MDP_WDMA Bit 8: MDP_WROT0 Bit 9: MDP_WROT1 Bit 10: DISP_OVL0 Bit 11: DISP_OVL1 Bit 12: DISP_OVL0_2L Bit 13: DISP_OVL1_2L Bit 14: DISP_RDMA0 Bit 15: DISP_RDMA1 Bit 16: DISP_WDMA0 Bit 17: DISP_WDMA1 Bit 18: DISP_COLOR Bit 19: DISP_CCORR Bit 20: DISP_AAL Bit 21: DISP_GAMMA Bit 22: DISP_OD Bit 23: DISP_DITHER Bit 24: DISP_UFOE Bit 25: DISP_DSC Bit 26: DISP_DSI0 FIFO Bit 27: DISP_DSI1 FIFO Bit 28: DISP_DPI Others: Reserved

14000128 MMSYS_HW_DCM_DIS_CLR MMSYS Hardware DCM Disable Clear 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DCM_DIS0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCM_DIS0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**HW_DCM_DIS_CLR0**	DCM_DIS0	**Clears hardware DCM 0 disable** 0: No effect

Bit(s)	Mnemonic	Name	Description
			1: Enable HW DCM Bit 0: MDP_RDMA0 Bit 1: MDP_RDMA1 Bit 2: MDP_RSZ0 Bit 3: MDP_RSZ1 Bit 4: MDP_RSZ2 Bit 5: MDP_TDSHP Bit 6: MDP_COLOR Bit 7: MDP_WDMA Bit 8: MDP_WROT0 Bit 9: MDP_WROT1 Bit 10: DISP_OVL0 Bit 11: DISP_OVL1 Bit 12: DISP_OVL0_2L Bit 13: DISP_OVL1_2L Bit 14: DISP_RDMA0 Bit 15: DISP_RDMA1 Bit 16: DISP_WDMA0 Bit 17: DISP_WDMA1 Bit 18: DISP_COLOR Bit 19: DISP_CCORR Bit 20: DISP_AAL Bit 21: DISP_GAMMA Bit 22: DISP_OD Bit 23: DISP_DITHER Bit 24: DISP_UFOE Bit 25: DISP_DSC Bit 26: DISP_DSI0 FIFO Bit 27: DISP_DSI1 FIFO Bit 28: DISP_DPI Others: Reserved

14000130 MMSYS_HW_DCM_DIS1 MMSYS Hardware DCM Disable 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DCM_DIS1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCM_DIS1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	HW_DCM_DIS1	DCM_DIS1	**Disables hardware DCM 1** 0: Enable HW DCM 1: Disable HW DCM Bit 0: DSI0 Bit 1: DSI1 Others: Reserved

14000134 MMSYS_HW_DCM_DIS_SET1 **MMSYS Hardware DCM Disable Set 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DCM_DIS1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCM_DIS1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**HW_DCM_DIS_SET1**	DCM_DIS1	**Sets up hardware DCM 1 disable** 0: No effect 1: Disable HW DCM Bit 0: DSI0 Bit 1: DSI1 Others: Reserved

14000138 MMSYS_HW_DCM_DIS_CLR1 **MMSYS Hardware DCM Disable Clear 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DCM_DIS1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCM_DIS1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**HW_DCM_DIS_CLR1**	DCM_DIS1	**Clears hardware DCM 1 disable** 0: No effect 1: Enable HW DCM Bit 0: DSI0 Bit 1: DSI1 Others: Reserved

14000140 MMSYS_SW0_RST_B **MMSYS Software Reset** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SW0_RST_B															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SW0_RST_B															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	**SW0_RST_B**	SW0_RST_B	**Software reset 0** 0: Reset 1: Does not reset Bit 0: SMI_COMMON Bit 1: SMI_LARB0 Bit 2: SMI_LARB5 Bit 3: CAM_MDP Bit 4: MDP_RDMA0 Bit 5: MDP_RDMA1 Bit 6: MDP_RSZ0 Bit 7: MDP_RSZ1 Bit 8: MDP_RSZ2 Bit 9: MDP_TDSHP Bit 10: MDP_COLOR Bit 11: MDP_WDMA Bit 12: MDP_WROT0 Bit 13: MDP_WROT1 Bit 14: FAKE_ENG Bit 15: DISP_OVL0 Bit 16: DISP_OVL1 Bit 17: DISP_OVL0_2L Bit 18: DISP_OVL1_2L Bit 19: DISP_RDMA0 Bit 20: DISP_RDMA1 Bit 21: DISP_WDMA0 Bit 22: DISP_WDMA1 Bit 23: DISP_COLOR Bit 24: DISP_CCORR Bit 25: DISP_AAL Bit 26: DISP_GAMMA Bit 27: DISP_OD Bit 28: DISP_DITHER Bit 29: DISP_UFOE Bit 30: DISP_DSC Bit 31: DISP_SPLIT

14000144 MMSYS_SW1_RST_B **MMSYS Software Reset** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SW1_RST_B															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SW1_RST_B															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	**SW1_RST_B**	SW1_RST_B	**Reserved register** 0: Reset 1: Does not reset

Bit(s)	Mnemonic	Name	Description
			Bit 0: DSI0 Bit 1: DSI1 Bit 2: DPI Bit 3: SMI_COMMON_GLB Bit 4: SMI_LARB0_GLB Bit 5: SMI_LARB5_GLB Bit 6: AXI_ASIF Bit 7: SMI_N21MUX Bit 8: FAKE_ENG2 Others: Reserved

14000150 MMSYS_LCM_RST_B LCM Reset 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MMSYS_LCM_RST_B
Type																RW
Reset																1

Bit(s)	Mnemonic	Name	Description
0	MMSYS_LCM_RST_B	MMSYS_LCM_RST_B	Resets LCM 0: Reset 1: Does not reset

14000168 SMI_N21MUX_CFG_WR SMI_N21MUX_CFG_WR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMI_N21MUX_CFG_WR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMI_N21MUX_CFG_WR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	SMI_N21MUX_CFG_WR	SMI_N21MUX_CFG_WR	SMI_N21MUX_CFG_WR

1400016C SMI_N21MUX_CFG_RD SMI_N21MUX_CFG_RD 00000005

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	SMI_N21MUX_CFG_RD															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMI_N21MUX_CFG_RD															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit(s)	Mnemonic	Name	Description
31:0	**SMI_N21MUX_CFG_RD**	SMI_N21MUX_CFG_RD	SMI_N21MUX_CFG_RD

14000170 ELA2GMC_BASE_ADDR ELA2GMC_BASE_ADDR 00200000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ELA2GMC_BASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ELA2GMC_BASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ELA2GMC_BASE_ADDR**	ELA2GMC_BASE_ADDR	ELA2GMC_BASE_ADDR

14000174 ELA2GMC_BASE_ADDR_END ELA2GMC_BASE_ADDR_END 00240000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ELA2GMC_BASE_ADDR_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ELA2GMC_BASE_ADDR_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ELA2GMC_BASE_ADDR_END**	ELA2GMC_BASE_ADDR_END	ELA2GMC_BASE_ADDR_END

14000178 ELA2GMC_FINAL_ADDR ELA2GMC_FINAL_ADDR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ELA2GMC_FINAL_ADDR															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ELA2GMC_FINAL_ADDR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ELA2GMC_FINAL_ADDR**	ELA2GMC_FINAL_ADDR	ELA2GMC_FINAL_ADDR

1400017C ELA2GMC_STATUS ELA2GMC_STATUS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															ELA2GMC_FIFO_EMPTY	ELA2GMC_ERROR_FLAG
Type															RU	RU
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	**ELA2GMC_FIFO_EMPTY**	ELA2GMC_FIFO_EMPTY	ELA2GMC_FIFO_EMPTY
0	**ELA2GMC_ERROR_FLAG**	ELA2GMC_ERROR_FLAG	ELA2GMC_ERROR_FLAG

14000180 LARB4_AXI_ASIF_CFG_WD LARB4_AXI_ASIF_CFG_WD 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LARB4_AXI_ASIF_CFG_WD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LARB4_AXI_ASIF_CFG_WD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**LARB4_AXI_ASIF_CFG_WD**	LARB4_AXI_ASIF_CFG_WD	LARB4_AXI_ASIF_CFG_WD

14000184 LARB4_AXI_ASIF_CFG_R LARB4_AXI_ASIF_CFG_RD 00000000

D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LARB4_AXI_ASIF_CFG_RD															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LARB4_AXI_ASIF_CFG_RD															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**LARB4_AXI_ASIF_CFG_RD**	LARB4_AXI_ASIF_CFG_RD	LARB4_AXI_ASIF_CFG_RD

14000190 PROC_TRACK_EMI_BUSY_CON **Proc_Track EMI Busy Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PROC_TRACK_CFG_EMI_CHN_DIS			PROC_TRACK_EMI_BUSY_CONST	PROC_TRACK_EMI_BUSY_SEL
Type												RW			RW	RW
Reset												0			0	0

Bit(s)	Mnemonic	Name	Description
4	**PROC_TRACK_CFG_EMI_CHN_DIS**	PROC_TRACK_CFG_EMI_CHN_DIS	PROC_TRACK_CFG_EMI_CHN_DIS
1	**PROC_TRACK_EMI_BUSY_CONST**	PROC_TRACK_EMI_BUSY_CONST	PROC_TRACK_EMI_BUSY_CONST
0	**PROC_TRACK_EMI_BUSY_SEL**	PROC_TRACK_EMI_BUSY_SEL	PROC_TRACK_EMI_BUSY_SEL

14000200 DISP_FAKE_ENG_EN **DISP Fake Engine Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															DFE_START	DFE_EN
Type															RW	RW

Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	**DFE_START**	DFE_START	**After this bit is enabled, DFE will start to issue read/write command immediately.** Follow the programming sequence: Write DISP_FAKE_ENG_CON0; Write DISP_FAKE_ENG_CON1; Write DISP_FAKE_ENG_RD_ADDR; Write DISP_FAKE_ENG_WR_ADDR; Write DISP_FAKE_ENG_EN = 1; Write DISP_FAKE_ENG_EN = 3; While ((*DISP_FAKE_ENG_STATE & 1)!=0); *DISP_FAKE_ENG = 1; 0: Stop DFE 1: Start DFE
0	**DFE_EN**	DFE_EN	**Enables DISP Fake Engine** 0: Disable DFE 1: Enable DFE

14000204 DISP_FAKE_ENG_RST **DISP Fake Engine Reset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**DISP_FAKE_ENG_RST**
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**DISP_FAKE_ENG_RST**	DISP_FAKE_ENG_RST	**Resets DISP fake engine** 0: Does not reset 1: Reset

14000208 DISP_FAKE_ENG_CON0 **DISP Fake Engine Control 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**DFE_WR_PAT**				**DFE_DRE_EN**	**DFE_LOOP_MODE**			**DFE_TEST_LEN**			
Type					RW				RW	RW			RW			
Reset					0	0	0	0	0	0			0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DFE_TEST_LEN**															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24	**DFE_WR_PAT**	DFE_WR_PAT	**Controls Disp_fake_eng write pattern control** 0000: all zero 0001: toggle every 16bits 0010: toggle every 32bits 0011: toggle every 64bits 0100: toggle every 128bits 0101: toggle every 256bits 0110: toggle every 512bits 0111: all one
23	**DFE_DRE_EN**	DFE_DRE_EN	**When DRE is enabled, DFE will keep busy but mask commands to EMI.** 0: Disable 1: Enable
22	**DFE_LOOP_MODE**	DFE_LOOP_MODE	**When loop mode is enabled, DFE will issue read/write command continuously until DFE_START=0.** 0: Normal mode 1: Enable loop mode
19:0	**DFE_TEST_LEN**	DFE_TEST_LEN	**DFE test length in normal mode**

1400020C DISP_FAKE_ENG_CON1 **DISP Fake Engine Control 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									DFE_ULTRA_EN	DFE_ULTRA_CNT			DFE_PREULTRA_EN	DFE_PREULTRA_CNT		
Type									RW	RW			RW	RW		
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DFE_BURST_LENGTH				DFE_WR_DIS	DFE_RD_DIS	DFE_SLOW_DOWN									
Type	RW				RW	RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23	**DFE_ULTRA_EN**	DFE_ULTRA_EN	**DFE ultra enable** 0: Disable ultra request 1: Enable ultra request
22:20	**DFE_ULTRA_CNT**	DFE_ULTRA_CNT	**DFE ultra ratio** 0~7: ultra percentage
19	**DFE_PREULTRA_EN**	DFE_PREULTRA_EN	**DFE preultra enable** 0: Disable preultra request 1: Enable preultra request
18:16	**DFE_PREULTRA_CNT**	DFE_PREULTRA_CNT	**DFE preultra ratio** 0~7: preultra percentage
15:12	**DFE_BURST_LENGTH**	DFE_BURST_LENGTH	**DFE request burst length** 0~7: single/burst-2~8
11	**DFE_WR_DIS**	DFE_WR_DIS	**Disables DFE write commands** 0: Enable write requests 1: Disable write requests

Bit(s)	Mnemonic	Name	Description
10	**DFE_RD_DIS**	DFE_RD_DIS	**Disables DFE read commands** 0: Enable read requests 1: Disable read requests
9:0	**DFE_SLOW_DOWN**	DFE_SLOW_DOWN	**Slow-down counter**

14000210 DISP_FAKE_ENG_RD_ADDR — DISP Fake Engine Read Address — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DISP_FAKE_ENG_RD_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_FAKE_ENG_RD_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DISP_FAKE_ENG_RD_ADDR**	DISP_FAKE_ENG_RD_ADDR	DISP fake engine read address

14000214 DISP_FAKE_ENG_WR_ADDR — DISP Fake Engine Write Address — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DISP_FAKE_ENG_WR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_FAKE_ENG_WR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DISP_FAKE_ENG_WR_ADDR**	DISP_FAKE_ENG_WR_ADDR	DISP fake engine write address

14000218 DISP_FAKE_ENG_STATE — DISP Fake Engine Status — 00001100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DFE_RD_ST			DFE_WR_ST											DFE_BUSY
Type		RU			RU											RU

Reset		0	0	1	0	0	0	1								0

Bit(s)	Mnemonic	Name	Description
14:12	**DFE_RD_ST**	DFE_RD_ST	**DFE read engine state** 001: Idle 010: Busy 100: Finish
11:8	**DFE_WR_ST**	DFE_WR_ST	**DFE write engine state** 0001: Idle 0010: Busy 0100: Last 1000: Finish
0	**DFE_BUSY**	DFE_BUSY	**DFE busy**

14000220 DISP_FAKE_ENG2_EN **DISP Fake Engine 2 Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															DFE_START	DFE_EN
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	**DFE_START**	DFE_START	**After this bit is enabled, DFE will start to issue read/write command immediately.** Follow the programming sequence: Write DISP_FAKE_ENG_CON0; Write DISP_FAKE_ENG_CON1; Write DISP_FAKE_ENG_RD_ADDR; Write DISP_FAKE_ENG_WR_ADDR; Write DISP_FAKE_ENG_EN = 1; Write DISP_FAKE_ENG_EN = 3; While ((*DISP_FAKE_ENG_STATE & 1)!=0); *DISP_FAKE_ENG = 1; 0: Stop DFE 1: Start DFE
0	**DFE_EN**	DFE_EN	**Enables DISP Fake Engine** 0: Disable DFE 1: Enable DFE

14000224 DISP_FAKE_ENG2_RST **DISP Fake Engine 2 Reset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name																DISP_FAKE_ENG_RST
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**DISP_FAKE_ENG_RST**	DISP_FAKE_ENG_RST	**Resets DISP fake engine** 0: Does not reset 1: Reset

14000228 DISP_FAKE_ENG2_CON0 **DISP Fake Engine 2 Control 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DFE_WR_PAT				DFE_DRE_EN	DFE_LOOP_MODE			DFE_TEST_LEN			
Type					RW				RW	RW			RW			
Reset					0	0	0	0	0	0			0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DFE_TEST_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24	**DFE_WR_PAT**	DFE_WR_PAT	**Controls DISP_FAKE_ENG write pattern** 0000: All zero 0001: Toggle every 16 bits 0010: Toggle every 32 bits 0011: Toggle every 64 bits 0100: Toggle every 128 bits 0101: Toggle every 256 bits 0110: Toggle every 512 bits 0111: All one
23	**DFE_DRE_EN**	DFE_DRE_EN	**When DRE is enabled, DFE will keep busy but mask commands to EMI.** 0: Disable 1: Enable
22	**DFE_LOOP_MODE**	DFE_LOOP_MODE	**When loop mode is enabled, DFE will issue read/write command continuously until DFE_START=0.** 0: Normal mode 1: Enable loop mode
19:0	**DFE_TEST_LEN**	DFE_TEST_LEN	**DFE test length in normal mode**

1400022C DISP_FAKE_ENG2_CON1 **DISP Fake Engine 2 Control 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									DFE_ULTR	DFE_ULTRA_CNT			DFE_PREU	DFE_PREULTRA_CNT		

									A_EN				LTRA_EN			
Type									RW	RW			RW	RW		
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DFE_BURST_LENGTH				DFE_WR_DIS	DFE_RD_DIS	DFE_SLOW_DOWN									
Type	RW				RW	RW	RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23	**DFE_ULTRA_EN**	DFE_ULTRA_EN	**Enables DFE ultra** 0: Disable ultra request 1: Enable ultra request
22:20	**DFE_ULTRA_CNT**	DFE_ULTRA_CNT	**DFE ultra ratio** 0~7: Ultra percentage
19	**DFE_PREULTRA_EN**	DFE_PREULTRA_EN	**Enables DFE preultra** 0: Disable preultra request 1: Enable preultra request
18:16	**DFE_PREULTRA_CNT**	DFE_PREULTRA_CNT	**DFE preultra ratio** 0~7: Preultra percentage
15:12	**DFE_BURST_LENGTH**	DFE_BURST_LENGTH	**DFE request burst length** 0~7: Single/burst-2~8
11	**DFE_WR_DIS**	DFE_WR_DIS	**Disables DFE write commands** 0: Enable write requests 1: Disable write requests
10	**DFE_RD_DIS**	DFE_RD_DIS	**Disables DFE read commands** 0: Enable read requests 1: Disable read requests
9:0	**DFE_SLOW_DOWN**	DFE_SLOW_DOWN	**Slow-down counter**

14000230 DISP_FAKE_ENG2_RD_ADDR — DISP Fake Engine 2 Read Address — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DISP_FAKE_ENG_RD_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_FAKE_ENG_RD_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DISP_FAKE_ENG_RD_ADDR**	DISP_FAKE_ENG_RD_ADDR	DISP fake engine read address

14000234 DISP_FAKE_ENG2_WR_ADDR — DISP Fake Engine 2 Write Address — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	DISP_FAKE_ENG_WR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_FAKE_ENG_WR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DISP_FAKE_ENG_WR_ADDR**	DISP_FAKE_ENG_WR_ADDR	DISP fake engine write address

14000238 DISP_FAKE_ENG2_STATE — DISP Fake Engine 2 Status — 00001100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DFE_RD_ST			DFE_WR_ST											DFE_BUSY
Type		RU			RU											RU
Reset		0	0	1	0	0	0	1								0

Bit(s)	Mnemonic	Name	Description
14:12	**DFE_RD_ST**	DFE_RD_ST	**DFE read engine state** 001: Idle 010: Busy 100: Finish
11:8	**DFE_WR_ST**	DFE_WR_ST	**DFE write engine state** 0001: Idle 0010: Busy 0100: Last 1000: Finish
0	**DFE_BUSY**	DFE_BUSY	**DFE busy**

14000800 MMSYS_MBIST_CON — MMSYS MBIST Control — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														MMSYS_MBIST_BACKGROUND		
Type														RW		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMSYS_MBIST_RSTB				MMSYS_MBIST_SCANOUT_SEL				MMSYS_MBIST_DEBUG		MMSYS_MBIST_FAILOUT_SEL					
Type	RW				RW				RW		RW					

Reset	0				0	0	0	0	0		0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
18:16	**MMSYS_MBIST_BACKGROUND**	MMSYS_MBIST_BACKGROUND	MMSYS_MBIST_BACKGROUND
15	**MMSYS_MBIST_RSTB**	MMSYS_MBIST_RSTB	MMSYS_MBIST_RSTB
11:8	**MMSYS_MBIST_SCANOUT_SEL**	MMSYS_MBIST_SCANOUT_SEL	MMSYS_MBIST_SCANOUT_SEL
7	**MMSYS_MBIST_DEBUG**	MMSYS_MBIST_DEBUG	MMSYS_MBIST_DEBUG
5:0	**MMSYS_MBIST_FAILOUT_SEL**	MMSYS_MBIST_FAILOUT_SEL	MMSYS_MBIST_FAILOUT_SEL

14000804 MMSYS_MBIST_DONE — MMSYS MBIST Done — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										MMSYS_MBIST_DONE						
Type										RU						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMSYS_MBIST_DONE															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
22:0	**MMSYS_MBIST_DONE**	MMSYS_MBIST_DONE	MMSYS MBIST done

14000808 MMSYS_MBIST_HOLDB — MMSYS MBIST holdb — FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMSYS_MBIST_RESERVED									MMSYS_MBIST_HOLDB						
Type	RW									RW						
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMSYS_MBIST_HOLDB															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:23	**MMSYS_MBIST_RESERVED**	MMSYS_MBIST_RESERVED	MMSYS MBIST reserved
22:0	**MMSYS_MBIST_HOLDB**	MMSYS_MBIST_HOLDB	MMSYS MBIST holdb

1400080C MMSYS_MBIST_MODE — MMSYS MBIST Mode — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name										MMSYS_MBIST_MODE						
Type										RW						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMSYS_MBIST_MODE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
22:0	**MMSYS_MBIST_MODE**	MMSYS_MBIST_MODE	MMSYS MBIST mode

14000810 MMSYS_MBIST_FAIL0 MMSYS MBIST Fail 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMSYS_MBIST_FAIL0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMSYS_MBIST_FAIL0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**MMSYS_MBIST_FAIL0**	MMSYS_MBIST_FAIL0	MMSYS MBIST fail 0

14000814 MMSYS_MBIST_FAIL1 MMSYS MBIST Fail 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMSYS_MBIST_FAIL1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMSYS_MBIST_FAIL1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**MMSYS_MBIST_FAIL1**	MMSYS_MBIST_FAIL1	MMSYS MBIST fail 1

14000818 MMSYS_MBIST_FAIL2 MMSYS MBIST Fail 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMSYS_MBIST_FAIL2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMSYS_MBIST_FAIL2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**MMSYS_MBIST_FAIL2**	MMSYS_MBIST_FAIL2	MMSYS MBIST fail 2

1400081C MMSYS_MBIST_FAIL3 MMSYS MBIST Fail 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMSYS_MBIST_FAIL3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMSYS_MBIST_FAIL3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**MMSYS_MBIST_FAIL3**	MMSYS_MBIST_FAIL3	MMSYS MBIST fail 3

14000820 MMSYS_MBIST_BSEL0 MMSYS MBIST BSEL 0 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDP_TDSHP_MBIST_BSEL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
15:0	**MDP_TDSHP_MBIST_BSEL**	MDP_TDSHP_MBIST_BSEL	MDP_TDSHP_MBIST_BSEL

14000824 MMSYS_MBIST_BSEL1 MMSYS MBIST BSEL 1 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MDP_WROT1_MBIST_BSEL								MDP_WROT0_MBIST_BSEL							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDP_RDMA1_MBIST_BSEL						MDP_RDMA0_MBIST_BSEL									
Type	RW						RW									

Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24	**MDP_WROT1_MBIST_BSEL**	MDP_WROT1_MBIST_BSEL	MDP_WROT1_MBIST_BSEL
23:16	**MDP_WROT0_MBIST_BSEL**	MDP_WROT0_MBIST_BSEL	MDP_WROT0_MBIST_BSEL
15:10	**MDP_RDMA1_MBIST_BSEL**	MDP_RDMA1_MBIST_BSEL	MDP_RDMA1_MBIST_BSEL
9:0	**MDP_RDMA0_MBIST_BSEL**	MDP_RDMA0_MBIST_BSEL	MDP_RDMA0_MBIST_BSEL

14000828 MMSYS_MBIST_BSEL2 — MMSYS MBIST BSEL 2 — 0FFF0FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					MDP_RSZ1_MBIST_BSEL											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					MDP_RSZ0_MBIST_BSEL											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
27:16	**MDP_RSZ1_MBIST_BSEL**	MDP_RSZ1_MBIST_BSEL	MDP_RSZ1_MBIST_BSEL
11:0	**MDP_RSZ0_MBIST_BSEL**	MDP_RSZ0_MBIST_BSEL	MDP_RSZ0_MBIST_BSEL

1400082C MMSYS_MBIST_BSEL3 — MMSYS MBIST BSEL 3 — 003F0FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											DISP_UFOE_MBIST_BSEL					
Type											RW					
Reset											1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					MDP_RSZ2_MBIST_BSEL											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
21:16	**DISP_UFOE_MBIST_BSEL**	DISP_UFOE_MBIST_BSEL	DISP_UFOE_MBIST_BSEL
11:0	**MDP_RSZ2_MBIST_BSEL**	MDP_RSZ2_MBIST_BSEL	MDP_RSZ2_MBIST_BSEL

14000840 MDP_RDMA_MEM_DELSEL — MDP_RDMA Memory Delay Select — AAAAAAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MDP_RDMA1_MEM_DELSEL															
Type	RW															
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDP_RDMA0_MEM_DELSEL															
Type	RW															
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
31:16	**MDP_RDMA1_MEM_DELSEL**	MDP_RDMA1_MEM_DELSEL	MDP_RDMA1_MEM_DELSEL
15:0	**MDP_RDMA0_MEM_DELSEL**	MDP_RDMA0_MEM_DELSEL	MDP_RDMA0_MEM_DELSEL

14000844 MDP_RSZ_MEM_DELSEL — MDP_RSZ Memory Delay Select — 0AAAAAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					MDP_RSZ_MEM_DELSEL											
Type					RW											
Reset					1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDP_RSZ_MEM_DELSEL															
Type	RW															
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
27:0	**MDP_RSZ_MEM_DELSEL**	MDP_RSZ_MEM_DELSEL	MDP_RSZ_MEM_DELSEL

14000848 MDP_TDSHP_MEM_DELSEL — MDP_TDSHP Memory Delay Select — 0000000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													MDP_TDSHP_MEM_DELSEL			
Type													RW			
Reset													1	0	1	0

Bit(s)	Mnemonic	Name	Description
3:0	**MDP_TDSHP_MEM_DELSEL**	MDP_TDSHP_MEM_DELSEL	MDP_TDSHP_MEM_DELSEL

1400084C MDP_WDMA_MEM_DELSEL — MDP_WDMA Memory Delay Select — 000000AA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MDP_WDMA_MEM_DELSEL							
Type									RW							
Reset									1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0	**MDP_WDMA_MEM_DELSEL**	MDP_WDMA_MEM_DELSEL	MDP_WDMA_MEM_DELSEL

14000850 MDP_WROT_MEM_DELSEL **MDP_WROT Memory Delay Select** **0AAAAAAA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					MDP_WROT_MEM_DELSEL											
Type					RW											
Reset					1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDP_WROT_MEM_DELSEL															
Type	RW															
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
27:0	**MDP_WROT_MEM_DELSEL**	MDP_WROT_MEM_DELSEL	MDP_WROT_MEM_DELSEL

14000854 DISP_OVL_MEM_DELSEL **DISP_OVL Memory Delay Select** **0000000A**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DISP_OVL_MEM_DELSEL			
Type													RW			
Reset													1	0	1	0

Bit(s)	Mnemonic	Name	Description
3:0	**DISP_OVL_MEM_DELSEL**	DISP_OVL_MEM_DELSEL	DISP_OVL_MEM_DELSEL

14000858 DISP_OVL_2L_MEM_DELSEL **DISP_OVL_2L Memory Delay Select** **0000000A**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DISP_OVL_2L_MEM_DELSEL			
Type													RW			
Reset													1	0	1	0

Bit(s)	Mnemonic	Name	Description
3:0	**DISP_OVL_2L_MEM_DELSEL**	DISP_OVL_2L_MEM_DELSEL	DISP_OVL_2L_MEM_DELSEL

1400085C DISP_RDMA_MEM_DELSEL — **DISP_RDMA Memory Delay Select** — **0000000A**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DISP_RDMA_MEM_DELSEL			
Type													RW			
Reset													1	0	1	0

Bit(s)	Mnemonic	Name	Description
3:0	**DISP_RDMA_MEM_DELSEL**	DISP_RDMA_MEM_DELSEL	DISP_RDMA_MEM_DELSEL

14000860 DISP_WDMA0_MEM_DELSEL — **DISP_WDMA0 Memory Delay Select** — **000000AA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DISP_WDMA0_MEM_DELSEL							
Type									RW							
Reset									1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0	**DISP_WDMA0_MEM_DELSEL**	DISP_WDMA0_MEM_DELSEL	DISP_WDMA0_MEM_DELSEL

14000864 DISP_WDMA1 — **DISP_WDMA1 Memory Delay** — **000000AA**

_MEM_DELSEL Select

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DISP_WDMA1_MEM_DELSEL							
Type									RW							
Reset									1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0	**DISP_WDMA1_MEM_DELSEL**	DISP_WDMA1_MEM_DELSEL	DISP_WDMA1_MEM_DELSEL

14000868 DISP_GAMMA_MEM_DELSEL **DISP_GAMMA Memory Delay Select** **0000000A**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DISP_GAMMA_MEM_DELSEL			
Type													RW			
Reset													1	0	1	0

Bit(s)	Mnemonic	Name	Description
3:0	**DISP_GAMMA_MEM_DELSEL**	DISP_GAMMA_MEM_DELSEL	DISP_GAMMA_MEM_DELSEL

1400086C DSI_MEM_DELSEL **DSI Memory Delay Select** **0000000A**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DSI_MEM_DELSEL			
Type													RW			
Reset													1	0	1	0

Bit(s)	Mnemonic	Name	Description
3:0	**DSI_MEM_DELSEL**	DSI_MEM_DELSEL	DSI_MEM_DELSEL

14000870 DISP_UFOE_MEM_DELSEL — **DISP_UFOE Memory Delay Select** — **00000AAA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DISP_UFOE_MEM_DELSEL											
Type					RW											
Reset					1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
11:0	**DISP_UFOE_MEM_DELSEL**	DISP_UFOE_MEM_DELSEL	DISP_UFOE_MEM_DELSEL

14000874 DISP_DSC_MEM_DELSEL — **DISP_DSC Memory Delay Select** — **0000AAAA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_DSC_MEM_DELSEL															
Type	RW															
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
15:0	**DISP_DSC_MEM_DELSEL**	DISP_DSC_MEM_DELSEL	DISP_DSC_MEM_DELSEL

14000878 DISP_OD_MEM_DELSELo — **DISP_OD Memory Delay Select o** — **AAAAAAAA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DISP_OD_MEM_DELSELo															
Type	RW															
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_OD_MEM_DELSELo															
Type	RW															
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
31:0	**DISP_OD_MEM_DELSELo**	DISP_OD_MEM_DELSELo	DISP_OD_MEM_DELSELo

1400087C DISP_OD_MEM_DELSEL1 — **DISP_OD Memory Delay Select 1** — **00000AAA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DISP_OD_MEM_DELSEL1											
Type					RW											
Reset					1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
11:0	**DISP_OD_MEM_DELSEL1**	DISP_OD_MEM_DELSEL1	DISP_OD_MEM_DELSEL1

14000880 MMSYS_DEBUG_OUT_SEL — MMSYS Debug Output Select — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												MMSYS_DEBUG_OUT_SEL				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0	**MMSYS_DEBUG_OUT_SEL**	MMSYS_DEBUG_OUT_SEL	MMSYS_DEBUG_OUT_SEL

14000884 MMSYS_MBIST_RP_RST_B — MMSYS MBIST Repair Reset — 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MMSYS_MBIST_RP_RST_B
Type																RW
Reset																1

Bit(s)	Mnemonic	Name	Description
0	**MMSYS_MBIST_RP_RST_B**	MMSYS_MBIST_RP_RST_B	MMSYS MBIST Repair Reset

14000888 MMSYS_MBIST_RP_FAIL **MMSYS MBIST Repair Fail** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															MDP_WROT1_MBIST_RP_FAIL	MDP_WROT0_MBIST_RP_FAIL
Type															RU	RU
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	**MDP_WROT1_MBIST_RP_FAIL**	MDP_WROT1_MBIST_RP_FAIL	MMSYS MBIST Repair Fail
0	**MDP_WROT0_MBIST_RP_FAIL**	MDP_WROT0_MBIST_RP_FAIL	

1400088C MMSYS_MBIST_RP_OK **MMSYS MBIST Repair OK** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															MDP_WROT1_MBIST_RP_OK	MDP_WROT0_MBIST_RP_OK
Type															RU	RU
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	**MDP_WROT1_MBIST_RP_OK**	MDP_WROT1_MBIST_RP_OK	MMSYS MBIST Repair OK
0	**MDP_WROT0_MBIST_RP_OK**	MDP_WROT0_MBIST_RP_OK	

14000890 MMSYS_DUMMY0 **MMSYS Dummy Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMSYS_DUMMY0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMSYS_DUMMY0												DISP_OVL1_SOUT_EC			

													O_SEL_IN			
Type	RW												RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:4	**MMSYS_DUMMY0**	MMSYS_DUMMY0	**MMSYS_DUMMY0**
3:0	**DISP_OVL1_SOUT_ECO_SEL_IN**	DISP_OVL1_SOUT_ECO_SEL_IN	**Selects DISP_OVL1_MOUT path 2 output** 0: Output to DISP_OVL0_SEL 1: Output to DISP_OVL0 Others: Reserved

14000894 MMSYS_DUMMY1 MMSYS Dummy Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMSYS_DUMMY1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMSYS_DUMMY1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**MMSYS_DUMMY1**	MMSYS_DUMMY1	MMSYS_DUMMY1

14000898 MMSYS_DUMMY2 MMSYS Dummy Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMSYS_DUMMY2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMSYS_DUMMY2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**MMSYS_DUMMY2**	MMSYS_DUMMY2	MMSYS_DUMMY2

1400089C MMSYS_DUMMY3 MMSYS Dummy Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMSYS_DUMMY3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMSYS_DUMMY3															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**MMSYS_DUMMY3**	MMSYS_DUMMY3	MMSYS_DUMMY3

140008A0 DISP_DL_VALID_0 DISP Direct Link Valid Status 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DISP_DL_VALID_0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_DL_VALID_0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DISP_DL_VALID_0**	DISP_DL_VALID_0	DISP direct link valid status 0

140008A4 DISP_DL_VALID_1 DISP Direct Link Valid Status 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DISP_DL_VALID_1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_DL_VALID_1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DISP_DL_VALID_1**	DISP_DL_VALID_1	DISP direct link valid status 1

140008A8 DISP_DL_READY_0 DISP Direct Link READY Status 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DISP_DL_READY_0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_DL_READY_0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DISP_DL_READY_0**	DISP_DL_READY_0	DISP direct link ready status 0

Bit(s)	Mnemonic	Name	Description

140008AC DISP_DL_READY_1 — **DISP Direct Link READY Status 1** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DISP_DL_READY_1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_DL_READY_1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	DISP_DL_READY_1	DISP_DL_READY_1	DISP direct link ready status 1

140008B0 MDP_DL_VALID_0 — **MDP Direct Link Valid Status 0** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MDP_DL_VALID_0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDP_DL_VALID_0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	MDP_DL_VALID_0	MDP_DL_VALID_0	MDP direct link valid status 0

140008B4 MDP_DL_VALID_1 — **MDP Direct Link Valid Status 1** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MDP_DL_VALID_1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDP_DL_VALID_1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	MDP_DL_VALID_1	MDP_DL_VALID_1	MDP direct link valid status 1

140008B8 MDP_DL_READY_0 — **MDP Direct Link READY Status 0** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MDP_DL_READY_0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDP_DL_READY_0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**MDP_DL_READY_0**	MDP_DL_READY_0	MDP direct link ready status 0

140008BC MDP_DL_READY_1 — MDP Direct Link READY Status 1 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MDP_DL_READY_1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDP_DL_READY_1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**MDP_DL_READY_1**	MDP_DL_READY_1	MDP direct link ready status 1

140008C0 SMI_LARB0_GREQ — SMI LARB0 Request — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SMI_LARB5_GREQ									
Type							RU									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SMI_LARB0_GREQ							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25:16	**SMI_LARB5_GREQ**	SMI_LARB5_GREQ	SMI LARB5 request
7:0	**SMI_LARB0_GREQ**	SMI_LARB0_GREQ	SMI LARB0 request

140008D0 DISP_MOUT_MASK — DISP Multiple Output Mask Status — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									DISP_MOUT_MASK							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_MOUT_MASK															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0	**DISP_MOUT_MASK**	DISP_MOUT_MASK	DISP multiple output mask status

140008D4 MDP_MOUT_MASK **MDP Multiple Output Mask Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									MDP_MOUT_MASK							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDP_MOUT_MASK															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0	**MDP_MOUT_MASK**	MDP_MOUT_MASK	MDP multiple output mask status

Module name: DISP_UFOE Base address: (+14019000h)

Address	Name	Width	Register Function
14019000	**DISP_UFO_START**	32	Configuration
14019004	**DISP_UFO_INTEN**	32	Interrupt Enable
14019008	**DISP_UFO_INTSTA**	32	Interrupt Status
1401900C	**DISP_UFO_DBUF**	32	UFO DBUF Control
14019014	**DISP_UFO_CRC**	32	CRC Enable
14019018	**DISP_UFO_SW_SCRATCH**	32	Software Scratch
14019020	**DISP_UFO_CR0P6_PAD**	32	CR0.6 Padding Control
14019024	**DISP_UFO_LR_OVERLAP**	32	LR Overlap
14019028	**DISP_UFO_CK_ON**	32	Clock Force On
14019030	**DISP_UFO_STALL_CG**	32	Clock gating during stall
14019050	**DISP_UFO_FRAME_WIDTH**	32	Wrapper Internal IP Width
14019054	**DISP_UFO_FRAME_HEIGHT**	32	Wrapper Internal IP Height
14019058	**DISP_UFO_OUTEN**	32	Output Enable Control
140190F0	**DISP_UFO_R0_CRC**	32	Wrapper R0 CRC
14019100	**DISP_UFO_CFG_0B**	32	DISP_UFO_CFG_0
14019104	**DISP_UFO_CFG_1B**	32	DISP_UFO_CFG_1
14019108	**DISP_UFO_CFG_2B**	32	DISP_UFO_CFG_2

Address	Name	Width	Register Function
1401910C	DISP_UFO_CFG_3B	32	DISP_UFO_CFG_3
14019110	DISP_UFO_CFG_4B	32	DISP_UFO_CFG_4
14019120	DISP_UFO_RO_0B	32	DISP_UFO_RO_0
14019124	DISP_UFO_RO_1B	32	DISP_UFO_RO_1
14019128	DISP_UFO_RO_2B	32	DISP_UFO_RO_2
1401912C	DISP_UFO_RO_3B	32	DISP_UFO_RO_3
14019130	DISP_UFO_RO_4B	32	DISP_UFO_RO_4
14019140	DISP_UFO_DBG0	32	DISP_UFO_DBG0
14019144	DISP_UFO_DBG1	32	DISP_UFO_DBG1
14019148	DISP_UFO_DBG2	32	DISP_UFO_DBG2
1401914C	DISP_UFO_DBG3	32	DISP_UFO_DBG3
14019150	DISP_UFO_DBG4	32	DISP_UFO_DBG4
14019154	DISP_UFO_DBG5	32	DISP_UFO_DBG5
14019158	DISP_UFO_DBG6	32	DISP_UFO_DBG6
1401915C	DISP_UFO_DBG7	32	DISP_UFO_DBG7

14019000 DISP_UFO_START Configuration 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									disp_ufo_dbg_sel							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								disp_ufo_sw_rst_engine					disp_ufo_lr_mode	disp_ufo_bypass	disp_ufo_out_sel	disp_ufo_start
Type								RW					RW	RW	RW	RW
Reset								0					0	1	0	0

Bit(s)	Name	Description
23:16	disp_ufo_dbg_sel	Selects debugging
8	disp_ufo_sw_rst_engine	Resets engine
3	disp_ufo_lr_mode	LR mode
2	disp_ufo_bypass	Bypases engine
1	disp_ufo_out_sel	Selects output
0	disp_ufo_start	Starts disp_color engine

14019004 DISP_UFO_INTEN Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name														disp_ufo_inten_fr_underrun	disp_ufo_inten_fr_done	disp_ufo_inten_fr_complete
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	disp_ufo_inten_fr_underrun	**Enables interrupt** frame_underrun
1	disp_ufo_inten_fr_done	**Enables interrupt** frame_done
0	disp_ufo_inten_fr_complete	**Enables interrupt** frame_complete

14019008 DISP_UFO_INTSTA **Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														disp_ufo_intsta_fr_underrun	disp_ufo_intsta_fr_done	disp_ufo_intsta_fr_complete
Type														A1	A1	A1
Reset														0	0	0

Bit(s)	Name	Description
2	disp_ufo_intsta_fr_underrun	**Interrupt status** Frame underrun
1	disp_ufo_intsta_fr_done	**Interrupt status** Frame done
0	disp_ufo_intsta_fr_complete	**Interrupt status** Frame completed

1401900C DISP_UFO_DBUF **UFO DBUF Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												disp_ufo_dbuf_dis				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	disp_ufo_dbuf_dis	Disables UFO shadow

14019014 DISP_UFO_CRC CRC Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														disp_ufo_crc_clr	disp_ufo_crc_start	disp_ufo_crc_cen
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	disp_ufo_crc_clr	Clears CRC
1	disp_ufo_crc_start	Starts CRC
0	disp_ufo_crc_cen	Enables CRC

14019018 DISP_UFO_SW_SCRATCH Software Scratch 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	disp_ufo_sw_scratch															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	disp_ufo_sw_scratch															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	disp_ufo_sw_scratch	sw_scratch

14019020 DISP_UFO_CR0P6_PAD CR0.6 Padding Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												disp_ufo_str_pad		disp_ufo_str_pad_num		

												_mode				
Type												RW		RW		
Reset												0		0	0	0

Bit(s)	Name	Description
4	disp_ufo_str_pad_mode	0: Pad to each (1/3 line) stream 1: Pad to each (2/3 line) stream
2:0	disp_ufo_str_pad_num	**Padding bytes**

14019024 DISP_UFO_LR_OVERLAP **LR Overlap** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						disp_ufo_lr_overlap										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	disp_ufo_lr_overlap	LR overlap

14019028 DISP_UFO_CK_ON **Clock Force On** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														disp_ufo_c_ck_on	disp_ufo_g_ck_on	disp_ufo_f_ck_on
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	disp_ufo_c_ck_on	Forces UFO core clock on
1	disp_ufo_g_ck_on	Forces gated clock on
0	disp_ufo_f_ck_on	Forces free-run clock on

14019030 DISP_UFO_STALL_CG **Clock gating during stall** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																disp_ufo_hg_stall_cg_on
Type																RW
Reset																0

Bit(s)	Name	Description
0	disp_ufo_hg_stall_cg_on	Stall hg clock during stall

14019050 DISP_UFO_FRAME_WIDTH — Wrapper Internal IP Width — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					disp_ufo_frame_width											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	disp_ufo_frame_width	Wrapper internal IP width

14019054 DISP_UFO_FRAME_HEIGHT — Wrapper Internal IP Height — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				disp_ufo_frame_height												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	disp_ufo_frame_height	Wrapper internal IP height

14019058 DISP_UFO_OUTEN — Output Enable Control — 00000040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								disp_ufo_out_stop	disp_ufo_out_th							
Type								RW	RW							
Reset								0	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
8	disp_ufo_out_stop	disp_ufo_out_stop
7:0	disp_ufo_out_th	disp_ufo_out_th

140190F0 DISP_UFO_R0_CRC — Wrapper R0 CRC — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															disp_ufo_engine_end	disp_ufo_crc_rdy_0
Type															RU	RU
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	disp_ufo_crc_out_0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	disp_ufo_engine_end	Engine end
16	disp_ufo_crc_rdy_0	Wrapper R0 CRC RDY
15:0	disp_ufo_crc_out_0	Wrapper R0 CRC data

14019100 DISP_UFO_CFG_0B — DISP_UFO_CFG_0 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	disp_ufo_cfg_0b															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	disp_ufo_cfg_0b															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	disp_ufo_cfg_0b	UFO configuration 0

14019104 DISP_UFO_CFG_1B **DISP_UFO_CFG_1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	disp_ufo_cfg_1b															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	disp_ufo_cfg_1b															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	disp_ufo_cfg_1b	UFO configuration 1

14019108 DISP_UFO_CFG_2B **DISP_UFO_CFG_2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	disp_ufo_cfg_2b															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	disp_ufo_cfg_2b															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	disp_ufo_cfg_2b	UFO configuration 2

1401910C DISP_UFO_CFG_3B **DISP_UFO_CFG_3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	disp_ufo_cfg_3b															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	disp_ufo_cfg_3b															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	disp_ufo_cfg_3b	UFO configuratino 3

14019110 DISP_UFO_CFG_4B **DISP_UFO_CFG_4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	disp_ufo_cfg_4b															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	disp_ufo_cfg_4b															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	disp_ufo_cfg_4b	UFO configuration 4

14019120 DISP_UFO_RO_0B DISP_UFO_RO_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	disp_ufo_ro_0b															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	disp_ufo_ro_0b															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	disp_ufo_ro_0b	UFO status 0

14019124 DISP_UFO_RO_1B DISP_UFO_RO_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	disp_ufo_ro_1b															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	disp_ufo_ro_1b															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	disp_ufo_ro_1b	UFO status 1

14019128 DISP_UFO_RO_2B DISP_UFO_RO_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	disp_ufo_ro_2b															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	disp_ufo_ro_2b															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	disp_ufo_ro_2b	UFO status 2

1401912C DISP_UFO_RO_3B DISP_UFO_RO_3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	disp_ufo_ro_3b															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	disp_ufo_ro_3b															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	disp_ufo_ro_3b	UFO status 3

14019130 DISP_UFO_RO_4B DISP_UFO_RO_4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	disp_ufo_ro_4b															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	disp_ufo_ro_4b															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	disp_ufo_ro_4b	UFO status 4

14019140 DISP_UFO_DBG0 DISP_UFO_DBG0 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				vcnt_in_relay												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					hcnt_in_relay											
Type					RU											
Reset					0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28:16	vcnt_in_relay	UFO debugging 0
11:0	hcnt_in_relay	UFO debugging 0

14019144 DISP_UFO_DBG1 DISP_UFO_DBG1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					fifo0_rptr											
Type					RU											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					fifo0_wptr											
Type					RU											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	fifo0_rptr	UFO debugging 1
11:0	fifo0_wptr	UFO debugging 1

14019148 DISP_UFO_DBG2 DISP_UFO_DBG2 02800280

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					fifo1_rptr											
Type					RU											
Reset					0	0	1	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					fifo1_wptr											
Type					RU											
Reset					0	0	1	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	fifo1_rptr	UFO debugging 2
11:0	fifo1_wptr	UFO debugging 2

1401914C DISP_UFO_DBG3 DISP_UFO_DBG3 05000500

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					fifo2_rptr											
Type					RU											
Reset					0	1	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					fifo2_wptr											
Type					RU											
Reset					0	1	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	fifo2_rptr	UFO debugging 3
11:0	fifo2_wptr	UFO debugging 3

14019150 DISP_UFO_DBG4 DISP_UFO_DBG4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					rec_fifo_rptr											
Type					RU											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					rec_fifo_wptr											
Type					RU											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	rec_fifo_rptr	UFO debugging 4
11:0	rec_fifo_wptr	UFO debugging 4

14019154 DISP_UFO_DBG5 DISP_UFO_DBG5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															obuf_acc	
Type															RU	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	obuf_acc															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:0	obuf_acc	UFO debugging 5

14019158 DISP_UFO_DBG6 DISP_UFO_DBG6 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				vcnt_octl												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	1	0

Bit(s)	Name	Description
12:0	vcnt_octl	UFO debugging 6

1401915C DISP_UFO_DBG7 DISP_UFO_DBG7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								fifob_cnt								
Type								RU								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	fifob_cnt	UFO debugging 7

Module name: MDP_RDMA0 Base address: (+14001000h)

Address	Name	Width	Register Function
14001000	EN	32	Enable Register
14001008	RESET	32	Reset Register
14001010	INTERRUPT_ENABLE	32	Interrupt Enable Register
14001018	INTERRUPT_STATUS	32	Interrupt Status Register
14001020	CON	32	Control Register
14001028	GMCIF_CON	32	GMC Interface Control Register
14001030	SRC_CON	32	Source Control Register
14001060	MF_BKGD_SIZE_IN_BYTE	32	Main Frame Background Size In Byte Register
14001068	MF_BKGD_SIZE_IN_PXL	32	Main Frame Background Size In Pixel Register
14001070	MF_SRC_SIZE	32	Main Frame Source Size Register
14001078	MF_CLIP_SIZE	32	Main Frame Clip Size Register
14001080	MF_OFFSET_1	32	Main Frame Offset 1 Register
14001088	MF_PAR	32	Main Frame Parameter Register
14001090	SF_BKGD_SIZE_IN_BYTE	32	Sub Frame Background Size In Byte Register
140010B8	SF_PAR	32	Sub Frame Parameter Register
140010C0	MB_DEPTH	32	Main Line Buffer Depth Control Register
140010C8	MB_BASE	32	Main Buffer Base Address Register
140010D0	MB_CON	32	Main Line Buffer Control Register
140010D8	SB_DEPTH	32	Sub Line Buffer Depth Control Register
140010E0	SB_BASE	32	Sub Buffer Base Address Register
140010E8	SB_CON	32	Sub Line Buffer Control Register
140010F0	VC1_RANGE	32	VC1 Range Control Register
14001100	SRC_END_0	32	Source End Address 0 Register
14001108	SRC_END_1	32	Source End Address 1 Register
14001110	SRC_END_2	32	Source End Address 2 Register
14001118	SRC_OFFSET_0	32	Source Address Offset 0 Register
14001120	SRC_OFFSET_1	32	Source Address Offset 1 Register
14001128	SRC_OFFSET_2	32	Source Address Offset 2 Register
14001130	SRC_OFFSET_W_0	32	Source Address Ring Buffer Start Offset 0 Register

Address	Name	Width	Register Function
14001138	SRC_OFFSET_W_1	32	Source Address Ring Buffer Start Offset 1 Register
14001140	SRC_OFFSET_W_2	32	Source Address Ring Buffer Start Offset 2 Register
14001148	SRC_OFFSET_0_P	32	Source Address Offset 0 in Pixel Register
14001200	TRANSFORM_0	32	Color Transform Control 0
14001208	TRANSFORM_1	32	Color Transform Control 1
14001210	TRANSFORM_2	32	Color Transform Control 2
14001218	TRANSFORM_3	32	Color Transform Control 3
14001220	TRANSFORM_4	32	Color Transform Control 4
14001228	TRANSFORM_5	32	Color Transform Control 5
14001230	TRANSFORM_6	32	Color Transform Control 6
14001238	TRANSFORM_7	32	Color Transform Control 7
14001240	DMABUF_CON_0	32	DMA Buffer 0 Control Register
14001248	DMAULTRA_CON_0	32	DMA Buffer 0 Ultra Control Register
14001250	DMABUF_CON_1	32	DMA Buffer 1 Control Register
14001258	DMAULTRA_CON_1	32	DMA Buffer 1 Ultra Control Register
14001260	DMABUF_CON_2	32	DMA Buffer 2 Control Register
14001268	DMAULTRA_CON_2	32	DMA Buffer 2 Ultra Control Register
14001270	PROC_TRACK_CON_0	32	DMA Processing tracking control 0
14001278	PROC_TRACK_CON_1	32	DMA Processing tracking control 1
14001280	PROC_TRACK_CON_2	32	DMA Processing tracking control 2
14001288	RESV_DUMMY_0	32	Reserved Dummy Register
14001300	CHKS_EXTR	32	Checksum For EXT Read
14001308	CHKS_INTW	32	Checksum For INT Writer
14001310	CHKS_INTR	32	Checksum For INT Read
14001318	CHKS_ROTO	32	Checksum For Rotator Output
14001320	CHKS_SRIY	32	Checksum For SRAM Input Y
14001328	CHKS_SRIU	32	Checksum For SRAM Input U
14001330	CHKS_SRIV	32	Checksum For SRAM Input V
14001338	CHKS_SROY	32	Checksum For SRAM Output Y
14001340	CHKS_SROU	32	Checksum For SRAM Output U
14001348	CHKS_SROV	32	Checksum For SRAM Output V
14001350	CHKS_VUPI	32	Checksum For Vertical Upsample Input
14001358	CHKS_VUPO	32	Checksum For Vertical Upsample Output
14001380	DEBUG_CON	32	Debug Control
14001400	MON_STA_0	32	Monitor For Status 0
14001408	MON_STA_1	32	Monitor For Status 1
14001410	MON_STA_2	32	Monitor For Status 2
14001418	MON_STA_3	32	Monitor For Status 3
14001420	MON_STA_4	32	Monitor For Status 4
14001428	MON_STA_5	32	Monitor For Status 5
14001430	MON_STA_6	32	Monitor For Status 6
14001438	MON_STA_7	32	Monitor For Status 7
14001440	MON_STA_8	32	Monitor For Status 8
14001448	MON_STA_9	32	Monitor For Status 9

Address	Name	Width	Register Function
14001450	MON_STA_10	32	Monitor For Status 10
14001458	MON_STA_11	32	Monitor For Status 11
14001460	MON_STA_12	32	Monitor For Status 12
14001468	MON_STA_13	32	Monitor For Status 13
14001470	MON_STA_14	32	Monitor For Status 14
14001478	MON_STA_15	32	Monitor For Status 15
14001480	MON_STA_16	32	Monitor For Status 16
14001488	MON_STA_17	32	Monitor For Status 17
14001490	MON_STA_18	32	Monitor For Status 18
14001498	MON_STA_19	32	Monitor For Status 19
140014A0	MON_STA_20	32	Monitor For Status 20
140014A8	MON_STA_21	32	Monitor For Status 21
140014B0	MON_STA_22	32	Monitor For Status 22
140014B8	MON_STA_23	32	Monitor For Status 23
140014C0	MON_STA_24	32	Monitor For Status 24
140014C8	MON_STA_25	32	Monitor For Status 25
140014D0	MON_STA_26	32	Monitor For Status 26
14001F00	SRC_BASE_0	32	Source Base Address 0 Register
14001F08	SRC_BASE_1	32	Source Base Address 1 Register
14001F10	SRC_BASE_2	32	Source Base Address 2 Register
14001F20	UFO_DEC_LENGTH_BASE_Y	32	UFO DECODER Y LENGTH TABLE BASE ADDRESS
14001F28	UFO_DEC_LENGTH_BASE_C	32	UFO DECODER C LENGTH TABLE BASE ADDRESS

14001000 EN **Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ROT_ENABLE
Type																RW
Reset																0

Bit(s)	Name	Description
0	ROT_ENABLE	**Rotator enabling signal** Only 1 can be written. 0: No rotator operation 1: Rotator is enabled to rotate a frame.

14001008 RESET **Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WARM_RESET
Type																A0
Reset																0

Bit(s)	Name	Description
0	WARM_RESET	**Resets rotator inner states after no pending bus transactions are left** Hardware will de-assert this signal after reset is done. 0: De-assert reset 1: Assert reset

14001010 INTERRUPT_ENABLE **Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														UNDERRUN_INT_EN	REG_UPDATE_INT_EN	FRAME_COMPLETE_INT_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	UNDERRUN_INT_EN	**Enables rotator under-run interrupt** 0: Disable 1: Enable
1	REG_UPDATE_INT_EN	**Enables rotator register updated interrupt** 0: Disable 1: Enable
0	FRAME_COMPLETE_INT_EN	**Enables rotator frame completed interrupt** 0: Disable 1: Enable

14001018 INTERRUPT_STATUS **Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														UNDERRUN	REG_UPDA	FRAME_CO

														_INT	TE_INT	MPLETE_INT
Type														RU	RU	RU
Reset														0	0	0

Bit(s)	Name	Description
2	UNDERRUN_INT	**Rotator under-run interrupt** SW can only write 0 to clear the interrupt. Writing 1 is ineffective.
1	REG_UPDATE_INT	**Rotator register updated interrupt** SW can only write 0 to clear the interrupt. Writing 1 is ineffective.
0	FRAME_COMPLETE_INT	**Rotator frame completed interrupt** SW can only write 0 to clear the interrupt. Writing 1 is ineffective.

14001020 CON **Control Register** **00000010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				LB_2B_MODE				BUFFER_MODE				SIMPLE_MODE				
Type				RW				RW				RW				
Reset				0				0				1				

Bit(s)	Name	Description
12	LB_2B_MODE	**Enables line-buffer (2) byte write merge mode to improve performance and reduce BW waste** Only works for scan-line source since they are the worst case compared to block source. 0: Disable 1: Enable
8	BUFFER_MODE	**Enables buffer mode** When buffer mode is 1, rotator will use a little more buffer to enhance performance. 0: Disable 1: Enable
4	SIMPLE_MODE	**MDP_RDMA simple configuration mode** 0: Turn off simple mode 1: Turn on simple mode

14001028 GMCIF_CON **GMC Interface Control Register** **00000330**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	THROTTLE_PERIOD												THROTTLE_EN		PRE_ULTRA_EN	
Type	RW												RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name			ULTRA_EN			WRITE_REQUEST_TYPE				READ_REQUEST_TYPE						COMMAND_DIV
Type			RW			RW				RW						RW
Reset			0	0		0	1	1		0	1	1				0

Bit(s)	Name	Description
31:20	THROTTLE_PERIOD	**Period of throttle control** Delayed cycles between two requests is 4*THROTTLE_PERIOD.
19	THROTTLE_EN	**Controls throttle of rotator** When it is enabled, cycles between two requests will be throttled by the value of THROTTLE_PERIOD. 0: Disable 1: Enable
17:16	PRE_ULTRA_EN	**Enables pre_ultra high request for read port** 0: Disable 1: Enable according to ultra_th_low/ultra_th_high 2: Always enable 3: Reserved
13:12	ULTRA_EN	**Enables ultra high request for read port** 0: Disable 1: Enable according to ultra_th_low/ultra_th_high 2: Always enable 3: Reserved
10:8	WRITE_REQUEST_TYPE	**Controls maximum request burst length** 0: Single access 1: Burst 2 access 2: Burst 3 access 3: Burst 4 access 4: Burst 5 access 5: Burst 6 access 6: Burst 7 access 7: Burst 8 access
6:4	READ_REQUEST_TYPE	**Controls maximum request burst length** The real burst length is according to the rotation. 0: Single access 1: Burst 2 access 2: Burst 3 access 3: Burst 4 access 4: Burst 5 access 5: Burst 6 access 6: Burst 7 access 7: Burst 8 access
0	COMMAND_DIV	**Controls if command across 256-byte boundary needs to be divided to 2 separate commands** 0: No division 1: Division is necessary.

14001030 SRC_CON Source Control Register 000A0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TOP_BOUNDARY	BOT_BOUNDARY	LEFT_BOUNDARY	RIGHT_BOUNDARY				RING_BUF_READ	BLOCK_10BIT_TILE_MODE	BLOCK_10BIT	LENGTH_TABLE_NOT_REV	BYTE_SWAP	UFO_DATA_IN_NOT_REV	UFO_DATA_OUT_NOT_REV	UNIFORM_CONFIG	IS_Y_LSB

Type	RW	RW	RW	RW				RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0				0	0	0	0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLOCK	SWAP	VDO_FIELD	VDO_MODE	UFO_DEC_EN	CUS_REP		COSITE	RGB_PAD	SRC_SWAP			SRC_FORMAT			
Type	RW	RW	RW	RW	RW	RW		RW	RW	RW			RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TOP_BOUNDARY	**If the boundary is the entire frame boundary, upsample filter of bundary-pixels will be processed with boundary repeated.** If the boundary is simply tile boundary, upsample filter of the boundary-pixels will be processed with the adjacent line or pixel. 0: The top boundary of the current tile is the tile boundary. 1: The top boundary of the current tile is the frame boundary.
30	BOT_BOUNDARY	**If the boundary is the entire frame boundary, upsample filter of bundary-pixels will be processed with boundary repeated.** If the boundary is simply tile boundary, upsample filter of the boundary-pixels will be processed with the adjacent line or pixel. 0: The bottom boundary of the current tile is the tile boundary. 1: The bottom boundary of the current tile is the frame boundary.
29	LEFT_BOUNDARY	**If the boundary is the whole frame boundary, upsample filter of the bundary-pixels will be processed with boundary repeated.** If the boundary is just a tile boundary, upsample filter of the boundary-pixels will be processed with the adjacent line or pixel. 0: The left boundary of the current tile is the tile boundary. 1: The left boundary of the current tile is the frame boundary.
28	RIGHT_BOUNDARY	**If the boundary is the entire frame boundary, upsample filter of bundary-pixels will be processed with boundary repeated.** If the boundary is simply tile boundary, upsample filter of the boundary-pixels will be processed with the adjacent line or pixel. 0: The right boundary of the current tile is the tile boundary. 1: The right boundary of the current tile is the frame boundary.
24	RING_BUF_READ	**Enables ring buffer read scheme** 0: Off. Normal read 1: Ring buffer read on. Address will be turned around between SRC_BASE + SRC_OFFSET and SRC_END.
23	BLOCK_10BIT_TILE_MODE	**Enables the HVEC tile mode memory foot print** Only takes effect when BLOCK_10BIT=1. Be ware that this tile mode is not the tile processing of MDP. 0: Read HVEC 10-bit non-tile mode 1: Read HVEC 10-bit tile mode
22	BLOCK_10BIT	**Enables 10-bit block mode. Only takes effect when SRC_FMT=NV12 & BLOCK=1** 0: Read 8-bit block format 1: Read 10-bit block format
21	LENGTH_TABLE_NOT_REV	**Only works in UFO mode.** Do not modify this bit. 0: Reverse the byte order of the UFO length table

Bit(s)	Name	Description
		1: Does not reverse the byte order of the UFO length table
20	BYTE_SWAP	**Only when legacy mode and src_format = RGB565 will this bit take effect.** 0: Little endian input 1: Big endian input; do byte swap for input
19	UFO_DATA_IN_NOT_REV	**Only works in UFO mode.** Do not modify this bit. 0: Reverse the byte order of the UFO core input data 1: Does not reverse the byte order of the UFO core input data
18	UFO_DATA_OUT_NOT_REV	**Only works in UFO mode.** Do not modify this bit. 0: Reverse the byte order of the UFO core output data 1: Does not reverse the byte order of the UFO core output data
17	UNIFORM_CONFIG	**Swaps between uniform config mode or legacy mode** Do not modify this bit. 0: Legacy mode 1: Uniform config
16	IS_Y_LSB	**Only when legacy mode and src_format = 422_I_SW, will this bit take effect.** 0: Y is packed in MSB byte 1: Y is packed in LSB byte
15	BLOCK	**Only works in uniform config mode.** 0: Raster scan mode 1: Block mode
14	SWAP	**Only works in uniform config mode.** 0: No swap 1: Swap
13	VDO_FIELD	**Only VDO_MODE =1 will this bit take effect.** 0: Top field 1: Bottom field
12	VDO_MODE	**Only when source format is HW video block YCbCr_420_SP will this bit take effect.** 0: Frame mode 1: Field mode
11	UFO_DEC_EN	**Turns on UFO_DEC to decode UFO stream from video decoder** 0: Turn off 1: Turn on
10:9	CUS_REP	**UV horizontal sampling method** 0: Filter 1: V repeat, H filter 2: H repeat, V filter 3: No V/H filter, will repeat the data
8	COSITE	**UV horizontal sample position for YUV420** 0: Non-cosited 1: Cosited
7	RGB_PAD	**Rotator RGB565 padding option** 0: Padding MSB 1: Padding 0
6:4	SRC_SWAP	**Only works in legacy mode.** Rotator YUV/RGB source swap. If the source is YUV/RGB order, output can be re-ordered as: 0: YUV/RGB 1: VUY/BGR, R/B swap 2: YVU/RBG, U/V swap 3: UVY/GBR 4: UYV/GRB 5: VYU/BRG

Bit(s)	Name	Description
3:0	SRC_FORMAT	**Rotator source frame format** 0: RGB565 1: RGB888 2: BGRA8888 3: ARGB8888 4: UYVY 5: YUY2 7: Y8 8: I420 (YV12) 9: I422 (YV16) 10: YV24 12: NV12 13: NV16 14: NV24

14001060 MF_BKGD_SIZE_IN_BYTE **Main Frame Background Size In Byte Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												MF_BKGD_WB				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MF_BKGD_WB															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	MF_BKGD_WB	**Rotator main frame background width in byte** Refer to the formula table.

14001068 MF_BKGD_SIZE_IN_PXL **Main Frame Background Size In Pixel Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												MF_BKGD_WP				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MF_BKGD_WP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	MF_BKGD_WP	**Rotator main frame background width in pixel** Refer to the formula table. Only used in 10-bit mode.

14001070 MF_SRC_SIZE **Main Frame Source Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MF_SRC_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MF_SRC_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	MF_SRC_H	**Rotator main frame source height** If its value is H, there will be H lines in a frame.
12:0	MF_SRC_W	**Rotator main frame source width** If its value is W, there will be W pixels in a line.

14001078 MF_CLIP_SIZE — Main Frame Clip Size Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MF_CLIP_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MF_CLIP_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	MF_CLIP_H	**Rotator main frame clip height** If its value is H, there will be H lines in a frame.
12:0	MF_CLIP_W	**Rotator main frame clip width** If its value is W, then there are W pixels in a line.

14001080 MF_OFFSET_1 — Main Frame Offset 1 Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											MF_OFFSET_H_1					
Type											RW					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												MF_OFFSET_W_1				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
21:16	MF_OFFSET_H_1	Rotator main frame height offset
4:0	MF_OFFSET_W_1	Rotator main frame width offset

14001088 MF_PAR **Main Frame Parameter Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MF_SB												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MF_SB						MF_JUMP									
Type	RW						RW									
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:12	MF_SB	**Rotator main frame seg size in byte** Refer to the formula table.
9:0	MF_JUMP	**Rotator main frame jump in byte** Refer to the formula table.

14001090 SF_BKGD_SIZE_IN_BYTE **Sub Frame Background Size In Byte Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												SF_BKGD_WB				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SF_BKGD_WB															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	SF_BKGD_WB	**Rotator sub frame background width in byte** Refer to the formula table.

140010B8 SF_PAR **Sub Frame Parameter Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				SF_SB												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SF_SB						SF_JUMP									
Type	RW						RW									
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:12	SF_SB	**Rotator sub frame seg size in byte** Refer to the formula table.
9:0	SF_JUMP	**Rotator sub frame jump in byte** Refer to the formula table.

140010C0 MB_DEPTH — Main Line Buffer Depth Control Register — 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										MB_DEPTH						
Type										RW						
Reset										0	0	1	0	0	0	0

Bit(s)	Name	Description
6:0	MB_DEPTH	**Rotator main buffer depth** The min. value is 2; max. value is 64. In SW scan line mode, its value can be arbitrary; else, the value must be set according to the formula table.

140010C8 MB_BASE — Main Buffer Base Address Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MB_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	MB_BASE	**Rotator main buffer base address** The buffer size should be RGB565: MB_LP*(SB_DEPTH + BUFFER_MODE)*2 Others: MB_LP*(SB_DEPTH + BUFFER_MODE) For MT6583/6517, set it to 0.

140010D0 MB_CON — Main Line Buffer Control Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			MB_LP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MB_PPS												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	MB_LP	**Rotator main buffer line pixel** Refer to the formula table.

Bit(s)	Name	Description
12:0	MB_PPS	**Rotator main buffer pixel number per segment** It is equal to MB_LP/(MB_DEPTH + BUFFER_MODE).

140010D8 SB_DEPTH — Sub Line Buffer Depth Control Register — 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SB_DEPTH						
Type										RW						
Reset										0	0	1	0	0	0	0

Bit(s)	Name	Description
6:0	SB_DEPTH	**Rotator sub buffer depth** The min. value is 2; max. value is 64. In SW scan line mode, its value can be arbitrary; else, the value must be set according to the formula table.

140010E0 SB_BASE — Sub Buffer Base Address Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SB_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SB_BASE	**Rotator sub buffer base address** Valid for all modes except for RGB565. The buffer size should be SB_LP*(SB_DEPTH + BUFFER_MODE)*2. For MT6583/MT6517, RGB565: 0x0 VDO 420 && vertical rotate: 0x5600 Others: 0x4400

140010E8 SB_CON — Sub Line Buffer Control Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SB_LP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name				SB_PPS													
Type				RW													
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	SB_LP	**Rotator sub buffer line pixel** Refer to the formula table.
12:0	SB_PPS	**Rotator sub buffer pixel number per segment** It is equal to SB_LP/(SB_DEPTH + BUFFER_MODE).

140010F0 VC1_RANGE **VC1 Range Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												VC1_ MAP_ PARA _C				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VC1_MAP_PARA_Y								VC1_ MAP_ EN				VC1_ RED_ EN
Type				RW								RW				RW
Reset				0	0	0	0	0				0				0

Bit(s)	Name	Description
20:16	VC1_MAP_PARA_C	**VC1 range mapping parameter for C** Range: N+9, N=0~7 0: Disable 1: Enable
12:8	VC1_MAP_PARA_Y	**VC1 range mapping parameter for Y** Range: N+9, N=0~7
4	VC1_MAP_EN	**Enables VC1 range mapping** 0: Disable 1: Enable
0	VC1_RED_EN	**Enables VC1 range reduction** 0: Disable 1: Enable

14001100 SRC_END_0 **Source End Address 0 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_END_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_END_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_END_0	**Ring buffer read scheme bottom address 0** SRC_BASE_0 <= read ptr < SRC_END_0

14001108 SRC_END_1 Source End Address 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_END_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_END_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_END_1	**Ring buffer read scheme bottom address 1** SRC_BASE_1 <= read ptr < SRC_END_1

14001110 SRC_END_2 Source End Address 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_END_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_END_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_END_2	**Ring buffer read scheme bottom address 2** SRC_BASE_2 <= read ptr < SRC_END_2

14001118 SRC_OFFSET_0 Source Address Offset 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_OFFSET_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_OFFSET_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_OFFSET_0	Source starting address = SRC_BASE_0 + SRC_OFFSET_0

14001120 SRC_OFFSET_1 Source Address Offset 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_OFFSET_1															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_OFFSET_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_OFFSET_1	Source starting address = SRC_BASE_1 + SRC_OFFSET_1

14001128 SRC_OFFSET_2 Source Address Offset 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_OFFSET_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_OFFSET_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_OFFSET_2	Source starting address = SRC_BASE_2 + SRC_OFFSET_2

14001130 SRC_OFFSET_W_0 Source Address Ring Buffer Start Offset 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_OFFSET_W_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SRC_OFFSET_W_0	**In ring buffer mode, address will roll back to** SRC_BASE0 + SRC_OFFSET_W_0 when crossing SRC_END0.

14001138 SRC_OFFSET_W_1 Source Address Ring Buffer Start Offset 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_OFFSET_W_1															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SRC_OFFSET_W_1	**In ring buffer mode, address will roll back to** SRC_BASE1 + SRC_OFFSET_W_1 when crossing SRC_END1.

14001140 SRC_OFFSET_W_2 **Source Address Ring Buffer Start Offset 2 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SRC_OFFSET_W_2**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SRC_OFFSET_W_2	**In ring buffer mode, address will roll back to** SRC_BASE2 + SRC_OFFSET_W_2 when crossing SRC_END2.

14001148 SRC_OFFSET_0_P **Source Address Offset 0 in Pixel Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SRC_OFFSET_0_P**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SRC_OFFSET_0_P**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_OFFSET_0_P	Source starting address offset in unit of pixel

14001200 TRANSFORM_ **Color Transform Control 0** **20010660**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CSC_ENABLE**	**CSC_ FORM AT**			**int_ matr ix_s el**							**ext_ matr ix_e n**				**TRANS_EN**
Type	RW	RW			RW							RW				RW
Reset	0	0	1	0	0	0	0	0				0				1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**OUT_S_2**	**OUT_S_1**	**OUT_S_0**		**CLAMP_S_2**	**CLAMP_S_1**	**CLAMP_S_0**		**IN_S_2**	**IN_S_1**	**IN_S_0**
Type						RW	RW	RW		RW	RW	RW		RW	RW	RW

Reset						1	1	0		1	1	0		0	0	0

Bit(s)	Name	Description
31	CSC_ENABLE	**Enables CSC**
30:28	CSC_FORMAT	**CSC format** 3'b010: Non-constant Luminance mode 3'b011: Constant Luminance mode Others: Reserved
27:24	int_matrix_sel	**If ext_matrix_en = 0, selects build-in matrix table** 4'b0000: RGB to JPEG 4'b0010: RGB to BT601 4'b0011: RGB to BT709 4'b0100: JPEG to RGB 4'b0110: BT601 to RGB 4'b0111: BT709 to RGB 4'b1000: JPEG to BT601 4'b1001: JPEG to BT709 4'b1010: BT601 to JPEG 4'b1011: BT709 to JPEG 4'b1100: BT709 to BT601 4'b1101: BT601 to BT709 Others: Reserved
20	ext_matrix_en	**Selects external matrix with programmable coefficient** 0: Use internal build-in matrix table 1: Use programmable coefficients
16	TRANS_EN	**Transform function enabling control** 0: Disable 1: Enable
10	OUT_S_2	**Output sign 2**
9	OUT_S_1	**Output sign 1**
8	OUT_S_0	**Output sign 0**
6	CLAMP_S_2	**Clamping sign 2**
5	CLAMP_S_1	**Clamping sign 1**
4	CLAMP_S_0	**Clamping sign 0**
2	IN_S_2	**Input sign 2**
1	IN_S_1	**Input sign 1**
0	IN_S_0	**Input sign 0**

14001208 TRANSFORM_1 Color Transform Control 1 18060000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				IN_OFFSET_2										IN_OFFSET_1		
Type				RW										RW		
Reset				1	1	0	0	0	0	0	0	0		1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IN_OFFSET_1							IN_OFFSET_0								
Type	RW							RW								
Reset	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:20	IN_OFFSET_2	Input offset 2
18:10	IN_OFFSET_1	Input offset 1
8:0	IN_OFFSET_0	Input offset 0

Bit(s)	Name	Description

14001210 TRANSFORM_2 **Color Transform Control 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				OUT_OFFSET_2										OUT_OFFSET_1		
Type				RW										RW		
Reset				0	0	0	0	0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OUT_OFFSET_1							OUT_OFFSET_0								
Type	RW							RW								
Reset	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:20	OUT_OFFSET_2	Output offset 2
18:10	OUT_OFFSET_1	Output offset 1
8:0	OUT_OFFSET_0	Output offset 0

14001218 TRANSFORM_3 **Color Transform Control 3** **00000400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_01												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_00												
Type				RW												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	C_01	**Transform coefficient 01, s2.10** Value range: -4 ~ 3.99
12:0	C_00	**Transform coefficient 00, s2.10** Value range: -4 ~ 3.99

14001220 TRANSFORM_4 **Color Transform Control 4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_10												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_02												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	C_10	**Transform coefficient 10, s2.10** Value range: -4 ~ 3.99
12:0	C_02	**Transform coefficient 02, s2.10** Value range: -4 ~ 3.99

14001228 TRANSFORM_5 Color Transform Control 5 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_12												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_11												
Type				RW												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	C_12	**Transform coefficient 12, s2.10** Value range: -4 ~ 3.99
12:0	C_11	**Transform coefficient 11, s2.10** Value range: -4 ~ 3.99

14001230 TRANSFORM_6 Color Transform Control 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_21												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_20												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	C_21	**Transform coefficient 21, s2.10** Value range: -4 ~ 3.99
12:0	C_20	**Transform coefficient 20, s2.10** Value range: -4 ~ 3.99

14001238 TRANSFORM_7 Color Transform Control 7 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name				C_22												
Type				RW												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	C_22	**Transform coefficient 22, s2.10** Value range: -4 ~ 3.99

14001240 DMABUF_CON_0 DMA Buffer 0 Control Register 03000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						EXTRD_ARB_MAX_0				BUF_RESV_SIZE_0						
Type						RW				RW						
Reset						0	1	1		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										ISSUE_REQ_TH_0						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	EXTRD_ARB_MAX_0	**Maximum outstanding ability for DMA buffer 0** 0-7 denotes outstanding number 1-8.
22:16	BUF_RESV_SIZE_0	**Buffer size reserved for overflow prevention and FIFO size test** fifo_pseudo_size = (fifo_real_size-buf_resv_size)
6:0	ISSUE_REQ_TH_0	**Issues normal requests when FIFO valid data <= fifo_pseudo_size - issue_req_th and keeps issuing requests until valid data in command phase = fifo_pseudo_size**

14001248 DMAULTRA_CON_0 DMA Buffer 0 Ultra Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PRE_ULTRA_TH_HIGH_OFS_0								ULTRA_TH_HIGH_OFS_0						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PRE_ULTRA_TH_LOW_OFS_0								ULTRA_TH_LOW_0						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	PRE_ULTRA_TH_HIGH_OFS_0	**pre_ultra_th_high = ultra_th_high + pre_ultra_th_high_ofs**
22:16	ULTRA_TH_HIGH_OFS_0	**ultra_th_high = pre_ultra_th_low + ultra_th_high_ofs**
14:8	PRE_ULTRA_TH_LOW_OFS_0	**pre_ultra_th_low = ultra_th_low + pre_ultra_th_low_ofs** Issues pre-ultra high requests when FIFO valid data <=

Bit(s)	Name	Description
6:0	ULTRA_TH_LOW_0	pre_ultra_th_low and keeps it asserted until FIFO valid data >= pre_ultra_th_high **Issues ultra high requests when FIFO valid data <= ultra_th_low** and keeps it asserted until FIFO valid data >= ultra_th_high

14001250 DMABUF_CON_1 **DMA Buffer 1 Control Register** **03000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						EXTRD_ARB_MAX_1					BUF_RESV_SIZE_1					
Type						RW					RW					
Reset						0	1	1			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ISSUE_REQ_TH_1					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
26:24	EXTRD_ARB_MAX_1	**Maximum outstanding ability for DMA buffer 1** 0-7 denotes outstanding number 1-8.
21:16	BUF_RESV_SIZE_1	**Buffer size reserved for overflow prevention and FIFO size test** fifo_pseudo_size = (fifo_real_size-buf_resv_size)
5:0	ISSUE_REQ_TH_1	**Issues normal requests when FIFO valid data <= fifo_pseudo_size - issue_req_th and keeps issuing requests until valid data in command phase = fifo_pseudo_size**

14001258 DMAULTRA_CON_1 **DMA Buffer 1 Ultra Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			PRE_ULTRA_TH_HIGH_OFS_1								ULTRA_TH_HIGH_OFS_1					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			PRE_ULTRA_TH_LOW_OFS_1								ULTRA_TH_LOW_1					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
29:24	PRE_ULTRA_TH_HIGH_OFS_1	**pre_ultra_th_high = ultra_th_high + pre_ultra_th_high_ofs**
21:16	ULTRA_TH_HIGH_OFS_1	**ultra_th_high = pre_ultra_th_low + ultra_th_high_ofs**
13:8	PRE_ULTRA_TH_LOW_OFS_1	**pre_ultra_th_low = ultra_th_low + pre_ultra_th_low_ofs** Issues pre-ultra high requests when FIFO valid data <= pre_ultra_th_low and keeps it asserted until FIFO valid data >=

Bit(s)	Name	Description
5:0	ULTRA_TH_LOW_1	pre_ultra_th_high **Issues ultra high requests when FIFO valid data <= ultra_th_low,** and keeps it asserted until FIFO valid data >= ultra_th_high

14001260 DMABUF_CON_2 DMA Buffer 2 Control Register 03000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						EXTRD_ARB_MAX_2						BUF_RESV_SIZE_2				
Type						RW						RW				
Reset						0	1	1				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												ISSUE_REQ_TH_2				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
26:24	EXTRD_ARB_MAX_2	**Maximum outstanding ability for DMA buffer 2** 0-7 denotes outstanding number 1-8.
20:16	BUF_RESV_SIZE_2	**Buffer size reserved for overflow prevention and FIFO size test** fifo_pseudo_size = (fifo_real_size-buf_resv_size)
4:0	ISSUE_REQ_TH_2	**Issues normal requests when FIFO valid data <= fifo_pseudo_size - issue_req_th and keeps issuing requests until valid data in command phase = fifo_pseudo_size**

14001268 DMAULTRA_CON_2 DMA Buffer 2 Ultra Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				PRE_ULTRA_TH_HIGH_OFS_2								ULTRA_TH_HIGH_OFS_2				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PRE_ULTRA_TH_LOW_OFS_2								ULTRA_TH_LOW_2				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
28:24	PRE_ULTRA_TH_HIGH_OFS_2	**pre_ultra_th_high = ultra_th_high + pre_ultra_th_high_ofs**
20:16	ULTRA_TH_HIGH_OFS_2	**ultra_th_high = pre_ultra_th_low + ultra_th_high_ofs**
12:8	PRE_ULTRA_TH_LOW_OFS_2	**pre_ultra_th_low = ultra_th_low + pre_ultra_th_low_ofs** Issues pre-ultra high requests when FIFO valid data <= pre_ultra_th_low and keeps it asserted until FIFO valid data >=

Bit(s)	Name	Description
4:0	ULTRA_TH_LOW_2	pre_ultra_th_high **Issues ultra high requests when FIFO valid data <= ultra_th_low** and keeps it asserted until FIFO valid data >= ultra_th_high

14001270 PROC_TRACK_CON_0 **DMA Processing tracking control 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		IGNORE_INIT_LATENCY	STOP_GREQ_EN	PROC_PRE_ULTRA_EN												
Type		RW	RW	RW												
Reset		0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TRACK_WINDOW											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	IGNORE_INIT_LATENCY	**Ignores initial latency from SOF to the first proc_one**
29	STOP_GREQ_EN	**Enables stop_greq of process tracking**
28	PROC_PRE_ULTRA_EN	**Enables pre_ultra of the process tracking** If this bit is enabled, pre_ultra will be contolled by process tracking unit.
11:0	TRACK_WINDOW	**Tracking window** Unit: bclk_ck cycle

14001278 PROC_TRACK_CON_1 **DMA Processing tracking control 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									TARGET_CNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TARGET_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	TARGET_CNT	**Target process count during TRACK_WINDOW** It is a 16.8 fix point number.

14001280 PROC_TRACK_CON_2 **DMA Processing tracking control 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									STOP_CNT							

Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STOP_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	STOP_CNT	If processing counter > STOP_CNT, stop issuing greq.

14001288 RESV_DUMMY_0 Reserved Dummy Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_DUMMY_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_DUMMY_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_DUMMY_0	**Dummy register** Reserved

14001300 CHKS_EXTR Checksum For EXT Read 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_EXTR_CRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_EXTR_CRC															CHKS_EXTR_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_EXTR_CRC	Checksum result for external (EMI) read data
0	CHKS_EXTR_CLR	Clears checksum to 0

14001308 CHKS_INTW Checksum For INT Writer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_INTW_CRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	CHKS_INTW_CRC															CHKS_INTW_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_INTW_CRC	Checksum result for internal (SYSRAM) write data
0	CHKS_INTW_CLR	Clears checksum to 0

14001310 CHKS_INTR Checksum For INT Read 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_INTR_CRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_INTR_CRC															CHKS_INTR_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_INTR_CRC	Checksum result for internal (SYSRAM) read data
0	CHKS_INTR_CLR	Clears checksum to 0

14001318 CHKS_ROTO Checksum For Rotator Output 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_ROTO_CRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_ROTO_CRC															CHKS_ROTO_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_ROTO_CRC	Checksum result for rotator output data to SCL
0	CHKS_ROTO_CLR	Clears checksum to 0

14001320 CHKS_SRIY Checksum For SRAM Input Y 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_SRIY_CRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_SRIY_CRC															CHKS_SRIY_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_SRIY_CRC	Checksum result for EMI data buffer SRAM input Y
0	CHKS_SRIY_CLR	Clears checksum to 0

14001328 CHKS_SRIU Checksum For SRAM Input U 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_SRIU_CRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_SRIU_CRC															CHKS_SRIU_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_SRIU_CRC	Checksum result for EMI data buffer SRAM input U
0	CHKS_SRIU_CLR	Clears checksum to 0

14001330 CHKS_SRIV Checksum For SRAM Input V 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_SRIV_CRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_SRIV_CRC															CHKS_SRIV_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_SRIV_CRC	Checksum result for EMI data buffer SRAM input V
0	CHKS_SRIV_CLR	Clears checksum to 0

14001338 CHKS_SROY Checksum For SRAM Output Y 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_SROY_CRC															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_SROY_CRC															CHKS_SROY_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_SROY_CRC	Checksum result for EMI data buffer SRAM output Y
0	CHKS_SROY_CLR	Clears checksum to 0

14001340 CHKS_SROU Checksum For SRAM Output U 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_SROU_CRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_SROU_CRC															CHKS_SROU_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_SROU_CRC	Checksum result for EMI data buffer SRAM output U
0	CHKS_SROU_CLR	Clears checksum to 0

14001348 CHKS_SROV Checksum For SRAM Output V 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_SROV_CRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_SROV_CRC															CHKS_SROV_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_SROV_CRC	Checksum result for EMI data buffer SRAM output V
0	CHKS_SROV_CLR	Clears checksum to 0

14001350 CHKS_VUPI Checksum For Vertical Upsample Input 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	CHKS_VUPI_CRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_VUPI_CRC															CHKS_VUPI_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_VUPI_CRC	Checksum result for vertical chroma upsample line buffer (SRAM) input
0	CHKS_VUPI_CLR	Clears checksum to 0

14001358 CHKS_VUPO **Checksum For Vertical Upsample Output** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_VUPO_CRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_VUPO_CRC															CHKS_VUPO_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_VUPO_CRC	Checksum result for vertical chroma upsample line buffer (SRAM) output
0	CHKS_VUPO_CLR	Clears checksum to 0

14001380 DEBUG_CON **Debug Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				debug_out_sel								CHKS_TRB_SEL				CHKS_CRC_EN
Type				RW								RW				RW
Reset				0	0	0	0	0				0				0

Bit(s)	Name	Description
12:8	debug_out_sel	**Debugging output sel 0-22 mapped to MON_STA0-22**
4	CHKS_TRB_SEL	**Controls all checksum registers** 0: CHKS_INTW/CHKS_INTR sel transpose buffer 0

Bit(s)	Name	Description
0	CHKS_CRC_EN	1: CHKS_INTW/CHKS_INTR sel transpose buffer 1 **Controls all checksum registers** 0: Disable. Default to omit power consumption 1: Enable checksum for debugging

14001400 MON_STA_0 Monitor For Status 0 00000090

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_0	Monitor mdp_rdma status

14001408 MON_STA_1 Monitor For Status 1 00600100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_1															
Type	RU															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_1	Monitor mdp_rdma status

14001410 MON_STA_2 Monitor For Status 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_2	Monitor mdp_rdma status

14001418 MON_STA_3 Monitor For Status 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_3	Monitor mdp_rdma status

14001420 MON_STA_4 Monitor For Status 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_4															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_4															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_4	Monitor mdp_rdma status

14001428 MON_STA_5 Monitor For Status 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_5															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_5															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_5	Monitor mdp_rdma status

14001430 MON_STA_6 Monitor For Status 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_6															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_6															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_6	Monitor mdp_rdma status

14001438 MON_STA_7 Monitor For Status 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_7															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_7															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_7	Monitor mdp_rdma status

14001440 MON_STA_8 Monitor For Status 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_8															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_8															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_8	Monitor mdp_rdma status

14001448 MON_STA_9 Monitor For Status 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_9															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_9															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_9	Monitor mdp_rdma status

14001450 MON_STA_10 Monitor For Status 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_10															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_10															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_10	Monitor mdp_rdma status

14001458 MON_STA_11 Monitor For Status 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_11															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_11															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_11	Monitor mdp_rdma status

14001460 MON_STA_12 Monitor For Status 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_12															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_12															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_12	Monitor mdp_rdma status

14001468 MON_STA_13 Monitor For Status 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_13															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_13															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_13	Monitor mdp_rdma status

Bit(s)	Name	Description

14001470 MON_STA_14 Monitor For Status 14 00002000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_14															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_14															
Type	RU															
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_14	Monitor mdp_rdma status

14001478 MON_STA_15 Monitor For Status 15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_15															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_15															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_15	Monitor mdp_rdma status

14001480 MON_STA_16 Monitor For Status 16 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_16															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_16															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_16	Monitor mdp_rdma status

14001488 MON_STA_17 Monitor For Status 17 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_17															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_17															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_17	Monitor mdp_rdma status

14001490 MON_STA_18 Monitor For Status 18 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_18															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_18															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_18	Monitor mdp_rdma status

14001498 MON_STA_19 Monitor For Status 19 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_19															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_19															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_19	Monitor mdp_rdma status

140014A0 MON_STA_20 Monitor For Status 20 00002000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_20															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_20															
Type	RU															
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_20	Monitor mdp_rdma status

140014A8 MON_STA_21 Monitor For Status 21 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_21															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_21															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_21	Monitor mdp_rdma status

140014B0 MON_STA_22 Monitor For Status 22 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_22															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_22															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_22	Monitor mdp_rdma status

140014B8 MON_STA_23 Monitor For Status 23 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_23															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_23															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_23	Monitor mdp_rdma status

140014C0 MON_STA_24 Monitor For Status 24 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_24															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_24															

Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_24	Monitor mdp_rdma status

140014C8 MON_STA_25 Monitor For Status 25 00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_25															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_25															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_25	Monitor mdp_rdma status

140014D0 MON_STA_26 Monitor For Status 26 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_26															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_26															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_26	Monitor mdp_rdma status

14001F00 SRC_BASE_0 Source Base Address 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_BASE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_BASE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_BASE_0	**Rotator source starting base address 0** Base address of the first plane of source frame. In 2- or 3-plane mode, the first plane should be Y plane.

14001F08 SRC_BASE_1 Source Base Address 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_BASE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_BASE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_BASE_1	**Rotator source starting base address 1** When the source frame has 2 or 3 planes, it represents the base address of the second plane. In 2-plane mode, the second plane should be UV plane. In 3-plane mode, the second plane should be U plane.

14001F10 SRC_BASE_2 Source Base Address 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_BASE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_BASE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_BASE_2	**Rotator source starting base address 2** When the source frame has 3 planes, it represents the base address of the third plane. The existed third plane should be V plane.

14001F20 UFO_DEC_LENGTH_BASE_Y UFO DECODER Y LENGTH TABLE BASE ADDRESS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UFO_DEC_Y_LEN_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UFO_DEC_Y_LEN_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	UFO_DEC_Y_LEN_BASE	Base address of UFO decoder length table Y

14001F28 UFO_DEC_LENGTH_BASE_C — **UFO DECODER C LENGTH TABLE BASE ADDRESS** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UFO_DEC_C_LEN_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UFO_DEC_C_LEN_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	UFO_DEC_C_LEN_BASE	Base address of UFO decoder length table C

Module name: MDP_RDMA1 Base address: (+14002000h)

Address	Name	Width	Register Function
14002000	EN	32	Enable Register
14002008	RESET	32	Reset Register
14002010	INTERRUPT_ENABLE	32	Interrupt Enable Register
14002018	INTERRUPT_STATUS	32	Interrupt Status Register
14002020	CON	32	Control Register
14002028	GMCIF_CON	32	GMC Interface Control Register
14002030	SRC_CON	32	Source Control Register
14002060	MF_BKGD_SIZE_IN_BYTE	32	Main Frame Background Size In Byte Register
14002068	MF_BKGD_SIZE_IN_PXL	32	Main Frame Background Size In Pixel Register
14002070	MF_SRC_SIZE	32	Main Frame Source Size Register
14002078	MF_CLIP_SIZE	32	Main Frame Clip Size Register
14002080	MF_OFFSET_1	32	Main Frame Offset 1 Register
14002088	MF_PAR	32	Main Frame Parameter Register
14002090	SF_BKGD_SIZE_IN_BYTE	32	Sub Frame Background Size In Byte Register
140020B8	SF_PAR	32	Sub Frame Parameter Register
140020C0	MB_DEPTH	32	Main Line Buffer Depth Control Register
140020C8	MB_BASE	32	Main Buffer Base Address Register
140020D0	MB_CON	32	Main Line Buffer Control Register
140020D8	SB_DEPTH	32	Sub Line Buffer Depth Control Register
140020E0	SB_BASE	32	Sub Buffer Base Address Register
140020E8	SB_CON	32	Sub Line Buffer Control Register
140020F0	VC1_RANGE	32	VC1 Range Control Register
14002100	SRC_END_0	32	Source End Address 0 Register
14002108	SRC_END_1	32	Source End Address 1 Register
14002110	SRC_END_2	32	Source End Address 2 Register
14002118	SRC_OFFSET_0	32	Source Address Offset 0 Register

Address	Name	Width	Register Function
14002120	SRC_OFFSET_1	32	Source Address Offset 1 Register
14002128	SRC_OFFSET_2	32	Source Address Offset 2 Register
14002130	SRC_OFFSET_W_0	32	Source Address Ring Buffer Start Offset 0 Register
14002138	SRC_OFFSET_W_1	32	Source Address Ring Buffer Start Offset 1 Register
14002140	SRC_OFFSET_W_2	32	Source Address Ring Buffer Start Offset 2 Register
14002148	SRC_OFFSET_0_P	32	Source Address Offset 0 in Pixel Register
14002200	TRANSFORM_0	32	Color Transform Control 0
14002208	TRANSFORM_1	32	Color Transform Control 1
14002210	TRANSFORM_2	32	Color Transform Control 2
14002218	TRANSFORM_3	32	Color Transform Control 3
14002220	TRANSFORM_4	32	Color Transform Control 4
14002228	TRANSFORM_5	32	Color Transform Control 5
14002230	TRANSFORM_6	32	Color Transform Control 6
14002238	TRANSFORM_7	32	Color Transform Control 7
14002240	DMABUF_CON_0	32	DMA Buffer 0 Control Register
14002248	DMAULTRA_CON_0	32	DMA Buffer 0 Ultra Control Register
14002250	DMABUF_CON_1	32	DMA Buffer 1 Control Register
14002258	DMAULTRA_CON_1	32	DMA Buffer 1 Ultra Control Register
14002260	DMABUF_CON_2	32	DMA Buffer 2 Control Register
14002268	DMAULTRA_CON_2	32	DMA Buffer 2 Ultra Control Register
14002270	PROC_TRACK_CON_0	32	DMA Processing Tracking Control 0
14002278	PROC_TRACK_CON_1	32	DMA Processing Tracking Control 1
14002280	PROC_TRACK_CON_2	32	DMA Processing Tracking Control 2
14002288	RESV_DUMMY_0	32	Reserved Dummy Register
14002300	CHKS_EXTR	32	Checksum For EXT Read
14002308	CHKS_INTW	32	Checksum For INT Writer
14002310	CHKS_INTR	32	Checksum For INT Read
14002318	CHKS_ROTO	32	Checksum For Rotator Output
14002320	CHKS_SRIY	32	Checksum For SRAM Input Y
14002328	CHKS_SRIU	32	Checksum For SRAM Input U
14002330	CHKS_SRIV	32	Checksum For SRAM Input V
14002338	CHKS_SROY	32	Checksum For SRAM Output Y
14002340	CHKS_SROU	32	Checksum For SRAM Output U
14002348	CHKS_SROV	32	Checksum For SRAM Output V
14002350	CHKS_VUPI	32	Checksum For Vertical Upsample Input
14002358	CHKS_VUPO	32	Checksum For Vertical Upsample Output
14002380	DEBUG_CON	32	Debug Control
14002400	MON_STA_0	32	Monitor for Status 0
14002408	MON_STA_1	32	Monitor for Status 1
14002410	MON_STA_2	32	Monitor for Status 2
14002418	MON_STA_3	32	Monitor for Status 3
14002420	MON_STA_4	32	Monitor for Status 4
14002428	MON_STA_5	32	Monitor for Status 5
14002430	MON_STA_6	32	Monitor for Status 6

Address	Name	Width	Register Function
14002438	MON_STA_7	32	Monitor for Status 7
14002440	MON_STA_8	32	Monitor for Status 8
14002448	MON_STA_9	32	Monitor for Status 9
14002450	MON_STA_10	32	Monitor for Status 10
14002458	MON_STA_11	32	Monitor for Status 11
14002460	MON_STA_12	32	Monitor for Status 12
14002468	MON_STA_13	32	Monitor for Status 13
14002470	MON_STA_14	32	Monitor for Status 14
14002478	MON_STA_15	32	Monitor for Status 15
14002480	MON_STA_16	32	Monitor for Status 16
14002488	MON_STA_17	32	Monitor for Status 17
14002490	MON_STA_18	32	Monitor for Status 18
14002498	MON_STA_19	32	Monitor for Status 19
140024A0	MON_STA_20	32	Monitor for Status 20
140024A8	MON_STA_21	32	Monitor for Status 21
140024B0	MON_STA_22	32	Monitor for Status 22
140024B8	MON_STA_23	32	Monitor for Status 23
140024C0	MON_STA_24	32	Monitor for Status 24
140024C8	MON_STA_25	32	Monitor for Status 25
140024D0	MON_STA_26	32	Monitor for Status 26
14002F00	SRC_BASE_0	32	Source Base Address 0 Register
14002F08	SRC_BASE_1	32	Source Base Address 1 Register
14002F10	SRC_BASE_2	32	Source Base Address 2 Register
14002F20	UFO_DEC_LENGTH_BASE_Y	32	UFO Decoder Y Length Table Base Address
14002F28	UFO_DEC_LENGTH_BASE_C	32	UFO Decoder C Length Table Base Address

14002000 EN **Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ROT_ENABLE
Type																RW
Reset																0

Bit(s)	Name	Description
0	ROT_ENABLE	**Rotator enabling signal** Only 1 can be written. 0: No rotator operation 1: Rotator is enabled to rotate a frame.

14002008 RESET **Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WARM_RESET
Type																A0
Reset																0

Bit(s)	Name	Description
0	WARM_RESET	**Resets rotator inner states after no pending bus transactions are left** Hardware will de-assert this signal after reset is done. 0: De-assert reset 1: Assert reset

14002010 INTERRUPT_ENABLE **Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														UNDERRUN_INT_EN	REG_UPDATE_INT_EN	FRAME_COMPLETE_INT_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	UNDERRUN_INT_EN	**Enables rotator under-run interrupt** 0: Disable 1: Enable
1	REG_UPDATE_INT_EN	**Enables rotator register updated interrupt** 0: Disable 1: Enable
0	FRAME_COMPLETE_INT_EN	**Enables rotator frame completed interrupt** 0: Disable 1: Enable

14002018 INTERRUPT_STATUS **Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														UNDERRUN_INT	REG_UPDATE_INT	FRAME_COMPLETE_INT
Type														RU	RU	RU
Reset														0	0	0

Bit(s)	Name	Description
2	UNDERRUN_INT	**Rotator under-run interrupt** SW can only write 0 to clear the interrupt. Writing 1 is ineffective.
1	REG_UPDATE_INT	**Rotator register updated interrupt** SW can only write 0 to clear the interrupt. Writing 1 is ineffective.
0	FRAME_COMPLETE_INT	**Rotator frame completed interrupt** SW can only write 0 to clear the interrupt. Writing 1 is ineffective.

14002020 CON **Control Register** **00000010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				LB_2B_MODE				BUFFER_MODE				SIMPLE_MODE				
Type				RW				RW				RW				
Reset				0				0				1				

Bit(s)	Name	Description
12	LB_2B_MODE	**Enables line-buffer (2) byte write merge mode to improve performance and reduce BW waste** Only works for scan-line source since they are the worst case compared to block source. 0: Disable 1: Enable
8	BUFFER_MODE	**Enables buffer mode** When buffer mode is 1, rotator will use a little more buffer to enhance performance. 0: Disable 1: Enable
4	SIMPLE_MODE	**MDP_RDMA simple configuration mode** 0: Turn off simple mode 1: Turn on simple mode

14002028 GMCIF_CON **GMC Interface Control Register** **00000330**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	THROTTLE_PERIOD												THROTTLE_EN		PRE_ULTRA_EN	

Type	RW												RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ULTRA_EN			WRITE_REQUEST_TYPE				READ_REQUEST_TYPE						COMMAND_DIV
Type			RW			RW				RW						RW
Reset			0	0		0	1	1		0	1	1				0

Bit(s)	Name	Description
31:20	THROTTLE_PERIOD	**Period of throttle control** Delayed cycles between two requests is 4*THROTTLE_PERIOD.
19	THROTTLE_EN	**Controls throttle of rotator** When it is enabled, cycles between two requests will be throttled by the value of THROTTLE_PERIOD. 0: Disable 1: Enable
17:16	PRE_ULTRA_EN	**Enables pre_ultra high request for read port** 0: Disable 1: Enable according to ultra_th_low/ultra_th_high 2: Always enable 3: Reserved
13:12	ULTRA_EN	**Enables ultra high request for read port** 0: Disable 1: Enable according to ultra_th_low/ultra_th_high 2: Always enable 3: Reserved
10:8	WRITE_REQUEST_TYPE	**Controls maximum request burst length** 0: Single access 1: Burst 2 access 2: Burst 3 access 3: Burst 4 access 4: Burst 5 access 5: Burst 6 access 6: Burst 7 access 7: Burst 8 access
6:4	READ_REQUEST_TYPE	**Controls maximum request burst length** The real burst length is according to the rotation. 0: Single access 1: Burst 2 access 2: Burst 3 access 3: Burst 4 access 4: Burst 5 access 5: Burst 6 access 6: Burst 7 access 7: Burst 8 access
0	COMMAND_DIV	**Controls if command across 256-byte boundary needs to be divided to 2 separate commands** 0: No division 1: Division is necessary.

14002030 SRC_CON **Source Control Register** **00020000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TOP_BOUN	BOT_BOUN	LEFT_BOU	RIGHT_BO				RING_BUF	BLOCK_10	BLOCK_10	LENGTH_T	BYTE_SWA	UFO_DATA	UFO_DATA	UNIFORM_	IS_Y_LSB

	DARY	DARY	NDARY	UNDARY				_READ	BIT_TILE_MODE	BIT	ABLE_NOT_REV	P	_IN_NOT_REV	_OUT_NOT_REV	CONFIG	
Type	RW	RW	RW	RW				RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0				0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLOCK	SWAP	VDO_FIELD	VDO_MODE	UFO_DEC_EN	CUS_REP		COSITE	RGB_PAD	SRC_SWAP			SRC_FORMAT			
Type	RW	RW	RW	RW	RW	RW		RW	RW	RW			RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TOP_BOUNDARY	**If the boundary is the entire frame boundary, upsample filter of bundary-pixels will be processed with boundary repeated.** If the boundary is simply tile boundary, upsample filter of the boundary-pixels will be processed with the adjacent line or pixel. 0: The top boundary of the current tile is the tile boundary. 1: The top boundary of the current tile is the frame boundary.
30	BOT_BOUNDARY	**If the boundary is the entire frame boundary, upsample filter of bundary-pixels will be processed with boundary repeate.** If the boundary is simply tile boundary, upsample filter of the boundary-pixels will be processed with the adjacent line or pixel. 0: The bottom boundary of the current tile is the tile boundary. 1: The bottom boundary of the current tile is the frame boundary.
29	LEFT_BOUNDARY	**If the boundary is the whole frame boundary, upsample filter of the bundary-pixels will be processed with boundary repeated.** If the boundary is just a tile boundary, upsample filter of the boundary-pixels will be processed with the adjacent line or pixel. 0: The left boundary of the current tile is the tile boundary. 1: The left boundary of the current tile is the frame boundary.
28	RIGHT_BOUNDARY	**If the boundary is the entire frame boundary, upsample filter of bundary-pixels will be processed with boundary repeated.** If the boundary is simply tile boundary, upsample filter of the boundary-pixels will be processed with the adjacent line or pixel. 0: The right boundary of the current tile is the tile boundary. 1: The right boundary of the current tile is the frame boundary.
24	RING_BUF_READ	**Enables ring buffer read scheme** 0: Off. Normal read 1: Ring buffer read on. Address will be turned around between SRC_BASE + SRC_OFFSET and SRC_END.
23	BLOCK_10BIT_TILE_MODE	**Enables the HVEC tile mode memory foot print. Only takes effect when BLOCK_10BIT=1.** Be ware that this tile mode is not the tile processing of MDP. 0: Read HVEC 10-bit non-tile mode 1: Read HVEC 10-bit tile mode
22	BLOCK_10BIT	**Enables 10-bit block mode. Only takes effect when SRC_FMT=NV12 & BLOCK=1** 0: Read 8-bit block format 1: Read 10-bit block format

Bit(s)	Name	Description
21	LENGTH_TABLE_NOT_REV	**Only works in UFO mode.** Do not modify this bit. 0: Reverse the byte order of UFO length table 1: Does not reverse the byte order of UFOI length table
20	BYTE_SWAP	**Only when legacy mode and src_format = RGB565 will this bit take effect.** 0: Little endian input 1: Big endian input; do byte swap for input.
19	UFO_DATA_IN_NOT_REV	**Only works in UFO mode.** Do not modify this bit. 0: Reverse the byte order of UFO core input data 1: Does not reverse the byte order of UFO core input data
18	UFO_DATA_OUT_NOT_REV	**Only works in UFO mode.** Do not modify this bit. 0: Reverse the byte order of UFO core output data 1: Does not reverse the byte order of UFO core output data
17	UNIFORM_CONFIG	**Swaps between uniform config mode and legacy mode** Do not modify this bit. 0: Legacy mode 1: Uniform config
16	IS_Y_LSB	**Only when legacy mode and src_format = 422_I_SW will this bit take effect.** 0: Y is packed in MSB byte 1: Y is packed in LSB byte
15	BLOCK	**Only works in uniform config mode** 0: Raster scan mode 1: Block mode
14	SWAP	**Only works in uniform config mode** 0: No swap 1: Swap
13	VDO_FIELD	**When when VDO_MODE= 1 will this bit take effect.** 0: Top field 1: Bottom field
12	VDO_MODE	**Only when source format is HW video block YCbCr_420_SP will this bit takes effect.** 0: Frame mode 1: Field mode
11	UFO_DEC_EN	**Turns on UFO_DEC to decode UFO stream from video decoder** 0: Turn off 1: Turn on
10:9	CUS_REP	**UV horizontal sampling method** 0: Filter 1: V repeat, H filter 2: H repeat, V filter 3: No V/H filter, will repeat the data
8	COSITE	**UV horizontal sample position for YUV420** 0: Non-cosited 1: Cosited
7	RGB_PAD	**Rotator RGB565 padding option** 0: Padding MSB 1: Padding 0
6:4	SRC_SWAP	**Only works in legacy mode.** Rotator YUV/RGB source swap. If the source is YUV/RGB order, output can be re-ordered as: 0: YUV/RGB 1: VUY/BGR, R/B swap 2: YVU/RBG, U/V swap

Bit(s)	Name	Description
		3: UVY/GBR 4: UYV/GRB 5: VYU/BRG
3:0	SRC_FORMAT	**Rotator source frame format** 0: RGB565 1: RGB888 2: BGRA8888 3: ARGB8888 4: UYVY 5: YUY2 7: Y8 8: I420 (YV12) 9: I422 (YV16) 10: YV24 12: NV12 13: NV16 14: NV24

14002060 MF_BKGD_SIZE_IN_BYTE **Main Frame Background Size In Byte Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												MF_BKGD_WB				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MF_BKGD_WB															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	MF_BKGD_WB	**Rotator main frame background width in byte** Refer to the formula table.

14002068 MF_BKGD_SIZE_IN_PXL **Main Frame Background Size In Pixel Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												MF_BKGD_WP				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MF_BKGD_WP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	MF_BKGD_WP	**Rotator main frame background width in pixel** Refer to the formula table. Only used in 10bit mode.

14002070 MF_SRC_SIZE **Main Frame Source Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MF_SRC_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MF_SRC_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	MF_SRC_H	**Rotator main frame source height** If its value is H, there will be H lines in a frame.
12:0	MF_SRC_W	**Rotator main frame source width** If its value is W, there will be W pixels in a line.

14002078 MF_CLIP_SIZE **Main Frame Clip Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MF_CLIP_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MF_CLIP_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	MF_CLIP_H	**Rotator main frame clip height** If its value is H, there will be H lines in a frame.
12:0	MF_CLIP_W	**Rotator main frame clip width** If its value is W, then there are W pixels in a line.

14002080 MF_OFFSET_1 **Main Frame Offset 1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											MF_OFFSET_H_1					
Type											RW					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												MF_OFFSET_W_1				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
21:16	MF_OFFSET_H_1	Rotator main frame height offset
4:0	MF_OFFSET_W_1	Rotator main frame width offset

Bit(s)	Name	Description

14002088 MF_PAR **Main Frame Parameter Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MF_SB												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MF_SB						MF_JUMP									
Type	RW						RW									
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:12	MF_SB	**Rotator main frame seg size in byte** Refer to the formula table.
9:0	MF_JUMP	**Rotator main frame jump in byte** Refer to the formula table.

14002090 SF_BKGD_SIZE_IN_BYTE **Sub Frame Background Size In Byte Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												SF_BKGD_WB				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SF_BKGD_WB															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	SF_BKGD_WB	**Rotator sub frame background width in byte** Refer to the formula table.

140020B8 SF_PAR **Sub Frame Parameter Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				SF_SB												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SF_SB						SF_JUMP									
Type	RW						RW									
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:12	SF_SB	**Rotator sub frame seg size in byte** Refer to the formula table.
9:0	SF_JUMP	**Rotator sub frame jump in byte**

Bit(s)	Name	Description
		Refer to the formula table.

140020C0 MB_DEPTH — Main Line Buffer Depth Control Register — 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										MB_DEPTH						
Type										RW						
Reset										0	0	1	0	0	0	0

Bit(s)	Name	Description
6:0	MB_DEPTH	**Rotator main buffer depth** The minimum value is 2, and the maximum value is 64. In SW scan line mode, its value could be arbitrary; else, the value must be set according to the formula table.

140020C8 MB_BASE — Main Buffer Base Address Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MB_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	MB_BASE	**Rotator main buffer base address** The buffer size should be: RGB565: MB_LP*(SB_DEPTH + BUFFER_MODE)*2 Others: MB_LP*(SB_DEPTH + BUFFER_MODE) For MT6583/6517, set it to 0.

140020D0 MB_CON — Main Line Buffer Control Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			MB_LP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MB_PPS												
Type				RW												

Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	MB_LP	**Rotator main buffer line pixel** Refer to the formula table.
12:0	MB_PPS	**Rotator main buffer pixel number per segment** It is equal to MB_LP/(MB_DEPTH + BUFFER_MODE).

140020D8 SB_DEPTH — Sub Line Buffer Depth Control Register — 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SB_DEPTH						
Type										RW						
Reset										0	0	1	0	0	0	0

Bit(s)	Name	Description
6:0	SB_DEPTH	**Rotator sub buffer depth** The minimum value is 2, and the maximum value is 64. In SW scan line mode, its value could be arbitrary; else, the value must be set according to the formula table.

140020E0 SB_BASE — Sub Buffer Base Address Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SB_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SB_BASE	**Rotator sub buffer base address** Valid for all mode except RGB565. The buffer size should be SB_LP*(SB_DEPTH + BUFFER_MODE)*2. For MT6583/MT6517, RGB565: 0x0 VDO 420 && vertical rotate: 0x5600 Others: 0x4400

140020E8 SB_CON — Sub Line Buffer Control Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name			SB_LP													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SB_PPS												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	SB_LP	**Rotator sub buffer line pixel** Refer to the formula table.
12:0	SB_PPS	**Rotator sub buffer pixel number per segment** It is equal to SB_LP/(SB_DEPTH + BUFFER_MODE).

140020F0 VC1_RANGE **VC1 Range Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												VC1_ MAP_ PARA _C				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VC1_MAP_PARA_Y								VC1_ MAP_ EN				VC1_ RED_ EN
Type				RW								RW				RW
Reset				0	0	0	0	0				0				0

Bit(s)	Name	Description
20:16	VC1_MAP_PARA_C	**VC1 range mapping parameter for C** Range: N+9, N=0~7 0: Disable 1: Enable
12:8	VC1_MAP_PARA_Y	**VC1 range mapping parameter for Y** Range: N+9, N=0~7
4	VC1_MAP_EN	**Enables VC1 range mapping** 0: Disable 1: Enable
0	VC1_RED_EN	**Enables VC1 range reduction** 0: Disable 1: Enable

14002100 SRC_END_0 **Source End Address 0 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_END_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_END_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_END_0	**Ring buffer read scheme bottom address 0** SRC_BASE_0 <= read ptr < SRC_END_0

14002108 SRC_END_1 Source End Address 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_END_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_END_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_END_1	**Ring buffer read scheme bottom address 1** SRC_BASE_1 <= read ptr < SRC_END_1

14002110 SRC_END_2 Source End Address 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_END_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_END_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_END_2	**Ring buffer read scheme bottom address 2** SRC_BASE_2 <= read ptr < SRC_END_2

14002118 SRC_OFFSET_0 Source Address Offset 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_OFFSET_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_OFFSET_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_OFFSET_0	Source starting address = SRC_BASE_0 + SRC_OFFSET_0

14002120 SRC_OFFSET_1 Source Address Offset 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_OFFSET_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_OFFSET_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_OFFSET_1	Source starting address = SRC_BASE_1 + SRC_OFFSET_1

14002128 SRC_OFFSET_2 Source Address Offset 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_OFFSET_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_OFFSET_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_OFFSET_2	Source starting address = SRC_BASE_2 + SRC_OFFSET_2

14002130 SRC_OFFSET_W_0 Source Address Ring Buffer Start Offset 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_OFFSET_W_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SRC_OFFSET_W_0	**In ring buffer mode, address will roll back to** SRC_BASE0 + SRC_OFFSET_W_0 when crossing SRC_END0.

14002138 SRC_OFFSET_W_1 Source Address Ring Buffer Start Offset 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_OFFSET_W_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SRC_OFFSET_W_1	**In ring buffer mode, address will roll back to** SRC_BASE1 + SRC_OFFSET_W_1 when crossing SRC_END1.

14002140 SRC_OFFSET_W_2 **Source Address Ring Buffer Start Offset 2 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_OFFSET_W_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SRC_OFFSET_W_2	**In ring buffer mode, address will roll back to** SRC_BASE2 + SRC_OFFSET_W_2 when crossing SRC_END2.

14002148 SRC_OFFSET_0_P **Source Address Offset 0 in Pixel Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_OFFSET_0_P															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_OFFSET_0_P															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_OFFSET_0_P	Source starting address offset in unit of pixel

14002200 TRANSFORM_ **Color Transform Control 0** **20010660**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSC_ENABLE	CSC_FORMAT			int_matrix_sel							ext_matrix_en				TRANS_EN
Type	RW	RW			RW							RW				RW
Reset	0	0	1	0	0	0	0	0				0				1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name						OUT_S_2	OUT_S_1	OUT_S_0		CLAMP_S_2	CLAMP_S_1	CLAMP_S_0		IN_S_2	IN_S_1	IN_S_0
Type						RW	RW	RW		RW	RW	RW		RW	RW	RW
Reset						1	1	0		1	1	0		0	0	0

Bit(s)	Name	Description
31	CSC_ENABLE	**Enables CSC**
30:28	CSC_FORMAT	**CSC format** 3'b010: Non-constant Luminance mode 3'b011: Constant Luminance mode Others: Reserved
27:24	int_matrix_sel	**If ext_matrix_en = 0, selects build-in matrix table** 4'b0000: RGB to JPEG 4'b0010: RGB to BT601 4'b0011: RGB to BT709 4'b0100: JPEG to RGB 4'b0110: BT601 to RGB 4'b0111: BT709 to RGB 4'b1000: JPEG to BT601 4'b1001: JPEG to BT709 4'b1010: BT601 to JPEG 4'b1011: BT709 to JPEG 4'b1100: BT709 to BT601 4'b1101: BT601 to BT709 Others: Reserved
20	ext_matrix_en	**Selects external matrix with programmable coefficient** 0: Use internal build-in matrix table 1: Use programmable coefficients
16	TRANS_EN	**Transform function enabling control** 0: Disable 1: Enable
10	OUT_S_2	**Output sign 2**
9	OUT_S_1	**Output sign 1**
8	OUT_S_0	**Output sign 0**
6	CLAMP_S_2	**Clamping sign 2**
5	CLAMP_S_1	**Clamping sign 1**
4	CLAMP_S_0	**Clamping sign 0**
2	IN_S_2	**Input sign 2**
1	IN_S_1	**Input sign 1**
0	IN_S_0	**Input sign 0**

14002208 TRANSFORM_1 Color Transform Control 1 18060000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				IN_OFFSET_2										IN_OFFSET_1		
Type				RW										RW		
Reset				1	1	0	0	0	0	0	0	0		1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IN_OFFSET_1							IN_OFFSET_0								
Type	RW							RW								
Reset	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
28:20	IN_OFFSET_2	Input offset 2
18:10	IN_OFFSET_1	Input offset 1
8:0	IN_OFFSET_0	Input offset 0

14002210 TRANSFORM_2 Color Transform Control 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				OUT_OFFSET_2										OUT_OFFSET_1		
Type				RW										RW		
Reset				0	0	0	0	0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OUT_OFFSET_1							OUT_OFFSET_0								
Type	RW							RW								
Reset	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:20	OUT_OFFSET_2	Output offset 2
18:10	OUT_OFFSET_1	Output offset 1
8:0	OUT_OFFSET_0	Output offset 0

14002218 TRANSFORM_3 Color Transform Control 3 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_01												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_00												
Type				RW												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	C_01	**Transform coefficient 01, s2.10** Value range: -4 ~ 3.99
12:0	C_00	**Transform coefficient 00, s2.10** Value range: -4 ~ 3.99

14002220 TRANSFORM_4 Color Transform Control 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_10												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_02												
Type				RW												

Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	C_10	**Transform coefficient 10, s2.10** Value range: -4 ~ 3.99
12:0	C_02	**Transform coefficient 02, s2.10** Value range: -4 ~ 3.99

14002228 TRANSFORM 5 Color Transform Control 5 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_12												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_11												
Type				RW												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	C_12	**Transform coefficient 12, s2.10** Value range: -4 ~ 3.99
12:0	C_11	**Transform coefficient 11, s2.10** Value range: -4 ~ 3.99

14002230 TRANSFORM 6 Color Transform Control 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_21												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_20												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	C_21	**Transform coefficient 21, s2.10** Value range: -4 ~ 3.99
12:0	C_20	**Transform coefficient 20, s2.10** Value range: -4 ~ 3.99

14002238 TRANSFORM 7 Color Transform Control 7 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_22												
Type				RW												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	C_22	**Transform coefficient 22, s2.10** Value range: -4 ~ 3.99

14002240 DMABUF_CON_0 **DMA Buffer 0 Control Register** **03000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						EXTRD_ARB_MAX_0				BUF_RESV_SIZE_0						
Type						RW				RW						
Reset						0	1	1		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										ISSUE_REQ_TH_0						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	EXTRD_ARB_MAX_0	**Maximum outstanding ability for DMA buffer 0** 0-7 denotes outstanding number 1-8.
22:16	BUF_RESV_SIZE_0	**Buffer size reserved for overflow prevention and FIFO size test** fifo_pseudo_size = (fifo_real_size-buf_resv_size)
6:0	ISSUE_REQ_TH_0	**Issues normal requests when FIFO valid data <= fifo_pseudo_size - issue_req_th and keeps issuing requests until valid data in command phase = fifo_pseudo_size**

14002248 DMAULTRA_CON_0 **DMA Buffer 0 Ultra Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PRE_ULTRA_TH_HIGH_OFS_0								ULTRA_TH_HIGH_OFS_0						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PRE_ULTRA_TH_LOW_OFS_0								ULTRA_TH_LOW_0						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	PRE_ULTRA_TH_HIGH_OFS_0	**pre_ultra_th_high = ultra_th_high + pre_ultra_th_high_ofs**
22:16	ULTRA_TH_HIGH_OFS_0	**ultra_th_high = pre_ultra_th_low + ultra_th_high_ofs**
14:8	PRE_ULTRA_TH_LOW_OFS_0	**pre_ultra_th_low = ultra_th_low +**

Bit(s)	Name	Description
6:0	ULTRA_TH_LOW_0	**pre_ultra_th_low_ofs** Issues pre-ultra high requests when FIFO valid data <= pre_ultra_th_low and keeps it asserted until FIFO valid data >= pre_ultra_th_high **Issues ultra high requests when FIFO valid data <= ultra_th_low** and keeps it asserted until FIFO valid data >= ultra_th_high

14002250 DMABUF_CON_1 **DMA Buffer 1 Control Register** **03000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						EXTRD_ARB_MAX_1					BUF_RESV_SIZE_1					
Type						RW					RW					
Reset						0	1	1			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ISSUE_REQ_TH_1					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
26:24	EXTRD_ARB_MAX_1	**Maximum outstanding ability for DMA buffer 1** 0-7 denotes outstanding number 1-8.
21:16	BUF_RESV_SIZE_1	**Buffer size reserved for overflow prevention and FIFO size test** fifo_pseudo_size = (fifo_real_size-buf_resv_size)
5:0	ISSUE_REQ_TH_1	**Issues normal requests when FIFO valid data <= fifo_pseudo_size - issue_req_th and keeps issuing requests until valid data in command phase = fifo_pseudo_size**

14002258 DMAULTRA_CON_1 **DMA Buffer 1 Ultra Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			PRE_ULTRA_TH_HIGH_OFS_1								ULTRA_TH_HIGH_OFS_1					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			PRE_ULTRA_TH_LOW_OFS_1								ULTRA_TH_LOW_1					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
29:24	PRE_ULTRA_TH_HIGH_OFS_1	**pre_ultra_th_high = ultra_th_high + pre_ultra_th_high_ofs**
21:16	ULTRA_TH_HIGH_OFS_1	**ultra_th_high = pre_ultra_th_low + ultra_th_high_ofs**
13:8	PRE_ULTRA_TH_LOW_OFS_1	**pre_ultra_th_low = ultra_th_low + pre_ultra_th_low_ofs** Issues pre-ultra high requests when FIFO valid data <=

Bit(s)	Name	Description
5:0	ULTRA_TH_LOW_1	pre_ultra_th_low and keeps it asserted until FIFO valid data >= pre_ultra_th_high **Issues ultra high requests when FIFO valid data <= ultra_th_low,** and keeps it asserted until FIFO valid data >= ultra_th_high

14002260 DMABUF_CON_2 **DMA Buffer 2 Control Register** **03000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						EXTRD_ARB_MAX_2						BUF_RESV_SIZE_2				
Type						RW						RW				
Reset						0	1	1				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												ISSUE_REQ_TH_2				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
26:24	EXTRD_ARB_MAX_2	**Maximum outstanding ability for DMA buffer 2** 0-7 denotes outstanding number 1-8.
20:16	BUF_RESV_SIZE_2	**Buffer size reserved for overflow prevention and FIFO size test** fifo_pseudo_size = (fifo_real_size-buf_resv_size)
4:0	ISSUE_REQ_TH_2	**Issues normal requests when FIFO valid data <= fifo_pseudo_size - issue_req_th and keeps issuing requests until valid data in command phase = fifo_pseudo_size**

14002268 DMAULTRA_CON_2 **DMA Buffer 2 Ultra Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				PRE_ULTRA_TH_HIGH_OFS_2								ULTRA_TH_HIGH_OFS_2				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PRE_ULTRA_TH_LOW_OFS_2								ULTRA_TH_LOW_2				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
28:24	PRE_ULTRA_TH_HIGH_OFS_2	**pre_ultra_th_high = ultra_th_high + pre_ultra_th_high_ofs**
20:16	ULTRA_TH_HIGH_OFS_2	**ultra_th_high = pre_ultra_th_low + ultra_th_high_ofs**
12:8	PRE_ULTRA_TH_LOW_OFS_2	**pre_ultra_th_low = ultra_th_low + pre_ultra_th_low_ofs** Issues pre-ultra high requests when FIFO valid data <=

Bit(s)	Name	Description
4:0	ULTRA_TH_LOW_2	pre_ultra_th_low and keeps it asserted until FIFO valid data >= pre_ultra_th_high **Issues ultra high requests when FIFO valid data <= ultra_th_low** and keeps it asserted until FIFO valid data >= ultra_th_high

14002270 PROC_TRACK_CON_0 DMA Processing Tracking Control 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		IGNORE_INIT_LATENCY	STOP_GREQ_EN	PROC_PRE_ULTRA_EN												
Type		RW	RW	RW												
Reset		0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TRACK_WINDOW											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	IGNORE_INIT_LATENCY	**Ignores initial latency from SOF to the first proc_one**
29	STOP_GREQ_EN	**Enables stop_greq of the process tracking**
28	PROC_PRE_ULTRA_EN	**Enables pre_ultra of the process tracking** If this bit is enabled, pre_ultra will be contolled by process tracking unit.
11:0	TRACK_WINDOW	**Tracking window** Unit: bclk_ck cycle

14002278 PROC_TRACK_CON_1 DMA Processing Tracking Control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									TARGET_CNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TARGET_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	TARGET_CNT	**Target process count during TRACK_WINDOW** It is a 16.8 fix point number.

14002280 PROC_TRACK_CON_2 DMA Processing Tracking Control 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									STOP_CNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STOP_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	STOP_CNT	If processing counter > STOP_CNT, stop issuing greq.

14002288 RESV_DUMMY_0 Reserved Dummy Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_DUMMY_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_DUMMY_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_DUMMY_0	**Dummy register** Reserved

14002300 CHKS_EXTR Checksum For EXT Read 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_EXTR_CRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_EXTR_CRC															CHKS_EXTR_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_EXTR_CRC	Checksum result for external (EMI) read data
0	CHKS_EXTR_CLR	Clears checksum to 0

14002308 CHKS_INTW Checksum For INT Writer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_INTW_CRC															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_INTW_CRC															CHKS_INTW_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_INTW_CRC	Checksum result for internal (SYSRAM) write data
0	CHKS_INTW_CLR	Clears checksum to 0

14002310 CHKS_INTR Checksum For INT Read 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_INTR_CRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_INTR_CRC															CHKS_INTR_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_INTR_CRC	Checksum result for internal (SYSRAM) read data
0	CHKS_INTR_CLR	Clears checksum to 0

14002318 CHKS_ROTO Checksum For Rotator Output 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_ROTO_CRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_ROTO_CRC															CHKS_ROTO_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_ROTO_CRC	Checksum result for rotator output data to SCL
0	CHKS_ROTO_CLR	Clears checksum to 0

14002320 CHKS_SRIY Checksum For SRAM Input Y 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_SRIY_CRC															

Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_SRIY_CRC															CHKS_SRIY_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_SRIY_CRC	Checksum result for EMI data buffer SRAM input Y
0	CHKS_SRIY_CLR	Clears checksum to 0

14002328 CHKS_SRIU Checksum For SRAM Input U 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_SRIU_CRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_SRIU_CRC															CHKS_SRIU_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_SRIU_CRC	Checksum result for EMI data buffer SRAM input U
0	CHKS_SRIU_CLR	Clears checksum to 0

14002330 CHKS_SRIV Checksum For SRAM Input V 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_SRIV_CRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_SRIV_CRC															CHKS_SRIV_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_SRIV_CRC	Checksum result for EMI data buffer SRAM input V
0	CHKS_SRIV_CLR	Clears checksum to 0

14002338 CHKS_SROY Checksum For SRAM Output Y 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	CHKS_SROY_CRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_SROY_CRC															CHKS_SROY_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_SROY_CRC	Checksum result for EMI data buffer SRAM output Y
0	CHKS_SROY_CLR	Clears checksum to 0

14002340 CHKS_SROU Checksum For SRAM Output U 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_SROU_CRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_SROU_CRC															CHKS_SROU_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_SROU_CRC	Checksum result for EMI data buffer SRAM output U
0	CHKS_SROU_CLR	Clears checksum to 0

14002348 CHKS_SROV Checksum For SRAM Output V 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_SROV_CRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_SROV_CRC															CHKS_SROV_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_SROV_CRC	Checksum result for EMI data buffer SRAM output V
0	CHKS_SROV_CLR	Clears checksum to 0

14002350 CHKS_VUPI Checksum For Vertical 00000000

Upsample Input

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_VUPI_CRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_VUPI_CRC															CHKS_VUPI_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_VUPI_CRC	Checksum result for vertical chroma upsample line buffer (SRAM) input
0	CHKS_VUPI_CLR	Clears checksum to 0

14002358 CHKS_VUPO Checksum For Vertical Upsample Output 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKS_VUPO_CRC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKS_VUPO_CRC															CHKS_VUPO_CLR
Type	RU															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CHKS_VUPO_CRC	Checksum result for vertical chroma upsample line buffer (SRAM) output
0	CHKS_VUPO_CLR	Clears checksum to 0

14002380 DEBUG_CON Debug Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				debug_out_sel								CHKS_TRB_SEL				CHKS_CRC_EN
Type				RW								RW				RW
Reset				0	0	0	0	0				0				0

Bit(s)	Name	Description
12:8	debug_out_sel	**Debugging output sel 0-22 mapped to MON_STA0-22**

Bit(s)	Name	Description
4	CHKS_TRB_SEL	**Controls all checksum registers** 0: CHKS_INTW/CHKS_INTR sel transpose buffer 0 1: CHKS_INTW/CHKS_INTR sel transpose buffer 1
0	CHKS_CRC_EN	**Controls all checksum registers** 0: Disable. Default to omit power consumption 1: Enable checksum for debugging

14002400 MON_STA_0 Monitor for Status 0 00000090

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_0	Monitor mdp_rdma status

14002408 MON_STA_1 Monitor for Status 1 00600100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_1															
Type	RU															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_1	Monitor mdp_rdma status

14002410 MON_STA_2 Monitor for Status 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_2	Monitor mdp_rdma status

14002418 MON_STA_3 Monitor for Status 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_3	Monitor mdp_rdma status

14002420 MON_STA_4 Monitor for Status 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_4															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_4															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_4	Monitor mdp_rdma status

14002428 MON_STA_5 Monitor for Status 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_5															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_5															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_5	Monitor mdp_rdma status

14002430 MON_STA_6 Monitor for Status 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_6															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_6															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_6	Monitor mdp_rdma status

14002438 MON_STA_7 Monitor for Status 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_7															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_7															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_7	Monitor mdp_rdma status

14002440 MON_STA_8 Monitor for Status 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_8															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_8															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_8	Monitor mdp_rdma status

14002448 MON_STA_9 Monitor for Status 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_9															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_9															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_9	Monitor mdp_rdma status

14002450 MON_STA_10 Monitor for Status 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_10															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_10															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_10	Monitor mdp_rdma status

14002458 MON_STA_11 Monitor for Status 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_11															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_11															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_11	Monitor mdp_rdma status

14002460 MON_STA_12 Monitor for Status 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_12															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_12															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_12	Monitor mdp_rdma status

14002468 MON_STA_13 Monitor for Status 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_13															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_13															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_13	Monitor mdp_rdma status

14002470 MON_STA_14 Monitor for Status 14 00002000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_14															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_14															
Type	RU															
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_14	Monitor mdp_rdma status

14002478 MON_STA_15 Monitor for Status 15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_15															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_15															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_15	Monitor mdp_rdma status

14002480 MON_STA_16 Monitor for Status 16 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_16															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_16															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_16	Monitor mdp_rdma status

14002488 MON_STA_17 Monitor for Status 17 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_17															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_17															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_17	Monitor mdp_rdma status

14002490 MON_STA_18 Monitor for Status 18 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_18															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_18															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_18	Monitor mdp_rdma status

14002498 MON_STA_19 Monitor for Status 19 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_19															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_19															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_19	Monitor mdp_rdma status

140024A0 MON_STA_20 Monitor for Status 20 00002000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_20															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_20															
Type	RU															
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_20	Monitor mdp_rdma status

Bit(s)	Name	Description

140024A8 MON_STA_21 Monitor for Status 21 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_21															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_21															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_21	Monitor mdp_rdma status

140024B0 MON_STA_22 Monitor for Status 22 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_22															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_22															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_22	Monitor mdp_rdma status

140024B8 MON_STA_23 Monitor for Status 23 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_23															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_23															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_23	Monitor mdp_rdma status

140024C0 MON_STA_24 Monitor for Status 24 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_24															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_24															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_24	Monitor mdp_rdma status

140024C8 MON_STA_25 Monitor for Status 25 00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_25															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_25															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_25	Monitor mdp_rdma status

140024D0 MON_STA_26 Monitor for Status 26 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MON_STA_26															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MON_STA_26															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MON_STA_26	Monitor mdp_rdma status

14002F00 SRC_BASE_0 Source Base Address 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_BASE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_BASE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_BASE_0	**Rotator source starting base address 0** Base address of the first plane of source frame. In 2- or 3-plane

Bit(s)	Name	Description
		mode, the first plane should be Y plane.

14002F08 SRC_BASE_1 Source Base Address 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_BASE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_BASE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_BASE_1	**Rotator source starting base address 1** When the source frame has 2 or 3 planes, it represents the base address of the second plane. In 2-plane mode, the second plane should be UV plane. In 3-plane mode, the second plane should be U plane.

14002F10 SRC_BASE_2 Source Base Address 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_BASE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_BASE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_BASE_2	**Rotator source starting base address 2** When the source frame has 3 planes, it represents the base address of the third plane. The existed third plane should be V plane.

14002F20 UFO_DEC_LENGTH_BASE_Y UFO Decoder Y Length Table Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UFO_DEC_Y_LEN_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UFO_DEC_Y_LEN_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
31:0	UFO_DEC_Y_LEN_BASE	**Base address of UFO decoder length table Y**

14002F28 UFO_DEC_LENGTH_BASE_C **UFO Decoder C Length Table Base Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UFO_DEC_C_LEN_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UFO_DEC_C_LEN_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	UFO_DEC_C_LEN_BASE	Base address of UFO decoder length table C

Module name: MDP_RSZ0 Base address: (+14003000h)
Module name: MDP_RSZ1 Base address: (+14004000h)
Module name: MDP_RSZ2 Base address: (+14005000h)

Address	Name	Width	Register Function
14003000	RSZ_ENABLE	32	RSZ Enable AND Reset
14003004	RSZ_CONTROL_1	32	RSZ Control 1
14003008	RSZ_CONTROL_2	32	RSZ Control 2
1400300C	RSZ_INT_FLAG	32	RSZ Interrupt Flag
14003010	RSZ_INPUT_IMAGE	32	RSZ Input Image
14003014	RSZ_OUTPUT_IMAGE	32	RSZ Output Image
14003018	RSZ_HORIZONTAL_COEFF_STEP	32	RSZ_HORIZONTAL_COEFF_STEP
1400301C	RSZ_VERTICAL_COEFF_STEP	32	RSZ_VERTICAL_COEFF_STEP
14003020	RSZ_LUMA_HORIZONTAL_INTEGER_OFFSET	32	RSZ_LUMA_HORIZONTAL_INTEGER_OFFSET
14003024	RSZ_LUMA_HORIZONTAL_SUBPIXEL_OFFSET	32	RSZ_LUMA_HORIZONTAL_SUBPIXEL_OFFSET
14003028	RSZ_LUMA_VERTICAL_INTEGER_OFFSET	32	RSZ_LUMA_VERTICAL_INTEGER_OFFSET
1400302C	RSZ_LUMA_VERTICAL_SUBPIXEL_OFFSET	32	RSZ_LUMA_VERTICAL_SUBPIXEL_OFFSET
14003030	RSZ_CHROMA_HORIZONTAL_INTEGER_OFFSET	32	RSZ_CHROMA_HORIZONTAL_INTEGER_OFFSET
14003034	RSZ_CHROMA_HORIZONTAL_SUBPIX	32	RSZ_CHROMA_HORIZONTAL_SUBPIXEL_OFFSET

Address	Name	Width	Register Function
	EL_OFFSET		
14003038	RSZ_CHROMA_VERTICAL_INTEGER_OFFSET	32	RSZ_CHROMA_VERTICAL_INTEGER_OFFSET
1400303C	RSZ_CHROMA_VERTICAL_SUBPIXEL_OFFSET	32	RSZ_CHROMA_VERTICAL_SUBPIXEL_OFFSET
14003040	RSZ_RSV	32	RSZ_RSV
14003044	RSZ_DEBUG_SEL	32	RSZ_DEBUG_SEL
14003048	RSZ_DEBUG	32	RSZ_DEBUG
1400304C	RSZ_TAP_ADAPT	32	RSZ_TAP_ADAPT
14003050	RSZ_TBL_SEL	32	RSZ_TBL_SEL
14003054	RSZ_IBSE	32	RSZ_IBSE
14003058	RSZ_DEMO_IN_HMASK	32	RSZ_DEMO_IN_HMASK
1400305C	RSZ_DEMO_IN_VMASK	32	RSZ_DEMO_IN_VMASK
14003060	RSZ_DEMO_OUT_HMASK	32	RSZ_DEMO_OUT_HMASK
14003064	RSZ_DEMO_OUT_VMASK	32	RSZ_DEMO_OUT_VMASK
140030FC	RSZ_ATPG	32	RSZ_ATPG

14003000 RSZ_ENABLE **RSZ Enable AND Reset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RSZ_RST
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RSZ_EN
Type																RW
Reset																0

Bit(s)	Name	Description
16	RSZ_RST	Resizer Reset bit
0	RSZ_EN	Resizer Enable bit

14003004 RSZ_CONTROL_1 **RSZ Control 1** **814A0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSZ_INT_WCLR_EN	RSZ_ INTE N					RSZ_VERTICAL_TABLE_SELECT					RSZ_HORIZONTAL_TABLE_SELECT				
Type	RW	RW					RW					RW				
Reset	1	0	0	0			0	1	0	1	0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RSZ_TRUNCATION_BIT_V			RSZ_TRUNCATION_BIT_H			RSZ_LBCSON_MODE	RSZ_VERTICAL_ALGORITHM		RSZ_HORIZONTAL_ALGORITHM		RSZ_VERTICAL_FIRST			RSZ_VERTICAL_EN	RSZ_HORIZONTAL_EN
Type	RW			RW			RW	RW		RW		RW			RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
31	RSZ_INT_WCLR_EN	**Enables interrupt write-clear** 0: Interrupt read-clear 1: Interrupt write-clear
30:28	RSZ_INTEN	**Enables interrupt** Bit 2: Error interrupt Bit 1: Frame end interrupt Bit 0: Frame start interrupt
25:21	RSZ_VERTICAL_TABLE_SELECT	**Double buffer.** Selects vertical scaling coefficient table 4 tap: [0:25] (1x up ~ 1/2x down) Cubic accumulation: [0:19] (blur ~ sharp)
20:16	RSZ_HORIZONTAL_TABLE_SELECT	**Double buffer.** Selects horizontal scaling coefficient table 4 tap: [0:25] (1x up ~ 1/2x down) Cubic accumulation: [0:19] (blur ~ sharp)
15:13	RSZ_TRUNCATION_BIT_V	**Double buffer.** Cubic accumulation parameter Truncate weighting bit for high ratio down-sample
12:10	RSZ_TRUNCATION_BIT_H	**Double buffer.** Cubic accumulation parameter Truncate weighting bit for high ratio down-sample
9	RSZ_LBCSON_MODE	**Double buffer.** Line buffer control CS on mode
8:7	RSZ_VERTICAL_ALGORITHM	**Double buffer.** Vertical scaling algorithm 0: 4 tap 1: n tap source accumulation 2: 4n tap cubic accumulation 3: Reserved
6:5	RSZ_HORIZONTAL_ALGORITHM	**Double buffer.** Horizontal scaling algorithm 0: 4 tap 1: n tap source accumulation 2: 4n tap cubic accumulation 3: Reserved
4	RSZ_VERTICAL_FIRST	**Double buffer.** 0: Horiznotal first then vertical scaling 1: Vertical first then horizontal scaling
1	RSZ_VERTICAL_EN	**Double buffer.** Enables vertical scaling function.
0	RSZ_HORIZONTAL_EN	**Double buffer.** Enables horizontal scaling function.

14003008 RSZ_CONTROL_2 RSZ Control 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RSZ_DEMO_MODE		RSZ_DEMO_SWAP	RSZ_DEMO_EN
Type													RW		RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3:2	RSZ_DEMO_MODE	**0: all function** 1: tap-adaptive only 2: in-band-signal-preservation only
1	RSZ_DEMO_SWAP	**0: inside window** 1: outside window
0	RSZ_DEMO_EN	**0: disable** 1: enable

1400300C RSZ_INT_FLAG **RSZ Interrupt Flag** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RSZ_SOF_RESET	RSZ_SIZE_ERR			RSZ_FRAME_END	RSZ_FRAME_START
Type											RO	RO			RO	RO
Reset											0	0			0	0

Bit(s)	Name	Description
5	RSZ_SOF_RESET	SOF reset interrupt
4	RSZ_SIZE_ERR	Size error Interrupt
1	RSZ_FRAME_END	Frame end interrupt
0	RSZ_FRAME_START	Frame start interrupt

14003010 RSZ_INPUT_IMAGE **RSZ Input Image** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSZ_INPUT_IMAGE_H															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_INPUT_IMAGE_W															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RSZ_INPUT_IMAGE_H	**Double buffer** Height of imput image
15:0	RSZ_INPUT_IMAGE_W	**Double buffer**

Bit(s)	Name	Description
		Width of input image

14003014 RSZ_OUTPUT_IMAGE — RSZ Output Image — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSZ_OUTPUT_IMAGE_H															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_OUTPUT_IMAGE_W															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RSZ_OUTPUT_IMAGE_H	**Double buffer** Height of output image
15:0	RSZ_OUTPUT_IMAGE_W	**Double buffer** Width of output image

14003018 RSZ_HORIZONTAL_COEFF_STEP — RSZ_HORIZONTAL_COEFF_STEP — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										RSZ_HORIZONTAL_COEFF_STEP						
Type										RW						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_HORIZONTAL_COEFF_STEP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
22:0	RSZ_HORIZONTAL_COEFF_STEP	**Double buffer** Horiznotal scaling ratio

1400301C RSZ_VERTICAL_COEFF_STEP — RSZ_VERTICAL_COEFF_STEP — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										RSZ_VERTICAL_COEFF_STEP						
Type										RW						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_VERTICAL_COEFF_STEP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
22:0	RSZ_VERTICAL_COEFF_STEP	**Double buffer** Vertical scaling ratio

14003020 RSZ_LUMA_HORIZONTAL_INTEGER_OFFSET RSZ_LUMA_HORIZONTAL_INTEGER_OFFSET 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_LUMA_HORIZONTAL_INTEGER_OFFSET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RSZ_LUMA_HORIZONTAL_INTEGER_OFFSET	**Double buffer** Horizontal luma integer offset

14003024 RSZ_LUMA_HORIZONTAL_SUBPIXEL_OFFSET RSZ_LUMA_HORIZONTAL_SUBPIXEL_OFFSET 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												RSZ_LUMA_HORIZONTAL_SUBPIXEL_OFFSET				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_LUMA_HORIZONTAL_SUBPIXEL_OFFSET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	RSZ_LUMA_HORIZONTAL_SUBPIXEL_OFFSET	**Double buffer** Horizontal luma sub-pixel offset

14003028 RSZ_LUMA_VERTICAL_INTEGER_OFFSET RSZ_LUMA_VERTICAL_INTEGER_OFFSET 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_LUMA_VERTICAL_INTEGER_OFFSET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RSZ_LUMA_VERTICAL_INTEGER_OFFSET	**Double buffer** Vertical luma integer offset

1400302C RSZ_LUMA_VERTICAL_SUBPIXEL_OFFSET RSZ_LUMA_VERTICAL_SUBPIXEL_OFFSET 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												RSZ_LUMA_VERTICAL_SUBPIXEL_OFFSET				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_LUMA_VERTICAL_SUBPIXEL_OFFSET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	RSZ_LUMA_VERTICAL_SUBPIXEL_OFFSET	**Double buffer** Vertical luma sub-pixel offset

14003030 RSZ_CHROMA_HORIZONTAL_INTEGER_OFFSET RSZ_CHROMA_HORIZONTAL_INTEGER_OFFSET 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_CHROMA_HORIZONTAL_INTEGER_OFFSET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RSZ_CHROMA_HORIZONTAL_INTEGER_OFFSET	**Double buffer** Horizontal chroma integer offset

14003034 RSZ_CHROMA_HORIZONTAL_SUBPIXEL_OFFSET RSZ_CHROMA_HORIZONTAL_SUBPIXEL_OFFSET 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												RSZ_CHROMA_HORIZONTAL_SUBPIXEL_OFFSET				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_CHROMA_HORIZONTAL_SUBPIXEL_OFFSET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	RSZ_CHROMA_HORIZONTAL_SUBPIXEL_OFFSET	**Double buffer** Horizontal chroma sub-pixel offset

14003038 RSZ_CHROMA_VERTICAL_INTEGER_OFFSET RSZ_CHROMA_VERTICAL_INTEGER_OFFSET 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_CHROMA_VERTICAL_INTEGER_OFFSET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RSZ_CHROMA_VERTICAL_INTEGER_OFFSET	**Double buffer** Vertical chroma integer offset

1400303C RSZ_CHROMA_VERTICAL_SUBPIXEL_OFFSET RSZ_CHROMA_VERTICAL_SUBPIXEL_OFFSET 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												RSZ_CHROMA_VERTICAL_SUBPIXEL_OFFSET				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_CHROMA_VERTICAL_SUBPIXEL_OFFSET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	RSZ_CHROMA_VERTICAL_SUBPIXEL_OFFSET	**Double buffer** Vertical chroma sub-pixel offset

14003040 RSZ_RSV **RSZ_RSV** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSZ_RSV															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_RSV															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RSZ_RSV	**Dering parameter** In projects without dering function, this register is reserved.

14003044 RSZ_DEBUG_SEL **RSZ_DEBUG_SEL** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RSZ_DEBUG_SEL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RSZ_DEBUG_SEL	Selects debugging

14003048 RSZ_DEBUG **RSZ_DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSZ_DEBUG															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_DEBUG															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RSZ_DEBUG	Debugging register

1400304C RSZ_TAP_ADAPT **RSZ_TAP_ADAPT** **00210808**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						RSZ_TAP_	RSZ_TAP_ADAPT_EDGE_THR						RSZ_TAP_ADAPT_DC_CORING			

						ADAPT_EN										
Type						RW	RW						RW			
Reset						0	0	0	0	0	1	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_TAP_ADAPT_DC_CORING	RSZ_TAP_ADAPT_VAR_CORING					RSZ_TAP_ADAPT_FALLBACK_RATIO						RSZ_TAP_ADAPT_SLOPE			
Type	RW	RW					RW						RW			
Reset	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
26	RSZ_TAP_ADAPT_EN	**Tap-adaptive enable bit**
25:20	RSZ_TAP_ADAPT_EDGE_THR	**Double buffer** Tap-adaptive edge threshold
19:15	RSZ_TAP_ADAPT_DC_CORING	**Double buffer** Tap-adaptive DC coring
14:10	RSZ_TAP_ADAPT_VAR_CORING	**Double buffer** Tap-adaptive Variance coring
9:4	RSZ_TAP_ADAPT_FALLBACK_RATIO	**Double buffer** Tap-adaptive fallback ratio
3:0	RSZ_TAP_ADAPT_SLOPE	**Double buffer** Tap-adaptive slope

14003050 RSZ_TBL_SEL RSZ_TBL_SEL 00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RSZ_TBL_HW_SEL
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
16	RSZ_TBL_HW_SEL	**Double buffer** 0: Default setting 1: Table index: 9~11

14003054 RSZ_IBSE RSZ_IBSE 00040100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RSZ_IBSE_EN	RSZ_IBSE_CLIP_EN										RSZ_IBSE_CLIP_RATIO			
Type		RW	RW										RW			
Reset		0	0										0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RSZ_IBSE_CLIP_RATIO	RSZ_IBSE_CLIP_THR								RSZ_IBSE_GAIN_MID						RSZ_IBSE_TBL_IDX_MID	
Type	RW	RW								RW						RW	
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	RSZ_IBSE_EN	In-Band-Signal-Enhancement enable bit
29	RSZ_IBSE_CLIP_EN	Soft clip enable bit
19:15	RSZ_IBSE_CLIP_RATIO	Soft clip ratio
14:7	RSZ_IBSE_CLIP_THR	Soft clip positive threshold
6:2	RSZ_IBSE_GAIN_MID	In-Band-Signal-Enhancement mid-band gain
1:0	RSZ_IBSE_TBL_IDX_MID	In-Band-Signal-Enhancement mid-band table index

14003058 RSZ_DEMO_IN_HMASK RSZ_DEMO_IN_HMASK 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSZ_DEMO_IN_MASK_HSTART															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_DEMO_IN_MASK_HEND															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RSZ_DEMO_IN_MASK_HSTART	Horizontal start position of demo window defined in input domain
15:0	RSZ_DEMO_IN_MASK_HEND	Horizontal end position of demo window defined in input domain

1400305C RSZ_DEMO_IN_VMASK RSZ_DEMO_IN_VMASK 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSZ_DEMO_IN_MASK_VSTART															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_DEMO_IN_MASK_VEND															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RSZ_DEMO_IN_MASK_VSTART	Vertical start position of demo window defined in input domain
15:0	RSZ_DEMO_IN_MASK_VEND	Vertical end position of demo window defined in input domain

14003060 RSZ_DEMO_O RSZ_DEMO_OUT_HMASK 00000000

UT_HMASK

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSZ_DEMO_OUT_MASK_HSTART															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_DEMO_OUT_MASK_HEND															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RSZ_DEMO_OUT_MASK_HSTART	Horizontal start position of demo window defined in output domain
15:0	RSZ_DEMO_OUT_MASK_HEND	Horizontal end position of demo window defined in output domain

14003064 RSZ_DEMO_OUT_VMASK RSZ_DEMO_OUT_VMASK 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSZ_DEMO_OUT_MASK_VSTART															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RSZ_DEMO_OUT_MASK_VEND															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RSZ_DEMO_OUT_MASK_VSTART	Vertical start position of demo window defined in output domain
15:0	RSZ_DEMO_OUT_MASK_VEND	Vertical end position of demo window defined in output domain

140030FC RSZ_ATPG RSZ_ATPG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RSZ_ATPG_CT	RSZ_ATPG_OB
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RSZ_ATPG_CT	
0	RSZ_ATPG_OB	

Module name: MDP_WROTo Base address: (+14007000h)

Address	Name	Width	Register Function
14007000	MDP_WROToVIDO_CTRL	32	VIDO Control
14007004	MDP_WROToVIDO_DMA_PERF	32	VIDO DMA Performance
14007008	MDP_WROToVIDO_MAIN_BUF_SIZE	32	VIDO DMA Main Buffer Size
14007010	MDP_WROToVIDO_SOFT_RST	32	VIDO Software Reset
14007014	MDP_WROToVIDO_SOFT_RST_STAT	32	VIDO Software Reset Status
14007018	MDP_WROToVIDO_INT_EN	32	VIDO Interrupt Enable
1400701C	MDP_WROToVIDO_INT	32	VIDO Interrupt
14007020	MDP_WROToVIDO_CROP_OFST	32	VIDO Image Cropping Offset
14007024	MDP_WROToVIDO_TAR_SIZE	32	VIDO Target Image Size
1400702C	MDP_WROToVIDO_OFST_ADDR	32	VIDO Offset Address
14007030	MDP_WROToVIDO_STRIDE	32	VIDO Stride
14007038	MDP_WROToVIDO_OFST_ADDR_C	32	VIDO Offset Address Chroma
1400703C	MDP_WROToVIDO_STRIDE_C	32	VIDO Stride Chroma
14007054	MDP_WROToVIDO_DITHER	32	VIDO Dithering
14007068	MDP_WROToVIDO_OFST_ADDR_V	32	VIDO Offset Address Chroma 2
1400706C	MDP_WROToVIDO_STRIDE_V	32	VIDO Stride Chroma 2
14007070	MDP_WROToVIDO_RSV_1	32	VIDO Spare Registers
14007074	MDP_WROToVIDO_DMA_PREULTRA	32	VIDO Pre Ultra Setting
14007078	MDP_WROToVIDO_IN_SIZE	32	VIDO Input Image Size
1400707C	MDP_WROToVIDO_ROT_EN	32	VIDO Rotation Enable
14007080	MDP_WROToVIDO_FIFO_TEST	32	DMA FIFO Test
14007084	MDP_WROToVIDO_MAT_CTRL	32	VIDO Matrix Control
14007088	MDP_WROToVIDO_MAT_RMY	32	VIDO Y2R Conversion Parameter Ro
1400708C	MDP_WROToVIDO_MAT_RMV	32	VIDO Y2R Conversion Parameter R1
14007090	MDP_WROToVIDO_MAT_GMY	32	VIDO Y2R Conversion Parameter Go
14007094	MDP_WROToVIDO_MAT_BMY	32	VIDO Y2R Conversion Parameter Bo

Address	Name	Width	Register Function
14007098	MDP_WROTOVIDO_MAT_BMV	32	VIDO Y2R Conversion Parameter B1
1400709C	MDP_WROTOVIDO_MAT_PREADD	32	VIDO Y2R Conversion Parameter Extended Add on YUV
140070A0	MDP_WROTOVIDO_MAT_POSTADD	32	VIDO Y2R Conversion Parameter Extended Add on RGB
140070A4	MDP_WROTOVIDO_DITHER_00	32	VIDO Dithering Control Register 0
140070AC	MDP_WROTOVIDO_DITHER_02	32	VIDO Dithering Control Register 2
140070B0	MDP_WROTOVIDO_DITHER_03	32	VIDO Dithering Control Register 3
140070B4	MDP_WROTOVIDO_DITHER_04	32	VIDO Dithering Control Register 4
140070B8	MDP_WROTOVIDO_DITHER_05	32	VIDO Dithering Control Register 5
140070BC	MDP_WROTOVIDO_DITHER_06	32	VIDO Dithering Control Register 6
140070C0	MDP_WROTOVIDO_DITHER_07	32	VIDO Dithering Control Register 7
140070C4	MDP_WROTOVIDO_DITHER_08	32	VIDO Dithering Control Register 8
140070C8	MDP_WROTOVIDO_DITHER_09	32	VIDO Dithering Control Register 9
140070CC	MDP_WROTOVIDO_DITHER_10	32	VIDO Dithering Control Register 10
140070D0	MDP_WROTOVIDO_DEBUG	32	VIDO Debug Register
140070D4	MDP_WROTOVIDO_ARB_SW_CTL	32	VIDO DMA Arbiter Software Control
140070E0	MDP_WROTOMDP_WROT_TRACK_CTL	32	MDP WROT Pre-ultra Track Control
140070E4	MDP_WROTOMDP_WROT_TRACK_WINDOW	32	MDP WROT Pre-ultra Track Window
140070E8	MDP_WROTOMDP_WROT_TRACK_TARGET	32	MDP WROT Pre-ultra Track Target
140070EC	MDP_WROTOMDP_WROT_TRACK_STOP	32	MDP WROT Pre-ultra Track Stop
140070F0	MDP_WROTOMDP_WROT_TRACK_PROC_CNT0	32	MDP WROTPre-ultra Track Proc Counter 0
140070F4	MDP_WROTOMDP_WROT_TRACK_PROC_CNT1	32	MDP WROTPre-ultra Track Proc Counter 1
14007F00	MDP_WROTOVIDO_BASE_ADDR	32	VIDO Base Address
14007F04	MDP_WROTOVIDO_BASE_ADDR_C	32	VIDO Base Address Chroma
14007F08	MDP_WROTOVIDO_BASE_ADDR_V	32	VIDO Base Address Chroma 2

14007000 MDP_WROTOVIDO_CTRL **VIDO Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VIDO_UV_YSEL		VIDO_UV_XSEL			VIDO_SOF_RESET_EN		VIDO_FLIP			VIDO_ROTATION					
Type	RW		RW			RW		RW			RW					
Reset	0	0	0	0		0		0			0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		VIDO_PREULTRA_EN	VIDO_PRI_EN	VIDO_CROP_EN				VIDO_UNIFORM_SWAP				VIDO_BLK_OPTION	VIDO_UNIFORM_FORMAT			
Type		RW	RW	RW				RW				RW	RW			
Reset		0	0	0				0				0	0	0	0	0

Bit(s)	Name	Description
31:30	VIDO_UV_YSEL	**Selects vertical UV** 0: Pick from 0. 0,2,4... 1: Pick from 1. 1,3,5... 2: Pick every pixel
29:28	VIDO_UV_XSEL	**Selects horizontal UV** 0: Pick from 0. 0,2,4... 1: Pick from 1. 1,3,5... 2: Pick every pixel
26	VIDO_SOF_RESET_EN	**Enables SOF reset** 0: No SOF reset 1: Do Soft reset process on receiving SOF
24	VIDO_FLIP	**Enables horizontal flip** Note: The flip action is done after horizontal 0: No flip 1: Flip
21:20	VIDO_ROTATION	**Rotation angle** 0: 0 degree 1: 90 degree 2: 180 degree 3: 270 degree
14	VIDO_PREULTRA_EN	**Enables pre-ultra**
13	VIDO_PRI_EN	**Enables PRI threshold**
12	VIDO_CROP_EN	**Double buffer** VIDO cropping function enabling bit
8	VIDO_UNIFORM_SWAP	
4	VIDO_BLK_OPTION	**Performance improve option** 0: Disable 1: Enable
3:0	VIDO_UNIFORM_FORMAT	

14007004 MDP_WROTOVIDO_DMA_PERF **VIDO DMA Performance** **3F000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			VIDO_CH2_SMI_GROUP_NUM		VIDO_CH1_SMI_GROUP_NUM		VIDO_CH0_SMI_GROUP_NUM		VIDO_FIFO_PRI_THR							

Type			RW		RW		RW		RW							
Reset			1	1	1	1	1	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_FIFO_PRI_THR				VIDO_FIFO_PRI_LOW_THR											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:28	VIDO_CH2_SMI_GROUP_NUM	**SMI request grouping number** It will launch consecutive SMI requests by this number for this channel. 0: 1 consecutive request 1: 2 consecutive requests 2: 3 consecutive requests 3: 4 consecutive requests
27:26	VIDO_CH1_SMI_GROUP_NUM	**SMI request grouping number** It will launch consecutive SMI requests by this number for this channel. 0: 1 consecutive request 1: 2 consecutive requests 2: 3 consecutive requests 3: 4 consecutive requests
25:24	VIDO_CH0_SMI_GROUP_NUM	**SMI request grouping number** It will launch consecutive SMI requests by this number for this channel. 0: 1 consecutive request 1: 2 consecutive requests 2: 3 consecutive requests 3: 4 consecutive requests
23:12	VIDO_FIFO_PRI_THR	**For priority control signal** If the FIFO amount is bigger than THR, the priority control signal will be asserted.
11:0	VIDO_FIFO_PRI_LOW_THR	**PRI low threshold**

14007008 MDP_WROT0V IDO_MAIN_B UF_SIZE VIDO DMA Main Buffer Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_MAIN_BLK_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		VIDO_MAIN_BUF_LINE_NUM								VIDO_FILT_TYPE_V				VIDO_FILT_TYPE_H		
Type		RW								RW				RW		
Reset		0	0	0	0	0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
28:16	VIDO_MAIN_BLK_WIDTH	**Width of line block in main working buffer** Unit: Pixel
14:8	VIDO_MAIN_BUF_LINE_NUM	**Line number of main working buffer in FIFO or single buffer mode**
6:4	VIDO_FILT_TYPE_V	**Chroma horizontal down sample filter type** 0: Bypass

Bit(s)	Name	Description
		1: Forward [1 2 1] filter 2: Backward [1 2 1] filter 3: Forward [1 1] filter 4: Backward [1 1] filter
2:0	VIDO_FILT_TYPE_H	**Chroma horizontal down sample filter type** 0: Bypass 1: Forward [1 2 1] filter 2: Backward [1 2 1] filter 3: Forward [1 1] filter 4: Backward [1 1] filter

14007010 MDP_WROTOV IDO_SOFT_RST VIDO Software Reset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VIDO_SOFT_RST
Type																RW
Reset																0

Bit(s)	Name	Description
0	VIDO_SOFT_RST	**VIDO software reset** For software reset is required, write 1 until VIDO_SOFT_RST_STAT = 1 . When VIDO_SOFT_RST_STAT = 1, write 0. Then, polling until VIDO_SOFT_RST_STAT = 0.

14007014 MDP_WROTOV IDO_SOFT_RST_STAT VIDO Software Reset Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VIDO_SOFT_RST_STAT
Type																RU
Reset																0

Bit(s)	Name	Description
0	VIDO_SOFT_RST_STAT	**VIDO software reset status** This status will be 1 when soft reset is active, and be 0 when soft

Bit(s)	Name	Description
		reset is completed.

14007018 MDP_WROTOV IDO_INT_EN VIDO Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			VIDO_CSR_DEBUG											VIDO_INT_WC_3_EN	VIDO_INT_WC_2_EN	VIDO_INT_1_EN
Type			RW											RW	RW	RW
Reset			0	0	0	0	0	0						0	0	0

Bit(s)	Name	Description
13:8	VIDO_CSR_DEBUG	**Controls VIDO debugging register**
2	VIDO_INT_WC_3_EN	**Enables VIDO rotate finish status clear**
1	VIDO_INT_WC_2_EN	**Controls VIDO frame done status**
0	VIDO_INT_1_EN	**Enables VIDO interrupt 1** Interrupt situation: Crop setting is not correct.

1400701C MDP_WROTOV IDO_INT VIDO Interrupt 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														VIDO_INT_3	VIDO_INT_2	VIDO_INT_1
Type														A0	A0	A0
Reset														1	1	1

Bit(s)	Name	Description
2	VIDO_INT_3	**VIDO status** Situation: Luma rotation done. Turn on VIDO_INT_WC_3_EN and write 1 to clear.
1	VIDO_INT_2	**VIDO status** Situation: Frame done = 0. INT turns on VIDO_INT_WC_2_EN and write 1 to clear
0	VIDO_INT_1	**VIDO interrupt 1** Interrupt situation: Crop setting is not correct Turn on VIDO_INT_WC_EN and write 1 to clear.

14007020 MDP_WROTOV IDO_CROP_OFST VIDO Image Cropping Offset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name				VIDO_CROP_OFST_Y												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_CROP_OFST_X												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	VIDO_CROP_OFST_Y	**Double buffer** Y channel offset position for cropping. If VIDO_FORMAT is YUV422 or YUV422V, y channel width must be multiple of 2.
12:0	VIDO_CROP_OFST_X	**Double buffer** Y channel offset position for cropping. If VIDO_FORMAT is YUV422 or YUV422V, y channel width must be multiple of 2.

14007024 MDP_WROTOV IDO_TAR_SI ZE — VIDO Target Image Size — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_YSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_XSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	VIDO_YSIZE	**Double buffer** Y channel height of target image
12:0	VIDO_XSIZE	**Double buffer** Y channel width of Target image If VIDO_FORMAT is YUV422 or YUV422V, y channel width must be multiple of 2.

1400702C MDP_WROTOV IDO_OFST_A DDR — VIDO Offset Address — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VIDO_OFST_ADDR											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_OFST_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
27:0	VIDO_OFST_ADDR	**Double buffer** VIDO offset address 1. It follows the definition of Base Address 1.

14007030 MDP_WROTOVIDO_STRIDE VIDO Stride 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_STRIDE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	VIDO_STRIDE	**Double buffer** VIDO stride 1. It follows the definition of Base Address 2.

14007038 MDP_WROTOVIDO_OFST_ADDR_C VIDO Offset Address Chroma 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VIDO_OFST_ADDR_C											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_OFST_ADDR_C															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:0	VIDO_OFST_ADDR_C	**Double buffer** VIDO offset address 2. It follows the definition of Base Address 2.

1400703C MDP_WROTOVIDO_STRIDE_C VIDO Stride Chroma 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_STRIDE_C															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	VIDO_STRIDE_C	**Double buffer**

Bit(s)	Name	Description
		VIDO stride 2. It follows the definition of Base Address 2.

14007054 MDP_WROTOV IDO_DITHER VIDO Dithering 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VIDO_XRGB_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VIDO_DIT_EN
Type																RW
Reset																0

Bit(s)	Name	Description
31:24	VIDO_XRGB_DUMMY	XRGB format 8-bit dummy data
0	VIDO_DIT_EN	Enables VIDO dithering

14007068 MDP_WROTOV IDO_OFST_ADDR_V VIDO Offset Address Chroma 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VIDO_OFST_ADDR_V											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_OFST_ADDR_V															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:0	VIDO_OFST_ADDR_V	**Double buffer** VIDO offset address 3. It follows the definition of Base Address 3.

1400706C MDP_WROTOV IDO_STRIDE_V VIDO Stride Chroma 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_STRIDE_V															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
15:0	VIDO_STRIDE_V	**Double buffer** VIDO stride 3. It follows the definition of Base Address 3.

14007070 MDP_WROTOVIDO_RSV_1 VIDO Spare Registers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VIDO_RSV_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_RSV_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VIDO_RSV_1	VIDO spare registers

14007074 MDP_WROTOVIDO_DMA_PREULTRA VIDO Pre Ultra Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									VIDO_FIFO_PREULTRA_THR							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_FIFO_PREULTRA_THR				VIDO_FIFO_PREULTRA_THR_LOW											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:12	VIDO_FIFO_PREULTRA_THR	Pre-ultra high threshold
11:0	VIDO_FIFO_PREULTRA_THR_LOW	Pre-ultra low threshold

14007078 MDP_WROTOVIDO_IN_SIZE VIDO Input Image Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_IN_YSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_IN_XSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
28:16	VIDO_IN_YSIZE	**Double buffer** Y channel height of input image
12:0	VIDO_IN_XSIZE	**Double buffer** Y channel width of Input image If VIDO_FORMAT is YUV422 or YUV422V, y channel width must be multiple of 2.

1400707C MDP_WROTOVIDO_ROT_EN VIDO Rotation Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VIDO_ROT_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	VIDO_ROT_EN	Enables rotation

14007080 MDP_WROTOVIDO_FIFO_T EST DMA FIFO Test 00000080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					VIDO_FIFO_SIZE											
Type					RW											
Reset					0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	VIDO_FIFO_SIZE	ROT FIFO size

14007084 MDP_WROTOVIDO_MAT_CT RL VIDO Matrix Control 00000040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									VIDO_MTX_ SEL						VIDO_EXT_MTX_EN	VIDO_MAT_EN

Type									RW						RW	RW
Reset									0	1	0	0			0	0

Bit(s)	Name	Description
7:4	VIDO_MTX_SEL	**Double buffer** Selects color matrix format Default: 601 to 709 0: RGB to JPEG 2: RGB to 601 3: RGB to 709 4: JPEG to RGB 6: 601 to RGB 7: 709 to RGB 8: JPEG to 601 9: JPEG to 709 10: 601 to JPEG 11: 709 to JPEG 12: 709 to 601
1	VIDO_EXT_MTX_EN	**Double buffer** Selects color matrix auto mode 0: Use auto mode 1: Use programmable coeff
0	VIDO_MAT_EN	**Double buffer** Enables matrix 0: Bypass 1: Enable

14007088 MDP_WROT0V_IDO_MAT_RM_Y **VIDO Y2R Conversion Parameter R0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_RMU												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_RMY												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	VIDO_RMU	VIDO YUV2RGB program parameter for R color of U component
12:0	VIDO_RMY	VIDO YUV2RGB program parameter for R color of Y component

1400708C MDP_WROT0V_IDO_MAT_RM_V **VIDO Y2R Conversion Parameter R1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_GMY												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_RMV												

Type				RW													
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	VIDO_GMY	VIDO YUV2RGB program parameter for G color of Y component
12:0	VIDO_RMV	VIDO YUV2RGB program parameter for R color of V component

14007090 MDP_WROTOV_VIDO_MAT_GM_Y VIDO Y2R Conversion Parameter G0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_GMV												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_GMU												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	VIDO_GMV	VIDO YUV2RGB program parameter for G color of V component
12:0	VIDO_GMU	VIDO YUV2RGB program parameter for G color of U component

14007094 MDP_WROTOV_VIDO_MAT_BM_Y VIDO Y2R Conversion Parameter B0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_BMU												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_BMY												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	VIDO_BMU	VIDO YUV2RGB program parameter for B color of U component
12:0	VIDO_BMY	VIDO YUV2RGB program parameter for B color of Y component

14007098 MDP_WROTOV_VIDO_MAT_BM_V VIDO Y2R Conversion Parameter B1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_BMV												
Type				RW												

Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	VIDO_BMV	VIDO YUV2RGB program parameter for B color of V component

1400709C MDP_WROTOV IDO_MAT_PR EADD **VIDO Y2R Conversion Parameter Extended Add on YUV** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_VA										VIDO_UA		
Type				RW										RW		
Reset				0	0	0	0	0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_UA							VIDO_YA								
Type	RW							RW								
Reset	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:20	VIDO_VA	VIDO YUV2RGB program parameter for V to add extended offset
18:10	VIDO_UA	VIDO YUV2RGB program parameter for U to add extended offset
8:0	VIDO_YA	VIDO YUV2RGB program parameter for Y to add extended offset

140070A0 MDP_WROTOV IDO_MAT_PO STADD **VIDO Y2R Conversion Parameter Extended Add on RGB** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_BA										VIDO_GA		
Type				RW										RW		
Reset				0	0	0	0	0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_GA							VIDO_RA								
Type	RW							RW								
Reset	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:20	VIDO_BA	VIDO YUV2RGB program parameter for B to add extended offset
18:10	VIDO_GA	VIDO YUV2RGB program parameter for G to add extended offset
8:0	VIDO_RA	VIDO YUV2RGB program parameter for R to add extended offset

140070A4 MDP_WROTOV IDO_DITHER_00 **VIDO Dithering Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	frame_done_del										crc_clr	crc_start	crc_cen	wrap_mode	out_sel	start
Type	RW										RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
15:8	frame_done_del	**Frame done return delay**
5	crc_clr	**Write 1 to clear CRC result.**
4	crc_start	**Write 1 to start CRC counting.**
3	crc_cen	0: Turn off CRC engine CG 1: Turn on CRC engine CG
2	wrap_mode	**Enables rounding for dithering function** When the rounding method is used, both running order and error dispersion cannot be used.
1	out_sel	0: Bypass dither 1: Through dither
0	start	0: No dither 1: Start dither engine

140070AC MDP_WROT0V IDO_DITHER_02 **VIDO Dithering Control Register 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	w_demo															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			round_en	rdither_en	lfsr_en	edither_en	left_en		fphase_r	fphase_en	fphase					
Type			RW	RW	RW	RW	RW		RW	RW	RW					
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	w_demo	**Short line length**
13	round_en	**Enables rounding for dithering function** When the rounding method is used, both running order and error dispersion cannot be used.
12	rdither_en	**Enables running order dithering** The running order dithering must be set when ROUND_EN is set to 0. The running order dithering can run with error dispersion when EDOTHER_EN is set to 1.
11	lfsr_en	**Enables LFSR-type dithering**
10	edither_en	**Enables error dispersion dithering** The error dispersion dithering must be set when ROUND_EN is set to 0. The running order dithering can run with error dispersion when RDITHER_EN is set to 1.
9:8	left_en	**Enables left part of screen dither** 0: Dither runs at full screen. 1: Dither runs at left part of screen.
7	fphase_r	**Dither SubPixel addend**
6	fphase_en	**Running order dithering frame** Enables phase control
5:0	fphase	**Running order dithering frame phase increment** Note:

Bit(s)	Name	Description
		If ROUND_EN = 1, the output will be rounding only (no matter what RDITHER_EN and EDITHER_EN setting are). RDITHER_EN and EDITHER_EN can work together.

140070B0 MDP_WROT0V IDO_DITHER_03 VIDO Dithering Control Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											drmod_b		drmod_g		drmod_r	
Type											RW		RW		RW	
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:4	drmod_b	**Selects dither mode** 0: No dither 1: 12-bit dither to 10-bit 2: 12-bit dither to 8-bit 3: 12-bit dither to 6-bit
3:2	drmod_g	**Selects dither mode** 0: No dither 1: 12-bit dither to 10-bit 2: 12-bit dither to 8-bit 3: 12-bit dither to 6-bit
1:0	drmod_r	**Selects dither mode** 0: No dither 1: 12-bit dither to 10-bit 2: 12-bit dither to 8-bit 3: 12-bit dither to 6-bit

140070B4 MDP_WROT0V IDO_DITHER_04 VIDO Dithering Control Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ink		ink_data_b										ink_data_g			
Type	RW		RW										RW			
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ink_data_g						ink_data_r									
Type	RW						RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	ink	Enables ink
29:20	ink_data_b	Ink data for B
19:10	ink_data_g	Ink data for G
9:0	ink_data_r	Ink data for R

140070B8 MDP_WROTOV_IDO_DITHER_05 **VIDO Dithering Control Register 5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	h_active															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		lsb_off	sub_b		sub_g		sub_r		subpix_en	fphase_bit			fphase_sel		fphase_ctrl	
Type		RW	RW		RW		RW		RW	RW			RW		RW	
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	h_active	**Active region of dither IP**
14	lsb_off	**Turns off LSB for dither function**
13:12	sub_b	**Dither SubPixel addend**
11:10	sub_g	**Dither SubPixel addend**
9:8	sub_r	**Dither SubPixel addend**
7	subpix_en	**Enables sub pix dither mode** 0: Pix dither mode 1: Sub pix dither mode
6:4	fphase_bit	**fphase_bit XOR bus number** Note: This function checks reg_fphase_sel. Only 0, 1, 2, 4 and 6 are available. 0: No effect on fphase (XOR disabled)
3:2	fphase_sel	**fphase XOR function: fphase does self bit-wise xor** Note: This function checks reg_fphase_sel. Only bit 2, bit 4 and bit 6 are available. 0: Disable fphase XOR 1: Effect fphase[0]~[1] base on the value of reg_fphase_sel is 1 or 2 2: Effect fphase[0]~[3] base on the value of reg_fphase_sel is 1, 2 or 4 3: Effect fphase[0]~[5] base on the value of reg_fphase_sel is 1, 2, 4 or 6
1:0	fphase_ctrl	**Selects fphase range to add with rdither table** 00: 0~63 01: 0~16 10: 0~3

140070BC MDP_WROTOV_IDO_DITHER_06 **VIDO Dithering Control Register 6** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											debug_mode		new_bit_mode	diff_shift		
Type											RW		RW	RW		
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	test pin_en	rshift_b				rshift_g				rshift_r					table_en	
Type	RW	RW				RW				RW					RW	
Reset	0	0	0	0		0	0	0		0	0	0			0	0

Bit(s)	Name	Description
21:20	debug_mode	1: Enable debugging mode
19	new_bit_mode	1: Enable modified test algorithm
18:16	diff_shift	**Debugging mode difference shift positions**
15	testpin_en	**Enables testpin input**
14:12	rshift_b	**B right shift position after IP output**
10:8	rshift_g	**G right shift position after IP output**
6:4	rshift_r	**R right shift position after IP output**
1:0	table_en	**Active bit of magic table for running order** 01: Phase active in bit3 ~ bit0 10: Phase active in bit1 ~ bit0 Else: Phase active in bit5 ~ bit0

140070C0 MDP_WROTOV IDO_DITHER_07 **VIDO Dithering Control Register 7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		lsb_err_shift_r				ovflw_bit_r				add_lshift_r				input_rshift_r		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
14:12	lsb_err_shift_r	Selects RED LSB error bit
10:8	ovflw_bit_r	Selects RED overflow bit
6:4	add_lshift_r	RED addend left shift bits
2:0	input_rshift_r	RED input right shift bits

140070C4 MDP_WROTOV IDO_DITHER_08 **VIDO Dithering Control Register 8** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		lsb_err_shift_g				ovflw_bit_g				add_lshift_g				input_rshift_g		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
14:12	lsb_err_shift_g	Selects BLUE LSB error bit
10:8	ovflw_bit_g	Selects BLUE overflow bit
6:4	add_lshift_g	BLUE addend left shift bits
2:0	input_rshift_g	BLUE input right shift bits

140070C8 MDP_WROTOV_IDO_DITHER_09 VIDO Dithering Control Register 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		lsb_err_shift_b				ovflw_bit_b				add_lshift_b				input_rshift_b		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
14:12	lsb_err_shift_b	Selects GREEN LSB error bit
10:8	ovflw_bit_b	Selects GREEN overflow bit
6:4	add_lshift_b	GREEN addend left shift bits
2:0	input_rshift_b	GREEN input right shift bits

140070CC MDP_WROTOV_IDO_DITHER_10 VIDO Dithering Control Register 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																crc_rdy
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crc_out															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	crc_rdy	CRC ready
15:0	crc_out	CRC result

140070D0 MDP_WROTOV_IDO_DEBUG VIDO Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	debug_out															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	debug_out															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	debug_out	Debug out

140070D4 MDP_WROTOVIDO_ARB_SW_CTL — **VIDO DMA Arbiter Software Control** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														dma_arb_sw_ctl_sel		dma_arb_sw_ctl_en
Type														RW		RW
Reset														0	0	0

Bit(s)	Name	Description
2:1	dma_arb_sw_ctl_sel	Selects DMA aribiter channel
0	dma_arb_sw_ctl_en	Enables software control DMA arbiter.

140070E0 MDP_WROTOMDP_WROT_TRACK_CTL — **MDP WROT Pre-ultra Track Control** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												proc_track_pre_ultra_mux	proc_track_pause_track	proc_track_ignore_init_latency	proc_track_stop_greq_en	proc_track_pre_ultra_en
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	proc_track_pre_ultra_mux	Selects the pre-ultra signal from fifo or proc_track engine
3	proc_track_pause_track	Pause tracking
2	proc_track_ignore_init_latency	Ignores the initial latency from sof to first pixel
1	proc_track_stop_greq_en	Enables proc_track stop greq function
0	proc_track_pre_ultra_en	Enables proc_track pre-ultra function

140070E4 MDP_WROTOMDP_WROT_TRACK_WINDOW — **MDP WROT Pre-ultra Track Window** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					proc_track_window											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	proc_track_window	Proc_track window

140070E8 MDP_WROT0_MDP_WROT_TRACK_TARGET — MDP WROT Pre-ultra Track Target — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									proc_track_target_cnt							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	proc_track_target_cnt															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	proc_track_target_cnt	Proc_track target count

140070EC MDP_WROT0_MDP_WROT_TRACK_STOP — MDP WROT Pre-ultra Track Stop — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									proc_track_stop_cnt							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	proc_track_stop_cnt															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	proc_track_stop_cnt	Proc_track stop count

140070F0 MDP_WROT0_MDP_WROT_TRACK_PROC_CNT0 — MDP WROTPre-ultra Track Proc Counter 0 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	proc_track_proc_cnt_0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	proc_track_proc_cnt_0															

Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	proc_track_proc_cnt_0	Proc_track processing count low byte

140070F4 MDP_WROTOMDP_WROT_TRACK_PROC_CNT1 MDP WROTPre-ultra Track Proc Counter 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																proc_track_proc_cnt_1
Type																RU
Reset																0

Bit(s)	Name	Description
0	proc_track_proc_cnt_1	Proc_track processing count high byte

14007F00 MDP_WROTOVIDO_BASE_ADDR VIDO Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VIDO_BASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_BASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VIDO_BASE_ADDR	**Double buffer** VIDO base address 1. The definition of this base address depends on the format: 1. One plane format: Base address of plane-1 2. Two plane format: Base address of plane-1

14007F04 MDP_WROTOVIDO_BASE_ADDR_C VIDO Base Address Chroma 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VIDO_BASE_ADDR_C															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_BASE_ADDR_C															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VIDO_BASE_ADDR_C	**Double buffer** VIDO base address 2. The definition of this base address depends on the format: 1. One plane format: Don't care. 2. Two plane format: Base address of plane-2

14007F08 MDP_WROT0VIDO_BASE_ADDR_V VIDO Base Address Chroma 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VIDO_BASE_ADDR_V															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_BASE_ADDR_V															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VIDO_BASE_ADDR_V	**Double buffer** VIDO base address 3. The definition of this base address depends on the format: 1. One plane format, two plane format: Don't care. 2. Three plane format: V plane

Module name: MDP_WROT1 Base address: (+14008000h)

Address	Name	Width	Register Function
14008000	MDP_WROT1VIDO_CTRL	32	VIDO Control
14008004	MDP_WROT1VIDO_DMA_PERF	32	VIDO DMA Performance
14008008	MDP_WROT1VIDO_MAIN_BUF_SIZE	32	VIDO DMA Main Buffer Size
14008010	MDP_WROT1VIDO_SOFT_RST	32	VIDO Software Reset
14008014	MDP_WROT1VIDO_SOFT_RST_STAT	32	VIDO Software Reset Status
14008018	MDP_WROT1VIDO_INT_EN	32	VIDO Interrupt Enable
1400801C	MDP_WROT1VIDO_INT	32	VIDO Interrupt
14008020	MDP_WROT1VIDO_CROP_OFST	32	VIDO Image Cropping Offset
14008024	MDP_WROT1VIDO_TAR_SIZE	32	VIDO Target Image Size

Address	Name	Width	Register Function
1400802C	MDP_WROT1VIDO_OFST_ADDR	32	VIDO Offset Address
14008030	MDP_WROT1VIDO_STRIDE	32	VIDO Stride
14008038	MDP_WROT1VIDO_OFST_ADDR_C	32	VIDO Offset Address Chroma
1400803C	MDP_WROT1VIDO_STRIDE_C	32	VIDO Stride Chroma
14008054	MDP_WROT1VIDO_DITHER	32	VIDO Dithering
14008068	MDP_WROT1VIDO_OFST_ADDR_V	32	VIDO Offset Address Chroma 2
1400806C	MDP_WROT1VIDO_STRIDE_V	32	VIDO Stride Chroma 2
14008070	MDP_WROT1VIDO_RSV_1	32	VIDO Spare Registers
14008074	MDP_WROT1VIDO_DMA_PREULTRA	32	VIDO Pre Ultra Setting
14008078	MDP_WROT1VIDO_IN_SIZE	32	VIDO Input Image Size
1400807C	MDP_WROT1VIDO_ROT_EN	32	VIDO Rotation Enable
14008080	MDP_WROT1VIDO_FIFO_TEST	32	DMA FIFO Test
14008084	MDP_WROT1VIDO_MAT_CTRL	32	VIDO Matrix Control
14008088	MDP_WROT1VIDO_MAT_RMY	32	VIDO Y2R Conversion Parameter R0
1400808C	MDP_WROT1VIDO_MAT_RMV	32	VIDO Y2R Conversion Parameter R1
14008090	MDP_WROT1VIDO_MAT_GMY	32	VIDO Y2R Conversion Parameter G0
14008094	MDP_WROT1VIDO_MAT_BMY	32	VIDO Y2R Conversion Parameter B0
14008098	MDP_WROT1VIDO_MAT_BMV	32	VIDO Y2R Conversion Parameter B1
1400809C	MDP_WROT1VIDO_MAT_PREADD	32	VIDO Y2R Conversion Parameter Extended Add on YUV
140080A0	MDP_WROT1VIDO_MAT_POSTADD	32	VIDO Y2R Conversion Parameter Extended Add on RGB
140080A4	MDP_WROT1VIDO_DITHER_00	32	VIDO Dithering Control Register 0
140080AC	MDP_WROT1VIDO_DITHER_02	32	VIDO Dithering Control Register 2
140080B0	MDP_WROT1VIDO_DITHER_03	32	VIDO Dithering Control Register 3
140080B4	MDP_WROT1VIDO_DITHER_04	32	VIDO Dithering Control Register 4
140080B8	MDP_WROT1VIDO_DITHER_05	32	VIDO Dithering Control Register 5
140080BC	MDP_WROT1VIDO_DITHER_06	32	VIDO Dithering Control Register 6
140080C0	MDP_WROT1VIDO_DITHER_07	32	VIDO Dithering Control Register 7

Address	Name	Width	Register Function
140080C4	MDP_WROT1VIDO_DITHER_08	32	VIDO Dithering Control Register 8
140080C8	MDP_WROT1VIDO_DITHER_09	32	VIDO Dithering Control Register 9
140080CC	MDP_WROT1VIDO_DITHER_10	32	VIDO Dithering Control Register 10
140080D0	MDP_WROT1VIDO_DEBUG	32	VIDO Debug Register
140080D4	MDP_WROT1VIDO_ARB_SW_CTL	32	VIDO DMA Arbiter Software Control
140080E0	MDP_WROT1MDP_WROT_TRACK_CTL	32	MDP WROT Pre-ultra Track Control
140080E4	MDP_WROT1MDP_WROT_TRACK_WINDOW	32	MDP WROT Pre-ultra Track Window
140080E8	MDP_WROT1MDP_WROT_TRACK_TARGET	32	MDP WROT Pre-ultra Track Target
140080EC	MDP_WROT1MDP_WROT_TRACK_STOP	32	MDP WROT Pre-ultra Track Stop
140080F0	MDP_WROT1MDP_WROT_TRACK_PROC_CNT0	32	MDP WROTPre-ultra Track Proc Counter 0
140080F4	MDP_WROT1MDP_WROT_TRACK_PROC_CNT1	32	MDP WROTPre-ultra Track Proc Counter 1
14008F00	MDP_WROT1VIDO_BASE_ADDR	32	VIDO Base Address
14008F04	MDP_WROT1VIDO_BASE_ADDR_C	32	VIDO Base Address Chroma
14008F08	MDP_WROT1VIDO_BASE_ADDR_V	32	VIDO Base Address Chroma 2

14008000 MDP_WROT1VIDO_CTRL **VIDO Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VIDO_UV_YSEL		VIDO_UV_XSEL			VIDO_SOF_RESET_EN		VIDO_FLIP			VIDO_ROTATION					
Type	RW		RW			RW		RW			RW					
Reset	0	0	0	0		0		0			0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		VIDO_PREULTRA_EN	VIDO_PRI_EN	VIDO_CROP_EN				VIDO_UNIFORM_SWAP				VIDO_BLK_OPTION	VIDO_UNIFORM_FORMAT			
Type		RW	RW	RW				RW				RW	RW			
Reset		0	0	0				0				0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
31:30	VIDO_UV_YSEL	**Selects vertical UV** 0: Pick from 0. 0,2,4... 1: Pick from 1. 1,3,5... 2: Pick every pixel
29:28	VIDO_UV_XSEL	**Selects horizontal UV** 0: Pick from 0. 0,2,4... 1: Pick from 1. 1,3,5... 2: Pick every pixel
26	VIDO_SOF_RESET_EN	**Enables SOF reset** 0: No SOF reset 1: Do Soft reset process on receiving SOF
24	VIDO_FLIP	**Enables horizontal flip** Note: The flip action is done after horizontal 0: No flip 1: Flip
21:20	VIDO_ROTATION	**Rotation angle** 0: 0 degree 1: 90 degree 2: 180 degree 3: 270 degree
14	VIDO_PREULTRA_EN	**Enables pre-ultra**
13	VIDO_PRI_EN	**Enables PRI threshold**
12	VIDO_CROP_EN	**Double buffer** VIDO cropping function enabling bit
8	VIDO_UNIFORM_SWAP	
4	VIDO_BLK_OPTION	**Performance improve option** 0: Disable 1: Enable
3:0	VIDO_UNIFORM_FORMAT	

14008004 MDP_WROT1V IDO_DMA_PE RF **VIDO DMA Performance** **3F000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			VIDO_CH2_SMI_GROUP_NUM		VIDO_CH1_SMI_GROUP_NUM		VIDO_CH0_SMI_GROUP_NUM		VIDO_FIFO_PRI_THR							
Type			RW		RW		RW		RW							
Reset			1	1	1	1	1	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_FIFO_PRI_THR				VIDO_FIFO_PRI_LOW_THR											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:28	VIDO_CH2_SMI_GROUP_NUM	**SMI request grouping number** It will launch consecutive SMI requests by this number for this channel. 0: 1 consecutive request 1: 2 consecutive requests 2: 3 consecutive requests 3: 4 consecutive requests
27:26	VIDO_CH1_SMI_GROUP_NUM	**SMI request grouping number** It will launch consecutive SMI requests by this number for this channel.

Bit(s)	Name	Description
		0: 1 consecutive request 1: 2 consecutive requests 2: 3 consecutive requests 3: 4 consecutive requests
25:24	VIDO_CH0_SMI_GROUP_NUM	**SMI request grouping number** It will launch consecutive SMI requests by this number for this channel. 0: 1 consecutive request 1: 2 consecutive requests 2: 3 consecutive requests 3: 4 consecutive requests
23:12	VIDO_FIFO_PRI_THR	**For priority control signal** If the FIFO amount is bigger than THR, the priority control signal will be asserted.
11:0	VIDO_FIFO_PRI_LOW_THR	**PRI low threshold**

14008008 MDP_WROT1V_VIDO_MAIN_BUF_SIZE VIDO DMA Main Buffer Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_MAIN_BLK_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		VIDO_MAIN_BUF_LINE_NUM								VIDO_FILT_TYPE_V				VIDO_FILT_TYPE_H		
Type		RW								RW				RW		
Reset		0	0	0	0	0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
28:16	VIDO_MAIN_BLK_WIDTH	**Width of line block in main working buffer** Unit: Pixel
14:8	VIDO_MAIN_BUF_LINE_NUM	**Line number of main working buffer in FIFO or single buffer mode**
6:4	VIDO_FILT_TYPE_V	**Chroma horizontal down sample filter type** 0: Bypass 1: Forward [1 2 1] filter 2: Backward [1 2 1] filter 3: Forward [1 1] filter 4: Backward [1 1] filter
2:0	VIDO_FILT_TYPE_H	**Chroma horizontal down sample filter type** 0: Bypass 1: Forward [1 2 1] filter 2: Backward [1 2 1] filter 3: Forward [1 1] filter 4: Backward [1 1] filter

14008010 MDP_WROT1V_VIDO_SOFT_RST VIDO Software Reset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VIDO_SOFT_RST
Type																RW
Reset																0

Bit(s)	Name	Description
0	VIDO_SOFT_RST	**VIDO software reset** For software reset is required, write 1 until VIDO_SOFT_RST_STAT = 1 . When VIDO_SOFT_RST_STAT = 1, write 0. Then, polling until VIDO_SOFT_RST_STAT = 0.

14008014 MDP_WROT1VIDO_SOFT_RST_STAT VIDO Software Reset Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VIDO_SOFT_RST_STAT
Type																RU
Reset																0

Bit(s)	Name	Description
0	VIDO_SOFT_RST_STAT	**VIDO software reset status** This status will be 1 when soft reset is active, and be 0 when soft reset is completed.

14008018 MDP_WROT1VIDO_INT_EN VIDO Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			VIDO_CSR_DEBUG											VIDO_INT_WC_3_EN	VIDO_INT_WC_2_EN	VIDO_INT_1_EN
Type			RW											RW	RW	RW
Reset			0	0	0	0	0	0						0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
13:8	VIDO_CSR_DEBUG	**Controls VIDO debugging register**
2	VIDO_INT_WC_3_EN	**Enables VIDO rotate finish status clear**
1	VIDO_INT_WC_2_EN	**Controls VIDO frame done status**
0	VIDO_INT_1_EN	**Enables VIDO interrupt 1** Interrupt situation: Crop setting is not correct.

1400801C MDP_WROT1V IDO_INT VIDO Interrupt 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														VIDO_INT_3	VIDO_INT_2	VIDO_INT_1
Type														A0	A0	A0
Reset														1	1	1

Bit(s)	Name	Description
2	VIDO_INT_3	**VIDO status** Situation: Luma rotation done. Turn on VIDO_INT_WC_3_EN and write 1 to clear.
1	VIDO_INT_2	**VIDO status** Situation: Frame done = 0. INT turns on VIDO_INT_WC_2_EN and write 1 to clear
0	VIDO_INT_1	**VIDO interrupt 1** Interrupt situation: Crop setting is not correct Turn on VIDO_INT_WC_EN and write 1 to clear.

14008020 MDP_WROT1V IDO_CROP_OFST VIDO Image Cropping Offset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_CROP_OFST_Y												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_CROP_OFST_X												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	VIDO_CROP_OFST_Y	**Double buffer** Y channel offset position for cropping. If VIDO_FORMAT is YUV422 or YUV422V, y channel width must be multiple of 2.
12:0	VIDO_CROP_OFST_X	**Double buffer** Y channel offset position for cropping. If VIDO_FORMAT is YUV422 or YUV422V, y channel width must be multiple of 2.

14008024 MDP_WROT1V_VIDO_TAR_SIZE VIDO Target Image Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_YSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_XSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	VIDO_YSIZE	**Double buffer** Y channel height of target image
12:0	VIDO_XSIZE	**Double buffer** Y channel width of Target image If VIDO_FORMAT is YUV422 or YUV422V, y channel width must be multiple of 2.

1400802C MDP_WROT1V_VIDO_OFST_ADDR VIDO Offset Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VIDO_OFST_ADDR											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_OFST_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:0	VIDO_OFST_ADDR	**Double buffer** VIDO offset address 1. It follows the definition of Base Address 1.

14008030 MDP_WROT1V_VIDO_STRIDE VIDO Stride 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_STRIDE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	VIDO_STRIDE	**Double buffer** VIDO stride 1. It follows the definition of Base Address 2.

14008038 MDP_WROT1V IDO_OFST_ADDR_C VIDO Offset Address Chroma 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VIDO_OFST_ADDR_C											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_OFST_ADDR_C															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:0	VIDO_OFST_ADDR_C	**Double buffer** VIDO offset address 2. It follows the definition of Base Address 2.

1400803C MDP_WROT1V IDO_STRIDE_C VIDO Stride Chroma 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_STRIDE_C															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	VIDO_STRIDE_C	**Double buffer** VIDO stride 2. It follows the definition of Base Address 2.

14008054 MDP_WROT1V IDO_DITHER VIDO Dithering 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VIDO _XRG B_DU MMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VIDO_DIT_EN
Type																RW
Reset																0

Bit(s)	Name	Description
31:24	VIDO_XRGB_DUMMY	XRGB format 8-bit dummy data
0	VIDO_DIT_EN	Enables VIDO dithering

14008068 MDP_WROT1V_VIDO_OFST_ADDR_V VIDO Offset Address Chroma 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VIDO_OFST_ADDR_V											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_OFST_ADDR_V															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:0	VIDO_OFST_ADDR_V	**Double buffer** VIDO offset address 3. It follows the definition of Base Address 3.

1400806C MDP_WROT1V_VIDO_STRIDE_V VIDO Stride Chroma 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_STRIDE_V															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	VIDO_STRIDE_V	**Double buffer** VIDO stride 3. It follows the definition of Base Address 3.

14008070 MDP_WROT1V_VIDO_RSV_1 VIDO Spare Registers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VIDO_RSV_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_RSV_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VIDO_RSV_1	VIDO spare registers

14008074 MDP_WROT1V_VIDO_DMA_PREULTRA VIDO Pre Ultra Setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name									VIDO_FIFO_PREULTRA_THR							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_FIFO_PREULTRA_THR				VIDO_FIFO_PREULTRA_THR_LOW											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:12	VIDO_FIFO_PREULTRA_THR	Pre-ultra high threshold
11:0	VIDO_FIFO_PREULTRA_THR_LOW	Pre-ultra low threshold

14008078 MDP_WROT1VIDO_IN_SIZE VIDO Input Image Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_IN_YSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_IN_XSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	VIDO_IN_YSIZE	**Double buffer** Y channel height of input image
12:0	VIDO_IN_XSIZE	**Double buffer** Y channel width of Input image If VIDO_FORMAT is YUV422 or YUV422V, y channel width must be multiple of 2.

1400807C MDP_WROT1VIDO_ROT_EN VIDO Rotation Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VIDO_ROT_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	VIDO_ROT_EN	Enables rotation

14008080 MDP_WROT1V_VIDO_FIFO_TEST **DMA FIFO Test** **00000080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					VIDO_FIFO_SIZE											
Type					RW											
Reset					0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	VIDO_FIFO_SIZE	ROT FIFO size

14008084 MDP_WROT1V_VIDO_MAT_CTRL **VIDO Matrix Control** **00000040**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									VIDO_MTX_SEL						VIDO_EXT_MTX_EN	VIDO_MAT_EN
Type									RW						RW	RW
Reset									0	1	0	0			0	0

Bit(s)	Name	Description
7:4	VIDO_MTX_SEL	**Double buffer** Selects color matrix format Default: 601 to 709 0: RGB to JPEG 2: RGB to 601 3: RGB to 709 4: JPEG to RGB 6: 601 to RGB 7: 709 to RGB 8: JPEG to 601 9: JPEG to 709 10: 601 to JPEG 11: 709 to JPEG 12: 709 to 601
1	VIDO_EXT_MTX_EN	**Double buffer** Selects color matrix auto mode 0: Use auto mode 1: Use programmable coeff
0	VIDO_MAT_EN	**Double buffer** Enables matrix 0: Bypass 1: Enable

14008088 MDP_WROT1V_IDO_MAT_RM_Y **VIDO Y2R Conversion Parameter R0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_RMU												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_RMY												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	VIDO_RMU	VIDO YUV2RGB program parameter for R color of U component
12:0	VIDO_RMY	VIDO YUV2RGB program parameter for R color of Y component

1400808C MDP_WROT1V_IDO_MAT_RM_V **VIDO Y2R Conversion Parameter R1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_GMY												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_RMV												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	VIDO_GMY	VIDO YUV2RGB program parameter for G color of Y component
12:0	VIDO_RMV	VIDO YUV2RGB program parameter for R color of V component

14008090 MDP_WROT1V_IDO_MAT_GM_Y **VIDO Y2R Conversion Parameter G0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_GMV												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_GMU												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	VIDO_GMV	VIDO YUV2RGB program parameter for G color of V component
12:0	VIDO_GMU	VIDO YUV2RGB program parameter for G color of U component

14008094 MDP_WROT1V_IDO_MAT_BM Y — VIDO Y2R Conversion Parameter B0 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_BMU												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_BMY												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	VIDO_BMU	VIDO YUV2RGB program parameter for B color of U component
12:0	VIDO_BMY	VIDO YUV2RGB program parameter for B color of Y component

14008098 MDP_WROT1V_IDO_MAT_BM V — VIDO Y2R Conversion Parameter B1 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VIDO_BMV												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	VIDO_BMV	VIDO YUV2RGB program parameter for B color of V component

1400809C MDP_WROT1V_IDO_MAT_PR EADD — VIDO Y2R Conversion Parameter Extended Add on YUV — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_VA										VIDO_UA		
Type				RW										RW		
Reset				0	0	0	0	0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_UA							VIDO_YA								
Type	RW							RW								
Reset	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:20	VIDO_VA	VIDO YUV2RGB program parameter for V to add extended offset
18:10	VIDO_UA	VIDO YUV2RGB program parameter for U to add extended offset
8:0	VIDO_YA	VIDO YUV2RGB program parameter for Y to add extended offset

140080A0 MDP_WROT1V_VIDO_MAT_PO STADD — **VIDO Y2R Conversion Parameter Extended Add on RGB** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VIDO_BA										VIDO_GA		
Type				RW										RW		
Reset				0	0	0	0	0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_GA							VIDO_RA								
Type	RW							RW								
Reset	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:20	VIDO_BA	VIDO YUV2RGB program parameter for B to add extended offset
18:10	VIDO_GA	VIDO YUV2RGB program parameter for G to add extended offset
8:0	VIDO_RA	VIDO YUV2RGB program parameter for R to add extended offset

140080A4 MDP_WROT1V_VIDO_DITHER_00 — **VIDO Dithering Control Register 0** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	frame_done_del										crc_clr	crc_start	crc_cen	wrap_mode	out_sel	start
Type	RW										RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
15:8	frame_done_del	**Frame done return delay**
5	crc_clr	**Write 1 to clear CRC result.**
4	crc_start	**Write 1 to start CRC counting.**
3	crc_cen	0: Turn off CRC engine CG 1: Turn on CRC engine CG
2	wrap_mode	**Enables rounding for dithering function** When the rounding method is used, both running order and error dispersion cannot be used.
1	out_sel	0: Bypass dither 1: Through dither
0	start	0: No dither 1: Start dither engine

140080AC MDP_WROT1V_VIDO_DITHER_02 — **VIDO Dithering Control Register 2** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	w_demo															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name			round_en	rdither_en	lfsr_en	edither_en	left_en		fphase_r	fphase_en	fphase					
Type			RW	RW	RW	RW	RW		RW	RW	RW					
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	w_demo	**Short line length**
13	round_en	**Enables rounding for dithering function** When the rounding method is used, both running order and error dispersion cannot be used.
12	rdither_en	**Enables running order dithering** The running order dithering must be set when ROUND_EN is set to 0. The running order dithering can run with error dispersion when EDOTHER_EN is set to 1.
11	lfsr_en	**Enables LFSR-type dithering**
10	edither_en	**Enables error dispersion dithering** The error dispersion dithering must be set when ROUND_EN is set to 0. The running order dithering can run with error dispersion when RDITHER_EN is set to 1.
9:8	left_en	**Enables left part of screen dither** 0: Dither runs at full screen. 1: Dither runs at left part of screen.
7	fphase_r	**Dither SubPixel addend**
6	fphase_en	**Running order dithering frame** Enables phase control
5:0	fphase	**Running order dithering frame phase increment** *Note:* *If ROUND_EN = 1, the output will be rounding only (no matter what RDITHER_EN and EDITHER_EN setting are).* *RDITHER_EN and EDITHER_EN can work together.*

140080B0 MDP_WROT1V IDO_DITHER_03 **VIDO Dithering Control Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											drmod_b		drmod_g		drmod_r	
Type											RW		RW		RW	
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:4	drmod_b	**Selects dither mode** 0: No dither 1: 12-bit dither to 10-bit 2: 12-bit dither to 8-bit 3: 12-bit dither to 6-bit
3:2	drmod_g	**Selects dither mode** 0: No dither 1: 12-bit dither to 10-bit 2: 12-bit dither to 8-bit 3: 12-bit dither to 6-bit

Bit(s)	Name	Description
1:0	drmod_r	**Selects dither mode** 0: No dither 1: 12-bit dither to 10-bit 2: 12-bit dither to 8-bit 3: 12-bit dither to 6-bit

140080B4 MDP_WROT1V_VIDO_DITHER_04 **VIDO Dithering Control Register 4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ink		ink_data_b										ink_data_g			
Type	RW		RW										RW			
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ink_data_g						ink_data_r									
Type	RW						RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	ink	Enables ink
29:20	ink_data_b	Ink data for B
19:10	ink_data_g	Ink data for G
9:0	ink_data_r	Ink data for R

140080B8 MDP_WROT1V_VIDO_DITHER_05 **VIDO Dithering Control Register 5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	h_active															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		lsb_off	sub_b		sub_g		sub_r		subpix_en	fphase_bit			fphase_sel		fphase_ctrl	
Type		RW	RW		RW		RW		RW	RW			RW		RW	
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	h_active	**Active region of dither IP**
14	lsb_off	**Turns off LSB for dither function**
13:12	sub_b	**Dither SubPixel addend**
11:10	sub_g	**Dither SubPixel addend**
9:8	sub_r	**Dither SubPixel addend**
7	subpix_en	**Enables sub pix dither mode** 0: Pix dither mode 1: Sub pix dither mode
6:4	fphase_bit	**fphase_bit XOR bus number** Note: This function checks reg_fphase_sel. Only 0, 1, 2, 4 and 6 are available. 0: No effect on fphase (XOR disabled)
3:2	fphase_sel	**fphase XOR function: fphase does self bit-wise xor** Note: This function checks reg_fphase_sel. Only bit 2, bit 4 and bit 6 are available.

Bit(s)	Name	Description
		0: Disable fphase XOR 1: Effect fphase[0]~[1] base on the value of reg_fphase_sel is 1 or 2 2: Effect fphase[0]~[3] base on the value of reg_fphase_sel is 1, 2 or 4 3: Effect fphase[0]~[5] base on the value of reg_fphase_sel is 1, 2, 4 or 6
1:0	fphase_ctrl	**Selects fphase range to add with rdither table** 00: 0~63 01: 0~16 10: 0~3

140080BC MDP_WROT1V_VIDO_DITHER_06 **VIDO Dithering Control Register 6** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											debug_mode		new_bit_mode	diff_shift		
Type											RW		RW	RW		
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	testpin_en	rshift_b				rshift_g				rshift_r					table_en	
Type	RW	RW				RW				RW					RW	
Reset	0	0	0	0		0	0	0		0	0	0			0	0

Bit(s)	Name	Description
21:20	debug_mode	1: Enable debugging mode
19	new_bit_mode	1: Enable modified test algorithm
18:16	diff_shift	**Debugging mode difference shift positions**
15	testpin_en	**Enables testpin input**
14:12	rshift_b	**B right shift position after IP output**
10:8	rshift_g	**G right shift position after IP output**
6:4	rshift_r	**R right shift position after IP output**
1:0	table_en	**Active bit of magic table for running order** 01: Phase active in bit3 ~ bit0 10: Phase active in bit1 ~ bit0 Else: Phase active in bit5 ~ bit0

140080C0 MDP_WROT1V_VIDO_DITHER_07 **VIDO Dithering Control Register 7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		lsb_err_shift_r				ovflw_bit_r				add_lshift_r				input_rshift_r		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
14:12	lsb_err_shift_r	Selects RED LSB error bit
10:8	ovflw_bit_r	Selects RED overflow bit
6:4	add_lshift_r	RED addend left shift bits
2:0	input_rshift_r	RED input right shift bits

140080C4 MDP_WROT1V_VIDO_DITHER_08 **VIDO Dithering Control Register 8** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		lsb_err_shift_g				ovflw_bit_g				add_lshift_g				input_rshift_g		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
14:12	lsb_err_shift_g	Selects BLUE LSB error bit
10:8	ovflw_bit_g	Selects BLUE overflow bit
6:4	add_lshift_g	BLUE addend left shift bits
2:0	input_rshift_g	BLUE input right shift bits

140080C8 MDP_WROT1V_VIDO_DITHER_09 **VIDO Dithering Control Register 9** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		lsb_err_shift_b				ovflw_bit_b				add_lshift_b				input_rshift_b		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
14:12	lsb_err_shift_b	Selects GREEN LSB error bit
10:8	ovflw_bit_b	Selects GREEN overflow bit
6:4	add_lshift_b	GREEN addend left shift bits
2:0	input_rshift_b	GREEN input right shift bits

140080CC MDP_WROT1V_VIDO_DITHER_10 **VIDO Dithering Control Register 10** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																crc_rdy
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	crc_out															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	crc_rdy	CRC ready
15:0	crc_out	CRC result

140080D0 MDP_WROT1VIDO_DEBUG VIDO Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	debug_out															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	debug_out															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	debug_out	Debug out

140080D4 MDP_WROT1VIDO_ARB_SW_CTL VIDO DMA Arbiter Software Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														dma_arb_sw_ctl_sel		dma_arb_sw_ctl_en
Type														RW		RW
Reset														0	0	0

Bit(s)	Name	Description
2:1	dma_arb_sw_ctl_sel	Selects DMA aribiter channel
0	dma_arb_sw_ctl_en	Enables software control DMA arbiter.

140080E0 MDP_WROT1MDP_WROT_TRACK_CTL MDP WROT Pre-ultra Track Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												proc	proc	proc	proc	proc

												_track_pre_ultra_mux	_track_pause_track	_track_ignore_init_latency	_track_stop_greq_en	_track_pre_ultra_en
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	proc_track_pre_ultra_mux	Selects the pre-ultra signal from fifo or proc_track engine
3	proc_track_pause_track	Pause tracking
2	proc_track_ignore_init_latency	Ignores the initial latency from sof to first pixel
1	proc_track_stop_greq_en	Enables proc_track stop greq function
0	proc_track_pre_ultra_en	Enables proc_track pre-ultra function

140080E4 MDP_WROT1MDP_WROT_TRACK_WINDOW — MDP WROT Pre-ultra Track Window — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					proc_track_window											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	proc_track_window	Proc_track window

140080E8 MDP_WROT1MDP_WROT_TRACK_TARGET — MDP WROT Pre-ultra Track Target — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									proc_track_target_cnt							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	proc_track_target_cnt															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	proc_track_target_cnt	**Proc_track target count**

140080EC MDP_WROT1M — MDP WROT Pre-ultra Track — 00000000

DP_WROT_TRACK_STOP **Stop**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									proc_track_stop_cnt							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	proc_track_stop_cnt															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	proc_track_stop_cnt	Proc_track stop count

140080F0 MDP_WROT1MDP_WROT_TRACK_PROC_CNT0 **MDP WROTPre-ultra Track Proc Counter 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	proc_track_proc_cnt_0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	proc_track_proc_cnt_0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	proc_track_proc_cnt_0	Proc_track processing count low byte

140080F4 MDP_WROT1MDP_WROT_TRACK_PROC_CNT1 **MDP WROTPre-ultra Track Proc Counter 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																proc_track_proc_cnt_1
Type																RU
Reset																0

Bit(s)	Name	Description
0	proc_track_proc_cnt_1	Proc_track processing count high byte

14008F00 MDP_WROT1V_VIDO_BASE_ADDR VIDO Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VIDO_BASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_BASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VIDO_BASE_ADDR	**Double buffer** VIDO base address 1. The definition of this base address depends on the format: 1. One plane format: Base address of plane-1 2. Two plane format: Base address of plane-1

14008F04 MDP_WROT1V_VIDO_BASE_ADDR_C VIDO Base Address Chroma 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VIDO_BASE_ADDR_C															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_BASE_ADDR_C															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VIDO_BASE_ADDR_C	**Double buffer** VIDO base address 2. The definition of this base address depends on the format: 1. One plane format: Don't care. 2. Two plane format: Base address of plane-2

14008F08 MDP_WROT1V_VIDO_BASE_ADDR_V VIDO Base Address Chroma 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VIDO_BASE_ADDR_V															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VIDO_BASE_ADDR_V															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VIDO_BASE_ADDR_V	**Double buffer** VIDO base address 3. The definition of this base address depends

Bit(s)	Name	Description
		on the format: 1. One plane format, two plane format: Don't care. 2. Three plane format: V plane

Module name: MDP_TDSHP Base address: (+14009000h)

Address	Name	Width	Register Function
14009000	MDP_TDSHP_00	32	MDP_TDSHP_00
14009004	MDP_TDSHP_01	32	MDP_TDSHP_01
14009008	MDP_TDSHP_02	32	MDP_TDSHP_02
1400900C	MDP_TDSHP_03	32	MDP_TDSHP_03
14009014	MDP_TDSHP_05	32	MDP_TDSHP_05
14009018	MDP_TDSHP_06	32	MDP_TDSHP_06
1400901C	MDP_TDSHP_07	32	MDP_TDSHP_07
14009020	MDP_TDSHP_08	32	MDP_TDSHP_08
14009024	MDP_TDSHP_09	32	MDP_TDSHP_09
14009040	MDP_PBC_00	32	MDP_PBC_00
14009044	MDP_PBC_01	32	MDP_PBC_01
14009048	MDP_PBC_02	32	MDP_PBC_02
1400904C	MDP_PBC_03	32	MDP_PBC_03
14009050	MDP_PBC_04	32	MDP_PBC_04
14009054	MDP_PBC_05	32	MDP_PBC_05
14009058	MDP_PBC_06	32	MDP_PBC_06
1400905C	MDP_PBC_07	32	MDP_PBC_07
14009060	MDP_PBC_08	32	MDP_PBC_08
14009064	MDP_HIST_CFG_00	32	MDP_HIST_CFG_00
14009068	MDP_HIST_CFG_01	32	MDP_HIST_CFG_01
1400906C	MDP_LUMA_HIST_00	32	Result of Luma Histogram 0
14009070	MDP_LUMA_HIST_01	32	Result of Luma Histogram 1
14009074	MDP_LUMA_HIST_02	32	Result of Luma Histogram 2
14009078	MDP_LUMA_HIST_03	32	Result of Luma Histogram 3
1400907C	MDP_LUMA_HIST_04	32	Result of Luma Histogram 4
14009080	MDP_LUMA_HIST_05	32	Result of Luma Histogram 5
14009084	MDP_LUMA_HIST_06	32	Result of Luma Histogram 6
1400908C	MDP_LUMA_HIST_07	32	Result of Luma Histogram 7
14009090	MDP_LUMA_HIST_08	32	Result of Luma Histogram 8
14009094	MDP_LUMA_HIST_09	32	Result of Luma Histogram 9
14009098	MDP_LUMA_HIST_10	32	Result of Luma Histogram 10
1400909C	MDP_LUMA_HIST_	32	Result of Luma Histogram 11

Address	Name	Width	Register Function
	11		
140090A0	MDP_LUMA_HIST_12	32	Result of Luma Histogram 12
140090A4	MDP_LUMA_HIST_13	32	Result of Luma Histogram 13
140090A8	MDP_LUMA_HIST_14	32	Result of Luma Histogram 14
140090AC	MDP_LUMA_HIST_15	32	Result of Luma Histogram 15
140090B0	MDP_LUMA_HIST_16	32	Result of Luma Histogram 16
140090B4	MDP_LUMA_SUM	32	Result of luma sum
140090BC	MDP_Y_FTN_1_0_MAIN	32	2nd Y Transfer Function 1, 0
140090C0	MDP_Y_FTN_3_2_MAIN	32	2nd Y Transfer Function 3, 2
140090C4	MDP_Y_FTN_5_4_MAIN	32	2nd Y Transfer Function 5, 4
140090C8	MDP_Y_FTN_7_6_MAIN	32	2nd Y Transfer Function 7, 6
140090CC	MDP_Y_FTN_9_8_MAIN	32	2nd Y Transfer Function 9, 8
140090D0	MDP_Y_FTN_11_10_MAIN	32	2nd Y Transfer Function 11, 10
140090D4	MDP_Y_FTN_13_12_MAIN	32	2nd Y Transfer Function 13, 12
140090D8	MDP_Y_FTN_15_14_MAIN	32	2nd Y Transfer Function 15, 14
140090DC	MDP_Y_FTN_17_16_MAIN	32	2nd Y Transfer Function 17, 16
140090E0	MDP_C_BOOST_MAIN	32	Chroma Boost
140090E4	MDP_C_BOOST_MAIN_2	32	Chroma Boost 2
140090E8	MDP_TDSHP_C_BOOST_MAIN	32	TDSHP Chroma Boost
140090EC	MDP_TDSHP_C_BOOST_MAIN_2	32	TDSHP Chroma Boost 2
140090FC	MDP_TDSHP_ATPG	32	MDP_TDSHP_ATPG
14009100	MDP_TDSHP_CTRL	32	MDP_TDSHP_CTRL
14009104	MDP_TDSHP_INTEN	32	MDP_TDSHP_INTEN
14009108	MDP_TDSHP_INTSTA	32	MDP_TDSHP_INTSTA
1400910C	MDP_TDSHP_STATUS	32	MDP_TDSHP_STATUS
14009110	MDP_TDSHP_CFG	32	MDP_TDSHP_CFG
14009114	MDP_TDSHP_INPUT_COUNT	32	MDP_TDSHP_INPUT_COUNT
14009118	MDP_TDSHP_CHKSUM	32	Input or Output Data Checksum
1400911C	MDP_TDSHP_OUTPUT_COUNT	32	MDP_TDSHP_OUTPUT_COUNT
14009120	MDP_TDSHP_INPUT_SIZE	32	MDP_TDSHP_INPUT_SIZE

Address	Name	Width	Register Function
14009124	MDP_TDSHP_OUTPUT_OFFSET	32	MDP_TDSHP_OUTPUT_OFFSET
14009128	MDP_TDSHP_OUTPUT_SIZE	32	MDP_TDSHP_OUTPUT_SIZE
1400912C	MDP_TDSHP_BLANK_WIDTH	32	MDP_TDSHP_BLANK_WIDTH
14009130	MDP_TDSHP_DEMO_HMASK	32	MDP_TDSHP_DEMO_HMASK
14009134	MDP_TDSHP_DEMO_VMASK	32	MDP_TDSHP_DEMO_VMASK
1400914C	MDP_TDSHP_DUMMY_REG	32	MDP_TDSHP_DUMMY_REG
14009200	MDP_LUMA_HIST_INIT_00	32	MDP_LUMA_HIST_INIT_00
14009204	MDP_LUMA_HIST_INIT_01	32	MDP_LUMA_HIST_INIT_01
14009208	MDP_LUMA_HIST_INIT_02	32	MDP_LUMA_HIST_INIT_02
1400920C	MDP_LUMA_HIST_INIT_03	32	MDP_LUMA_HIST_INIT_03
14009210	MDP_LUMA_HIST_INIT_04	32	MDP_LUMA_HIST_INIT_04
14009214	MDP_LUMA_HIST_INIT_05	32	MDP_LUMA_HIST_INIT_05
14009218	MDP_LUMA_HIST_INIT_06	32	MDP_LUMA_HIST_INIT_06
1400921C	MDP_LUMA_HIST_INIT_07	32	MDP_LUMA_HIST_INIT_07
14009220	MDP_LUMA_HIST_INIT_08	32	MDP_LUMA_HIST_INIT_08
14009224	MDP_LUMA_HIST_INIT_09	32	MDP_LUMA_HIST_INIT_09
14009228	MDP_LUMA_HIST_INIT_10	32	MDP_LUMA_HIST_INIT_10
1400922C	MDP_LUMA_HIST_INIT_11	32	MDP_LUMA_HIST_INIT_11
14009230	MDP_LUMA_HIST_INIT_12	32	MDP_LUMA_HIST_INIT_12
14009234	MDP_LUMA_HIST_INIT_13	32	MDP_LUMA_HIST_INIT_13
14009238	MDP_LUMA_HIST_INIT_14	32	MDP_LUMA_HIST_INIT_14
1400923C	MDP_LUMA_HIST_INIT_15	32	MDP_LUMA_HIST_INIT_15
14009240	MDP_LUMA_HIST_INIT_16	32	MDP_LUMA_HIST_INIT_16
14009244	MDP_LUMA_SUM_INIT	32	MDP_LUMA_SUM_INIT
14009250	MDP_DC_DBG_CFG_MAIN	32	MDP_DC_DBG_CFG_MAIN
14009254	MDP_DC_WIN_X_MAIN	32	MDP_DC_WIN_X_MAIN
14009258	MDP_DC_WIN_Y_MAIN	32	MDP_DC_WIN_Y_MAIN

Address	Name	Width	Register Function
1400925C	MDP_DC_TWO_D_W1	32	MDP_DC_TWO_D_W1
14009260	MDP_DC_TWO_D_W1_RESULT_INIT	32	MDP_DC_TWO_D_W1_RESULT_INIT
14009264	MDP_DC_TWO_D_W1_RESULT	32	MDP_DC_TWO_D_W1_RESULT
14009300	MDP_EDF_GAIN_00	32	MDP_EDF_GAIN_00
14009304	MDP_EDF_GAIN_01	32	MDP_EDF_GAIN_01
14009308	MDP_EDF_GAIN_02	32	MDP_EDF_GAIN_02
1400930C	MDP_EDF_GAIN_03	32	MDP_EDF_GAIN_03
14009310	MDP_EDF_GAIN_04	32	MDP_EDF_GAIN_04
14009314	MDP_EDF_GAIN_05	32	MDP_EDF_GAIN_05
14009320	MDP_TDSHP_10	32	MDP_TDSHP_10
14009324	MDP_TDSHP_11	32	MDP_TDSHP_11
14009328	MDP_TDSHP_12	32	MDP_TDSHP_12
1400932C	MDP_TDSHP_13	32	MDP_TDSHP_13
14009330	PAT1_GEN_SET	32	Configuration
14009334	PAT1_GEN_FRM_SIZE	32	Configuration
14009338	PAT1_GEN_COLOR0	32	Configuration
1400933C	PAT1_GEN_COLOR1	32	Configuration
14009340	PAT1_GEN_COLOR2	32	Configuration
14009344	PAT1_GEN_POS	32	Configuration
14009354	PAT1_GEN_TILE_POS	32	Configuration
14009358	PAT1_GEN_TILE_OV	32	Configuration
14009360	PAT2_GEN_SET	32	Configuration
14009368	PAT2_GEN_COLOR0	32	Configuration
1400936C	PAT2_GEN_COLOR1	32	Configuration
14009374	PAT2_GEN_POS	32	Configuration
14009378	PAT2_GEN_CURSOR_RB0	32	Readback
1400937C	PAT2_GEN_CURSOR_RB1	32	Readback
14009384	PAT2_GEN_TILE_POS	32	Configuration
14009388	PAT2_GEN_TILE_OV	32	Configuration

14009000 MDP_TDSHP_00 MDP_TDSHP_00 00102010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDS_EN	TDS_BYPASS_MID	TDS_BYPASS_HIGH	TDS_ADAP_LUMA_BP		TDS_INK_SEL			TDS_GAIN_MID							
Type	RW	RW	RW	RW		RW			RW							
Reset	0	0	0	0		0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDS_GAIN_HIGH								TDS_COR_GAIN							

Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31	TDS_EN	**Enables 2D sharpness**
30	TDS_BYPASS_MID	**Bypasses middle band**
29	TDS_BYPASS_HIGH	**Bypasses high band**
28	TDS_ADAP_LUMA_BP	**Adaptive luma bypass** 0: Normal function 1: Bypass
26:24	TDS_INK_SEL	**Selects ink mode** 2'd0: Disable ink mode 2'd1: Ink mode of difference at final output 2'd2: PBC coverage ink 2'd3: PBC strength ink
23:16	TDS_GAIN_MID	**Mid-band gain before merge**
15:8	TDS_GAIN_HIGH	**High-band gain before merge**
7:0	TDS_COR_GAIN	**Final AC soft coring gain** TDS_GAIN*((TDS_COR_RATIO + 8) >> 4)

14009004 MDP_TDSHP_01 MDP_TDSHP_01 04020208

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDS_COR_THR								TDS_COR_ZERO							
Type	RW								RW							
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TDS_GAIN								TDS_LIMIT_RATIO			
Type					RW								RW			
Reset					0	0	1	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:24	TDS_COR_THR	**Final AC coring threshold**
23:16	TDS_COR_ZERO	**Final AC zero threshold**
11:4	TDS_GAIN	**Final AC gain** Gain = reg/0x20
3:0	TDS_LIMIT_RATIO	**Final AC soft limit ratio**

14009008 MDP_TDSHP_02 MDP_TDSHP_02 18300300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDS_LIMIT								TDS_BOUND							
Type	RW								RW							
Reset	0	0	0	1	1	0	0	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDS_COR_VALUE															
Type	RW															
Reset	0	0	0	0	0	0	1	1								

Bit(s)	Name	Description
31:24	TDS_LIMIT	**Final AC positive limit**

Bit(s)	Name	Description
23:16	TDS_BOUND	**Final AC postive bound**
15:8	TDS_COR_VALUE	**Final AC coring value** TDS_COR_ZERO + ((TDS_COR_THR - TDS_COR_ZERO)*(16 - TDS_COR_RATIO) + 8) >> 4

1400900C MDP_TDSHP_03 **MDP_TDSHP_03** **8802080A**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDS_CLIP_EN			TDS_ CLIP _RAT IO					TDS_CLIP_THR							
Type	RW			RW					RW							
Reset	1			0	1	0	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TDS_AC_LPF_COE						TDS_SAT_PROC					
Type					RW						RW					
Reset					1	0	0	0			0	0	1	0	1	0

Bit(s)	Name	Description
31	TDS_CLIP_EN	**Enables final AC clip**
28:24	TDS_CLIP_RATIO	**Final AC clip ratio**
23:16	TDS_CLIP_THR	**Final AC clip positive threshold**
11:8	TDS_AC_LPF_COE	**0: Disable** 1~15: As old design
5:0	TDS_SAT_PROC	**Saturation process strength** Max. value: 32

14009014 MDP_TDSHP_05 **MDP_TDSHP_05** **00183048**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDS_YLEV_P000								TDS_YLEV_P016							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDS_YLEV_P032								TDS_YLEV_P048							
Type	RW								RW							
Reset	0	0	1	1	0	0	0	0	0	1	0	0	1	0	0	0

Bit(s)	Name	Description
31:24	TDS_YLEV_P000	**Y level dependent sharpness point 0** Gain = reg/0x80
23:16	TDS_YLEV_P016	**Y level dependent sharpness point 64** Gain = reg/0x80
15:8	TDS_YLEV_P032	**Y level dependent sharpness point 128** Gain = reg/0x80
7:0	TDS_YLEV_P048	**Y level dependent sharpness point 192** Gain = reg/0x80

14009018 MDP_TDSHP_ **MDP_TDSHP_06** **60687078**

06

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDS_YLEV_P064								TDS_YLEV_P080							
Type	RW								RW							
Reset	0	1	1	0	0	0	0	0	0	1	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDS_YLEV_P096								TDS_YLEV_P112							
Type	RW								RW							
Reset	0	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0

Bit(s)	Name	Description
31:24	TDS_YLEV_P064	**Y level dependent sharpness point 256** Gain = reg/0x80
23:16	TDS_YLEV_P080	**Y level dependent sharpness point 320** Gain = reg/0x80
15:8	TDS_YLEV_P096	**Y level dependent sharpness point 384** Gain = reg/0x80
7:0	TDS_YLEV_P112	**Y level dependent sharpness point 448** Gain = reg/0x80

1400901C MDP_TDSHP_07 MDP_TDSHP_07 807B7670

07

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDS_YLEV_P128								TDS_YLEV_P144							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDS_YLEV_P160								TDS_YLEV_P176							
Type	RW								RW							
Reset	0	1	1	1	0	1	1	0	0	1	1	1	0	0	0	0

Bit(s)	Name	Description
31:24	TDS_YLEV_P128	**Y level dependent sharpness point 512** Gain = reg/0x80
23:16	TDS_YLEV_P144	**Y level dependent sharpness point 576** Gain = reg/0x80
15:8	TDS_YLEV_P160	**Y level dependent sharpness point 640** Gain = reg/0x80
7:0	TDS_YLEV_P176	**Y level dependent sharpness point 704** Gain = reg/0x80

14009020 MDP_TDSHP_08 MDP_TDSHP_08 6B66605B

08

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDS_YLEV_P192								TDS_YLEV_P208							
Type	RW								RW							
Reset	0	1	1	0	1	0	1	1	0	1	1	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDS_YLEV_P224								TDS_YLEV_P240							
Type	RW								RW							
Reset	0	1	1	0	0	0	0	0	0	1	0	1	1	0	1	1

Bit(s)	Name	Description
31:24	TDS_YLEV_P192	**Y level dependent sharpness point 768** Gain = reg/0x80
23:16	TDS_YLEV_P208	**Y level dependent sharpness point 832** Gain = reg/0x80
15:8	TDS_YLEV_P224	**Y level dependent sharpness point 896** Gain = reg/0x80
7:0	TDS_YLEV_P240	**Y level dependent sharpness point 960** Gain = reg/0x80

14009024 MDP_TDSHP_09 MDP_TDSHP_09 56104000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDS_YLEV_P256										TDS_YLEV_ALPHA					
Type	RW										RW					
Reset	0	1	0	1	0	1	1	0			0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TDS_YLEV_EN														
Type		RW														
Reset		1														

Bit(s)	Name	Description
31:24	TDS_YLEV_P256	**Y level dependent sharpness point 1024** Gain = reg/0x80
21:16	TDS_YLEV_ALPHA	**Y level dependent sharpness blending alpha**
14	TDS_YLEV_EN	**Enables Y level dependent sharpness**

14009040 MDP_PBC_00 MDP_PBC_00 8C02730C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PBC1_EN	PBC1_LPF_EN	PBC1_GAIN								PBC1_RSLOPE_1					
Type	RW	RW	RW								RW					
Reset	1	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PBC1_RSLOPE_1				PBC1_THETA_R						PBC1_RADIUS_R					
Type	RW				RW						RW					
Reset	0	1	1	1	0	0	1	1	0	0	0	0	1	1	0	0

Bit(s)	Name	Description
31	PBC1_EN	0: Disable 1: Enable
30	PBC1_LPF_EN	Enables PBC low-pass filter
29:22	PBC1_GAIN	PBC band gain
21:12	PBC1_RSLOPE_1	For (PBC_RADIUS_C < PBC_RADIUS_RANGE), 1024/PBC_RADIUS_C
11:6	PBC1_THETA_R	Theta range for PBC
5:0	PBC1_RADIUS_R	Radius range for PBC

14009044 MDP_PBC_01 **MDP_PBC_01** **7F1A1550**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PBC1_THETA_C								PBC1_RADIUS_C							
Type	RW								RW							
Reset	0	1	1	1	1	1	1	1	0	0	0	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PBC1_TSLOPE										PBC1_LPF_GAIN					
Type	RW										RW					
Reset	0	0	0	1	0	1	0	1	0	1	0	1	0	0	0	0

Bit(s)	Name	Description
31:24	PBC1_THETA_C	Theta center for PBC
23:16	PBC1_RADIUS_C	Radius center for PBC
15:6	PBC1_TSLOPE	1024/PBC_THETA_RANGE
5:0	PBC1_LPF_GAIN	PBC low-pass filter gain

14009048 MDP_PBC_02 **MDP_PBC_02** **15410C20**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PBC1_RSLOPE												PBC1_CONF_GAIN			
Type	RW												RW			
Reset	0	0	0	1	0	1	0	1	0	1			0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PBC1_EDGE_EN	PBC1_EDGE_THR								PBC1_EDGE_SLOPE					
Type		RW	RW								RW					
Reset		0	0	0	1	1	0	0			1	0	0	0	0	0

Bit(s)	Name	Description
31:22	PBC1_RSLOPE	1024/PBC_RADIUS_RANGE
19:16	PBC1_CONF_GAIN	PBC confidence gain
14	PBC1_EDGE_EN	Enables PBC edge preservation
13:8	PBC1_EDGE_THR	PBC edge threshold
5:0	PBC1_EDGE_SLOPE	PBC edge slope

1400904C MDP_PBC_03 **MDP_PBC_03** **C4020618**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PBC2_EN	PBC2_LPF_EN	PBC2_GAIN								PBC2_RSLOPE_1					
Type	RW	RW	RW								RW					
Reset	1	1	0	0	0	1	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PBC2_RSLOPE_1				PBC2_THETA_R						PBC2_RADIUS_R					
Type	RW				RW						RW					
Reset	0	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0

Bit(s)	Name	Description
31	PBC2_EN	0: Disable 1: Enable

Bit(s)	Name	Description
30	PBC2_LPF_EN	Enables PBC low-pass filter
29:22	PBC2_GAIN	PBC band gain
21:12	PBC2_RSLOPE_1	For (PBC_RADIUS_C < PBC_RADIUS_RANGE), 1024/PBC_RADIUS_C
11:6	PBC2_THETA_R	Theta range for PBC
5:0	PBC2_RADIUS_R	Radius range for PBC

14009050 MDP_PBC_04 MDP_PBC_04 60200AD0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PBC2_THETA_C								PBC2_RADIUS_C							
Type	RW								RW							
Reset	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PBC2_TSLOPE										PBC2_LPF_GAIN					
Type	RW										RW					
Reset	0	0	0	0	1	0	1	0	1	1	0	1	0	0	0	0

Bit(s)	Name	Description
31:24	PBC2_THETA_C	Theta center for PBC
23:16	PBC2_RADIUS_C	Radius center for PBC
15:6	PBC2_TSLOPE	1024/PBC_THETA_RANGE
5:0	PBC2_LPF_GAIN	PBC low-pass filter gain

14009054 MDP_PBC_05 MDP_PBC_05 0AC54C20

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PBC2_RSLOPE												PBC2_CONF_GAIN			
Type	RW												RW			
Reset	0	0	0	0	1	0	1	0	1	1			0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PBC2_EDGE_EN	PBC2_EDGE_THR								PBC2_EDGE_SLOPE					
Type		RW	RW								RW					
Reset		1	0	0	1	1	0	0			1	0	0	0	0	0

Bit(s)	Name	Description
31:22	PBC2_RSLOPE	1024/PBC_RADIUS_RANGE
19:16	PBC2_CONF_GAIN	PBC confidence gain
14	PBC2_EDGE_EN	Enables PBC edge preservation
13:8	PBC2_EDGE_THR	PBC edge threshold
5:0	PBC2_EDGE_SLOPE	PBC edge slope

14009058 MDP_PBC_06 MDP_PBC_06 89011420

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PBC3_EN	PBC3_LPF_EN	PBC3_GAIN								PBC3_RSLOPE_1					
Type	RW	RW	RW								RW					
Reset	1	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PBC3_RSLOPE_1				PBC3_THETA_R						PBC3_RADIUS_R					
Type	RW				RW						RW					
Reset	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31	PBC3_EN	0: Disable 1: Enable
30	PBC3_LPF_EN	Enables PBC low-pass filter
29:22	PBC3_GAIN	PBC band gain
21:12	PBC3_RSLOPE_1	For (PBC_RADIUS_C < PBC_RADIUS_RANGE), 1024/PBC_RADIUS_C
11:6	PBC3_THETA_R	Theta range for PBC
5:0	PBC3_RADIUS_R	Radius range for PBC

1400905C MDP_PBC_07 MDP_PBC_07 E03C1010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PBC3_THETA_C								PBC3_RADIUS_C							
Type	RW								RW							
Reset	1	1	1	0	0	0	0	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PBC3_TSLOPE										PBC3_LPF_GAIN					
Type	RW										RW					
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:24	PBC3_THETA_C	Theta center for PBC
23:16	PBC3_RADIUS_C	Radius center for PBC
15:6	PBC3_TSLOPE	1024/PBC_THETA_RANGE
5:0	PBC3_LPF_GAIN	PBC low-pass filter gain

14009060 MDP_PBC_08 MDP_PBC_08 08010C20

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PBC3_RSLOPE												PBC3_CONF_GAIN			
Type	RW												RW			
Reset	0	0	0	0	1	0	0	0	0	0			0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PBC3_EDGE_EN	PBC3_EDGE_THR								PBC3_EDGE_SLOPE					
Type		RW	RW								RW					
Reset		0	0	0	1	1	0	0			1	0	0	0	0	0

Bit(s)	Name	Description
31:22	PBC3_RSLOPE	1024/PBC_RADIUS_RANGE
19:16	PBC3_CONF_GAIN	PBC confidence gain
14	PBC3_EDGE_EN	Enables PBC edge preservation
13:8	PBC3_EDGE_THR	PBC edge threshold
5:0	PBC3_EDGE_SLOPE	PBC edge slope

14009064 MDP_HIST_CFG_00 **MDP_HIST_CFG_00** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HIST_WIN_X_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_WIN_X_START															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	HIST_WIN_X_END	**Histogram window** X end position
15:0	HIST_WIN_X_START	**Histogram window** X start position

14009068 MDP_HIST_CFG_01 **MDP_HIST_CFG_01** **FFFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HIST_WIN_Y_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_WIN_Y_START															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	HIST_WIN_Y_END	**Histogram window** Y end position
15:0	HIST_WIN_Y_START	**Histogram window** Y start position

1400906C MDP_LUMA_HIST_00 **Result of Luma Histogram 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_00										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_00															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_00	Luma histogram bin 0

14009070 MDP_LUMA_HIST_01 Result of Luma Histogram 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_01										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_01															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_01	Luma histogram bin 1

14009074 MDP_LUMA_HIST_02 Result of Luma Histogram 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_02										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_02															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_02	Luma histogram bin 2

14009078 MDP_LUMA_HIST_03 Result of Luma Histogram 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_03										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_03															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_03	Luma histogram bin 3

1400907C MDP_LUMA_HIST_04 Result of Luma Histogram 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_04										

Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_04															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_04	Luma histogram bin 4

14009080 MDP_LUMA_HIST_05 Result of Luma Histogram 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LUMA_HIST_05															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_05															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_05	Luma histogram bin 5

14009084 MDP_LUMA_HIST_06 Result of Luma Histogram 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LUMA_HIST_06															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_06															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_06	Luma histogram bin 6

1400908C MDP_LUMA_HIST_07 Result of Luma Histogram 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LUMA_HIST_07															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_07															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_07	Luma histogram bin 7

14009090 MDP_LUMA_HIST_08 Result of Luma Histogram 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_08										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_08															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_08	Luma histogram bin 8

14009094 MDP_LUMA_HIST_09 Result of Luma Histogram 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_09										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_09															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_09	Luma histogram bin 9

14009098 MDP_LUMA_HIST_10 Result of Luma Histogram 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_10										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_10															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
26:0	LUMA_HIST_10	Luma histogram bin 10

1400909C MDP_LUMA_HIST_11 Result of Luma Histogram 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_11										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_11															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_11	Luma histogram bin 11

140090A0 MDP_LUMA_HIST_12 Result of Luma Histogram 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_12										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_12															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_12	Luma histogram bin 12

140090A4 MDP_LUMA_HIST_13 Result of Luma Histogram 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_13										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_13															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_13	Luma histogram bin 13

140090A8 MDP_LUMA_HIST_14 **Result of Luma Histogram 14** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_14										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_14															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_14	Luma histogram bin 14

140090AC MDP_LUMA_HIST_15 **Result of Luma Histogram 15** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_15										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_15															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_15	Luma histogram bin 15

140090B0 MDP_LUMA_HIST_16 **Result of Luma Histogram 16** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						LUMA_HIST_16										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_HIST_16															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	LUMA_HIST_16	Luma histogram bin 16

140090B4 MDP_LUMA_SUM **Result of luma sum** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LUMA_SUM															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_SUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LUMA_SUM	Luma sum. of current frame

140090BC MDP_Y_FTN_1_0_MAIN 2nd Y Transfer Function 1, 0 00200000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								Y_FTN_1								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								Y_FTN_0								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	Y_FTN_1	Control point of luma curve on luma level 16 (8 bits)
8:0	Y_FTN_0	Control point of luma curve on luma level 0 (8 bits)

140090C0 MDP_Y_FTN_3_2_MAIN 2nd Y Transfer Function 3, 2 00600040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								Y_FTN_3								
Type								RW								
Reset								0	0	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								Y_FTN_2								
Type								RW								
Reset								0	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	Y_FTN_3	Control point of luma curve on luma level 48 (8 bits)
8:0	Y_FTN_2	Control point of luma curve on luma level 32 (8 bits)

140090C4 MDP_Y_FTN_5_4_MAIN 2nd Y Transfer Function 5, 4 00A00080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								Y_FTN_5								
Type								RW								
Reset								0	1	0	1	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								Y_FTN_4								
Type								RW								
Reset								0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	Y_FTN_5	Control point of luma curve on luma level 80 (8 bits)
8:0	Y_FTN_4	Control point of luma curve on luma level 64 (8 bits)

140090C8 MDP_Y_FTN_7_6_MAIN **2nd Y Transfer Function 7, 6** **00E000C0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								Y_FTN_7								
Type								RW								
Reset								0	1	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								Y_FTN_6								
Type								RW								
Reset								0	1	1	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	Y_FTN_7	Control point of luma curve on luma level 112 (8 bits)
8:0	Y_FTN_6	Control point of luma curve on luma level 96 (8 bits)

140090CC MDP_Y_FTN_9_8_MAIN **2nd Y Transfer Function 9, 8** **01200100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								Y_FTN_9								
Type								RW								
Reset								1	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								Y_FTN_8								
Type								RW								
Reset								1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	Y_FTN_9	Control point of luma curve on luma level 144 (8 bits)
8:0	Y_FTN_8	Control point of luma curve on luma level 128 (8 bits)

140090D0 MDP_Y_FTN_11_10_MAIN **2nd Y Transfer Function 11, 10** **01600140**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								Y_FTN_11								
Type								RW								
Reset								1	0	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name								Y_FTN_10								
Type								RW								
Reset								1	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	Y_FTN_11	Control point of luma curve on luma level 176 (8 bits)
8:0	Y_FTN_10	Control point of luma curve on luma level 160 (8 bits)

140090D4 MDP_Y_FTN_13_12_MAIN — 2nd Y Transfer Function 13, 12 — 01A00180

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								Y_FTN_13								
Type								RW								
Reset								1	1	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								Y_FTN_12								
Type								RW								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	Y_FTN_13	Control point of luma curve on luma level 208 (8 bits)
8:0	Y_FTN_12	Control point of luma curve on luma level 192 (8 bits)

140090D8 MDP_Y_FTN_15_14_MAIN — 2nd Y Transfer Function 15, 14 — 01E001C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								Y_FTN_15								
Type								RW								
Reset								1	1	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								Y_FTN_14								
Type								RW								
Reset								1	1	1	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	Y_FTN_15	Control point of luma curve on luma level 240 (8 bits)
8:0	Y_FTN_14	Control point of luma curve on luma level 224 (8 bits)

140090DC MDP_Y_FTN_17_16_MAIN — 2nd Y Transfer Function 17, 16 — 00000200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							Y_FTN_16									

Type							RW									
Reset							1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	Y_FTN_16	Control point of luma curve on luma level 256 (8 bits)

140090E0 MDP_C_BOOST_MAIN — Chroma Boost — FF802080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NEW_CBOOST_LMT_U								NEW_CBOOST_LMT_L							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			NEW_CBOOST_EN						CBOOST_GAIN							
Type			RW						RW							
Reset			1						1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	NEW_CBOOST_LMT_U	Chroma boost gain upper bound
23:16	NEW_CBOOST_LMT_L	Chroma boost gain lower bound
13	NEW_CBOOST_EN	0: Disable new chroma boost 1: Enable new chroma boost
7:0	CBOOST_GAIN	128 denotes 1.0

140090E4 MDP_C_BOOST_MAIN_2 — Chroma Boost 2 — 10000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CBOOST_YCONST														CBOOST_YOFFSET_SEL	
Type	RW														RW	
Reset	0	0	0	1	0	0	0	0							0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										CBOOST_YOFFSET						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	CBOOST_YCONST	Y constant value of chroma boost
17:16	CBOOST_YOFFSET_SEL	Limit function of CBOOST_YOFFSET
6:0	CBOOST_YOFFSET	Y offset value of chroma boost

140090E8 MDP_TDSHP_C_BOOST_MAIN — TDSHP Chroma Boost — FF802080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDSH P_CB OOST _LMT _U								TDSHP_CBOOST_LMT_L							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			TDSH P_CB OOST _EN						TDSHP_CBOOST_GAIN							
Type			RW						RW							
Reset			1						1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	TDSHP_CBOOST_LMT_U	**[TDSHP] Chroma boost gain upper bound**
23:16	TDSHP_CBOOST_LMT_L	**[TDSHP] Chroma boost gain lower bound**
13	TDSHP_CBOOST_EN	**[TDSHP]** 0: Disable new chroma boost 1: Enable new chroma boost
7:0	TDSHP_CBOOST_GAIN	**[TDSHP] 128 denotes 1.0**

140090EC MDP_TDSHP_C_BOOST_MAIN_2 — TDSHP Chroma Boost 2 — 08000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDSH P_CB OOST _YCO NST														TDSH P_CB OOST _YOF FSET _SEL	
Type	RW														RW	
Reset	0	0	0	0	1	0	0	0							0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										TDSHP_CBOOST_YOFFSET						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	TDSHP_CBOOST_YCONST	[TDSHP] Y constant value of chroma boost
17:16	TDSHP_CBOOST_YOFFSET_SEL	[TDSHP] Limit function of CBOOST_YOFFSET
6:0	TDSHP_CBOOST_YOFFSET	[TDSHP] Y offset value of chroma boost

140090FC MDP_TDSHP_ATPG — MDP_TDSHP_ATPG — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															TDSH P_AT PG_C T	TDSH P_AT PG_O B
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	TDSHP_ATPG_CT	
0	TDSHP_ATPG_OB	

14009100 MDP_TDSHP_CTRL MDP_TDSHP_CTRL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															TDSHP_RESET	TDSHP_CTRL_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	TDSHP_RESET	0: De-assert software reset 1: Essert software reset
0	TDSHP_CTRL_EN	Enables TDSHP

14009104 MDP_TDSHP_INTEN MDP_TDSHP_INTEN 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FRAME_UNDERRUN_EN	OF_END_INT_EN	IF_END_INT_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FRAME_UNDERRUN_EN	Enables frame underrun interrupt
1	OF_END_INT_EN	Enables output frame end interrupt
0	IF_END_INT_EN	Enables input frame end interrupt

14009108 MDP_TDSHP_INTSTA MDP_TDSHP_INTSTA 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FRAME_UNDERRUN	OF_END_INT	IF_END_INT
Type														RO	RO	RO
Reset														0	0	0

Bit(s)	Name	Description
2	FRAME_UNDERRUN	1: Frame underrun (write 0 to clear)
1	OF_END_INT	1: Output frame end (write 0 to clear)
0	IF_END_INT	1: Input frame end (write 0 to clear)

1400910C MDP_TDSHP_STATUS **MDP_TDSHP_STATUS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TDSHP_HANDSHAKE						TDSHP_STATUS	
Type									RO						RO	
Reset									0	0	0	0			0	0

Bit(s)	Name	Description
7:4	TDSHP_HANDSHAKE	
1:0	TDSHP_STATUS	

14009110 MDP_TDSHP_CFG **MDP_TDSHP_CFG** **000000C0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							stop_to_wdma	dcm_dis	COLOR_HIST_EN	LUMA_HIST_EN	DEMO_SWAP	DEMO_EN		FIFO_POSIT	FIFO_EN	RELAY_MODE
Type							RW	RW	RW	RW	RW	RW		RW	RW	RW
Reset							0	0	1	1	0	0		0	0	0

Bit(s)	Name	Description
9	stop_to_wdma	0: Normal path 1: Signal stop to WDMA
8	dcm_dis	0: Enable DCM 1: Disable DCM
7	COLOR_HIST_EN	0: Disable color histogram 1: Enable color histogram

Bit(s)	Name	Description
6	LUMA_HIST_EN	0: Disable luma histogram 1: Enable luma histogram
5	DEMO_SWAP	0: Sharpness inside window 1: Sharpness outside window
4	DEMO_EN	0: Disable 1: Enable
2	FIFO_POSIT	0: Before TDSHP (input prefetch) 1: Behind TDSHP (output buffer)
1	FIFO_EN	0: Disable 1: Enable
0	RELAY_MODE	0: Disable 1: Enable

14009114 MDP_TDSHP_INPUT_COUNT MDP_TDSHP_INPUT_COUNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				INP_LINE_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				INP_PIX_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	INP_LINE_CNT	
12:0	INP_PIX_CNT	

14009118 MDP_TDSHP_CHKSUM Input or Output Data Checksum 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKSUM_EN		CHKSUM_SEL						CHKSUM							
Type	RW		RW						RO							
Reset	0		0	0					0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKSUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	CHKSUM_EN	0: Disable 1: Enable
29:28	CHKSUM_SEL	2'b00: Check input data 2'b01: Check output data
23:0	CHKSUM	

1400911C MDP_TDSHP_OUTPUT_COUNT MDP_TDSHP_OUTPUT_COUNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				OUTP_LINE_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OUTP_PIX_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	OUTP_LINE_CNT	
12:0	OUTP_PIX_CNT	

14009120 MDP_TDSHP_INPUT_SIZE MDP_TDSHP_INPUT_SIZE 01080190

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				IN_HSIZE												
Type				RW												
Reset				0	0	0	0	1	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				IN_VSIZE												
Type				RW												
Reset				0	0	0	0	1	1	0	0	1	0	0	0	0

Bit(s)	Name	Description
28:16	IN_HSIZE	Input active width
12:0	IN_VSIZE	Input active height

14009124 MDP_TDSHP_OUTPUT_OFFSET MDP_TDSHP_OUTPUT_OFFSET 00040000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									OUT_ HOFF SET							
Type									RW							
Reset									0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									OUT_VOFFSET							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	OUT_HOFFSET	Output active width offset
7:0	OUT_VOFFSET	Output active height offset

14009128 MDP_TDSHP_OUTPUT_SIZE MDP_TDSHP_OUTPUT_SIZE 01000190

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				OUT_HSIZE												
Type				RW												
Reset				0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OUT_VSIZE												
Type				RW												
Reset				0	0	0	0	1	1	0	0	1	0	0	0	0

Bit(s)	Name	Description
28:16	OUT_HSIZE	Output active width
12:0	OUT_VSIZE	Output active height

1400912C MDP_TDSHP_BLANK_WIDTH MDP_TDSHP_BLANK_WIDTH 00130202

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									HSYNC_WIDTH							
Type									RW							
Reset									0	0	0	1	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VSYNC_HSYNC_WIDTH								VSYNC_HACT_WIDTH							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0

Bit(s)	Name	Description
23:16	HSYNC_WIDTH	Hsync width
15:8	VSYNC_HSYNC_WIDTH	Hsync width in vsync region
7:0	VSYNC_HACT_WIDTH	Hactive width in vsync region

14009130 MDP_TDSHP_DEMO_HMASK MDP_TDSHP_DEMO_HMASK 00010084

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DEMO_MASK_HSTART												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DEMO_MASK_HEND												
Type				RW												
Reset				0	0	0	0	0	1	0	0	0	0	1	0	0

Bit(s)	Name	Description
28:16	DEMO_MASK_HSTART	Horizontal start position of demo window
12:0	DEMO_MASK_HEND	Horizontal end position of demo window

Bit(s)	Name	Description

14009134 MDP_TDSHP_DEMO_VMASK — **MDP_TDSHP_DEMO_VMASK** — **00010190**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DEMO_MASK_VSTART												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DEMO_MASK_VEND												
Type				RW												
Reset				0	0	0	0	1	1	0	0	1	0	0	0	0

Bit(s)	Name	Description
28:16	DEMO_MASK_VSTART	Vertical start position of demo window
12:0	DEMO_MASK_VEND	Vertical end position of demo window

1400914C MDP_TDSHP_DUMMY_REG — **MDP_TDSHP_DUMMY_REG** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	APB_REG_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	APB_REG_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	APB_REG_DUMMY	

14009200 MDP_LUMA_HIST_INIT_0 — **MDP_LUMA_HIST_INIT_00** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_00										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_00															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_00	Initial value of luma histogram bin 0

14009204 MDP_LUMA_HIST_INIT_01 MDP_LUMA_HIST_INIT_01 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_01										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_01															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_01	Initial value of luma histogram bin 1

14009208 MDP_LUMA_HIST_INIT_02 MDP_LUMA_HIST_INIT_02 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_02										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_02															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_02	Initial value of luma histogram bin 2

1400920C MDP_LUMA_HIST_INIT_03 MDP_LUMA_HIST_INIT_03 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_03										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_03															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_03	Initial value of luma histogram bin 3

14009210 MDP_LUMA_H MDP_LUMA_HIST_INIT_04 00000000

IST_INIT_0
4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_04										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_04															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_04	Initial value of luma histogram bin 4

14009214 MDP_LUMA_HIST_INIT_05 MDP_LUMA_HIST_INIT_05 00000000

IST_INIT_0
5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_05										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_05															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_05	Initial value of luma histogram bin 5

14009218 MDP_LUMA_HIST_INIT_06 MDP_LUMA_HIST_INIT_06 00000000

IST_INIT_0
6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_06										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_06															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_06	Initial value of luma histogram bin 6

1400921C MDP_LUMA_HIST_INIT_0 MDP_LUMA_HIST_INIT_07 00000000

7

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_07										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_07															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_07	Initial value of luma histogram bin 7

14009220 MDP_LUMA_HIST_INIT_0 8 — MDP_LUMA_HIST_INIT_08 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_08										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_08															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_08	Initial value of luma histogram bin 8

14009224 MDP_LUMA_HIST_INIT_0 9 — MDP_LUMA_HIST_INIT_09 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_09										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_09															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_09	Initial value of luma histogram bin 9

14009228 MDP_LUMA_HIST_INIT_1 — MDP_LUMA_HIST_INIT_10 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name						HIST_BIN_INIT_10										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_10	Initial value of luma histogram bin 10

1400922C MDP_LUMA_HIST_INIT_1 1 **MDP_LUMA_HIST_INIT_11** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_11										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_11	Initial value of luma histogram bin 11

14009230 MDP_LUMA_HIST_INIT_1 2 **MDP_LUMA_HIST_INIT_12** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_12										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_12	Initial value of luma histogram bin 12

14009234 MDP_LUMA_HIST_INIT_1 3 **MDP_LUMA_HIST_INIT_13** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_13										

Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_13	Initial value of luma histogram bin 13

14009238 MDP_LUMA_HIST_INIT_14 MDP_LUMA_HIST_INIT_14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_14										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_14															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_14	Initial value of luma histogram bin 14

1400923C MDP_LUMA_HIST_INIT_15 MDP_LUMA_HIST_INIT_15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_15										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_15	Initial value of luma histogram bin 15

14009240 MDP_LUMA_HIST_INIT_16 MDP_LUMA_HIST_INIT_16 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HIST_BIN_INIT_16										
Type						RW										

Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_BIN_INIT_16															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	HIST_BIN_INIT_16	Initial value of luma histogram bin 16

14009244 MDP_LUMA_SUM_INIT MDP_LUMA_SUM_INIT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HIST_SUM_INIT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIST_SUM_INIT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	HIST_SUM_INIT	Initial value of luma sum

14009250 MDP_DC_DBG_CFG_MAIN MDP_DC_DBG_CFG_MAIN 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														W1_INK_EN	DC_SPLIT_SWAP	DC_SPLIT_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	W1_INK_EN	**Enables ink for w1**
1	DC_SPLIT_SWAP	**Swaps DC demo window or not** 0: Does not swap 1: Swap demo window
0	DC_SPLIT_EN	**Splits DC demo window or not** 0: Process the whole window 1: Split DC demo window

14009254 MDP_DC_WIN_X_MAIN MDP_DC_WIN_X_MAIN FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DC_WIN_X_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DC_WIN_X_START															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DC_WIN_X_END	X end for DC processing window
15:0	DC_WIN_X_START	X start for DC processing window

14009258 MDP_DC_WIN_Y_MAIN MDP_DC_WIN_Y_MAIN FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DC_WIN_Y_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DC_WIN_Y_START															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DC_WIN_Y_END	Y end for DC processing window
15:0	DC_WIN_Y_START	Y start for DC processing window

1400925C MDP_DC_TWO_D_W1 MDP_DC_TWO_D_W1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	W1_SAT_UPPER								W1_SAT_LOWER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	W1_HUE_UPPER								W1_HUE_LOWER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	W1_SAT_UPPER	Saturation upper bound for accumulation
23:16	W1_SAT_LOWER	Saturation lower bound for accumulation
15:8	W1_HUE_UPPER	Hue upper bound for accumulation
7:0	W1_HUE_LOWER	Hue lower bound for accumulation

14009260 MDP_DC_TWO_D_W1_RESULT_INIT MDP_DC_TWO_D_W1_RESULT_INIT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										W1_RESULT_INIT						
Type										RW						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	W1_RESULT_INIT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
22:0	W1_RESULT_INIT	Initial value of w1

14009264 MDP_DC_TWO_D_W1_RESULT MDP_DC_TWO_D_W1_RESULT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										W1_RESULT						
Type										RO						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	W1_RESULT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
22:0	W1_RESULT	Result of w1

14009300 MDP_EDF_GAIN_00 MDP_EDF_GAIN_00 80401002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EDF_GAIN_EN			EDF_ FLAT _GAI N					EDF_DETAIL_GAIN							
Type	RW			RW					RW							
Reset	1			0	0	0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				EDF_EDGE_GAIN										EDF_CLIP_RATIO_INC		
Type				RW										RW		
Reset				1	0	0	0	0						0	1	0

Bit(s)	Name	Description
31	EDF_GAIN_EN	**Enables edge/detail/flat gain**
28:24	EDF_FLAT_GAIN	**Flat gain** Unit: 1/16
23:16	EDF_DETAIL_GAIN	**Detail gain** Unit: 1/16
12:8	EDF_EDGE_GAIN	**Edge gain** Unit: 1/16
2:0	EDF_CLIP_RATIO_INC	**Clip ratio increment when edge/detail/flat gain is**

Bit(s)	Name	Description
		enabled

14009304 MDP_EDF_GAIN_01 **MDP_EDF_GAIN_01** **2041E0F0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		EDF_FLAT_TH							EDF_DETAIL_RISE_TH						EDF_DETAIL_FALL_TH	
Type		RW							RW						RW	
Reset		0	1	0	0	0	0		0	1	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EDF_DETAIL_FALL_TH							EDF_EDGE_TH								
Type	RW							RW								
Reset	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
30:25	EDF_FLAT_TH	Flat threshold
23:18	EDF_DETAIL_RISE_TH	Detail rise threshold
17:9	EDF_DETAIL_FALL_TH	Detail fall threshold
8:0	EDF_EDGE_TH	Edge threshold

14009308 MDP_EDF_GAIN_02 **MDP_EDF_GAIN_02** **04050A0A**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						EDF_FLAT_SLOPE								EDF_DETAIL_RISE_SLOPE		
Type						RW								RW		
Reset						1	0	0						1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				EDF_DETAIL_FALL_SLOPE								EDF_EDGE_SLOPE				
Type				RW								RW				
Reset				0	1	0	1	0				0	1	0	1	0

Bit(s)	Name	Description
26:24	EDF_FLAT_SLOPE	**Flat slope**
18:16	EDF_DETAIL_RISE_SLOPE	**Detail rise slope** Unit: 1/2
12:8	EDF_DETAIL_FALL_SLOPE	**Detail fall slope** Unit: 1/64
4:0	EDF_EDGE_SLOPE	**Sdge slope** Unit: 1/64

1400930C MDP_EDF_GAIN_03 **MDP_EDF_GAIN_03** **00083007**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				EDF_EDGE_MAG_TH								EDF_EDGE_MAG_SLOPE				
Type				RW								RW				
Reset				0	0	0	0	0				0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name		EDF_EDGE_MONO_TH											EDF_EDGE_MONO_SLOPE			
Type		RW											RW			
Reset		0	1	1	0	0	0	0					0	1	1	1

Bit(s)	Name	Description
28:24	EDF_EDGE_MAG_TH	**Edge magnitude threshold**
20:16	EDF_EDGE_MAG_SLOPE	**Edge magnitude slope** Unit: 1/32
14:8	EDF_EDGE_MONO_TH	**Edge monotone threshold**
3:0	EDF_EDGE_MONO_SLOPE	**Edge monotone slope** Unit: 1/32

14009310 MDP_EDF_GAIN_04 **MDP_EDF_GAIN_04** **20100800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			EDF_EDGE_TREND_TH									EDF_EDGE_TREND_SLOPE				
Type			RW									RW				
Reset			1	0	0	0	0	0				1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				EDF_EDGE_TREND_FLAT_MAG												
Type				RW												
Reset				0	1	0	0	0								

Bit(s)	Name	Description
29:24	EDF_EDGE_TREND_TH	**Edge trend threshold**
20:16	EDF_EDGE_TREND_SLOPE	**Edge trend slope** Unit: 1/16
12:8	EDF_EDGE_TREND_FLAT_MAG	**Edge trend flat magnitude threshold**

14009314 MDP_EDF_GAIN_05 **MDP_EDF_GAIN_05** **00202020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									EDF_BLD_WGT_TREND							
Type									RW							
Reset									0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EDF_BLD_WGT_MONO								EDF_BLD_WGT_MAG							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
23:16	EDF_BLD_WGT_TREND	**Blending weight for trend** Unit: 1/32
15:8	EDF_BLD_WGT_MONO	**Blending weight for monotone** Unit: 1/32
7:0	EDF_BLD_WGT_MAG	**Blending weight for magnitude** Unit: 1/32

14009320 MDP_TDSHP_10 MDP_TDSHP_10 04020008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDS_MID_COR_THR								TDS_MID_COR_ZERO							
Type	RW								RW							
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TDS_MID_LIMIT_RATIO			
Type													RW			
Reset													1	0	0	0

Bit(s)	Name	Description
31:24	TDS_MID_COR_THR	Mid AC coring threshold
23:16	TDS_MID_COR_ZERO	Mid AC zero threshold
3:0	TDS_MID_LIMIT_RATIO	Mid AC soft limit ratio

14009324 MDP_TDSHP_11 MDP_TDSHP_11 18300310

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDS_MID_LIMIT								TDS_MID_BOUND							
Type	RW								RW							
Reset	0	0	0	1	1	0	0	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDS_MID_COR_VALUE								TDS_MID_COR_GAIN							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:24	TDS_MID_LIMIT	**Mid AC positive limit**
23:16	TDS_MID_BOUND	**Mid AC postive bound**
15:8	TDS_MID_COR_VALUE	**Mid AC coring value** TDS_COR_ZERO + ((TDS_COR_THR - TDS_COR_ZERO)*(16 - TDS_COR_RATIO) + 8) >> 4
7:0	TDS_MID_COR_GAIN	**Mid AC soft coring gain** TDS_GAIN*((TDS_COR_RATIO + 8) >> 4)

14009328 MDP_TDSHP_12 MDP_TDSHP_12 04020008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDS_HIGH_COR_THR								TDS_HIGH_COR_ZERO							
Type	RW								RW							
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TDS_HIGH_LIMIT_RATIO			
Type													RW			
Reset													1	0	0	0

Bit(s)	Name	Description
31:24	TDS_HIGH_COR_THR	High AC coring threshold
23:16	TDS_HIGH_COR_ZERO	High AC zero threshold
3:0	TDS_HIGH_LIMIT_RATIO	High AC soft limit ratio

1400932C MDP_TDSHP_13 **MDP_TDSHP_13** **18300310**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDS_HIGH_LIMIT								TDS_HIGH_BOUND							
Type	RW								RW							
Reset	0	0	0	1	1	0	0	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDS_HIGH_COR_VALUE								TDS_HIGH_COR_GAIN							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:24	TDS_HIGH_LIMIT	**High AC positive limit**
23:16	TDS_HIGH_BOUND	**High AC postive bound**
15:8	TDS_HIGH_COR_VALUE	**High AC coring value** TDS_COR_ZERO + ((TDS_COR_THR - TDS_COR_ZERO)*(16 - TDS_COR_RATIO) + 8) >> 4
7:0	TDS_HIGH_COR_GAIN	**High AC soft coring gain** TDS_GAIN*((TDS_COR_RATIO + 8) >> 4)

14009330 PAT1_GEN_SET **Configuration** **0000004C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									reg_pat1_pat_type							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									reg_pat1_grid_size				reg_pat1_grid_show			reg_pat1_pat_gen_en
Type									RW				RW			RW
Reset									0	1	0	0	1	1		0

Bit(s)	Name	Description
23:16	reg_pat1_pat_type	**Enables pattern gen**
7:4	reg_pat1_grid_size	**Grid size: 2^(n+1), n<=11**
3:2	reg_pat1_grid_show	**[0]: Show grid** [1]: Show boundary
0	reg_pat1_pat_gen_en	**Pattern type** 0: Pure color 1: Cursor 2: Ramp 3: Grid

14009334 PAT1_GEN_FRM_SIZE **Configuration** **04380780**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				reg_pat1_frm_size_v												
Type				RW												
Reset				0	0	1	0	0	0	0	1	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				reg_pat1_frm_size_h												
Type				RW												
Reset				0	0	1	1	1	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	reg_pat1_frm_size_v	Frame real size in V
12:0	reg_pat1_frm_size_h	Frame real size in H

14009338 PAT1_GEN_COLOR0 **Configuration** **03FF03FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							reg_pat1_color_u									
Type							RW									
Reset							1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							reg_pat1_color_y									
Type							RW									
Reset							1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
25:16	reg_pat1_color_u	fg color U
9:0	reg_pat1_color_y	fg color Y

1400933C PAT1_GEN_COLOR1 **Configuration** **000003FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							reg_pat1_bg_color _y									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							reg_pat1_color_v									
Type							RW									
Reset							1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
25:16	reg_pat1_bg_color_y	bg color Y
9:0	reg_pat1_color_v	fg color V

14009340 PAT1_GEN_C **Configuration** **00000000**

OLOR2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							reg_pat1_bg_color _v									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							reg_pat1_bg_color_u									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	reg_pat1_bg_color_v	bg color V
9:0	reg_pat1_bg_color_u	bg color U

14009344 PAT1_GEN_POS **Configuration** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				reg_pat1_pos_y												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				reg_pat1_pos_x												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	reg_pat1_pos_y	Position Y
12:0	reg_pat1_pos_x	Position X

14009354 PAT1_GEN_TILE_POS **Configuration** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				reg_pat1_tile_pos_y												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				reg_pat1_tile_pos_x												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	reg_pat1_tile_pos_y	Tile origin postion Y
12:0	reg_pat1_tile_pos_x	Tile origin postion X

14009358 PAT1_GEN_TILE_OV **Configuration** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_pat1_tile_ov_y								reg_pat1_tile_ov_x							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	reg_pat1_tile_ov_y	Tile overlap Y
7:0	reg_pat1_tile_ov_x	Tile overlap X

14009360 PAT2_GEN_SET **Configuration** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									reg_ pat2 _pat _typ e							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															reg_ pat2 _cur sor_ show	reg_ pat2 _pat _gen _en
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
23:16	reg_pat2_pat_type	**Enables pattern gen**
1	reg_pat2_cursor_show	**Shows cursor cross line**
0	reg_pat2_pat_gen_en	**Pattern type** 0: Pure color 1: Cursor 2: Ramp 3: Grid

14009368 PAT2_GEN_COLOR0 **Configuration** **03FF03FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							reg_pat2_color_u									
Type							RW									
Reset							1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							reg_pat2_color_y									
Type							RW									
Reset							1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
25:16	reg_pat2_color_u	fg color U

Bit(s)	Name	Description
9:0	reg_pat2_color_y	fg color Y

1400936C PAT2_GEN_COLOR1 **Configuration** **000003FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							reg_pat2_color_v									
Type							RW									
Reset							1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
9:0	reg_pat2_color_v	fg color V

14009374 PAT2_GEN_POS **Configuration** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				reg_pat2_pos_y												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				reg_pat2_pos_x												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	reg_pat2_pos_y	position Y
12:0	reg_pat2_pos_x	position X

14009378 PAT2_GEN_CURSOR_RB0 **Readback** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							pat2_rb_cursor_u									
Type							RO									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							pat2_rb_cursor_y									
Type							RO									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	pat2_rb_cursor_u	Cursor readback U
9:0	pat2_rb_cursor_y	Cursor readback Y

Bit(s)	Name	Description

1400937C PAT2_GEN_CURSOR_RB1 **Readback** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							pat2_rb_cursor_v									
Type							RO									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	pat2_rb_cursor_v	Cursor readback V

14009384 PAT2_GEN_TILE_POS **Configuration** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				reg_pat2_tile_pos_y												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				reg_pat2_tile_pos_x												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	reg_pat2_tile_pos_y	Tile origin postion Y
12:0	reg_pat2_tile_pos_x	Tile origin postion X

14009388 PAT2_GEN_TILE_OV **Configuration** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_pat2_tile_ov_y								reg_pat2_tile_ov_x							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	reg_pat2_tile_ov_y	Tile overlap Y
7:0	reg_pat2_tile_ov_x	Tile overlap X

Module name: DISP_OVL0 Base address: (+1400b000h)

Address	Name	Width	Register Function
1400B000	OVL_STA	32	Overlay Status Monitor
1400B004	OVL_INTEN	32	Overlay Interrupt Enable
1400B008	OVL_INTSTA	32	Overlay Interrupt Status
1400B00C	OVL_EN	32	Overlay Enable
1400B010	OVL_TRIG	32	Overlay Trigger
1400B014	OVL_RST	32	Overlay Reset
1400B020	OVL_ROI_SIZE	32	Overlay ROI Size
1400B024	OVL_DATAPATH_CON	32	Overlay Datapath Control
1400B028	OVL_ROI_BGCLR	32	Overlay Background Color
1400B02C	OVL_SRC_CON	32	Overlay Source Control
1400B030	OVL_L0_CON	32	Overlay Layer 0 Control
1400B034	OVL_L0_SRCKEY	32	Overlay Layer 0 Source Key
1400B038	OVL_L0_SRC_SIZE	32	Overlay Layer 0 Source Size
1400B03C	OVL_L0_OFFSET	32	Overlay Layer 0 Offset
1400BF40	OVL_L0_ADDR	32	Overlay Layer 0 Memory Address
1400B044	OVL_L0_PITCH	32	Overlay Layer 0 Pitch
1400B048	OVL_L0_TILE	32	Overlay Layer 0 Tile Control
1400B04C	OVL_L0_CLIP	32	Overlay Layer 0 Clip
1400B050	OVL_L1_CON	32	Overlay Layer 1 Control
1400B054	OVL_L1_SRCKEY	32	Overlay Layer 1 Source Key
1400B058	OVL_L1_SRC_SIZE	32	Overlay Layer 1 Source Size
1400B05C	OVL_L1_OFFSET	32	Overlay Layer 1 Offset
1400BF60	OVL_L1_ADDR	32	Overlay Layer 1 Memory Address
1400B064	OVL_L1_PITCH	32	Overlay Layer 1 Pitch
1400B068	OVL_L1_TILE	32	Overlay Layer 1 Tile Control
1400B06C	OVL_L1_CLIP	32	Overlay Layer 1 Clip
1400B070	OVL_L2_CON	32	Overlay Layer 2 Control
1400B074	OVL_L2_SRCKEY	32	Overlay Layer 2 Source Key
1400B078	OVL_L2_SRC_SIZE	32	Overlay Layer 2 Source Size
1400B07C	OVL_L2_OFFSET	32	Overlay Layer 2 Offset
1400BF80	OVL_L2_ADDR	32	Overlay Layer 2 Memory Address
1400B084	OVL_L2_PITCH	32	Overlay Layer 2 Pitch
1400B088	OVL_L2_TILE	32	Overlay Layer 2 Tile Control
1400B08C	OVL_L2_CLIP	32	Overlay Layer 2 Clip
1400B090	OVL_L3_CON	32	Overlay Layer 3 Control
1400B094	OVL_L3_SRCKEY	32	Overlay Layer 3 Source Key
1400B098	OVL_L3_SRC_SIZE	32	Overlay Layer 3 Source Size
1400B09C	OVL_L3_OFFSET	32	Overlay Layer 3 Offset
1400BFA0	OVL_L3_ADDR	32	Overlay Layer 3 Memory Address
1400B0A4	OVL_L3_PITCH	32	Overlay Layer 3 Pitch
1400B0A8	OVL_L3_TILE	32	Overlay Layer 3 Tile Control
1400B0AC	OVL_L3_CLIP	32	Overlay Layer 3 Clip
1400B0C0	OVL_RDMA0_CTRL	32	Overlay RDMA0 Control
1400B0C8	OVL_RDMA0_MEM_	32	**Overlay RDMA0 Memory GMC Setting**

Address	Name	Width	Register Function
	GMC_SETTING1		
1400B0CC	OVL_RDMA0_MEM_SLOW_CON	32	Overlay RDMA0 Memory Slow Control
1400B0D0	OVL_RDMA0_FIFO_CTRL	32	Overlay RDMA0 FIFO Control
1400B0E0	OVL_RDMA1_CTRL	32	Overlay RDMA1 Control
1400B0E8	OVL_RDMA1_MEM_GMC_SETTING1	32	Overlay RDMA1 Memory GMC Setting
1400B0EC	OVL_RDMA1_MEM_SLOW_CON	32	Overlay RDMA1 Memory Slow Control
1400B0F0	OVL_RDMA1_FIFO_CTRL	32	Overlay RDMA1 FIFO Control
1400B100	OVL_RDMA2_CTRL	32	Overlay RDMA2 Control
1400B108	OVL_RDMA2_MEM_GMC_SETTING1	32	Overlay RDMA2 Memory GMC Setting
1400B10C	OVL_RDMA2_MEM_SLOW_CON	32	Overlay RDMA2 Memory Slow Control
1400B110	OVL_RDMA2_FIFO_CTRL	32	Overlay RDMA2 FIFO Control
1400B120	OVL_RDMA3_CTRL	32	Overlay RDMA3 Control
1400B128	OVL_RDMA3_MEM_GMC_SETTING1	32	Overlay RDMA3 Memory GMC Setting
1400B12C	OVL_RDMA3_MEM_SLOW_CON	32	Overlay RDMA3 Memory Slow Control
1400B130	OVL_RDMA3_FIFO_CTRL	32	Overlay RDMA3 FIFO Control
1400B134	OVL_L0_Y2R_PARA_R0	32	Overlay L0 Y2R Conversion Parameter R0
1400B138	OVL_L0_Y2R_PARA_R1	32	Overlay L0 Y2R Conversion Parameter R1
1400B13C	OVL_L0_Y2R_PARA_G0	32	Overlay L0 Y2R Conversion Parameter G0
1400B140	OVL_L0_Y2R_PARA_G1	32	Overlay L0 Y2R Conversion Parameter G1
1400B144	OVL_L0_Y2R_PARA_B0	32	Overlay L0 Y2R Conversion Parameter B0
1400B148	OVL_L0_Y2R_PARA_B1	32	Overlay L0 Y2R Conversion Parameter B1
1400B14C	OVL_L0_Y2R_PARA_YUV_A_0	32	Overlay L0 Y2R Conversion Parameter Extended Add on YUV 0
1400B150	OVL_L0_Y2R_PARA_YUV_A_1	32	Overlay L0 Y2R Conversion Parameter Extended Add on YUV 1
1400B154	OVL_L0_Y2R_PARA_RGB_A_0	32	Overlay L0 Y2R Conversion Parameter Extended Add on RGB 0
1400B158	OVL_L0_Y2R_PARA_RGB_A_1	32	Overlay L0 Y2R Conversion Parameter Extended Add on RGB 1
1400B15C	OVL_L1_Y2R_PARA_R0	32	Overlay L1 Y2R Conversion Parameter R0
1400B160	OVL_L1_Y2R_PARA_R1	32	Overlay L1 Y2R Conversion Parameter R1
1400B164	OVL_L1_Y2R_PARA_G0	32	Overlay L1 Y2R Conversion Parameter G0
1400B168	OVL_L1_Y2R_PARA_G1	32	Overlay L1 Y2R Conversion Parameter G1

Address	Name	Width	Register Function
1400B16C	OVL_L1_Y2R_PARA_B0	32	Overlay L1 Y2R Conversion Parameter B0
1400B170	OVL_L1_Y2R_PARA_B1	32	Overlay L1 Y2R Conversion Parameter B1
1400B174	OVL_L1_Y2R_PARA_YUV_A_0	32	Overlay L1 Y2R Conversion Parameter Extended Add on YUV 0
1400B178	OVL_L1_Y2R_PARA_YUV_A_1	32	Overlay L1 Y2R Conversion Parameter Extended Add on YUV 1
1400B17C	OVL_L1_Y2R_PARA_RGB_A_0	32	Overlay L1 Y2R Conversion Parameter Extended Add on RGB 0
1400B180	OVL_L1_Y2R_PARA_RGB_A_1	32	Overlay L1 Y2R Conversion Parameter Extended Add on RGB 1
1400B184	OVL_L2_Y2R_PARA_R0	32	Overlay L2 Y2R Conversion Parameter R0
1400B188	OVL_L2_Y2R_PARA_R1	32	Overlay L2 Y2R Conversion Parameter R1
1400B18C	OVL_L2_Y2R_PARA_G0	32	Overlay L2 Y2R Conversion Parameter G0
1400B190	OVL_L2_Y2R_PARA_G1	32	Overlay L2 Y2R Conversion Parameter G1
1400B194	OVL_L2_Y2R_PARA_B0	32	Overlay L2 Y2R Conversion Parameter B0
1400B198	OVL_L2_Y2R_PARA_B1	32	Overlay L2 Y2R Conversion Parameter B1
1400B19C	OVL_L2_Y2R_PARA_YUV_A_0	32	Overlay L2 Y2R Conversion Parameter Extended Add on YUV 0
1400B1A0	OVL_L2_Y2R_PARA_YUV_A_1	32	Overlay L2 Y2R Conversion Parameter Extended Add on YUV 1
1400B1A4	OVL_L2_Y2R_PARA_RGB_A_0	32	Overlay L2 Y2R Conversion Parameter Extended Add on RGB 0
1400B1A8	OVL_L2_Y2R_PARA_RGB_A_1	32	Overlay L2 Y2R Conversion Parameter Extended Add on RGB 1
1400B1AC	OVL_L3_Y2R_PARA_R0	32	Overlay L3 Y2R Conversion Parameter R0
1400B1B0	OVL_L3_Y2R_PARA_R1	32	Overlay L3 Y2R Conversion Parameter R1
1400B1B4	OVL_L3_Y2R_PARA_G0	32	Overlay L3 Y2R Conversion Parameter G0
1400B1B8	OVL_L3_Y2R_PARA_G1	32	Overlay L3 Y2R Conversion Parameter G1
1400B1BC	OVL_L3_Y2R_PARA_B0	32	Overlay L3 Y2R Conversion Parameter B0
1400B1C0	OVL_L3_Y2R_PARA_B1	32	Overlay L3 Y2R Conversion Parameter B1
1400B1C4	OVL_L3_Y2R_PARA_YUV_A_0	32	Overlay L3 Y2R Conversion Parameter Extended Add on YUV 0
1400B1C8	OVL_L3_Y2R_PARA_YUV_A_1	32	Overlay L3 Y2R Conversion Parameter Extended Add on YUV 1
1400B1CC	OVL_L3_Y2R_PARA_RGB_A_0	32	Overlay L3 Y2R Conversion Parameter Extended Add on RGB 0
1400B1D0	OVL_L3_Y2R_PARA_RGB_A_1	32	Overlay L3 Y2R Conversion Parameter Extended Add on RGB 1
1400B1D4	OVL_DEBUG_MON_SEL	32	Overlay Debug Monitor Select

Address	Name	Width	Register Function
1400B1E0	OVL_RDMA0_MEM_GMC_SETTING2	32	Overlay RDMA0 Memory GMC Setting
1400B1E4	OVL_RDMA1_MEM_GMC_SETTING2	32	Overlay RDMA1 Memory GMC Setting
1400B1E8	OVL_RDMA2_MEM_GMC_SETTING2	32	Overlay RDMA2 Memory GMC Setting
1400B1EC	OVL_RDMA3_MEM_GMC_SETTING2	32	Overlay RDMA3 Memory GMC Setting
1400B1F0	OVL_RDMA_BURST_CON0	32	Overlay RDMA Burst Control
1400B1F4	OVL_RDMA_BURST_CON1	32	Overlay RDMA Burst Control
1400B1F8	OVL_RDMA_GREQ_NUM	32	Overlay RDMA GREQ Number
1400B1FC	OVL_RDMA_GREQ_URG_NUM	32	Overlay RDMA GREQ Number
1400B200	OVL_DUMMY_REG	32	Overlay Dummy Register
1400B208	OVL_GDRDY_PRD	32	Overlay SMI GDRDY Period
1400B20C	OVL_RDMA_ULTRA_SRC	32	Overlay RDMA Ultra SRC
1400B210	OVL_RDMA0_BUF_LOW	32	Overlay RDMA BUF Low
1400B214	OVL_RDMA1_BUF_LOW	32	Overlay RDMA BUF Low
1400B218	OVL_RDMA2_BUF_LOW	32	Overlay RDMA BUF Low
1400B21C	OVL_RDMA3_BUF_LOW	32	Overlay RDMA BUF Low
1400B230	OVL_SMI_DBG	32	Overlay SMI Arbiter Debug Monitor
1400B234	OVL_GREQ_LAYER_CNT	32	Overlay Layer GREQ Counter
1400B238	OVL_GDRDY_PRD_NUM	32	Overlay SMI GDRDY Period Number
1400B240	OVL_FLOW_CTRL_DBG	32	Overlay Flow Control Debug Monitor
1400B244	OVL_ADDCON_DBG	32	Overlay Address Control Debug
1400B24C	OVL_RDMA0_DBG	32	Overlay RDMA0 Debug Monitor
1400B250	OVL_RDMA1_DBG	32	Overlay RDMA1 Debug Monitor
1400B254	OVL_RDMA2_DBG	32	Overlay RDMA2 Debug Monitor
1400B258	OVL_RDMA3_DBG	32	Overlay RDMA3 Debug Monitor
1400B25C	OVL_L0_CLR	32	Overlay Layer 0 Constant Color
1400B260	OVL_L1_CLR	32	Overlay Layer 1 Constant Color
1400B264	OVL_L2_CLR	32	Overlay Layer 2 Constant Color
1400B268	OVL_L3_CLR	32	Overlay Layer 3 Constant Color
1400B26C	OVL_LC_CLR	32	Overlay Constant Layer Color
1400B270	OVL_CRC	32	Overlay CRC
1400B280	OVL_LC_CON	32	Overlay Constant Layer Control
1400B284	OVL_LC_SRCKEY	32	Overlay Constant Layer Source Key
1400B288	OVL_LC_SRC_SIZE	32	Overlay Layer C Source Size
1400B28C	OVL_LC_OFFSET	32	Overlay Layer C Offset
1400B290	OVL_LC_SRC_SEL	32	Overlay Constant Layer Source Selection

Address	Name	Width	Register Function
1400B29C	OVL_BANK_CON	32	Overlay Bank Control
1400B2A0	OVL_FUNC_DCM0	32	Overlay Functional DCM0 Control
1400B2A4	OVL_FUNC_DCM1	32	Overlay Functional DCM1 Control
1400BFC0	OVL_SECURE	32	Overlay Layer Secure Bit

1400B000 OVL_STA **Overlay Status Monitor** **0000001E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RDMA3_IDLE	RDMA2_IDLE	RDMA1_IDLE	RDMA0_IDLE	OVL_RUN
Type												RU	RU	RU	RU	RU
Reset												1	1	1	1	0

Bit(s)	Mnemonic	Name	Description
4		RDMA3_IDLE	**Status of overlay RDMA3** 0: RDMA is in running. 1: Overlay RDMA are all idle.
3		RDMA2_IDLE	**Status of overlay RDMA2** 0: RDMA is in running. 1: Overlay RDMA are all idle.
2		RDMA1_IDLE	**Status of overlay RDMA1** 0: RDMA is in running. 1: Overlay RDMA are all idle.
1		RDMA0_IDLE	**Status of overlay RDMA0** 0: RDMA is in running. 1: Overlay RDMA are all idle.
0		OVL_RUN	**Status of overlay engine** 0: Overlay is idle. 1: Overlay is running.

1400B004 OVL_INTEN **Overlay Interrupt Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ABNORMAL_SOF_INTEN	RDMA3_SMI_UNDERFLOW_INTEN	RDMA2_SMI_UNDERFLOW_INTEN	RDMA1_SMI_UNDERFLOW_INTEN	RDMA0_SMI_UNDERFLOW_INTEN	RDMA3_EOF_ABNORMAL_INTEN	RDMA2_EOF_ABNORMAL_INTEN	RDMA1_EOF_ABNORMAL_INTEN	RDMA0_EOF_ABNORMAL_INTEN	OVL_FME_HWRST_DONE_INTEN	OVL_FME_SWRST_DONE_INTEN	OVL_FME_UND_INTEN	OVL_FME_CPL_INTEN	OVL_REG_CMT_INTEN
Type			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13		ABNORMAL_SOF_INTEN	**Control abnormal SOF interrupt**
12		RDMA3_SMI_UNDERFLOW_INTEN	**Control RDMA3 SMI Underflow interrupt** 0: Disable RDMA3 SMI data underflow interrupt 1: Enable RDMA3 SMI data underflow interrupt
11		RDMA2_SMI_UNDERFLOW_INTEN	**Control RDMA2 SMI Underflow interrupt** 0: Disable RDMA2 SMI data underflow interrupt 1: Enable RDMA2 SMI data underflow interrupt
10		RDMA1_SMI_UNDERFLOW_INTEN	**Control RDMA1 SMI underflow interrupt** 0: Disable RDMA1 SMI data underflow interrupt 1: Enable RDMA1 SMI data underflow interrupt
9		RDMA0_SMI_UNDERFLOW_INTEN	**Control RDMA0 SMI underflow interrupt** 0: Disable RDMA0 SMI data underflow interrupt 1: Enable RDMA0 SMI data underflow interrupt
8		RDMA3_EOF_ABNORMAL_INTEN	**Control RDMA3 EOF abnormal interrupt** 0: Disable RDMA3 EOF abnormal interrupt 1: Enable RDMA3 EOF abnormal interrupt
7		RDMA2_EOF_ABNORMAL_INTEN	**Control RDMA2 EOF abnormal interrupt** 0: Disable RDMA2 EOF abnormal interrupt 1: Enable RDMA2 EOF abnormal interrupt
6		RDMA1_EOF_ABNORMAL_INTEN	**Control RDMA1 EOF abnormal interrupt** 0: Disable RDMA1 EOF abnormal interrupt 1: Enable RDMA1 EOF abnormal interrupt
5		RDMA0_EOF_ABNORMAL_INTEN	**Control RDMA0 EOF abnormal interrupt** 0: Disable RDMA0 EOF abnormal interrupt 1: Enable RDMA0 EOF abnormal interrupt
4		OVL_FME_HWRST_DONE_INTEN	**Control frame HW reset done interrupt** 0: Disable frame HW reset done interrupt 1: Enable frame HW reset done interrupt
3		OVL_FME_SWRST_DONE_INTEN	**Control frame SW reset done interrupt** 0: Disable frame SW reset done interrupt 1: Enable frame SW reset done interrupt
2		OVL_FME_UND_INTEN	**Control frame underflow interrupt** 0: Disable frame underflow interrupt 1: Enable frame underflow interrupt
1		OVL_FME_CPL_INTEN	**Control frame complete interrupt** 0: Disable frame complete interrupt 1: Enable frame complete interrupt
0		OVL_REG_CMT_INTEN	**Control register setting complete interrupt** 0: Disable register commit interrupt 1: Enable register commit interrupt

1400B008 OVL_INTSTA **Overlay Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**ABNORMAL_SOF_INTSTA**	**RDMA3_SMI_UNDERFLOW_INTSTA**	**RDMA2_SMI_UNDERFLOW_INTSTA**	**RDMA1_SMI_UNDERFLOW_INTSTA**	**RDMA0_SMI_UNDERFLOW_INTSTA**	**RDMA3_EOF_ABNORMAL_INTSTA**	**RDMA2_EOF_ABNORMAL_INTSTA**	**RDMA1_EOF_ABNORMAL_INTSTA**	**RDMA0_EOF_ABNORMAL_INTSTA**	**OVL_FME_HWRST_DONE_INTSTA**	**OVL_FME_SWRST_DONE_INTSTA**	**OVL_FME_UND_INTSTA**	**OVL_FME_CPL_INTSTA**	**OVL_REG_CMT_INTSTA**

Type			A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13		ABNORMAL_SOF_INTSTA	
12		RDMA3_SMI_UNDERFLOW_INTSTA	**RDMA3 SMI status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA3 SMI data are not underflow. 1: RDMA3 SMI data are underflow.
11		RDMA2_SMI_UNDERFLOW_INTSTA	**RDMA2 SMI status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA2 SMI data are not underflow. 1: RDMA2 SMI data are underflow.
10		RDMA1_SMI_UNDERFLOW_INTSTA	**RDMA1 SMI status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA1 SMI data are not underflow. 1: RDMA1 SMI data are underflow.
9		RDMA0_SMI_UNDERFLOW_INTSTA	**RDMA0 SMI status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA0 SMI data are not underflow. 1: RDMA0 SMI data are underflow.
8		RDMA3_EOF_ABNORMAL_INTSTA	**RDMA3 status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA3 complete normally 1: RDMA3 not complete till EOF
7		RDMA2_EOF_ABNORMAL_INTSTA	**RDMA2 status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA2 complete normally 1: RDMA2 not complete till EOF
6		RDMA1_EOF_ABNORMAL_INTSTA	**RDMA1 status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA1 complete normally 1: RDMA1 not complete till EOF
5		RDMA0_EOF_ABNORMAL_INTSTA	**RDMA0 status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA0 complete normally 1: RDMA0 not complete till EOF
4		OVL_FME_HWRST_DONE_INTSTA	**Overlay HW reset done status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: No HW reset/HW reset is not done. 1: HW reset is done.
3		OVL_FME_SWRST_DONE_INTSTA	**Overlay SW reset done status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: No SW reset/SW reset is not done. 1: SW reset is done.
2		OVL_FME_UND_INTSTA	**Overlay frame underflow status** Controls interrupt write-clear. Cleared by writing 0;

Bit(s)	Mnemonic	Name	Description
			writing 1 is useless. 0: Frame complete w/o underflow 1: Frame not complete w/ underflow
1		OVL_FME_CPL_INTSTA	**Overlay frame complete status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: Frame not complete 1: Frame complete
0		OVL_REG_CMT_INTSTA	**Overlay register commit status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: Regsiter is not set from shadow register to working register. 1: Register is set to working register done.

1400B00C OVL_EN **Overlay Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																IGNORE_ABNORMAL_SOF
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							HG_FSMI_CK_ON	HG_FOVL_CK_ON								OVL_EN
Type							RW	RW								RW
Reset							0	0								0

Bit(s)	Mnemonic	Name	Description
16		IGNORE_ABNORMAL_SOF	
9		HG_FSMI_CK_ON	
8		HG_FOVL_CK_ON	
0	**OVEN**	OVL_EN	**Enables overlay engine** 0: Disable overlay 1: Enable overlay

1400B010 OVL_TRIG **Overlay Trigger** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							CRC_CLR	CRC_EN								OVL_SW_TRIG
Type							RW	RW								RW
Reset							0	0								0

Bit(s)	Mnemonic	Name	Description
9		CRC_CLR	
8		CRC_EN	
0	**OVTR**	OVL_SW_TRIG	**SW trigger to enable overlay engine** 0: When using HW trigger (SOF), this bit should be 0. 1: SW control to enable overlay engine.

1400B014 OVL_RST **Overlay Reset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OVL_SMI_IOBUF_HARD_RST	OVL_SMI_IOBUF_RST	OVL_SMI_HARD_RST	OVL_SMI_RST												
Type	RW	RW	RW	RW												
Reset	0	0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																OVL_RST
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
31		OVL_SMI_IOBUF_HARD_RST	**OVL is forced to reset when SMI BUSY hang issue occurs (careful)**
30		OVL_SMI_IOBUF_RST	
29		OVL_SMI_HARD_RST	
28		OVL_SMI_RST	
0		OVL_RST	**Overlay SW reset control for engine (high active)** 1: Reset engine

1400B020 OVL_ROI_SIZE **Overlay ROI Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				ROI_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				ROI_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**ROIH**	ROI_H	**Overlay ROI width** Range: 1 ~ 8191. For 3D display, this value should be 2 ~ 8191.

Bit(s)	Mnemonic	Name	Description
12:0	**ROIW**	ROI_W	**Overlay ROI width** Range: 1 ~ 8191. For 3D display, this value should be 2 ~ 8191.

1400B024 OVL_DATAPATH_CON **Overlay Datapath Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									RDMA3_OUT_SEL	RDMA2_OUT_SEL	RDMA1_OUT_SEL	RDMA0_OUT_SEL			PQ_OUT_SEL	
Type									OTHER	OTHER	OTHER	OTHER			OTHER	
Reset									0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OVL_GAMMA_OUT	ADOBE_LAYER		ADOBE_MODE	L3_GPU_MODE	L2_GPU_MODE	L1_GPU_MODE	L0_GPU_MODE					OUTPUT_NO_RND	BGCLR_IN_SEL	OVL_RANDOM_BGCLR_EN	LAYER_SMI_ID_EN
Type	RW	RW		RW	RW	RW	RW	RW					RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
23	**RDMA3SEL**	RDMA3_OUT_SEL	**Selects output path of RDMA3** 0: OVL Layer 3 1: PQ direct link output
22	**RDMA2SEL**	RDMA2_OUT_SEL	**Selects output path of RDMA2** 0: OVL Layer 2 1: PQ direct link output
21	**RDMA1SEL**	RDMA1_OUT_SEL	**Selects output path of RDMA1** 0: OVL Layer 1 1: PQ direct link output
20	**RDMA0SEL**	RDMA0_OUT_SEL	**Selects output path of RDMA0** 0: OVL Layer 0 1: PQ direct link output
17:16	**PQSEL**	PQ_OUT_SEL	**Selects PQ direct link output data** 00: RDMA0 01: RDMA1 10: RDMA2 11: RDMA3
15	**OVL_GAMMA_OUT**	OVL_GAMMA_OUT	**Wide-gamut OVL output GAMMA table path** (shares GAMMA-table with layer Adobe_mode) 0: Disable OVL output GAMMA table 1: Enable OVL output GAMMA table
14:13	**ADOBE_LAYER**	ADOBE_LAYER	**Selects wide-gamut layer Adobe** 0: Select Layer 0 adobe_path 1: Select Layer 1 adobe_path 2: Select Layer 2 adobe_path 3: Select Layer 3 adobe_path
12	**ADOBE**	ADOBE_MODE	**Wide-gamut layer Adobe mode** (shares GAMMA-table with ovl_gamma_out mode)

Bit(s)	Mnemonic	Name	Description
			0: Disable layer Adobe path 1: Enable layer Adobe path
11	**L3_GPU**	L3_GPU_MODE	**Wide-gamut Layer 3 GPU path mode** 0: Disable Layer 3 GPU path 1: Enable Layer 3 GPU path
10	**L2_GPU**	L2_GPU_MODE	**Wide-gamut Layer 2 GPU path mode** 0: Disable Layer 2 GPU path 1: Enable Layer 2 GPU path
9	**L1_GPU**	L1_GPU_MODE	**Wide-gamut Layer 1 GPU path mode** 0: Disable Layer 1 GPU path 1: Enable Layer 1 GPU path
8	**L0_GPU**	L0_GPU_MODE	**Wide-gamut Layer 0 GPU path mode** 0: Disable Layer 0 GPU path 1: Enable Layer 0 GPU path
3		OUTPUT_NO_RND	
2		BGCLR_IN_SEL	**OVL BGCLR direct link path** 0: Disable OVL BGCLR direct link input 1: Enable OVL BGCLR direct link input
1		OVL_RANDOM_BGCLR_EN	**When OVL_RANDOM_BGCLR_EN=1, layer_en[i] should be set to 0 to allow the background color to pass through the Blend engine.** 0: Disable random background color pattern 1: Enable random background color pattern
0	**LAYER_SMI_ID_EN**	LAYER_SMI_ID_E N	**Supports OVL SMI ID function** 0: Disable SMI ID 1: Enable SMI ID

1400B028 OVL_ROI_BGCLR **Overlay Background Color** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24	**BGDA**	ALPHA	Alpha component of ROI window background color
23:16	**BGDR**	RED	Red component of ROI window background color
15:8	**BGDG**	GREEN	Green component of ROI window background color
7:0	**BGDB**	BLUE	Blue component of ROI window background color

1400B02C OVL_SRC_CON **Overlay Source Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												LC_EN	L3_EN	L2_EN	L1_EN	L0_EN
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4	**LCEN**	LC_EN	**Set up this bit to enable overlay constant layer.** 0: Disable constant layer 1: Enable constant layer
3	**L3EN**	L3_EN	**Set up this bit to enable overlay Layer 3.** 0: Disable Layer 3 1: Enable Layer 3
2	**L2EN**	L2_EN	**Set up this bit to enable overlay Layer 2.** 0: Disable Layer 2 1: Enable Layer 2
1	**L1EN**	L1_EN	**Set up this bit to enable overlay Layer 1.** 0: Disable Layer 1 1: Enable Layer 1
0	**L0EN**	L0_EN	**Set up this bit to enable overlay Layer 0.** 0: Disable Layer 0 1: Enable Layer 0

1400B030 OVL_L0_CON **Overlay Layer 0 Control** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSTKEY_EN	SRCKEY_EN	LAYER_SRC		MTX_EN	MTX_AUTO_DIS	RGB_SWAP	BYTE_SWAP	CLRFMT_MAN	R_FIRST	LANDSCAPE	EN_3D	INT_MTX_SEL			
Type	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLRFMT				EXT_MTX_EN	HORIZONTAL_FLIP_EN	VERTICAL_FLIP_EN	ALPHA_EN	ALPHA							
Type	RW				OTHER	RW	RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**DKEN**	DSTKEY_EN	**Enables destination color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable destination color key 1: Enable destination color key
30	**SKEN**	SRCKEY_EN	**Enables source color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable source color key 1: Enable source color key
29:28	**LSRC**	LAYER_SRC	**Selects layer pixel from memory/constant color/SCL/PQ** 00: Layer pixel from memory RDMA0 01: Layer pixel from constant color

Bit(s)	Mnemonic	Name	Description
			10: Layer pixel from UFOd 11: Layer pixel from PQ
27		MTX_EN	
26		MTX_AUTO_DIS	
25	**RGSW**	RGB_SWAP	**No use**
24	**BTSW**	BYTE_SWAP	**Swaps unified color format** 0: RGB565, BGR888, BGRA8888, ABGR8888, UYVY, YUYV 1: BGR565, RGB888, RGBA8888, ARGB8888, VYUY, YVYU
23		CLRFMT_MAN	
22		R_FIRST	**Right eye image first when in 3D mode** 0: Show left eye image first in 3D mode 1: Show right eye image first in 3D mode
21		LANDSCAPE	**Enables 3D landscape mode** 0: 3D portrait mode 1: 3D landscape mode
20		EN_3D	**Enables 3D mode** 0: 2D mode 1: 3D mode
19:16	**MTX**	INT_MTX_SEL	**Selects color matrix table** 0000: MTX_RGB_TO_JPEG 0010: MTX_RGB_TO_BT601 0011: MTX_RGB_TO_BT709 0100: MTX_JPEG_TO_RGB 0110: MTX_BT601_TO_RGB 0111: MTX_BT709_TO_RGB 1000: MTX_JPEG_TO_BT601 1001: MTX_JPEG_TO_BT709 1010: MTX_BT601_TO_JPEG 1011: MTX_BT709_TO_JPEG 1100: MTX_BT709_TO_BT601 1101: MTX_BT601_TO_BT709 Others: HW default (JPEG_TO_RGB)
15:12	**CFMT**	CLRFMT	**//--OLD define for reference only** 0000: RGB888 0001: RGB565 0010: ARGB8888 0011: PARGB8888 0100: xARGB8888 1000: YUYV 1001: UYVY 1010: YVYU 1011: VYUY 1111: YUV444 Others: Reserved color format 0000: RGB565 0001: RGB888 0010: RGBA8888/BGRA8888 0011: ARGB8888/ABGR8888 0100: UVVY, VYUY 0101: YUYV, YVYU
11	**MTXEN**	EXT_MTX_EN	**Enables external programmable coeff** 0: Matrix coeff 1: Programmable coeff
10	**HFE**	HORIZONTAL_FLI	**Enables horizontal flip**

Bit(s)	Mnemonic	Name	Description
		P_EN	0: Disable horizontal flip 1: Enable horizontal flip
9	**VFE**	VERTICAL_FLIP_ EN	**Enables vertical flip** 0: Disable vertical flip 1: Enable vertical flip
8	**AEN**	ALPHA_EN	**Enables alpha blending** 0: Disable alpha blending 1: Enable alpha blending
7:0	**APHA**	ALPHA	**Constant alpha value**

1400B034 OVL_Lo_SRCKEY **Overlay Layer 0 Source Key** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SKEY**	SRCKEY	**Layer source color key** Active when source color key is enabled.

1400B038 OVL_Lo_SRC_SIZE **Overlay Layer 0 Source Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				Lo_SRC_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				Lo_SRC_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**LoH**	Lo_SRC_H	**Layer source height** Range: 0 ~ 8191
12:0	**LoW**	Lo_SRC_W	**Layer source width** Range: 0 ~ 8191

1400B03C OVL_Lo_OFFSET **Overlay Layer 0 Offset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				Lo_YOFF												

Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				Lo_XOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**LoH**	Lo_YOFF	**Layer vertical Y offset** Range: 0 ~ 8191
12:0	**LoXO**	Lo_XOFF	**Layer horizontal X offset** Range: 0 ~ 8191

1400BF40 OVL_Lo_ADDR Overlay Layer 0 Memory Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Lo_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Lo_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**LoAD**	Lo_ADDR	Layer memory buffer address

1400B044 OVL_Lo_PITCH Overlay Layer 0 Pitch 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SURFL_EN	Lo_BLEND_RND_SHT		Lo_CONST_BLD	Lo_DRGB_SEL_EXT	Lo_DA_SEL_EXT	Lo_SRGB_SEL_EXT	Lo_SA_SEL_EXT	Lo_DRGB_SEL		Lo_DA_SEL		Lo_SRGB_SEL		Lo_SA_SEL	
Type	RW	RW		RW	RW	RW	RW	RW	RW		RW		RW		RW	
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Lo_SRC_PITCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**LoSP**	SURFL_EN	**Enables layer surface dlinger alpha_blending** 0: Disable surface flinger alpha_blending 1: Enable surface flinger alpha_blending
30		Lo_BLEND_RND_SHT	
28		Lo_CONST_BLD	
27		Lo_DRGB_SEL_EXT	**Selects layer destination_RGB alpha**
26		Lo_DA_SEL_EXT	**Selects layer destination_Alpha alpha**

Bit(s)	Mnemonic	Name	Description
25		Lo_SRGB_SEL_EX T	**Selects layer source_RGB alpha**
24		Lo_SA_SEL_EXT	**Selects layer source_Alpha alpha**
23:22	**LoSP**	Lo_DRGB_SEL	**Selects layer destination_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
21:20	**LoSP**	Lo_DA_SEL	**Selects layer destination_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
19:18	**LoSP**	Lo_SRGB_SEL	**Selects layer source_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
17:16	**LoSP**	Lo_SA_SEL	**Selects layer source_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
15:0	**LoSP**	Lo_SRC_PITCH	**Layer source pitch**

1400B048 OVL_Lo_TILE **Overlay Layer 0 Tile Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TILE_HORI_BLOCK_NUM										TILE_EN	TILE_WIDTH_SEL	TILE_HEIGHT			
Type	OTHER										OTHER	OTHER	OTHER			
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TILE_HEIGHT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**TILE_BLKS**	TILE_HORI_BLOCK_NUM	**Number of horizontal blocks**
21	**TILE_EN**	TILE_EN	**Enables tile mode** 0: Disable 1: Enable
20	**TILE_W**	TILE_WIDTH_SEL	**Width of tile** 0: 16 1: 32
19:0	**TILE_H**	TILE_HEIGHT	**Height of source tile mode**

1400B04C OVL_Lo_CLIP **Overlay Layer 0 Clip** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	Lo_SRC_BOTTOM_CLIP								Lo_SRC_TOP_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Lo_SRC_RIGHT_CLIP								Lo_SRC_LEFT_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**Lo_SRC_BOTTOM_CLIP**	Lo_SRC_BOTTOM_CLIP	Layer 0 bottom clip
23:16	**Lo_SRC_TOP_CLI P**	Lo_SRC_TOP_CLI P	Layer 0 top clip
15:8	**Lo_SRC_RIGHT_C LIP**	Lo_SRC_RIGHT_C LIP	Layer 0 right clip
7:0	**Lo_SRC_LEFT_CL IP**	Lo_SRC_LEFT_CL IP	Layer 0 left clip

1400B050 OVL_L1_CON **Overlay Layer 1 Control** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSTKEY_EN	SRCKEY_EN	LAYER_SRC		MTX_EN	MTX_AUTO_DIS	RGB_SWAP	BYTE_SWAP	CLRFMT_MAN	R_FIRST	LANDSCAPE	EN_3D	INT_MTX_SEL			
Type	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLRFMT				EXT_MTX_EN	HORIZONTAL_FLIP_EN	VERTICAL_FLIP_EN	ALPHA_EN	ALPHA							
Type	RW				OTHER	RW	RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**DKEN**	DSTKEY_EN	**Enables destination color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable destination color key 1: Enable destination color key
30	**SKEN**	SRCKEY_EN	**Enables source color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable source color key 1: Enable source color key
29:28	**LSRC**	LAYER_SRC	**Selects layer pixel from memory/constant color/SCL/PQ** 00: Layer pixel from memory RDMA1 01: Layer pixel from constant color 10: Layer pixel from UFOd 11: Layer pixel from PQ
27		MTX_EN	
26		MTX_AUTO_DIS	
25	**RGSW**	RGB_SWAP	**No use**
24	**BTSW**	BYTE_SWAP	**Swaps unified color format** 0: RGB565, BGR888, BGRA8888, ABGR8888, UYVY, YUYV

Bit(s)	Mnemonic	Name	Description
			1: BGR565, RGB888, RGBA8888, ARGB8888, VYUY, YVYU
23		CLRFMT_MAN	
22		R_FIRST	**Right eye image first when in 3D mode** 0: Show left eye image first in 3D mode 1: Show right eye image first in 3D mode
21		LANDSCAPE	**Enables 3D landscape mode** 0: 3D portrait mode 1: 3D landscape mode
20		EN_3D	**Enables 3D mode** 0: 2D mode 1: 3D mode
19:16	**MTX**	INT_MTX_SEL	**Selects color matrix table** 0000: MTX_RGB_TO_JPEG 0010: MTX_RGB_TO_BT601 0011: MTX_RGB_TO_BT709 0100: MTX_JPEG_TO_RGB 0110: MTX_BT601_TO_RGB 0111: MTX_BT709_TO_RGB 1000: MTX_JPEG_TO_BT601 1001: MTX_JPEG_TO_BT709 1010: MTX_BT601_TO_JPEG 1011: MTX_BT709_TO_JPEG 1100: MTX_BT709_TO_BT601 1101: MTX_BT601_TO_BT709 Others: HW default (JPEG_TO_RGB)
15:12	**CFMT**	CLRFMT	**//--OLD define for reference only** 0000: RGB888 0001: RGB565 0010: ARGB8888 0011: PARGB8888 0100: xARGB8888 1000: YUYV 1001: UYVY 1010: YVYU 1011: VYUY 1111: YUV444 Others: Reserved color format 0000: RGB565 0001: RGB888 0010: RGBA8888/BGRA8888 0011: ARGB8888/ABGR8888 0100: UVVY, VYUY 0101: YUYV, YVYU
11	**MTXEN**	EXT_MTX_EN	**Enables external programmable coeff** 0: Matrix coeff 1: Programmable coeff
10	**HFE**	HORIZONTAL_FLIP_EN	**Enables horizontal flip** 0: Disable horizontal flip 1: Enable horizontal flip
9	**VFE**	VERTICAL_FLIP_ EN	**Enables vertical flip** 0: Disable vertical flip 1: Enable vertical flip
8	**AEN**	ALPHA_EN	**Enables alpha blending** 0: Disable alpha blending 1: Enable alpha blending
7:0	**APHA**	ALPHA	**Constant alpha value**

Bit(s)	Mnemonic	Name	Description

1400B054 OVL_L1_SRCKEY Overlay Layer 1 Source Key 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SKEY**	SRCKEY	**Layer source color key** Active when source color key is enabled.

1400B058 OVL_L1_SRC_SIZE Overlay Layer 1 Source Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L1_SRC_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L1_SRC_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**L1H**	L1_SRC_H	**Layer source height** Range: 0 ~ 8191
12:0	**L1W**	L1_SRC_W	**Layer source width** Range: 0 ~ 8191

1400B05C OVL_L1_OFFSET Overlay Layer 1 Offset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L1_YOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L1_XOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**L1H**	L1_YOFF	**Layer vertical Y offset**

Bit(s)	Mnemonic	Name	Description
12:0	**L1XO**	L1_XOFF	Range: 0 ~ 8191 **Layer horizontal X offset** Range: 0 ~ 8191

1400BF60 OVL_L1_ADDR **Overlay Layer 1 Memory Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L1_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L1_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**L1AD**	L1_ADDR	Layer memory buffer address

1400B064 OVL_L1_PITCH **Overlay Layer 1 Pitch** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SURFL_EN	L1_BLEND_RND_SHT		L1_CONST_BLD	L1_DRGB_SEL_EXT	L1_DA_SEL_EXT	L1_SRGB_SEL_EXT	L1_SA_SEL_EXT	L1_DRGB_SEL		L1_DA_SEL		L1_SRGB_SEL		L1_SA_SEL	
Type	RW	RW		RW	RW	RW	RW	RW	RW		RW		RW		RW	
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L1_SRC_PITCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**L1SP**	SURFL_EN	**Enables layer surface dlinger alpha_blending** 0: Disable surface flinger alpha_blending 1: Enable surface flinger alpha_blending
30		L1_BLEND_RND_SHT	
28		L1_CONST_BLD	
27		L1_DRGB_SEL_EXT	**Selects layer destination_RGB alpha**
26		L1_DA_SEL_EXT	**Selects layer destination_Alpha alpha**
25		L1_SRGB_SEL_EXT	**Selects layer source_RGB alpha**
24		L1_SA_SEL_EXT	**Selects layer source_Alpha alpha**
23:22	**L1SP**	L1_DRGB_SEL	**Selects layer destination_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
21:20	**L1SP**	L1_DA_SEL	**Selects layer destination_Alpha alpha** 00: ONE 01: Src_Alpha

Bit(s)	Mnemonic	Name	Description
			10: 1-Src_Alpha 11: Reserved
19:18	**L1SP**	L1_SRGB_SEL	**Selects layer source_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
17:16	**L1SP**	L1_SA_SEL	**Selects layer source_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
15:0	**L1SP**	L1_SRC_PITCH	**Layer source pitch**

1400B068 OVL_L1_TILE **Overlay Layer 1 Tile Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TILE_HORI_BLOCK_NUM										TILE_EN	TILE_WIDTH_SEL	TILE_HEIGHT			
Type	OTHER										OTHER	OTHER	OTHER			
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TILE_HEIGHT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**TILE_BLKS**	TILE_HORI_BLOCK_NUM	**Number of horizontal blocks**
21	**TILE_EN**	TILE_EN	**Enables tile mode** 0: Disable 1: Enable
20	**TILE_W**	TILE_WIDTH_SEL	**Width of tile** 0: 16 1: 32
19:0	**TILE_H**	TILE_HEIGHT	**Height of source tile mode**

1400B06C OVL_L1_CLIP **Overlay Layer 1 Clip** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L1_SRC_BOTTOM_CLIP								L1_SRC_TOP_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L1_SRC_RIGHT_CLIP								L1_SRC_LEFT_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
31:24	**L1_SRC_BOTTOM_CLIP**	L1_SRC_BOTTOM_CLIP	Layer 1 bottom clip
23:16	**L1_SRC_TOP_CLIP**	L1_SRC_TOP_CLIP	Layer 1 top clip
15:8	**L1_SRC_RIGHT_CLIP**	L1_SRC_RIGHT_CLIP	Layer 1 right clip
7:0	**L1_SRC_LEFT_CLIP**	L1_SRC_LEFT_CLIP	Layer 1 left clip

1400B070 OVL_L2_CON **Overlay Layer 2 Control** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSTKEY_EN	SRCKEY_EN	LAYER_SRC		MTX_EN	MTX_AUTO_DIS	RGB_SWAP	BYTE_SWAP	CLRFMT_MAN	R_FIRST	LANDSCAPE	EN_3D	INT_MTX_SEL			
Type	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLRFMT				EXT_MTX_EN	HORIZONTAL_FLIP_EN	VERTICAL_FLIP_EN	ALPHA_EN	ALPHA							
Type	RW				OTHER	RW	RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**DKEN**	DSTKEY_EN	**Enables destination color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable destination color key 1: Enable destination color key
30	**SKEN**	SRCKEY_EN	**Enables source color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable source color key 1: Enable source color key
29:28	**LSRC**	LAYER_SRC	**Selects layer pixel from memory/constant color/SCL/PQ** 00: Layer pixel from memory RDMA2 01: Layer pixel from constant color 10: Layer pixel from UFOd 11: Layer pixel from PQ
27		MTX_EN	
26		MTX_AUTO_DIS	
25	**RGSW**	RGB_SWAP	**No use**
24	**BTSW**	BYTE_SWAP	**Swaps unified color format** 0: RGB565, BGR888, BGRA8888, ABGR8888, UYVY, YUYV 1: BGR565, RGB888, RGBA8888, ARGB8888, VYUY, YVYU
23		CLRFMT_MAN	
22		R_FIRST	**Right eye image first when in 3D mode** 0: Show left eye image first in 3D mode 1: Show right eye image first in 3D mode
21		LANDSCAPE	**Enables 3D landscape mode** 0: 3D portrait mode 1: 3D landscape mode

Bit(s)	Mnemonic	Name	Description
20		EN_3D	**Enables 3D mode** 0: 2D mode 1: 3D mode
19:16	**MTX**	INT_MTX_SEL	**Selects color matrix table** 0000: MTX_RGB_TO_JPEG 0010: MTX_RGB_TO_BT601 0011: MTX_RGB_TO_BT709 0100: MTX_JPEG_TO_RGB 0110: MTX_BT601_TO_RGB 0111: MTX_BT709_TO_RGB 1000: MTX_JPEG_TO_BT601 1001: MTX_JPEG_TO_BT709 1010: MTX_BT601_TO_JPEG 1011: MTX_BT709_TO_JPEG 1100: MTX_BT709_TO_BT601 1101: MTX_BT601_TO_BT709 Others: HW default (JPEG_TO_RGB)
15:12	**CFMT**	CLRFMT	**//--OLD define for reference only** 0000: RGB888 0001: RGB565 0010: ARGB8888 0011: PARGB8888 0100: xARGB8888 1000: YUYV 1001: UYVY 1010: YVYU 1011: VYUY 1111: YUV444 Others: Reserved color format 0000: RGB565 0001: RGB888 0010: RGBA8888/BGRA8888 0011: ARGB8888/ABGR8888 0100: UVVY, VYUY 0101: YUYV, YVYU
11	**MTXEN**	EXT_MTX_EN	**Enables external programmable coeff** 0: Matrix coeff 1: Programmable coeff
10	**HFE**	HORIZONTAL_FLIP_EN	**Enables horizontal flip** 0: Disable horizontal flip 1: Enable horizontal flip
9	**VFE**	VERTICAL_FLIP_ EN	**Enables vertical flip** 0: Disable vertical flip 1: Enable vertical flip
8	**AEN**	ALPHA_EN	**Enables alpha blending** 0: Disable alpha blending 1: Enable alpha blending
7:0	**APHA**	ALPHA	**Constant alpha value**

1400B074 OVL_L2_SRC_KEY **Overlay Layer 2 Source Key** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SKEY**	SRCKEY	**Layer source color key** Active when source color key is enabled.

1400B078 OVL_L2_SRC_SIZE — Overlay Layer 2 Source Size — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L2_SRC_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L2_SRC_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**L2H**	L2_SRC_H	**Layer source height** Range: 0 ~ 8191
12:0	**L2W**	L2_SRC_W	**Layer source width** Range: 0 ~ 8191

1400B07C OVL_L2_OFFSET — Overlay Layer 2 Offset — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L2_YOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L2_XOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**L2H**	L2_YOFF	**Layer vertical Y offset** Range: 0 ~ 8191
12:0	**L2XO**	L2_XOFF	**Layer horizontal X offset** Range: 0 ~ 8191

1400BF80 OVL_L2_ADDR — Overlay Layer 2 Memory Address — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L2_ADDR															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L2_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**L2AD**	L2_ADDR	Layer memory buffer address

1400B084 OVL_L2_PITCH **Overlay Layer 2 Pitch** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L2_SURFL_EN	L2_BLEND_RND_SHT		L2_CONST_BLD	L2_DRGB_SEL_EXT	L2_DA_SEL_EXT	L2_SRGB_SEL_EXT	L2_SA_SEL_EXT	L2_DRGB_SEL		L2_DA_SEL		L2_SRGB_SEL		L2_SA_SEL	
Type	RW	RW		RW	RW	RW	RW	RW	RW		RW		RW		RW	
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L2_SRC_PITCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**L2SP**	SURFL_EN	**Enables layer surface dlinger alpha_blending** 0: Disable surface flinger alpha_blending 1: Enable surface flinger alpha_blending
30		L2_BLEND_RND_SHT	
28		L2_CONST_BLD	
27		L2_DRGB_SEL_EXT	**Selects layer destination_RGB alpha**
26		L2_DA_SEL_EXT	**Selects layer destination_Alpha alpha**
25		L2_SRGB_SEL_EXT	**Selects layer source_RGB alpha**
24		L2_SA_SEL_EXT	**Selects layer source_Alpha alpha**
23:22	**L2SP**	L2_DRGB_SEL	**Selects layer destination_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
21:20	**L2SP**	L2_DA_SEL	**Selects layer destination_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
19:18	**L2SP**	L2_SRGB_SEL	**Selects layer source_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
17:16	**L2SP**	L2_SA_SEL	**Selects layer source_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved

Bit(s)	Mnemonic	Name	Description
15:0	**L2SP**	L2_SRC_PITCH	**Layer source pitch**

1400B088 OVL_L2_TILE Overlay Layer 2 Tile Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TILE_HORI_BLOCK_NUM										TILE_EN	TILE_WIDTH_SEL	TILE_HEIGHT			
Type	OTHER										OTHER	OTHER	OTHER			
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TILE_HEIGHT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**TILE_BLKS**	TILE_HORI_BLOCK_NUM	**Number of horizontal blocks**
21	**TILE_EN**	TILE_EN	**Enables tile mode** 0: Disable 1: Enable
20	**TILE_W**	TILE_WIDTH_SEL	**Width of tile** 0: 16 1: 32
19:0	**TILE_H**	TILE_HEIGHT	**Height of source tile mode**

1400B08C OVL_L2_CLIP Overlay Layer 2 Clip 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L2_SRC_BOTTOM_CLIP								L2_SRC_TOP_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L2_SRC_RIGHT_CLIP								L2_SRC_LEFT_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**L2_SRC_BOTTOM_CLIP**	L2_SRC_BOTTOM_CLIP	Layer 2 bottom clip
23:16	**L2_SRC_TOP_CLIP**	L2_SRC_TOP_CLIP	Layer 2 top clip
15:8	**L2_SRC_RIGHT_CLIP**	L2_SRC_RIGHT_CLIP	Layer 2 right clip
7:0	**L2_SRC_LEFT_CLIP**	L2_SRC_LEFT_CLIP	Layer 2 left clip

1400B090 OVL_L3_CON Overlay Layer 3 Control 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSTK	SRCK	LAYER_SRC		MTX_	MTX_	RGB_	BYTE	CLRF	R_FI	LAND	EN_3	INT_MTX_SEL			

	EY_EN	EY_EN			EN	AUTO_DIS	SWAP	_SWAP	MT_MAN	RST	SCAPE	D				
Type	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLRFMT				EXT_MTX_EN	HORIZONTAL_FLIP_EN	VERTICAL_FLIP_EN	ALPHA_EN	ALPHA							
Type	RW				OTHER	RW	RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**DKEN**	DSTKEY_EN	**Enables destination color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable destination color key 1: Enable destination color key
30	**SKEN**	SRCKEY_EN	**Enables source color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable source color key 1: Enable source color key
29:28	**LSRC**	LAYER_SRC	**Selects layer pixel from memory/constant color/SCL/PQ** 00: Layer pixel from memory RDMA3 01: Layer pixel from constant color 10: Layer pixel from UFOd 11: Layer pixel from PQ
27		MTX_EN	
26		MTX_AUTO_DIS	
25	**RGSW**	RGB_SWAP	**No use**
24	**BTSW**	BYTE_SWAP	**Swaps unified color format** 1: BGR565, RGB888, RGBA8888, ARGB8888, VYUY, YVYU 0: RGB565, BGR888, BGRA8888, ABGR8888, UYVY, YUYV
23		CLRFMT_MAN	
22		R_FIRST	**Right eye image first when in 3D mode** 0: Show left eye image first in 3D mode 1: Show right eye image first in 3D mode
21		LANDSCAPE	**Enables 3D landscape mode** 0: 3D portrait mode 1: 3D landscape mode
20		EN_3D	**Enables 3D mode** 0: 2D mode 1: 3D mode
19:16	**MTX**	INT_MTX_SEL	**Selects color matrix table** 0000: MTX_RGB_TO_JPEG 0010: MTX_RGB_TO_BT601 0011: MTX_RGB_TO_BT709 0100: MTX_JPEG_TO_RGB 0110: MTX_BT601_TO_RGB 0111: MTX_BT709_TO_RGB 1000: MTX_JPEG_TO_BT601 1001: MTX_JPEG_TO_BT709 1010: MTX_BT601_TO_JPEG

Bit(s)	Mnemonic	Name	Description
			1011: MTX_BT709_TO_JPEG 1100: MTX_BT709_TO_BT601 1101: MTX_BT601_TO_BT709 Others: HW default (JPEG_TO_RGB)
15:12	**CFMT**	CLRFMT	**//--OLD define for reference only** 0000: RGB888 0001: RGB565 0010: ARGB8888 0011: PARGB8888 0100: xARGB8888 1000: YUYV 1001: UYVY 1010: YVYU 1011: VYUY 1111: YUV444 Others: Reserved color format 0000: RGB565 0001: RGB888 0010: RGBA8888/BGRA8888 0011: ARGB8888/ABGR8888 0100: UVVY, VYUY 0101: YUYV, YVYU
11	**MTXEN**	EXT_MTX_EN	**Enables external programmable coeff** 0: Matrix coeff 1: Programmable coeff
10	**HFE**	HORIZONTAL_FLIP_EN	**Enables horizontal flip** 0: Disable horizontal flip 1: Enable horizontal flip
9	**VFE**	VERTICAL_FLIP_ EN	**Enables vertical flip** 0: Disable vertical flip 1: Enable vertical flip
8	**AEN**	ALPHA_EN	**Enables alpha blending** 0: Disable alpha blending 1: Enable alpha blending
7:0	**APHA**	ALPHA	**Constant alpha value**

1400B094 OVL_L3_SRCKEY **Overlay Layer 3 Source Key** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SKEY**	SRCKEY	**Layer source color key** Active when source color key is enabled.

1400B098 OVL_L3_SRC **Overlay Layer 3 Source Size** **00000000**

_SIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L3_SRC_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L3_SRC_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**L3H**	L3_SRC_H	**Layer source height** Range: 0 ~ 8191
12:0	**L3W**	L3_SRC_W	**Layer source width** Range: 0 ~ 8191

1400B09C OVL_L3_OFFSET **Overlay Layer 3 Offset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L3_YOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L3_XOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**L3H**	L3_YOFF	**Layer vertical Y offset** Range: 0 ~ 8191
12:0	**L3XO**	L3_XOFF	**Layer horizontal X offset** Range: 0 ~ 8191

1400BFA0 OVL_L3_ADDR **Overlay Layer 3 Memory Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L3_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L3_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**L3AD**	L3_ADDR	Layer memory buffer address

1400B0A4 OVL_L3_PITCH **Overlay Layer 3 Pitch** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SURFL_EN	L3_BLEND_RND_SHT		L3_CONST_BLD	L3_DRGB_SEL_EXT	L3_DA_SEL_EXT	L3_SRGB_SEL_EXT	L3_SA_SEL_EXT	L3_DRGB_SEL		L3_DA_SEL		L3_SRGB_SEL		L3_SA_SEL	
Type	RW	RW		RW	RW	RW	RW	RW	RW		RW		RW		RW	
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L3_SRC_PITCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**L3SP**	SURFL_EN	**Enables layer surface dlinger alpha_blending** 0: Disable surface flinger alpha_blending 1: Enable surface flinger alpha_blending
30		L3_BLEND_RND_SHT	
28		L3_CONST_BLD	
27		L3_DRGB_SEL_EXT	**Selects layer destination_RGB alpha**
26		L3_DA_SEL_EXT	**Selects layer destination_Alpha alpha**
25		L3_SRGB_SEL_EXT	**Selects layer source_RGB alpha**
24		L3_SA_SEL_EXT	**Selects layer source_Alpha alpha**
23:22	**L3SP**	L3_DRGB_SEL	**Selects layer destination_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
21:20	**L3SP**	L3_DA_SEL	**Selects layer destination_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
19:18	**L3SP**	L3_SRGB_SEL	**Selects layer source_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
17:16	**L3SP**	L3_SA_SEL	**Selects layer source_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
15:0	**L3SP**	L3_SRC_PITCH	**Layer source pitch**

1400B0A8 OVL_L3_TILE **Overlay Layer 3 Tile Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TILE_HORI_BLOCK_NUM										TILE_EN	TILE_WIDTH_SEL	TILE_HEIGHT			
Type	OTHER										OTHER	OTHER	OTHER			

Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TILE_HEIGHT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**TILE_BLKS**	TILE_HORI_BLOCK_NUM	**Number of horizontal blocks**
21	**TILE_EN**	TILE_EN	**Enables tile mode** 0: Disable 1: Enable
20	**TILE_W**	TILE_WIDTH_SEL	**Width of tile** 0: 16 1: 32
19:0	**TILE_H**	TILE_HEIGHT	**Height of source tile mode**

1400B0AC OVL_L3_CLIP — Overlay Layer 3 Clip — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L3_SRC_BOTTOM_CLIP								L3_SRC_TOP_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L3_SRC_RIGHT_CLIP								L3_SRC_LEFT_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**L3_SRC_BOTTOM_CLIP**	L3_SRC_BOTTOM_CLIP	Layer 3 bottom clip
23:16	**L3_SRC_TOP_CLIP**	L3_SRC_TOP_CLIP	Layer 3 top clip
15:8	**L3_SRC_RIGHT_CLIP**	L3_SRC_RIGHT_CLIP	Layer 3 right clip
7:0	**L3_SRC_LEFT_CLIP**	L3_SRC_LEFT_CLIP	Layer 3 left clip

1400B0C0 OVL_RDMA0_CTRL — Overlay RDMA0 Control — 03FF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						RDMA0_FIFO_USED_SIZE										
Type						RU										
Reset						0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RDMA0_INTERLACE				RDMA0_EN
Type												OTHER				RW
Reset												0				0

Bit(s)	Mnemonic	Name	Description
26:16		RDMA0_FIFO_USED_SIZE	**Overlay RDMA0 used size**
4		RDMA0_INTERLACE	**Overlay RDMA0 interlace** 0: Disable 1: Enable
0		RDMA0_EN	**Overlay RDMA0 Enable** 0: Disable 1: Enable

1400B0C8 OVL_RDMA0_MEM_GMC_SETTING1 **Overlay RDMA0 Memory GMC Setting** **1010FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA0_PRE_ULTRA_THRESHOLD_HIGH_OFS								RDMA0_ULTRA_THRESHOLD_HIGH_OFS							
Type	OTHER								OTHER							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA0_PRE_ULTRA_THRESHOLD								RDMA0_ULTRA_THRESHOLD							
Type	OTHER								OTHER							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		RDMA0_PRE_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA0 pre_ultra threshold high offset
23:16		RDMA0_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA0 ultra threshold high offset
15:8		RDMA0_PRE_ULTRA_THRESHOLD	Overlay RDMA0 pre_ultra threshold
7:0		RDMA0_ULTRA_THRESHOLD	Overlay RDMA0 ultra threshold

1400B0CC OVL_RDMA0_MEM_SLOW_CON **Overlay RDMA0 Memory Slow Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA0_SLOW_CNT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RDMA0_SLOW_EN
Type																OTHER
Reset																0

Bit(s)	Mnemonic	Name	Description
31:16		RDMA0_SLOW_CNT	**Overlay RDMA0 memory slow-down counter** After this SLOW_CNT, SMI will raise greq again. 10: 10 cycles between 2 greq at least

Bit(s)	Mnemonic	Name	Description
0		RDMA0_SLOW_EN	33: 33 cycles between 2 greq at least **Enables overlay RDMA0 memory slow-down** 0: Disable slow-down 1: Enable slow-down

1400B0D0 OVL_RDMA0_FIFO_CTRL **Overlay RDMA0 FIFO Control** **01200000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA0_FIFO_UND_EN						RDMA0_FIFO_SIZE									
Type	OTHER						RW									
Reset	0						0	1	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RDMA0_FIFO_THRD									
Type							OTHER									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		RDMA0_FIFO_UND_EN	**Overlay RDMA0 FIFO underflow control** 0: Disable FIFO underflow 1: Enable FIFO underflow
25:16		RDMA0_FIFO_SIZ E	**Overlay RDMA0 FIFO size** Unit: 16 bytes 128: FIFO size is 128*128.
9:0		RDMA0_FIFO_THR D	**Overlay RDMA0 FIFO output valid threshold** Unit: 16 bytes. This value should be smaller than SRC_W*SRC_H*bpp >> 2. 0, 1: If FIFO pointer >= 1, RDMA will send data valid to OVL. 2: If FIFO pointer >= 2, RDMA will send data valid to OVL.

1400B0E0 OVL_RDMA1_CTRL **Overlay RDMA1 Control** **03FF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						RDMA1_FIFO_USED_SIZE										
Type						RU										
Reset						0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RDMA1_INTERLACE				RDMA1_EN
Type												OTHER				RW
Reset												0				0

Bit(s)	Mnemonic	Name	Description
26:16		RDMA1_FIFO_USE D_SIZE	**Overlay RDMA1 used size**

Bit(s)	Mnemonic	Name	Description
4		RDMA1_INTERLACE	**Overlay RDMA1 interlace** 0: Disable 1: Enable
0		RDMA1_EN	**Enables overlay RDMA1** 0: Disable 1: Enable

1400B0E8 OVL_RDMA1_MEM_GMC_SETTING1 **Overlay RDMA1 Memory GMC Setting** **1010FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA1_PRE_ULTRA_THRESHOLD_HIGH_OFS								RDMA1_ULTRA_THRESHOLD_HIGH_OFS							
Type	OTHER								OTHER							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA1_PRE_ULTRA_THRESHOLD								RDMA1_ULTRA_THRESHOLD							
Type	OTHER								OTHER							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		RDMA1_PRE_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA1 pre_ultra threshold high offset
23:16		RDMA1_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA1 ultra threshold high offset
15:8		RDMA1_PRE_ULTRA_THRESHOLD	Overlay RDMA1 pre_ultra threshold
7:0		RDMA1_ULTRA_THRESHOLD	Overlay RDMA1 ultra threshold

1400B0EC OVL_RDMA1_MEM_SLOW_CON **Overlay RDMA1 Memory Slow Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA1_SLOW_CNT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RDMA1_SLOW_EN
Type																OTHER
Reset																0

Bit(s)	Mnemonic	Name	Description
31:16		RDMA1_SLOW_CNT	**Overlay RDMA1 memory slow-down counter** After this SLOW_CNT, SMI will raise greq again. 10: 10 cycles between 2 greq at least 33: 33 cycles between 2 greq at least

Bit(s)	Mnemonic	Name	Description
0		RDMA1_SLOW_EN	**Enables overlay RDMA1 memory slow-down** 0: Disable slow-down 1: Enable slow-down

1400B0F0 OVL_RDMA1_FIFO_CTRL **Overlay RDMA1 FIFO Control** **01200000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA1_FIFO_UND_EN						RDMA1_FIFO_SIZE									
Type	OTHER						RW									
Reset	0						0	1	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RDMA1_FIFO_THRD									
Type							OTHER									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		RDMA1_FIFO_UND_EN	**Overlay RDMA1 FIFO underflow control** 0: Disable FIFO underflow 1: Enable FIFO underflow
25:16		RDMA1_FIFO_SIZE	**Overlay RDMA1 FIFO size** Unit: 16 bytes 128: FIFO size is 128*128.
9:0		RDMA1_FIFO_THRD	**Overlay RDMA1 FIFO output valid threshold** Unit: 16 bytes. This value should be smaller than SRC_W*SRC_H*bpp >> 2. 0, 1: If FIFO pointer >= 1, RDMA will send data valid to OVL. 2: If FIFO pointer >= 2, RDMA will send data valid to OVL.

1400B100 OVL_RDMA2_CTRL **Overlay RDMA2 Control** **03FF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						RDMA2_FIFO_USED_SIZE										
Type						RU										
Reset						0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RDMA2_INTERLACE				RDMA2_EN
Type												OTHER				RW
Reset												0				0

Bit(s)	Mnemonic	Name	Description
26:16		RDMA2_FIFO_USED_SIZE	**Overlay RDMA2 used size**
4		RDMA2_INTERLACE	**Overlay RDMA2 interlace**

Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable
0		RDMA2_EN	**Enables overlay RDMA2** 0: Disable 1: Enable

1400B108 OVL_RDMA2_MEM_GMC_SETTING1 Overlay RDMA2 Memory GMC Setting 1010FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA2_PRE_ULTRA_THRESHOLD_HIGH_OFS								RDMA2_ULTRA_THRESHOLD_HIGH_OFS							
Type	OTHER								OTHER							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA2_PRE_ULTRA_THRESHOLD								RDMA2_ULTRA_THRESHOLD							
Type	OTHER								OTHER							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		RDMA2_PRE_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA2 pre_ultra threshold high offset
23:16		RDMA2_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA2 ultra threshold high offset
15:8		RDMA2_PRE_ULTRA_THRESHOLD	Overlay RDMA2 pre_ultra threshold
7:0		RDMA2_ULTRA_THRESHOLD	Overlay RDMA2 ultra threshold

1400B10C OVL_RDMA2_MEM_SLOW_CON Overlay RDMA2 Memory Slow Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA2_SLOW_CNT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RDMA2_SLOW_EN
Type																OTHER
Reset																0

Bit(s)	Mnemonic	Name	Description
31:16		RDMA2_SLOW_CNT	**Overlay RDMA2 memory slow-down counter** After this SLOW_CNT, SMI will raise greq again. 10: 10 cycles between 2 greq at least 33: 33 cycles between 2 greq at least
0		RDMA2_SLOW_EN	**Enables overlay RDMA2 memory slow-down**

Bit(s)	Mnemonic	Name	Description
			0: Disable slow-down 1: Enable slow-down

1400B110 OVL_RDMA2_FIFO_CTRL **Overlay RDMA2 FIFO Control** **01200000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA2_FIFO_UND_EN						RDMA2_FIFO_SIZE									
Type	OTHER						RW									
Reset	0						0	1	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RDMA2_FIFO_THRD									
Type							OTHER									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		RDMA2_FIFO_UND_EN	**Overlay RDMA2 FIFO underflow control** 0: Disable FIFO underflow 1: Enable FIFO underflow
25:16		RDMA2_FIFO_SIZE	**Overlay RDMA2 FIFO size** Unit: 16 bytes 128: FIFO size is 128*128.
9:0		RDMA2_FIFO_THRD	**Overlay RDMA2 FIFO output valid threshold** Unit: 16 bytes. This value should be smaller than SRC_W*SRC_H*bpp >> 2. 0, 1: If FIFO pointer >= 1, RDMA will send data valid to OVL. 2: If FIFO pointer >= 2, RDMA will send data valid to OVL.

1400B120 OVL_RDMA3_CTRL **Overlay RDMA3 Control** **03FF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						RDMA3_FIFO_USED_SIZE										
Type						RU										
Reset						0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RDMA3_INTERLACE				RDMA3_EN
Type												OTHER				RW
Reset												0				0

Bit(s)	Mnemonic	Name	Description
26:16		RDMA3_FIFO_USED_SIZE	**Overlay RDMA3 used size**
4		RDMA3_INTERLACE	**Overlay RDMA3 interlace**

Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable
0		RDMA3_EN	**Enables overlay RDMA3** 0: Disable 1: Enable

1400B128 OVL_RDMA3_MEM_GMC_SETTING1 Overlay RDMA3 Memory GMC Setting 1010FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA3_PRE_ULTRA_THRESHOLD_HIGH_OFS								RDMA3_ULTRA_THRESHOLD_HIGH_OFS							
Type	OTHER								OTHER							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA3_PRE_ULTRA_THRESHOLD								RDMA3_ULTRA_THRESHOLD							
Type	OTHER								OTHER							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		RDMA3_PRE_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA3 pre_ultra threshold high offset
23:16		RDMA3_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA3 ultra threshold high offset
15:8		RDMA3_PRE_ULTRA_THRESHOLD	Overlay RDMA3 pre_ultra threshold
7:0		RDMA3_ULTRA_THRESHOLD	Overlay RDMA3 ultra threshold

1400B12C OVL_RDMA3_MEM_SLOW_CON Overlay RDMA3 Memory Slow Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA3_SLOW_CNT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RDMA3_SLOW_EN
Type																OTHER
Reset																0

Bit(s)	Mnemonic	Name	Description
31:16		RDMA3_SLOW_CNT	**Overlay RDMA3 memory slow-down counter** After this SLOW_CNT, SMI will raise greq again. 10: 10 cycles between 2 greq at least 33: 33 cycles between 2 greq at least
0		RDMA3_SLOW_EN	**Enables overlay RDMA3 memory slow-down**

Bit(s)	Mnemonic	Name	Description
			0: Disable slow-down 1: Enable slow-down

1400B130 OVL_RDMA3_FIFO_CTRL **Overlay RDMA3 FIFO Control** **01200000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA3_FIFO_UND_EN						RDMA3_FIFO_SIZE									
Type	OTHER						RW									
Reset	0						0	1	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RDMA3_FIFO_THRD									
Type							OTHER									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		RDMA3_FIFO_UND_EN	**Overlay RDMA3 FIFO underflow control** 0: Disable FIFO underflow 1: Enable FIFO underflow
25:16		RDMA3_FIFO_SIZE	**Overlay RDMA3 FIFO size** Unit: 16 bytes 128: FIFO size is 128*128.
9:0		RDMA3_FIFO_THRD	**Overlay RDMA3 FIFO output valid threshold** Unit: 16 bytes. This value should be smaller than SRC_W*SRC_H*bpp >> 2. 0, 1: If FIFO pointer >= 1, RDMA will send data valid to OVL. 2: If FIFO pointer >= 2, RDMA will send data valid to OVL.

1400B134 OVL_L0_Y2R_PARA_R0 **Overlay L0 Y2R Conversion Parameter R0** **00000400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_RMU												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_RMU	Overlay L0 YUV2RGB program parameter for R color of U component
12:0		C_CF_RMY	Overlay L0 YUV2RGB program parameter for R color of Y component

1400B138 OVL_Lo_Y2R_PARA_R1 **Overlay Lo Y2R Conversion Parameter R1** **0000057C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMV												
Type				OTHER												
Reset				0	0	1	0	1	0	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_RMV	Overlay Lo YUV2RGB program parameter for R color of V component

1400B13C OVL_Lo_Y2R_PARA_Go **Overlay Lo Y2R Conversion Parameter Go** **1EA80400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_GMU												
Type				OTHER												
Reset				1	1	1	1	0	1	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_GMU	Overlay Lo YUV2RGB program parameter for G color of U component
12:0		C_CF_GMY	Overlay Lo YUV2RGB program parameter for G color of Y component

1400B140 OVL_Lo_Y2R_PARA_G1 **Overlay Lo Y2R Conversion Parameter G1** **00001D35**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMV												
Type				OTHER												
Reset				1	1	1	0	1	0	0	1	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_GMV	Overlay Lo YUV2RGB program parameter for G color of V component

1400B144 OVL_Lo_Y2R_PARA_Bo **Overlay Lo Y2R Conversion Parameter Bo** **06EE0400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_BMU												
Type				OTHER												
Reset				0	0	1	1	0	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_BMU	Overlay Lo YUV2RGB program parameter for B color of U component
12:0		C_CF_BMY	Overlay Lo YUV2RGB program parameter for B color of Y component

1400B148 OVL_Lo_Y2R_PARA_B1 **Overlay Lo Y2R Conversion Parameter B1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMV												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_BMV	Overlay Lo YUV2RGB program parameter for B color of V component

1400B14C OVL_Lo_Y2R_PARA_YUV_A_o **Overlay Lo Y2R Conversion Parameter Extended Add on YUV o** **01800000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_UA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_YA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_UA	Overlay Lo YUV2RGB program parameter for U to add extended offset
8:0		C_CF_YA	Overlay Lo YUV2RGB program parameter for Y to add

Bit(s)	Mnemonic	Name	Description
			extended offset

1400B150 OVL_L0_Y2R_PARA_YUVA_1 **Overlay L0 Y2R Conversion Parameter Extended Add on YUV 1** **00000180**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_VA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_VA	Overlay L0 YUV2RGB program parameter for V to add extended offset

1400B154 OVL_L0_Y2R_PARA_RGBA_0 **Overlay L0 Y2R Conversion Parameter Extended Add on RGB 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_GA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_RA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_GA	Overlay L0 YUV2RGB program parameter for G to add extended offset
8:0		C_CF_RA	Overlay L0 YUV2RGB program parameter for R to add extended offset

1400B158 OVL_L0_Y2R_PARA_RGBA_1 **Overlay L0 Y2R Conversion Parameter Extended Add on RGB 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_BA								
Type								OTHER								

Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_BA	Overlay L0 YUV2RGB program parameter for B to add extended offset

1400B15C OVL_L1_Y2R_PARA_R0 Overlay L1 Y2R Conversion Parameter R0 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_RMU												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_RMU	Overlay L1 YUV2RGB program parameter for R color of U component
12:0		C_CF_RMY	Overlay L1 YUV2RGB program parameter for R color of Y component

1400B160 OVL_L1_Y2R_PARA_R1 Overlay L1 Y2R Conversion Parameter R1 0000057C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMV												
Type				OTHER												
Reset				0	0	1	0	1	0	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_RMV	Overlay L1 YUV2RGB program parameter for R color of V component

1400B164 OVL_L1_Y2R_PARA_G0 Overlay L1 Y2R Conversion Parameter G0 1EA80400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_GMU												
Type				OTHER												
Reset				1	1	1	1	0	1	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMY												

Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_GMU	Overlay L1 YUV2RGB program parameter for G color of U component
12:0		C_CF_GMY	Overlay L1 YUV2RGB program parameter for G color of Y component

1400B168 OVL_L1_Y2R_PARA_G1 **Overlay L1 Y2R Conversion Parameter G1** **00001D35**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMV												
Type				OTHER												
Reset				1	1	1	0	1	0	0	1	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_GMV	Overlay L1 YUV2RGB program parameter for G color of V component

1400B16C OVL_L1_Y2R_PARA_B0 **Overlay L1 Y2R Conversion Parameter B0** **06EE0400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_BMU												
Type				OTHER												
Reset				0	0	1	1	0	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_BMU	Overlay L1 YUV2RGB program parameter for B color of U component
12:0		C_CF_BMY	Overlay L1 YUV2RGB program parameter for B color of Y component

1400B170 OVL_L1_Y2R_PARA_B1 **Overlay L1 Y2R Conversion Parameter B1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMV												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_BMV	Overlay L1 YUV2RGB program parameter for B color of V component

1400B174 OVL_L1_Y2R_PARA_YUV_A_0 Overlay L1 Y2R Conversion Parameter Extended Add on YUV 0 01800000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_UA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_YA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_UA	Overlay L1 YUV2RGB program parameter for U to add extended offset
8:0		C_CF_YA	Overlay L1 YUV2RGB program parameter for Y to add extended offset

1400B178 OVL_L1_Y2R_PARA_YUV_A_1 Overlay L1 Y2R Conversion Parameter Extended Add on YUV 1 00000180

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_VA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_VA	Overlay L1 YUV2RGB program parameter for V to add extended offset

1400B17C OVL_L1_Y2R_PARA_RGB_A_0 Overlay L1 Y2R Conversion Parameter Extended Add on RGB 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_GA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_RA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_GA	Overlay L1 YUV2RGB program parameter for G to add extended offset
8:0		C_CF_RA	Overlay L1 YUV2RGB program parameter for R to add extended offset

1400B180 OVL_L1_Y2R_PARA_RGBA_1 — **Overlay L1 Y2R Conversion Parameter Extended Add on RGB 1** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_BA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_BA	Overlay L1 YUV2RGB program parameter for B to add extended offset

1400B184 OVL_L2_Y2R_PARA_R0 — **Overlay L2 Y2R Conversion Parameter R0** — **00000400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_RMU												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_RMU	Overlay L2 YUV2RGB program parameter for R color of U component
12:0		C_CF_RMY	Overlay L2 YUV2RGB program parameter for R color of Y component

1400B188 OVL_L2_Y2R_PARA_R1 **Overlay L2 Y2R Conversion Parameter R1** **0000057C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMV												
Type				OTHER												
Reset				0	0	1	0	1	0	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_RMV	Overlay L2 YUV2RGB program parameter for R color of V component

1400B18C OVL_L2_Y2R_PARA_G0 **Overlay L2 Y2R Conversion Parameter G0** **1EA80400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_GMU												
Type				OTHER												
Reset				1	1	1	1	0	1	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_GMU	Overlay L2 YUV2RGB program parameter for G color of U component
12:0		C_CF_GMY	Overlay L2 YUV2RGB program parameter for G color of Y component

1400B190 OVL_L2_Y2R_PARA_G1 **Overlay L2 Y2R Conversion Parameter G1** **00001D35**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMV												
Type				OTHER												
Reset				1	1	1	0	1	0	0	1	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_GMV	Overlay L2 YUV2RGB program parameter for G color of V component

Bit(s)	Mnemonic	Name	Description

1400B194 OVL_L2_Y2R_PARA_B0 — **Overlay L2 Y2R Conversion Parameter B0** — **06EE0400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_BMU												
Type				OTHER												
Reset				0	0	1	1	0	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_BMU	Overlay L2 YUV2RGB program parameter for B color of U component
12:0		C_CF_BMY	Overlay L2 YUV2RGB program parameter for B color of Y component

1400B198 OVL_L2_Y2R_PARA_B1 — **Overlay L2 Y2R Conversion Parameter B1** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMV												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_BMV	Overlay L2 YUV2RGB program parameter for B color of V component

1400B19C OVL_L2_Y2R_PARA_YUVA_0 — **Overlay L2 Y2R Conversion Parameter Extended Add on YUV 0** — **01800000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_UA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_YA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_UA	Overlay L2 YUV2RGB program parameter for U to add extended offset
8:0		C_CF_YA	Overlay L2 YUV2RGB program parameter for Y to add extended offset

1400B1A0 OVL_L2_Y2R_PARA_YUV_A_1 **Overlay L2 Y2R Conversion Parameter Extended Add on YUV 1** **00000180**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_VA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_VA	Overlay L2 YUV2RGB program parameter for V to add extended offset

1400B1A4 OVL_L2_Y2R_PARA_RGB_A_0 **Overlay L2 Y2R Conversion Parameter Extended Add on RGB 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_GA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_RA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_GA	Overlay L2 YUV2RGB program parameter for G to add extended offset
8:0		C_CF_RA	Overlay L2 YUV2RGB program parameter for R to add extended offset

1400B1A8 OVL_L2_Y2R_PARA_RGB_A_1 **Overlay L2 Y2R Conversion Parameter Extended Add on RGB 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_BA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_BA	Overlay L2 YUV2RGB program parameter for B to add extended offset

1400B1AC OVL_L3_Y2R_PARA_R0 Overlay L3 Y2R Conversion Parameter R0 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_RMU												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_RMU	Overlay L3 YUV2RGB program parameter for R color of U component
12:0		C_CF_RMY	Overlay L3 YUV2RGB program parameter for R color of Y component

1400B1B0 OVL_L3_Y2R_PARA_R1 Overlay L3 Y2R Conversion Parameter R1 0000057C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMV												
Type				OTHER												
Reset				0	0	1	0	1	0	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_RMV	Overlay L3 YUV2RGB program parameter for R color of V component

1400B1B4 OVL_L3_Y2R_PARA_G0 Overlay L3 Y2R Conversion Parameter G0 1EA80400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_GMU												
Type				OTHER												

Reset				1	1	1	1	0	1	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_GMU	Overlay L3 YUV2RGB program parameter for G color of U component
12:0		C_CF_GMY	Overlay L3 YUV2RGB program parameter for G color of Y component

1400B1B8 OVL_L3_Y2R_PARA_G1 — Overlay L3 Y2R Conversion Parameter G1 — 00001D35

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMV												
Type				OTHER												
Reset				1	1	1	0	1	0	0	1	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_GMV	Overlay L3 YUV2RGB program parameter for G color of V component

1400B1BC OVL_L3_Y2R_PARA_B0 — Overlay L3 Y2R Conversion Parameter B0 — 06EE0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_BMU												
Type				OTHER												
Reset				0	0	1	1	0	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_BMU	Overlay L3 YUV2RGB program parameter for B color of U component
12:0		C_CF_BMY	Overlay L3 YUV2RGB program parameter for B color of Y component

1400B1C0 OVL_L3_Y2R_PARA_B1 — Overlay L3 Y2R Conversion Parameter B1 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMV												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_BMV	Overlay L3 YUV2RGB program parameter for B color of V component

1400B1C4 OVL_L3_Y2R_PARA_YUV_A_0 **Overlay L3 Y2R Conversion Parameter Extended Add on YUV 0** **01800000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_UA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_YA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_UA	Overlay L3 YUV2RGB program parameter for U to add extended offset
8:0		C_CF_YA	Overlay L3 YUV2RGB program parameter for Y to add extended offset

1400B1C8 OVL_L3_Y2R_PARA_YUV_A_1 **Overlay L3 Y2R Conversion Parameter Extended Add on YUV 1** **00000180**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_VA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_VA	Overlay L3 YUV2RGB program parameter for V to add extended offset

1400B1CC OVL_L3_Y2R_PARA_RGB_A_0 — **Overlay L3 Y2R Conversion Parameter Extended Add on RGB 0** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_GA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_RA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_GA	Overlay L3 YUV2RGB program parameter for G to add extended offset
8:0		C_CF_RA	Overlay L3 YUV2RGB program parameter for R to add extended offset

1400B1D0 OVL_L3_Y2R_PARA_RGB_A_1 — **Overlay L3 Y2R Conversion Parameter Extended Add on RGB 1** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_BA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_BA	Overlay L3 YUV2RGB program parameter for B to add extended offset

1400B1D4 OVL_DEBUG_MON_SEL — **Overlay Debug Monitor Select** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DBG_MON_SEL			
Type													WO			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0		DBG_MON_SEL	Overlay Debug Monitor Select

Bit(s)	Mnemonic	Name	Description

1400B1E0 OVL_RDMA0_MEM_GMC_SETTING2 **Overlay RDMA0 Memory GMC Setting** **205F00BF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RDMA0_FORCE_REQ_THRESHOLD	RDMA0_REQ_THRESHOLD_ULTRA	RDMA0_REQ_THRESHOLD_PREULTRA		RDMA0_ISSUE_REQ_THRESHOLD_URG										
Type		RW	RW	RW		RW										
Reset		0	1	0		0	0	0	0	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RDMA0_ISSUE_REQ_THRESHOLD										
Type						RW										
Reset						0	0	0	1	0	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30		RDMA0_FORCE_REQ_THRESHOLD	
29		RDMA0_REQ_THRESHOLD_ULTRA	
28		RDMA0_REQ_THRESHOLD_PREULTRA	
26:16		RDMA0_ISSUE_REQ_THRESHOLD_URG	
10:0		RDMA0_ISSUE_REQ_THRESHOLD	Overlay RDMA0 issue request threshold (0 for best performance)

1400B1E4 OVL_RDMA1_MEM_GMC_SETTING2 **Overlay RDMA1 Memory GMC Setting** **205F00BF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RDMA1_FORCE_REQ_THRESHOLD	RDMA1_REQ_THRESHOLD_ULTRA	RDMA1_REQ_THRESHOLD_PREULTRA		RDMA1_ISSUE_REQ_THRESHOLD_URG										
Type		RW	RW	RW		RW										
Reset		0	1	0		0	0	0	0	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RDMA1_ISSUE_REQ_THRESHOLD										
Type						RW										
Reset						0	0	0	1	0	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30		RDMA1_FORCE_REQ_THRESHOLD	

Bit(s)	Mnemonic	Name	Description
29		RDMA1_REQ_THRESHOLD_ULTRA	
28		RDMA1_REQ_THRESHOLD_PREULTRA	
26:16		RDMA1_ISSUE_REQ_THRESHOLD_URG	
10:0		RDMA1_ISSUE_REQ_THRESHOLD	Overlay RDMA1 issue request threshold(0 for best performance)

1400B1E8 OVL_RDMA2_MEM_GMC_SETTING2 **Overlay RDMA2 Memory GMC Setting** **205F00BF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RDMA2_FORCE_REQ_THRESHOLD	RDMA2_REQ_THRESHOLD_ULTRA	RDMA2_REQ_THRESHOLD_PREULTRA		RDMA2_ISSUE_REQ_THRESHOLD_URG										
Type		RW	RW	RW		RW										
Reset		0	1	0		0	0	0	0	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RDMA2_ISSUE_REQ_THRESHOLD										
Type						RW										
Reset						0	0	0	1	0	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30		RDMA2_FORCE_REQ_THRESHOLD	
29		RDMA2_REQ_THRESHOLD_ULTRA	
28		RDMA2_REQ_THRESHOLD_PREULTRA	
26:16		RDMA2_ISSUE_REQ_THRESHOLD_URG	
10:0		RDMA2_ISSUE_REQ_THRESHOLD	Overlay RDMA2 issue request threshold(0 for best performance)

1400B1EC OVL_RDMA3_MEM_GMC_SETTING2 **Overlay RDMA3 Memory GMC Setting** **205F00BF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RDMA3_FORCE_REQ_THRESHOLD	RDMA3_REQ_THRESHOLD_ULTRA	RDMA3_REQ_THRESHOLD_PREULTRA		RDMA3_ISSUE_REQ_THRESHOLD_URG										
Type		RW	RW	RW		RW										
Reset		0	1	0		0	0	0	0	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name						RDMA3_ISSUE_REQ_THRESHOLD										
Type						RW										
Reset						0	0	0	1	0	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30		RDMA3_FORCE_REQ_THRESHOLD	
29		RDMA3_REQ_THRESHOLD_ULTRA	
28		RDMA3_REQ_THRESHOLD_PREULTRA	
26:16		RDMA3_ISSUE_REQ_THRESHOLD_URG	
10:0		RDMA3_ISSUE_REQ_THRESHOLD	Overlay RDMA3 issue request threshold(0 for best performance)

1400B1F0 OVL_RDMA_BURST_CON0 Overlay RDMA Burst Control 07775533

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				BURST_128B_BOUND		BURST15A_32B				BURST14A_32B				BURST13A_32B		
Type				RW		RW				RW				RW		
Reset				0		1	1	1		1	1	1		1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		BURST12A_32B				BURST11A_32B				BURST10A_32B				BURST9A_32B		
Type		RW				RW				RW				RW		
Reset		1	0	1		1	0	1		0	1	1		0	1	1

Bit(s)	Mnemonic	Name	Description
28		BURST_128B_BOUND	
26:24		BURST15A_32B	First burst slice for a 32B aligned burst of length 15
22:20		BURST14A_32B	First burst slice for a 32B aligned burst of length 14
18:16		BURST13A_32B	First burst slice for a 32B aligned burst of length 13
14:12		BURST12A_32B	First burst slice for a 32B aligned burst of length 12
10:8		BURST11A_32B	First burst slice for a 32B aligned burst of length 11
6:4		BURST10A_32B	First burst slice for a 32B aligned burst of length 10
2:0		BURST9A_32B	First burst slice for a 32B aligned burst of length 9

1400B1F4 OVL_RDMA_BURST_CON1 Overlay RDMA Burst Control 06666442

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						BURST15A_N32B				BURST14A_N32B				BURST13A_N32B		
Type						RW				RW				RW		
Reset						1	1	0		1	1	0		1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		BURST12A_N32B				BURST11A_N32B				BURST10A_N32B				BURST9A_N32B		
Type		RW				RW				RW				RW		

Reset		1	1	0		1	0	0		1	0	0		0	1	0

Bit(s)	Mnemonic	Name	Description
26:24		BURST15A_N32B	First burst slice for a non-32B aligned burst of length 15
22:20		BURST14A_N32B	First burst slice for a non-32B aligned burst of length 14
18:16		BURST13A_N32B	First burst slice for a non-32B aligned burst of length 13
14:12		BURST12A_N32B	First burst slice for a non-32B aligned burst of length 12
10:8		BURST11A_N32B	First burst slice for a non-32B aligned burst of length 11
6:4		BURST10A_N32B	First burst slice for a non-32B aligned burst of length 10
2:0		BURST9A_N32B	First burst slice for a non-32B aligned burst of length 9

1400B1F8 OVL_RDMA_GREQ_NUM **Overlay RDMA GREQ Number** **510FBBBB**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IOBUF_FLUSH_ULTRA	IOBUF_FLUSH_PREULTRA		GRP_BRK_STOP	GREQ_STOP_EN	GREQ_DIS_CNT			OSTD_GREQ_NUM							
Type	RW	RW		RW	RW	RW			RW							
Reset	0	1		1	0	0	0	1	0	0	0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LAYER3_GREQ_NUM				LAYER2_GREQ_NUM				LAYER1_GREQ_NUM				LAYER0_GREQ_NUM			
Type	RW				RW				RW				RW			
Reset	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1

Bit(s)	Mnemonic	Name	Description
31		IOBUF_FLUSH_ULTRA	
30		IOBUF_FLUSH_PREULTRA	
28		GRP_BRK_STOP	**Stop GREQ when group breaks**
27		GREQ_STOP_EN	**Stop each GREQ after GLCOMD**
26:24		GREQ_DIS_CNT	
23:16		OSTD_GREQ_NUM	
15:12	**LAYER3_GREQ_NUM**	LAYER3_GREQ_NUM	**OVL Layer 3 multi-greq number** Max.: 7
11:8	**LAYER2_GREQ_NUM**	LAYER2_GREQ_NUM	**OVL Layer 2 multi-greq number** Max.: 7
7:4	**LAYER1_GREQ_NUM**	LAYER1_GREQ_NUM	**OVL Layer 1 multi-greq number** Max.: 7
3:0	**LAYER0_GREQ_NUM**	LAYER0_GREQ_NUM	**OVL Layer 0 multi-greq number** Max.: 7

1400B1FC OVL_RDMA_GREQ_URG_NUM **Overlay RDMA GREQ Number** **20305555**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GREQ_NUM_SHT		GREQ_NUM_SHT_VAL	ARG_URG_BIAS			ARG_GREQ_URG_TH									
Type	RW		RW	RW			RW									

Reset	0	0	1	0			0	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LAYER3_GREQ_URG_NUM				LAYER2_GREQ_URG_NUM				LAYER1_GREQ_URG_NUM				LAYER0_GREQ_URG_NUM			
Type	RW				RW				RW				RW			
Reset	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
31:30		GREQ_NUM_SHT	
29		GREQ_NUM_SHT_VAL	
28		ARG_URG_BIAS	
25:16		ARG_GREQ_URG_TH	
15:12		LAYER3_GREQ_URG_NUM	**OVL Layer 3 multi-greq number** Max.: 7
11:8		LAYER2_GREQ_URG_NUM	**OVL Layer 2 multi-greq number** Max.: 7
7:4		LAYER1_GREQ_URG_NUM	**OVL Layer 1 multi-greq number** Max.: 7
3:0		LAYER0_GREQ_URG_NUM	**OVL Layer 0 multi-greq number** Max.: 7 (GREQ_URG_NUM <= GREQ_NUM)

1400B200 OVL_DUMMY_REG Overlay Dummy Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OVERLAY_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OVERLAY_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		OVERLAY_DUMMY	Overlay dummy register

1400B208 OVL_GDRDY_PRD Overlay SMI GDRDY Period 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									GDRDY_PRD							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDRDY_PRD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		GDRDY_PRD	

Bit(s)	Mnemonic	Name	Description

1400B20C OVL_RDMA_ULTRA_SRC **Overlay RDMA Ultra SRC** **0000A050**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ULTRA_RDMA_SRC		ULTRA_ROI_END_SRC		ULTRA_SMI_SRC		ULTRA_BUF_SRC		PREULTRA_RDMA_SRC		PREULTRA_ROI_END_SRC		PREULTRA_SMI_SRC		PREULTRA_BUF_SRC	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	1	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:14		ULTRA_RDMA_SRC	
13:12		ULTRA_ROI_END_SRC	
11:10		ULTRA_SMI_SRC	
9:8		ULTRA_BUF_SRC	
7:6		PREULTRA_RDMA_SRC	
5:4		PREULTRA_ROI_END_SRC	
3:2		PREULTRA_SMI_SRC	
1:0		PREULTRA_BUF_SRC	

1400B210 OVL_RDMA0_BUF_LOW **Overlay RDMA BUF Low** **00030020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											BUF_LOW_PREULTRA_TH					
Type											RW					
Reset											0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF_LOW_PREULTRA_TH						BUF_LOW_ULTRA_TH									
Type	RW						RW									
Reset	0	0	0	0			0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:12		BUF_LOW_PREULTRA_TH	
9:0		BUF_LOW_ULTRA_TH	

1400B214 OVL_RDMA1_BUF_LOW **Overlay RDMA BUF Low** **00030020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											BUF_LOW_PREULTRA_ TH					
Type											RW					
Reset											0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF_LOW_PREULTRA_ TH						BUF_LOW_ULTRA_TH									
Type	RW						RW									
Reset	0	0	0	0			0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:12		BUF_LOW_PREULTRA_TH	
9:0		BUF_LOW_ULTRA_TH	

1400B218 OVL_RDMA2_BUF_LOW **Overlay RDMA BUF Low** **00030020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											BUF_LOW_PREULTRA_ TH					
Type											RW					
Reset											0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF_LOW_PREULTRA_ TH						BUF_LOW_ULTRA_TH									
Type	RW						RW									
Reset	0	0	0	0			0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:12		BUF_LOW_PREULTRA_TH	
9:0		BUF_LOW_ULTRA_TH	

1400B21C OVL_RDMA3_BUF_LOW **Overlay RDMA BUF Low** **00030020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											BUF_LOW_PREULTRA_ TH					
Type											RW					
Reset											0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF_LOW_PREULTRA_ TH						BUF_LOW_ULTRA_TH									
Type	RW						RW									
Reset	0	0	0	0			0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:12		BUF_LOW_PREULTRA_TH	
9:0		BUF_LOW_ULTRA_TH	

Bit(s)	Mnemonic	Name	Description

1400B230 OVL_SMI_DBG **Overlay SMI Arbiter Debug Monitor** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SMI_FSM									
Type							RU									
Reset							0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
9:0		SMI_FSM	Overlay SMI arbiter FSM state

1400B234 OVL_GREQ_LAYER_CNT **Overlay Layer GREQ Counter** **01010101**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			LAYER3_GREQ_CNT								LAYER2_GREQ_CNT					
Type			RU								RU					
Reset			0	0	0	0	0	1			0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			LAYER1_GREQ_CNT								LAYER0_GREQ_CNT					
Type			RU								RU					
Reset			0	0	0	0	0	1			0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
29:24		LAYER3_GREQ_CNT	RDMA Layer 3 greq counter
21:16		LAYER2_GREQ_CNT	RDMA Layer 2 greq counter
13:8		LAYER1_GREQ_CNT	RDMA Layer 1 greq counter
5:0		LAYER0_GREQ_CNT	RDMA Layer 0 greq counter

1400B238 OVL_GDRDY_PRD_NUM **Overlay SMI GDRDY Period Number** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									GDRDY_PRD_NUM							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDRDY_PRD_NUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		GDRDY_PRD_NUM	

Bit(s)	Mnemonic	Name	Description

1400B240 OVL_FLOW_CTRL_DBG **Overlay Flow Control Debug Monitor** **000FBC01**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OVL_UPD_REG	REG_UPDATE	OVL_CLR	OVL_START	OVL_RUNNING	FRAME_DONE	FRAME_UNDERRUN	FRAME_SWRST_DONE	FRAME_HWRST_DONE		TRIG	RST	RDMA0_IDLE	RDMA1_IDLE	RDMA2_IDLE	RDMA3_IDLE
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU		RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0		0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OUT_IDLE		OVL_OUT_READY	OVL_OUT_VALID	BLEND_IDLE	ADDCON_IDLE	FSM_STATE									
Type	RU		RU	RU	RU	RU	RU									
Reset	1		1	1	1	1	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31		OVL_UPD_REG	**Overlay prepare to update register**
30		REG_UPDATE	**Updates overlay register**
29		OVL_CLR	**Clears overlay**
28		OVL_START	**Starts overlay**
27		OVL_RUNNING	**Overlay running**
26		FRAME_DONE	**Overlay frame complete**
25		FRAME_UNDERRUN	**Overlay frame underrun**
24		FRAME_SWRST_DONE	**Overlay frame reset done**
23		FRAME_HWRST_DONE	**Overlay EOF reset done**
21		TRIG	**Triggers overlay**
20		RST	**Resets overlay**
19		RDMA0_IDLE	**Overlay RDMA0 idle state**
18		RDMA1_IDLE	**Overlay RDMA1 idle state**
17		RDMA2_IDLE	**Overlay RDMA2 idle state**
16		RDMA3_IDLE	**Overlay RDMA3 idle state**
15		OUT_IDLE	**Overlay output relay idle state**
13		OVL_OUT_READY	**Overlay out_ready**
12		OVL_OUT_VALID	**Overlay out_valid**
11		BLEND_IDLE	**Overlay alpha blending idle state**
10		ADDCON_IDLE	**Overlay addcon idle state**
9:0		FSM_STATE	**Overlay flow control FSM state** 0x1: IDLE 0x2: WAIT 0x4: PREPARE 0x8: UPD_REG 0x10: ENG_CLR 0x20: ENG_ACT 0x40: H_WAIT_W_RST 0x80: S_WAIT_W_RST 0x100: H_W_RST 0x200: S_W_RST

1400B244 OVL_ADDCON_DBG Overlay Address Control Debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L3_WIN_HIT	L2_WIN_HIT		ROI_Y												
Type	RU	RU		RU												
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L1_WIN_HIT	L0_WIN_HIT		ROI_X												
Type	RU	RU		RU												
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		L3_WIN_HIT	Overlay Layer 3 pixel hit
30		L2_WIN_HIT	Overlay Layer 2 pixel hit
28:16		ROI_Y	Overlay pixel process vertical Y position
15		L1_WIN_HIT	Overlay Layer 1 pixel hit
14		L0_WIN_HIT	Overlay Layer 0 pixel hit
12:0		ROI_X	Overlay pixel process horizontal X position

1400B24C OVL_RDMA0_DBG Overlay RDMA0 Debug Monitor 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMI_GREQ	RDMA0_SMI_BUSY	RDMA0_OUT_VALID	RDMA0_OUT_READY	RDMA0_OUT_DATA											
Type	RU	RU	RU	RU	RU											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA0_OUT_DATA												RDMA0_LAYER_GREQ	RDMA0_WRAM_RST_CS		
Type	RU												RU	RU		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31		SMI_GREQ	Overlay 4-to-1 SMI request
30		RDMA0_SMI_BUSY	Overlay RDMA0 SMI busy
29		RDMA0_OUT_VALI D	Overlay RDMA0 output valid
28		RDMA0_OUT_READ Y	Overlay RDMA0 output ready
27:4		RDMA0_OUT_DATA	Overlay RDMA0 output data
3		RDMA0_LAYER_GR EQ	Overlay RDMA0 SMI request
2:0		RDMA0_WRAM_RST _CS	Overlay RDMA0 warm reset current state

1400B250 OVL_RDMA1_ Overlay RDMA1 Debug Monitor 00000001

DBG

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMI_GREQ	RDMA1_SMI_BUSY	RDMA1_OUT_VALID	RDMA1_OUT_READY	RDMA1_OUT_DATA											
Type	RU	RU	RU	RU	RU											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA1_OUT_DATA												RDMA1_LAYER_GREQ	RDMA1_WRAM_RST_CS		
Type	RU												RU	RU		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31		SMI_GREQ	Overlay 4-to-1 SMI request
30		RDMA1_SMI_BUSY	Overlay RDMA1 SMI busy
29		RDMA1_OUT_VALI D	Overlay RDMA1 output valid
28		RDMA1_OUT_READ Y	Overlay RDMA1 output ready
27:4		RDMA1_OUT_DATA	Overlay RDMA1 output data
3		RDMA1_LAYER_GR EQ	Overlay RDMA1 SMI request
2:0		RDMA1_WRAM_RST _CS	Overlay RDMA1 warm reset current state

1400B254 OVL_RDMA2_DBG **Overlay RDMA2 Debug Monitor** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMI_GREQ	RDMA2_SMI_BUSY	RDMA2_OUT_VALID	RDMA2_OUT_READY	RDMA2_OUT_DATA											
Type	RU	RU	RU	RU	RU											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA2_OUT_DATA												RDMA2_LAYER_GREQ	RDMA2_WRAM_RST_CS		
Type	RU												RU	RU		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31		SMI_GREQ	Overlay 4-to-1 SMI request
30		RDMA2_SMI_BUSY	Overlay RDMA2 SMI busy
29		RDMA2_OUT_VALI D	Overlay RDMA2 output valid
28		RDMA2_OUT_READ Y	Overlay RDMA2 output ready
27:4		RDMA2_OUT_DATA	Overlay RDMA2 output data
3		RDMA2_LAYER_GR EQ	Overlay RDMA2 SMI request
2:0		RDMA2_WRAM_RST _CS	Overlay RDMA2 warm reset current state

1400B258 OVL_RDMA3_DBG **Overlay RDMA3 Debug Monitor** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMI_GREQ	RDMA3_SMI_BUSY	RDMA3_OUT_VALID	RDMA3_OUT_READY	RDMA3_OUT_DATA											
Type	RU	RU	RU	RU	RU											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA3_OUT_DATA												RDMA3_LAYER_GREQ	RDMA3_WRAM_RST_CS		
Type	RU												RU	RU		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31		SMI_GREQ	Overlay 4-to-1 SMI request
30		RDMA3_SMI_BUSY	Overlay RDMA3 SMI busy
29		RDMA3_OUT_VALI D	Overlay RDMA3 output valid
28		RDMA3_OUT_READ Y	Overlay RDMA3 output ready
27:4		RDMA3_OUT_DATA	Overlay RDMA3 output data
3		RDMA3_LAYER_GR EQ	Overlay RDMA3 SMI request
2:0		RDMA3_WRAM_RST _CS	Overlay RDMA3 warm reset current state

1400B25C OVL_L0_CLR **Overlay Layer 0 Constant Color** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		ALPHA	Alpha component of L0 constant color
23:16		RED	Red component of L0 constant color
15:8		GREEN	Green component of L0 constant color
7:0		BLUE	Blue component of L0 constant color

1400B260 OVL_L1_CLR **Overlay Layer 1 Constant Color** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							

Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		ALPHA	Alpha component of L1 constant color
23:16		RED	Red component of L1 constant color
15:8		GREEN	Green component of L1 constant color
7:0		BLUE	Blue component of L1 constant color

1400B264 OVL_L2_CLR Overlay Layer 2 Constant Color FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		ALPHA	Alpha component of L2 constant color
23:16		RED	Red component of L2 constant color
15:8		GREEN	Green component of L2 constant color
7:0		BLUE	Blue component of L2 constant color

1400B268 OVL_L3_CLR Overlay Layer 3 Constant Color FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		ALPHA	Alpha component of L3 constant color
23:16		RED	Red component of L3 constant color
15:8		GREEN	Green component of L3 constant color
7:0		BLUE	Blue component of L3 constant color

1400B26C OVL_LC_CLR Overlay Constant Layer Color FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							

Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		ALPHA	Alpha component of constant layer color
23:16		RED	Red component of constant layer color
15:8		GREEN	Green component of constant layer color
7:0		BLUE	Blue component of constant layer color

1400B270 OVL_CRC **Overlay CRC** **7FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRC_RDY	CRC_OUT														
Type	RU	RU														
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRC_OUT															
Type	RU															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31		CRC_RDY	
30:0		CRC_OUT	

1400B280 OVL_LC_CON **Overlay Constant Layer Control** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSTKEY_EN	SRCKEY_EN	LAYER_SRC							R_FIRST	LANDSCAPE	EN_3D				
Type	RW	RW	RW							RW	RW	RW				
Reset	0	0	0	0						0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								ALPHA_EN	ALPHA							
Type								RW	RW							
Reset								0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**DKEN**	DSTKEY_EN	**Enables destination color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable destination color key 1: Enable destination color key
30	**SKEN**	SRCKEY_EN	**Enables source color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable source color key 1: Enable source color key
29:28	**LSRC**	LAYER_SRC	**Selects layer pixel from memory/constant color/SCL/PQ** 00: Layer pixel from constant color 01: Layer pixel from constant color

Bit(s)	Mnemonic	Name	Description
			10: Layer pixel from UFOd 11: Layer pixel from PQ
22		R_FIRST	**Right eye image first when in 3D mode** 0: Show left eye image first in 3D mode 1: Show right eye image first in 3D mode
21		LANDSCAPE	**Enables 3D landscape mode** 0: 3D portrait mode 1: 3D landscape mode
20		EN_3D	**Enables 3D mode** 0: 2D mode 1: 3D mode
8	**AEN**	ALPHA_EN	**Enables alpha blending** 0: Disable alpha blending 1: Enable alpha blending
7:0	**APHA**	ALPHA	**Constant alpha value**

1400B284 OVL_LC_SRCKEY Overlay Constant Layer Source Key 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SKEY**	SRCKEY	**Layer source color key** Active when source color key is enabled.

1400B288 OVL_LC_SRC_SIZE Overlay Layer C Source Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LC_SRC_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				LC_SRC_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**LCH**	LC_SRC_H	**Layer source height** Range: 0 ~ 4095
12:0	**LCW**	LC_SRC_W	**Layer source width** Range: 0 ~ 4095

1400B28C OVL_LC_OFFSET — Overlay Layer C Offset — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LC_YOFF											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					LC_XOFF											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**LCH**	LC_YOFF	**Layer vertical Y offset** Range: 0 ~ 4095
11:0	**LCXO**	LC_XOFF	**Layer horizontal X offset** Range: 0 ~ 4095

1400B290 OVL_LC_SRC_SEL — Overlay Constant Layer Source Selection — 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SURFL_EN	LC_BLEND_RND_SHT		LC_CONST_BLD	LC_DRGB_SEL_EXT	LC_DA_SEL_EXT	LC_SRGB_SEL_EXT	LC_SA_SEL_EXT	LC_D RGB_SEL		LC_D A_SEL		LC_S RGB_SEL		LC_SA_SEL	
Type	RW	RW		RW	RW	RW	RW	RW	RW		RW		RW		RW	
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CONST_LAYER_SEL		
Type														RW		
Reset														1	0	0

Bit(s)	Mnemonic	Name	Description
31	**LCSP**	SURFL_EN	**Enables layer surface dlinger alpha_blending** 0: Disable surface flinger alpha_blending 1: Enable surface flinger alpha_blending
30		LC_BLEND_RND_SHT	
28		LC_CONST_BLD	
27		LC_DRGB_SEL_EXT	**Selects layer destination_RGB alpha**
26		LC_DA_SEL_EXT	**Selects layer destination_Alpha alpha**
25		LC_SRGB_SEL_EXT	**Selects layer source_RGB alpha**
24		LC_SA_SEL_EXT	**Selects layer source_Alpha alpha**
23:22	**LCSP**	LC_DRGB_SEL	**Selects layer destination_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
21:20	**LCSP**	LC_DA_SEL	**Selects layer destination_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved

Bit(s)	Mnemonic	Name	Description
19:18	**LCSP**	LC_SRGB_SEL	**Selects layer source_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
17:16	**LCSP**	LC_SA_SEL	**Selects layer source_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
2:0	**LCSP**	CONST_LAYER_SE L	**Layer source pitch**

1400B29C OVL_BANK_CON Overlay Bank Control 00000008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												OVL_BANK_CON				
Type												RW				
Reset												0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		OVL_BANK_CON	

1400B2A0 OVL_FUNC_DCM0 Overlay Functional DCM0 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OVL_FUNC_DCM0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OVL_FUNC_DCM0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		OVL_FUNC_DCM0	Controls functional DCM0

1400B2A4 OVL_FUNC_DCM1 Overlay Functional DCM1 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OVL_FUNC_DCM1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OVL_FUNC_DCM1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		OVL_FUNC_DCM1	Controls functional DCM1

1400BFC0 OVL_SECURE Overlay Layer Secure Bit 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													L3_SECURE	L2_SECURE	L1_SECURE	L0_SECURE
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3		L3_SECURE	Layer 3 secure bit
2		L2_SECURE	Layer 2 secure bit
1		L1_SECURE	Layer 1 secure bit
0		L0_SECURE	Layer 0 secure bit

Module name: DISP_OVL1 Base address: (+1400c000h)

Address	Name	Width	Register Function
1400C000	OVL_STA	32	Overlay Status Monitor
1400C004	OVL_INTEN	32	Overlay Interrupt Enable
1400C008	OVL_INTSTA	32	Overlay Interrupt Status
1400C00C	OVL_EN	32	Overlay Enable
1400C010	OVL_TRIG	32	Overlay Trigger
1400C014	OVL_RST	32	Overlay Reset
1400C020	OVL_ROI_SIZE	32	Overlay ROI Size
1400C024	OVL_DATAPATH_CON	32	Overlay Datapath Control
1400C028	OVL_ROI_BGCLR	32	Overlay Background Color
1400C02C	OVL_SRC_CON	32	Overlay Source Control
1400C030	OVL_L0_CON	32	Overlay Layer 0 Control
1400C034	OVL_L0_SRCKEY	32	Overlay Layer 0 Source Key
1400C038	OVL_L0_SRC_SIZE	32	Overlay Layer 0 Source Size
1400C03C	OVL_L0_OFFSET	32	Overlay Layer 0 Offset
1400CF40	OVL_L0_ADDR	32	Overlay Layer 0 Memory Address
1400C044	OVL_L0_PITCH	32	Overlay Layer 0 Pitch
1400C048	OVL_L0_TILE	32	Overlay Layer 0 Tile Control

Address	Name	Width	Register Function
1400C04C	OVL_L0_CLIP	32	Overlay Layer 0 Clip
1400C050	OVL_L1_CON	32	Overlay Layer 1 Control
1400C054	OVL_L1_SRCKEY	32	Overlay Layer 1 Source Key
1400C058	OVL_L1_SRC_SIZE	32	Overlay Layer 1 Source Size
1400C05C	OVL_L1_OFFSET	32	Overlay Layer 1 Offset
1400CF60	OVL_L1_ADDR	32	Overlay Layer 1 Memory Address
1400C064	OVL_L1_PITCH	32	Overlay Layer 1 Pitch
1400C068	OVL_L1_TILE	32	Overlay Layer 1 Tile Control
1400C06C	OVL_L1_CLIP	32	Overlay Layer 1 Clip
1400C070	OVL_L2_CON	32	Overlay Layer 2 Control
1400C074	OVL_L2_SRCKEY	32	Overlay Layer 2 Source Key
1400C078	OVL_L2_SRC_SIZE	32	Overlay Layer 2 Source Size
1400C07C	OVL_L2_OFFSET	32	Overlay Layer 2 Offset
1400CF80	OVL_L2_ADDR	32	Overlay Layer 2 Memory Address
1400C084	OVL_L2_PITCH	32	Overlay Layer 2 Pitch
1400C088	OVL_L2_TILE	32	Overlay Layer 2 Tile Control
1400C08C	OVL_L2_CLIP	32	Overlay Layer 2 Clip
1400C090	OVL_L3_CON	32	Overlay Layer 3 Control
1400C094	OVL_L3_SRCKEY	32	Overlay Layer 3 Source Key
1400C098	OVL_L3_SRC_SIZE	32	Overlay Layer 3 Source Size
1400C09C	OVL_L3_OFFSET	32	Overlay Layer 3 Offset
1400CFA0	OVL_L3_ADDR	32	Overlay Layer 3 Memory Address
1400C0A4	OVL_L3_PITCH	32	Overlay Layer 3 Pitch
1400C0A8	OVL_L3_TILE	32	Overlay Layer 3 Tile Control
1400C0AC	OVL_L3_CLIP	32	Overlay Layer 3 Clip
1400C0C0	OVL_RDMA0_CTRL	32	Overlay RDMA0 Control
1400C0C8	OVL_RDMA0_MEM_GMC_SETTING1	32	Overlay RDMA0 Memory GMC Setting
1400C0CC	OVL_RDMA0_MEM_SLOW_CON	32	Overlay RDMA0 Memory Slow Control
1400C0D0	OVL_RDMA0_FIFO_CTRL	32	Overlay RDMA0 FIFO Control
1400C0E0	OVL_RDMA1_CTRL	32	Overlay RDMA1 Control
1400C0E8	OVL_RDMA1_MEM_GMC_SETTING1	32	Overlay RDMA1 Memory GMC Setting
1400C0EC	OVL_RDMA1_MEM_SLOW_CON	32	Overlay RDMA1 Memory Slow Control
1400C0F0	OVL_RDMA1_FIFO_CTRL	32	Overlay RDMA1 FIFO Control
1400C100	OVL_RDMA2_CTRL	32	Overlay RDMA2 Control
1400C108	OVL_RDMA2_MEM_GMC_SETTING1	32	Overlay RDMA2 Memory GMC Setting
1400C10C	OVL_RDMA2_MEM_SLOW_CON	32	Overlay RDMA2 Memory Slow Control
1400C110	OVL_RDMA2_FIFO_CTRL	32	Overlay RDMA2 FIFO Control
1400C120	OVL_RDMA3_CTRL	32	Overlay RDMA3 Control
1400C128	OVL_RDMA3_MEM_GMC_SETTING1	32	Overlay RDMA3 Memory GMC Setting

Address	Name	Width	Register Function
1400C12C	OVL_RDMA3_MEM_SLOW_CON	32	Overlay RDMA3 Memory Slow Control
1400C130	OVL_RDMA3_FIFO_CTRL	32	Overlay RDMA3 FIFO Control
1400C134	OVL_L0_Y2R_PARA_R0	32	Overlay L0 Y2R Conversion Parameter R0
1400C138	OVL_L0_Y2R_PARA_R1	32	Overlay L0 Y2R Conversion Parameter R1
1400C13C	OVL_L0_Y2R_PARA_G0	32	Overlay L0 Y2R Conversion Parameter G0
1400C140	OVL_L0_Y2R_PARA_G1	32	Overlay L0 Y2R Conversion Parameter G1
1400C144	OVL_L0_Y2R_PARA_B0	32	Overlay L0 Y2R Conversion Parameter B0
1400C148	OVL_L0_Y2R_PARA_B1	32	Overlay L0 Y2R Conversion Parameter B1
1400C14C	OVL_L0_Y2R_PARA_YUV_A_0	32	Overlay L0 Y2R Conversion Parameter Extended Add on YUV 0
1400C150	OVL_L0_Y2R_PARA_YUV_A_1	32	Overlay L0 Y2R Conversion Parameter Extended Add on YUV 1
1400C154	OVL_L0_Y2R_PARA_RGB_A_0	32	Overlay L0 Y2R Conversion Parameter Extended Add on RGB 0
1400C158	OVL_L0_Y2R_PARA_RGB_A_1	32	Overlay L0 Y2R Conversion Parameter Extended Add on RGB 1
1400C15C	OVL_L1_Y2R_PARA_R0	32	Overlay L1 Y2R Conversion Parameter R0
1400C160	OVL_L1_Y2R_PARA_R1	32	Overlay L1 Y2R Conversion Parameter R1
1400C164	OVL_L1_Y2R_PARA_G0	32	Overlay L1 Y2R Conversion Parameter G0
1400C168	OVL_L1_Y2R_PARA_G1	32	Overlay L1 Y2R Conversion Parameter G1
1400C16C	OVL_L1_Y2R_PARA_B0	32	Overlay L1 Y2R Conversion Parameter B0
1400C170	OVL_L1_Y2R_PARA_B1	32	Overlay L1 Y2R Conversion Parameter B1
1400C174	OVL_L1_Y2R_PARA_YUV_A_0	32	Overlay L1 Y2R Conversion Parameter Extended Add on YUV 0
1400C178	OVL_L1_Y2R_PARA_YUV_A_1	32	Overlay L1 Y2R Conversion Parameter Extended Add on YUV 1
1400C17C	OVL_L1_Y2R_PARA_RGB_A_0	32	Overlay L1 Y2R Conversion Parameter Extended Add on RGB 0
1400C180	OVL_L1_Y2R_PARA_RGB_A_1	32	Overlay L1 Y2R Conversion Parameter Extended Add on RGB 1
1400C184	OVL_L2_Y2R_PARA_R0	32	Overlay L2 Y2R Conversion Parameter R0
1400C188	OVL_L2_Y2R_PARA_R1	32	Overlay L2 Y2R Conversion Parameter R1
1400C18C	OVL_L2_Y2R_PARA_G0	32	Overlay L2 Y2R Conversion Parameter G0
1400C190	OVL_L2_Y2R_PARA_G1	32	Overlay L2 Y2R Conversion Parameter G1
1400C194	OVL_L2_Y2R_PARA_B0	32	Overlay L2 Y2R Conversion Parameter B0

Address	Name	Width	Register Function
1400C198	OVL_L2_Y2R_PARA_B1	32	Overlay L2 Y2R Conversion Parameter B1
1400C19C	OVL_L2_Y2R_PARA_YUV_A_0	32	Overlay L2 Y2R Conversion Parameter Extended Add on YUV 0
1400C1A0	OVL_L2_Y2R_PARA_YUV_A_1	32	Overlay L2 Y2R Conversion Parameter Extended Add on YUV 1
1400C1A4	OVL_L2_Y2R_PARA_RGB_A_0	32	Overlay L2 Y2R Conversion Parameter Extended Add on RGB 0
1400C1A8	OVL_L2_Y2R_PARA_RGB_A_1	32	Overlay L2 Y2R Conversion Parameter Extended Add on RGB 1
1400C1AC	OVL_L3_Y2R_PARA_R0	32	Overlay L3 Y2R Conversion Parameter R0
1400C1B0	OVL_L3_Y2R_PARA_R1	32	Overlay L3 Y2R Conversion Parameter R1
1400C1B4	OVL_L3_Y2R_PARA_G0	32	Overlay L3 Y2R Conversion Parameter G0
1400C1B8	OVL_L3_Y2R_PARA_G1	32	Overlay L3 Y2R Conversion Parameter G1
1400C1BC	OVL_L3_Y2R_PARA_B0	32	Overlay L3 Y2R Conversion Parameter B0
1400C1C0	OVL_L3_Y2R_PARA_B1	32	Overlay L3 Y2R Conversion Parameter B1
1400C1C4	OVL_L3_Y2R_PARA_YUV_A_0	32	Overlay L3 Y2R Conversion Parameter Extended Add on YUV 0
1400C1C8	OVL_L3_Y2R_PARA_YUV_A_1	32	Overlay L3 Y2R Conversion Parameter Extended Add on YUV 1
1400C1CC	OVL_L3_Y2R_PARA_RGB_A_0	32	Overlay L3 Y2R Conversion Parameter Extended Add on RGB 0
1400C1D0	OVL_L3_Y2R_PARA_RGB_A_1	32	Overlay L3 Y2R Conversion Parameter Extended Add on RGB 1
1400C1D4	OVL_DEBUG_MON_SEL	32	Overlay Debug Monitor Select
1400C1E0	OVL_RDMA0_MEM_GMC_SETTING2	32	Overlay RDMA0 Memory GMC Setting
1400C1E4	OVL_RDMA1_MEM_GMC_SETTING2	32	Overlay RDMA1 Memory GMC Setting
1400C1E8	OVL_RDMA2_MEM_GMC_SETTING2	32	Overlay RDMA2 Memory GMC Setting
1400C1EC	OVL_RDMA3_MEM_GMC_SETTING2	32	Overlay RDMA3 Memory GMC Setting
1400C1F0	OVL_RDMA_BURST_CON0	32	Overlay RDMA Burst Control
1400C1F4	OVL_RDMA_BURST_CON1	32	Overlay RDMA Burst Control
1400C1F8	OVL_RDMA_GREQ_NUM	32	Overlay RDMA GREQ Number
1400C1FC	OVL_RDMA_GREQ_URG_NUM	32	Overlay RDMA GREQ Number
1400C200	OVL_DUMMY_REG	32	Overlay Dummy Register
1400C208	OVL_GDRDY_PRD	32	Overlay SMI GDRDY Period
1400C20C	OVL_RDMA_ULTRA_SRC	32	Overlay RDMA Ultra SRC
1400C210	OVL_RDMA0_BUF_LOW	32	Overlay RDMA BUF Low

Address	Name	Width	Register Function
1400C214	OVL_RDMA1_BUF_LOW	32	Overlay RDMA BUF Low
1400C218	OVL_RDMA2_BUF_LOW	32	Overlay RDMA BUF Low
1400C21C	OVL_RDMA3_BUF_LOW	32	Overlay RDMA BUF Low
1400C230	OVL_SMI_DBG	32	Overlay SMI Arbiter Debug Monitor
1400C234	OVL_GREQ_LAYER_CNT	32	Overlay Layer GREQ Counter
1400C238	OVL_GDRDY_PRD_NUM	32	Overlay SMI GDRDY Period Number
1400C240	OVL_FLOW_CTRL_DBG	32	Overlay Flow Control Debug Monitor
1400C244	OVL_ADDCON_DBG	32	Overlay Address Control Debug
1400C24C	OVL_RDMA0_DBG	32	Overlay RDMA0 Debug Monitor
1400C250	OVL_RDMA1_DBG	32	Overlay RDMA1 Debug Monitor
1400C254	OVL_RDMA2_DBG	32	Overlay RDMA2 Debug Monitor
1400C258	OVL_RDMA3_DBG	32	Overlay RDMA3 Debug Monitor
1400C25C	OVL_L0_CLR	32	Overlay Layer 0 Constant Color
1400C260	OVL_L1_CLR	32	Overlay Layer 1 Constant Color
1400C264	OVL_L2_CLR	32	Overlay Layer 2 Constant Color
1400C268	OVL_L3_CLR	32	Overlay Layer 3 Constant Color
1400C26C	OVL_LC_CLR	32	Overlay Constant Layer Color
1400C270	OVL_CRC	32	Overlay CRC
1400C280	OVL_LC_CON	32	Overlay Constant Layer Control
1400C284	OVL_LC_SRCKEY	32	Overlay Constant Layer Source Key
1400C288	OVL_LC_SRC_SIZE	32	Overlay Layer C Source Size
1400C28C	OVL_LC_OFFSET	32	Overlay Layer C Offset
1400C290	OVL_LC_SRC_SEL	32	Overlay Constant Layer Source Selection
1400C29C	OVL_BANK_CON	32	Overlay Bank Control
1400C2A0	OVL_FUNC_DCM0	32	Overlay Functional DCM0 Control
1400C2A4	OVL_FUNC_DCM1	32	Overlay Functional DCM1 Control
1400CFC0	OVL_SECURE	32	Overlay Layer Secure Bit

1400C000 OVL_STA **Overlay Status Monitor** **0000001E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RDMA3_IDLE	RDMA2_IDLE	RDMA1_IDLE	RDMA0_IDLE	OVL_RUN
Type												RU	RU	RU	RU	RU
Reset												1	1	1	1	0

Bit(s)	Mnemonic	Name	Description
4		RDMA3_IDLE	**Status of overlay RDMA3**

Bit(s)	Mnemonic	Name	Description
			0: RDMA is in running. 1: Overlay RDMA are all idle.
3		RDMA2_IDLE	**Status of overlay RDMA2** 0: RDMA is in running. 1: Overlay RDMA are all idle.
2		RDMA1_IDLE	**Status of overlay RDMA1** 0: RDMA is in running. 1: Overlay RDMA are all idle.
1		RDMA0_IDLE	**Status of overlay RDMA0** 0: RDMA is in running. 1: Overlay RDMA are all idle.
0		OVL_RUN	**Status of overlay engine** 0: Overlay is idle. 1: Overlay is running.

1400C004 OVL_INTEN **Overlay Interrupt Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ABNORMAL_SOF_INTEN	RDMA3_SMI_UNDERFLOW_INTEN	RDMA2_SMI_UNDERFLOW_INTEN	RDMA1_SMI_UNDERFLOW_INTEN	RDMA0_SMI_UNDERFLOW_INTEN	RDMA3_EOF_ABNORMAL_INTEN	RDMA2_EOF_ABNORMAL_INTEN	RDMA1_EOF_ABNORMAL_INTEN	RDMA0_EOF_ABNORMAL_INTEN	OVL_FME_HWRST_DONE_INTEN	OVL_FME_SWRST_DONE_INTEN	OVL_FME_UND_INTEN	OVL_FME_CPL_INTEN	OVL_REG_CMT_INTEN
Type			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13		ABNORMAL_SOF_INTEN	**Control abnormal SOF interrupt**
12		RDMA3_SMI_UNDERFLOW_INTEN	**Control RDMA3 SMI Underflow interrupt** 0: Disable RDMA3 SMI data underflow interrupt 1: Enable RDMA3 SMI data underflow interrupt
11		RDMA2_SMI_UNDERFLOW_INTEN	**Control RDMA2 SMI Underflow interrupt** 0: Disable RDMA2 SMI data underflow interrupt 1: Enable RDMA2 SMI data underflow interrupt
10		RDMA1_SMI_UNDERFLOW_INTEN	**Control RDMA1 SMI underflow interrupt** 0: Disable RDMA1 SMI data underflow interrupt 1: Enable RDMA1 SMI data underflow interrupt
9		RDMA0_SMI_UNDERFLOW_INTEN	**Control RDMA0 SMI underflow interrupt** 0: Disable RDMA0 SMI data underflow interrupt 1: Enable RDMA0 SMI data underflow interrupt
8		RDMA3_EOF_ABNORMAL_INTEN	**Control RDMA3 EOF abnormal interrupt** 0: Disable RDMA3 EOF abnormal interrupt 1: Enable RDMA3 EOF abnormal interrupt
7		RDMA2_EOF_ABNORMAL_INTEN	**Control RDMA2 EOF abnormal interrupt** 0: Disable RDMA2 EOF abnormal interrupt 1: Enable RDMA2 EOF abnormal interrupt
6		RDMA1_EOF_ABNORMAL_INTEN	**Control RDMA1 EOF abnormal interrupt** 0: Disable RDMA1 EOF abnormal interrupt 1: Enable RDMA1 EOF abnormal interrupt

Bit(s)	Mnemonic	Name	Description
5		RDMA0_EOF_ABNORMAL_INTEN	**Control RDMA0 EOF abnormal interrupt** 0: Disable RDMA0 EOF abnormal interrupt 1: Enable RDMA0 EOF abnormal interrupt
4		OVL_FME_HWRST_DONE_INTEN	**Control frame HW reset done interrupt** 0: Disable frame HW reset done interrupt 1: Enable frame HW reset done interrupt
3		OVL_FME_SWRST_DONE_INTEN	**Control frame SW reset done interrupt** 0: Disable frame SW reset done interrupt 1: Enable frame SW reset done interrupt
2		OVL_FME_UND_INTEN	**Control frame underflow interrupt** 0: Disable frame underflow interrupt 1: Enable frame underflow interrupt
1		OVL_FME_CPL_INTEN	**Control frame complete interrupt** 0: Disable frame complete interrupt 1: Enable frame complete interrupt
0		OVL_REG_CMT_INTEN	**Control register setting complete interrupt** 0: Disable register commit interrupt 1: Enable register commit interrupt

1400C008 OVL_INTSTA **Overlay Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ABNORMAL_SOF_INTSTA	RDMA3_SMI_UNDERFLOW_INTSTA	RDMA2_SMI_UNDERFLOW_INTSTA	RDMA1_SMI_UNDERFLOW_INTSTA	RDMA0_SMI_UNDERFLOW_INTSTA	RDMA3_EOF_ABNORMAL_INTSTA	RDMA2_EOF_ABNORMAL_INTSTA	RDMA1_EOF_ABNORMAL_INTSTA	RDMA0_EOF_ABNORMAL_INTSTA	OVL_FME_HWRST_DONE_INTSTA	OVL_FME_SWRST_DONE_INTSTA	OVL_FME_UND_INTSTA	OVL_FME_CPL_INTSTA	OVL_REG_CMT_INTSTA
Type			A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13		ABNORMAL_SOF_INTSTA	
12		RDMA3_SMI_UNDERFLOW_INTSTA	**RDMA3 SMI status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA3 SMI data are not underflow. 1: RDMA3 SMI data are underflow.
11		RDMA2_SMI_UNDERFLOW_INTSTA	**RDMA2 SMI status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA2 SMI data are not underflow. 1: RDMA2 SMI data are underflow.
10		RDMA1_SMI_UNDERFLOW_INTSTA	**RDMA1 SMI status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA1 SMI data are not underflow. 1: RDMA1 SMI data are underflow.
9		RDMA0_SMI_UNDERFLOW_INTSTA	**RDMA0 SMI status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless.

Bit(s)	Mnemonic	Name	Description
			0: RDMA0 SMI data are not underflow. 1: RDMA0 SMI data are underflow.
8		RDMA3_EOF_ABNORMAL_INTSTA	**RDMA3 status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA3 complete normally 1: RDMA3 not complete till EOF
7		RDMA2_EOF_ABNORMAL_INTSTA	**RDMA2 status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA2 complete normally 1: RDMA2 not complete till EOF
6		RDMA1_EOF_ABNORMAL_INTSTA	**RDMA1 status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA1 complete normally 1: RDMA1 not complete till EOF
5		RDMA0_EOF_ABNORMAL_INTSTA	**RDMA0 status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA0 complete normally 1: RDMA0 not complete till EOF
4		OVL_FME_HWRST_DONE_INTSTA	**Overlay HW reset done status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: No HW reset/HW reset is not done. 1: HW reset is done.
3		OVL_FME_SWRST_DONE_INTSTA	**Overlay SW reset done status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: No SW reset/SW reset is not done. 1: SW reset is done.
2		OVL_FME_UND_INTSTA	**Overlay frame underflow status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: Frame complete w/o underflow 1: Frame not complete w/ underflow
1		OVL_FME_CPL_INTSTA	**Overlay frame complete status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: Frame not complete 1: Frame complete
0		OVL_REG_CMT_INTSTA	**Overlay register commit status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: Regsiter is not set from shadow register to working register. 1: Register is set to working register done.

1400C00C OVL_EN **Overlay Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																IGNORE_ABNORMAL_SOF
Type																RW

Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							HG_FSMI_CK_ON	HG_FOVL_CK_ON								OVL_EN
Type							RW	RW								RW
Reset							0	0								0

Bit(s)	Mnemonic	Name	Description
16		IGNORE_ABNORMAL_SOF	
9		HG_FSMI_CK_ON	
8		HG_FOVL_CK_ON	
0	**OVEN**	OVL_EN	**Enables overlay engine** 0: Disable overlay 1: Enable overlay

1400C010 OVL_TRIG **Overlay Trigger** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							CRC_CLR	CRC_EN								OVL_SW_TRIG
Type							RW	RW								RW
Reset							0	0								0

Bit(s)	Mnemonic	Name	Description
9		CRC_CLR	
8		CRC_EN	
0	**OVTR**	OVL_SW_TRIG	**SW trigger to enable overlay engine** 0: When using HW trigger (SOF), this bit should be 0. 1: SW control to enable overlay engine.

1400C014 OVL_RST **Overlay Reset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OVL_SMI_IOBUF_HARD_RST	OVL_SMI_IOBUF_RST	OVL_SMI_HARD_RST	OVL_SMI_RST												
Type	RW	RW	RW	RW												
Reset	0	0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																OVL_RST
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
31		OVL_SMI_IOBUF_HARD_RST	**OVL is forced to reset when SMI BUSY hang issue occurs (careful)**
30		OVL_SMI_IOBUF_RST	
29		OVL_SMI_HARD_RST	
28		OVL_SMI_RST	
0		OVL_RST	**Overlay SW reset control for engine (high active)** 1: Reset engine

1400C020 OVL_ROI_SIZE **Overlay ROI Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				ROI_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				ROI_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**ROIH**	ROI_H	**Overlay ROI width** Range: 1 ~ 8191. For 3D display, this value should be 2 ~ 8191.
12:0	**ROIW**	ROI_W	**Overlay ROI width** Range: 1 ~ 8191. For 3D display, this value should be 2 ~ 8191.

1400C024 OVL_DATAPATH_CON **Overlay Datapath Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									RDMA3_OUT_SEL	RDMA2_OUT_SEL	RDMA1_OUT_SEL	RDMA0_OUT_SEL			PQ_OUT_SEL	
Type									OTHER	OTHER	OTHER	OTHER			OTHER	
Reset									0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OVL_GAMMA_OUT	ADOBE_LAYER		ADOBE_MODE	L3_GPU_MODE	L2_GPU_MODE	L1_GPU_MODE	L0_GPU_MODE					OUTPUT_NO_RND	BGCLR_IN_SEL	OVL_RANDOM_BGCLR_EN	LAYER_SMI_ID_EN
Type	RW	RW		RW	RW	RW	RW	RW					RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
23	**RDMA3SEL**	RDMA3_OUT_SEL	**Selects output path of RDMA3** 0: OVL Layer 3 1: PQ direct link output
22	**RDMA2SEL**	RDMA2_OUT_SEL	**Selects output path of RDMA2** 0: OVL Layer 2 1: PQ direct link output
21	**RDMA1SEL**	RDMA1_OUT_SEL	**Selects output path of RDMA1** 0: OVL Layer 1 1: PQ direct link output
20	**RDMA0SEL**	RDMA0_OUT_SEL	**Selects output path of RDMA0** 0: OVL Layer 0 1: PQ direct link output
17:16	**PQSEL**	PQ_OUT_SEL	**Selects PQ direct link output data** 00: RDMA0 01: RDMA1 10: RDMA2 11: RDMA3
15	**OVL_GAMMA_OUT**	OVL_GAMMA_OUT	**Wide-gamut OVL output GAMMA table path** (shares GAMMA-table with layer Adobe_mode) 0: Disable OVL output GAMMA table 1: Enable OVL output GAMMA table
14:13	**ADOBE_LAYER**	ADOBE_LAYER	**Selects wide-gamut layer Adobe** 0: Select Layer 0 adobe_path 1: Select Layer 1 adobe_path 2: Select Layer 2 adobe_path 3: Select Layer 3 adobe_path
12	**ADOBE**	ADOBE_MODE	**Wide-gamut layer Adobe mode** (shares GAMMA-table with ovl_gamma_out mode) 0: Disable layer Adobe path 1: Enable layer Adobe path
11	**L3_GPU**	L3_GPU_MODE	**Wide-gamut Layer 3 GPU path mode** 0: Disable Layer 3 GPU path 1: Enable Layer 3 GPU path
10	**L2_GPU**	L2_GPU_MODE	**Wide-gamut Layer 2 GPU path mode** 0: Disable Layer 2 GPU path 1: Enable Layer 2 GPU path
9	**L1_GPU**	L1_GPU_MODE	**Wide-gamut Layer 1 GPU path mode** 0: Disable Layer 1 GPU path 1: Enable Layer 1 GPU path
8	**L0_GPU**	L0_GPU_MODE	**Wide-gamut Layer 0 GPU path mode** 0: Disable Layer 0 GPU path 1: Enable Layer 0 GPU path
3		OUTPUT_NO_RND	
2		BGCLR_IN_SEL	**OVL BGCLR direct link path** 0: Disable OVL BGCLR direct link input 1: Enable OVL BGCLR direct link input
1		OVL_RANDOM_BGCLR_EN	**When OVL_RANDOM_BGCLR_EN=1, layer_en[i] should be set to 0 to allow the background color to pass through the Blend engine.** 0: Disable random background color pattern 1: Enable random background color pattern
0	**LAYER_SMI_ID_EN**	LAYER_SMI_ID_E N	**Supports OVL SMI ID function** 0: Disable SMI ID 1: Enable SMI ID

1400C028 OVL_ROI_BGCLR Overlay Background Color FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24	**BGDA**	ALPHA	Alpha component of ROI window background color
23:16	**BGDR**	RED	Red component of ROI window background color
15:8	**BGDG**	GREEN	Green component of ROI window background color
7:0	**BGDB**	BLUE	Blue component of ROI window background color

1400C02C OVL_SRC_CON Overlay Source Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												LC_EN	L3_EN	L2_EN	L1_EN	L0_EN
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4	**LCEN**	LC_EN	**Set up this bit to enable overlay constant layer.** 0: Disable constant layer 1: Enable constant layer
3	**L3EN**	L3_EN	**Set up this bit to enable overlay Layer 3.** 0: Disable Layer 3 1: Enable Layer 3
2	**L2EN**	L2_EN	**Set up this bit to enable overlay Layer 2.** 0: Disable Layer 2 1: Enable Layer 2
1	**L1EN**	L1_EN	**Set up this bit to enable overlay Layer 1.** 0: Disable Layer 1 1: Enable Layer 1
0	**L0EN**	L0_EN	**Set up this bit to enable overlay Layer 0.** 0: Disable Layer 0 1: Enable Layer 0

1400C030 OVL_L0_CON Overlay Layer 0 Control 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSTKEY_EN	SRCKEY_EN	LAYER_SRC		MTX_EN	MTX_AUTO_DIS	RGB_SWAP	BYTE_SWAP	CLRFMT_MAN	R_FIRST	LANDSCAPE	EN_3D	INT_MTX_SEL			

Type	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLRFMT				EXT_MTX_EN	HORIZONTAL_FLIP_EN	VERTICAL_FLIP_EN	ALPHA_EN	ALPHA							
Type	RW				OTHER	RW	RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**DKEN**	DSTKEY_EN	**Enables destination color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable destination color key 1: Enable destination color key
30	**SKEN**	SRCKEY_EN	**Enables source color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable source color key 1: Enable source color key
29:28	**LSRC**	LAYER_SRC	**Selects layer pixel from memory/constant color/SCL/PQ** 00: Layer pixel from memory RDMA0 01: Layer pixel from constant color 10: Layer pixel from UFOd 11: Layer pixel from PQ
27		MTX_EN	
26		MTX_AUTO_DIS	
25	**RGSW**	RGB_SWAP	**No use**
24	**BTSW**	BYTE_SWAP	**Swaps unified color format** 0: RGB565, BGR888, BGRA8888, ABGR8888, UYVY, YUYV 1: BGR565, RGB888, RGBA8888, ARGB8888, VYUY, YVYU
23		CLRFMT_MAN	
22		R_FIRST	**Right eye image first when in 3D mode** 0: Show left eye image first in 3D mode 1: Show right eye image first in 3D mode
21		LANDSCAPE	**Enables 3D landscape mode** 0: 3D portrait mode 1: 3D landscape mode
20		EN_3D	**Enables 3D mode** 0: 2D mode 1: 3D mode
19:16	**MTX**	INT_MTX_SEL	**Selects color matrix table** 0000: MTX_RGB_TO_JPEG 0010: MTX_RGB_TO_BT601 0011: MTX_RGB_TO_BT709 0100: MTX_JPEG_TO_RGB 0110: MTX_BT601_TO_RGB 0111: MTX_BT709_TO_RGB 1000: MTX_JPEG_TO_BT601 1001: MTX_JPEG_TO_BT709 1010: MTX_BT601_TO_JPEG 1011: MTX_BT709_TO_JPEG 1100: MTX_BT709_TO_BT601

Bit(s)	Mnemonic	Name	Description
			1101: MTX_BT601_TO_BT709 Others: HW default (JPEG_TO_RGB)
15:12	**CFMT**	CLRFMT	**//--OLD define for reference only** 0000: RGB888 0001: RGB565 0010: ARGB8888 0011: PARGB8888 0100: xARGB8888 1000: YUYV 1001: UYVY 1010: YVYU 1011: VYUY 1111: YUV444 Others: Reserved color format 0000: RGB565 0001: RGB888 0010: RGBA8888/BGRA8888 0011: ARGB8888/ABGR8888 0100: UVVY, VYUY 0101: YUYV, YVYU
11	**MTXEN**	EXT_MTX_EN	**Enables external programmable coeff** 0: Matrix coeff 1: Programmable coeff
10	**HFE**	HORIZONTAL_FLIP_EN	**Enables horizontal flip** 0: Disable horizontal flip 1: Enable horizontal flip
9	**VFE**	VERTICAL_FLIP_ EN	**Enables vertical flip** 0: Disable vertical flip 1: Enable vertical flip
8	**AEN**	ALPHA_EN	**Enables alpha blending** 0: Disable alpha blending 1: Enable alpha blending
7:0	**APHA**	ALPHA	**Constant alpha value**

1400C034 OVL_L0_SRC_KEY **Overlay Layer 0 Source Key** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SKEY**	SRCKEY	**Layer source color key** Active when source color key is enabled.

1400C038 OVL_L0_SRC_SIZE **Overlay Layer 0 Source Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name				Lo_SRC_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				Lo_SRC_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**LoH**	Lo_SRC_H	**Layer source height** Range: 0 ~ 8191
12:0	**LoW**	Lo_SRC_W	**Layer source width** Range: 0 ~ 8191

1400C03C OVL_Lo_OFFSET **Overlay Layer 0 Offset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				Lo_YOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				Lo_XOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**LoH**	Lo_YOFF	**Layer vertical Y offset** Range: 0 ~ 8191
12:0	**LoXO**	Lo_XOFF	**Layer horizontal X offset** Range: 0 ~ 8191

1400CF40 OVL_Lo_ADDR **Overlay Layer 0 Memory Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Lo_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Lo_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**LoAD**	Lo_ADDR	Layer memory buffer address

1400C044 OVL_Lo_PITCH **Overlay Layer 0 Pitch** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SURFL_EN	Lo_BLEND_RND_SHT		Lo_CONST_BLD	Lo_DRGB_SEL_EXT	Lo_DA_SEL_EXT	Lo_SRGB_SEL_EXT	Lo_SA_SEL_EXT	Lo_DRGB_SEL		Lo_DA_SEL		Lo_SRGB_SEL		Lo_SA_SEL	
Type	RW	RW		RW	RW	RW	RW	RW	RW		RW		RW		RW	
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Lo_SRC_PITCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**LoSP**	SURFL_EN	**Enables layer surface dlinger alpha_blending** 0: Disable surface flinger alpha_blending 1: Enable surface flinger alpha_blending
30		Lo_BLEND_RND_SHT	
28		Lo_CONST_BLD	
27		Lo_DRGB_SEL_EXT	**Selects layer destination_RGB alpha**
26		Lo_DA_SEL_EXT	**Selects layer destination_Alpha alpha**
25		Lo_SRGB_SEL_EXT	**Selects layer source_RGB alpha**
24		Lo_SA_SEL_EXT	**Selects layer source_Alpha alpha**
23:22	**LoSP**	Lo_DRGB_SEL	**Selects layer destination_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
21:20	**LoSP**	Lo_DA_SEL	**Selects layer destination_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
19:18	**LoSP**	Lo_SRGB_SEL	**Selects layer source_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
17:16	**LoSP**	Lo_SA_SEL	**Selects layer source_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
15:0	**LoSP**	Lo_SRC_PITCH	**Layer source pitch**

1400C048 OVL_Lo_TILE Overlay Layer 0 Tile Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TILE_HORI_BLOCK_NUM										TILE_EN	TILE_WIDTH_SEL	TILE_HEIGHT			
Type	OTHER										OTHER	OTHER	OTHER			
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	TILE_HEIGHT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**TILE_BLKS**	TILE_HORI_BLOCK_NUM	**Number of horizontal blocks**
21	**TILE_EN**	TILE_EN	**Enables tile mode** 0: Disable 1: Enable
20	**TILE_W**	TILE_WIDTH_SEL	**Width of tile** 0: 16 1: 32
19:0	**TILE_H**	TILE_HEIGHT	**Height of source tile mode**

1400C04C OVL_L0_CLIP Overlay Layer 0 Clip 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L0_SRC_BOTTOM_CLIP								L0_SRC_TOP_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L0_SRC_RIGHT_CLIP								L0_SRC_LEFT_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**L0_SRC_BOTTOM_CLIP**	L0_SRC_BOTTOM_CLIP	Layer 0 bottom clip
23:16	**L0_SRC_TOP_CLIP**	L0_SRC_TOP_CLIP	Layer 0 top clip
15:8	**L0_SRC_RIGHT_CLIP**	L0_SRC_RIGHT_CLIP	Layer 0 right clip
7:0	**L0_SRC_LEFT_CLIP**	L0_SRC_LEFT_CLIP	Layer 0 left clip

1400C050 OVL_L1_CON Overlay Layer 1 Control 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSTKEY_EN	SRCKEY_EN	LAYER_SRC		MTX_EN	MTX_AUTO_DIS	RGB_SWAP	BYTE_SWAP	CLRFMT_MAN	R_FIRST	LANDSCAPE	EN_3D	INT_MTX_SEL			
Type	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLRFMT				EXT_MTX_EN	HORIZONTAL_FLIP_EN	VERTICAL_FLIP_EN	ALPHA_EN	ALPHA							
Type	RW				OTHER	RW	RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**DKEN**	DSTKEY_EN	**Enables destination color key**

Bit(s)	Mnemonic	Name	Description
			SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable destination color key 1: Enable destination color key
30	**SKEN**	SRCKEY_EN	**Enables source color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable source color key 1: Enable source color key
29:28	**LSRC**	LAYER_SRC	**Selects layer pixel from memory/constant color/SCL/PQ** 00: Layer pixel from memory RDMA1 01: Layer pixel from constant color 10: Layer pixel from UFOd 11: Layer pixel from PQ
27		MTX_EN	
26		MTX_AUTO_DIS	
25	**RGSW**	RGB_SWAP	**No use**
24	**BTSW**	BYTE_SWAP	**Swaps unified color format** 0: RGB565, BGR888, BGRA8888, ABGR8888, UYVY, YUYV 1: BGR565, RGB888, RGBA8888, ARGB8888, VYUY, YVYU
23		CLRFMT_MAN	
22		R_FIRST	**Right eye image first when in 3D mode** 0: Show left eye image first in 3D mode 1: Show right eye image first in 3D mode
21		LANDSCAPE	**Enables 3D landscape mode** 0: 3D portrait mode 1: 3D landscape mode
20		EN_3D	**Enables 3D mode** 0: 2D mode 1: 3D mode
19:16	**MTX**	INT_MTX_SEL	**Selects color matrix table** 0000: MTX_RGB_TO_JPEG 0010: MTX_RGB_TO_BT601 0011: MTX_RGB_TO_BT709 0100: MTX_JPEG_TO_RGB 0110: MTX_BT601_TO_RGB 0111: MTX_BT709_TO_RGB 1000: MTX_JPEG_TO_BT601 1001: MTX_JPEG_TO_BT709 1010: MTX_BT601_TO_JPEG 1011: MTX_BT709_TO_JPEG 1100: MTX_BT709_TO_BT601 1101: MTX_BT601_TO_BT709 Others: HW default (JPEG_TO_RGB)
15:12	**CFMT**	CLRFMT	**//--OLD define for reference only** 0000: RGB888 0001: RGB565 0010: ARGB8888 0011: PARGB8888 0100: xARGB8888 1000: YUYV 1001: UYVY 1010: YVYU 1011: VYUY

Bit(s)	Mnemonic	Name	Description
			1111: YUV444 Others: Reserved color format 0000: RGB565 0001: RGB888 0010: RGBA8888/BGRA8888 0011: ARGB8888/ABGR8888 0100: UVVY, VYUY 0101: YUYV, YVYU
11	**MTXEN**	EXT_MTX_EN	**Enables external programmable coeff** 0: Matrix coeff 1: Programmable coeff
10	**HFE**	HORIZONTAL_FLIP_EN	**Enables horizontal flip** 0: Disable horizontal flip 1: Enable horizontal flip
9	**VFE**	VERTICAL_FLIP_ EN	**Enables vertical flip** 0: Disable vertical flip 1: Enable vertical flip
8	**AEN**	ALPHA_EN	**Enables alpha blending** 0: Disable alpha blending 1: Enable alpha blending
7:0	**APHA**	ALPHA	**Constant alpha value**

1400C054 OVL_L1_SRCKEY **Overlay Layer 1 Source Key** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SKEY**	SRCKEY	**Layer source color key** Active when source color key is enabled.

1400C058 OVL_L1_SRCSIZE **Overlay Layer 1 Source Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L1_SRC_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L1_SRC_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**L1H**	L1_SRC_H	**Layer source height**

Bit(s)	Mnemonic	Name	Description
12:0	**L1W**	L1_SRC_W	Range: 0 ~ 8191 **Layer source width** Range: 0 ~ 8191

1400C05C OVL_L1_OFFSET Overlay Layer 1 Offset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L1_YOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L1_XOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**L1H**	L1_YOFF	**Layer vertical Y offset** Range: 0 ~ 8191
12:0	**L1XO**	L1_XOFF	**Layer horizontal X offset** Range: 0 ~ 8191

1400CF60 OVL_L1_ADDR Overlay Layer 1 Memory Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L1_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L1_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**L1AD**	L1_ADDR	Layer memory buffer address

1400C064 OVL_L1_PITCH Overlay Layer 1 Pitch 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SURFL_EN	L1_BLEND_RND_SHT		L1_CONST_BLD	L1_DRGB_SEL_EXT	L1_DA_SEL_EXT	L1_SRGB_SEL_EXT	L1_SA_SEL_EXT	L1_DRGB_SEL		L1_DA_SEL		L1_SRGB_SEL		L1_SA_SEL	
Type	RW	RW		RW	RW	RW	RW	RW	RW		RW		RW		RW	
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L1_SRC_PITCH															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	L1SP	SURFL_EN	**Enables layer surface dlinger alpha_blending** 0: Disable surface flinger alpha_blending 1: Enable surface flinger alpha_blending
30		L1_BLEND_RND_SHT	
28		L1_CONST_BLD	
27		L1_DRGB_SEL_EXT	**Selects layer destination_RGB alpha**
26		L1_DA_SEL_EXT	**Selects layer destination_Alpha alpha**
25		L1_SRGB_SEL_EXT	**Selects layer source_RGB alpha**
24		L1_SA_SEL_EXT	**Selects layer source_Alpha alpha**
23:22	L1SP	L1_DRGB_SEL	**Selects layer destination_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
21:20	L1SP	L1_DA_SEL	**Selects layer destination_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
19:18	L1SP	L1_SRGB_SEL	**Selects layer source_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
17:16	L1SP	L1_SA_SEL	**Selects layer source_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
15:0	L1SP	L1_SRC_PITCH	**Layer source pitch**

1400C068 OVL_L1_TILE **Overlay Layer 1 Tile Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TILE_HORI_BLOCK_NUM										TILE_EN	TILE_WIDTH_SEL	TILE_HEIGHT			
Type	OTHER										OTHER	OTHER	OTHER			
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TILE_HEIGHT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	TILE_BLKS	TILE_HORI_BLOCK_NUM	**Number of horizontal blocks**
21	TILE_EN	TILE_EN	**Enables tile mode** 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable
20	**TILE_W**	TILE_WIDTH_SEL	**Width of tile** 0: 16 1: 32
19:0	**TILE_H**	TILE_HEIGHT	**Height of source tile mode**

1400C06C OVL_L1_CLIP **Overlay Layer 1 Clip** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L1_SRC_BOTTOM_CLIP								L1_SRC_TOP_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L1_SRC_RIGHT_CLIP								L1_SRC_LEFT_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**L1_SRC_BOTTOM_CLIP**	L1_SRC_BOTTOM_CLIP	Layer 1 bottom clip
23:16	**L1_SRC_TOP_CLIP**	L1_SRC_TOP_CLIP	Layer 1 top clip
15:8	**L1_SRC_RIGHT_CLIP**	L1_SRC_RIGHT_CLIP	Layer 1 right clip
7:0	**L1_SRC_LEFT_CLIP**	L1_SRC_LEFT_CLIP	Layer 1 left clip

1400C070 OVL_L2_CON **Overlay Layer 2 Control** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSTKEY_EN	SRCKEY_EN	LAYER_SRC		MTX_EN	MTX_AUTO_DIS	RGB_SWAP	BYTE_SWAP	CLRFMT_MAN	R_FIRST	LANDSCAPE	EN_3D	INT_MTX_SEL			
Type	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLRFMT				EXT_MTX_EN	HORIZONTAL_FLIP_EN	VERTICAL_FLIP_EN	ALPHA_EN	ALPHA							
Type	RW				OTHER	RW	RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**DKEN**	DSTKEY_EN	**Enables destination color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable destination color key 1: Enable destination color key
30	**SKEN**	SRCKEY_EN	**Enables source color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable source color key 1: Enable source color key

Bit(s)	Mnemonic	Name	Description
29:28	**LSRC**	LAYER_SRC	**Selects layer pixel from memory/constant color/SCL/PQ** 00: Layer pixel from memory RDMA2 01: Layer pixel from constant color 10: Layer pixel from UFOd 11: Layer pixel from PQ
27		MTX_EN	
26		MTX_AUTO_DIS	
25	**RGSW**	RGB_SWAP	**No use**
24	**BTSW**	BYTE_SWAP	**Swaps unified color format** 0: RGB565, BGR888, BGRA8888, ABGR8888, UYVY, YUYV 1: BGR565, RGB888, RGBA8888, ARGB8888, VYUY, YVYU
23		CLRFMT_MAN	
22		R_FIRST	**Right eye image first when in 3D mode** 0: Show left eye image first in 3D mode 1: Show right eye image first in 3D mode
21		LANDSCAPE	**Enables 3D landscape mode** 0: 3D portrait mode 1: 3D landscape mode
20		EN_3D	**Enables 3D mode** 0: 2D mode 1: 3D mode
19:16	**MTX**	INT_MTX_SEL	**Selects color matrix table** 0000: MTX_RGB_TO_JPEG 0010: MTX_RGB_TO_BT601 0011: MTX_RGB_TO_BT709 0100: MTX_JPEG_TO_RGB 0110: MTX_BT601_TO_RGB 0111: MTX_BT709_TO_RGB 1000: MTX_JPEG_TO_BT601 1001: MTX_JPEG_TO_BT709 1010: MTX_BT601_TO_JPEG 1011: MTX_BT709_TO_JPEG 1100: MTX_BT709_TO_BT601 1101: MTX_BT601_TO_BT709 Others: HW default (JPEG_TO_RGB)
15:12	**CFMT**	CLRFMT	**//--OLD define for reference only** 0000: RGB888 0001: RGB565 0010: ARGB8888 0011: PARGB8888 0100: xARGB8888 1000: YUYV 1001: UYVY 1010: YVYU 1011: VYUY 1111: YUV444 Others: Reserved color format 0000: RGB565 0001: RGB888 0010: RGBA8888/BGRA8888 0011: ARGB8888/ABGR8888 0100: UVVY, VYUY 0101: YUYV, YVYU
11	**MTXEN**	EXT_MTX_EN	**Enables external programmable coeff**

Bit(s)	Mnemonic	Name	Description
			0: Matrix coeff 1: Programmable coeff
10	**HFE**	HORIZONTAL_FLIP_EN	**Enables horizontal flip** 0: Disable horizontal flip 1: Enable horizontal flip
9	**VFE**	VERTICAL_FLIP_ EN	**Enables vertical flip** 0: Disable vertical flip 1: Enable vertical flip
8	**AEN**	ALPHA_EN	**Enables alpha blending** 0: Disable alpha blending 1: Enable alpha blending
7:0	**APHA**	ALPHA	**Constant alpha value**

1400C074 OVL_L2_SRCKEY Overlay Layer 2 Source Key 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SKEY**	SRCKEY	**Layer source color key** Active when source color key is enabled.

1400C078 OVL_L2_SRCSIZE Overlay Layer 2 Source Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L2_SRC_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L2_SRC_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**L2H**	L2_SRC_H	**Layer source height** Range: 0 ~ 8191
12:0	**L2W**	L2_SRC_W	**Layer source width** Range: 0 ~ 8191

1400C07C OVL_L2_OFFSET Overlay Layer 2 Offset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L2_YOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L2_XOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**L2H**	L2_YOFF	**Layer vertical Y offset** Range: 0 ~ 8191
12:0	**L2XO**	L2_XOFF	**Layer horizontal X offset** Range: 0 ~ 8191

1400CF80 OVL_L2_ADDR **Overlay Layer 2 Memory Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L2_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L2_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**L2AD**	L2_ADDR	Layer memory buffer address

1400C084 OVL_L2_PITCH **Overlay Layer 2 Pitch** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SURFL_EN	L2_BLEND_RND_SHT		L2_CONST_BLD	L2_DRGB_SEL_EXT	L2_DA_SEL_EXT	L2_SRGB_SEL_EXT	L2_SA_SEL_EXT	L2_DRGB_SEL		L2_DA_SEL		L2_SRGB_SEL		L2_SA_SEL	
Type	RW	RW		RW	RW	RW	RW	RW	RW		RW		RW		RW	
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L2_SRC_PITCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**L2SP**	SURFL_EN	**Enables layer surface dlinger alpha_blending** 0: Disable surface flinger alpha_blending 1: Enable surface flinger alpha_blending
30		L2_BLEND_RND_SHT	
28		L2_CONST_BLD	

Bit(s)	Mnemonic	Name	Description
27		L2_DRGB_SEL_EXT	**Selects layer destination_RGB alpha**
26		L2_DA_SEL_EXT	**Selects layer destination_Alpha alpha**
25		L2_SRGB_SEL_EXT	**Selects layer source_RGB alpha**
24		L2_SA_SEL_EXT	**Selects layer source_Alpha alpha**
23:22	**L2SP**	L2_DRGB_SEL	**Selects layer destination_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
21:20	**L2SP**	L2_DA_SEL	**Selects layer destination_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
19:18	**L2SP**	L2_SRGB_SEL	**Selects layer source_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
17:16	**L2SP**	L2_SA_SEL	**Selects layer source_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
15:0	**L2SP**	L2_SRC_PITCH	**Layer source pitch**

1400C088 OVL_L2_TILE **Overlay Layer 2 Tile Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TILE_HORI_BLOCK_NUM										TILE_EN	TILE_WIDTH_SEL	TILE_HEIGHT			
Type	OTHER										OTHER	OTHER	OTHER			
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TILE_HEIGHT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**TILE_BLKS**	TILE_HORI_BLOCK_NUM	**Number of horizontal blocks**
21	**TILE_EN**	TILE_EN	**Enables tile mode** 0: Disable 1: Enable
20	**TILE_W**	TILE_WIDTH_SEL	**Width of tile** 0: 16 1: 32
19:0	**TILE_H**	TILE_HEIGHT	**Height of source tile mode**

1400C08C OVL_L2_CLI **Overlay Layer 2 Clip** **00000000**

P

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L2_SRC_BOTTOM_CLIP								L2_SRC_TOP_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L2_SRC_RIGHT_CLIP								L2_SRC_LEFT_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**L2_SRC_BOTTOM_CLIP**	L2_SRC_BOTTOM_CLIP	Layer 2 bottom clip
23:16	**L2_SRC_TOP_CLI P**	L2_SRC_TOP_CLI P	Layer 2 top clip
15:8	**L2_SRC_RIGHT_C LIP**	L2_SRC_RIGHT_C LIP	Layer 2 right clip
7:0	**L2_SRC_LEFT_CL IP**	L2_SRC_LEFT_CL IP	Layer 2 left clip

1400C090 OVL_L3_CON **Overlay Layer 3 Control** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSTKEY_EN	SRCKEY_EN	LAYER_SRC		MTX_EN	MTX_AUTO_DIS	RGB_SWAP	BYTE_SWAP	CLRFMT_MAN	R_FIRST	LANDSCAPE	EN_3D	INT_MTX_SEL			
Type	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLRFMT				EXT_MTX_EN	HORIZONTAL_FLIP_EN	VERTICAL_FLIP_EN	ALPHA_EN	ALPHA							
Type	RW				OTHER	RW	RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**DKEN**	DSTKEY_EN	**Enables destination color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable destination color key 1: Enable destination color key
30	**SKEN**	SRCKEY_EN	**Enables source color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable source color key 1: Enable source color key
29:28	**LSRC**	LAYER_SRC	**Selects layer pixel from memory/constant color/SCL/PQ** 00: Layer pixel from memory RDMA3 01: Layer pixel from constant color 10: Layer pixel from UFOd 11: Layer pixel from PQ
27		MTX_EN	
26		MTX_AUTO_DIS	
25	**RGSW**	RGB_SWAP	**No use**

Bit(s)	Mnemonic	Name	Description
24	**BTSW**	BYTE_SWAP	**Swaps unified color format** 1: BGR565, RGB888, RGBA8888, ARGB8888, VYUY, YVYU 0: RGB565, BGR888, BGRA8888, ABGR8888, UYVY, YUYV
23		CLRFMT_MAN	
22		R_FIRST	**Right eye image first when in 3D mode** 0: Show left eye image first in 3D mode 1: Show right eye image first in 3D mode
21		LANDSCAPE	**Enables 3D landscape mode** 0: 3D portrait mode 1: 3D landscape mode
20		EN_3D	**Enables 3D mode** 0: 2D mode 1: 3D mode
19:16	**MTX**	INT_MTX_SEL	**Selects color matrix table** 0000: MTX_RGB_TO_JPEG 0010: MTX_RGB_TO_BT601 0011: MTX_RGB_TO_BT709 0100: MTX_JPEG_TO_RGB 0110: MTX_BT601_TO_RGB 0111: MTX_BT709_TO_RGB 1000: MTX_JPEG_TO_BT601 1001: MTX_JPEG_TO_BT709 1010: MTX_BT601_TO_JPEG 1011: MTX_BT709_TO_JPEG 1100: MTX_BT709_TO_BT601 1101: MTX_BT601_TO_BT709 Others: HW default (JPEG_TO_RGB)
15:12	**CFMT**	CLRFMT	**//--OLD define for reference only** 0000: RGB888 0001: RGB565 0010: ARGB8888 0011: PARGB8888 0100: xARGB8888 1000: YUYV 1001: UYVY 1010: YVYU 1011: VYUY 1111: YUV444 Others: Reserved color format 0000: RGB565 0001: RGB888 0010: RGBA8888/BGRA8888 0011: ARGB8888/ABGR8888 0100: UVVY, VYUY 0101: YUYV, YVYU
11	**MTXEN**	EXT_MTX_EN	**Enables external programmable coeff** 0: Matrix coeff 1: Programmable coeff
10	**HFE**	HORIZONTAL_FLIP_EN	**Enables horizontal flip** 0: Disable horizontal flip 1: Enable horizontal flip
9	**VFE**	VERTICAL_FLIP_ EN	**Enables vertical flip** 0: Disable vertical flip 1: Enable vertical flip
8	**AEN**	ALPHA_EN	**Enables alpha blending**

Bit(s)	Mnemonic	Name	Description
			0: Disable alpha blending 1: Enable alpha blending
7:0	**APHA**	ALPHA	**Constant alpha value**

1400C094 OVL_L3_SRCKEY Overlay Layer 3 Source Key 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SKEY**	SRCKEY	**Layer source color key** Active when source color key is enabled.

1400C098 OVL_L3_SRC_SIZE Overlay Layer 3 Source Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L3_SRC_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L3_SRC_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**L3H**	L3_SRC_H	**Layer source height** Range: 0 ~ 8191
12:0	**L3W**	L3_SRC_W	**Layer source width** Range: 0 ~ 8191

1400C09C OVL_L3_OFFSET Overlay Layer 3 Offset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L3_YOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L3_XOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**L3H**	L3_YOFF	**Layer vertical Y offset** Range: 0 ~ 8191
12:0	**L3XO**	L3_XOFF	**Layer horizontal X offset** Range: 0 ~ 8191

1400CFA0 OVL_L3_ADDR **Overlay Layer 3 Memory Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**L3_ADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**L3_ADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**L3AD**	L3_ADDR	Layer memory buffer address

1400C0A4 OVL_L3_PITCH **Overlay Layer 3 Pitch** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SURFL_EN**	**L3_BLEND_RND_SHT**		**L3_CONST_BLD**	**L3_DRGB_SEL_EXT**	**L3_DA_SEL_EXT**	**L3_SRGB_SEL_EXT**	**L3_SA_SEL_EXT**	**L3_DRGB_SEL**		**L3_DA_SEL**		**L3_SRGB_SEL**		**L3_SA_SEL**	
Type	RW	RW		RW	RW	RW	RW	RW	RW		RW		RW		RW	
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**L3_SRC_PITCH**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**L3SP**	SURFL_EN	**Enables layer surface dlinger alpha_blending** 0: Disable surface flinger alpha_blending 1: Enable surface flinger alpha_blending
30		L3_BLEND_RND_SHT	
28		L3_CONST_BLD	
27		L3_DRGB_SEL_EXT	**Selects layer destination_RGB alpha**
26		L3_DA_SEL_EXT	**Selects layer destination_Alpha alpha**
25		L3_SRGB_SEL_EXT	**Selects layer source_RGB alpha**
24		L3_SA_SEL_EXT	**Selects layer source_Alpha alpha**
23:22	**L3SP**	L3_DRGB_SEL	**Selects layer destination_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved

Bit(s)	Mnemonic	Name	Description
21:20	**L3SP**	L3_DA_SEL	**Selects layer destination_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
19:18	**L3SP**	L3_SRGB_SEL	**Selects layer source_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
17:16	**L3SP**	L3_SA_SEL	**Selects layer source_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
15:0	**L3SP**	L3_SRC_PITCH	**Layer source pitch**

1400C0A8 OVL_L3_TILE Overlay Layer 3 Tile Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TILE_HORI_BLOCK_NUM										TILE_EN	TILE_WIDTH_SEL	TILE_HEIGHT			
Type	OTHER										OTHER	OTHER	OTHER			
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TILE_HEIGHT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**TILE_BLKS**	TILE_HORI_BLOCK_NUM	**Number of horizontal blocks**
21	**TILE_EN**	TILE_EN	**Enables tile mode** 0: Disable 1: Enable
20	**TILE_W**	TILE_WIDTH_SEL	**Width of tile** 0: 16 1: 32
19:0	**TILE_H**	TILE_HEIGHT	**Height of source tile mode**

1400C0AC OVL_L3_CLIP Overlay Layer 3 Clip 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L3_SRC_BOTTOM_CLIP								L3_SRC_TOP_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L3_SRC_RIGHT_CLIP								L3_SRC_LEFT_CLIP							
Type	RW								RW							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**L3_SRC_BOTTOM_CLIP**	L3_SRC_BOTTOM_CLIP	Layer 3 bottom clip
23:16	**L3_SRC_TOP_CLI P**	L3_SRC_TOP_CLI P	Layer 3 top clip
15:8	**L3_SRC_RIGHT_C LIP**	L3_SRC_RIGHT_C LIP	Layer 3 right clip
7:0	**L3_SRC_LEFT_CL IP**	L3_SRC_LEFT_CL IP	Layer 3 left clip

1400C0C0 OVL_RDMA0_CTRL **Overlay RDMA0 Control** **03FF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						RDMA 0_FI FO_U SED_ SIZE										
Type						RU										
Reset						0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RDMA 0_IN TERL ACE				RDMA 0_EN
Type												OTHER				RW
Reset												0				0

Bit(s)	Mnemonic	Name	Description
26:16		RDMA0_FIFO_USE D_SIZE	**Overlay RDMA0 used size**
4		RDMA0_INTERLAC E	**Overlay RDMA0 interlace** 0: Disable 1: Enable
0		RDMA0_EN	**Overlay RDMA0 Enable** 0: Disable 1: Enable

1400C0C8 OVL_RDMA0_MEM_GMC_SETTING1 **Overlay RDMA0 Memory GMC Setting** **1010FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA0_PRE_ULTRA_THRESHOLD_HIGH_OF S								RDMA0_ULTRA_THRESHOLD_HIGH_OFS							
Type	OTHER								OTHER							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA0_PRE_ULTRA_THRESHOLD								RDMA0_ULTRA_THRESHOLD							
Type	OTHER								OTHER							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		RDMA0_PRE_ULTR A_THRESHOLD_HI GH_OFS	Overlay RDMA0 pre_ultra threshold high offset
23:16		RDMA0_ULTRA_TH	Overlay RDMA0 ultra threshold high offset

Bit(s)	Mnemonic	Name	Description
		RESHOLD_HIGH_OFS	
15:8		RDMA0_PRE_ULTRA_THRESHOLD	Overlay RDMA0 pre_ultra threshold
7:0		RDMA0_ULTRA_THRESHOLD	Overlay RDMA0 ultra threshold

1400C0CC OVL_RDMA0_MEM_SLOW_CON **Overlay RDMA0 Memory Slow Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA0_SLOW_CNT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RDMA0_SLOW_EN
Type																OTHER
Reset																0

Bit(s)	Mnemonic	Name	Description
31:16		RDMA0_SLOW_CNT	**Overlay RDMA0 memory slow-down counter** After this SLOW_CNT, SMI will raise greq again. 10: 10 cycles between 2 greq at least 33: 33 cycles between 2 greq at least
0		RDMA0_SLOW_EN	**Enables overlay RDMA0 memory slow-down** 0: Disable slow-down 1: Enable slow-down

1400C0D0 OVL_RDMA0_FIFO_CTRL **Overlay RDMA0 FIFO Control** **01200000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA0_FIFO_UND_EN						RDMA0_FIFO_SIZE									
Type	OTHER						RW									
Reset	0						0	1	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RDMA0_FIFO_THRD									
Type							OTHER									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		RDMA0_FIFO_UND_EN	**Overlay RDMA0 FIFO underflow control** 0: Disable FIFO underflow 1: Enable FIFO underflow
25:16		RDMA0_FIFO_SIZ E	**Overlay RDMA0 FIFO size**

Bit(s)	Mnemonic	Name	Description
			Unit: 16 bytes 128: FIFO size is 128*128.
9:0		RDMA0_FIFO_THR D	**Overlay RDMA0 FIFO output valid threshold** Unit: 16 bytes. This value should be smaller than SRC_W*SRC_H*bpp >> 2. 0, 1: If FIFO pointer >= 1, RDMA will send data valid to OVL. 2: If FIFO pointer >= 2, RDMA will send data valid to OVL.

1400C0E0 OVL_RDMA1_CTRL **Overlay RDMA1 Control** **03FF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						RDMA 1_FI FO_U SED_ SIZE										
Type						RU										
Reset						0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RDMA 1_IN TERL ACE				RDMA 1_EN
Type												OTHER				RW
Reset												0				0

Bit(s)	Mnemonic	Name	Description
26:16		RDMA1_FIFO_USE D_SIZE	**Overlay RDMA1 used size**
4		RDMA1_INTERLAC E	**Overlay RDMA1 interlace** 0: Disable 1: Enable
0		RDMA1_EN	**Enables overlay RDMA1** 0: Disable 1: Enable

1400C0E8 OVL_RDMA1_MEM_GMC_SETTING1 **Overlay RDMA1 Memory GMC Setting** **1010FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA1_PRE_ULTRA_THRESHOLD_HIGH_OF S								RDMA1_ULTRA_THRESHOLD_HIGH_OFS							
Type	OTHER								OTHER							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA1_PRE_ULTRA_THRESHOLD								RDMA1_ULTRA_THRESHOLD							
Type	OTHER								OTHER							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		RDMA1_PRE_ULTR A_THRESHOLD_HI GH_OFS	Overlay RDMA1 pre_ultra threshold high offset
23:16		RDMA1_ULTRA_TH	Overlay RDMA1 ultra threshold high offset

Bit(s)	Mnemonic	Name	Description
		RESHOLD_HIGH_OFS	
15:8		RDMA1_PRE_ULTRA_THRESHOLD	Overlay RDMA1 pre_ultra threshold
7:0		RDMA1_ULTRA_THRESHOLD	Overlay RDMA1 ultra threshold

1400C0EC OVL_RDMA1_MEM_SLOW_CON **Overlay RDMA1 Memory Slow Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA1_SLOW_CNT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RDMA1_SLOW_EN
Type																OTHER
Reset																0

Bit(s)	Mnemonic	Name	Description
31:16		RDMA1_SLOW_CNT	**Overlay RDMA1 memory slow-down counter** After this SLOW_CNT, SMI will raise greq again. 10: 10 cycles between 2 greq at least 33: 33 cycles between 2 greq at least
0		RDMA1_SLOW_EN	**Enables overlay RDMA1 memory slow-down** 0: Disable slow-down 1: Enable slow-down

1400C0F0 OVL_RDMA1_FIFO_CTRL **Overlay RDMA1 FIFO Control** **01200000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA1_FIFO_UND_EN						RDMA1_FIFO_SIZE									
Type	OTHER						RW									
Reset	0						0	1	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RDMA1_FIFO_THRD									
Type							OTHER									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		RDMA1_FIFO_UND_EN	**Overlay RDMA1 FIFO underflow control** 0: Disable FIFO underflow 1: Enable FIFO underflow
25:16		RDMA1_FIFO_SIZ E	**Overlay RDMA1 FIFO size** Unit: 16 bytes

Bit(s)	Mnemonic	Name	Description
			128: FIFO size is 128*128.
9:0		RDMA1_FIFO_THR D	**Overlay RDMA1 FIFO output valid threshold** Unit: 16 bytes. This value should be smaller than SRC_W*SRC_H*bpp >> 2. 0, 1: If FIFO pointer >= 1, RDMA will send data valid to OVL. 2: If FIFO pointer >= 2, RDMA will send data valid to OVL.

1400C100 OVL_RDMA2_CTRL **Overlay RDMA2 Control** **03FF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						RDMA2_FIFO_USED_SIZE										
Type						RU										
Reset						0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RDMA2_INTERLACE				RDMA2_EN
Type												OTHER				RW
Reset												0				0

Bit(s)	Mnemonic	Name	Description
26:16		RDMA2_FIFO_USED_SIZE	**Overlay RDMA2 used size**
4		RDMA2_INTERLAC E	**Overlay RDMA2 interlace** 0: Disable 1: Enable
0		RDMA2_EN	**Enables overlay RDMA2** 0: Disable 1: Enable

1400C108 OVL_RDMA2_MEM_GMC_SETTING1 **Overlay RDMA2 Memory GMC Setting** **1010FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA2_PRE_ULTRA_THRESHOLD_HIGH_OFS								RDMA2_ULTRA_THRESHOLD_HIGH_OFS							
Type	OTHER								OTHER							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA2_PRE_ULTRA_THRESHOLD								RDMA2_ULTRA_THRESHOLD							
Type	OTHER								OTHER							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		RDMA2_PRE_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA2 pre_ultra threshold high offset
23:16		RDMA2_ULTRA_THRESHOLD_HIGH_O	Overlay RDMA2 ultra threshold high offset

Bit(s)	Mnemonic	Name	Description
15:8		FS RDMA2_PRE_ULTRA_THRESHOLD	Overlay RDMA2 pre_ultra threshold
7:0		RDMA2_ULTRA_THRESHOLD	Overlay RDMA2 ultra threshold

1400C10C OVL_RDMA2_MEM_SLOW_CON **Overlay RDMA2 Memory Slow Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA2_SLOW_CNT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RDMA2_SLOW_EN
Type																OTHER
Reset																0

Bit(s)	Mnemonic	Name	Description
31:16		RDMA2_SLOW_CNT	**Overlay RDMA2 memory slow-down counter** After this SLOW_CNT, SMI will raise greq again. 10: 10 cycles between 2 greq at least 33: 33 cycles between 2 greq at least
0		RDMA2_SLOW_EN	**Enables overlay RDMA2 memory slow-down** 0: Disable slow-down 1: Enable slow-down

1400C110 OVL_RDMA2_FIFO_CTRL **Overlay RDMA2 FIFO Control** **01200000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA2_FIFO_UND_EN						RDMA2_FIFO_SIZE									
Type	OTHER						RW									
Reset	0						0	1	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RDMA2_FIFO_THRD									
Type							OTHER									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		RDMA2_FIFO_UND_EN	**Overlay RDMA2 FIFO underflow control** 0: Disable FIFO underflow 1: Enable FIFO underflow
25:16		RDMA2_FIFO_SIZE	**Overlay RDMA2 FIFO size** Unit: 16 bytes 128: FIFO size is 128*128.

Bit(s)	Mnemonic	Name	Description
9:0		RDMA2_FIFO_THR D	**Overlay RDMA2 FIFO output valid threshold** Unit: 16 bytes. This value should be smaller than SRC_W*SRC_H*bpp >> 2. 0, 1: If FIFO pointer >= 1, RDMA will send data valid to OVL. 2: If FIFO pointer >= 2, RDMA will send data valid to OVL.

1400C120 OVL_RDMA3_CTRL **Overlay RDMA3 Control** **03FF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						RDMA3_FIFO_USED_SIZE										
Type						RU										
Reset						0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RDMA3_INTERLACE				RDMA3_EN
Type												OTHER				RW
Reset												0				0

Bit(s)	Mnemonic	Name	Description
26:16		RDMA3_FIFO_USE D_SIZE	**Overlay RDMA3 used size**
4		RDMA3_INTERLAC E	**Overlay RDMA3 interlace** 0: Disable 1: Enable
0		RDMA3_EN	**Enables overlay RDMA3** 0: Disable 1: Enable

1400C128 OVL_RDMA3_MEM_GMC_SETTING1 **Overlay RDMA3 Memory GMC Setting** **1010FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA3_PRE_ULTRA_THRESHOLD_HIGH_OFS								RDMA3_ULTRA_THRESHOLD_HIGH_OFS							
Type	OTHER								OTHER							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA3_PRE_ULTRA_THRESHOLD								RDMA3_ULTRA_THRESHOLD							
Type	OTHER								OTHER							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		RDMA3_PRE_ULTR A_THRESHOLD_HI GH_OFS	Overlay RDMA3 pre_ultra threshold high offset
23:16		RDMA3_ULTRA_TH RESHOLD_HIGH_O FS	Overlay RDMA3 ultra threshold high offset

Bit(s)	Mnemonic	Name	Description
15:8		RDMA3_PRE_ULTRA_THRESHOLD	Overlay RDMA3 pre_ultra threshold
7:0		RDMA3_ULTRA_THRESHOLD	Overlay RDMA3 ultra threshold

1400C12C OVL_RDMA3_MEM_SLOW_CON **Overlay RDMA3 Memory Slow Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA3_SLOW_CNT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RDMA3_SLOW_EN
Type																OTHER
Reset																0

Bit(s)	Mnemonic	Name	Description
31:16		RDMA3_SLOW_CNT	**Overlay RDMA3 memory slow-down counter** After this SLOW_CNT, SMI will raise greq again. 10: 10 cycles between 2 greq at least 33: 33 cycles between 2 greq at least
0		RDMA3_SLOW_EN	**Enables overlay RDMA3 memory slow-down** 0: Disable slow-down 1: Enable slow-down

1400C130 OVL_RDMA3_FIFO_CTRL **Overlay RDMA3 FIFO Control** **01200000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA3_FIFO_UND_EN						RDMA3_FIFO_SIZE									
Type	OTHER						RW									
Reset	0						0	1	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RDMA3_FIFO_THRD									
Type							OTHER									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		RDMA3_FIFO_UND_EN	**Overlay RDMA3 FIFO underflow control** 0: Disable FIFO underflow 1: Enable FIFO underflow
25:16		RDMA3_FIFO_SIZE	**Overlay RDMA3 FIFO size** Unit: 16 bytes 128: FIFO size is 128*128.
9:0		RDMA3_FIFO_THRD	**Overlay RDMA3 FIFO output valid threshold**

Bit(s)	Mnemonic	Name	Description
			Unit: 16 bytes. This value should be smaller than SRC_W*SRC_H*bpp >> 2. 0, 1: If FIFO pointer >= 1, RDMA will send data valid to OVL. 2: If FIFO pointer >= 2, RDMA will send data valid to OVL.

1400C134 OVL_L0_Y2R_PARA_R0 **Overlay L0 Y2R Conversion Parameter R0** **00000400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_RMU												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_RMU	Overlay L0 YUV2RGB program parameter for R color of U component
12:0		C_CF_RMY	Overlay L0 YUV2RGB program parameter for R color of Y component

1400C138 OVL_L0_Y2R_PARA_R1 **Overlay L0 Y2R Conversion Parameter R1** **0000057C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMV												
Type				OTHER												
Reset				0	0	1	0	1	0	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_RMV	Overlay L0 YUV2RGB program parameter for R color of V component

1400C13C OVL_L0_Y2R_PARA_G0 **Overlay L0 Y2R Conversion Parameter G0** **1EA80400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_GMU												
Type				OTHER												
Reset				1	1	1	1	0	1	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMY												

Type				OTHER													
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_GMU	Overlay Lo YUV2RGB program parameter for G color of U component
12:0		C_CF_GMY	Overlay Lo YUV2RGB program parameter for G color of Y component

1400C140 OVL_Lo_Y2R_PARA_G1 **Overlay Lo Y2R Conversion Parameter G1** **00001D35**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMV												
Type				OTHER												
Reset				1	1	1	0	1	0	0	1	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_GMV	Overlay Lo YUV2RGB program parameter for G color of V component

1400C144 OVL_Lo_Y2R_PARA_Bo **Overlay Lo Y2R Conversion Parameter Bo** **06EE0400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_BMU												
Type				OTHER												
Reset				0	0	1	1	0	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_BMU	Overlay Lo YUV2RGB program parameter for B color of U component
12:0		C_CF_BMY	Overlay Lo YUV2RGB program parameter for B color of Y component

1400C148 OVL_Lo_Y2R_PARA_B1 **Overlay Lo Y2R Conversion Parameter B1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMV												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_BMV	Overlay Lo YUV2RGB program parameter for B color of V component

1400C14C OVL_Lo_Y2R_PARA_YUV_A_0 — **Overlay Lo Y2R Conversion Parameter Extended Add on YUV 0** — **01800000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_UA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_YA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_UA	Overlay Lo YUV2RGB program parameter for U to add extended offset
8:0		C_CF_YA	Overlay Lo YUV2RGB program parameter for Y to add extended offset

1400C150 OVL_Lo_Y2R_PARA_YUV_A_1 — **Overlay Lo Y2R Conversion Parameter Extended Add on YUV 1** — **00000180**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_VA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_VA	Overlay Lo YUV2RGB program parameter for V to add extended offset

1400C154 OVL_Lo_Y2R_PARA_RGB_A_0 — **Overlay Lo Y2R Conversion Parameter Extended Add on RGB 0** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_GA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_RA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_GA	Overlay L0 YUV2RGB program parameter for G to add extended offset
8:0		C_CF_RA	Overlay L0 YUV2RGB program parameter for R to add extended offset

1400C158 OVL_L0_Y2R_PARA_RGBA_1 **Overlay L0 Y2R Conversion Parameter Extended Add on RGB 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_BA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_BA	Overlay L0 YUV2RGB program parameter for B to add extended offset

1400C15C OVL_L1_Y2R_PARA_R0 **Overlay L1 Y2R Conversion Parameter R0** **00000400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_RMU												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_RMU	Overlay L1 YUV2RGB program parameter for R color of U component
12:0		C_CF_RMY	Overlay L1 YUV2RGB program parameter for R color of Y component

1400C160 OVL_L1_Y2R_PARA_R1 **Overlay L1 Y2R Conversion Parameter R1** **0000057C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMV												
Type				OTHER												
Reset				0	0	1	0	1	0	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_RMV	Overlay L1 YUV2RGB program parameter for R color of V component

1400C164 OVL_L1_Y2R_PARA_G0 **Overlay L1 Y2R Conversion Parameter G0** **1EA80400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_GMU												
Type				OTHER												
Reset				1	1	1	1	0	1	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_GMU	Overlay L1 YUV2RGB program parameter for G color of U component
12:0		C_CF_GMY	Overlay L1 YUV2RGB program parameter for G color of Y component

1400C168 OVL_L1_Y2R_PARA_G1 **Overlay L1 Y2R Conversion Parameter G1** **00001D35**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMV												
Type				OTHER												
Reset				1	1	1	0	1	0	0	1	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_GMV	Overlay L1 YUV2RGB program parameter for G color of V component

Bit(s)	Mnemonic	Name	Description

1400C16C OVL_L1_Y2R_PARA_B0 — **Overlay L1 Y2R Conversion Parameter B0** — **06EE0400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_BMU												
Type				OTHER												
Reset				0	0	1	1	0	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_BMU	Overlay L1 YUV2RGB program parameter for B color of U component
12:0		C_CF_BMY	Overlay L1 YUV2RGB program parameter for B color of Y component

1400C170 OVL_L1_Y2R_PARA_B1 — **Overlay L1 Y2R Conversion Parameter B1** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMV												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_BMV	Overlay L1 YUV2RGB program parameter for B color of V component

1400C174 OVL_L1_Y2R_PARA_YUVA_0 — **Overlay L1 Y2R Conversion Parameter Extended Add on YUV 0** — **01800000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_UA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_YA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_UA	Overlay L1 YUV2RGB program parameter for U to add extended offset
8:0		C_CF_YA	Overlay L1 YUV2RGB program parameter for Y to add extended offset

1400C178 OVL_L1_Y2R_PARA_YUV_A_1 Overlay L1 Y2R Conversion Parameter Extended Add on YUV 1 00000180

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_VA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_VA	Overlay L1 YUV2RGB program parameter for V to add extended offset

1400C17C OVL_L1_Y2R_PARA_RGB_A_0 Overlay L1 Y2R Conversion Parameter Extended Add on RGB 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_GA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_RA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_GA	Overlay L1 YUV2RGB program parameter for G to add extended offset
8:0		C_CF_RA	Overlay L1 YUV2RGB program parameter for R to add extended offset

1400C180 OVL_L1_Y2R_PARA_RGB_A_1 Overlay L1 Y2R Conversion Parameter Extended Add on RGB 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_BA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_BA	Overlay L1 YUV2RGB program parameter for B to add extended offset

1400C184 OVL_L2_Y2R_PARA_R0 Overlay L2 Y2R Conversion Parameter R0 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_RMU												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_RMU	Overlay L2 YUV2RGB program parameter for R color of U component
12:0		C_CF_RMY	Overlay L2 YUV2RGB program parameter for R color of Y component

1400C188 OVL_L2_Y2R_PARA_R1 Overlay L2 Y2R Conversion Parameter R1 0000057C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMV												
Type				OTHER												
Reset				0	0	1	0	1	0	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_RMV	Overlay L2 YUV2RGB program parameter for R color of V component

1400C18C OVL_L2_Y2R_PARA_G0 Overlay L2 Y2R Conversion Parameter G0 1EA80400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_GMU												
Type				OTHER												

Reset				1	1	1	1	0	1	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_GMU	Overlay L2 YUV2RGB program parameter for G color of U component
12:0		C_CF_GMY	Overlay L2 YUV2RGB program parameter for G color of Y component

1400C190 OVL_L2_Y2R_PARA_G1 **Overlay L2 Y2R Conversion Parameter G1** **00001D35**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMV												
Type				OTHER												
Reset				1	1	1	0	1	0	0	1	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_GMV	Overlay L2 YUV2RGB program parameter for G color of V component

1400C194 OVL_L2_Y2R_PARA_B0 **Overlay L2 Y2R Conversion Parameter B0** **06EE0400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_BMU												
Type				OTHER												
Reset				0	0	1	1	0	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_BMU	Overlay L2 YUV2RGB program parameter for B color of U component
12:0		C_CF_BMY	Overlay L2 YUV2RGB program parameter for B color of Y component

1400C198 OVL_L2_Y2R_PARA_B1 **Overlay L2 Y2R Conversion Parameter B1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMV												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_BMV	Overlay L2 YUV2RGB program parameter for B color of V component

1400C19C OVL_L2_Y2R_PARA_YUVA_0 **Overlay L2 Y2R Conversion Parameter Extended Add on YUV 0** **01800000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_UA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_YA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_UA	Overlay L2 YUV2RGB program parameter for U to add extended offset
8:0		C_CF_YA	Overlay L2 YUV2RGB program parameter for Y to add extended offset

1400C1A0 OVL_L2_Y2R_PARA_YUVA_1 **Overlay L2 Y2R Conversion Parameter Extended Add on YUV 1** **00000180**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_VA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_VA	Overlay L2 YUV2RGB program parameter for V to add extended offset

1400C1A4 OVL_L2_Y2R_PARA_RGB_A_0 — Overlay L2 Y2R Conversion Parameter Extended Add on RGB 0 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_GA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_RA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_GA	Overlay L2 YUV2RGB program parameter for G to add extended offset
8:0		C_CF_RA	Overlay L2 YUV2RGB program parameter for R to add extended offset

1400C1A8 OVL_L2_Y2R_PARA_RGB_A_1 — Overlay L2 Y2R Conversion Parameter Extended Add on RGB 1 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_BA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_BA	Overlay L2 YUV2RGB program parameter for B to add extended offset

1400C1AC OVL_L3_Y2R_PARA_R0 — Overlay L3 Y2R Conversion Parameter R0 — 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_RMU												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_RMU	Overlay L3 YUV2RGB program parameter for R color of U component

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_RMY	Overlay L3 YUV2RGB program parameter for R color of Y component

1400C1B0 OVL_L3_Y2R_PARA_R1 **Overlay L3 Y2R Conversion Parameter R1** **0000057C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMV												
Type				OTHER												
Reset				0	0	1	0	1	0	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_RMV	Overlay L3 YUV2RGB program parameter for R color of V component

1400C1B4 OVL_L3_Y2R_PARA_G0 **Overlay L3 Y2R Conversion Parameter G0** **1EA80400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_GMU												
Type				OTHER												
Reset				1	1	1	1	0	1	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_GMU	Overlay L3 YUV2RGB program parameter for G color of U component
12:0		C_CF_GMY	Overlay L3 YUV2RGB program parameter for G color of Y component

1400C1B8 OVL_L3_Y2R_PARA_G1 **Overlay L3 Y2R Conversion Parameter G1** **00001D35**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMV												
Type				OTHER												
Reset				1	1	1	0	1	0	0	1	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_GMV	**Overlay L3 YUV2RGB program parameter for G color of V component**

1400C1BC OVL_L3_Y2R_PARA_B0 **Overlay L3 Y2R Conversion Parameter B0** **06EE0400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_BMU												
Type				OTHER												
Reset				0	0	1	1	0	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_BMU	Overlay L3 YUV2RGB program parameter for B color of U component
12:0		C_CF_BMY	Overlay L3 YUV2RGB program parameter for B color of Y component

1400C1C0 OVL_L3_Y2R_PARA_B1 **Overlay L3 Y2R Conversion Parameter B1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMV												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_BMV	Overlay L3 YUV2RGB program parameter for B color of V component

1400C1C4 OVL_L3_Y2R_PARA_YUVA_0 **Overlay L3 Y2R Conversion Parameter Extended Add on YUV 0** **01800000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_UA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_YA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_UA	Overlay L3 YUV2RGB program parameter for U to add extended offset
8:0		C_CF_YA	Overlay L3 YUV2RGB program parameter for Y to add extended offset

1400C1C8 OVL_L3_Y2R_PARA_YUVA_1 **Overlay L3 Y2R Conversion Parameter Extended Add on YUV 1** **00000180**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_VA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_VA	Overlay L3 YUV2RGB program parameter for V to add extended offset

1400C1CC OVL_L3_Y2R_PARA_RGBA_0 **Overlay L3 Y2R Conversion Parameter Extended Add on RGB 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_GA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_RA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_GA	Overlay L3 YUV2RGB program parameter for G to add extended offset
8:0		C_CF_RA	Overlay L3 YUV2RGB program parameter for R to add extended offset

1400C1D0 OVL_L3_Y2R_PARA_RGBA_1 **Overlay L3 Y2R Conversion Parameter Extended Add on RGB 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_BA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_BA	Overlay L3 YUV2RGB program parameter for B to add extended offset

1400C1D4 OVL_DEBUG_MON_SEL Overlay Debug Monitor Select 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DBG_MON_SEL			
Type													WO			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0		DBG_MON_SEL	Overlay Debug Monitor Select

1400C1E0 OVL_RDMA0_MEM_GMC_SETTING2 Overlay RDMA0 Memory GMC Setting 205F00BF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RDMA0_FORCE_REQ_THRESHOLD	RDMA0_REQ_THRESHOLD_ULTRA	RDMA0_REQ_THRESHOLD_PREULTRA		RDMA0_ISSUE_REQ_THRESHOLD_URG										
Type		RW	RW	RW		RW										
Reset		0	1	0		0	0	0	0	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RDMA0_ISSUE_REQ_THRESHOLD										
Type						RW										
Reset						0	0	0	1	0	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30		RDMA0_FORCE_REQ_THRESHOLD	
29		RDMA0_REQ_THRESHOLD_ULTRA	
28		RDMA0_REQ_THRESHOLD_PREULTRA	
26:16		RDMA0_ISSUE_RE	

Bit(s)	Mnemonic	Name	Description
10:0		Q_THRESHOLD_URG RDMA0_ISSUE_REQ_THRESHOLD	Overlay RDMA0 issue request threshold (0 for best performance)

1400C1E4 OVL_RDMA1_MEM_GMC_SETTING2 **Overlay RDMA1 Memory GMC Setting** **205F00BF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RDMA1_FORCE_REQ_THRESHOLD	RDMA1_REQ_THRESHOLD_ULTRA	RDMA1_REQ_THRESHOLD_PREULTRA		RDMA1_ISSUE_REQ_THRESHOLD_URG										
Type		RW	RW	RW		RW										
Reset		0	1	0		0	0	0	0	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RDMA1_ISSUE_REQ_THRESHOLD										
Type						RW										
Reset						0	0	0	1	0	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30		RDMA1_FORCE_REQ_THRESHOLD	
29		RDMA1_REQ_THRESHOLD_ULTRA	
28		RDMA1_REQ_THRESHOLD_PREULTRA	
26:16		RDMA1_ISSUE_REQ_THRESHOLD_URG	
10:0		RDMA1_ISSUE_REQ_THRESHOLD	Overlay RDMA1 issue request threshold(0 for best performance)

1400C1E8 OVL_RDMA2_MEM_GMC_SETTING2 **Overlay RDMA2 Memory GMC Setting** **205F00BF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RDMA2_FORCE_REQ_THRESHOLD	RDMA2_REQ_THRESHOLD_ULTRA	RDMA2_REQ_THRESHOLD_PREULTRA		RDMA2_ISSUE_REQ_THRESHOLD_URG										
Type		RW	RW	RW		RW										
Reset		0	1	0		0	0	0	0	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RDMA2_ISSUE_REQ_THRESHOLD										
Type						RW										
Reset						0	0	0	1	0	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30		RDMA2_FORCE_REQ_THRESHOLD	
29		RDMA2_REQ_THRESHOLD_ULTRA	
28		RDMA2_REQ_THRESHOLD_PREULTRA	
26:16		RDMA2_ISSUE_REQ_THRESHOLD_URG	
10:0		RDMA2_ISSUE_REQ_THRESHOLD	Overlay RDMA2 issue request threshold(0 for best performance)

1400C1EC OVL_RDMA3_MEM_GMC_SETTING2 **Overlay RDMA3 Memory GMC Setting** **205F00BF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RDMA3_FORCE_REQ_THRESHOLD	RDMA3_REQ_THRESHOLD_ULTRA	RDMA3_REQ_THRESHOLD_PREULTRA		RDMA3_ISSUE_REQ_THRESHOLD_URG										
Type		RW	RW	RW		RW										
Reset		0	1	0		0	0	0	0	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RDMA3_ISSUE_REQ_THRESHOLD										
Type						RW										
Reset						0	0	0	1	0	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30		RDMA3_FORCE_REQ_THRESHOLD	
29		RDMA3_REQ_THRESHOLD_ULTRA	
28		RDMA3_REQ_THRESHOLD_PREULTRA	
26:16		RDMA3_ISSUE_REQ_THRESHOLD_URG	
10:0		RDMA3_ISSUE_REQ_THRESHOLD	Overlay RDMA3 issue request threshold(0 for best performance)

1400C1F0 OVL_RDMA_BURST_CON0 **Overlay RDMA Burst Control** **07775533**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				BURST_128B_BOUND		BURST15A_32B				BURST14A_32B				BURST13A_32B		
Type				RW		RW				RW				RW		
Reset				0		1	1	1		1	1	1		1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		BURST12A_32B				BURST11A_32B				BURST10A_32B				BURST9A_32B		
Type		RW				RW				RW				RW		

Reset		1	0	1		1	0	1		0	1	1		0	1	1

Bit(s)	Mnemonic	Name	Description
28		BURST_128B_BOU ND	
26:24		BURST15A_32B	First burst slice for a 32B aligned burst of length 15
22:20		BURST14A_32B	First burst slice for a 32B aligned burst of length 14
18:16		BURST13A_32B	First burst slice for a 32B aligned burst of length 13
14:12		BURST12A_32B	First burst slice for a 32B aligned burst of length 12
10:8		BURST11A_32B	First burst slice for a 32B aligned burst of length 11
6:4		BURST10A_32B	First burst slice for a 32B aligned burst of length 10
2:0		BURST9A_32B	First burst slice for a 32B aligned burst of length 9

1400C1F4 OVL_RDMA_BURST_CON1 Overlay RDMA Burst Control 06666442

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						BURST15A_N32B				BURST14A_N32B				BURST13A_N32B		
Type						RW				RW				RW		
Reset						1	1	0		1	1	0		1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		BURST12A_N32B				BURST11A_N32B				BURST10A_N32B				BURST9A_N32B		
Type		RW				RW				RW				RW		
Reset		1	1	0		1	0	0		1	0	0		0	1	0

Bit(s)	Mnemonic	Name	Description
26:24		BURST15A_N32B	First burst slice for a non-32B aligned burst of length 15
22:20		BURST14A_N32B	First burst slice for a non-32B aligned burst of length 14
18:16		BURST13A_N32B	First burst slice for a non-32B aligned burst of length 13
14:12		BURST12A_N32B	First burst slice for a non-32B aligned burst of length 12
10:8		BURST11A_N32B	First burst slice for a non-32B aligned burst of length 11
6:4		BURST10A_N32B	First burst slice for a non-32B aligned burst of length 10
2:0		BURST9A_N32B	First burst slice for a non-32B aligned burst of length 9

1400C1F8 OVL_RDMA_GREQ_NUM Overlay RDMA GREQ Number 510FBBBB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IOBUF_FLUSH_ULTRA	IOBUF_FLUSH_PREULTRA		GRP_BRK_STOP	GREQ_STOP_EN	GREQ_DIS_CNT			OSTD_GREQ_NUM							
Type	RW	RW		RW	RW	RW			RW							
Reset	0	1		1	0	0	0	1	0	0	0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LAYER3_GREQ_NUM				LAYER2_GREQ_NUM				LAYER1_GREQ_NUM				LAYER0_GREQ_NUM			
Type	RW				RW				RW				RW			
Reset	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1

Bit(s)	Mnemonic	Name	Description
31		IOBUF_FLUSH_UL TRA	

Bit(s)	Mnemonic	Name	Description
30		IOBUF_FLUSH_PREULTRA	
28		GRP_BRK_STOP	**Stop GREQ when group breaks**
27		GREQ_STOP_EN	**Stop each GREQ after GLCOMD**
26:24		GREQ_DIS_CNT	
23:16		OSTD_GREQ_NUM	
15:12	**LAYER3_GREQ_NUM**	LAYER3_GREQ_NUM	**OVL Layer 3 multi-greq number** Max.: 7
11:8	**LAYER2_GREQ_NUM**	LAYER2_GREQ_NUM	**OVL Layer 2 multi-greq number** Max.: 7
7:4	**LAYER1_GREQ_NUM**	LAYER1_GREQ_NUM	**OVL Layer 1 multi-greq number** Max.: 7
3:0	**LAYER0_GREQ_NUM**	LAYER0_GREQ_NUM	**OVL Layer 0 multi-greq number** Max.: 7

1400C1FC OVL_RDMA_GREQ_URG_NUM **Overlay RDMA GREQ Number** **20305555**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GREQ_NUM_SHT		GREQ_NUM_SHT_VAL	ARG_URG_BIAS			ARG_GREQ_URG_TH									
Type	RW		RW	RW			RW									
Reset	0	0	1	0			0	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LAYER3_GREQ_URG_NUM				LAYER2_GREQ_URG_NUM				LAYER1_GREQ_URG_NUM				LAYER0_GREQ_URG_NUM			
Type	RW				RW				RW				RW			
Reset	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
31:30		GREQ_NUM_SHT	
29		GREQ_NUM_SHT_VAL	
28		ARG_URG_BIAS	
25:16		ARG_GREQ_URG_TH	
15:12		LAYER3_GREQ_URG_NUM	**OVL Layer 3 multi-greq number** Max.: 7
11:8		LAYER2_GREQ_URG_NUM	**OVL Layer 2 multi-greq number** Max.: 7
7:4		LAYER1_GREQ_URG_NUM	**OVL Layer 1 multi-greq number** Max.: 7
3:0		LAYER0_GREQ_URG_NUM	**OVL Layer 0 multi-greq number** Max.: 7 (GREQ_URG_NUM <= GREQ_NUM)

1400C200 OVL_DUMMY_REG **Overlay Dummy Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OVERLAY_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OVERLAY_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		OVERLAY_DUMMY	Overlay dummy register

1400C208 OVL_GDRDY_PRD Overlay SMI GDRDY Period 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									GDRDY_PRD							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDRDY_PRD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		GDRDY_PRD	

1400C20C OVL_RDMA_ULTRA_SRC Overlay RDMA Ultra SRC 0000A050

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ULTRA_RDMA_SRC		ULTRA_ROI_END_SRC		ULTRA_SMI_SRC		ULTRA_BUF_SRC		PREULTRA_RDMA_SRC		PREULTRA_ROI_END_SRC		PREULTRA_SMI_SRC		PREULTRA_BUF_SRC	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	1	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:14		ULTRA_RDMA_SRC	
13:12		ULTRA_ROI_END_SRC	
11:10		ULTRA_SMI_SRC	
9:8		ULTRA_BUF_SRC	
7:6		PREULTRA_RDMA_SRC	
5:4		PREULTRA_ROI_END_SRC	
3:2		PREULTRA_SMI_SRC	
1:0		PREULTRA_BUF_SRC	

1400C210 OVL_RDMA0_BUF_LOW **Overlay RDMA BUF Low** **00030020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											BUF_LOW_PREULTRA_TH					
Type											RW					
Reset											0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF_LOW_PREULTRA_TH						BUF_LOW_ULTRA_TH									
Type	RW						RW									
Reset	0	0	0	0			0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:12		BUF_LOW_PREULTRA_TH	
9:0		BUF_LOW_ULTRA_TH	

1400C214 OVL_RDMA1_BUF_LOW **Overlay RDMA BUF Low** **00030020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											BUF_LOW_PREULTRA_TH					
Type											RW					
Reset											0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF_LOW_PREULTRA_TH						BUF_LOW_ULTRA_TH									
Type	RW						RW									
Reset	0	0	0	0			0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:12		BUF_LOW_PREULTRA_TH	
9:0		BUF_LOW_ULTRA_TH	

1400C218 OVL_RDMA2_BUF_LOW **Overlay RDMA BUF Low** **00030020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											BUF_LOW_PREULTRA_TH					
Type											RW					
Reset											0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF_LOW_PREULTRA_TH						BUF_LOW_ULTRA_TH									
Type	RW						RW									
Reset	0	0	0	0			0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
21:12		BUF_LOW_PREULTRA_TH	
9:0		BUF_LOW_ULTRA_TH	

1400C21C OVL_RDMA3_BUF_LOW **Overlay RDMA BUF Low** **00030020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											BUF_LOW_PREULTRA_TH					
Type											RW					
Reset											0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF_LOW_PREULTRA_TH						BUF_LOW_ULTRA_TH									
Type	RW						RW									
Reset	0	0	0	0			0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:12		BUF_LOW_PREULTRA_TH	
9:0		BUF_LOW_ULTRA_TH	

1400C230 OVL_SMI_DBG **Overlay SMI Arbiter Debug Monitor** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SMI_FSM									
Type							RU									
Reset							0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
9:0		SMI_FSM	Overlay SMI arbiter FSM state

1400C234 OVL_GREQ_LAYER_CNT **Overlay Layer GREQ Counter** **01010101**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			LAYER3_GREQ_CNT								LAYER2_GREQ_CNT					
Type			RU								RU					
Reset			0	0	0	0	0	1			0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			LAYER1_GREQ_CNT								LAYER0_GREQ_CNT					
Type			RU								RU					
Reset			0	0	0	0	0	1			0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
29:24		LAYER3_GREQ_CNT	RDMA Layer 3 greq counter
21:16		LAYER2_GREQ_CNT	RDMA Layer 2 greq counter
13:8		LAYER1_GREQ_CNT	RDMA Layer 1 greq counter
5:0		LAYER0_GREQ_CNT	RDMA Layer 0 greq counter

1400C238 OVL_GDRDY_PRD_NUM **Overlay SMI GDRDY Period Number** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									GDRDY_PRD_NUM							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDRDY_PRD_NUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		GDRDY_PRD_NUM	

1400C240 OVL_FLOW_CTRL_DBG **Overlay Flow Control Debug Monitor** **000FBC01**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OVL_UPD_REG	REG_UPDATE	OVL_CLR	OVL_START	OVL_RUNNING	FRAME_DONE	FRAME_UNDERRUN	FRAME_SWRST_DONE	FRAME_HWRST_DONE		TRIG	RST	RDMA0_IDLE	RDMA1_IDLE	RDMA2_IDLE	RDMA3_IDLE
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU		RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0		0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OUT_IDLE		OVL_OUT_READY	OVL_OUT_VALID	BLEND_IDLE	ADDCON_IDLE	FSM_STATE									
Type	RU		RU	RU	RU	RU	RU									
Reset	1		1	1	1	1	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31		OVL_UPD_REG	**Overlay prepare to update register**
30		REG_UPDATE	**Updates overlay register**
29		OVL_CLR	**Clears overlay**
28		OVL_START	**Starts overlay**
27		OVL_RUNNING	**Overlay running**
26		FRAME_DONE	**Overlay frame complete**
25		FRAME_UNDERRUN	**Overlay frame underrun**
24		FRAME_SWRST_DONE	**Overlay frame reset done**
23		FRAME_HWRST_DONE	**Overlay EOF reset done**
21		TRIG	**Triggers overlay**

Bit(s)	Mnemonic	Name	Description
20		RST	**Resets overlay**
19		RDMA0_IDLE	**Overlay RDMA0 idle state**
18		RDMA1_IDLE	**Overlay RDMA1 idle state**
17		RDMA2_IDLE	**Overlay RDMA2 idle state**
16		RDMA3_IDLE	**Overlay RDMA3 idle state**
15		OUT_IDLE	**Overlay output relay idle state**
13		OVL_OUT_READY	**Overlay out_ready**
12		OVL_OUT_VALID	**Overlay out_valid**
11		BLEND_IDLE	**Overlay alpha blending idle state**
10		ADDCON_IDLE	**Overlay addcon idle state**
9:0		FSM_STATE	**Overlay flow control FSM state** 0x1: IDLE 0x2: WAIT 0x4: PREPARE 0x8: UPD_REG 0x10: ENG_CLR 0x20: ENG_ACT 0x40: H_WAIT_W_RST 0x80: S_WAIT_W_RST 0x100: H_W_RST 0x200: S_W_RST

1400C244 OVL_ADDCON_DBG **Overlay Address Control Debug** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L3_WIN_HIT	L2_WIN_HIT		ROI_Y												
Type	RU	RU		RU												
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L1_WIN_HIT	L0_WIN_HIT		ROI_X												
Type	RU	RU		RU												
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		L3_WIN_HIT	Overlay Layer 3 pixel hit
30		L2_WIN_HIT	Overlay Layer 2 pixel hit
28:16		ROI_Y	Overlay pixel process vertical Y position
15		L1_WIN_HIT	Overlay Layer 1 pixel hit
14		L0_WIN_HIT	Overlay Layer 0 pixel hit
12:0		ROI_X	Overlay pixel process horizontal X position

1400C24C OVL_RDMA0_DBG **Overlay RDMA0 Debug Monitor** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMI_GREQ	RDMA0_SMI_BU	RDMA0_OUT_VA	RDMA0_OUT_RE	RDMA0_OUT_DATA											

		SY	LID	ADY												
Type	RU	RU	RU	RU	RU											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA0_OUT_DATA												RDMA0_LAYER_GREQ	RDMA0_WRAM_RST_CS		
Type	RU												RU	RU		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31		SMI_GREQ	Overlay 4-to-1 SMI request
30		RDMA0_SMI_BUSY	Overlay RDMA0 SMI busy
29		RDMA0_OUT_VALI D	Overlay RDMA0 output valid
28		RDMA0_OUT_READ Y	Overlay RDMA0 output ready
27:4		RDMA0_OUT_DATA	Overlay RDMA0 output data
3		RDMA0_LAYER_GR EQ	Overlay RDMA0 SMI request
2:0		RDMA0_WRAM_RST _CS	Overlay RDMA0 warm reset current state

1400C250 OVL_RDMA1_DBG — Overlay RDMA1 Debug Monitor — 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMI_GREQ	RDMA1_SMI_BUSY	RDMA1_OUT_VALID	RDMA1_OUT_READY	RDMA1_OUT_DATA											
Type	RU	RU	RU	RU	RU											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA1_OUT_DATA												RDMA1_LAYER_GREQ	RDMA1_WRAM_RST_CS		
Type	RU												RU	RU		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31		SMI_GREQ	Overlay 4-to-1 SMI request
30		RDMA1_SMI_BUSY	Overlay RDMA1 SMI busy
29		RDMA1_OUT_VALI D	Overlay RDMA1 output valid
28		RDMA1_OUT_READ Y	Overlay RDMA1 output ready
27:4		RDMA1_OUT_DATA	Overlay RDMA1 output data
3		RDMA1_LAYER_GR EQ	Overlay RDMA1 SMI request
2:0		RDMA1_WRAM_RST _CS	Overlay RDMA1 warm reset current state

1400C254 OVL_RDMA2_DBG — Overlay RDMA2 Debug Monitor — 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMI_	RDMA	RDMA	RDMA	RDMA2_OUT_DATA											

	GREQ	2_SMI_BUSY	2_OUT_VALID	2_OUT_READY												
Type	RU	RU	RU	RU	RU											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA2_OUT_DATA												RDMA2_LAYER_GREQ	RDMA2_WRAM_RST_CS		
Type	RU												RU	RU		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31		SMI_GREQ	Overlay 4-to-1 SMI request
30		RDMA2_SMI_BUSY	Overlay RDMA2 SMI busy
29		RDMA2_OUT_VALI D	Overlay RDMA2 output valid
28		RDMA2_OUT_READ Y	Overlay RDMA2 output ready
27:4		RDMA2_OUT_DATA	Overlay RDMA2 output data
3		RDMA2_LAYER_GR EQ	Overlay RDMA2 SMI request
2:0		RDMA2_WRAM_RST _CS	Overlay RDMA2 warm reset current state

1400C258 OVL_RDMA3_DBG **Overlay RDMA3 Debug Monitor** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMI_GREQ	RDMA3_SMI_BUSY	RDMA3_OUT_VALID	RDMA3_OUT_READY	RDMA3_OUT_DATA											
Type	RU	RU	RU	RU	RU											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA3_OUT_DATA												RDMA3_LAYER_GREQ	RDMA3_WRAM_RST_CS		
Type	RU												RU	RU		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31		SMI_GREQ	Overlay 4-to-1 SMI request
30		RDMA3_SMI_BUSY	Overlay RDMA3 SMI busy
29		RDMA3_OUT_VALI D	Overlay RDMA3 output valid
28		RDMA3_OUT_READ Y	Overlay RDMA3 output ready
27:4		RDMA3_OUT_DATA	Overlay RDMA3 output data
3		RDMA3_LAYER_GR EQ	Overlay RDMA3 SMI request
2:0		RDMA3_WRAM_RST _CS	Overlay RDMA3 warm reset current state

1400C25C OVL_L0_CLR **Overlay Layer 0 Constant Color** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		ALPHA	Alpha component of Lo constant color
23:16		RED	Red component of Lo constant color
15:8		GREEN	Green component of Lo constant color
7:0		BLUE	Blue component of Lo constant color

1400C260 OVL_L1_CLR Overlay Layer 1 Constant Color FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		ALPHA	Alpha component of L1 constant color
23:16		RED	Red component of L1 constant color
15:8		GREEN	Green component of L1 constant color
7:0		BLUE	Blue component of L1 constant color

1400C264 OVL_L2_CLR Overlay Layer 2 Constant Color FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		ALPHA	Alpha component of L2 constant color
23:16		RED	Red component of L2 constant color
15:8		GREEN	Green component of L2 constant color
7:0		BLUE	Blue component of L2 constant color

1400C268 OVL_L3_CLR Overlay Layer 3 Constant Color FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		ALPHA	Alpha component of L3 constant color
23:16		RED	Red component of L3 constant color
15:8		GREEN	Green component of L3 constant color
7:0		BLUE	Blue component of L3 constant color

1400C26C OVL_LC_CLR Overlay Constant Layer Color FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		ALPHA	Alpha component of constant layer color
23:16		RED	Red component of constant layer color
15:8		GREEN	Green component of constant layer color
7:0		BLUE	Blue component of constant layer color

1400C270 OVL_CRC Overlay CRC 7FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRC_RDY	CRC_OUT														
Type	RU	RU														
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRC_OUT															
Type	RU															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31		CRC_RDY	
30:0		CRC_OUT	

1400C280 OVL_LC_CON Overlay Constant Layer Control 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSTKEY_E	SRCKEY_E	LAYER_SRC							R_FIRST	LANDSCAP	EN_3D				

	N	N									E					
Type	RW	RW	RW							RW	RW	RW				
Reset	0	0	0	0						0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								ALPHA_EN	ALPHA							
Type								RW	RW							
Reset								0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**DKEN**	DSTKEY_EN	**Enables destination color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable destination color key 1: Enable destination color key
30	**SKEN**	SRCKEY_EN	**Enables source color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable source color key 1: Enable source color key
29:28	**LSRC**	LAYER_SRC	**Selects layer pixel from memory/constant color/SCL/PQ** 00: Layer pixel from constant color 01: Layer pixel from constant color 10: Layer pixel from UFOd 11: Layer pixel from PQ
22		R_FIRST	**Right eye image first when in 3D mode** 0: Show left eye image first in 3D mode 1: Show right eye image first in 3D mode
21		LANDSCAPE	**Enables 3D landscape mode** 0: 3D portrait mode 1: 3D landscape mode
20		EN_3D	**Enables 3D mode** 0: 2D mode 1: 3D mode
8	**AEN**	ALPHA_EN	**Enables alpha blending** 0: Disable alpha blending 1: Enable alpha blending
7:0	**APHA**	ALPHA	**Constant alpha value**

1400C284 OVL_LC_SRCKEY Overlay Constant Layer Source Key 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SKEY**	SRCKEY	**Layer source color key** Active when source color key is enabled.

Bit(s)	Mnemonic	Name	Description

1400C288 OVL_LC_SRC_SIZE **Overlay Layer C Source Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LC_SRC_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				LC_SRC_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	LCH	LC_SRC_H	**Layer source height** Range: 0 ~ 4095
12:0	LCW	LC_SRC_W	**Layer source width** Range: 0 ~ 4095

1400C28C OVL_LC_OFFSET **Overlay Layer C Offset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LC_YOFF											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					LC_XOFF											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	LCH	LC_YOFF	**Layer vertical Y offset** Range: 0 ~ 4095
11:0	LCXO	LC_XOFF	**Layer horizontal X offset** Range: 0 ~ 4095

1400C290 OVL_LC_SRC_SEL **Overlay Constant Layer Source Selection** **00000004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SURFL_EN	LC_BLEND_RND_SHT		LC_CONST_BLD	LC_DRGB_SEL_EXT	LC_DA_SEL_EXT	LC_SRGB_SEL_EXT	LC_SA_SEL_EXT	LC_D RGB_SEL		LC_D A_SEL		LC_S RGB_SEL		LC_SA_SEL	
Type	RW	RW		RW	RW	RW	RW	RW	RW		RW		RW		RW	
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CONST_LAYER_SEL		

Type														RW		
Reset														1	0	0

Bit(s)	Mnemonic	Name	Description
31	**LCSP**	SURFL_EN	**Enables layer surface dlinger alpha_blending** 0: Disable surface flinger alpha_blending 1: Enable surface flinger alpha_blending
30		LC_BLEND_RND_SHT	
28		LC_CONST_BLD	
27		LC_DRGB_SEL_EXT	**Selects layer destination_RGB alpha**
26		LC_DA_SEL_EXT	**Selects layer destination_Alpha alpha**
25		LC_SRGB_SEL_EXT	**Selects layer source_RGB alpha**
24		LC_SA_SEL_EXT	**Selects layer source_Alpha alpha**
23:22	**LCSP**	LC_DRGB_SEL	**Selects layer destination_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
21:20	**LCSP**	LC_DA_SEL	**Selects layer destination_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
19:18	**LCSP**	LC_SRGB_SEL	**Selects layer source_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
17:16	**LCSP**	LC_SA_SEL	**Selects layer source_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
2:0	**LCSP**	CONST_LAYER_SEL	**Layer source pitch**

1400C29C OVL_BANK_CON Overlay Bank Control 00000008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												OVL_BANK_CON				
Type												RW				
Reset												0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		OVL_BANK_CON	

1400C2A0 OVL_FUNC_D Overlay Functional DCM0 00000000

CM0 Control

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OVL_FUNC_DCM0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OVL_FUNC_DCM0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		OVL_FUNC_DCM0	Controls functional DCM0

1400C2A4 OVL_FUNC_DCM1 Overlay Functional DCM1 Control **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OVL_FUNC_DCM1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OVL_FUNC_DCM1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		OVL_FUNC_DCM1	Controls functional DCM1

1400CFC0 OVL_SECURE Overlay Layer Secure Bit **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													L3_SECURE	L2_SECURE	L1_SECURE	L0_SECURE
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3		L3_SECURE	Layer 3 secure bit
2		L2_SECURE	Layer 2 secure bit
1		L1_SECURE	Layer 1 secure bit
0		L0_SECURE	Layer 0 secure bit

Module name: DISP_OVL0_2L Base address: (+1400d000h)

Address	Name	Width	Register Function
1400D000	OVL_STA	32	Overlay Status Monitor
1400D004	OVL_INTEN	32	Overlay Interrupt Enable
1400D008	OVL_INTSTA	32	Overlay Interrupt Status
1400D00C	OVL_EN	32	Overlay Enable
1400D010	OVL_TRIG	32	Overlay Trigger
1400D014	OVL_RST	32	Overlay Reset
1400D020	OVL_ROI_SIZE	32	Overlay ROI Size
1400D024	OVL_DATAPATH_CON	32	Overlay Datapath Control
1400D028	OVL_ROI_BGCLR	32	Overlay Background Color
1400D02C	OVL_SRC_CON	32	Overlay Source Control
1400D030	OVL_L0_CON	32	Overlay Layer 0 Control
1400D034	OVL_L0_SRCKEY	32	Overlay Layer 0 Source Key
1400D038	OVL_L0_SRC_SIZE	32	Overlay Layer 0 Source Size
1400D03C	OVL_L0_OFFSET	32	Overlay Layer 0 Offset
1400DF40	OVL_L0_ADDR	32	Overlay Layer 0 Memory Address
1400D044	OVL_L0_PITCH	32	Overlay Layer 0 Pitch
1400D048	OVL_L0_TILE	32	Overlay Layer 0 Tile Control
1400D04C	OVL_L0_CLIP	32	Overlay Layer 0 Clip
1400D050	OVL_L1_CON	32	Overlay Layer 1 Control
1400D054	OVL_L1_SRCKEY	32	Overlay Layer 1 Source Key
1400D058	OVL_L1_SRC_SIZE	32	Overlay Layer 1 Source Size
1400D05C	OVL_L1_OFFSET	32	Overlay Layer 1 Offset
1400DF60	OVL_L1_ADDR	32	Overlay Layer 1 Memory Address
1400D064	OVL_L1_PITCH	32	Overlay Layer 1 Pitch
1400D068	OVL_L1_TILE	32	Overlay Layer 1 Tile Control
1400D06C	OVL_L1_CLIP	32	Overlay Layer 1 Clip
1400D088	OVL_L2_TILE	32	Overlay Layer 2 Tile Control
1400D090	OVL_L3_CON	32	Overlay Layer 3 Control
1400D09C	OVL_L3_OFFSET	32	Overlay Layer 3 Offset
1400D0A8	OVL_L3_TILE	32	Overlay Layer 3 Tile Control
1400D0C0	OVL_RDMA0_CTRL	32	Overlay RDMA0 Control
1400D0C8	OVL_RDMA0_MEM_GMC_SETTING1	32	Overlay RDMA0 Memory GMC Setting
1400D0CC	OVL_RDMA0_MEM_SLOW_CON	32	Overlay RDMA0 Memory Slow Control
1400D0D0	OVL_RDMA0_FIFO_CTRL	32	Overlay RDMA0 FIFO Control
1400D0E0	OVL_RDMA1_CTRL	32	Overlay RDMA1 Control
1400D0E8	OVL_RDMA1_MEM_GMC_SETTING1	32	Overlay RDMA1 Memory GMC Setting
1400D0EC	OVL_RDMA1_MEM_SLOW_CON	32	Overlay RDMA1 Memory Slow Control
1400D0F0	OVL_RDMA1_FIFO_CTRL	32	Overlay RDMA1 FIFO Control
1400D108	OVL_RDMA2_MEM_GMC_SETTING1	32	Overlay RDMA2 Memory GMC Setting

Address	Name	Width	Register Function
1400D10C	OVL_RDMA2_MEM_SLOW_CON	32	Overlay RDMA2 Memory Slow Control
1400D110	OVL_RDMA2_FIFO_CTRL	32	Overlay RDMA2 FIFO Control
1400D120	OVL_RDMA3_CTRL	32	Overlay RDMA3 Control
1400D128	OVL_RDMA3_MEM_GMC_SETTING1	32	Overlay RDMA3 Memory GMC Setting
1400D12C	OVL_RDMA3_MEM_SLOW_CON	32	Overlay RDMA3 Memory Slow Control
1400D130	OVL_RDMA3_FIFO_CTRL	32	Overlay RDMA3 FIFO Control
1400D134	OVL_L0_Y2R_PARA_R0	32	Overlay L0 Y2R Conversion Parameter R0
1400D138	OVL_L0_Y2R_PARA_R1	32	Overlay L0 Y2R Conversion Parameter R1
1400D13C	OVL_L0_Y2R_PARA_G0	32	Overlay L0 Y2R Conversion Parameter G0
1400D140	OVL_L0_Y2R_PARA_G1	32	Overlay L0 Y2R Conversion Parameter G1
1400D144	OVL_L0_Y2R_PARA_B0	32	Overlay L0 Y2R Conversion Parameter B0
1400D148	OVL_L0_Y2R_PARA_B1	32	Overlay L0 Y2R Conversion Parameter B1
1400D14C	OVL_L0_Y2R_PARA_YUV_A_0	32	Overlay L0 Y2R Conversion Parameter Extended Add on YUV 0
1400D150	OVL_L0_Y2R_PARA_YUV_A_1	32	Overlay L0 Y2R Conversion Parameter Extended Add on YUV 1
1400D154	OVL_L0_Y2R_PARA_RGB_A_0	32	Overlay L0 Y2R Conversion Parameter Extended Add on RGB 0
1400D158	OVL_L0_Y2R_PARA_RGB_A_1	32	Overlay L0 Y2R Conversion Parameter Extended Add on RGB 1
1400D15C	OVL_L1_Y2R_PARA_R0	32	Overlay L1 Y2R Conversion Parameter R0
1400D160	OVL_L1_Y2R_PARA_R1	32	Overlay L1 Y2R Conversion Parameter R1
1400D164	OVL_L1_Y2R_PARA_G0	32	Overlay L1 Y2R Conversion Parameter G0
1400D168	OVL_L1_Y2R_PARA_G1	32	Overlay L1 Y2R Conversion Parameter G1
1400D16C	OVL_L1_Y2R_PARA_B0	32	Overlay L1 Y2R Conversion Parameter B0
1400D170	OVL_L1_Y2R_PARA_B1	32	Overlay L1 Y2R Conversion Parameter B1
1400D174	OVL_L1_Y2R_PARA_YUV_A_0	32	Overlay L1 Y2R Conversion Parameter Extended Add on YUV 0
1400D178	OVL_L1_Y2R_PARA_YUV_A_1	32	Overlay L1 Y2R Conversion Parameter Extended Add on YUV 1
1400D17C	OVL_L1_Y2R_PARA_RGB_A_0	32	Overlay L1 Y2R Conversion Parameter Extended Add on RGB 0
1400D180	OVL_L1_Y2R_PARA_RGB_A_1	32	Overlay L1 Y2R Conversion Parameter Extended Add on RGB 1
1400D184	OVL_L2_Y2R_PARA_R0	32	Overlay L2 Y2R Conversion Parameter R0
1400D188	OVL_L2_Y2R_PAR	32	Overlay L2 Y2R Conversion Parameter R1

Address	Name	Width	Register Function
	A_R1		
1400D18C	OVL_L2_Y2R_PARA_G0	32	Overlay L2 Y2R Conversion Parameter G0
1400D190	OVL_L2_Y2R_PARA_G1	32	Overlay L2 Y2R Conversion Parameter G1
1400D194	OVL_L2_Y2R_PARA_B0	32	Overlay L2 Y2R Conversion Parameter B0
1400D198	OVL_L2_Y2R_PARA_B1	32	Overlay L2 Y2R Conversion Parameter B1
1400D19C	OVL_L2_Y2R_PARA_YUV_A_0	32	Overlay L2 Y2R Conversion Parameter Extended Add on YUV 0
1400D1A0	OVL_L2_Y2R_PARA_YUV_A_1	32	Overlay L2 Y2R Conversion Parameter Extended Add on YUV 1
1400D1A4	OVL_L2_Y2R_PARA_RGB_A_0	32	Overlay L2 Y2R Conversion Parameter Extended Add on RGB 0
1400D1A8	OVL_L2_Y2R_PARA_RGB_A_1	32	Overlay L2 Y2R Conversion Parameter Extended Add on RGB 1
1400D1AC	OVL_L3_Y2R_PARA_R0	32	Overlay L3 Y2R Conversion Parameter R0
1400D1B0	OVL_L3_Y2R_PARA_R1	32	Overlay L3 Y2R Conversion Parameter R1
1400D1B4	OVL_L3_Y2R_PARA_G0	32	Overlay L3 Y2R Conversion Parameter G0
1400D1B8	OVL_L3_Y2R_PARA_G1	32	Overlay L3 Y2R Conversion Parameter G1
1400D1BC	OVL_L3_Y2R_PARA_B0	32	Overlay L3 Y2R Conversion Parameter B0
1400D1C0	OVL_L3_Y2R_PARA_B1	32	Overlay L3 Y2R Conversion Parameter B1
1400D1C4	OVL_L3_Y2R_PARA_YUV_A_0	32	Overlay L3 Y2R Conversion Parameter Extended Add on YUV 0
1400D1C8	OVL_L3_Y2R_PARA_YUV_A_1	32	Overlay L3 Y2R Conversion Parameter Extended Add on YUV 1
1400D1CC	OVL_L3_Y2R_PARA_RGB_A_0	32	Overlay L3 Y2R Conversion Parameter Extended Add on RGB 0
1400D1D0	OVL_L3_Y2R_PARA_RGB_A_1	32	Overlay L3 Y2R Conversion Parameter Extended Add on RGB 1
1400D1D4	OVL_DEBUG_MON_SEL	32	Overlay Debug Monitor Select
1400D1E0	OVL_RDMA0_MEM_GMC_SETTING2	32	Overlay RDMA0 Memory GMC Setting
1400D1E4	OVL_RDMA1_MEM_GMC_SETTING2	32	Overlay RDMA1 Memory GMC Setting
1400D1F0	OVL_RDMA_BURST_CON0	32	Overlay RDMA Burst Control
1400D1F4	OVL_RDMA_BURST_CON1	32	Overlay RDMA Burst Control
1400D1F8	OVL_RDMA_GREQ_NUM	32	Overlay RDMA GREQ Number
1400D1FC	OVL_RDMA_GREQ_URG_NUM	32	Overlay RDMA GREQ Number
1400D200	OVL_DUMMY_REG	32	Overlay Dummy Register
1400D208	OVL_GDRDY_PRD	32	Overlay SMI GDRDY Period
1400D20C	OVL_RDMA_ULTRA	32	Overlay RDMA Ultra SRC

Address	Name	Width	Register Function
	SRC		
1400D210	OVL_RDMA0_BUF_LOW	32	Overlay RDMA BUF Low
1400D214	OVL_RDMA1_BUF_LOW	32	Overlay RDMA BUF Low
1400D230	OVL_SMI_DBG	32	Overlay SMI Arbiter Debug Monitor
1400D234	OVL_GREQ_LAYER_CNT	32	Overlay Layer GREQ Counter
1400D238	OVL_GDRDY_PRD_NUM	32	Overlay SMI GDRDY Period Number
1400D240	OVL_FLOW_CTRL_DBG	32	Overlay Flow Control Debug Monitor
1400D244	OVL_ADDCON_DBG	32	Overlay Address Control Debug
1400D24C	OVL_RDMA0_DBG	32	Overlay RDMA0 Debug Monitor
1400D250	OVL_RDMA1_DBG	32	Overlay RDMA1 Debug Monitor
1400D25C	OVL_L0_CLR	32	Overlay Layer 0 Constant Color
1400D260	OVL_L1_CLR	32	Overlay Layer 1 Constant Color
1400D26C	OVL_LC_CLR	32	Overlay Constant Layer Color
1400D270	OVL_CRC	32	Overlay CRC
1400D280	OVL_LC_CON	32	Overlay Constant Layer Control
1400D284	OVL_LC_SRCKEY	32	Overlay Constant Layer Source Key
1400D288	OVL_LC_SRC_SIZE	32	Overlay Layer C Source Size
1400D28C	OVL_LC_OFFSET	32	Overlay Layer C Offset
1400D290	OVL_LC_SRC_SEL	32	Overlay Constant Layer Source Selection
1400D29C	OVL_BANK_CON	32	Overlay Bank Control
1400DFC0	OVL_SECURE	32	Overlay Layer Secure Bit

1400D000 OVL_STA **Overlay Status Monitor** **00000006**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**RDMA1_IDLE**	**RDMA0_IDLE**	**OVL_RUN**
Type														RU	RU	RU
Reset														1	1	0

Bit(s)	Mnemonic	Name	Description
2		RDMA1_IDLE	**Status of overlay RDMA1** 0: RDMA is in running. 1: Overlay RDMA are all idle.
1		RDMA0_IDLE	**Status of overlay RDMA0** 0: RDMA is in running. 1: Overlay RDMA are all idle.
0		OVL_RUN	**Status of overlay engine** 0: Overlay is idle. 1: Overlay is running.

Bit(s)	Mnemonic	Name	Description

1400D004 OVL_INTEN **Overlay Interrupt Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ABNORMAL_SOF_INTEN			RDMA1_SMI_UNDERFLOW_INTEN	RDMA0_SMI_UNDERFLOW_INTEN			RDMA1_EOF_ABNORMAL_INTEN	RDMA0_EOF_ABNORMAL_INTEN	OVL_FME_HWRST_DONE_INTEN	OVL_FME_SWRST_DONE_INTEN	OVL_FME_UND_INTEN	OVL_FME_CPL_INTEN	OVL_REG_CMT_INTEN
Type			RW			RW	RW			RW	RW	RW	RW	RW	RW	RW
Reset			0			0	0			0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13		ABNORMAL_SOF_INTEN	**Control abnormal SOF interrupt**
10		RDMA1_SMI_UNDERFLOW_INTEN	**Control RDMA1 SMI underflow interrupt** 0: Disable RDMA1 SMI data underflow interrupt 1: Enable RDMA1 SMI data underflow interrupt
9		RDMA0_SMI_UNDERFLOW_INTEN	**Control RDMA0 SMI underflow interrupt** 0: Disable RDMA0 SMI data underflow interrupt 1: Enable RDMA0 SMI data underflow interrupt
6		RDMA1_EOF_ABNORMAL_INTEN	**Control RDMA1 EOF abnormal interrupt** 0: Disable RDMA1 EOF abnormal interrupt 1: Enable RDMA1 EOF abnormal interrupt
5		RDMA0_EOF_ABNORMAL_INTEN	**Control RDMA0 EOF abnormal interrupt** 0: Disable RDMA0 EOF abnormal interrupt 1: Enable RDMA0 EOF abnormal interrupt
4		OVL_FME_HWRST_DONE_INTEN	**Control frame HW reset done interrupt** 0: Disable frame HW reset done interrupt 1: Enable frame HW reset done interrupt
3		OVL_FME_SWRST_DONE_INTEN	**Control frame SW reset done interrupt** 0: Disable frame SW reset done interrupt 1: Enable frame SW reset done interrupt
2		OVL_FME_UND_INTEN	**Control frame underflow interrupt** 0: Disable frame underflow interrupt 1: Enable frame underflow interrupt
1		OVL_FME_CPL_INTEN	**Control frame complete interrupt** 0: Disable frame complete interrupt 1: Enable frame complete interrupt
0		OVL_REG_CMT_INTEN	**Control register setting complete interrupt** 0: Disable register commit interrupt 1: Enable register commit interrupt

1400D008 OVL_INTSTA **Overlay Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ABNORMAL_SOF_INTSTA			RDMA1_SMI_UNDERFLOW_INTSTA	RDMA0_SMI_UNDERFLOW_INTSTA			RDMA1_EOF_ABNORMAL_INTSTA	RDMA0_EOF_ABNORMAL_INTSTA	OVL_FME_HWRST_DONE_INTSTA	OVL_FME_SWRST_DONE_INTSTA	OVL_FME_UND_INTSTA	OVL_FME_CPL_INTSTA	OVL_REG_CMT_INTSTA
Type			A1			A1	A1			A1	A1	A1	A1	A1	A1	A1
Reset			0			0	0			0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13		ABNORMAL_SOF_INTSTA	
10		RDMA1_SMI_UNDERFLOW_INTSTA	**RDMA1 SMI status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA1 SMI data are not underflow. 1: RDMA1 SMI data are underflow.
9		RDMA0_SMI_UNDERFLOW_INTSTA	**RDMA0 SMI status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA0 SMI data are not underflow. 1: RDMA0 SMI data are underflow.
6		RDMA1_EOF_ABNORMAL_INTSTA	**RDMA1 status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA1 complete normally 1: RDMA1 not complete till EOF
5		RDMA0_EOF_ABNORMAL_INTSTA	**RDMA0 status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA0 complete normally 1: RDMA0 not complete till EOF
4		OVL_FME_HWRST_DONE_INTSTA	**Overlay HW reset done status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: No HW reset/HW reset is not done. 1: HW reset is done.
3		OVL_FME_SWRST_DONE_INTSTA	**Overlay SW reset done status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: No SW reset/SW reset is not done. 1: SW reset is done.
2		OVL_FME_UND_INTSTA	**Overlay frame underflow status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: Frame complete w/o underflow 1: Frame not complete w/ underflow
1		OVL_FME_CPL_INTSTA	**Overlay frame complete status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: Frame not complete 1: Frame complete
0		OVL_REG_CMT_INTSTA	**Overlay register commit status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: Regsiter is not set from shadow register to working register. 1: Register is set to working register done.

Bit(s)	Mnemonic	Name	Description

1400D00C OVL_EN **Overlay Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																IGNORE_ABNORMAL_SOF
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							HG_FSMI_CK_ON	HG_FOVL_CK_ON								OVL_EN
Type							RW	RW								RW
Reset							0	0								0

Bit(s)	Mnemonic	Name	Description
16		IGNORE_ABNORMAL_SOF	
9		HG_FSMI_CK_ON	
8		HG_FOVL_CK_ON	
0	**OVEN**	OVL_EN	**Enables overlay engine** 0: Disable overlay 1: Enable overlay

1400D010 OVL_TRIG **Overlay Trigger** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							CRC_CLR	CRC_EN								OVL_SW_TRIG
Type							RW	RW								RW
Reset							0	0								0

Bit(s)	Mnemonic	Name	Description
9		CRC_CLR	
8		CRC_EN	
0	**OVTR**	OVL_SW_TRIG	**SW trigger to enable overlay engine** 0: When using HW trigger (SOF), this bit should be 0. 1: SW control to enable overlay engine.

1400D014 OVL_RST **Overlay Reset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																OVL_RST
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		OVL_RST	**Overlay SW reset control for engine (high active)** 1: Reset engine

1400D020 OVL_ROI_SIZE Overlay ROI Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				ROI_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				ROI_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**ROIH**	ROI_H	**Overlay ROI width** Range: 1 ~ 8191. For 3D display, this value should be 2 ~ 8191.
12:0	**ROIW**	ROI_W	**Overlay ROI width** Range: 1 ~ 8191. For 3D display, this value should be 2 ~ 8191.

1400D024 OVL_DATAPATH_CON Overlay Datapath Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									RDMA3_OUT_SEL	RDMA2_OUT_SEL	RDMA1_OUT_SEL	RDMA0_OUT_SEL			PQ_OUT_SEL	
Type									OTHER	OTHER	OTHER	OTHER			OTHER	
Reset									0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OVL_GAMMA_OUT	ADOBE_LAYER		ADOBE_MODE			L1_GPU_MODE	Lo_GPU_MODE					OUTPUT_NO_RND	BGCLR_IN_SEL	OVL_RANDOM_BGCLR_EN	LAYER_SMI_ID_EN
Type	RW	RW		RW			RW	RW					RW	RW	RW	RW
Reset	0	0	0	0			0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
23	**RDMA3SEL**	RDMA3_OUT_SEL	**Selects output path of RDMA3**

Bit(s)	Mnemonic	Name	Description
			0: OVL Layer 3 1: PQ direct link output
22	**RDMA2SEL**	RDMA2_OUT_SEL	**Selects output path of RDMA2** 0: OVL Layer 2 1: PQ direct link output
21	**RDMA1SEL**	RDMA1_OUT_SEL	**Selects output path of RDMA1** 0: OVL Layer 1 1: PQ direct link output
20	**RDMA0SEL**	RDMA0_OUT_SEL	**Selects output path of RDMA0** 0: OVL Layer 0 1: PQ direct link output
17:16	**PQSEL**	PQ_OUT_SEL	**Selects PQ direct link output data** 00: RDMA0 01: RDMA1 10: RDMA2 11: RDMA3
15	**OVL_GAMMA_OUT**	OVL_GAMMA_OUT	**Wide-gamut OVL output GAMMA table path** (shares GAMMA-table with layer Adobe_mode) 0: Disable OVL output GAMMA table 1: Enable OVL output GAMMA table
14:13	**ADOBE_LAYER**	ADOBE_LAYER	**Selects wide-gamut layer Adobe** 0: Select Layer 0 adobe_path 1: Select Layer 1 adobe_path 2: Select Layer 2 adobe_path 3: Select Layer 3 adobe_path
12	**ADOBE**	ADOBE_MODE	**Wide-gamut layer Adobe mode** (shares GAMMA-table with ovl_gamma_out mode) 0: Disable layer Adobe path 1: Enable layer Adobe path
9	**L1_GPU**	L1_GPU_MODE	**Wide-gamut Layer 1 GPU path mode** 0: Disable Layer 1 GPU path 1: Enable Layer 1 GPU path
8	**L0_GPU**	L0_GPU_MODE	**Wide-gamut Layer 0 GPU path mode** 0: Disable Layer 0 GPU path 1: Enable Layer 0 GPU path
3		OUTPUT_NO_RND	
2		BGCLR_IN_SEL	**OVL BGCLR direct link path** 0: Disable OVL BGCLR direct link input 1: Enable OVL BGCLR direct link input
1		OVL_RANDOM_BGCLR_EN	**When OVL_RANDOM_BGCLR_EN=1, layer_en[i] should be set to 0 to allow the background color to pass through the Blend engine.** 0: Disable random background color pattern 1: Enable random background color pattern
0	**LAYER_SMI_ID_EN**	LAYER_SMI_ID_E N	**Supports OVL SMI ID function** 0: Disable SMI ID 1: Enable SMI ID

1400D028 OVL_ROI_BGCLR **Overlay Background Color** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							
Type	RW								RW							

Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24	**BGDA**	ALPHA	Alpha component of ROI window background color
23:16	**BGDR**	RED	Red component of ROI window background color
15:8	**BGDG**	GREEN	Green component of ROI window background color
7:0	**BGDB**	BLUE	Blue component of ROI window background color

1400D02C OVL_SRC_CON **Overlay Source Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												LC_EN			L1_EN	Lo_EN
Type												RW			RW	RW
Reset												0			0	0

Bit(s)	Mnemonic	Name	Description
4	**LCEN**	LC_EN	**Set up this bit to enable overlay constant layer.** 0: Disable constant layer 1: Enable constant layer
1	**L1EN**	L1_EN	**Set up this bit to enable overlay Layer 1.** 0: Disable Layer 1 1: Enable Layer 1
0	**LoEN**	Lo_EN	**Set up this bit to enable overlay Layer 0.** 0: Disable Layer 0 1: Enable Layer 0

1400D030 OVL_Lo_CON **Overlay Layer 0 Control** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSTKEY_EN	SRCKEY_EN	LAYER_SRC		MTX_EN	MTX_AUTO_DIS	RGB_SWAP	BYTE_SWAP	CLRFMT_MAN	R_FIRST	LANDSCAPE	EN_3D	INT_MTX_SEL			
Type	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLRFMT				EXT_MTX_EN	HORIZONTAL_FLIP_EN	VERTICAL_FLIP_EN	ALPHA_EN	ALPHA							
Type	RW				OTHER	RW	RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
31	**DKEN**	DSTKEY_EN	**Enables destination color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable destination color key 1: Enable destination color key
30	**SKEN**	SRCKEY_EN	**Enables source color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable source color key 1: Enable source color key
29:28	**LSRC**	LAYER_SRC	**Selects layer pixel from memory/constant color/SCL/PQ** 00: Layer pixel from memory RDMA0 01: Layer pixel from constant color 10: Layer pixel from UFOd 11: Layer pixel from PQ
27		MTX_EN	
26		MTX_AUTO_DIS	
25	**RGSW**	RGB_SWAP	**No use**
24	**BTSW**	BYTE_SWAP	**Swaps unified color format** 0: RGB565, BGR888, BGRA8888, ABGR8888, UYVY, YUYV 1: BGR565, RGB888, RGBA8888, ARGB8888, VYUY, YVYU
23		CLRFMT_MAN	
22		R_FIRST	**Right eye image first when in 3D mode** 0: Show left eye image first in 3D mode 1: Show right eye image first in 3D mode
21		LANDSCAPE	**Enables 3D landscape mode** 0: 3D portrait mode 1: 3D landscape mode
20		EN_3D	**Enables 3D mode** 0: 2D mode 1: 3D mode
19:16	**MTX**	INT_MTX_SEL	**Selects color matrix table** 0000: MTX_RGB_TO_JPEG 0010: MTX_RGB_TO_BT601 0011: MTX_RGB_TO_BT709 0100: MTX_JPEG_TO_RGB 0110: MTX_BT601_TO_RGB 0111: MTX_BT709_TO_RGB 1000: MTX_JPEG_TO_BT601 1001: MTX_JPEG_TO_BT709 1010: MTX_BT601_TO_JPEG 1011: MTX_BT709_TO_JPEG 1100: MTX_BT709_TO_BT601 1101: MTX_BT601_TO_BT709 Others: HW default (JPEG_TO_RGB)
15:12	**CFMT**	CLRFMT	**//--OLD define for reference only** 0000: RGB888 0001: RGB565 0010: ARGB8888 0011: PARGB8888 0100: xARGB8888 1000: YUYV 1001: UYVY 1010: YVYU

Bit(s)	Mnemonic	Name	Description
			1011: VYUY 1111: YUV444 Others: Reserved color format 0000: RGB565 0001: RGB888 0010: RGBA8888/BGRA8888 0011: ARGB8888/ABGR8888 0100: UVVY, VYUY 0101: YUYV, YVYU
11	**MTXEN**	EXT_MTX_EN	**Enables external programmable coeff** 0: Matrix coeff 1: Programmable coeff
10	**HFE**	HORIZONTAL_FLIP_EN	**Enables horizontal flip** 0: Disable horizontal flip 1: Enable horizontal flip
9	**VFE**	VERTICAL_FLIP_ EN	**Enables vertical flip** 0: Disable vertical flip 1: Enable vertical flip
8	**AEN**	ALPHA_EN	**Enables alpha blending** 0: Disable alpha blending 1: Enable alpha blending
7:0	**APHA**	ALPHA	**Constant alpha value**

1400D034 OVL_Lo_SRCKEY **Overlay Layer 0 Source Key** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SKEY**	SRCKEY	**Layer source color key** Active when source color key is enabled.

1400D038 OVL_Lo_SRCSIZE **Overlay Layer 0 Source Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				Lo_SRC_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				Lo_SRC_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
28:16	**LoH**	Lo_SRC_H	**Layer source height** Range: 0 ~ 8191
12:0	**LoW**	Lo_SRC_W	**Layer source width** Range: 0 ~ 8191

1400D03C OVL_Lo_OFFSET Overlay Layer 0 Offset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				Lo_YOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				Lo_XOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**LoH**	Lo_YOFF	**Layer vertical Y offset** Range: 0 ~ 8191
12:0	**LoXO**	Lo_XOFF	**Layer horizontal X offset** Range: 0 ~ 8191

1400DF40 OVL_Lo_ADDR Overlay Layer 0 Memory Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Lo_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Lo_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**LoAD**	Lo_ADDR	Layer memory buffer address

1400D044 OVL_Lo_PITCH Overlay Layer 0 Pitch 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SURFL_EN	Lo_BLEND_RND_SHT		Lo_CONST_BLD	Lo_DRGB_SEL_EXT	Lo_DA_SEL_EXT	Lo_SRGB_SEL_EXT	Lo_SA_SEL_EXT	Lo_DRGB_SEL		Lo_DA_SEL		Lo_SRGB_SEL		Lo_SA_SEL	
Type	RW	RW		RW	RW	RW	RW	RW	RW		RW		RW		RW	
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Lo_SRC_PITCH															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**LoSP**	SURFL_EN	**Enables layer surface dlinger alpha_blending** 0: Disable surface flinger alpha_blending 1: Enable surface flinger alpha_blending
30		Lo_BLEND_RND_SHT	
28		Lo_CONST_BLD	
27		Lo_DRGB_SEL_EXT	**Selects layer destination_RGB alpha**
26		Lo_DA_SEL_EXT	**Selects layer destination_Alpha alpha**
25		Lo_SRGB_SEL_EXT	**Selects layer source_RGB alpha**
24		Lo_SA_SEL_EXT	**Selects layer source_Alpha alpha**
23:22	**LoSP**	Lo_DRGB_SEL	**Selects layer destination_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
21:20	**LoSP**	Lo_DA_SEL	**Selects layer destination_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
19:18	**LoSP**	Lo_SRGB_SEL	**Selects layer source_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
17:16	**LoSP**	Lo_SA_SEL	**Selects layer source_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
15:0	**LoSP**	Lo_SRC_PITCH	**Layer source pitch**

1400D048 OVL_Lo_TILE **Overlay Layer 0 Tile Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TILE_HORI_BLOCK_NUM										TILE_EN	TILE_WIDTH_SEL	TILE_HEIGHT			
Type	OTHER										OTHER	OTHER	OTHER			
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TILE_HEIGHT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**TILE_BLKS**	TILE_HORI_BLOCK_NUM	**Number of horizontal blocks**
21	**TILE_EN**	TILE_EN	**Enables tile mode** 0: Disable

Bit(s)	Mnemonic	Name	Description
20	**TILE_W**	TILE_WIDTH_SEL	1: Enable **Width of tile** 0: 16 1: 32
19:0	**TILE_H**	TILE_HEIGHT	**Height of source tile mode**

1400D04C OVL_L0_CLIP **Overlay Layer 0 Clip** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L0_SRC_BOTTOM_CLIP								L0_SRC_TOP_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L0_SRC_RIGHT_CLIP								L0_SRC_LEFT_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**L0_SRC_BOTTOM_CLIP**	L0_SRC_BOTTOM_CLIP	Layer 0 bottom clip
23:16	**L0_SRC_TOP_CLIP**	L0_SRC_TOP_CLIP	Layer 0 top clip
15:8	**L0_SRC_RIGHT_CLIP**	L0_SRC_RIGHT_CLIP	Layer 0 right clip
7:0	**L0_SRC_LEFT_CLIP**	L0_SRC_LEFT_CLIP	Layer 0 left clip

1400D050 OVL_L1_CON **Overlay Layer 1 Control** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSTKEY_EN	SRCKEY_EN	LAYER_SRC		MTX_EN	MTX_AUTO_DIS	RGB_SWAP	BYTE_SWAP	CLRFMT_MAN	R_FIRST	LANDSCAPE	EN_3D	INT_MTX_SEL			
Type	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLRFMT				EXT_MTX_EN	HORIZONTAL_FLIP_EN	VERTICAL_FLIP_EN	ALPHA_EN	ALPHA							
Type	RW				OTHER	RW	RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**DKEN**	DSTKEY_EN	**Enables destination color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable destination color key 1: Enable destination color key
30	**SKEN**	SRCKEY_EN	**Enables source color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable source color key 1: Enable source color key

Bit(s)	Mnemonic	Name	Description
29:28	**LSRC**	LAYER_SRC	**Selects layer pixel from memory/constant color/SCL/PQ** 00: Layer pixel from memory RDMA1 01: Layer pixel from constant color 10: Layer pixel from UFOd 11: Layer pixel from PQ
27		MTX_EN	
26		MTX_AUTO_DIS	
25	**RGSW**	RGB_SWAP	**No use**
24	**BTSW**	BYTE_SWAP	**Swaps unified color format** 0: RGB565, BGR888, BGRA8888, ABGR8888, UYVY, YUYV 1: BGR565, RGB888, RGBA8888, ARGB8888, VYUY, YVYU
23		CLRFMT_MAN	
22		R_FIRST	**Right eye image first when in 3D mode** 0: Show left eye image first in 3D mode 1: Show right eye image first in 3D mode
21		LANDSCAPE	**Enables 3D landscape mode** 0: 3D portrait mode 1: 3D landscape mode
20		EN_3D	**Enables 3D mode** 0: 2D mode 1: 3D mode
19:16	**MTX**	INT_MTX_SEL	**Selects color matrix table** 0000: MTX_RGB_TO_JPEG 0010: MTX_RGB_TO_BT601 0011: MTX_RGB_TO_BT709 0100: MTX_JPEG_TO_RGB 0110: MTX_BT601_TO_RGB 0111: MTX_BT709_TO_RGB 1000: MTX_JPEG_TO_BT601 1001: MTX_JPEG_TO_BT709 1010: MTX_BT601_TO_JPEG 1011: MTX_BT709_TO_JPEG 1100: MTX_BT709_TO_BT601 1101: MTX_BT601_TO_BT709 Others: HW default (JPEG_TO_RGB)
15:12	**CFMT**	CLRFMT	**//--OLD define for reference only** 0000: RGB888 0001: RGB565 0010: ARGB8888 0011: PARGB8888 0100: xARGB8888 1000: YUYV 1001: UYVY 1010: YVYU 1011: VYUY 1111: YUV444 Others: Reserved color format 0000: RGB565 0001: RGB888 0010: RGBA8888/BGRA8888 0011: ARGB8888/ABGR8888 0100: UVVY, VYUY 0101: YUYV, YVYU
11	**MTXEN**	EXT_MTX_EN	**Enables external programmable coeff**

Bit(s)	Mnemonic	Name	Description
			0: Matrix coeff 1: Programmable coeff
10	**HFE**	HORIZONTAL_FLIP_EN	**Enables horizontal flip** 0: Disable horizontal flip 1: Enable horizontal flip
9	**VFE**	VERTICAL_FLIP_ EN	**Enables vertical flip** 0: Disable vertical flip 1: Enable vertical flip
8	**AEN**	ALPHA_EN	**Enables alpha blending** 0: Disable alpha blending 1: Enable alpha blending
7:0	**APHA**	ALPHA	**Constant alpha value**

1400D054 OVL_L1_SRCKEY Overlay Layer 1 Source Key 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SKEY**	SRCKEY	**Layer source color key** Active when source color key is enabled.

1400D058 OVL_L1_SRCSIZE Overlay Layer 1 Source Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L1_SRC_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L1_SRC_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**L1H**	L1_SRC_H	**Layer source height** Range: 0 ~ 8191
12:0	**L1W**	L1_SRC_W	**Layer source width** Range: 0 ~ 8191

1400D05C OVL_L1_OFFSET Overlay Layer 1 Offset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name				L1_YOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L1_XOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**L1H**	L1_YOFF	**Layer vertical Y offset** Range: 0 ~ 8191
12:0	**L1XO**	L1_XOFF	**Layer horizontal X offset** Range: 0 ~ 8191

1400DF60 OVL_L1_ADDR **Overlay Layer 1 Memory Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L1_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L1_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**L1AD**	L1_ADDR	Layer memory buffer address

1400D064 OVL_L1_PITCH **Overlay Layer 1 Pitch** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SURFL_EN	L1_BLEND_RND_SHT		L1_CONST_BLD	L1_DRGB_SEL_EXT	L1_DA_SEL_EXT	L1_SRGB_SEL_EXT	L1_SA_SEL_EXT	L1_DRGB_SEL		L1_DA_SEL		L1_SRGB_SEL		L1_SA_SEL	
Type	RW	RW		RW	RW	RW	RW	RW	RW		RW		RW		RW	
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L1_SRC_PITCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**L1SP**	SURFL_EN	**Enables layer surface dlinger alpha_blending** 0: Disable surface flinger alpha_blending 1: Enable surface flinger alpha_blending
30		L1_BLEND_RND_SHT	
28		L1_CONST_BLD	
27		L1_DRGB_SEL_EX T	**Selects layer destination_RGB alpha**

Bit(s)	Mnemonic	Name	Description
26		L1_DA_SEL_EXT	**Selects layer destination_Alpha alpha**
25		L1_SRGB_SEL_EX T	**Selects layer source_RGB alpha**
24		L1_SA_SEL_EXT	**Selects layer source_Alpha alpha**
23:22	**L1SP**	L1_DRGB_SEL	**Selects layer destination_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
21:20	**L1SP**	L1_DA_SEL	**Selects layer destination_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
19:18	**L1SP**	L1_SRGB_SEL	**Selects layer source_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
17:16	**L1SP**	L1_SA_SEL	**Selects layer source_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
15:0	**L1SP**	L1_SRC_PITCH	**Layer source pitch**

1400D068 OVL_L1_TILE **Overlay Layer 1 Tile Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TILE_HORI_BLOCK_NUM										TILE_EN	TILE_WIDTH_SEL	TILE_HEIGHT			
Type	OTHER										OTHER	OTHER	OTHER			
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TILE_HEIGHT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**TILE_BLKS**	TILE_HORI_BLOCK_NUM	**Number of horizontal blocks**
21	**TILE_EN**	TILE_EN	**Enables tile mode** 0: Disable 1: Enable
20	**TILE_W**	TILE_WIDTH_SEL	**Width of tile** 0: 16 1: 32
19:0	**TILE_H**	TILE_HEIGHT	**Height of source tile mode**

1400D06C OVL_L1_CLIP **Overlay Layer 1 Clip** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L1_SRC_BOTTOM_CLIP								L1_SRC_TOP_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L1_SRC_RIGHT_CLIP								L1_SRC_LEFT_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**L1_SRC_BOTTOM_CLIP**	L1_SRC_BOTTOM_CLIP	Layer 1 bottom clip
23:16	**L1_SRC_TOP_CLI P**	L1_SRC_TOP_CLI P	Layer 1 top clip
15:8	**L1_SRC_RIGHT_CLIP**	L1_SRC_RIGHT_C LIP	Layer 1 right clip
7:0	**L1_SRC_LEFT_CLIP**	L1_SRC_LEFT_CL IP	Layer 1 left clip

1400D088 OVL_L2_TILE Overlay Layer 2 Tile Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TILE_HORI_BLOCK_NUM										TILE_EN	TILE_WIDTH_SEL	TILE_HEIGHT			
Type	OTHER										OTHER	OTHER	OTHER			
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TILE_HEIGHT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**TILE_BLKS**	TILE_HORI_BLOCK_NUM	**Number of horizontal blocks**
21	**TILE_EN**	TILE_EN	**Enables tile mode** 0: Disable 1: Enable
20	**TILE_W**	TILE_WIDTH_SEL	**Width of tile** 0: 16 1: 32
19:0	**TILE_H**	TILE_HEIGHT	**Height of source tile mode**

1400D090 OVL_L3_CON Overlay Layer 3 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					EXT_MTX_EN											

Type					OTHER											
Reset					0											

Bit(s)	Mnemonic	Name	Description
11	**MTXEN**	EXT_MTX_EN	**Enables external programmable coeff** 0: Matrix coeff 1: Programmable coeff

1400D09C OVL_L3_OFFSET **Overlay Layer 3 Offset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L3_XOFF												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0	**L3XO**	L3_XOFF	**Layer horizontal X offset** Range: 0 ~ 8191

1400D0A8 OVL_L3_TILE **Overlay Layer 3 Tile Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TILE_HORI_BLOCK_NUM										TILE_EN	TILE_WIDTH_SEL	TILE_HEIGHT			
Type	OTHER										OTHER	OTHER	OTHER			
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TILE_HEIGHT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**TILE_BLKS**	TILE_HORI_BLOCK_NUM	**Number of horizontal blocks**
21	**TILE_EN**	TILE_EN	**Enables tile mode** 0: Disable 1: Enable
20	**TILE_W**	TILE_WIDTH_SEL	**Width of tile** 0: 16 1: 32
19:0	**TILE_H**	TILE_HEIGHT	**Height of source tile mode**

1400D0C0 OVL_RDMA0_CTRL — Overlay RDMA0 Control — 03FF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						RDMA0_FIFO_USED_SIZE										
Type						RU										
Reset						0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RDMA0_INTERLACE				RDMA0_EN
Type												OTHER				RW
Reset												0				0

Bit(s)	Mnemonic	Name	Description
26:16		RDMA0_FIFO_USED_SIZE	**Overlay RDMA0 used size**
4		RDMA0_INTERLACE	**Overlay RDMA0 interlace** 0: Disable 1: Enable
0		RDMA0_EN	**Overlay RDMA0 Enable** 0: Disable 1: Enable

1400D0C8 OVL_RDMA0_MEM_GMC_SETTING1 — Overlay RDMA0 Memory GMC Setting — 1010FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA0_PRE_ULTRA_THRESHOLD_HIGH_OFS								RDMA0_ULTRA_THRESHOLD_HIGH_OFS							
Type	OTHER								OTHER							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA0_PRE_ULTRA_THRESHOLD								RDMA0_ULTRA_THRESHOLD							
Type	OTHER								OTHER							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		RDMA0_PRE_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA0 pre_ultra threshold high offset
23:16		RDMA0_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA0 ultra threshold high offset
15:8		RDMA0_PRE_ULTRA_THRESHOLD	Overlay RDMA0 pre_ultra threshold
7:0		RDMA0_ULTRA_THRESHOLD	Overlay RDMA0 ultra threshold

1400D0CC OVL_RDMA0_MEM_SLOW_CON — Overlay RDMA0 Memory Slow Control — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RDMA0_SLOW_CNT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RDMA0_SLOW_EN
Type																OTHER
Reset																0

Bit(s)	Mnemonic	Name	Description
31:16		RDMA0_SLOW_CNT	**Overlay RDMA0 memory slow-down counter** After this SLOW_CNT, SMI will raise greq again. 10: 10 cycles between 2 greq at least 33: 33 cycles between 2 greq at least
0		RDMA0_SLOW_EN	**Enables overlay RDMA0 memory slow-down** 0: Disable slow-down 1: Enable slow-down

1400D0D0 OVL_RDMA0_FIFO_CTRL **Overlay RDMA0 FIFO Control** **00800000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA0_FIFO_UND_EN						RDMA0_FIFO_SIZE									
Type	OTHER						RW									
Reset	0						0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RDMA0_FIFO_THRD									
Type							OTHER									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		RDMA0_FIFO_UND_EN	**Overlay RDMA0 FIFO underflow control** 0: Disable FIFO underflow 1: Enable FIFO underflow
25:16		RDMA0_FIFO_SIZE	**Overlay RDMA0 FIFO size** Unit: 16 bytes 128: FIFO size is 128*128.
9:0		RDMA0_FIFO_THRD	**Overlay RDMA0 FIFO output valid threshold** Unit: 16 bytes. This value should be smaller than SRC_W*SRC_H*bpp >> 2. 0, 1: If FIFO pointer >= 1, RDMA will send data valid to OVL. 2: If FIFO pointer >= 2, RDMA will send data valid to OVL.

1400D0E0 OVL_RDMA1_CTRL **Overlay RDMA1 Control** **03FF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						RDMA 1_FI FO_U SED_ SIZE										
Type						RU										
Reset						0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RDMA 1_IN TERL ACE				RDMA 1_EN
Type												OTHER				RW
Reset												0				0

Bit(s)	Mnemonic	Name	Description
26:16		RDMA1_FIFO_USE D_SIZE	**Overlay RDMA1 used size**
4		RDMA1_INTERLAC E	**Overlay RDMA1 interlace** 0: Disable 1: Enable
0		RDMA1_EN	**Enables overlay RDMA1** 0: Disable 1: Enable

1400D0E8 OVL_RDMA1_MEM_GMC_SETTING1 **Overlay RDMA1 Memory GMC Setting** **1010FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA1_PRE_ULTRA_THRESHOLD_HIGH_OF S								RDMA1_ULTRA_THRESHOLD_HIGH_OFS							
Type	OTHER								OTHER							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA1_PRE_ULTRA_THRESHOLD								RDMA1_ULTRA_THRESHOLD							
Type	OTHER								OTHER							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		RDMA1_PRE_ULTR A_THRESHOLD_HI GH_OFS	Overlay RDMA1 pre_ultra threshold high offset
23:16		RDMA1_ULTRA_TH RESHOLD_HIGH_O FS	Overlay RDMA1 ultra threshold high offset
15:8		RDMA1_PRE_ULTR A_THRESHOLD	Overlay RDMA1 pre_ultra threshold
7:0		RDMA1_ULTRA_TH RESHOLD	Overlay RDMA1 ultra threshold

1400D0EC OVL_RDMA1_MEM_SLOW_CON **Overlay RDMA1 Memory Slow Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA 1_SL OW_C NT															
Type	OTHER															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RDMA1_SLOW_EN
Type																OTHER
Reset																0

Bit(s)	Mnemonic	Name	Description
31:16		RDMA1_SLOW_CNT	**Overlay RDMA1 memory slow-down counter** After this SLOW_CNT, SMI will raise greq again. 10: 10 cycles between 2 greq at least 33: 33 cycles between 2 greq at least
0		RDMA1_SLOW_EN	**Enables overlay RDMA1 memory slow-down** 0: Disable slow-down 1: Enable slow-down

1400D0F0 OVL_RDMA1_FIFO_CTRL **Overlay RDMA1 FIFO Control** **00800000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA1_FIFO_UND_EN						RDMA1_FIFO_SIZE									
Type	OTHER						RW									
Reset	0						0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RDMA1_FIFO_THRD									
Type							OTHER									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		RDMA1_FIFO_UND_EN	**Overlay RDMA1 FIFO underflow control** 0: Disable FIFO underflow 1: Enable FIFO underflow
25:16		RDMA1_FIFO_SIZE	**Overlay RDMA1 FIFO size** Unit: 16 bytes 128: FIFO size is 128*128.
9:0		RDMA1_FIFO_THRD	**Overlay RDMA1 FIFO output valid threshold** Unit: 16 bytes. This value should be smaller than SRC_W*SRC_H*bpp >> 2. 0, 1: If FIFO pointer >= 1, RDMA will send data valid to OVL. 2: If FIFO pointer >= 2, RDMA will send data valid to OVL.

1400D108 OVL_RDMA2_MEM_GMC_SETTING1 **Overlay RDMA2 Memory GMC Setting** **10100000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA2_PRE_ULTRA_THRESHOLD_HIGH								RDMA2_ULTRA_THRESHOLD_HIGH_OFS							

	GH_O FS															
Type	OTHER								OTHER							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
31:24		RDMA2_PRE_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA2 pre_ultra threshold high offset
23:16		RDMA2_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA2 ultra threshold high offset

1400D10C OVL_RDMA2_MEM_SLOW_CON **Overlay RDMA2 Memory Slow Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA2_SLOW_CNT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RDMA2_SLOW_EN
Type																OTHER
Reset																0

Bit(s)	Mnemonic	Name	Description
31:16		RDMA2_SLOW_CNT	**Overlay RDMA2 memory slow-down counter** After this SLOW_CNT, SMI will raise greq again. 10: 10 cycles between 2 greq at least 33: 33 cycles between 2 greq at least
0		RDMA2_SLOW_EN	**Enables overlay RDMA2 memory slow-down** 0: Disable slow-down 1: Enable slow-down

1400D110 OVL_RDMA2_FIFO_CTRL **Overlay RDMA2 FIFO Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA2_FIFO_UND_EN															
Type	OTHER															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RDMA2_FIFO_THRD									

Type							OTHER									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		RDMA2_FIFO_UND _EN	**Overlay RDMA2 FIFO underflow control** 0: Disable FIFO underflow 1: Enable FIFO underflow
9:0		RDMA2_FIFO_THR D	**Overlay RDMA2 FIFO output valid threshold** Unit: 16 bytes. This value should be smaller than SRC_W*SRC_H*bpp >> 2. 0, 1: If FIFO pointer >= 1, RDMA will send data valid to OVL. 2: If FIFO pointer >= 2, RDMA will send data valid to OVL.

1400D120 OVL_RDMA3_CTRL **Overlay RDMA3 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RDMA3_INTERLACE				
Type												OTHER				
Reset												0				

Bit(s)	Mnemonic	Name	Description
4		RDMA3_INTERLAC E	**Overlay RDMA3 interlace** 0: Disable 1: Enable

1400D128 OVL_RDMA3_MEM_GMC_SETTING1 **Overlay RDMA3 Memory GMC Setting** **10100000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA3_PRE_ULTRA_THRESHOLD_HIGH_OFS								RDMA3_ULTRA_THRESHOLD_HIGH_OFS							
Type	OTHER								OTHER							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
31:24		RDMA3_PRE_ULTR A_THRESHOLD_HI GH_OFS	Overlay RDMA3 pre_ultra threshold high offset

Bit(s)	Mnemonic	Name	Description
23:16		RDMA3_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA3 ultra threshold high offset

1400D12C OVL_RDMA3_MEM_SLOW_CON **Overlay RDMA3 Memory Slow Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA3_SLOW_CNT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RDMA3_SLOW_EN
Type																OTHER
Reset																0

Bit(s)	Mnemonic	Name	Description
31:16		RDMA3_SLOW_CNT	**Overlay RDMA3 memory slow-down counter** After this SLOW_CNT, SMI will raise greq again. 10: 10 cycles between 2 greq at least 33: 33 cycles between 2 greq at least
0		RDMA3_SLOW_EN	**Enables overlay RDMA3 memory slow-down** 0: Disable slow-down 1: Enable slow-down

1400D130 OVL_RDMA3_FIFO_CTRL **Overlay RDMA3 FIFO Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA3_FIFO_UND_EN						RDMA3_FIFO_SIZE									
Type	OTHER						RO									
Reset	0						0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RDMA3_FIFO_THRD									
Type							OTHER									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		RDMA3_FIFO_UND_EN	**Overlay RDMA3 FIFO underflow control** 0: Disable FIFO underflow 1: Enable FIFO underflow
25:16		RDMA3_FIFO_SIZE	**Overlay RDMA3 FIFO size** Unit: 16 bytes 128: FIFO size is 128*128.
9:0		RDMA3_FIFO_THRD	**Overlay RDMA3 FIFO output valid threshold** Unit: 16 bytes. This value should be smaller than

Bit(s)	Mnemonic	Name	Description
			SRC_W*SRC_H*bpp >> 2. 0, 1: If FIFO pointer >= 1, RDMA will send data valid to OVL. 2: If FIFO pointer >= 2, RDMA will send data valid to OVL.

1400D134 OVL_L0_Y2R_PARA_R0 Overlay L0 Y2R Conversion Parameter R0 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_RMU												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_RMU	Overlay L0 YUV2RGB program parameter for R color of U component
12:0		C_CF_RMY	Overlay L0 YUV2RGB program parameter for R color of Y component

1400D138 OVL_L0_Y2R_PARA_R1 Overlay L0 Y2R Conversion Parameter R1 0000057C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMV												
Type				OTHER												
Reset				0	0	1	0	1	0	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_RMV	Overlay L0 YUV2RGB program parameter for R color of V component

1400D13C OVL_L0_Y2R_PARA_G0 Overlay L0 Y2R Conversion Parameter G0 1EA80400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_GMU												
Type				OTHER												
Reset				1	1	1	1	0	1	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMY												

Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_GMU	Overlay Lo YUV2RGB program parameter for G color of U component
12:0		C_CF_GMY	Overlay Lo YUV2RGB program parameter for G color of Y component

1400D140 OVL_Lo_Y2R_PARA_G1 — Overlay Lo Y2R Conversion Parameter G1 — 00001D35

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMV												
Type				OTHER												
Reset				1	1	1	0	1	0	0	1	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_GMV	Overlay Lo YUV2RGB program parameter for G color of V component

1400D144 OVL_Lo_Y2R_PARA_B0 — Overlay Lo Y2R Conversion Parameter B0 — 06EE0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_BMU												
Type				OTHER												
Reset				0	0	1	1	0	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_BMU	Overlay Lo YUV2RGB program parameter for B color of U component
12:0		C_CF_BMY	Overlay Lo YUV2RGB program parameter for B color of Y component

1400D148 OVL_Lo_Y2R_PARA_B1 — Overlay Lo Y2R Conversion Parameter B1 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMV												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_BMV	Overlay L0 YUV2RGB program parameter for B color of V component

1400D14C OVL_L0_Y2R_PARA_YUV_A_0 Overlay L0 Y2R Conversion Parameter Extended Add on YUV 0 01800000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_UA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_YA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_UA	Overlay L0 YUV2RGB program parameter for U to add extended offset
8:0		C_CF_YA	Overlay L0 YUV2RGB program parameter for Y to add extended offset

1400D150 OVL_L0_Y2R_PARA_YUV_A_1 Overlay L0 Y2R Conversion Parameter Extended Add on YUV 1 00000180

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_VA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_VA	Overlay L0 YUV2RGB program parameter for V to add extended offset

1400D154 OVL_L0_Y2R_PARA_RGB_A_0 Overlay L0 Y2R Conversion Parameter Extended Add on RGB 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name								C_CF_GA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_RA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_GA	Overlay L0 YUV2RGB program parameter for G to add extended offset
8:0		C_CF_RA	Overlay L0 YUV2RGB program parameter for R to add extended offset

1400D158 OVL_L0_Y2R_PARA_RGBA_1 **Overlay L0 Y2R Conversion Parameter Extended Add on RGB 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_BA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_BA	Overlay L0 YUV2RGB program parameter for B to add extended offset

1400D15C OVL_L1_Y2R_PARA_R0 **Overlay L1 Y2R Conversion Parameter R0** **00000400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_RMU												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_RMU	Overlay L1 YUV2RGB program parameter for R color of U component
12:0		C_CF_RMY	Overlay L1 YUV2RGB program parameter for R color of Y component

1400D160 OVL_L1_Y2R_PARA_R1 **Overlay L1 Y2R Conversion Parameter R1** **0000057C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMV												
Type				OTHER												
Reset				0	0	1	0	1	0	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_RMV	Overlay L1 YUV2RGB program parameter for R color of V component

1400D164 OVL_L1_Y2R_PARA_G0 **Overlay L1 Y2R Conversion Parameter G0** **1EA80400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_GMU												
Type				OTHER												
Reset				1	1	1	1	0	1	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_GMU	Overlay L1 YUV2RGB program parameter for G color of U component
12:0		C_CF_GMY	Overlay L1 YUV2RGB program parameter for G color of Y component

1400D168 OVL_L1_Y2R_PARA_G1 **Overlay L1 Y2R Conversion Parameter G1** **00001D35**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMV												
Type				OTHER												
Reset				1	1	1	0	1	0	0	1	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_GMV	Overlay L1 YUV2RGB program parameter for G color of V component

1400D16C OVL_L1_Y2R_PARA_B0 **Overlay L1 Y2R Conversion Parameter B0** **06EE0400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_BMU												
Type				OTHER												
Reset				0	0	1	1	0	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_BMU	Overlay L1 YUV2RGB program parameter for B color of U component
12:0		C_CF_BMY	Overlay L1 YUV2RGB program parameter for B color of Y component

1400D170 OVL_L1_Y2R_PARA_B1 **Overlay L1 Y2R Conversion Parameter B1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMV												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_BMV	Overlay L1 YUV2RGB program parameter for B color of V component

1400D174 OVL_L1_Y2R_PARA_YUV_A_0 **Overlay L1 Y2R Conversion Parameter Extended Add on YUV 0** **01800000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_UA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_YA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_UA	Overlay L1 YUV2RGB program parameter for U to add extended offset
8:0		C_CF_YA	Overlay L1 YUV2RGB program parameter for Y to add

Bit(s)	Mnemonic	Name	Description
			extended offset

1400D178 OVL_L1_Y2R_PARA_YUVA_1 **Overlay L1 Y2R Conversion Parameter Extended Add on YUV 1** **00000180**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_VA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_VA	Overlay L1 YUV2RGB program parameter for V to add extended offset

1400D17C OVL_L1_Y2R_PARA_RGBA_0 **Overlay L1 Y2R Conversion Parameter Extended Add on RGB 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_GA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_RA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_GA	Overlay L1 YUV2RGB program parameter for G to add extended offset
8:0		C_CF_RA	Overlay L1 YUV2RGB program parameter for R to add extended offset

1400D180 OVL_L1_Y2R_PARA_RGBA_1 **Overlay L1 Y2R Conversion Parameter Extended Add on RGB 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_BA								
Type								OTHER								

Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_BA	Overlay L1 YUV2RGB program parameter for B to add extended offset

1400D184 OVL_L2_Y2R_PARA_R0 Overlay L2 Y2R Conversion Parameter R0 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_RMU												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_RMU	Overlay L2 YUV2RGB program parameter for R color of U component
12:0		C_CF_RMY	Overlay L2 YUV2RGB program parameter for R color of Y component

1400D188 OVL_L2_Y2R_PARA_R1 Overlay L2 Y2R Conversion Parameter R1 0000057C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMV												
Type				OTHER												
Reset				0	0	1	0	1	0	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_RMV	Overlay L2 YUV2RGB program parameter for R color of V component

1400D18C OVL_L2_Y2R_PARA_G0 Overlay L2 Y2R Conversion Parameter G0 1EA80400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_GMU												
Type				OTHER												
Reset				1	1	1	1	0	1	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMY												

Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_GMU	Overlay L2 YUV2RGB program parameter for G color of U component
12:0		C_CF_GMY	Overlay L2 YUV2RGB program parameter for G color of Y component

1400D190 OVL_L2_Y2R_PARA_G1 **Overlay L2 Y2R Conversion Parameter G1** **00001D35**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMV												
Type				OTHER												
Reset				1	1	1	0	1	0	0	1	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_GMV	Overlay L2 YUV2RGB program parameter for G color of V component

1400D194 OVL_L2_Y2R_PARA_B0 **Overlay L2 Y2R Conversion Parameter B0** **06EE0400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_BMU												
Type				OTHER												
Reset				0	0	1	1	0	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_BMU	Overlay L2 YUV2RGB program parameter for B color of U component
12:0		C_CF_BMY	Overlay L2 YUV2RGB program parameter for B color of Y component

1400D198 OVL_L2_Y2R_PARA_B1 **Overlay L2 Y2R Conversion Parameter B1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMV												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_BMV	Overlay L2 YUV2RGB program parameter for B color of V component

1400D19C OVL_L2_Y2R_PARA_YUV_A_0 Overlay L2 Y2R Conversion Parameter Extended Add on YUV 0 01800000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_UA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_YA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_UA	Overlay L2 YUV2RGB program parameter for U to add extended offset
8:0		C_CF_YA	Overlay L2 YUV2RGB program parameter for Y to add extended offset

1400D1A0 OVL_L2_Y2R_PARA_YUV_A_1 Overlay L2 Y2R Conversion Parameter Extended Add on YUV 1 00000180

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_VA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_VA	Overlay L2 YUV2RGB program parameter for V to add extended offset

1400D1A4 OVL_L2_Y2R_PARA_RGB_A_0 Overlay L2 Y2R Conversion Parameter Extended Add on RGB 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_GA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_RA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_GA	Overlay L2 YUV2RGB program parameter for G to add extended offset
8:0		C_CF_RA	Overlay L2 YUV2RGB program parameter for R to add extended offset

1400D1A8 OVL_L2_Y2R_PARA_RGBA_1 — **Overlay L2 Y2R Conversion Parameter Extended Add on RGB 1** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_BA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_BA	Overlay L2 YUV2RGB program parameter for B to add extended offset

1400D1AC OVL_L3_Y2R_PARA_R0 — **Overlay L3 Y2R Conversion Parameter R0** — **00000400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_RMU												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_RMU	Overlay L3 YUV2RGB program parameter for R color of U component
12:0		C_CF_RMY	Overlay L3 YUV2RGB program parameter for R color of Y component

1400D1B0 OVL_L3_Y2R_PARA_R1 **Overlay L3 Y2R Conversion Parameter R1** **0000057C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMV												
Type				OTHER												
Reset				0	0	1	0	1	0	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_RMV	Overlay L3 YUV2RGB program parameter for R color of V component

1400D1B4 OVL_L3_Y2R_PARA_G0 **Overlay L3 Y2R Conversion Parameter G0** **1EA80400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_GMU												
Type				OTHER												
Reset				1	1	1	1	0	1	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_GMU	Overlay L3 YUV2RGB program parameter for G color of U component
12:0		C_CF_GMY	Overlay L3 YUV2RGB program parameter for G color of Y component

1400D1B8 OVL_L3_Y2R_PARA_G1 **Overlay L3 Y2R Conversion Parameter G1** **00001D35**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMV												
Type				OTHER												
Reset				1	1	1	0	1	0	0	1	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_GMV	Overlay L3 YUV2RGB program parameter for G color of V component

1400D1BC OVL_L3_Y2R_PARA_B0 **Overlay L3 Y2R Conversion Parameter B0** **06EE0400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_BMU												
Type				OTHER												
Reset				0	0	1	1	0	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_BMU	Overlay L3 YUV2RGB program parameter for B color of U component
12:0		C_CF_BMY	Overlay L3 YUV2RGB program parameter for B color of Y component

1400D1C0 OVL_L3_Y2R_PARA_B1 **Overlay L3 Y2R Conversion Parameter B1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMV												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_BMV	Overlay L3 YUV2RGB program parameter for B color of V component

1400D1C4 OVL_L3_Y2R_PARA_YUVA_0 **Overlay L3 Y2R Conversion Parameter Extended Add on YUV 0** **01800000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_UA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_YA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_UA	Overlay L3 YUV2RGB program parameter for U to add extended offset

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_YA	Overlay L3 YUV2RGB program parameter for Y to add extended offset

1400D1C8 OVL_L3_Y2R_PARA_YUVA_1 **Overlay L3 Y2R Conversion Parameter Extended Add on YUV 1** **00000180**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_VA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_VA	Overlay L3 YUV2RGB program parameter for V to add extended offset

1400D1CC OVL_L3_Y2R_PARA_RGBA_0 **Overlay L3 Y2R Conversion Parameter Extended Add on RGB 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_GA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_RA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_GA	Overlay L3 YUV2RGB program parameter for G to add extended offset
8:0		C_CF_RA	Overlay L3 YUV2RGB program parameter for R to add extended offset

1400D1D0 OVL_L3_Y2R_PARA_RGBA_1 **Overlay L3 Y2R Conversion Parameter Extended Add on RGB 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_BA								

Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_BA	Overlay L3 YUV2RGB program parameter for B to add extended offset

1400D1D4 OVL_DEBUG_MON_SEL **Overlay Debug Monitor Select** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DBG_MON_SEL			
Type													WO			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0		DBG_MON_SEL	Overlay Debug Monitor Select

1400D1E0 OVL_RDMA0_MEM_GMC_SETTING2 **Overlay RDMA0 Memory GMC Setting** **205F00BF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RDMA0_FORCE_REQ_THRESHOLD	RDMA0_REQ_THRESHOLD_ULTRA	RDMA0_REQ_THRESHOLD_PREULTRA		RDMA0_ISSUE_REQ_THRESHOLD_URG										
Type		RW	RW	RW		RW										
Reset		0	1	0		0	0	0	0	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RDMA0_ISSUE_REQ_THRESHOLD										
Type						RW										
Reset						0	0	0	1	0	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30		RDMA0_FORCE_REQ_THRESHOLD	
29		RDMA0_REQ_THRESHOLD_ULTRA	
28		RDMA0_REQ_THRESHOLD_PREULTRA	
26:16		RDMA0_ISSUE_REQ_THRESHOLD_URG	
10:0		RDMA0_ISSUE_REQ_THRESHOLD	Overlay RDMA0 issue request threshold (0 for best performance)

Bit(s)	Mnemonic	Name	Description

1400D1E4 OVL_RDMA1_MEM_GMC_SETTING2 — **Overlay RDMA1 Memory GMC Setting** — **205F00BF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RDMA1_FORCE_REQ_THRESHOLD	RDMA1_REQ_THRESHOLD_ULTRA	RDMA1_REQ_THRESHOLD_PREULTRA		RDMA1_ISSUE_REQ_THRESHOLD_URG										
Type		RW	RW	RW		RW										
Reset		0	1	0		0	0	0	0	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RDMA1_ISSUE_REQ_THRESHOLD										
Type						RW										
Reset						0	0	0	1	0	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30		RDMA1_FORCE_REQ_THRESHOLD	
29		RDMA1_REQ_THRESHOLD_ULTRA	
28		RDMA1_REQ_THRESHOLD_PREULTRA	
26:16		RDMA1_ISSUE_REQ_THRESHOLD_URG	
10:0		RDMA1_ISSUE_REQ_THRESHOLD	Overlay RDMA1 issue request threshold (0 for best performance)

1400D1F0 OVL_RDMA_BURST_CON0 — **Overlay RDMA Burst Control** — **07775533**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				BURST_128B_BOUND		BURST15A_32B				BURST14A_32B				BURST13A_32B		
Type				RW		RW				RW				RW		
Reset				0		1	1	1		1	1	1		1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		BURST12A_32B				BURST11A_32B				BURST10A_32B				BURST9A_32B		
Type		RW				RW				RW				RW		
Reset		1	0	1		1	0	1		0	1	1		0	1	1

Bit(s)	Mnemonic	Name	Description
28		BURST_128B_BOUND	
26:24		BURST15A_32B	First burst slice for a 32B aligned burst of length 15
22:20		BURST14A_32B	First burst slice for a 32B aligned burst of length 14
18:16		BURST13A_32B	First burst slice for a 32B aligned burst of length 13
14:12		BURST12A_32B	First burst slice for a 32B aligned burst of length 12

Bit(s)	Mnemonic	Name	Description
10:8		BURST11A_32B	First burst slice for a 32B aligned burst of length 11
6:4		BURST10A_32B	First burst slice for a 32B aligned burst of length 10
2:0		BURST9A_32B	First burst slice for a 32B aligned burst of length 9

1400D1F4 OVL_RDMA_BURST_CON1 Overlay RDMA Burst Control 06666442

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						BURST15A_N32B				BURST14A_N32B				BURST13A_N32B		
Type						RW				RW				RW		
Reset						1	1	0		1	1	0		1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		BURST12A_N32B				BURST11A_N32B				BURST10A_N32B				BURST9A_N32B		
Type		RW				RW				RW				RW		
Reset		1	1	0		1	0	0		1	0	0		0	1	0

Bit(s)	Mnemonic	Name	Description
26:24		BURST15A_N32B	First burst slice for a non-32B aligned burst of length 15
22:20		BURST14A_N32B	First burst slice for a non-32B aligned burst of length 14
18:16		BURST13A_N32B	First burst slice for a non-32B aligned burst of length 13
14:12		BURST12A_N32B	First burst slice for a non-32B aligned burst of length 12
10:8		BURST11A_N32B	First burst slice for a non-32B aligned burst of length 11
6:4		BURST10A_N32B	First burst slice for a non-32B aligned burst of length 10
2:0		BURST9A_N32B	First burst slice for a non-32B aligned burst of length 9

1400D1F8 OVL_RDMA_GREQ_NUM Overlay RDMA GREQ Number 510F00BB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IOBUF_FLUSH_ULTRA	IOBUF_FLUSH_PREULTRA		GRP_BRK_STOP	GREQ_STOP_EN	GREQ_DIS_CNT			OSTD_GREQ_NUM							
Type	RW	RW		RW	RW	RW			RW							
Reset	0	1		1	0	0	0	1	0	0	0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LAYER1_GREQ_NUM				LAYER0_GREQ_NUM			
Type									RW				RW			
Reset									1	0	1	1	1	0	1	1

Bit(s)	Mnemonic	Name	Description
31		IOBUF_FLUSH_ULTRA	
30		IOBUF_FLUSH_PREULTRA	
28		GRP_BRK_STOP	**Stop GREQ when group breaks**
27		GREQ_STOP_EN	**Stop each GREQ after GLCOMD**
26:24		GREQ_DIS_CNT	
23:16		OSTD_GREQ_NUM	
7:4	LAYER1_GREQ_NU	LAYER1_GREQ_NU M	**OVL Layer 1 multi-greq number**

Bit(s)	Mnemonic	Name	Description
	M		Max.: 7
3:0	LAYERo_GREQ_NUM	LAYERo_GREQ_NU M	**OVL Layer o multi-greq number**
	M		Max.: 7

1400D1FC OVL_RDMA_GREQ_URG_NUM — Overlay RDMA GREQ Number — 20300055

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GREQ_NUM_SHT		GREQ_NUM_SHT_VAL	ARG_URG_BIAS			ARG_GREQ_URG_TH									
Type	RW		RW	RW			RW									
Reset	0	0	1	0			0	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LAYER1_GREQ_URG_NUM				LAYERo_GREQ_URG_NUM			
Type									RW				RW			
Reset									0	1	0	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
31:30		GREQ_NUM_SHT	
29		GREQ_NUM_SHT_V AL	
28		ARG_URG_BIAS	
25:16		ARG_GREQ_URG_T H	
7:4		LAYER1_GREQ_UR G_NUM	**OVL Layer 1 multi-greq number** Max.: 7
3:0		LAYERo_GREQ_UR G_NUM	**OVL Layer o multi-greq number** Max.: 7 (GREQ_URG_NUM <= GREQ_NUM)

1400D200 OVL_DUMMY_REG — Overlay Dummy Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OVERLAY_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OVERLAY_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		OVERLAY_DUMMY	Overlay dummy register

1400D208 OVL_GDRDY_PRD — Overlay SMI GDRDY Period — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name									GDRDY_PRD							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDRDY_PRD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		GDRDY_PRD	

1400D20C OVL_RDMA_ULTRA_SRC **Overlay RDMA Ultra SRC** **0000A050**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ULTRA_RDMA_SRC		ULTRA_ROI_END_SRC		ULTRA_SMI_SRC		ULTRA_BUF_SRC		PREULTRA_RDMA_SRC		PREULTRA_ROI_END_SRC		PREULTRA_SMI_SRC		PREULTRA_BUF_SRC	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	1	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:14		ULTRA_RDMA_SRC	
13:12		ULTRA_ROI_END_SRC	
11:10		ULTRA_SMI_SRC	
9:8		ULTRA_BUF_SRC	
7:6		PREULTRA_RDMA_SRC	
5:4		PREULTRA_ROI_END_SRC	
3:2		PREULTRA_SMI_SRC	
1:0		PREULTRA_BUF_SRC	

1400D210 OVL_RDMA0_BUF_LOW **Overlay RDMA BUF Low** **00030020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											BUF_LOW_PREULTRA_TH					
Type											RW					
Reset											0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF_LOW_PREULTRA_TH						BUF_LOW_ULTRA_TH									
Type	RW						RW									
Reset	0	0	0	0			0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:12		BUF_LOW_PREULTRA_TH	
9:0		BUF_LOW_ULTRA_TH	

1400D214 OVL_RDMA1_BUF_LOW **Overlay RDMA BUF Low** **00030020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											BUF_LOW_PREULTRA_TH					
Type											RW					
Reset											0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF_LOW_PREULTRA_TH						BUF_LOW_ULTRA_TH									
Type	RW						RW									
Reset	0	0	0	0			0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:12		BUF_LOW_PREULTRA_TH	
9:0		BUF_LOW_ULTRA_TH	

1400D230 OVL_SMI_DBG **Overlay SMI Arbiter Debug Monitor** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SMI_FSM									
Type							RU									
Reset							0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
9:0		SMI_FSM	Overlay SMI arbiter FSM state

1400D234 OVL_GREQ_LAYER_CNT **Overlay Layer GREQ Counter** **00000101**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			LAYER1_GREQ_CNT								LAYER0_GREQ_CNT					
Type			RU								RU					
Reset			0	0	0	0	0	1			0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
13:8		LAYER1_GREQ_CNT	RDMA Layer 1 greq counter
5:0		LAYER0_GREQ_CNT	RDMA Layer 0 greq counter

1400D238 OVL_GDRDY_PRD_NUM **Overlay SMI GDRDY Period Number** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									GDRDY_PRD_NUM							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDRDY_PRD_NUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		GDRDY_PRD_NUM	

1400D240 OVL_FLOW_CTRL_DBG **Overlay Flow Control Debug Monitor** **000CBC01**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OVL_UPD_REG	REG_UPDATE	OVL_CLR	OVL_START	OVL_RUNNING	FRAME_DONE	FRAME_UNDERRUN	FRAME_SWRST_DONE	FRAME_HWRST_DONE		TRIG	RST	RDMA0_IDLE	RDMA1_IDLE		
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU		RU	RU	RU	RU		
Reset	0	0	0	0	0	0	0	0	0		0	0	1	1		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OUT_IDLE		OVL_OUT_READY	OVL_OUT_VALID	BLEND_IDLE	ADDCON_IDLE	FSM_STATE									
Type	RU		RU	RU	RU	RU	RU									
Reset	1		1	1	1	1	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31		OVL_UPD_REG	**Overlay prepare to update register**
30		REG_UPDATE	**Updates overlay register**
29		OVL_CLR	**Clears overlay**
28		OVL_START	**Starts overlay**
27		OVL_RUNNING	**Overlay running**
26		FRAME_DONE	**Overlay frame complete**
25		FRAME_UNDERRUN	**Overlay frame underrun**
24		FRAME_SWRST_DONE	**Overlay frame reset done**
23		FRAME_HWRST_DONE	**Overlay EOF reset done**
21		TRIG	**Triggers overlay**
20		RST	**Resets overlay**
19		RDMA0_IDLE	**Overlay RDMA0 idle state**

Bit(s)	Mnemonic	Name	Description
18		RDMA1_IDLE	**Overlay RDMA1 idle state**
15		OUT_IDLE	**Overlay output relay idle state**
13		OVL_OUT_READY	**Overlay out_ready**
12		OVL_OUT_VALID	**Overlay out_valid**
11		BLEND_IDLE	**Overlay alpha blending idle state**
10		ADDCON_IDLE	**Overlay addcon idle state**
9:0		FSM_STATE	**Overlay flow control FSM state** 0x1: IDLE 0x2: WAIT 0x4: PREPARE 0x8: UPD_REG 0x10: ENG_CLR 0x20: ENG_ACT 0x40: H_WAIT_W_RST 0x80: S_WAIT_W_RST 0x100: H_W_RST 0x200: S_W_RST

1400D244 OVL_ADDCON_DBG **Overlay Address Control Debug** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				ROI_Y												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L1_WIN_HIT	L0_WIN_HIT		ROI_X												
Type	RU	RU		RU												
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		ROI_Y	Overlay pixel process vertical Y position
15		L1_WIN_HIT	Overlay Layer 1 pixel hit
14		L0_WIN_HIT	Overlay Layer 0 pixel hit
12:0		ROI_X	Overlay pixel process horizontal X position

1400D24C OVL_RDMA0_DBG **Overlay RDMA0 Debug Monitor** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMI_GREQ	RDMA0_SMI_BUSY	RDMA0_OUT_VALID	RDMA0_OUT_READY	RDMA0_OUT_DATA											
Type	RU	RU	RU	RU	RU											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA0_OUT_DATA												RDMA0_LAYER_GREQ	RDMA0_WRAM_RST_CS		

Type	RU												RU	RU		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31		SMI_GREQ	Overlay 4-to-1 SMI request
30		RDMA0_SMI_BUSY	Overlay RDMA0 SMI busy
29		RDMA0_OUT_VALI D	Overlay RDMA0 output valid
28		RDMA0_OUT_READ Y	Overlay RDMA0 output ready
27:4		RDMA0_OUT_DATA	Overlay RDMA0 output data
3		RDMA0_LAYER_GR EQ	Overlay RDMA0 SMI request
2:0		RDMA0_WRAM_RST _CS	Overlay RDMA0 warm reset current state

1400D250 OVL_RDMA1_DBG — Overlay RDMA1 Debug Monitor — 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMI_GREQ	RDMA1_SMI_BUSY	RDMA1_OUT_VALID	RDMA1_OUT_READY	RDMA1_OUT_DATA											
Type	RU	RU	RU	RU	RU											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA1_OUT_DATA												RDMA1_LAYER_GREQ	RDMA1_WRAM_RST_CS		
Type	RU												RU	RU		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31		SMI_GREQ	Overlay 4-to-1 SMI request
30		RDMA1_SMI_BUSY	Overlay RDMA1 SMI busy
29		RDMA1_OUT_VALI D	Overlay RDMA1 output valid
28		RDMA1_OUT_READ Y	Overlay RDMA1 output ready
27:4		RDMA1_OUT_DATA	Overlay RDMA1 output data
3		RDMA1_LAYER_GR EQ	Overlay RDMA1 SMI request
2:0		RDMA1_WRAM_RST _CS	Overlay RDMA1 warm reset current state

1400D25C OVL_L0_CLR — Overlay Layer 0 Constant Color — FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
31:24		ALPHA	Alpha component of Lo constant color
23:16		RED	Red component of Lo constant color
15:8		GREEN	Green component of Lo constant color
7:0		BLUE	Blue component of Lo constant color

1400D260 OVL_L1_CLR **Overlay Layer 1 Constant Color** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		ALPHA	Alpha component of L1 constant color
23:16		RED	Red component of L1 constant color
15:8		GREEN	Green component of L1 constant color
7:0		BLUE	Blue component of L1 constant color

1400D26C OVL_LC_CLR **Overlay Constant Layer Color** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		ALPHA	Alpha component of constant layer color
23:16		RED	Red component of constant layer color
15:8		GREEN	Green component of constant layer color
7:0		BLUE	Blue component of constant layer color

1400D270 OVL_CRC **Overlay CRC** **7FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRC_RDY	CRC_OUT														
Type	RU	RU														
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRC_OUT															
Type	RU															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31		CRC_RDY	
30:0		CRC_OUT	

1400D280 OVL_LC_CON **Overlay Constant Layer Control** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSTKEY_EN	SRCKEY_EN	LAYER_SRC							R_FIRST	LANDSCAPE	EN_3D				
Type	RW	RW	RW							RW	RW	RW				
Reset	0	0	0	0						0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								ALPHA_EN	ALPHA							
Type								RW	RW							
Reset								0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**DKEN**	DSTKEY_EN	**Enables destination color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable destination color key 1: Enable destination color key
30	**SKEN**	SRCKEY_EN	**Enables source color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable source color key 1: Enable source color key
29:28	**LSRC**	LAYER_SRC	**Selects layer pixel from memory/constant color/SCL/PQ** 00: Layer pixel from constant color 01: Layer pixel from constant color 10: Layer pixel from UFOd 11: Layer pixel from PQ
22		R_FIRST	**Right eye image first when in 3D mode** 0: Show left eye image first in 3D mode 1: Show right eye image first in 3D mode
21		LANDSCAPE	**Enables 3D landscape mode** 0: 3D portrait mode 1: 3D landscape mode
20		EN_3D	**Enables 3D mode** 0: 2D mode 1: 3D mode
8	**AEN**	ALPHA_EN	**Enables alpha blending** 0: Disable alpha blending 1: Enable alpha blending
7:0	**APHA**	ALPHA	**Constant alpha value**

1400D284 OVL_LC_SRCKEY **Overlay Constant Layer Source Key** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SKEY**	SRCKEY	**Layer source color key** Active when source color key is enabled.

1400D288 OVL_LC_SRC_SIZE Overlay Layer C Source Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LC_SRC_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				LC_SRC_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**LCH**	LC_SRC_H	**Layer source height** Range: 0 ~ 4095
12:0	**LCW**	LC_SRC_W	**Layer source width** Range: 0 ~ 4095

1400D28C OVL_LC_OFFSET Overlay Layer C Offset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LC_YOFF											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					LC_XOFF											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**LCH**	LC_YOFF	**Layer vertical Y offset** Range: 0 ~ 4095
11:0	**LCXO**	LC_XOFF	**Layer horizontal X offset** Range: 0 ~ 4095

1400D290 OVL_LC_SRC_SEL Overlay Constant Layer Source Selection 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	SURFL_EN	LC_BLEND_RND_SHT		LC_CONST_BLD	LC_DRGB_SEL_EXT	LC_DA_SEL_EXT	LC_SRGB_SEL_EXT	LC_SA_SEL_EXT	LC_D RGB_SEL		LC_D A_SEL		LC_S RGB_SEL		LC_SA_SEL	
Type	RW	RW		RW	RW	RW	RW	RW	RW		RW		RW		RW	
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CONST_LAYER_SEL		
Type														RW		
Reset														1	0	0

Bit(s)	Mnemonic	Name	Description
31	**LCSP**	SURFL_EN	**Enables layer surface dlinger alpha_blending** 0: Disable surface flinger alpha_blending 1: Enable surface flinger alpha_blending
30		LC_BLEND_RND_SHT	
28		LC_CONST_BLD	
27		LC_DRGB_SEL_EXT	**Selects layer destination_RGB alpha**
26		LC_DA_SEL_EXT	**Selects layer destination_Alpha alpha**
25		LC_SRGB_SEL_EXT	**Selects layer source_RGB alpha**
24		LC_SA_SEL_EXT	**Selects layer source_Alpha alpha**
23:22	**LCSP**	LC_DRGB_SEL	**Selects layer destination_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
21:20	**LCSP**	LC_DA_SEL	**Selects layer destination_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
19:18	**LCSP**	LC_SRGB_SEL	**Selects layer source_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
17:16	**LCSP**	LC_SA_SEL	**Selects layer source_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
2:0	**LCSP**	CONST_LAYER_SEL	**Layer source pitch**

1400D29C OVL_BANK_CON **Overlay Bank Control** **00000008**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												OVL_BANK_CON				
Type												RW				

Reset												0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		OVL_BANK_CON	

1400DFC0 OVL_SECURE Overlay Layer Secure Bit 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															L1_SECURE	L0_SECURE
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1		L1_SECURE	Layer 1 secure bit
0		L0_SECURE	Layer 0 secure bit

Module name: DISP_OVL1_2L Base address: (+1400e000h)

Address	Name	Width	Register Function
1400E000	OVL_STA	32	Overlay Status Monitor
1400E004	OVL_INTEN	32	Overlay Interrupt Enable
1400E008	OVL_INTSTA	32	Overlay Interrupt Status
1400E00C	OVL_EN	32	Overlay Enable
1400E010	OVL_TRIG	32	Overlay Trigger
1400E014	OVL_RST	32	Overlay Reset
1400E020	OVL_ROI_SIZE	32	Overlay ROI Size
1400E024	OVL_DATAPATH_CON	32	Overlay Datapath Control
1400E028	OVL_ROI_BGCLR	32	Overlay Background Color
1400E02C	OVL_SRC_CON	32	Overlay Source Control
1400E030	OVL_L0_CON	32	Overlay Layer 0 Control
1400E034	OVL_L0_SRCKEY	32	Overlay Layer 0 Source Key
1400E038	OVL_L0_SRC_SIZE	32	Overlay Layer 0 Source Size
1400E03C	OVL_L0_OFFSET	32	Overlay Layer 0 Offset
1400EF40	OVL_L0_ADDR	32	Overlay Layer 0 Memory Address
1400E044	OVL_L0_PITCH	32	Overlay Layer 0 Pitch
1400E048	OVL_L0_TILE	32	Overlay Layer 0 Tile Control
1400E04C	OVL_L0_CLIP	32	Overlay Layer 0 Clip
1400E050	OVL_L1_CON	32	Overlay Layer 1 Control
1400E054	OVL_L1_SRCKEY	32	Overlay Layer 1 Source Key
1400E058	OVL_L1_SRC_SIZE	32	Overlay Layer 1 Source Size
1400E05C	OVL_L1_OFFSET	32	Overlay Layer 1 Offset

Address	Name	Width	Register Function
1400EF60	OVL_L1_ADDR	32	Overlay Layer 1 Memory Address
1400E064	OVL_L1_PITCH	32	Overlay Layer 1 Pitch
1400E068	OVL_L1_TILE	32	Overlay Layer 1 Tile Control
1400E06C	OVL_L1_CLIP	32	Overlay Layer 1 Clip
1400E088	OVL_L2_TILE	32	Overlay Layer 2 Tile Control
1400E090	OVL_L3_CON	32	Overlay Layer 3 Control
1400E09C	OVL_L3_OFFSET	32	Overlay Layer 3 Offset
1400E0A8	OVL_L3_TILE	32	Overlay Layer 3 Tile Control
1400E0C0	OVL_RDMA0_CTRL	32	Overlay RDMA0 Control
1400E0C8	OVL_RDMA0_MEM_GMC_SETTING1	32	Overlay RDMA0 Memory GMC Setting
1400E0CC	OVL_RDMA0_MEM_SLOW_CON	32	Overlay RDMA0 Memory Slow Control
1400E0D0	OVL_RDMA0_FIFO_CTRL	32	Overlay RDMA0 FIFO Control
1400E0E0	OVL_RDMA1_CTRL	32	Overlay RDMA1 Control
1400E0E8	OVL_RDMA1_MEM_GMC_SETTING1	32	Overlay RDMA1 Memory GMC Setting
1400E0EC	OVL_RDMA1_MEM_SLOW_CON	32	Overlay RDMA1 Memory Slow Control
1400E0F0	OVL_RDMA1_FIFO_CTRL	32	Overlay RDMA1 FIFO Control
1400E108	OVL_RDMA2_MEM_GMC_SETTING1	32	Overlay RDMA2 Memory GMC Setting
1400E10C	OVL_RDMA2_MEM_SLOW_CON	32	Overlay RDMA2 Memory Slow Control
1400E110	OVL_RDMA2_FIFO_CTRL	32	Overlay RDMA2 FIFO Control
1400E120	OVL_RDMA3_CTRL	32	Overlay RDMA3 Control
1400E128	OVL_RDMA3_MEM_GMC_SETTING1	32	Overlay RDMA3 Memory GMC Setting
1400E12C	OVL_RDMA3_MEM_SLOW_CON	32	Overlay RDMA3 Memory Slow Control
1400E130	OVL_RDMA3_FIFO_CTRL	32	Overlay RDMA3 FIFO Control
1400E134	OVL_L0_Y2R_PARA_R0	32	Overlay L0 Y2R Conversion Parameter R0
1400E138	OVL_L0_Y2R_PARA_R1	32	Overlay L0 Y2R Conversion Parameter R1
1400E13C	OVL_L0_Y2R_PARA_G0	32	Overlay L0 Y2R Conversion Parameter G0
1400E140	OVL_L0_Y2R_PARA_G1	32	Overlay L0 Y2R Conversion Parameter G1
1400E144	OVL_L0_Y2R_PARA_B0	32	Overlay L0 Y2R Conversion Parameter B0
1400E148	OVL_L0_Y2R_PARA_B1	32	Overlay L0 Y2R Conversion Parameter B1
1400E14C	OVL_L0_Y2R_PARA_YUV_A_0	32	Overlay L0 Y2R Conversion Parameter Extended Add on YUV 0
1400E150	OVL_L0_Y2R_PARA_YUV_A_1	32	Overlay L0 Y2R Conversion Parameter Extended Add on YUV 1
1400E154	OVL_L0_Y2R_PAR	32	Overlay L0 Y2R Conversion Parameter Extended Add on

Address	Name	Width	Register Function
	A_RGB_A_0		RGB 0
1400E158	OVL_L0_Y2R_PARA_RGB_A_1	32	Overlay L0 Y2R Conversion Parameter Extended Add on RGB 1
1400E15C	OVL_L1_Y2R_PARA_R0	32	Overlay L1 Y2R Conversion Parameter R0
1400E160	OVL_L1_Y2R_PARA_R1	32	Overlay L1 Y2R Conversion Parameter R1
1400E164	OVL_L1_Y2R_PARA_G0	32	Overlay L1 Y2R Conversion Parameter G0
1400E168	OVL_L1_Y2R_PARA_G1	32	Overlay L1 Y2R Conversion Parameter G1
1400E16C	OVL_L1_Y2R_PARA_B0	32	Overlay L1 Y2R Conversion Parameter B0
1400E170	OVL_L1_Y2R_PARA_B1	32	Overlay L1 Y2R Conversion Parameter B1
1400E174	OVL_L1_Y2R_PARA_YUV_A_0	32	Overlay L1 Y2R Conversion Parameter Extended Add on YUV 0
1400E178	OVL_L1_Y2R_PARA_YUV_A_1	32	Overlay L1 Y2R Conversion Parameter Extended Add on YUV 1
1400E17C	OVL_L1_Y2R_PARA_RGB_A_0	32	Overlay L1 Y2R Conversion Parameter Extended Add on RGB 0
1400E180	OVL_L1_Y2R_PARA_RGB_A_1	32	Overlay L1 Y2R Conversion Parameter Extended Add on RGB 1
1400E184	OVL_L2_Y2R_PARA_R0	32	Overlay L2 Y2R Conversion Parameter R0
1400E188	OVL_L2_Y2R_PARA_R1	32	Overlay L2 Y2R Conversion Parameter R1
1400E18C	OVL_L2_Y2R_PARA_G0	32	Overlay L2 Y2R Conversion Parameter G0
1400E190	OVL_L2_Y2R_PARA_G1	32	Overlay L2 Y2R Conversion Parameter G1
1400E194	OVL_L2_Y2R_PARA_B0	32	Overlay L2 Y2R Conversion Parameter B0
1400E198	OVL_L2_Y2R_PARA_B1	32	Overlay L2 Y2R Conversion Parameter B1
1400E19C	OVL_L2_Y2R_PARA_YUV_A_0	32	Overlay L2 Y2R Conversion Parameter Extended Add on YUV 0
1400E1A0	OVL_L2_Y2R_PARA_YUV_A_1	32	Overlay L2 Y2R Conversion Parameter Extended Add on YUV 1
1400E1A4	OVL_L2_Y2R_PARA_RGB_A_0	32	Overlay L2 Y2R Conversion Parameter Extended Add on RGB 0
1400E1A8	OVL_L2_Y2R_PARA_RGB_A_1	32	Overlay L2 Y2R Conversion Parameter Extended Add on RGB 1
1400E1AC	OVL_L3_Y2R_PARA_R0	32	Overlay L3 Y2R Conversion Parameter R0
1400E1B0	OVL_L3_Y2R_PARA_R1	32	Overlay L3 Y2R Conversion Parameter R1
1400E1B4	OVL_L3_Y2R_PARA_G0	32	Overlay L3 Y2R Conversion Parameter G0
1400E1B8	OVL_L3_Y2R_PARA_G1	32	Overlay L3 Y2R Conversion Parameter G1
1400E1BC	OVL_L3_Y2R_PARA_B0	32	Overlay L3 Y2R Conversion Parameter B0
1400E1C0	OVL_L3_Y2R_PAR	32	Overlay L3 Y2R Conversion Parameter B1

Address	Name	Width	Register Function
	A_B1		
1400E1C4	OVL_L3_Y2R_PARA_YUV_A_0	32	Overlay L3 Y2R Conversion Parameter Extended Add on YUV 0
1400E1C8	OVL_L3_Y2R_PARA_YUV_A_1	32	Overlay L3 Y2R Conversion Parameter Extended Add on YUV 1
1400E1CC	OVL_L3_Y2R_PARA_RGB_A_0	32	Overlay L3 Y2R Conversion Parameter Extended Add on RGB 0
1400E1D0	OVL_L3_Y2R_PARA_RGB_A_1	32	Overlay L3 Y2R Conversion Parameter Extended Add on RGB 1
1400E1D4	OVL_DEBUG_MON_SEL	32	Overlay Debug Monitor Select
1400E1E0	OVL_RDMA0_MEM_GMC_SETTING2	32	Overlay RDMA0 Memory GMC Setting
1400E1E4	OVL_RDMA1_MEM_GMC_SETTING2	32	Overlay RDMA1 Memory GMC Setting
1400E1F0	OVL_RDMA_BURST_CON0	32	Overlay RDMA Burst Control
1400E1F4	OVL_RDMA_BURST_CON1	32	Overlay RDMA Burst Control
1400E1F8	OVL_RDMA_GREQ_NUM	32	Overlay RDMA GREQ Number
1400E1FC	OVL_RDMA_GREQ_URG_NUM	32	Overlay RDMA GREQ Number
1400E200	OVL_DUMMY_REG	32	Overlay Dummy Register
1400E208	OVL_GDRDY_PRD	32	Overlay SMI GDRDY Period
1400E20C	OVL_RDMA_ULTRA_SRC	32	Overlay RDMA Ultra SRC
1400E210	OVL_RDMA0_BUF_LOW	32	Overlay RDMA BUF Low
1400E214	OVL_RDMA1_BUF_LOW	32	Overlay RDMA BUF Low
1400E230	OVL_SMI_DBG	32	Overlay SMI Arbiter Debug Monitor
1400E234	OVL_GREQ_LAYER_CNT	32	Overlay Layer GREQ Counter
1400E238	OVL_GDRDY_PRD_NUM	32	Overlay SMI GDRDY Period Number
1400E240	OVL_FLOW_CTRL_DBG	32	Overlay Flow Control Debug Monitor
1400E244	OVL_ADDCON_DBG	32	Overlay Address Control Debug
1400E24C	OVL_RDMA0_DBG	32	Overlay RDMA0 Debug Monitor
1400E250	OVL_RDMA1_DBG	32	Overlay RDMA1 Debug Monitor
1400E25C	OVL_L0_CLR	32	Overlay Layer 0 Constant Color
1400E260	OVL_L1_CLR	32	Overlay Layer 1 Constant Color
1400E26C	OVL_LC_CLR	32	Overlay Constant Layer Color
1400E270	OVL_CRC	32	Overlay CRC
1400E280	OVL_LC_CON	32	Overlay Constant Layer Control
1400E284	OVL_LC_SRCKEY	32	Overlay Constant Layer Source Key
1400E288	OVL_LC_SRC_SIZE	32	Overlay Layer C Source Size
1400E28C	OVL_LC_OFFSET	32	Overlay Layer C Offset
1400E290	OVL_LC_SRC_SEL	32	Overlay Constant Layer Source Selection
1400E29C	OVL_BANK_CON	32	Overlay Bank Control

Address	Name	Width	Register Function
1400EFC0	OVL_SECURE	32	Overlay Layer Secure Bit

1400E000 OVL_STA **Overlay Status Monitor** **00000006**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RDMA1_IDLE	RDMA0_IDLE	OVL_RUN
Type														RU	RU	RU
Reset														1	1	0

Bit(s)	Mnemonic	Name	Description
2		RDMA1_IDLE	**Status of overlay RDMA1** 0: RDMA is in running. 1: Overlay RDMA are all idle.
1		RDMA0_IDLE	**Status of overlay RDMA0** 0: RDMA is in running. 1: Overlay RDMA are all idle.
0		OVL_RUN	**Status of overlay engine** 0: Overlay is idle. 1: Overlay is running.

1400E004 OVL_INTEN **Overlay Interrupt Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ABNORMAL_SOF_INTEN			RDMA1_SMI_UNDERFLOW_INTEN	RDMA0_SMI_UNDERFLOW_INTEN			RDMA1_EOF_ABNORMAL_INTEN	RDMA0_EOF_ABNORMAL_INTEN	OVL_FME_HWRST_DONE_INTEN	OVL_FME_SWRST_DONE_INTEN	OVL_FME_UND_INTEN	OVL_FME_CPL_INTEN	OVL_REG_CMT_INTEN
Type			RW			RW	RW			RW	RW	RW	RW	RW	RW	RW
Reset			0			0	0			0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13		ABNORMAL_SOF_INTEN	**Control abnormal SOF interrupt**
10		RDMA1_SMI_UNDERFLOW_INTEN	**Control RDMA1 SMI underflow interrupt** 0: Disable RDMA1 SMI data underflow interrupt 1: Enable RDMA1 SMI data underflow interrupt
9		RDMA0_SMI_UNDERFLOW_INTEN	**Control RDMA0 SMI underflow interrupt** 0: Disable RDMA0 SMI data underflow interrupt 1: Enable RDMA0 SMI data underflow interrupt

Bit(s)	Mnemonic	Name	Description
6		RDMA1_EOF_ABNORMAL_INTEN	**Control RDMA1 EOF abnormal interrupt** 0: Disable RDMA1 EOF abnormal interrupt 1: Enable RDMA1 EOF abnormal interrupt
5		RDMA0_EOF_ABNORMAL_INTEN	**Control RDMA0 EOF abnormal interrupt** 0: Disable RDMA0 EOF abnormal interrupt 1: Enable RDMA0 EOF abnormal interrupt
4		OVL_FME_HWRST_DONE_INTEN	**Control frame HW reset done interrupt** 0: Disable frame HW reset done interrupt 1: Enable frame HW reset done interrupt
3		OVL_FME_SWRST_DONE_INTEN	**Control frame SW reset done interrupt** 0: Disable frame SW reset done interrupt 1: Enable frame SW reset done interrupt
2		OVL_FME_UND_INTEN	**Control frame underflow interrupt** 0: Disable frame underflow interrupt 1: Enable frame underflow interrupt
1		OVL_FME_CPL_INTEN	**Control frame complete interrupt** 0: Disable frame complete interrupt 1: Enable frame complete interrupt
0		OVL_REG_CMT_INTEN	**Control register setting complete interrupt** 0: Disable register commit interrupt 1: Enable register commit interrupt

1400E008 OVL_INTSTA Overlay Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ABNORMAL_SOF_INTSTA			RDMA1_SMI_UNDERFLOW_INTSTA	RDMA0_SMI_UNDERFLOW_INTSTA			RDMA1_EOF_ABNORMAL_INTSTA	RDMA0_EOF_ABNORMAL_INTSTA	OVL_FME_HWRST_DONE_INTSTA	OVL_FME_SWRST_DONE_INTSTA	OVL_FME_UND_INTSTA	OVL_FME_CPL_INTSTA	OVL_REG_CMT_INTSTA
Type			A1			A1	A1			A1	A1	A1	A1	A1	A1	A1
Reset			0			0	0			0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13		ABNORMAL_SOF_INTSTA	
10		RDMA1_SMI_UNDERFLOW_INTSTA	**RDMA1 SMI status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA1 SMI data are not underflow. 1: RDMA1 SMI data are underflow.
9		RDMA0_SMI_UNDERFLOW_INTSTA	**RDMA0 SMI status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA0 SMI data are not underflow. 1: RDMA0 SMI data are underflow.
6		RDMA1_EOF_ABNORMAL_INTSTA	**RDMA1 status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless.

Bit(s)	Mnemonic	Name	Description
			0: RDMA1 complete normally 1: RDMA1 not complete till EOF
5		RDMA0_EOF_ABNORMAL_INTSTA	**RDMA0 status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: RDMA0 complete normally 1: RDMA0 not complete till EOF
4		OVL_FME_HWRST_DONE_INTSTA	**Overlay HW reset done status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: No HW reset/HW reset is not done. 1: HW reset is done.
3		OVL_FME_SWRST_DONE_INTSTA	**Overlay SW reset done status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: No SW reset/SW reset is not done. 1: SW reset is done.
2		OVL_FME_UND_INTSTA	**Overlay frame underflow status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: Frame complete w/o underflow 1: Frame not complete w/ underflow
1		OVL_FME_CPL_INTSTA	**Overlay frame complete status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: Frame not complete 1: Frame complete
0		OVL_REG_CMT_INTSTA	**Overlay register commit status** Controls interrupt write-clear. Cleared by writing 0; writing 1 is useless. 0: Regsiter is not set from shadow register to working register. 1: Register is set to working register done.

1400E00C OVL_EN **Overlay Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																IGNORE_ABNORMAL_SOF
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							HG_FSMI_CK_ON	HG_FOVL_CK_ON								OVL_EN
Type							RW	RW								RW
Reset							0	0								0

Bit(s)	Mnemonic	Name	Description
16		IGNORE_ABNORMAL_SOF	
9		HG_FSMI_CK_ON	
8		HG_FOVL_CK_ON	

Bit(s)	Mnemonic	Name	Description
0	**OVEN**	OVL_EN	**Enables overlay engine** 0: Disable overlay 1: Enable overlay

1400E010 OVL_TRIG **Overlay Trigger** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**CRC_CLR**	**CRC_EN**								**OVL_SW_TRIG**
Type							RW	RW								RW
Reset							0	0								0

Bit(s)	Mnemonic	Name	Description
9		CRC_CLR	
8		CRC_EN	
0	**OVTR**	OVL_SW_TRIG	**SW trigger to enable overlay engine** 0: When using HW trigger (SOF), this bit should be 0. 1: SW control to enable overlay engine.

1400E014 OVL_RST **Overlay Reset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**OVL_RST**
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		OVL_RST	**Overlay SW reset control for engine (high active)** 1: Reset engine

1400E020 OVL_ROI_SIZE **Overlay ROI Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**ROI_H**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**ROI_W**												
Type				RW												

Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**ROIH**	ROI_H	**Overlay ROI width** Range: 1 ~ 8191. For 3D display, this value should be 2 ~ 8191.
12:0	**ROIW**	ROI_W	**Overlay ROI width** Range: 1 ~ 8191. For 3D display, this value should be 2 ~ 8191.

1400E024 OVL_DATAPATH_CON **Overlay Datapath Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									RDMA3_OUT_SEL	RDMA2_OUT_SEL	RDMA1_OUT_SEL	RDMA0_OUT_SEL			PQ_OUT_SEL	
Type									OTHER	OTHER	OTHER	OTHER			OTHER	
Reset									0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OVL_GAMMA_OUT	ADOBE_LAYER		ADOBE_MODE			L1_GPU_MODE	L0_GPU_MODE					OUTPUT_NO_RND	BGCLR_IN_SEL	OVL_RANDOM_BGCLR_EN	LAYER_SMI_ID_EN
Type	RW	RW		RW			RW	RW					RW	RW	RW	RW
Reset	0	0	0	0			0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
23	**RDMA3SEL**	RDMA3_OUT_SEL	**Selects output path of RDMA3** 0: OVL Layer 3 1: PQ direct link output
22	**RDMA2SEL**	RDMA2_OUT_SEL	**Selects output path of RDMA2** 0: OVL Layer 2 1: PQ direct link output
21	**RDMA1SEL**	RDMA1_OUT_SEL	**Selects output path of RDMA1** 0: OVL Layer 1 1: PQ direct link output
20	**RDMA0SEL**	RDMA0_OUT_SEL	**Selects output path of RDMA0** 0: OVL Layer 0 1: PQ direct link output
17:16	**PQSEL**	PQ_OUT_SEL	**Selects PQ direct link output data** 00: RDMA0 01: RDMA1 10: RDMA2 11: RDMA3
15	**OVL_GAMMA_OUT**	OVL_GAMMA_OUT	**Wide-gamut OVL output GAMMA table path** (shares GAMMA-table with layer Adobe_mode) 0: Disable OVL output GAMMA table 1: Enable OVL output GAMMA table
14:13	**ADOBE_LAYER**	ADOBE_LAYER	**Selects wide-gamut layer Adobe** 0: Select Layer 0 adobe_path 1: Select Layer 1 adobe_path 2: Select Layer 2 adobe_path 3: Select Layer 3 adobe_path

Bit(s)	Mnemonic	Name	Description
12	**ADOBE**	ADOBE_MODE	**Wide-gamut layer Adobe mode** (shares GAMMA-table with ovl_gamma_out mode) 0: Disable layer Adobe path 1: Enable layer Adobe path
9	**L1_GPU**	L1_GPU_MODE	**Wide-gamut Layer 1 GPU path mode** 0: Disable Layer 1 GPU path 1: Enable Layer 1 GPU path
8	**L0_GPU**	L0_GPU_MODE	**Wide-gamut Layer 0 GPU path mode** 0: Disable Layer 0 GPU path 1: Enable Layer 0 GPU path
3		OUTPUT_NO_RND	
2		BGCLR_IN_SEL	**OVL BGCLR direct link path** 0: Disable OVL BGCLR direct link input 1: Enable OVL BGCLR direct link input
1		OVL_RANDOM_BGCLR_EN	**When OVL_RANDOM_BGCLR_EN=1, layer_en[i] should be set to 0 to allow the background color to pass through the Blend engine.** 0: Disable random background color pattern 1: Enable random background color pattern
0	**LAYER_SMI_ID_EN**	LAYER_SMI_ID_EN	**Supports OVL SMI ID function** 0: Disable SMI ID 1: Enable SMI ID

1400E028 OVL_ROI_BGCLR **Overlay Background Color** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24	**BGDA**	ALPHA	Alpha component of ROI window background color
23:16	**BGDR**	RED	Red component of ROI window background color
15:8	**BGDG**	GREEN	Green component of ROI window background color
7:0	**BGDB**	BLUE	Blue component of ROI window background color

1400E02C OVL_SRC_CON **Overlay Source Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												LC_EN			L1_EN	Lo_EN
Type												RW			RW	RW

Reset												0			0	0

Bit(s)	Mnemonic	Name	Description
4	**LCEN**	LC_EN	**Set up this bit to enable overlay constant layer.** 0: Disable constant layer 1: Enable constant layer
1	**L1EN**	L1_EN	**Set up this bit to enable overlay Layer 1.** 0: Disable Layer 1 1: Enable Layer 1
0	**L0EN**	L0_EN	**Set up this bit to enable overlay Layer 0.** 0: Disable Layer 0 1: Enable Layer 0

1400E030 OVL_L0_CON **Overlay Layer 0 Control** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSTKEY_EN	SRCKEY_EN	LAYER_SRC		MTX_EN	MTX_AUTO_DIS	RGB_SWAP	BYTE_SWAP	CLRFMT_MAN	R_FIRST	LANDSCAPE	EN_3D	INT_MTX_SEL			
Type	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLRFMT				EXT_MTX_EN	HORIZONTAL_FLIP_EN	VERTICAL_FLIP_EN	ALPHA_EN	ALPHA							
Type	RW				OTHER	RW	RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**DKEN**	DSTKEY_EN	**Enables destination color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable destination color key 1: Enable destination color key
30	**SKEN**	SRCKEY_EN	**Enables source color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable source color key 1: Enable source color key
29:28	**LSRC**	LAYER_SRC	**Selects layer pixel from memory/constant color/SCL/PQ** 00: Layer pixel from memory RDMA0 01: Layer pixel from constant color 10: Layer pixel from UFOd 11: Layer pixel from PQ
27		MTX_EN	
26		MTX_AUTO_DIS	
25	**RGSW**	RGB_SWAP	**No use**
24	**BTSW**	BYTE_SWAP	**Swaps unified color format** 0: RGB565, BGR888, BGRA8888, ABGR8888, UYVY, YUYV 1: BGR565, RGB888, RGBA8888, ARGB8888, VYUY, YVYU
23		CLRFMT_MAN	
22		R_FIRST	**Right eye image first when in 3D mode**

Bit(s)	Mnemonic	Name	Description
			0: Show left eye image first in 3D mode 1: Show right eye image first in 3D mode
21		LANDSCAPE	**Enables 3D landscape mode** 0: 3D portrait mode 1: 3D landscape mode
20		EN_3D	**Enables 3D mode** 0: 2D mode 1: 3D mode
19:16	**MTX**	INT_MTX_SEL	**Selects color matrix table** 0000: MTX_RGB_TO_JPEG 0010: MTX_RGB_TO_BT601 0011: MTX_RGB_TO_BT709 0100: MTX_JPEG_TO_RGB 0110: MTX_BT601_TO_RGB 0111: MTX_BT709_TO_RGB 1000: MTX_JPEG_TO_BT601 1001: MTX_JPEG_TO_BT709 1010: MTX_BT601_TO_JPEG 1011: MTX_BT709_TO_JPEG 1100: MTX_BT709_TO_BT601 1101: MTX_BT601_TO_BT709 Others: HW default (JPEG_TO_RGB)
15:12	**CFMT**	CLRFMT	**//--OLD define for reference only** 0000: RGB888 0001: RGB565 0010: ARGB8888 0011: PARGB8888 0100: xARGB8888 1000: YUYV 1001: UYVY 1010: YVYU 1011: VYUY 1111: YUV444 Others: Reserved color format 0000: RGB565 0001: RGB888 0010: RGBA8888/BGRA8888 0011: ARGB8888/ABGR8888 0100: UVVY, VYUY 0101: YUYV, YVYU
11	**MTXEN**	EXT_MTX_EN	**Enables external programmable coeff** 0: Matrix coeff 1: Programmable coeff
10	**HFE**	HORIZONTAL_FLIP_EN	**Enables horizontal flip** 0: Disable horizontal flip 1: Enable horizontal flip
9	**VFE**	VERTICAL_FLIP_ EN	**Enables vertical flip** 0: Disable vertical flip 1: Enable vertical flip
8	**AEN**	ALPHA_EN	**Enables alpha blending** 0: Disable alpha blending 1: Enable alpha blending
7:0	**APHA**	ALPHA	**Constant alpha value**

1400E034 OVL_L0_SRC **Overlay Layer 0 Source Key** **00000000**

KEY

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SKEY**	SRCKEY	**Layer source color key** Active when source color key is enabled.

1400E038 OVL_Lo_SRC_SIZE **Overlay Layer 0 Source Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				Lo_SRC_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				Lo_SRC_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**LoH**	Lo_SRC_H	**Layer source height** Range: 0 ~ 8191
12:0	**LoW**	Lo_SRC_W	**Layer source width** Range: 0 ~ 8191

1400E03C OVL_Lo_OFFSET **Overlay Layer 0 Offset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				Lo_YOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				Lo_XOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**LoH**	Lo_YOFF	**Layer vertical Y offset** Range: 0 ~ 8191
12:0	**LoXO**	Lo_XOFF	**Layer horizontal X offset** Range: 0 ~ 8191

1400EF40 OVL_Lo_ADDR — Overlay Layer 0 Memory Address — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Lo_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Lo_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**LoAD**	Lo_ADDR	Layer memory buffer address

1400E044 OVL_Lo_PITCH — Overlay Layer 0 Pitch — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SURFL_EN	Lo_BLEND_RND_SHT		Lo_CONST_BLD	Lo_DRGB_SEL_EXT	Lo_DA_SEL_EXT	Lo_SRGB_SEL_EXT	Lo_SA_SEL_EXT	Lo_DRGB_SEL		Lo_DA_SEL		Lo_SRGB_SEL		Lo_SA_SEL	
Type	RW	RW		RW	RW	RW	RW	RW	RW		RW		RW		RW	
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Lo_SRC_PITCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**LoSP**	SURFL_EN	**Enables layer surface dlinger alpha_blending** 0: Disable surface flinger alpha_blending 1: Enable surface flinger alpha_blending
30		Lo_BLEND_RND_SHT	
28		Lo_CONST_BLD	
27		Lo_DRGB_SEL_EXT	**Selects layer destination_RGB alpha**
26		Lo_DA_SEL_EXT	**Selects layer destination_Alpha alpha**
25		Lo_SRGB_SEL_EXT	**Selects layer source_RGB alpha**
24		Lo_SA_SEL_EXT	**Selects layer source_Alpha alpha**
23:22	**LoSP**	Lo_DRGB_SEL	**Selects layer destination_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
21:20	**LoSP**	Lo_DA_SEL	**Selects layer destination_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
19:18	**LoSP**	Lo_SRGB_SEL	**Selects layer source_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha

Bit(s)	Mnemonic	Name	Description
			11: Reserved
17:16	**LoSP**	Lo_SA_SEL	**Selects layer source_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
15:0	**LoSP**	Lo_SRC_PITCH	**Layer source pitch**

1400E048 OVL_Lo_TILE **Overlay Layer 0 Tile Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TILE_HORI_BLOCK_NUM										TILE_EN	TILE_WIDTH_SEL	TILE_HEIGHT			
Type	OTHER										OTHER	OTHER	OTHER			
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TILE_HEIGHT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**TILE_BLKS**	TILE_HORI_BLOCK_NUM	**Number of horizontal blocks**
21	**TILE_EN**	TILE_EN	**Enables tile mode** 0: Disable 1: Enable
20	**TILE_W**	TILE_WIDTH_SEL	**Width of tile** 0: 16 1: 32
19:0	**TILE_H**	TILE_HEIGHT	**Height of source tile mode**

1400E04C OVL_Lo_CLIP **Overlay Layer 0 Clip** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Lo_SRC_BOTTOM_CLIP								Lo_SRC_TOP_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Lo_SRC_RIGHT_CLIP								Lo_SRC_LEFT_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**Lo_SRC_BOTTOM_CLIP**	Lo_SRC_BOTTOM_CLIP	Layer 0 bottom clip
23:16	**Lo_SRC_TOP_CLIP**	Lo_SRC_TOP_CLIP	Layer 0 top clip
15:8	**Lo_SRC_RIGHT_CLIP**	Lo_SRC_RIGHT_CLIP	Layer 0 right clip
7:0	**Lo_SRC_LEFT_CLIP**	Lo_SRC_LEFT_CLIP	Layer 0 left clip

Bit(s)	Mnemonic	Name	Description

1400E050 OVL_L1_CON **Overlay Layer 1 Control** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSTKEY_EN	SRCKEY_EN	LAYER_SRC		MTX_EN	MTX_AUTO_DIS	RGB_SWAP	BYTE_SWAP	CLRFMT_MAN	R_FIRST	LANDSCAPE	EN_3D	INT_MTX_SEL			
Type	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLRFMT				EXT_MTX_EN	HORIZONTAL_FLIP_EN	VERTICAL_FLIP_EN	ALPHA_EN	ALPHA							
Type	RW				OTHER	RW	RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**DKEN**	DSTKEY_EN	**Enables destination color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable destination color key 1: Enable destination color key
30	**SKEN**	SRCKEY_EN	**Enables source color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable source color key 1: Enable source color key
29:28	**LSRC**	LAYER_SRC	**Selects layer pixel from memory/constant color/SCL/PQ** 00: Layer pixel from memory RDMA1 01: Layer pixel from constant color 10: Layer pixel from UFOd 11: Layer pixel from PQ
27		MTX_EN	
26		MTX_AUTO_DIS	
25	**RGSW**	RGB_SWAP	**No use**
24	**BTSW**	BYTE_SWAP	**Swaps unified color format** 0: RGB565, BGR888, BGRA8888, ABGR8888, UYVY, YUYV 1: BGR565, RGB888, RGBA8888, ARGB8888, VYUY, YVYU
23		CLRFMT_MAN	
22		R_FIRST	**Right eye image first when in 3D mode** 0: Show left eye image first in 3D mode 1: Show right eye image first in 3D mode
21		LANDSCAPE	**Enables 3D landscape mode** 0: 3D portrait mode 1: 3D landscape mode
20		EN_3D	**Enables 3D mode** 0: 2D mode 1: 3D mode
19:16	**MTX**	INT_MTX_SEL	**Selects color matrix table** 0000: MTX_RGB_TO_JPEG 0010: MTX_RGB_TO_BT601

Bit(s)	Mnemonic	Name	Description
			0011: MTX_RGB_TO_BT709 0100: MTX_JPEG_TO_RGB 0110: MTX_BT601_TO_RGB 0111: MTX_BT709_TO_RGB 1000: MTX_JPEG_TO_BT601 1001: MTX_JPEG_TO_BT709 1010: MTX_BT601_TO_JPEG 1011: MTX_BT709_TO_JPEG 1100: MTX_BT709_TO_BT601 1101: MTX_BT601_TO_BT709 Others: HW default (JPEG_TO_RGB)
15:12	**CFMT**	CLRFMT	**//--OLD define for reference only** 0000: RGB888 0001: RGB565 0010: ARGB8888 0011: PARGB8888 0100: xARGB8888 1000: YUYV 1001: UYVY 1010: YVYU 1011: VYUY 1111: YUV444 Others: Reserved color format 0000: RGB565 0001: RGB888 0010: RGBA8888/BGRA8888 0011: ARGB8888/ABGR8888 0100: UVVY, VYUY 0101: YUYV, YVYU
11	**MTXEN**	EXT_MTX_EN	**Enables external programmable coeff** 0: Matrix coeff 1: Programmable coeff
10	**HFE**	HORIZONTAL_FLIP_EN	**Enables horizontal flip** 0: Disable horizontal flip 1: Enable horizontal flip
9	**VFE**	VERTICAL_FLIP_ EN	**Enables vertical flip** 0: Disable vertical flip 1: Enable vertical flip
8	**AEN**	ALPHA_EN	**Enables alpha blending** 0: Disable alpha blending 1: Enable alpha blending
7:0	**APHA**	ALPHA	**Constant alpha value**

1400E054 OVL_L1_SRCKEY **Overlay Layer 1 Source Key** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SKEY**	SRCKEY	**Layer source color key** Active when source color key is enabled.

1400E058 OVL_L1_SRC_SIZE — Overlay Layer 1 Source Size — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L1_SRC_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L1_SRC_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**L1H**	L1_SRC_H	**Layer source height** Range: 0 ~ 8191
12:0	**L1W**	L1_SRC_W	**Layer source width** Range: 0 ~ 8191

1400E05C OVL_L1_OFFSET — Overlay Layer 1 Offset — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				L1_YOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L1_XOFF												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**L1H**	L1_YOFF	**Layer vertical Y offset** Range: 0 ~ 8191
12:0	**L1XO**	L1_XOFF	**Layer horizontal X offset** Range: 0 ~ 8191

1400EF60 OVL_L1_ADDR — Overlay Layer 1 Memory Address — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L1_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L1_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**L1AD**	L1_ADDR	Layer memory buffer address

1400E064 OVL_L1_PITCH **Overlay Layer 1 Pitch** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SURFL_EN	L1_BLEND_RND_SHT		L1_CONST_BLD	L1_DRGB_SEL_EXT	L1_DA_SEL_EXT	L1_SRGB_SEL_EXT	L1_SA_SEL_EXT	L1_DRGB_SEL		L1_DA_SEL		L1_SRGB_SEL		L1_SA_SEL	
Type	RW	RW		RW	RW	RW	RW	RW	RW		RW		RW		RW	
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L1_SRC_PITCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**L1SP**	SURFL_EN	**Enables layer surface dlinger alpha_blending** 0: Disable surface flinger alpha_blending 1: Enable surface flinger alpha_blending
30		L1_BLEND_RND_SHT	
28		L1_CONST_BLD	
27		L1_DRGB_SEL_EXT	**Selects layer destination_RGB alpha**
26		L1_DA_SEL_EXT	**Selects layer destination_Alpha alpha**
25		L1_SRGB_SEL_EXT	**Selects layer source_RGB alpha**
24		L1_SA_SEL_EXT	**Selects layer source_Alpha alpha**
23:22	**L1SP**	L1_DRGB_SEL	**Selects layer destination_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
21:20	**L1SP**	L1_DA_SEL	**Selects layer destination_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
19:18	**L1SP**	L1_SRGB_SEL	**Selects layer source_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
17:16	**L1SP**	L1_SA_SEL	**Selects layer source_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
15:0	**L1SP**	L1_SRC_PITCH	**Layer source pitch**

1400E068 OVL_L1_TIL **Overlay Layer 1 Tile Control** **00000000**

E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TILE_HORI_BLOCK_NUM										TILE_EN	TILE_WIDTH_SEL	TILE_HEIGHT			
Type	OTHER										OTHER	OTHER	OTHER			
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TILE_HEIGHT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**TILE_BLKS**	TILE_HORI_BLOCK_NUM	**Number of horizontal blocks**
21	**TILE_EN**	TILE_EN	**Enables tile mode** 0: Disable 1: Enable
20	**TILE_W**	TILE_WIDTH_SEL	**Width of tile** 0: 16 1: 32
19:0	**TILE_H**	TILE_HEIGHT	**Height of source tile mode**

1400E06C OVL_L1_CLIP **Overlay Layer 1 Clip** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	L1_SRC_BOTTOM_CLIP								L1_SRC_TOP_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	L1_SRC_RIGHT_CLIP								L1_SRC_LEFT_CLIP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**L1_SRC_BOTTOM_CLIP**	L1_SRC_BOTTOM_CLIP	Layer 1 bottom clip
23:16	**L1_SRC_TOP_CLIP**	L1_SRC_TOP_CLIP	Layer 1 top clip
15:8	**L1_SRC_RIGHT_CLIP**	L1_SRC_RIGHT_CLIP	Layer 1 right clip
7:0	**L1_SRC_LEFT_CLIP**	L1_SRC_LEFT_CLIP	Layer 1 left clip

1400E088 OVL_L2_TILE **Overlay Layer 2 Tile Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TILE_HORI_BLOCK_NUM										TILE_EN	TILE_WIDTH_SEL	TILE_HEIGHT			
Type	OTHER										OTHER	OTHER	OTHER			
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TILE_HEIGHT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**TILE_BLKS**	TILE_HORI_BLOCK_NUM	**Number of horizontal blocks**
21	**TILE_EN**	TILE_EN	**Enables tile mode** 0: Disable 1: Enable
20	**TILE_W**	TILE_WIDTH_SEL	**Width of tile** 0: 16 1: 32
19:0	**TILE_H**	TILE_HEIGHT	**Height of source tile mode**

1400E090 OVL_L3_CON **Overlay Layer 3 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					EXT_MTX_EN											
Type					OTHER											
Reset					0											

Bit(s)	Mnemonic	Name	Description
11	**MTXEN**	EXT_MTX_EN	**Enables external programmable coeff** 0: Matrix coeff 1: Programmable coeff

1400E09C OVL_L3_OFFSET **Overlay Layer 3 Offset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				L3_XOFF												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0	**L3XO**	L3_XOFF	**Layer horizontal X offset** Range: 0 ~ 8191

1400E0A8 OVL_L3_TILE Overlay Layer 3 Tile Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TILE_HORI_BLOCK_NUM										TILE_EN	TILE_WIDTH_SEL	TILE_HEIGHT			
Type	OTHER										OTHER	OTHER	OTHER			
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TILE_HEIGHT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	TILE_BLKS	TILE_HORI_BLOCK_NUM	**Number of horizontal blocks**
21	TILE_EN	TILE_EN	**Enables tile mode** 0: Disable 1: Enable
20	TILE_W	TILE_WIDTH_SEL	**Width of tile** 0: 16 1: 32
19:0	TILE_H	TILE_HEIGHT	**Height of source tile mode**

1400E0C0 OVL_RDMA0_CTRL Overlay RDMA0 Control 03FF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						RDMA0_FIFO_USED_SIZE										
Type						RU										
Reset						0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RDMA0_INTERLACE				RDMA0_EN
Type												OTHER				RW
Reset												0				0

Bit(s)	Mnemonic	Name	Description
26:16		RDMA0_FIFO_USED_SIZE	**Overlay RDMA0 used size**
4		RDMA0_INTERLACE	**Overlay RDMA0 interlace** 0: Disable 1: Enable
0		RDMA0_EN	**Overlay RDMA0 Enable** 0: Disable 1: Enable

1400E0C8 OVL_RDMA0_MEM_GMC_SETTING1 Overlay RDMA0 Memory GMC Setting 1010FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA0_PRE_ULTRA_THRESHOLD_HIGH_OFS								RDMA0_ULTRA_THRESHOLD_HIGH_OFS							
Type	OTHER								OTHER							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA0_PRE_ULTRA_THRESHOLD								RDMA0_ULTRA_THRESHOLD							
Type	OTHER								OTHER							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		RDMA0_PRE_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA0 pre_ultra threshold high offset
23:16		RDMA0_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA0 ultra threshold high offset
15:8		RDMA0_PRE_ULTRA_THRESHOLD	Overlay RDMA0 pre_ultra threshold
7:0		RDMA0_ULTRA_THRESHOLD	Overlay RDMA0 ultra threshold

1400E0CC OVL_RDMA0_MEM_SLOW_CON — Overlay RDMA0 Memory Slow Control — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA0_SLOW_CNT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RDMA0_SLOW_EN
Type																OTHER
Reset																0

Bit(s)	Mnemonic	Name	Description
31:16		RDMA0_SLOW_CNT	**Overlay RDMA0 memory slow-down counter** After this SLOW_CNT, SMI will raise greq again. 10: 10 cycles between 2 greq at least 33: 33 cycles between 2 greq at least
0		RDMA0_SLOW_EN	**Enables overlay RDMA0 memory slow-down** 0: Disable slow-down 1: Enable slow-down

1400E0D0 OVL_RDMA0_FIFO_CTRL — Overlay RDMA0 FIFO Control — 00800000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA0_FIFO_UND_EN						RDMA0_FIFO_SIZE									

Type	OTHER						RW									
Reset	0						0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RDMA0_FIFO_THRD									
Type							OTHER									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		RDMA0_FIFO_UND_EN	**Overlay RDMA0 FIFO underflow control** 0: Disable FIFO underflow 1: Enable FIFO underflow
25:16		RDMA0_FIFO_SIZ E	**Overlay RDMA0 FIFO size** Unit: 16 bytes 128: FIFO size is 128*128.
9:0		RDMA0_FIFO_THR D	**Overlay RDMA0 FIFO output valid threshold** Unit: 16 bytes. This value should be smaller than SRC_W*SRC_H*bpp >> 2. 0, 1: If FIFO pointer >= 1, RDMA will send data valid to OVL. 2: If FIFO pointer >= 2, RDMA will send data valid to OVL.

1400E0E0 OVL_RDMA1_CTRL — Overlay RDMA1 Control — 03FF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						RDMA1_FIFO_USED_SIZE										
Type						RU										
Reset						0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RDMA1_INTERLACE				RDMA1_EN
Type												OTHER				RW
Reset												0				0

Bit(s)	Mnemonic	Name	Description
26:16		RDMA1_FIFO_USED_SIZE	**Overlay RDMA1 used size**
4		RDMA1_INTERLAC E	**Overlay RDMA1 interlace** 0: Disable 1: Enable
0		RDMA1_EN	**Enables overlay RDMA1** 0: Disable 1: Enable

1400E0E8 OVL_RDMA1_MEM_GMC_SETTING1 — Overlay RDMA1 Memory GMC Setting — 1010FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA1_PRE_ULTRA_THRESHOLD_HIGH_OFS								RDMA1_ULTRA_THRESHOLD_HIGH_OFS							
Type	OTHER								OTHER							

Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA1_PRE_ULTRA_THRESHOLD								RDMA1_ULTRA_THRESHOLD							
Type	OTHER								OTHER							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		RDMA1_PRE_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA1 pre_ultra threshold high offset
23:16		RDMA1_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA1 ultra threshold high offset
15:8		RDMA1_PRE_ULTRA_THRESHOLD	Overlay RDMA1 pre_ultra threshold
7:0		RDMA1_ULTRA_THRESHOLD	Overlay RDMA1 ultra threshold

1400E0EC OVL_RDMA1_MEM_SLOW_CON **Overlay RDMA1 Memory Slow Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA1_SLOW_CNT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RDMA1_SLOW_EN
Type																OTHER
Reset																0

Bit(s)	Mnemonic	Name	Description
31:16		RDMA1_SLOW_CNT	**Overlay RDMA1 memory slow-down counter** After this SLOW_CNT, SMI will raise greq again. 10: 10 cycles between 2 greq at least 33: 33 cycles between 2 greq at least
0		RDMA1_SLOW_EN	**Enables overlay RDMA1 memory slow-down** 0: Disable slow-down 1: Enable slow-down

1400E0F0 OVL_RDMA1_FIFO_CTRL **Overlay RDMA1 FIFO Control** **00800000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA1_FIFO_UND_EN						RDMA1_FIFO_SIZE									
Type	OTHER						RW									
Reset	0						0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name							RDMA1_FIFO_THRD									
Type							OTHER									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		RDMA1_FIFO_UND _EN	**Overlay RDMA1 FIFO underflow control** 0: Disable FIFO underflow 1: Enable FIFO underflow
25:16		RDMA1_FIFO_SIZ E	**Overlay RDMA1 FIFO size** Unit: 16 bytes 128: FIFO size is 128*128.
9:0		RDMA1_FIFO_THR D	**Overlay RDMA1 FIFO output valid threshold** Unit: 16 bytes. This value should be smaller than SRC_W*SRC_H*bpp >> 2. 0, 1: If FIFO pointer >= 1, RDMA will send data valid to OVL. 2: If FIFO pointer >= 2, RDMA will send data valid to OVL.

1400E108 OVL_RDMA2_MEM_GMC_SETTING1 — Overlay RDMA2 Memory GMC Setting — 10100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA 2_PR E_UL TRA_ THRE SHOL D_HI GH_O FS								RDMA 2_UL TRA_ THRE SHOL D_HI GH_O FS							
Type	OTHER								OTHER							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
31:24		RDMA2_PRE_ULTR A_THRESHOLD_HI GH_OFS	Overlay RDMA2 pre_ultra threshold high offset
23:16		RDMA2_ULTRA_TH RESHOLD_HIGH_O FS	Overlay RDMA2 ultra threshold high offset

1400E10C OVL_RDMA2_MEM_SLOW_CON — Overlay RDMA2 Memory Slow Control — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA 2_SL OW_C NT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RDMA 2_SL OW_E N
Type																OTHER

Reset																0

Bit(s)	Mnemonic	Name	Description
31:16		RDMA2_SLOW_CNT	**Overlay RDMA2 memory slow-down counter** After this SLOW_CNT, SMI will raise greq again. 10: 10 cycles between 2 greq at least 33: 33 cycles between 2 greq at least
0		RDMA2_SLOW_EN	**Enables overlay RDMA2 memory slow-down** 0: Disable slow-down 1: Enable slow-down

1400E110 OVL_RDMA2_FIFO_CTRL **Overlay RDMA2 FIFO Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA2_FIFO_UND_EN															
Type	OTHER															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RDMA2_FIFO_THRD									
Type							OTHER									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		RDMA2_FIFO_UND_EN	**Overlay RDMA2 FIFO underflow control** 0: Disable FIFO underflow 1: Enable FIFO underflow
9:0		RDMA2_FIFO_THR D	**Overlay RDMA2 FIFO output valid threshold** Unit: 16 bytes. This value should be smaller than SRC_W*SRC_H*bpp >> 2. 0, 1: If FIFO pointer >= 1, RDMA will send data valid to OVL. 2: If FIFO pointer >= 2, RDMA will send data valid to OVL.

1400E120 OVL_RDMA3_CTRL **Overlay RDMA3 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RDMA3_INTERLACE				
Type												OTHER				
Reset												0				

Bit(s)	Mnemonic	Name	Description
4		RDMA3_INTERLAC E	**Overlay RDMA3 interlace** 0: Disable 1: Enable

1400E128 OVL_RDMA3_MEM_GMC_SETTING1 **Overlay RDMA3 Memory GMC Setting** **10100000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA3_PRE_ULTRA_THRESHOLD_HIGH_OFS								RDMA3_ULTRA_THRESHOLD_HIGH_OFS							
Type	OTHER								OTHER							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
31:24		RDMA3_PRE_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA3 pre_ultra threshold high offset
23:16		RDMA3_ULTRA_THRESHOLD_HIGH_OFS	Overlay RDMA3 ultra threshold high offset

1400E12C OVL_RDMA3_MEM_SLOW_CON **Overlay RDMA3 Memory Slow Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA3_SLOW_CNT															
Type	OTHER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RDMA3_SLOW_EN
Type																OTHER
Reset																0

Bit(s)	Mnemonic	Name	Description
31:16		RDMA3_SLOW_CNT	**Overlay RDMA3 memory slow-down counter** After this SLOW_CNT, SMI will raise greq again. 10: 10 cycles between 2 greq at least 33: 33 cycles between 2 greq at least
0		RDMA3_SLOW_EN	**Enables overlay RDMA3 memory slow-down** 0: Disable slow-down 1: Enable slow-down

1400E130 OVL_RDMA3_FIFO_CTRL **Overlay RDMA3 FIFO Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA3_FIFO_UND_EN						RDMA3_FIFO_SIZE									
Type	OTHER						RO									
Reset	0						0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RDMA3_FIFO_THRD									
Type							OTHER									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		RDMA3_FIFO_UND_EN	**Overlay RDMA3 FIFO underflow control** 0: Disable FIFO underflow 1: Enable FIFO underflow
25:16		RDMA3_FIFO_SIZE	**Overlay RDMA3 FIFO size** Unit: 16 bytes 128: FIFO size is 128*128.
9:0		RDMA3_FIFO_THRD	**Overlay RDMA3 FIFO output valid threshold** Unit: 16 bytes. This value should be smaller than SRC_W*SRC_H*bpp >> 2. 0, 1: If FIFO pointer >= 1, RDMA will send data valid to OVL. 2: If FIFO pointer >= 2, RDMA will send data valid to OVL.

1400E134 OVL_L0_Y2R_PARA_R0 **Overlay L0 Y2R Conversion Parameter R0** **00000400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_RMU												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_RMU	Overlay L0 YUV2RGB program parameter for R color of U component
12:0		C_CF_RMY	Overlay L0 YUV2RGB program parameter for R color of Y component

1400E138 OVL_L0_Y2R_PARA_R1 **Overlay L0 Y2R Conversion Parameter R1** **0000057C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMV												
Type				OTHER												
Reset				0	0	1	0	1	0	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_RMV	Overlay Lo YUV2RGB program parameter for R color of V component

1400E13C OVL_Lo_Y2R_PARA_Go **Overlay Lo Y2R Conversion Parameter Go** **1EA80400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_GMU												
Type				OTHER												
Reset				1	1	1	1	0	1	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_GMU	Overlay Lo YUV2RGB program parameter for G color of U component
12:0		C_CF_GMY	Overlay Lo YUV2RGB program parameter for G color of Y component

1400E140 OVL_Lo_Y2R_PARA_G1 **Overlay Lo Y2R Conversion Parameter G1** **00001D35**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMV												
Type				OTHER												
Reset				1	1	1	0	1	0	0	1	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_GMV	Overlay Lo YUV2RGB program parameter for G color of V component

1400E144 OVL_Lo_Y2R_PARA_Bo **Overlay Lo Y2R Conversion Parameter Bo** **06EE0400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name				C_CF_BMU												
Type				OTHER												
Reset				0	0	1	1	0	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_BMU	Overlay Lo YUV2RGB program parameter for B color of U component
12:0		C_CF_BMY	Overlay Lo YUV2RGB program parameter for B color of Y component

1400E148 OVL_Lo_Y2R_PARA_B1 — **Overlay Lo Y2R Conversion Parameter B1** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMV												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_BMV	Overlay Lo YUV2RGB program parameter for B color of V component

1400E14C OVL_Lo_Y2R_PARA_YUVA_0 — **Overlay Lo Y2R Conversion Parameter Extended Add on YUV 0** — **01800000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_UA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_YA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_UA	Overlay Lo YUV2RGB program parameter for U to add extended offset
8:0		C_CF_YA	Overlay Lo YUV2RGB program parameter for Y to add extended offset

1400E150 OVL_L0_Y2R_PARA_YUVA_1 — **Overlay L0 Y2R Conversion Parameter Extended Add on YUV 1** — **00000180**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_VA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_VA	Overlay L0 YUV2RGB program parameter for V to add extended offset

1400E154 OVL_L0_Y2R_PARA_RGBA_0 — **Overlay L0 Y2R Conversion Parameter Extended Add on RGB 0** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_GA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_RA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_GA	Overlay L0 YUV2RGB program parameter for G to add extended offset
8:0		C_CF_RA	Overlay L0 YUV2RGB program parameter for R to add extended offset

1400E158 OVL_L0_Y2R_PARA_RGBA_1 — **Overlay L0 Y2R Conversion Parameter Extended Add on RGB 1** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_BA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_BA	Overlay L0 YUV2RGB program parameter for B to add extended offset

1400E15C OVL_L1_Y2R_PARA_R0 **Overlay L1 Y2R Conversion Parameter R0** **00000400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_RMU												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_RMU	Overlay L1 YUV2RGB program parameter for R color of U component
12:0		C_CF_RMY	Overlay L1 YUV2RGB program parameter for R color of Y component

1400E160 OVL_L1_Y2R_PARA_R1 **Overlay L1 Y2R Conversion Parameter R1** **0000057C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMV												
Type				OTHER												
Reset				0	0	1	0	1	0	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_RMV	Overlay L1 YUV2RGB program parameter for R color of V component

1400E164 OVL_L1_Y2R_PARA_G0 **Overlay L1 Y2R Conversion Parameter G0** **1EA80400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_GMU												
Type				OTHER												
Reset				1	1	1	1	0	1	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_GMU	Overlay L1 YUV2RGB program parameter for G color of U component
12:0		C_CF_GMY	Overlay L1 YUV2RGB program parameter for G color of Y component

1400E168 OVL_L1_Y2R_PARA_G1 **Overlay L1 Y2R Conversion Parameter G1** **00001D35**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMV												
Type				OTHER												
Reset				1	1	1	0	1	0	0	1	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_GMV	Overlay L1 YUV2RGB program parameter for G color of V component

1400E16C OVL_L1_Y2R_PARA_B0 **Overlay L1 Y2R Conversion Parameter B0** **06EE0400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_BMU												
Type				OTHER												
Reset				0	0	1	1	0	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_BMU	Overlay L1 YUV2RGB program parameter for B color of U component
12:0		C_CF_BMY	Overlay L1 YUV2RGB program parameter for B color of Y component

1400E170 OVL_L1_Y2R_PARA_B1 **Overlay L1 Y2R Conversion Parameter B1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMV												
Type				OTHER												

Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_BMV	Overlay L1 YUV2RGB program parameter for B color of V component

1400E174 OVL_L1_Y2R_PARA_YUV_A_0 Overlay L1 Y2R Conversion Parameter Extended Add on YUV 0 01800000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_UA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_YA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_UA	Overlay L1 YUV2RGB program parameter for U to add extended offset
8:0		C_CF_YA	Overlay L1 YUV2RGB program parameter for Y to add extended offset

1400E178 OVL_L1_Y2R_PARA_YUV_A_1 Overlay L1 Y2R Conversion Parameter Extended Add on YUV 1 00000180

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_VA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_VA	Overlay L1 YUV2RGB program parameter for V to add extended offset

1400E17C OVL_L1_Y2R_PARA_RGB_A_0 Overlay L1 Y2R Conversion Parameter Extended Add on RGB 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_GA								
Type								OTHER								

Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_RA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_GA	Overlay L1 YUV2RGB program parameter for G to add extended offset
8:0		C_CF_RA	Overlay L1 YUV2RGB program parameter for R to add extended offset

1400E180 OVL_L1_Y2R_PARA_RGBA_1 **Overlay L1 Y2R Conversion Parameter Extended Add on RGB 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_BA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_BA	Overlay L1 YUV2RGB program parameter for B to add extended offset

1400E184 OVL_L2_Y2R_PARA_R0 **Overlay L2 Y2R Conversion Parameter R0** **00000400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_RMU												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_RMU	Overlay L2 YUV2RGB program parameter for R color of U component
12:0		C_CF_RMY	Overlay L2 YUV2RGB program parameter for R color of Y component

1400E188 OVL_L2_Y2R_PARA_R1 **Overlay L2 Y2R Conversion Parameter R1** **0000057C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMV												
Type				OTHER												
Reset				0	0	1	0	1	0	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_RMV	Overlay L2 YUV2RGB program parameter for R color of V component

1400E18C OVL_L2_Y2R_PARA_G0 **Overlay L2 Y2R Conversion Parameter G0** **1EA80400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_GMU												
Type				OTHER												
Reset				1	1	1	1	0	1	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_GMU	Overlay L2 YUV2RGB program parameter for G color of U component
12:0		C_CF_GMY	Overlay L2 YUV2RGB program parameter for G color of Y component

1400E190 OVL_L2_Y2R_PARA_G1 **Overlay L2 Y2R Conversion Parameter G1** **00001D35**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMV												
Type				OTHER												
Reset				1	1	1	0	1	0	0	1	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_GMV	Overlay L2 YUV2RGB program parameter for G color of V component

1400E194 OVL_L2_Y2R **Overlay L2 Y2R Conversion** **06EE0400**

_PARA_B0 Parameter B0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_BMU												
Type				OTHER												
Reset				0	0	1	1	0	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_BMU	Overlay L2 YUV2RGB program parameter for B color of U component
12:0		C_CF_BMY	Overlay L2 YUV2RGB program parameter for B color of Y component

1400E198 OVL_L2_Y2R_PARA_B1 Overlay L2 Y2R Conversion Parameter B1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMV												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_BMV	Overlay L2 YUV2RGB program parameter for B color of V component

1400E19C OVL_L2_Y2R_PARA_YUVA_0 Overlay L2 Y2R Conversion Parameter Extended Add on YUV 0 01800000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_UA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_YA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_UA	Overlay L2 YUV2RGB program parameter for U to add extended offset
8:0		C_CF_YA	Overlay L2 YUV2RGB program parameter for Y to add extended offset

Bit(s)	Mnemonic	Name	Description

1400E1A0 OVL_L2_Y2R_PARA_YUVA_1 **Overlay L2 Y2R Conversion Parameter Extended Add on YUV 1** **00000180**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_VA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_VA	Overlay L2 YUV2RGB program parameter for V to add extended offset

1400E1A4 OVL_L2_Y2R_PARA_RGBA_0 **Overlay L2 Y2R Conversion Parameter Extended Add on RGB 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_GA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_RA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_GA	Overlay L2 YUV2RGB program parameter for G to add extended offset
8:0		C_CF_RA	Overlay L2 YUV2RGB program parameter for R to add extended offset

1400E1A8 OVL_L2_Y2R_PARA_RGBA_1 **Overlay L2 Y2R Conversion Parameter Extended Add on RGB 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_BA								
Type								OTHER								

Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_BA	Overlay L2 YUV2RGB program parameter for B to add extended offset

1400E1AC OVL_L3_Y2R_PARA_R0 Overlay L3 Y2R Conversion Parameter R0 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_RMU												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_RMU	Overlay L3 YUV2RGB program parameter for R color of U component
12:0		C_CF_RMY	Overlay L3 YUV2RGB program parameter for R color of Y component

1400E1B0 OVL_L3_Y2R_PARA_R1 Overlay L3 Y2R Conversion Parameter R1 0000057C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_RMV												
Type				OTHER												
Reset				0	0	1	0	1	0	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_RMV	Overlay L3 YUV2RGB program parameter for R color of V component

1400E1B4 OVL_L3_Y2R_PARA_G0 Overlay L3 Y2R Conversion Parameter G0 1EA80400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_GMU												
Type				OTHER												
Reset				1	1	1	1	0	1	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMY												

Type				OTHER													
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_GMU	Overlay L3 YUV2RGB program parameter for G color of U component
12:0		C_CF_GMY	Overlay L3 YUV2RGB program parameter for G color of Y component

1400E1B8 OVL_L3_Y2R_PARA_G1 **Overlay L3 Y2R Conversion Parameter G1** **00001D35**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_GMV												
Type				OTHER												
Reset				1	1	1	0	1	0	0	1	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_GMV	Overlay L3 YUV2RGB program parameter for G color of V component

1400E1BC OVL_L3_Y2R_PARA_B0 **Overlay L3 Y2R Conversion Parameter B0** **06EE0400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C_CF_BMU												
Type				OTHER												
Reset				0	0	1	1	0	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMY												
Type				OTHER												
Reset				0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		C_CF_BMU	Overlay L3 YUV2RGB program parameter for B color of U component
12:0		C_CF_BMY	Overlay L3 YUV2RGB program parameter for B color of Y component

1400E1C0 OVL_L3_Y2R_PARA_B1 **Overlay L3 Y2R Conversion Parameter B1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C_CF_BMV												
Type				OTHER												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		C_CF_BMV	Overlay L3 YUV2RGB program parameter for B color of V component

1400E1C4 OVL_L3_Y2R_PARA_YUV_A_0 Overlay L3 Y2R Conversion Parameter Extended Add on YUV 0 01800000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_UA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_YA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_UA	Overlay L3 YUV2RGB program parameter for U to add extended offset
8:0		C_CF_YA	Overlay L3 YUV2RGB program parameter for Y to add extended offset

1400E1C8 OVL_L3_Y2R_PARA_YUV_A_1 Overlay L3 Y2R Conversion Parameter Extended Add on YUV 1 00000180

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_VA								
Type								OTHER								
Reset								1	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_VA	Overlay L3 YUV2RGB program parameter for V to add extended offset

1400E1CC OVL_L3_Y2R_PARA_RGB_A_0 Overlay L3 Y2R Conversion Parameter Extended Add on RGB 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								C_CF_GA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_RA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16		C_CF_GA	Overlay L3 YUV2RGB program parameter for G to add extended offset
8:0		C_CF_RA	Overlay L3 YUV2RGB program parameter for R to add extended offset

1400E1D0 OVL_L3_Y2R_PARA_RGB_A_1 **Overlay L3 Y2R Conversion Parameter Extended Add on RGB 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_CF_BA								
Type								OTHER								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		C_CF_BA	Overlay L3 YUV2RGB program parameter for B to add extended offset

1400E1D4 OVL_DEBUG_MON_SEL **Overlay Debug Monitor Select** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DBG_MON_SEL			
Type													WO			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0		DBG_MON_SEL	Overlay Debug Monitor Select

1400E1E0 OVL_RDMA0_ **Overlay RDMA0 Memory GMC** **205F00BF**

MEM_GMC_SETTING2 **Setting**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RDMA0_FORCE_REQ_THRESHOLD	RDMA0_REQ_THRESHOLD_ULTRA	RDMA0_REQ_THRESHOLD_PREULTRA		RDMA0_ISSUE_REQ_THRESHOLD_URG										
Type		RW	RW	RW		RW										
Reset		0	1	0		0	0	0	0	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RDMA0_ISSUE_REQ_THRESHOLD										
Type						RW										
Reset						0	0	0	1	0	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30		RDMA0_FORCE_REQ_THRESHOLD	
29		RDMA0_REQ_THRESHOLD_ULTRA	
28		RDMA0_REQ_THRESHOLD_PREULTRA	
26:16		RDMA0_ISSUE_REQ_THRESHOLD_URG	
10:0		RDMA0_ISSUE_REQ_THRESHOLD	Overlay RDMA0 issue request threshold (0 for best performance)

1400E1E4 **OVL_RDMA1_MEM_GMC_SETTING2** **Overlay RDMA1 Memory GMC Setting** **205F00BF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RDMA1_FORCE_REQ_THRESHOLD	RDMA1_REQ_THRESHOLD_ULTRA	RDMA1_REQ_THRESHOLD_PREULTRA		RDMA1_ISSUE_REQ_THRESHOLD_URG										
Type		RW	RW	RW		RW										
Reset		0	1	0		0	0	0	0	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RDMA1_ISSUE_REQ_THRESHOLD										
Type						RW										
Reset						0	0	0	1	0	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30		RDMA1_FORCE_REQ_THRESHOLD	
29		RDMA1_REQ_THRESHOLD_ULTRA	
28		RDMA1_REQ_THRESHOLD_PREULTRA	
26:16		RDMA1_ISSUE_RE	

Bit(s)	Mnemonic	Name	Description
10:0		Q_THRESHOLD_UR G RDMA1_ISSUE_RE Q_THRESHOLD	Overlay RDMA1 issue request threshold (0 for best performance)

1400E1F0 OVL_RDMA_BURST_CON0 **Overlay RDMA Burst Control** **07775533**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				BURST_128B_BOUND		BURST15A_32B				BURST14A_32B				BURST13A_32B		
Type				RW		RW				RW				RW		
Reset				0		1	1	1		1	1	1		1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		BURST12A_32B				BURST11A_32B				BURST10A_32B				BURST9A_32B		
Type		RW				RW				RW				RW		
Reset		1	0	1		1	0	1		0	1	1		0	1	1

Bit(s)	Mnemonic	Name	Description
28		BURST_128B_BOU ND	
26:24		BURST15A_32B	First burst slice for a 32B aligned burst of length 15
22:20		BURST14A_32B	First burst slice for a 32B aligned burst of length 14
18:16		BURST13A_32B	First burst slice for a 32B aligned burst of length 13
14:12		BURST12A_32B	First burst slice for a 32B aligned burst of length 12
10:8		BURST11A_32B	First burst slice for a 32B aligned burst of length 11
6:4		BURST10A_32B	First burst slice for a 32B aligned burst of length 10
2:0		BURST9A_32B	First burst slice for a 32B aligned burst of length 9

1400E1F4 OVL_RDMA_BURST_CON1 **Overlay RDMA Burst Control** **06666442**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						BURST15A_N32B				BURST14A_N32B				BURST13A_N32B		
Type						RW				RW				RW		
Reset						1	1	0		1	1	0		1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		BURST12A_N32B				BURST11A_N32B				BURST10A_N32B				BURST9A_N32B		
Type		RW				RW				RW				RW		
Reset		1	1	0		1	0	0		1	0	0		0	1	0

Bit(s)	Mnemonic	Name	Description
26:24		BURST15A_N32B	First burst slice for a non-32B aligned burst of length 15
22:20		BURST14A_N32B	First burst slice for a non-32B aligned burst of length 14
18:16		BURST13A_N32B	First burst slice for a non-32B aligned burst of length 13
14:12		BURST12A_N32B	First burst slice for a non-32B aligned burst of length 12
10:8		BURST11A_N32B	First burst slice for a non-32B aligned burst of length 11
6:4		BURST10A_N32B	First burst slice for a non-32B aligned burst of length 10
2:0		BURST9A_N32B	First burst slice for a non-32B aligned burst of length 9

1400E1F8 OVL_RDMA_GREQ_NUM **Overlay RDMA GREQ Number** **510F00BB**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IOBUF_FLUSH_ULTRA	IOBUF_FLUSH_PREULTRA		GRP_BRK_STOP	GREQ_STOP_EN	GREQ_DIS_CNT			OSTD_GREQ_NUM							
Type	RW	RW		RW	RW	RW			RW							
Reset	0	1		1	0	0	0	1	0	0	0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LAYER1_GREQ_NUM				LAYER0_GREQ_NUM			
Type									RW				RW			
Reset									1	0	1	1	1	0	1	1

Bit(s)	Mnemonic	Name	Description
31		IOBUF_FLUSH_ULTRA	
30		IOBUF_FLUSH_PREULTRA	
28		GRP_BRK_STOP	**Stop GREQ when group breaks**
27		GREQ_STOP_EN	**Stop each GREQ after GLCOMD**
26:24		GREQ_DIS_CNT	
23:16		OSTD_GREQ_NUM	
7:4	**LAYER1_GREQ_NUM**	LAYER1_GREQ_NUM	**OVL Layer 1 multi-greq number** Max.: 7
3:0	**LAYER0_GREQ_NUM**	LAYER0_GREQ_NUM	**OVL Layer 0 multi-greq number** Max.: 7

1400E1FC OVL_RDMA_GREQ_URG_NUM **Overlay RDMA GREQ Number** **20300055**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GREQ_NUM_SHT		GREQ_NUM_SHT_VAL	ARG_URG_BIAS			ARG_GREQ_URG_TH									
Type	RW		RW	RW			RW									
Reset	0	0	1	0			0	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LAYER1_GREQ_URG_NUM				LAYER0_GREQ_URG_NUM			
Type									RW				RW			
Reset									0	1	0	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
31:30		GREQ_NUM_SHT	
29		GREQ_NUM_SHT_VAL	
28		ARG_URG_BIAS	
25:16		ARG_GREQ_URG_TH	
7:4		LAYER1_GREQ_URG_NUM	**OVL Layer 1 multi-greq number** Max.: 7

Bit(s)	Mnemonic	Name	Description
3:0		LAYERo_GREQ_URG_NUM	**OVL Layer o multi-greq number** Max.: 7 (GREQ_URG_NUM <= GREQ_NUM)

1400E200 OVL_DUMMY_REG **Overlay Dummy Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OVERLAY_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OVERLAY_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		OVERLAY_DUMMY	Overlay dummy register

1400E208 OVL_GDRDY_PRD **Overlay SMI GDRDY Period** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									GDRDY_PRD							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDRDY_PRD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		GDRDY_PRD	

1400E20C OVL_RDMA_ULTRA_SRC **Overlay RDMA Ultra SRC** **0000A050**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ULTRA_RDMA_SRC		ULTRA_ROI_END_SRC		ULTRA_SMI_SRC		ULTRA_BUF_SRC		PREULTRA_RDMA_SRC		PREULTRA_ROI_END_SRC		PREULTRA_SMI_SRC		PREULTRA_BUF_SRC	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	1	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
15:14		ULTRA_RDMA_SRC	
13:12		ULTRA_ROI_END_ SRC	
11:10		ULTRA_SMI_SRC	
9:8		ULTRA_BUF_SRC	
7:6		PREULTRA_RDMA_ SRC	
5:4		PREULTRA_ROI_E ND_SRC	
3:2		PREULTRA_SMI_S RC	
1:0		PREULTRA_BUF_S RC	

1400E210 OVL_RDMA0_BUF_LOW **Overlay RDMA BUF Low** **00030020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											BUF_LOW_PREULTRA_TH					
Type											RW					
Reset											0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF_LOW_PREULTRA_TH						BUF_LOW_ULTRA_TH									
Type	RW						RW									
Reset	0	0	0	0			0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:12		BUF_LOW_PREULT RA_TH	
9:0		BUF_LOW_ULTRA_ TH	

1400E214 OVL_RDMA1_BUF_LOW **Overlay RDMA BUF Low** **00030020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											BUF_LOW_PREULTRA_TH					
Type											RW					
Reset											0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF_LOW_PREULTRA_TH						BUF_LOW_ULTRA_TH									
Type	RW						RW									
Reset	0	0	0	0			0	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:12		BUF_LOW_PREULT RA_TH	
9:0		BUF_LOW_ULTRA_ TH	

1400E230 OVL_SMI_DB **Overlay SMI Arbiter Debug** **00000001**

G Monitor

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SMI_FSM									
Type							RU									
Reset							0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
9:0		SMI_FSM	Overlay SMI arbiter FSM state

1400E234 OVL_GREQ_LAYER_CNT Overlay Layer GREQ Counter 00000101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			LAYER1_GREQ_CNT								LAYER0_GREQ_CNT					
Type			RU								RU					
Reset			0	0	0	0	0	1			0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
13:8		LAYER1_GREQ_CNT	RDMA Layer 1 greq counter
5:0		LAYER0_GREQ_CNT	RDMA Layer 0 greq counter

1400E238 OVL_GDRDY_PRD_NUM Overlay SMI GDRDY Period Number 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									GDRDY_PRD_NUM							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDRDY_PRD_NUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		GDRDY_PRD_NUM	

1400E240 OVL_FLOW_CTRL_DBG Overlay Flow Control Debug Monitor 000CBC01

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	OVL_UPD_REG	REG_UPDATE	OVL_CLR	OVL_START	OVL_RUNNING	FRAME_DONE	FRAME_UNDERRUN	FRAME_SWRST_DONE	FRAME_HWRST_DONE		TRIG	RST	RDMA0_IDLE	RDMA1_IDLE		
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU		RU	RU	RU	RU		
Reset	0	0	0	0	0	0	0	0	0		0	0	1	1		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OUT_IDLE		OVL_OUT_READY	OVL_OUT_VALID	BLEND_IDLE	ADDCON_IDLE	FSM_STATE									
Type	RU		RU	RU	RU	RU	RU									
Reset	1		1	1	1	1	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31		OVL_UPD_REG	**Overlay prepare to update register**
30		REG_UPDATE	**Updates overlay register**
29		OVL_CLR	**Clears overlay**
28		OVL_START	**Starts overlay**
27		OVL_RUNNING	**Overlay running**
26		FRAME_DONE	**Overlay frame complete**
25		FRAME_UNDERRUN	**Overlay frame underrun**
24		FRAME_SWRST_DONE	**Overlay frame reset done**
23		FRAME_HWRST_DONE	**Overlay EOF reset done**
21		TRIG	**Triggers overlay**
20		RST	**Resets overlay**
19		RDMA0_IDLE	**Overlay RDMA0 idle state**
18		RDMA1_IDLE	**Overlay RDMA1 idle state**
15		OUT_IDLE	**Overlay output relay idle state**
13		OVL_OUT_READY	**Overlay out_ready**
12		OVL_OUT_VALID	**Overlay out_valid**
11		BLEND_IDLE	**Overlay alpha blending idle state**
10		ADDCON_IDLE	**Overlay addcon idle state**
9:0		FSM_STATE	**Overlay flow control FSM state** 0x1: IDLE 0x2: WAIT 0x4: PREPARE 0x8: UPD_REG 0x10: ENG_CLR 0x20: ENG_ACT 0x40: H_WAIT_W_RST 0x80: S_WAIT_W_RST 0x100: H_W_RST 0x200: S_W_RST

1400E244 OVL_ADDCON_DBG **Overlay Address Control Debug** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				ROI_Y												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	L1_WIN_HIT	L0_WIN_HIT		ROI_X												
Type	RU	RU		RU												
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16		ROI_Y	Overlay pixel process vertical Y position
15		L1_WIN_HIT	Overlay Layer 1 pixel hit
14		L0_WIN_HIT	Overlay Layer 0 pixel hit
12:0		ROI_X	Overlay pixel process horizontal X position

1400E24C OVL_RDMA0_DBG **Overlay RDMA0 Debug Monitor** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMI_GREQ	RDMA0_SMI_BUSY	RDMA0_OUT_VALID	RDMA0_OUT_READY	RDMA0_OUT_DATA											
Type	RU	RU	RU	RU	RU											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA0_OUT_DATA												RDMA0_LAYER_GREQ	RDMA0_WRAM_RST_CS		
Type	RU												RU	RU		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31		SMI_GREQ	Overlay 4-to-1 SMI request
30		RDMA0_SMI_BUSY	Overlay RDMA0 SMI busy
29		RDMA0_OUT_VALI D	Overlay RDMA0 output valid
28		RDMA0_OUT_READ Y	Overlay RDMA0 output ready
27:4		RDMA0_OUT_DATA	Overlay RDMA0 output data
3		RDMA0_LAYER_GR EQ	Overlay RDMA0 SMI request
2:0		RDMA0_WRAM_RST _CS	Overlay RDMA0 warm reset current state

1400E250 OVL_RDMA1_DBG **Overlay RDMA1 Debug Monitor** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMI_GREQ	RDMA1_SMI_BUSY	RDMA1_OUT_VALID	RDMA1_OUT_READY	RDMA1_OUT_DATA											
Type	RU	RU	RU	RU	RU											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA1_OUT_DATA												RDMA1_LAYER_GREQ	RDMA1_WRAM_RST_CS		

Type	RU												RU	RU		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31		SMI_GREQ	Overlay 4-to-1 SMI request
30		RDMA1_SMI_BUSY	Overlay RDMA1 SMI busy
29		RDMA1_OUT_VALI D	Overlay RDMA1 output valid
28		RDMA1_OUT_READ Y	Overlay RDMA1 output ready
27:4		RDMA1_OUT_DATA	Overlay RDMA1 output data
3		RDMA1_LAYER_GR EQ	Overlay RDMA1 SMI request
2:0		RDMA1_WRAM_RST _CS	Overlay RDMA1 warm reset current state

1400E25C OVL_L0_CLR **Overlay Layer 0 Constant Color** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		ALPHA	Alpha component of L0 constant color
23:16		RED	Red component of L0 constant color
15:8		GREEN	Green component of L0 constant color
7:0		BLUE	Blue component of L0 constant color

1400E260 OVL_L1_CLR **Overlay Layer 1 Constant Color** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		ALPHA	Alpha component of L1 constant color
23:16		RED	Red component of L1 constant color
15:8		GREEN	Green component of L1 constant color
7:0		BLUE	Blue component of L1 constant color

1400E26C OVL_LC_CLR **Overlay Constant Layer Color** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALPHA								RED							

Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GREEN								BLUE							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		ALPHA	Alpha component of constant layer color
23:16		RED	Red component of constant layer color
15:8		GREEN	Green component of constant layer color
7:0		BLUE	Blue component of constant layer color

1400E270 OVL_CRC Overlay CRC 7FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRC_RDY	CRC_OUT														
Type	RU	RU														
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRC_OUT															
Type	RU															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31		CRC_RDY	
30:0		CRC_OUT	

1400E280 OVL_LC_CON Overlay Constant Layer Control 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSTKEY_EN	SRCKEY_EN	LAYER_SRC							R_FIRST	LANDSCAPE	EN_3D				
Type	RW	RW	RW							RW	RW	RW				
Reset	0	0	0	0						0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								ALPHA_EN	ALPHA							
Type								RW	RW							
Reset								0	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**DKEN**	DSTKEY_EN	**Enables destination color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable destination color key 1: Enable destination color key
30	**SKEN**	SRCKEY_EN	**Enables source color key** SRCKEY_EN and DSTKEY_EN are exclusive settings. They cannot be enabled at the same time. 0: Disable source color key

Bit(s)	Mnemonic	Name	Description
			1: Enable source color key
29:28	**LSRC**	LAYER_SRC	**Selects layer pixel from memory/constant color/SCL/PQ** 00: Layer pixel from constant color 01: Layer pixel from constant color 10: Layer pixel from UFOd 11: Layer pixel from PQ
22		R_FIRST	**Right eye image first when in 3D mode** 0: Show left eye image first in 3D mode 1: Show right eye image first in 3D mode
21		LANDSCAPE	**Enables 3D landscape mode** 0: 3D portrait mode 1: 3D landscape mode
20		EN_3D	**Enables 3D mode** 0: 2D mode 1: 3D mode
8	**AEN**	ALPHA_EN	**Enables alpha blending** 0: Disable alpha blending 1: Enable alpha blending
7:0	**APHA**	ALPHA	**Constant alpha value**

1400E284 OVL_LC_SRCKEY Overlay Constant Layer Source Key 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRCKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SKEY**	SRCKEY	**Layer source color key** Active when source color key is enabled.

1400E288 OVL_LC_SRCSIZE Overlay Layer C Source Size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LC_SRC_H												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				LC_SRC_W												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**LCH**	LC_SRC_H	**Layer source height**

Bit(s)	Mnemonic	Name	Description
12:0	**LCW**	LC_SRC_W	Range: 0 ~ 4095 **Layer source width** Range: 0 ~ 4095

1400E28C OVL_LC_OFFSET **Overlay Layer C Offset** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					LC_YOFF											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					LC_XOFF											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**LCH**	LC_YOFF	**Layer vertical Y offset** Range: 0 ~ 4095
11:0	**LCXO**	LC_XOFF	**Layer horizontal X offset** Range: 0 ~ 4095

1400E290 OVL_LC_SRC_SEL **Overlay Constant Layer Source Selection** **00000004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SURFL_EN	LC_BLEND_RND_SHT		LC_CONST_BLD	LC_DRGB_SEL_EXT	LC_DA_SEL_EXT	LC_SRGB_SEL_EXT	LC_SA_SEL_EXT	LC_D RGB_SEL		LC_D A_SEL		LC_S RGB_SEL		LC_SA_SEL	
Type	RW	RW		RW	RW	RW	RW	RW	RW		RW		RW		RW	
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CONST_LAYER_SEL		
Type														RW		
Reset														1	0	0

Bit(s)	Mnemonic	Name	Description
31	**LCSP**	SURFL_EN	**Enables layer surface dlinger alpha_blending** 0: Disable surface flinger alpha_blending 1: Enable surface flinger alpha_blending
30		LC_BLEND_RND_SHT	
28		LC_CONST_BLD	
27		LC_DRGB_SEL_EXT	**Selects layer destination_RGB alpha**
26		LC_DA_SEL_EXT	**Selects layer destination_Alpha alpha**
25		LC_SRGB_SEL_EXT	**Selects layer source_RGB alpha**
24		LC_SA_SEL_EXT	**Selects layer source_Alpha alpha**
23:22	**LCSP**	LC_DRGB_SEL	**Selects layer destination_RGB alpha** 00: ONE 01: Src_Alpha

Bit(s)	Mnemonic	Name	Description
			10: 1-Src_Alpha 11: Reserved
21:20	**LCSP**	LC_DA_SEL	**Selects layer destination_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
19:18	**LCSP**	LC_SRGB_SEL	**Selects layer source_RGB alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
17:16	**LCSP**	LC_SA_SEL	**Selects layer source_Alpha alpha** 00: ONE 01: Src_Alpha 10: 1-Src_Alpha 11: Reserved
2:0	**LCSP**	CONST_LAYER_SE L	**Layer source pitch**

1400E29C OVL_BANK_CON **Overlay Bank Control** **00000008**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												OVL_BANK_CON				
Type												RW				
Reset												0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		OVL_BANK_CON	

1400EFC0 OVL_SECURE **Overlay Layer Secure Bit** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															L1_SECURE	L0_SECURE
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1		L1_SECURE	Layer 1 secure bit
0		L0_SECURE	Layer 0 secure bit

Module name: DISP_RDMA0 Base address: (+1400f000h)

Address	Name	Width	Register Function
1400F000	DISP_RDMA_INT_ENABLE	32	RDMA Interrupt Enable
1400F004	DISP_RDMA_INT_STATUS	32	RDMA Interrupt Status
1400F010	DISP_RDMA_GLOBAL_CON	32	RDMA Global Control
1400F014	DISP_RDMA_SIZE_CON_0	32	RDMA Size Control 0
1400F018	DISP_RDMA_SIZE_CON_1	32	RDMA Size Control 1
1400F01C	DISP_RDMA_TARGET_LINE	32	RDMA Target Line
1400F024	DISP_RDMA_MEM_CON	32	RDMA Memory Mode Control
1400F02C	DISP_RDMA_MEM_SRC_PITCH	32	RDMA Memory Mode Line Pitch
1400F030	DISP_RDMA_MEM_GMC_SETTING_0	32	RDMA Memory Mode GMC Setting 0
1400F034	DISP_RDMA_MEM_GMC_SETTING_1	32	RDMA Memory Mode GMC Setting 1
1400F038	DISP_RDMA_MEM_SLOW_CON	32	RDMA Memory Mode Slow Control
1400F03C	DISP_RDMA_MEM_GMC_SETTING_2	32	RDMA Memory Mode GMC Setting 2
1400F040	DISP_RDMA_FIFO_CON	32	RDMA FIFO Control
1400F044	DISP_RDMA_FIFO_LOG	32	RDMA_FIFO_LOG
1400F054	DISP_RDMA_C00	32	RDMA YUV to RGB Coefficient
1400F058	DISP_RDMA_C01	32	RDMA YUV to RGB Coefficient
1400F05C	DISP_RDMA_C02	32	RDMA YUV to RGB Coefficient
1400F060	DISP_RDMA_C10	32	RDMA YUV to RGB Coefficient
1400F064	DISP_RDMA_C11	32	RDMA YUV to RGB Coefficient
1400F068	DISP_RDMA_C12	32	RDMA YUV to RGB Coefficient
1400F06C	DISP_RDMA_C20	32	RDMA YUV to RGB Coefficient
1400F070	DISP_RDMA_C21	32	RDMA YUV to RGB Coefficient
1400F074	DISP_RDMA_C22	32	RDMA YUV to RGB Coefficient
1400F078	DISP_RDMA_PRE_ADD_0	32	RDMA YUV to RGB Coefficient
1400F07C	DISP_RDMA_PRE_ADD_1	32	RDMA YUV to RGB Coefficient
1400F080	DISP_RDMA_PRE_ADD_2	32	RDMA YUV to RGB Coefficient
1400F084	DISP_RDMA_POST_ADD_0	32	RDMA YUV to RGB Coefficient
1400F088	DISP_RDMA_POST_ADD_1	32	RDMA YUV to RGB Coefficient
1400F08C	DISP_RDMA_POST_ADD_2	32	RDMA YUV to RGB Coefficient
1400F090	DISP_RDMA_DUMM	32	RDMA Dummy Register

Address	Name	Width	Register Function
	Y		
1400F094	DISP_RDMA_DEBUG_OUT_SEL	32	RDMA Debug Output Selection
1400FF00	DISP_RDMA_MEM_START_ADDR	32	RDMA Memory Mode Start Address
1400F0A0	DISP_RDMA_BG_CON_0	32	Add Black Frame Outside of Image
1400F0A4	DISP_RDMA_BG_CON_1	32	Add Black Frame Outside of Image
1400F0A8	DISP_RDMA_THRESHOLD_FOR_SODI	32	RDMA Threshold Setting for SODI
1400F0AC	DISP_RDMA_THRESHOLD_FOR_DVFS	32	RDMA Threshold Setting for DVFS
1400F0B0	DISP_RDMA_SRAM_SEL	32	RDMA SRAM Selection
1400F0B4	DISP_RDMA_STALL_CG_CON	32	RDMA Internal Stall Clock Gated Configuration

1400F000 DISP_RDMA_INT_ENABLE **RDMA Interrupt Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										FIFO_EMPTY_INT_EN	TARGET_LINE_INT_EN	FIFO_UNDERFLOW_INT_EN	EOF_ABNORMAL_INT_EN	FRAME_END_INT_EN	FRAME_START_INT_EN	REG_UPDATE_INT_EN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	FIFO_EMPTY_INT_EN	**Enables FIFO empty interrupt** 0: Disable 1: Enable
5	TARGET_LINE_INT_EN	**Enables target line interrupt** 0: Disable 1: Enable
4	FIFO_UNDERFLOW_INT_EN	**Enables FIFO underflow interrupt** 0: Disable 1: Enable
3	EOF_ABNORMAL_INT_EN	**Enables abnormal EOF interrupt** 0: Disable 1: Enable
2	FRAME_END_INT_EN	**Enables frame end interrupt** 0: Disable 1: Enable
1	FRAME_START_INT_EN	**Enables frame start interrupt** 0: Disable 1: Enable

Bit(s)	Name	Description
0	REG_UPDATE_INT_EN	**Enables working register update done interrupt** 0: Disable 1: Enable

1400F004 DISP_RDMA_INT_STATUS **RDMA Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										FIFO_EMPTY_INT_FLAG	TARGET_LINE_INT_FLAG	FIFO_UNDERFLOW_INT_FLAG	EOF_ABNORMAL_INT_FLAG	FRAME_END_INT_FLAG	FRAME_START_INT_FLAG	REG_UPDATE_INT_FLAG
Type										A1	A1	A1	A1	A1	A1	A1
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	FIFO_EMPTY_INT_FLAG	**FIFO empty interrupt status** If FIFO is empty, this flag will be asserted.
5	TARGET_LINE_INT_FLAG	**Target line interrupt status** If line number reach the target line, this flag will be asserted.
4	FIFO_UNDERFLOW_INT_FLAG	**FIFO underflow interrupt status** If FIFO underflow is enabled and FIFO is exhausted, this flag will be asserted.
3	EOF_ABNORMAL_INT_FLAG	**Abnormal EOF interrupt status** If EOF is coming but one frame is not finished, this flag will be asserted.
2	FRAME_END_INT_FLAG	**Frame end interrupt status**
1	FRAME_START_INT_FLAG	**Frame start interrupt status**
0	REG_UPDATE_INT_FLAG	**Working register update done interrupt status**

1400F010 DISP_RDMA_GLOBAL_CON **RDMA Global Control** **00000100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SMI_BUSY		RESET_STATE						SOFT_RESET			MODE_SEL	ENGINE_EN
Type				RU		RU						RW			RW	RW
Reset				0		0	0	1				0			0	0

Bit(s)	Name	Description
12	SMI_BUSY	**GMC busy** If GMC request is accepted but GMC data not yet completely returned, this bit will be asserted.

Bit(s)	Name	Description
		0: Idle 1: Busy
10:8	RESET_STATE	**Soft reset state machine**
4	SOFT_RESET	**Soft reset** Write 1 to soft reset and write 0 to it, the polling reset state machine will be done (0x1). 0: Disable soft reset 1: Enable soft reset
1	MODE_SEL	**Selects mode** 0: Direct link mode 1: Memory mode
0	ENGINE_EN	**Controls engine enabling** 0: Engine off 1: Engine on

1400F014 DISP_RDMA_SIZE_CON_0 **RDMA Size Control 0** **00B00280**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									MATRIX_INT_MTX_SEL					MATRIX_WIDE_GAMUT_EN	MATRIX_ENABLE	MATRIX_EXT_MTX_EN
Type									RW					RW	RW	RW
Reset									1	0	1	1		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OUTPUT_FRAME_WIDTH												
Type				RW												
Reset				0	0	0	1	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:20	MATRIX_INT_MTX_SEL	**Selects pre-defined color transform coefficient** 4'b0000: RGB to JPEG 4'b0010: RGB to BT601 4'b0011: RGB to BT709 4'b0100: JPEG to RGB 4'b0110: BT601 to RGB 4'b0111: BT709 to RGB 4'b1000: JPEG to BT601 4'b1001: JPEG to BT709 4'b1010: BT601 to JPEG 4'b1011: BT709 to JPEG 4'b1100: BT709 to BT601 4'b1101: BT601 to BT709
18	MATRIX_WIDE_GAMUT_EN	**When MATRIX_ENABLE, the output data can be chosen.** 0: sRGB [0:255] 1: ext-sRGB [-512:511]
17	MATRIX_ENABLE	**Enables color format transformation** The output data are XRGB or XYUV. 0: Bypass color matrix 1: Does color matrix transformation
16	MATRIX_EXT_MTX_EN	**Enables color transformation external coefficients or not**

Bit(s)	Name	Description
		For internal coefficient, use INT_MTX_SEL to select the pre-defined coefficients. 0: Use internal coefficients for color transformation 1: Use external coefficients for color transformation
12:0	OUTPUT_FRAME_WIDTH	**Width of output frame**

1400F018 DISP_RDMA_SIZE_CON_1 **RDMA Size Control 1** **000001E0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													OUTPUT_FRAME_HEIGHT			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OUTPUT_FRAME_HEIGHT															
Type	RW															
Reset	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0

Bit(s)	Name	Description
19:0	OUTPUT_FRAME_HEIGHT	Height of output frame

1400F01C DISP_RDMA_TARGET_LINE **RDMA Target Line** **000000F0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													TARGET_LINE			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TARGET_LINE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
19:0	TARGET_LINE	Target line number to interrupt

1400F024 DISP_RDMA_MEM_CON **RDMA Memory Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEM_MODE_HORI_BLOCK_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MEM_MODE_UV_COSITE	MEM_MODE_UV_UPSAMPLE				MEM_MODE_INPUT_SWAP	MEM_MODE_INPUT_FORMAT						MEM_MODE_TILE_INTERL	MEM_MODE_TILE_EN

															ACE	
Type			RW	RW				RW	RW						RW	RW
Reset			0	0				0	0	0	0	0			0	0

Bit(s)	Name	Description
31:24	MEM_MODE_HORI_BLOCK_NUM	**Block number in horizontal direction** Only for tile-based memory mode.
13	MEM_MODE_UV_COSITE	**If UV_UPSAMPLE is on, choose the pixel to be cosited or not.** 0: Non-cosited 1: Cosited
12	MEM_MODE_UV_UPSAMPLE	**If input format is YUV422, UV channel can be duplicated or averaged.** 0: Duplicated 1: Averaged
8	MEM_MODE_INPUT_SWAP	**Memory mode input format** The engine translates the memory data according to the format. For direct link mode, keep it to 0.
7:4	MEM_MODE_INPUT_FORMAT	**Memory mode input format** The engine translates the memory data according to the format. For direct link mode, keep it to 0. RGB565, RGB888, ARGB8888 and UYVY are supported.
1	MEM_MODE_TILE_INTERLACE	**If tile mode is enabled, the output frame can be selected to be progressive or interlaced.** 0: Progressive 1: Interlace
0	MEM_MODE_TILE_EN	**When memory mode is enabled, tile-base memory allocation is supported.** 0: Raster scan mode 1: Tile mode

1400F02C DISP_RDMA_MEM_SRC_PITCH — RDMA Memory Mode Line Pitch — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEM_MODE_SRC_PITCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	MEM_MODE_SRC_PITCH	**Memory mode source image pitch** Refer to the "Memory Mode Control" section.

1400F030 DISP_RDMA_MEM_GMC_SETTING_0 — RDMA Memory Mode GMC Setting 0 — 00400020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					PRE_ULTRA_THRESHOLD_HIGH											

Type					RW											
Reset					0	0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PRE_ULTRA_THRESHOLD_LOW											
Type					RW											
Reset					0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
27:16	PRE_ULTRA_THRESHOLD_HIGH	
11:0	PRE_ULTRA_THRESHOLD_LOW	Unit: 16 bytes

1400F034 DISP_RDMA_MEM_GMC_SETTING_1 — RDMA Memory Mode GMC Setting 1 — 00300010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					ULTRA_THRESHOLD_HIGH											
Type					RW											
Reset					0	0	0	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ULTRA_THRESHOLD_LOW											
Type					RW											
Reset					0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
27:16	ULTRA_THRESHOLD_HIGH	Unit: 16 bytes
11:0	ULTRA_THRESHOLD_LOW	

1400F038 DISP_RDMA_MEM_SLOW_CON — RDMA Memory Mode Slow Control — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEM_MODE_SLOW_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MEM_MODE_SLOW_EN
Type																RW
Reset																0

Bit(s)	Name	Description
31:16	MEM_MODE_SLOW_COUNT	**GMC request slow-down counter** When MEM_MODE_SLOW_EN is 1, GMC request will not be continuous and the interval controlled by this register. Unit: Engine clock cycle time
0	MEM_MODE_SLOW_EN	**Enables GMC request slow-down** The bandwidth usage can be limited by this bit. 0: Disable slow-down

Bit(s)	Name	Description
		1: Enable slow-down

1400F03C DISP_RDMA_MEM_GMC_SETTING_2 — **RDMA Memory Mode GMC Setting 2** — **00000010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ISSUE_REQ_THRESHOLD											
Type					RW											
Reset					0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
11:0	ISSUE_REQ_THRESHOLD	

1400F040 DISP_RDMA_FIFO_CON — **RDMA FIFO Control** — **02000010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_UNDERFLOW_EN				FIFO_PSEUDO_SIZE											
Type	RW				RW											
Reset	0				0	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					OUTPUT_VALID_FIFO_THRESHOLD											
Type					RW											
Reset					0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31	FIFO_UNDERFLOW_EN	**Enables FIFO underflow** If FIFO is exhausted, the data output will be stopped. If the downstream engines need the non-blocked data, set up this bit; it will keep the non-blocked output, but the data will not be correct. 0: Disable underflow 1: Enable underflow
27:16	FIFO_PSEUDO_SIZE	**FIFO pseudo size depending on the SRAM size.** Unit: 16 bytes. In Jade, the recommended FIFO size is 512 (RDMA0), or 256 (RDMA1), and if mdp_wrot's SRAM can be used, it could be set 2048.
11:0	OUTPUT_VALID_FIFO_THRESHOLD	**Controls FIFO output threshold** Unit: 16 bytes. The register can hold the output data until the amount of data is over the threshold.

1400F044 DISP_RDMA_ — **RDMA_FIFO_LOG** — **00000FFF**

FIFO_LOG

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RDMA_FIFO_LOG											
Type					RU											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
11:0	RDMA_FIFO_LOG	FIFO minimal depth

1400F054 DISP_RDMA_C00 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C00												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C00	**Color matrix parameter** Refer to the "Color Matrix" section.

1400F058 DISP_RDMA_C01 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C01												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C01	**Color matrix parameter** Refer to the "Color Matrix" section.

1400F05C DISP_RDMA_C02 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C02												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C02	**Color matrix parameter** Refer to the "Color Matrix" section.

1400F060 DISP_RDMA_C10 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C10												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C10	**Color matrix parameter** Refer to the "Color Matrix" section.

1400F064 DISP_RDMA_C11 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C11												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C11	**Color matrix parameter** Refer to the "Color Matrix" section.

1400F068 DISP_RDMA_C12 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C12												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C12	**Color matrix parameter** Refer to the "Color Matrix" section.

1400F06C DISP_RDMA_C20 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C20												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C20	**Color matrix parameter** Refer to the "Color Matrix" section.

1400F070 DISP_RDMA_C21 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C21												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C21	**Color matrix parameter** Refer to the "Color Matrix" section.

1400F074 DISP_RDMA_C22 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C22												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C22	**Color matrix parameter** Refer to the "Color Matrix" section.

1400F078 DISP_RDMA_PRE_ADD_0 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DISP_RDMA_PRE_ADD_0								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	DISP_RDMA_PRE_ADD_0	**Color matrix parameter** Refer to the "Color Matrix" section.

1400F07C DISP_RDMA_PRE_ADD_1 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DISP_RDMA_PRE_ADD_1								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	DISP_RDMA_PRE_ADD_1	**Color matrix parameter** Refer to the "Color Matrix" section.

1400F080 DISP_RDMA_PRE_ADD_2 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DISP_RDMA_PRE_ADD_2								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	DISP_RDMA_PRE_ADD_2	**Color matrix parameter** Refer to the "Color Matrix" section.

1400F084 DISP_RDMA_POST_ADD_0 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DISP_RDMA_POST_ADD_0								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	DISP_RDMA_POST_ADD_0	**Color matrix parameter** Refer to the "Color Matrix" section.

1400F088 DISP_RDMA_POST_ADD_1 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DISP_RDMA_POST_ADD_1								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	DISP_RDMA_POST_ADD_1	**Color matrix parameter** Refer to the "Color Matrix" section.

1400F08C DISP_RDMA_POST_ADD_2 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name								DISP_RDMA_POST_ADD_2								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	DISP_RDMA_POST_ADD_2	**Color matrix parameter** Refer to the "Color Matrix" section.

1400F090 DISP_RDMA_DUMMY — RDMA Dummy Register — FFF00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DISP_RDMA_DUMMY															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_RDMA_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DISP_RDMA_DUMMY	Reserved

1400F094 DISP_RDMA_DEBUG_OUT_SEL — RDMA Debug Output Selection — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DISP_RDMA_DEBUG_OUT_SEL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	DISP_RDMA_DEBUG_OUT_SEL	Reserved

1400FF00 DISP_RDMA_MEM_START_ADDR — RDMA Memory Mode Start Address — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEM_MODE_START_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEM_MODE_START_ADDR															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEM_MODE_START_ADDR	**Memory mode start address** Refer to the "Memory Mode Control" section.

1400F0A0 DISP_RDMA_BG_CON_0 — Add Black Frame Outside of Image — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DISP_RDMA_BG_RIGHT												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_BG_LEFT												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	DISP_RDMA_BG_RIGHT	bg_right parameter
12:0	DISP_RDMA_BG_LEFT	bg_left parameter

1400F0A4 DISP_RDMA_BG_CON_1 — Add Black Frame Outside of Image — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DISP_RDMA_BG_BOTTOM												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_BG_TOP												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	DISP_RDMA_BG_BOTTOM	bg_bottom parameter
12:0	DISP_RDMA_BG_TOP	bg_top parameter

1400F0A8 DISP_RDMA_THRESHOLD_FOR_SODI — RDMA Threshold Setting for SODI — 00400020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DISP_RDMA_THRESHOLD_HIGH_FOR_SODI											
Type					RW											
Reset					0	0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DISP_RDMA_THRESHOLD_LOW_FOR_SODI											

Type					RW											
Reset					0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
27:16	DISP_RDMA_THRESHOLD_HIGH_FOR_SODI	Threshold high parameter for SODI
11:0	DISP_RDMA_THRESHOLD_LOW_FOR_SODI	Threshold low parameter for SODI

1400F0AC DISP_RDMA_THRESHOLD_FOR_DVFS — RDMA Threshold Setting for DVFS — 00400020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DISP_RDMA_THRESHOLD_HIGH_FOR_DVFS											
Type					RW											
Reset					0	0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DISP_RDMA_THRESHOLD_LOW_FOR_DVFS											
Type					RW											
Reset					0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
27:16	DISP_RDMA_THRESHOLD_HIGH_FOR_DVFS	Threshold high parameter for DVFS
11:0	DISP_RDMA_THRESHOLD_LOW_FOR_DVFS	Threshold low parameter for DVFS

1400F0B0 DISP_RDMA_SRAM_SEL — RDMA SRAM Selection — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DISP_RDMA_SRAM_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	DISP_RDMA_SRAM_SEL	**Selects SRAM** 0: DISP_RDMA SRAM 1: MDP_WROT SRAM

1400F0B4 DISP_RDMA_STALL_CG_C — RDMA Internal Stall Clock Gated Configuration — 00000000

ON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DISP_RDMA_MEM_CG	DISP_RDMA_REG_CG	DISP_RDMA_RELAY_CG	DISP_RDMA_FENG_CK_EN_CG	DISP_RDMA_FRAME_CTL_SHARED_BUF_CG	DISP_RDMA_FRAME_CTL_CG	DISP_RDMA_PRE_ENG_CG	DISP_RDMA_GMC_ENG_CG	DISP_RDMA_LINE_BUF_CG	DISP_RDMA_ASYNC_WRITE_CG	DISP_RDMA_ASYNC_READ_CG	DISP_RDMA_POST_ENG_CG
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	DISP_RDMA_MEM_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on
10	DISP_RDMA_REG_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on
9	DISP_RDMA_RELAY_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on
8	DISP_RDMA_FENG_CK_EN_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on
7	DISP_RDMA_FRAME_CTL_SHARED_BUF_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on
6	DISP_RDMA_FRAME_CTL_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on
5	DISP_RDMA_PRE_ENG_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on
4	DISP_RDMA_GMC_ENG_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on
3	DISP_RDMA_LINE_BUF_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on
2	DISP_RDMA_ASYNC_WRITE_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on
1	DISP_RDMA_ASYNC_READ_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on
0	DISP_RDMA_POST_ENG_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on

Module name: DISP_RDMA1 Base address: (+14010000h)

Address	Name	Width	Register Function
14010000	DISP_RDMA_INT_ENABLE	32	RDMA Interrupt Enable
14010004	DISP_RDMA_INT_STATUS	32	RDMA Interrupt Status
14010010	DISP_RDMA_GLOBAL_CON	32	RDMA Global Control
14010014	DISP_RDMA_SIZE_CON_0	32	RDMA Size Control 0
14010018	DISP_RDMA_SIZE_CON_1	32	RDMA Size Control 1
1401001C	DISP_RDMA_TARGET_LINE	32	RDMA Target Line
14010024	DISP_RDMA_MEM_CON	32	RDMA Memory Mode Control
1401002C	DISP_RDMA_MEM_SRC_PITCH	32	RDMA Memory Mode Line Pitch
14010030	DISP_RDMA_MEM_GMC_SETTING_0	32	RDMA Memory Mode GMC Setting 0
14010034	DISP_RDMA_MEM_GMC_SETTING_1	32	RDMA Memory Mode GMC Setting 1
14010038	DISP_RDMA_MEM_SLOW_CON	32	RDMA Memory Mode Slow Control
1401003C	DISP_RDMA_MEM_GMC_SETTING_2	32	RDMA Memory Mode GMC Setting 2
14010040	DISP_RDMA_FIFO_CON	32	RDMA FIFO Control
14010044	DISP_RDMA_FIFO_LOG	32	RDMA_FIFO_LOG
14010054	DISP_RDMA_C00	32	RDMA YUV to RGB Coefficient
14010058	DISP_RDMA_C01	32	RDMA YUV to RGB Coefficient
1401005C	DISP_RDMA_C02	32	RDMA YUV to RGB Coefficient
14010060	DISP_RDMA_C10	32	RDMA YUV to RGB Coefficient
14010064	DISP_RDMA_C11	32	RDMA YUV to RGB Coefficient
14010068	DISP_RDMA_C12	32	RDMA YUV to RGB Coefficient
1401006C	DISP_RDMA_C20	32	RDMA YUV to RGB Coefficient
14010070	DISP_RDMA_C21	32	RDMA YUV to RGB Coefficient
14010074	DISP_RDMA_C22	32	RDMA YUV to RGB Coefficient
14010078	DISP_RDMA_PRE_ADD_0	32	RDMA YUV to RGB Coefficient
1401007C	DISP_RDMA_PRE_ADD_1	32	RDMA YUV to RGB Coefficient
14010080	DISP_RDMA_PRE_ADD_2	32	RDMA YUV to RGB Coefficient
14010084	DISP_RDMA_POST_ADD_0	32	RDMA YUV to RGB Coefficient
14010088	DISP_RDMA_POST_ADD_1	32	RDMA YUV to RGB Coefficient
1401008C	DISP_RDMA_POST_ADD_2	32	RDMA YUV to RGB Coefficient
14010090	DISP_RDMA_DUMMY	32	RDMA Dummy Register

Address	Name	Width	Register Function
14010094	DISP_RDMA_DEBUG_OUT_SEL	32	RDMA Debug Output Selection
14010F00	DISP_RDMA_MEM_START_ADDR	32	RDMA Memory Mode Start Address
140100A0	DISP_RDMA_BG_CON_0	32	Add Black Frame Outside of Image
140100A4	DISP_RDMA_BG_CON_1	32	Add Black Frame Outside of Image
140100A8	DISP_RDMA_THRESHOLD_FOR_SODI	32	RDMA Threshold Setting for SODI
140100AC	DISP_RDMA_THRESHOLD_FOR_DVFS	32	RDMA Threshold Setting for DVFS
140100B0	DISP_RDMA_SRAM_SEL	32	RDMA SRAM Selection
140100B4	DISP_RDMA_STALL_CG_CON	32	RDMA Internal Stall Clock Gated Configuration

14010000 DISP_RDMA_INT_ENABLE RDMA Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										FIFO_EMPTY_INT_EN	TARGET_LINE_INT_EN	FIFO_UNDERFLOW_INT_EN	EOF_ABNORMAL_INT_EN	FRAME_END_INT_EN	FRAME_START_INT_EN	REG_UPDATE_INT_EN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	FIFO_EMPTY_INT_EN	**Enables FIFO empty interrupt** 0: Disable 1: Enable
5	TARGET_LINE_INT_EN	**Enables target line interrupt** 0: Disable 1: Enable
4	FIFO_UNDERFLOW_INT_EN	**Enables FIFO underflow interrupt** 0: Disable 1: Enable
3	EOF_ABNORMAL_INT_EN	**Enables abnormal EOF interrupt** 0: Disable 1: Enable
2	FRAME_END_INT_EN	**Enables frame end interrupt** 0: Disable 1: Enable
1	FRAME_START_INT_EN	**Enables frame start interrupt** 0: Disable 1: Enable

Bit(s)	Name	Description
0	REG_UPDATE_INT_EN	**Enables working register update done interrupt** 0: Disable 1: Enable

14010004 DISP_RDMA_INT_STATUS **RDMA Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										FIFO_EMPTY_INT_FLAG	TARGET_LINE_INT_FLAG	FIFO_UNDERFLOW_INT_FLAG	EOF_ABNORMAL_INT_FLAG	FRAME_END_INT_FLAG	FRAME_START_INT_FLAG	REG_UPDATE_INT_FLAG
Type										A1	A1	A1	A1	A1	A1	A1
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	FIFO_EMPTY_INT_FLAG	**FIFO empty interrupt status** If FIFO is empty, this flag will be asserted.
5	TARGET_LINE_INT_FLAG	**Target line interrupt status** If line number reach the target line, this flag will be asserted.
4	FIFO_UNDERFLOW_INT_FLAG	**FIFO underflow interrupt status** If FIFO underflow is enabled and FIFO is exhausted, this flag will be asserted.
3	EOF_ABNORMAL_INT_FLAG	**Abnormal EOF interrupt status** If EOF is coming but one frame is not finished, this flag will be asserted.
2	FRAME_END_INT_FLAG	**Frame end interrupt status**
1	FRAME_START_INT_FLAG	**Frame start interrupt status**
0	REG_UPDATE_INT_FLAG	**Working register update done interrupt status**

14010010 DISP_RDMA_GLOBAL_CON **RDMA Global Control** **00000100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SMI_BUSY		RESET_STATE						SOFT_RESET			MODE_SEL	ENGINE_EN
Type				RU		RU						RW			RW	RW
Reset				0		0	0	1				0			0	0

Bit(s)	Name	Description
12	SMI_BUSY	**GMC busy** If GMC request is accepted but GMC data not yet completely

Bit(s)	Name	Description
		returned, this bit will be asserted. 0: Idle 1: Busy
10:8	RESET_STATE	**Soft reset state machine**
4	SOFT_RESET	**Soft reset** Write 1 to soft reset and write 0 to it, the polling reset state machine will be done (0x1). 0: Disable soft reset 1: Enable soft reset
1	MODE_SEL	**Selects mode** 0: Direct link mode 1: Memory mode
0	ENGINE_EN	**Controls engine enabling** 0: Engine off 1: Engine on

14010014 DISP_RDMA_SIZE_CON_0 **RDMA Size Control 0** **00B00280**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									MATRIX_INT_MTX_SEL					MATRIX_WIDE_GAMUT_EN	MATRIX_ENABLE	MATRIX_EXT_MTX_EN
Type									RW					RW	RW	RW
Reset									1	0	1	1		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OUTPUT_FRAME_WIDTH												
Type				RW												
Reset				0	0	0	1	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:20	MATRIX_INT_MTX_SEL	**Selects pre-defined color transform coefficient** 4'b0000: RGB to JPEG 4'b0010: RGB to BT601 4'b0011: RGB to BT709 4'b0100: JPEG to RGB 4'b0110: BT601 to RGB 4'b0111: BT709 to RGB 4'b1000: JPEG to BT601 4'b1001: JPEG to BT709 4'b1010: BT601 to JPEG 4'b1011: BT709 to JPEG 4'b1100: BT709 to BT601 4'b1101: BT601 to BT709
18	MATRIX_WIDE_GAMUT_EN	**When MATRIX_ENABLE, the output data can be chosen.** 0: sRGB [0:255] 1: ext-sRGB [-512:511]
17	MATRIX_ENABLE	**Enables color format transformation** The output data are XRGB or XYUV. 0: Bypass color matrix

Bit(s)	Name	Description
		1: Does color matrix transformation
16	MATRIX_EXT_MTX_EN	**Enables color transformation external coefficients or not** For internal coefficient, use INT_MTX_SEL to select the pre-defined coefficients. 0: Use internal coefficients for color transformation 1: Use external coefficients for color transformation
12:0	OUTPUT_FRAME_WIDTH	**Width of output frame**

14010018 DISP_RDMA_SIZE_CON_1 **RDMA Size Control 1** **000001E0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													OUTPUT_FRAME_HEIGHT			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OUTPUT_FRAME_HEIGHT															
Type	RW															
Reset	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0

Bit(s)	Name	Description
19:0	OUTPUT_FRAME_HEIGHT	Height of output frame

1401001C DISP_RDMA_TARGET_LINE **RDMA Target Line** **000000F0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													TARGET_LINE			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TARGET_LINE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
19:0	TARGET_LINE	Target line number to interrupt

14010024 DISP_RDMA_MEM_CON **RDMA Memory Mode Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEM_MODE_HORI_BLOCK_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name			MEM_MODE_UV_COSITE	MEM_MODE_UV_UPSAMPLE				MEM_MODE_INPUT_SWAP	MEM_MODE_INPUT_FORMAT						MEM_MODE_TILE_INTERLACE	MEM_MODE_TILE_EN
Type			RW	RW				RW	RW						RW	RW
Reset			0	0				0	0	0	0	0			0	0

Bit(s)	Name	Description
31:24	MEM_MODE_HORI_BLOCK_NUM	**Block number in horizontal direction** Only for tile-based memory mode.
13	MEM_MODE_UV_COSITE	**If UV_UPSAMPLE is on, choose the pixel to be cosited or not.** 0: Non-cosited 1: Cosited
12	MEM_MODE_UV_UPSAMPLE	**If input format is YUV422, UV channel can be duplicated or averaged.** 0: Duplicated 1: Averaged
8	MEM_MODE_INPUT_SWAP	**Memory mode input format** The engine translates the memory data according to the format. For direct link mode, keep it to 0.
7:4	MEM_MODE_INPUT_FORMAT	**Memory mode input format** The engine translates the memory data according to the format. For direct link mode, keep it to 0. RGB565, RGB888, ARGB8888 and UYVY are supported.
1	MEM_MODE_TILE_INTERLACE	**If tile mode is enabled, the output frame can be selected to be progressive or interlaced.** 0: Progressive 1: Interlace
0	MEM_MODE_TILE_EN	**When memory mode is enabled, tile-base memory allocation is supported.** 0: Raster scan mode 1: Tile mode

1401002C DISP_RDMA_MEM_SRC_PITCH RDMA Memory Mode Line Pitch 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEM_MODE_SRC_PITCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	MEM_MODE_SRC_PITCH	**Memory mode source image pitch** Refer to the "Memory Mode Control" section.

14010030 DISP_RDMA_MEM_GMC_SETTING_0 — **RDMA Memory Mode GMC Setting 0** — **00400020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					PRE_ULTRA_THRESHOLD_HIGH											
Type					RW											
Reset					0	0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PRE_ULTRA_THRESHOLD_LOW											
Type					RW											
Reset					0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
27:16	PRE_ULTRA_THRESHOLD_HIGH	
11:0	PRE_ULTRA_THRESHOLD_LOW	Unit: 16 bytes

14010034 DISP_RDMA_MEM_GMC_SETTING_1 — **RDMA Memory Mode GMC Setting 1** — **00300010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					ULTRA_THRESHOLD_HIGH											
Type					RW											
Reset					0	0	0	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ULTRA_THRESHOLD_LOW											
Type					RW											
Reset					0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
27:16	ULTRA_THRESHOLD_HIGH	Unit: 16 bytes
11:0	ULTRA_THRESHOLD_LOW	

14010038 DISP_RDMA_MEM_SLOW_CON — **RDMA Memory Mode Slow Control** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEM_MODE_SLOW_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MEM_MODE_SLOW_EN
Type																RW
Reset																0

Bit(s)	Name	Description
31:16	MEM_MODE_SLOW_COUNT	**GMC request slow-down counter** When MEM_MODE_SLOW_EN is 1, GMC request will not be continuous and the interval controlled by this register. Unit: Engine clock cycle time
0	MEM_MODE_SLOW_EN	**Enables GMC request slow-down** The bandwidth usage can be limited by this bit. 0: Disable slow-down 1: Enable slow-down

1401003C DISP_RDMA_MEM_GMC_SETTING_2 **RDMA Memory Mode GMC Setting 2** **00000010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ISSUE_REQ_THRESHOLD											
Type					RW											
Reset					0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
11:0	ISSUE_REQ_THRESHOLD	

14010040 DISP_RDMA_FIFO_CON **RDMA FIFO Control** **02000010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_UNDERFLOW_EN				FIFO_PSEUDO_SIZE											
Type	RW				RW											
Reset	0				0	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					OUTPUT_VALID_FIFO_THRESHOLD											
Type					RW											
Reset					0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31	FIFO_UNDERFLOW_EN	**Enables FIFO underflow** If FIFO is exhausted, the data output will be stopped. If the downstream engines need the non-blocked data, set up this bit; it will keep the non-blocked output, but the data will not be correct. 0: Disable underflow 1: Enable underflow
27:16	FIFO_PSEUDO_SIZE	**FIFO pseudo size depending on the SRAM size.** Unit: 16 bytes. In Jade, the recommended FIFO size is 512

Bit(s)	Name	Description
11:0	OUTPUT_VALID_FIFO_THRESHOLD	(RDMA0), or 256 (RDMA1), and if mdp_wrot's SRAM can be used, it could be set 2048. **Controls FIFO output threshold** Unit: 16 bytes. The register can hold the output data until the amount of data is over the threshold.

14010044 DISP_RDMA_FIFO_LOG RDMA_FIFO_LOG 00000FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RDMA_FIFO_LOG											
Type					RU											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
11:0	RDMA_FIFO_LOG	FIFO minimal depth

14010054 DISP_RDMA_C00 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C00												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C00	**Color matrix parameter** Refer to the "Color Matrix" section.

14010058 DISP_RDMA_C01 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C01												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C01	**Color matrix parameter** Refer to the "Color Matrix" section.

1401005C DISP_RDMA_C02 **RDMA YUV to RGB Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C02												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C02	**Color matrix parameter** Refer to the "Color Matrix" section.

14010060 DISP_RDMA_C10 **RDMA YUV to RGB Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C10												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C10	**Color matrix parameter** Refer to the "Color Matrix" section.

14010064 DISP_RDMA_C11 **RDMA YUV to RGB Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C11												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C11	**Color matrix parameter** Refer to the "Color Matrix" section.

14010068 DISP_RDMA_C12 **RDMA YUV to RGB Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C12												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C12	**Color matrix parameter** Refer to the "Color Matrix" section.

1401006C DISP_RDMA_C20 **RDMA YUV to RGB Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C20												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C20	**Color matrix parameter** Refer to the "Color Matrix" section.

14010070 DISP_RDMA_C21 **RDMA YUV to RGB Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C21												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C21	**Color matrix parameter** Refer to the "Color Matrix" section.

14010074 DISP_RDMA_C22 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_C22												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DISP_RDMA_C22	**Color matrix parameter** Refer to the "Color Matrix" section.

14010078 DISP_RDMA_PRE_ADD_0 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DISP_RDMA_PRE_ADD_0								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	DISP_RDMA_PRE_ADD_0	**Color matrix parameter** Refer to the "Color Matrix" section.

1401007C DISP_RDMA_PRE_ADD_1 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DISP_RDMA_PRE_ADD_1								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	DISP_RDMA_PRE_ADD_1	**Color matrix parameter** Refer to the "Color Matrix" section.

14010080 DISP_RDMA_PRE_ADD_2 **RDMA YUV to RGB Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DISP_RDMA_PRE_ADD_2								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	DISP_RDMA_PRE_ADD_2	**Color matrix parameter** Refer to the "Color Matrix" section.

14010084 DISP_RDMA_POST_ADD_0 **RDMA YUV to RGB Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DISP_RDMA_POST_ADD_0								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	DISP_RDMA_POST_ADD_0	**Color matrix parameter** Refer to the "Color Matrix" section.

14010088 DISP_RDMA_POST_ADD_1 **RDMA YUV to RGB Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DISP_RDMA_POST_ADD_1								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	DISP_RDMA_POST_ADD_1	**Color matrix parameter** Refer to the "Color Matrix" section.

1401008C DISP_RDMA_POST_ADD_2 RDMA YUV to RGB Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DISP_RDMA_POST_ADD_2								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	DISP_RDMA_POST_ADD_2	**Color matrix parameter** Refer to the "Color Matrix" section.

14010090 DISP_RDMA_DUMMY RDMA Dummy Register FFF00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DISP_RDMA_DUMMY															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DISP_RDMA_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DISP_RDMA_DUMMY	**Reserved**

14010094 DISP_RDMA_DEBUG_OUT_SEL RDMA Debug Output Selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DISP_RDMA_DEBUG_OUT_SEL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	DISP_RDMA_DEBUG_OUT_SEL	**Reserved**

14010F00 DISP_RDMA_MEM_START_ADDR **RDMA Memory Mode Start Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEM_MODE_START_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEM_MODE_START_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEM_MODE_START_ADDR	**Memory mode start address** Refer to the "Memory Mode Control" section.

140100A0 DISP_RDMA_BG_CON_0 **Add Black Frame Outside of Image** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DISP_RDMA_BG_RIGHT												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_BG_LEFT												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	DISP_RDMA_BG_RIGHT	bg_right parameter
12:0	DISP_RDMA_BG_LEFT	bg_left parameter

140100A4 DISP_RDMA_BG_CON_1 **Add Black Frame Outside of Image** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DISP_RDMA_BG_BOTTOM												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DISP_RDMA_BG_TOP												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	DISP_RDMA_BG_BOTTOM	bg_bottom parameter
12:0	DISP_RDMA_BG_TOP	bg_top parameter

140100A8 DISP_RDMA_THRESHOLD_FOR_SODI — RDMA Threshold Setting for SODI — 00400020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DISP_RDMA_THRESHOLD_HIGH_FOR_SODI											
Type					RW											
Reset					0	0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DISP_RDMA_THRESHOLD_LOW_FOR_SODI											
Type					RW											
Reset					0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
27:16	DISP_RDMA_THRESHOLD_HIGH_FOR_SODI	Threshold high parameter for SODI
11:0	DISP_RDMA_THRESHOLD_LOW_FOR_SODI	Threshold low parameter for SODI

140100AC DISP_RDMA_THRESHOLD_FOR_DVFS — RDMA Threshold Setting for DVFS — 00400020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DISP_RDMA_THRESHOLD_HIGH_FOR_DVFS											
Type					RW											
Reset					0	0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DISP_RDMA_THRESHOLD_LOW_FOR_DVFS											
Type					RW											
Reset					0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
27:16	DISP_RDMA_THRESHOLD_HIGH_FOR_DVFS	Threshold high parameter for DVFS
11:0	DISP_RDMA_THRESHOLD_LOW_FOR_DVFS	Threshold low parameter for DVFS

140100B0 DISP_RDMA_SRAM_SEL — RDMA SRAM Selection — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DISP_RDMA_SRAM_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	DISP_RDMA_SRAM_SEL	**Selects SRAM** 0: DISP_RDMA SRAM 1: MDP_WROT SRAM

140100B4 DISP_RDMA_STALL_CG_CON — RDMA Internal Stall Clock Gated Configuration — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DISP_RDMA_MEM_CG	DISP_RDMA_REG_CG	DISP_RDMA_RELAY_CG	DISP_RDMA_FENG_CK_EN_CG	DISP_RDMA_FRAME_CTL_SHARED_BUF_CG	DISP_RDMA_FRAME_CTL_CG	DISP_RDMA_PRE_ENG_CG	DISP_RDMA_GMC_ENG_CG	DISP_RDMA_LINE_BUF_CG	DISP_RDMA_ASYNC_WRITE_CG	DISP_RDMA_ASYNC_READ_CG	DISP_RDMA_POST_ENG_CG
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	DISP_RDMA_MEM_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on
10	DISP_RDMA_REG_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on
9	DISP_RDMA_RELAY_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on
8	DISP_RDMA_FENG_CK_EN_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on
7	DISP_RDMA_FRAME_CTL_SHARED_BUF_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on
6	DISP_RDMA_FRAME_CTL_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on
5	DISP_RDMA_PRE_ENG_CG	**Enables submodule clock gated**

Bit(s)	Name	Description
		0: CG on, CLK off 1: CG off, CLK on
4	DISP_RDMA_GMC_ENG_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on
3	DISP_RDMA_LINE_BUF_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on
2	DISP_RDMA_ASYNC_WRITE_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on
1	DISP_RDMA_ASYNC_READ_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on
0	DISP_RDMA_POST_ENG_CG	**Enables submodule clock gated** 0: CG on, CLK off 1: CG off, CLK on

Module name: MDP_WDMA Base address: (+14006000h)

Address	Name	Width	Register Function
14006000	**WDMA_INTEN**	32	WDMA Interrupt Enable
14006004	**WDMA_INTSTA**	32	WDMA Interrupt Status
14006008	**WDMA_EN**	32	WDMA Enable
1400600C	**WDMA_RST**	32	WDMA Reset
14006010	**WDMA_SMI_CON**	32	WDMA SMI Control
14006014	**WDMA_CFG**	32	WDMA Config Register
14006018	**WDMA_SRC_SIZE**	32	WDMA Source Size Register
1400601C	**WDMA_CLIP_SIZE**	32	WDMA Clip Size Register
14006020	**WDMA_CLIP_COORD**	32	WDMA Clip Coordinate Register
14006028	**WDMA_DST_W_IN_BYTE**	32	WDMA Destination Width in Byte
1400602C	**WDMA_ALPHA**	32	WDMA Alpha
14006038	**WDMA_BUF_CON1**	32	WDMA Buffer Control 1
1400603C	**WDMA_BUF_CON2**	32	WDMA Buffer Control 2
14006040	**WDMA_C00**	32	WDMA Matrix Coefficient
14006044	**WDMA_C02**	32	WDMA Matrix Coefficient
14006048	**WDMA_C10**	32	WDMA Matrix Coefficient
1400604C	**WDMA_C12**	32	WDMA Matrix Coefficient
14006050	**WDMA_C20**	32	WDMA Matrix Coefficient
14006054	**WDMA_C22**	32	WDMA Matrix Coefficient
14006058	**WDMA_PRE_ADD0**	32	WDMA Matrix Coefficient
1400605C	**WDMA_PRE_ADD2**	32	WDMA Matrix Coefficient
14006060	**WDMA_POST_ADD0**	32	WDMA Matrix Coefficient
14006064	**WDMA_POST_ADD2**	32	WDMA Matrix Coefficient
14006078	**WDMA_DST_UV_PITCH**	32	WDMA UV Destination Width in Byte

Address	Name	Width	Register Function
14006080	WDMA_DST_ADDR_OFFSET0	32	WDMA Destination Address Offset 0
14006084	WDMA_DST_ADDR_OFFSET1	32	WDMA Destination Address Offset 1
14006088	WDMA_DST_ADDR_OFFSET2	32	WDMA Destination Address Offset 2
14006090	PROC_TRACK_CON_0	32	DMA Processing Tracking Control 0
14006094	PROC_TRACK_CON_1	32	DMA Processing Tracking Control 1
14006098	PROC_TRACK_CON_2	32	DMA Processing Tracking Control 2
140060A0	WDMA_FLOW_CTRL_DBG	32	WDMA Debug Port of flow_ctrl
140060A4	WDMA_EXEC_DBG	32	WDMA Debug Port of Exec Count
140060A8	WDMA_CT_DBG	32	WDMA Debug Port of Input Counter
140060AC	WDMA_SMI_TRAFFIC_DBG	32	WDMA Debug Port for SMI Traffic
140060B0	WDMA_PROC_TRACK_DBG_0	32	WDMA Debug Port for Process Track 0
140060B4	WDMA_PROC_TRACK_DBG_1	32	WDMA Debug Port for Process Track 1
140060B8	WDMA_DEBUG	32	WDMA Debug Port
14006100	WDMA_DUMMY	32	WDMA Dummy Register
14006E00	WDMA_DITHER_0	32	WDMA Dithering Control Register 0
14006E14	WDMA_DITHER_5	32	WDMA Dithering Control Register 5
14006E18	WDMA_DITHER_6	32	WDMA Dithering Control Register 6
14006E1C	WDMA_DITHER_7	32	WDMA Dithering Control Register 7
14006E20	WDMA_DITHER_8	32	WDMA Dithering Control Register 8
14006E24	WDMA_DITHER_9	32	WDMA Dithering Control Register 9
14006E28	WDMA_DITHER_10	32	WDMA Dithering Control Register 10
14006E2C	WDMA_DITHER_11	32	WDMA Dithering Control Register 11
14006E30	WDMA_DITHER_12	32	WDMA Dithering Control Register 12
14006E34	WDMA_DITHER_13	32	WDMA Dithering Control Register 13
14006E38	WDMA_DITHER_14	32	WDMA Dithering Control Register 14
14006E3C	WDMA_DITHER_15	32	WDMA Dithering Control Register 15
14006E40	WDMA_DITHER_16	32	WDMA Dithering Control Register 16
14006E44	WDMA_DITHER_17	32	WDMA Dithering Control Register 17
14006F00	WDMA_DST_ADDR0	32	WDMA Destination Address 0
14006F04	WDMA_DST_ADDR1	32	WDMA Destination Address 1
14006F08	WDMA_DST_ADDR2	32	WDMA Destination Address 2

14006000 WDMA_INTEN **WDMA Interrupt Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name															Frame_Underrun	Frame_Complete
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	**FUE**	Frame_Underrun	**Enables frame underrun interrupt** 0: Disable interrupt 1: Enable interrupt
0	**FCE**	Frame_Complete	**Enables frame completed interrupt** 0: Disable interrupt 1: Enable interrupt

14006004 WDMA_INTSTA **WDMA Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															Frame_Underrun	Frame_Complete
Type															A1	A1
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	**FU**	Frame_Underrun	**Incompletes one frame when WDMA receives EOF** SW writes this bit to clear IRQ. 0: WDMA idle or busy 1: WDMA incompletes one frame
0	**FC**	Frame_Complete	**Completes one frame before WDMA receives EOF** SW writes this bit to clear IRQ. 0: WDMA idle or busy 1: WDMA completes one frame

14006008 WDMA_EN **WDMA Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																Enable
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**EN**	Enable	**Enables WDMA or not** 0: Disable WDMA 1: Enable WDMA

1400600C WDMA_RST WDMA Reset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																Soft_Reset
Type																AO
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**RST**	Soft_Reset	**Soft reset to WDMA** Write this bit to trigger soft reset. WDMA will reset itself when bus transaction is done. SW must keep polling bit 0 of register WDMA_FLOW_CTRL_DBG until it is 1 to determine if the reset flow is done. 0: Write: No effect; Read: Reset is done . 1: Write: Trigger reset; Read: Reset is on-going.

14006010 WDMA_SMI_CON WDMA SMI Control 02240007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					SMI_V_REPEAT_NUM				SMI_U_REPEAT_NUM				SMI_Y_REPEAT_NUM			
Type					RW				RW				RW			
Reset					0	0	1	0	0	0	1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Slow_Count								Slow_Level			Slow_Enable	Threshold			
Type	RW								RW			RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
27:24	**V_NUM**	SMI_V_REPEAT_NUM	**Number of continuous V SMI commands** Only takes effects when out_format=YV12/NV12/NV21.
23:20	**U_NUM**	SMI_U_REPEAT_NUM	**Number of continuous U SMI commands** Only takes effects when out_format=YV12/NV12/NV21.
19:16	**Y_NUM**	SMI_Y_REPEAT_NUM	**Number of continuous Y SMI commands** Only takes effects when out_format=YV12/NV12/NV21.
15:8	**SC**	Slow_Count	**Slow-down counter of each write request** The actual slow-down count of each request is (slow_count*slow_level).
7:5	**SL**	Slow_Level	**Slow-down level of each write request** 0: slow_level=1 1: slow_level=2

Bit(s)	Mnemonic	Name	Description
			2: slow_level=4 4: slow_level=8
4	**SE**	Slow_Enable	**Enables slow-down of each write request or not** 0: Disable slow-down 1: Enable slow-down
3:0	**TH**	Threshold	**Restricts max. burst length of each write request** Max. burst length: Threshold + 1

14006014 WDMA_CFG WDMA Config Register 03020000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_SEL				INT_MTX_SEL										UNI_CONFIG	SWAP
Type	RW				RW										RW	RW
Reset	0	0	0	0	0	0	1	1							1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DNSP_SEL		EXT_MTX_EN	VERTICAL_AVG	CT_EN	UV_SWAP	RGB_SWAP	BYTE_SWAP	Out_Format							
Type	RW		RW	RW	RW	RW	RW	RW	RW							
Reset	0		0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:28	**DEBUG_SEL**	DEBUG_SEL	**For WDMA debugging selection**
27:24	**INT_MTX_SEL**	INT_MTX_SEL	**Selects pre-defined color transformation coefficient** 4'b0000: RGB to JPEG 4'b0010: RGB to BT601 4'b0011: RGB to BT709 4'b0100: JPEG to RGB 4'b0110: BT601 to RGB 4'b0111: BT709 to RGB 4'b1000: JPEG to BT601 4'b1001: JPEG to BT709 4'b1010: BT601 to JPEG 4'b1011: BT709 to JPEG 4'b1100: BT709 to BT601 4'b1101: BT601 to BT709
17	**UNICON**	UNI_CONFIG	**Uses uniform config or not** Do not modify this bit. 0: Disable uniform config 1: Enable uniform config
16	**SWAP**	SWAP	**Enables swap function to translate the output data format** Translated output data format: RGB565 -> BGR565 RGB888 -> BGR888 RGBA8888 -> BGRA8888 ARGB8888 -> ABGR8888 UYVY -> VYUY YUY2 -> YVYU IYUV -> YV12 NV12 -> NV21 0: Disable swap 1: Enable swap

Bit(s)	Mnemonic	Name	Description
15	**DNSP_SEL**	DNSP_SEL	**Selects YUV444 to YUV422 mode** 0: Drop odd pixel U/V 1: Apply [1 2 1] filter for U/V
13	**EXT_MTX_EN**	EXT_MTX_EN	**Enables color transformation external coefficients or not** For internal coefficient, use INT_MTX_SEL to select the pre-defined coefficients. For external coefficient, use register WDMA_C00 -> WDMA_POST_ADD. 0: Use internal coefficients for color transformation 1: Use External coefficients for color transformation
12	**V_AVG**	VERTICAL_AVG	**Enables vertical average or not** 0: Drop odd line pixels 1: Average in vertical while YUV444->YUV420
11	**CT_EN**	CT_EN	**Enables color transformation matrix or not** 0: Bypass color transformation matrix 1: Do color transformation
10	**UVS**	UV_SWAP	**Enables uv_swap or not** If the output format is UYVY (y1 v0 y0 u0), it will become (y1 u0 y0 v0) after UV swap. It takes no effect only when legacy mode and the output format is in RGB domain. 0: Disable uv swap 1: Enable uv swap
9	**RGBS**	RGB_SWAP	**Enables rgb_swap or not** If the output format is ARGB, it will become ABGR after RGB swap. It takes no effect only when legacy mode and the output format is in YUV domain. 0: Disable rgb swap 1: Enable rgb swap
8	**BYTES**	BYTE_SWAP	**Enables byte_swap or not** Takes no effect when output format is RGB565 or RGB888. If the output format is ARGB, it will become BGRA after byte swap. If the output format is UYVY(y1 v0 y0 u0), it will become (v0 y1 u0 y0) after byte swap. Only works in legacy mode. 0: Disable byte swap 1: Enable byte swap
7:4	**OF**	Out_Format	**Specifies output format of WDMA** 0: RGB565 1: RGB888 2: BGRA8888 3: ARGB8888 4: UYVY 5: YUY2 7: Y-only 8: IYUV (I420) 12: NV12

14006018 WDMA_SRC_SIZE **WDMA Source Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			Height													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			Width													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:16	**HGT**	Height	**Source height in pixels** Range: 0 ~ 2,047
13:0	**WTH**	Width	**Source width in pixels** Range: 0 ~ 2,047

1400601C WDMA_CLIP_SIZE **WDMA Clip Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			Height													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			Width													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:16	**HGT**	Height	**Clip height in pixels** Range: 0 ~ 2,047
13:0	**WTH**	Width	**Clip width in pixels** Range: 0 ~ 2,047

14006020 WDMA_CLIP_COORD **WDMA Clip Coordinate Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			Y_coord													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			X_coord													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:16	**CY**	Y_coord	**Y coordinate in pixels of clipped image** Range: 0 ~ 2,047
13:0	**CX**	X_coord	**X coordinate in pixels of clipped image** Range: 0 ~ 2,047

14006028 WDMA_DST_W_IN_BYTE **WDMA Destination Width in Byte** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dst_W_in_Byte															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**DWB**	Dst_W_in_Byte	**Destination width in bytes of each scan line** It is width*bpp. bpp: RGB565 -> 2, RGB888->3, ARGB->4, YV12->1, NV12->1, NV21->1

1400602C WDMA_ALPHA WDMA Alpha 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	A_Sel															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									A_Value							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**ASEL**	A_Sel	**Selects A source from pixel alpha or specified alpha** 0: Select pixle alpha from OVL 1: Select specfied A value
7:0	**A**	A_Value	**Specified A value**

14006038 WDMA_BUF_CON1 WDMA Buffer Control 1 10100100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ultra_Enable	Pre_Ultra_Enable		Frame_End_Ultra				issue_req_th								
Type	RW	RW		RW				RW								
Reset	0	0		1				0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								fifo_pseudo_size								
Type								RW								
Reset								1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**UE**	Ultra_Enable	**Enables ultra high request not**
30	**PUE**	Pre_Ultra_Enab le	**Enables pre-ultra high request**
28	**FEU**	Frame_End_Ultr a	**WDMA issues ultra high command at the end of the frame.**

Bit(s)	Mnemonic	Name	Description
24:16	**REQ_TH**	issue_req_th	**Threshold of data amount to release data from WDMA** WDMA starts sending data only when data amount in FIFO is larger than the set value.
8:0	**FIFO_SIZE**	fifo_pseudo_si ze	**Actually used FIFO entries** Keep it at default value. MDP_WDMA: 128. DISP_WDMA: 256.

1400603C WDMA_BUF_CON2 **WDMA Buffer Control 2** **10101010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ultra_th_high_ofs								pre_ultra_th_high_ofs							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ultra_th_low_ofs								pre_ultra_th_low							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**UL_H_OFFSET**	ultra_th_high_ ofs	**UH (ultra high threshold) = PUH + ultra_th_high_ofs** If FIFO size of WMDA > UH, WDMA will assert ultra high request.
23:16	**PUL_H_OFFSET**	pre_ultra_th_h igh_ofs	**PUH (pre_ultra high threshold) = UL + pre_ultra_th_high_ofs** If FIFO size of WMDA > PUH, WDMA will assert pre-ultra high request.
15:8	**UL_L_OFFSET**	ultra_th_low_o fs	**UL (ultra low threshold) = PUL + ultra_th_low_ofs** If FIFO size of WMDA < UL, WDMA will de-assert ultra high request.
7:0	**PUL_L_OFFSET**	pre_ultra_th_l ow	**PUL (pre_ultra low threshold) = pre_ultra_th_low** If FIFO size of WMDA < PUL, WDMA will de-assert pre-ultra high request.

14006040 WDMA_C00 **WDMA Matrix Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C01												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C00												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**C01**	C01	Matrix coefficient of C01
12:0	**C00**	C00	Matrix coefficient of C00

14006044 WDMA_C02 **WDMA Matrix Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C02												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0	C02	C02	Matrix coefficient of C02

14006048 WDMA_C10 **WDMA Matrix Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C11												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C10												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	C11	C11	Matrix coefficient of C11
12:0	C10	C10	Matrix coefficient of C10

1400604C WDMA_C12 **WDMA Matrix Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C12												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0	C12	C12	Matrix coefficient of C12

14006050 WDMA_C20 **WDMA Matrix Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C21												
Type				RW												

Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C20												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**C21**	C21	Matrix coefficient of C21
12:0	**C20**	C20	Matrix coefficient of C20

14006054 WDMA_C22 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C22												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0	**C22**	C22	Matrix coefficient of C22

14006058 WDMA_PRE_ADD0 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								PRE_ADD_1								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								PRE_ADD_0								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16	**PREADD1**	PRE_ADD_1	Matrix coefficient of pre add1
8:0	**PREADD0**	PRE_ADD_0	Matrix coefficient of pre add0

1400605C WDMA_PRE_ADD2 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								PRE_ADD_2								

Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0	**PREADD2**	PRE_ADD_2	Matrix coefficient of pre add2

14006060 WDMA_POST_ADD0 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								POST_ADD_1								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								POST_ADD_0								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16	**POSTADD1**	POST_ADD_1	Matrix coefficient of post add1
8:0	**POSTADD0**	POST_ADD_0	Matrix coefficient of post add0

14006064 WDMA_POST_ADD2 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								POST_ADD_2								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0	**POSTADD2**	POST_ADD_2	Matrix coefficient of post add2

14006078 WDMA_DST_UV_PITCH WDMA UV Destination Width in Byte 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UV_Dst_W_in_Byte															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**UV_Dst_W_in_Byte**	UV_Dst_W_in_Byte	UV pitch for YV12/NV12/NV21 output

14006080 WDMA_DST_ADDR_OFFSET **WDMA Destination Address Offset 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					WDMA_Destination_Address_offset0											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_Destination_Address_offset0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:0	**Address_offset 0**	WDMA_Destination_Address_offset0	**WDMA destination address offset 0** Final destination address = DST_ADDR + DST_ADDR_OFFSET

14006084 WDMA_DST_ADDR_OFFSET1 **WDMA Destination Address Offset 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					WDMA_Destination_Address_offset1											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_Destination_Address_offset1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:0	**Address_offset 1**	WDMA_Destination_Address_offset1	**WDMA destination address offset 1** U address offset for YV12 output; UV address offset for NV12/NV21 output

14006088 WDMA_DST_ADDR_OFFSET2 **WDMA Destination Address Offset 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					WDMA_Destination_Address_offset2											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_Destination_Address_offset2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:0	**Address_offset 2**	WDMA_Destination_Address_offset2	**WDMA destination address offset 2** V address offset for YV12 output

14006090 PROC_TRACK_CON_0 **DMA Processing Tracking Control 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		IGNORE_INIT_LATENCY	STOP_GREQ_EN	PROC_PRE_ULTRA_EN												
Type		RW	RW	RW												
Reset		0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TRACK_WINDOW											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30		IGNORE_INIT_LATENCY	**Ignores initial latency from SOF to the first proc_one**
29		STOP_GREQ_EN	**Enables stop_greq of the process tracking**
28		PROC_PRE_ULTRA_EN	**Enables pre_ultra of process tracking** If this bit is enabled, pre_ultra will be contolled by process tracking unit.
11:0		TRACK_WINDOW	**Tracking window** Unit: bclk_ck cycle

14006094 PROC_TRACK_CON_1 **DMA Processing Tracking Control 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									TARGET_CNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TARGET_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		TARGET_CNT	**Targets process count during a TRACK_WINDOW** It is s a 16.8 fix point number.

14006098 PROC_TRACK_CON_2 **DMA Processing Tracking Control 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name									STOP_CNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STOP_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		STOP_CNT	If processing counter > STOP_CNT, stop issuing greq.

140060A0 WDMA_FLOW_CTRL_DBG **WDMA Debug Port of flow_ctrl** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_IN_REQ	WDMA_IN_ACK	WDMA_GREQ	WDMA_FIFO_FULL			WDMA_STATE									
Type	RU	RU	RU	RU			RU									
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
15	**WDMA_IN_REQ**	WDMA_IN_REQ	**WDMA input request** IN_REQ=1 means the previous engine is sending data to WDMA and waiting for response from WDMA.
14	**WDMA_IN_ACK**	WDMA_IN_ACK	**Acknowledges WDMA input** IN_ACK=1 means WDMA is ready for the next pixel and is waiting for the previous engine to send the next pixel.
13	**WDMA_GREQ**	WDMA_GREQ	**WDMA SMI request** GREQ=1 means that WDMA is sending out an SMI request but no response from LARB.
12	**WDMA_FIFO_FULL**	WDMA_FIFO_FULL	**WDMA FIFO status is full or not**
9:0	**WDMA_STATE**	WDMA_STATE	**WDMA state machine** Read the current status of WDMA here. 00_0000_0001: Idle state 00_0000_0010: Clear state 00_0000_0100: Prepare state 1 00_0000_1000: Prepare state 2 00_0001_0000: Data transmit state 00_0010_0000: EOF prepare state 00_0100_0000: SW reset prepare state 00_1000_0000: EOF wait idle state 01_0000_0000: SW reset wait idle state 10_0000_0000: Frame completed state

140060A4 WDMA_EXEC_DBG **WDMA Debug Port of Exec Count** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											WDMA_FRAME_COMPLETE_CNT					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											WDMA_FRAME_RUN_CNT					
Type											RU					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:16	**CDBG**	WDMA_FRAME_COMPLETE_CNT	**Debugging status of complete cnt** When WDMA completes one frame (not SW reset or EOF reset), this counter will increase.
5:0	**EDBG**	WDMA_FRAME_RUN_CNT	**Debugging status of exec cnt** When WDMA receives SOF signal (Start Of Frame) from the MUTEX, this counter will increase.

140060A8 WDMA_CT_DBG — WDMA Debug Port of Input Counter — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			WDMA_INPUT_CNT_Y													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			WDMA_INPUT_CNT_X													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:16	**WDMA_INPUT_CNT_Y**	WDMA_INPUT_CNT_Y	**WDMA input counter in Y axis**
13:0	**WDMA_INPUT_CNT_X**	WDMA_INPUT_CNT_X	**WDMA input counter in X axis** How many pixels in a line are received by the WDMA. The total amount of received pixels is WDMA_INPUT_CNT_Y*SRC_W + WDMA_INPUT_CNT_X.

140060AC WDMA_SMI_TRAFFIC_DBG — WDMA Debug Port for SMI Traffic — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_SMI_TRAFFIC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_SMI_TRAFFIC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
31:0	**WDMA_SMI_STATUS**	WDMA_SMI_TRAFFIC	**Traffic status between WDMA and SMI** This counter should be 0 while WDMA is being sw reset.

140060B0 WDMA_PROC_TRACK_DBG **WDMA Debug Port for Process Track 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_PROC_CNT_MAX															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_PROC_CNT_MAX															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**WDMA_PROC_TRACK_MAX**	WDMA_PROC_CNT_MAX	**Process tracking status counter max. value** Write this register to clear the counter.

140060B4 WDMA_PROC_TRACK_DBG_1 **WDMA Debug Port for Process Track 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_PROC_CNT_MIN															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_PROC_CNT_MIN															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**WDMA_PROC_TRACK_MIN**	WDMA_PROC_CNT_MIN	**Process tracking status counter min. value** Write this register to clear the counter.

140060B8 WDMA_DEBUG **WDMA Debug Port** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_STA_DEBUG															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_STA_DEBUG															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CDBG**	WDMA_STA_DEBUG	**Trivil debugging status of WDMA**

Bit(s)	Mnemonic	Name	Description

14006100 WDMA_DUMMY WDMA Dummy Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	DUMMY	WDMA_DUMMY	WDMA dummy register

14006E00 WDMA_DITHER_0 WDMA Dithering Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								crc_clr				crc_start				crc_cen
Type								RW				RW				RW
Reset								0				0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	frame_done_del											out_sel				start
Type	RW											RW				RW
Reset	0	0	0	0	0	0	0	0				0				0

Bit(s)	Mnemonic	Name	Description
24		crc_clr	Write 1 to clear CRC result.
20		crc_start	Write 1 to start CRC counting.
16		crc_cen	
15:8		frame_done_del	Frame done return delay
4		out_sel	
0		start	

14006E14 WDMA_DITHER_5 WDMA Dithering Control Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	w_demo															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		w_demo	Short line length

14006E18 WDMA_DITHER_6 **WDMA Dithering Control Register 6** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																wrap_mode
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	left_en		fphase_r	fphase_en			fphase						round_en	rdither_en	lfsr_en	edither_en
Type	RW		RW	RW			RW						RW	RW	RW	RW
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		wrap_mode	**Enales rounding for dithering function** When rounding method is used, both running order and error dispersion cannot be used.
15:14		left_en	**Enables left part of screen dither** 0: Dither runs at full screen. 1: Dither runs at left part of screen.
13		fphase_r	**Dither SubPixel addend**
12		fphase_en	**Enables running order dithering frame phase control**
9:4		fphase	**Running order dithering frame phase increment.** Note: 1. If ROUND_EN = 1, the output will only be rounding (no matter what RDITHER_EN and EDITHER_EN settings are). 2. RDITHER_EN and EDITHER_EN can work together.
3		round_en	**Enables rounding for dithering function** When rounding method is used, both running order and error dispersion cannot be used.
2		rdither_en	**Enables running order dithering** Running order dithering must be set when ROUND_EN is set to 0. Running order dithering can run with error dispersion when EDOTHER_EN is set to 1.
1		lfsr_en	**Enables LFSR-type dithering**
0		edither_en	**Enables error dispersion dithering** Error dispersion dithering must be set when ROUND_EN is set to 0. Running order dithering can run with error dispersion when RDITHER_EN is set to 1.

14006E1C WDMA_DITHER_7 **WDMA Dithering Control Register 7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							drmo d_b				drmod_g				drmod_r	
Type							RW				RW				RW	
Reset							0	0			0	0			0	0

Bit(s)	Mnemonic	Name	Description
9:8		drmod_b	**Selects dither mode** 0: No dither 1: 12-bit dither to 10-bit 2: 12-bit dither to 8-bit 3: 12-bit dither to 6-bit
5:4		drmod_g	**Selects dither mode** 0: No dither 1: 12-bit dither to 10-bit 2: 12-bit dither to 8-bit 3: 12-bit dither to 6-bit
1:0		drmod_r	**Selects dither mode** 0: No dither 1: 12-bit dither to 10-bit 2: 12-bit dither to 8-bit 3: 12-bit dither to 6-bit

14006E20 WDMA_DITHER_8 **WDMA Dithering Control Register 8** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ink_ data _r									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ink
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
25:16		ink_data_r	Ink data for R
0		ink	Enables ink

14006E24 WDMA_DITHER_9 **WDMA Dithering Control Register 9** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ink_data_b									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							ink_data_g									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25:16		ink_data_b	Ink data for B
9:0		ink_data_g	Ink data for G

14006E28 WDMA_DITHER_10 WDMA Dithering Control Register 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						fpha se_b it					fphase_se l				fphase_ct rl	
Type						RW					RW				RW	
Reset						0	0	0			0	0			0	0

Bit(s)	Mnemonic	Name	Description
10:8		fphase_bit	**fphase_bit XOR bus number** *Note: This function checks reg_fphase_sel.* Only 0, 1, 2, 4 and 6 are available. 0: No effect on fphase (XOR disabled)
5:4		fphase_sel	**fphase XOR function: fphase do self bit-wise xor** *Note: This function checks reg_fphase_sel. Only bit 2, bit 4 and bit 6 are available.* 0: Disable fphase XOR 1: Effect fphase[0]~[1] based on the value of reg_fphase_sel is 1 or 2. 2: Effect fphase[0]~[3] based on the value of reg_fphase_sel is 1, 2 or 4. 3: Effect fphase[0]~[5] based on the value of reg_fphase_sel is 1, 2, 4 or 6.
1:0		fphase_ctrl	**Selects fphase range to add with rdither table.** 00: 0~63 01: 0~16 10: 0~3

14006E2C WDMA_DITHER_11 WDMA Dithering Control Register 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			sub_ b				sub_ g				sub_r					subp ix_e n
Type			RW				RW				RW					RW
Reset			0	0			0	0			0	0				0

Bit(s)	Mnemonic	Name	Description
13:12		sub_b	**Dither SubPixel addend**

Bit(s)	Mnemonic	Name	Description
9:8		sub_g	**Dither SubPixel addend**
5:4		sub_r	**Dither SubPixel addend**
0		subpix_en	**Enables sub pix dither mode** 0: Pix dither mode 1: Sub pix dither mode

14006E30 WDMA_DITHER_12 WDMA Dithering Control Register 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	h_active															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											table_en					lsb_off
Type											RW					RW
Reset											0	0				0

Bit(s)	Mnemonic	Name	Description
31:16		h_active	**Active region of dither IP**
5:4		table_en	**Active bit of magic table for running order** 01: Phase active in bit 3 ~ bit 0 10: Phase active in bit 1 ~ bit 0 Others: Phase active in bit 5 ~ bit 0
0		lsb_off	**Turns off LSB for dither function**

14006E34 WDMA_DITHER_13 WDMA Dithering Control Register 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						rshi ft_b				rshift_g				rshift_r		
Type						RW				RW				RW		
Reset						0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
10:8		rshift_b	B right shift position after IP output
6:4		rshift_g	G right shift position after IP output
2:0		rshift_r	R right shift position after IP output

14006E38 WDMA_DITHER_14 WDMA Dithering Control Register 14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							debug_mode			diff_shift						testpin_en
Type							RW			RW						RW
Reset							0	0		0	0	0				0

Bit(s)	Mnemonic	Name	Description
9:8		debug_mode	1: Enables debugging mode
6:4		diff_shift	Debugging mode difference shift positions
0		testpin_en	Enables testpin input

14006E3C WDMA_DITHER_15 **WDMA Dithering Control Register 15** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		lsb_err_shift_r				ovflw_bit_r				add_lshift_r				input_rshift_r		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																new_bit_mode
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
30:28		lsb_err_shift_r	RED LSB error bit select
26:24		ovflw_bit_r	RED overflow bit select
22:20		add_lshift_r	RED addend left shift bits
18:16		input_rshift_r	RED input right shift bits
0		new_bit_mode	1: Enables modified test algorithm

14006E40 WDMA_DITHER_16 **WDMA Dithering Control Register 16** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		lsb_err_shift_b				ovflw_bit_b				add_lshift_b				input_rshift_b		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		lsb_err_shift_g				ovflw_bit_g				add_lshift_g				input_rshift_g		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		lsb_err_shift_b	GREEN LSB error bit select
26:24		ovflw_bit_b	GREEN overflow bit select
22:20		add_lshift_b	GREEN addend left shift bits
18:16		input_rshift_b	GREEN input right shift bits

Bit(s)	Mnemonic	Name	Description
14:12		lsb_err_shift_ g	BLUE LSB error bit select
10:8		ovflw_bit_g	BLUE overflow bit select
6:4		add_lshift_g	BLUE addend left shift bits
2:0		input_rshift_g	BLUE input right shift bits

14006E44 WDMA_DITHER_17 WDMA Dithering Control Register 17 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																crc_rdy
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crc_out															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		crc_rdy	CRC ready
15:0		crc_out	CRC result

14006F00 WDMA_DST_ADDR0 WDMA Destination Address 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Addresso															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Addresso															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	ADDR0	Addresso	**Destination address of image** There is no alignment restriction. For YV12/NV12/NV21 data format, address 0 means the destination of Y.

14006F04 WDMA_DST_ADDR1 WDMA Destination Address 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Address1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Address1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**Address1**	Address1	**U address for YV12 output** UV address for NV12/NV21 output

14006F08 WDMA_DST_ADDR2 WDMA Destination Address 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Address2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Address2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**Address2**	Address2	V address for YV12 output

Module name: DISP_WDMA0 Base address: (+14011000h)

Address	Name	Width	Register Function
14011000	**WDMA_INTEN**	32	WDMA Interrupt Enable
14011004	**WDMA_INTSTA**	32	WDMA Interrupt Status
14011008	**WDMA_EN**	32	WDMA Enable
1401100C	**WDMA_RST**	32	WDMA Reset
14011010	**WDMA_SMI_CON**	32	WDMA SMI Control
14011014	**WDMA_CFG**	32	WDMA Config Register
14011018	**WDMA_SRC_SIZE**	32	WDMA Source Size Register
1401101C	**WDMA_CLIP_SIZE**	32	WDMA Clip Size Register
14011020	**WDMA_CLIP_COORD**	32	WDMA Clip Coordinate Register
14011028	**WDMA_DST_W_IN_BYTE**	32	WDMA Destination Width in Byte
1401102C	**WDMA_ALPHA**	32	WDMA Alpha
14011038	**WDMA_BUF_CON1**	32	WDMA Buffer Control 1
1401103C	**WDMA_BUF_CON2**	32	WDMA Buffer Control 2
14011040	**WDMA_C00**	32	WDMA Matrix Coefficient
14011044	**WDMA_C02**	32	WDMA Matrix Coefficient
14011048	**WDMA_C10**	32	WDMA Matrix Coefficient
1401104C	**WDMA_C12**	32	WDMA Matrix Coefficient
14011050	**WDMA_C20**	32	WDMA Matrix Coefficient
14011054	**WDMA_C22**	32	WDMA Matrix Coefficient
14011058	**WDMA_PRE_ADD0**	32	WDMA Matrix Coefficient
1401105C	**WDMA_PRE_ADD2**	32	WDMA Matrix Coefficient
14011060	**WDMA_POST_ADD0**	32	WDMA Matrix Coefficient
14011064	**WDMA_POST_ADD2**	32	WDMA Matrix Coefficient

Address	Name	Width	Register Function
14011078	WDMA_DST_UV_PITCH	32	WDMA UV Destination Width in Byte
14011080	WDMA_DST_ADDR_OFFSET0	32	WDMA Destination Address Offset 0
14011084	WDMA_DST_ADDR_OFFSET1	32	WDMA Destination Address Offset 1
14011088	WDMA_DST_ADDR_OFFSET2	32	WDMA Destination Address Offset 2
14011090	PROC_TRACK_CON_0	32	DMA Processing Tracking Control 0
14011094	PROC_TRACK_CON_1	32	DMA Processing Tracking Control 1
14011098	PROC_TRACK_CON_2	32	DMA Processing Tracking Control 2
140110A0	WDMA_FLOW_CTRL_DBG	32	WDMA Debug Port of flow_ctrl
140110A4	WDMA_EXEC_DBG	32	WDMA Debug Port of Exec Count
140110A8	WDMA_CT_DBG	32	WDMA Debug Port of Input Counter
140110AC	WDMA_SMI_TRAFFIC_DBG	32	WDMA Debug Port for SMI Traffic
140110B0	WDMA_PROC_TRACK_DBG_0	32	WDMA Debug Port for Process Track 0
140110B4	WDMA_PROC_TRACK_DBG_1	32	WDMA Debug Port for Process Track 1
140110B8	WDMA_DEBUG	32	WDMA Debug Port
14011100	WDMA_DUMMY	32	WDMA Dummy Register
14011E00	WDMA_DITHER_0	32	WDMA Dithering Control Register 0
14011E14	WDMA_DITHER_5	32	WDMA Dithering Control Register 5
14011E18	WDMA_DITHER_6	32	WDMA Dithering Control Register 6
14011E1C	WDMA_DITHER_7	32	WDMA Dithering Control Register 7
14011E20	WDMA_DITHER_8	32	WDMA Dithering Control Register 8
14011E24	WDMA_DITHER_9	32	WDMA Dithering Control Register 9
14011E28	WDMA_DITHER_10	32	WDMA Dithering Control Register 10
14011E2C	WDMA_DITHER_11	32	WDMA Dithering Control Register 11
14011E30	WDMA_DITHER_12	32	WDMA Dithering Control Register 12
14011E34	WDMA_DITHER_13	32	WDMA Dithering Control Register 13
14011E38	WDMA_DITHER_14	32	WDMA Dithering Control Register 14
14011E3C	WDMA_DITHER_15	32	WDMA Dithering Control Register 15
14011E40	WDMA_DITHER_16	32	WDMA Dithering Control Register 16
14011E44	WDMA_DITHER_17	32	WDMA Dithering Control Register 17
14011F00	WDMA_DST_ADDR0	32	WDMA Destination Address 0
14011F04	WDMA_DST_ADDR1	32	WDMA Destination Address 1
14011F08	WDMA_DST_ADDR2	32	WDMA Destination Address 2

14011000 WDMA_INTEN WDMA Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															Frame_Underrun	Frame_Complete
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	**FUE**	Frame_Underrun	**Enables frame underrun interrupt** 0: Disable interrupt 1: Enable interrupt
0	**FCE**	Frame_Complete	**Enables frame completed interrupt** 0: Disable interrupt 1: Enable interrupt

14011004 WDMA_INTSTA **WDMA Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															Frame_Underrun	Frame_Complete
Type															A1	A1
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	**FU**	Frame_Underrun	**Incompletes one frame when WDMA receives EOF** SW writes this bit to clear IRQ. 0: WDMA idle or busy 1: WDMA incompletes one frame
0	**FC**	Frame_Complete	**Completes one frame before WDMA receives EOF** SW writes this bit to clear IRQ. 0: WDMA idle or busy 1: WDMA completes one frame

14011008 WDMA_EN **WDMA Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																Enable
Type																RW

Reset																0

Bit(s)	Mnemonic	Name	Description
0	**EN**	Enable	**Enables WDMA or not** 0: Disable WDMA 1: Enable WDMA

1401100C WDMA_RST WDMA Reset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**Soft_Reset**
Type																AO
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**RST**	Soft_Reset	**Soft reset to WDMA** Write this bit to trigger soft reset. WDMA will reset itself when bus transaction is done. SW must keep polling bit 0 of register WDMA_FLOW_CTRL_DBG until it is 1 to determine if the reset flow is done. 0: Write: No effect; Read: Reset is done . 1: Write: Trigger reset; Read: Reset is on-going.

14011010 WDMA_SMI_CON WDMA SMI Control 02240007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					**SMI_V_REPEAT_NUM**				**SMI_U_REPEAT_NUM**				**SMI_Y_REPEAT_NUM**			
Type					RW				RW				RW			
Reset					0	0	1	0	0	0	1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**Slow_Count**								**Slow_Level**			**Slow_Enable**	**Threshold**			
Type	RW								RW			RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
27:24	**V_NUM**	SMI_V_REPEAT_NUM	**Number of continuous V SMI commands** Only takes effects when out_format=YV12/NV12/NV21.
23:20	**U_NUM**	SMI_U_REPEAT_NUM	**Number of continuous U SMI commands** Only takes effects when out_format=YV12/NV12/NV21.
19:16	**Y_NUM**	SMI_Y_REPEAT_NUM	**Number of continuous Y SMI commands** Only takes effects when out_format=YV12/NV12/NV21.
15:8	**SC**	Slow_Count	**Slow-down counter of each write request** The actual slow-down count of each request is (slow_count*slow_level).

Bit(s)	Mnemonic	Name	Description
7:5	**SL**	Slow_Level	**Slow-down level of each write request** 0: slow_level=1 1: slow_level=2 2: slow_level=4 4: slow_level=8
4	**SE**	Slow_Enable	**Enables slow-down of each write request or not** 0: Disable slow-down 1: Enable slow-down
3:0	**TH**	Threshold	**Restricts max. burst length of each write request** Max. burst length: Threshold + 1

14011014 WDMA_CFG WDMA Config Register 03020000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_SEL				INT_MTX_SEL										UNI_CONFIG	SWAP
Type	RW				RW										RW	RW
Reset	0	0	0	0	0	0	1	1							1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DNSP_SEL		EXT_MTX_EN	VERTICAL_AVG	CT_EN	UV_SWAP	RGB_SWAP	BYTE_SWAP	Out_Format							
Type	RW		RW	RW	RW	RW	RW	RW	RW							
Reset	0		0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:28	**DEBUG_SEL**	DEBUG_SEL	**For WDMA debugging selection**
27:24	**INT_MTX_SEL**	INT_MTX_SEL	**Selects pre-defined color transformation coefficient** 4'b0000: RGB to JPEG 4'b0010: RGB to BT601 4'b0011: RGB to BT709 4'b0100: JPEG to RGB 4'b0110: BT601 to RGB 4'b0111: BT709 to RGB 4'b1000: JPEG to BT601 4'b1001: JPEG to BT709 4'b1010: BT601 to JPEG 4'b1011: BT709 to JPEG 4'b1100: BT709 to BT601 4'b1101: BT601 to BT709
17	**UNICON**	UNI_CONFIG	**Uses uniform config or not** Do not modify this bit. 0: Disable uniform config 1: Enable uniform config
16	**SWAP**	SWAP	**Enables swap function to translate the output data format** Translated output data format: RGB565 -> BGR565 RGB888 -> BGR888 RGBA8888 -> BGRA8888 ARGB8888 -> ABGR8888 UYVY -> VYUY YUY2 -> YVYU IYUV -> YV12

Bit(s)	Mnemonic	Name	Description
			NV12 -> NV21 0: Disable swap 1: Enable swap
15	**DNSP_SEL**	DNSP_SEL	**Selects YUV444 to YUV422 mode** 0: Drop odd pixel U/V 1: Apply [1 2 1] filter for U/V
13	**EXT_MTX_EN**	EXT_MTX_EN	**Enables color transformation external coefficients or not** For internal coefficient, use INT_MTX_SEL to select the pre-defined coefficients. For external coefficient, use register WDMA_C00 -> WDMA_POST_ADD. 0: Use internal coefficients for color transformation 1: Use External coefficients for color transformation
12	**V_AVG**	VERTICAL_AVG	**Enables vertical average or not** 0: Drop odd line pixels 1: Average in vertical while YUV444->YUV420
11	**CT_EN**	CT_EN	**Enables color transformation matrix or not** 0: Bypass color transformation matrix 1: Do color transformation
10	**UVS**	UV_SWAP	**Enables uv_swap or not** If the output format is UYVY (y1 v0 y0 u0), it will become (y1 u0 y0 v0) after UV swap. It takes no effect only when legacy mode and the output format is in RGB domain. 0: Disable uv swap 1: Enable uv swap
9	**RGBS**	RGB_SWAP	**Enables rgb_swap or not** If the output format is ARGB, it will become ABGR after RGB swap. It takes no effect only when legacy mode and the output format is in YUV domain. 0: Disable rgb swap 1: Enable rgb swap
8	**BYTES**	BYTE_SWAP	**Enables byte_swap or not** Takes no effect when output format is RGB565 or RGB888. If the output format is ARGB, it will become BGRA after byte swap. If the output format is UYVY(y1 v0 y0 u0), it will become (v0 y1 u0 y0) after byte swap. Only works in legacy mode. 0: Disable byte swap 1: Enable byte swap
7:4	**OF**	Out_Format	**Specifies output format of WDMA** 0: RGB565 1: RGB888 2: BGRA8888 3: ARGB8888 4: UYVY 5: YUY2 7: Y-only 8: IYUV (I420) 12: NV12

14011018 WDMA_SRC_SIZE WDMA Source Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name			Height													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			Width													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:16	**HGT**	Height	**Source height in pixels** Range: 0 ~ 2,047
13:0	**WTH**	Width	**Source width in pixels** Range: 0 ~ 2,047

1401101C WDMA_CLIP_SIZE **WDMA Clip Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			Height													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			Width													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:16	**HGT**	Height	**Clip height in pixels** Range: 0 ~ 2,047
13:0	**WTH**	Width	**Clip width in pixels** Range: 0 ~ 2,047

14011020 WDMA_CLIP_COORD **WDMA Clip Coordinate Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			Y_coord													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			X_coord													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:16	**CY**	Y_coord	**Y coordinate in pixels of clipped image** Range: 0 ~ 2,047
13:0	**CX**	X_coord	**X coordinate in pixels of clipped image** Range: 0 ~ 2,047

14011028 WDMA_DST_W_IN_BYTE **WDMA Destination Width in Byte** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dst_W_in_Byte															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**DWB**	Dst_W_in_Byte	**Destination width in bytes of each scan line** It is width*bpp. bpp: RGB565 -> 2, RGB888->3, ARGB->4, YV12->1, NV12->1, NV21->1

1401102C WDMA_ALPHA **WDMA Alpha** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	A_Sel															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									A_Value							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**ASEL**	A_Sel	**Selects A source from pixel alpha or specified alpha** 0: Select pixle alpha from OVL 1: Select specfied A value
7:0	**A**	A_Value	**Specified A value**

14011038 WDMA_BUF_CON1 **WDMA Buffer Control 1** **10100100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ultra_Enable	Pre_Ultra_Enable		Frame_End_Ultra				issue_req_th								
Type	RW	RW		RW				RW								
Reset	0	0		1				0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								fifo_pseudo_size								
Type								RW								
Reset								1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**UE**	Ultra_Enable	**Enables ultra high request not**
30	**PUE**	Pre_Ultra_Enab le	**Enables pre-ultra high request**
28	**FEU**	Frame_End_Ultr a	**WDMA issues ultra high command at the end of the frame.**
24:16	**REQ_TH**	issue_req_th	**Threshold of data amount to release data from WDMA** WDMA starts sending data only when data amount in FIFO is larger than the set value.
8:0	**FIFO_SIZE**	fifo_pseudo_si ze	**Actually used FIFO entries** Keep it at default value. MDP_WDMA: 128. DISP_WDMA: 256.

1401103C WDMA_BUF_CON2 **WDMA Buffer Control 2** **10101010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ultra_th_high_ofs								pre_ultra_th_high_ofs							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ultra_th_low_ofs								pre_ultra_th_low							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**UL_H_OFFSET**	ultra_th_high_ ofs	**UH (ultra high threshold) = PUH + ultra_th_high_ofs** If FIFO size of WMDA > UH, WDMA will assert ultra high request.
23:16	**PUL_H_OFFSET**	pre_ultra_th_h igh_ofs	**PUH (pre_ultra high threshold) = UL + pre_ultra_th_high_ofs** If FIFO size of WMDA > PUH, WDMA will assert pre-ultra high request.
15:8	**UL_L_OFFSET**	ultra_th_low_o fs	**UL (ultra low threshold) = PUL + ultra_th_low_ofs** If FIFO size of WMDA < UL, WDMA will de-assert ultra high request.
7:0	**PUL_L_OFFSET**	pre_ultra_th_l ow	**PUL (pre_ultra low threshold) = pre_ultra_th_low** If FIFO size of WMDA < PUL, WDMA will de-assert pre-ultra high request.

14011040 WDMA_C00 **WDMA Matrix Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C01												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C00												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
28:16	**C01**	C01	Matrix coefficient of C01
12:0	**C00**	C00	Matrix coefficient of C00

14011044 WDMA_C02 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C02												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0	**C02**	C02	Matrix coefficient of C02

14011048 WDMA_C10 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C11												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C10												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**C11**	C11	Matrix coefficient of C11
12:0	**C10**	C10	Matrix coefficient of C10

1401104C WDMA_C12 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C12												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0	**C12**	C12	Matrix coefficient of C12

14011050 WDMA_C20 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C21												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C20												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**C21**	C21	Matrix coefficient of C21
12:0	**C20**	C20	Matrix coefficient of C20

14011054 WDMA_C22 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C22												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0	**C22**	C22	Matrix coefficient of C22

14011058 WDMA_PRE_ADD0 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								PRE_ADD_1								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								PRE_ADD_0								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16	**PREADD1**	PRE_ADD_1	Matrix coefficient of pre add1
8:0	**PREADD0**	PRE_ADD_0	Matrix coefficient of pre add0

1401105C WDMA_PRE_ADD2 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								PRE_ADD_2								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0	**PREADD2**	PRE_ADD_2	Matrix coefficient of pre add2

14011060 WDMA_POST_ADD0 — WDMA Matrix Coefficient — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								POST_ADD_1								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								POST_ADD_0								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16	**POSTADD1**	POST_ADD_1	Matrix coefficient of post add1
8:0	**POSTADD0**	POST_ADD_0	Matrix coefficient of post add0

14011064 WDMA_POST_ADD2 — WDMA Matrix Coefficient — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								POST_ADD_2								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0	**POSTADD2**	POST_ADD_2	Matrix coefficient of post add2

14011078 WDMA_DST_UV_PITCH — WDMA UV Destination Width in Byte — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UV_Dst_W_in_Byte															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**UV_Dst_W_in_Byte**	UV_Dst_W_in_By te	UV pitch for YV12/NV12/NV21 output

14011080 WDMA_DST_ADDR_OFFSET0 WDMA Destination Address Offset 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					WDMA_Destination_Address_offset0											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_Destination_Address_offset0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:0	**Address_offset 0**	WDMA_Destinati on_Address_off set0	**WDMA destination address offset 0** Final destination address = DST_ADDR + DST_ADDR_OFFSET

14011084 WDMA_DST_ADDR_OFFSET1 WDMA Destination Address Offset 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					WDMA_Destination_Address_offset1											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_Destination_Address_offset1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:0	**Address_offset 1**	WDMA_Destinati on_Address_off set1	**WDMA destination address offset 1** U address offset for YV12 output; UV address offset for NV12/NV21 output

14011088 WDMA_DST_ADDR_OFFSET2 WDMA Destination Address Offset 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					WDMA_Destination_Address_offset2											

Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_Destination_Address_offset2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:0	**Address_offset 2**	WDMA_Destination_Address_offset2	**WDMA destination address offset 2** V address offset for YV12 output

14011090 PROC_TRACK_CON_0 DMA Processing Tracking Control 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		IGNORE_INIT_LATENCY	STOP_GREQ_EN	PROC_PRE_ULTRA_EN												
Type		RW	RW	RW												
Reset		0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRACK_WINDOW															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30		IGNORE_INIT_LATENCY	**Ignores initial latency from SOF to the first proc_one**
29		STOP_GREQ_EN	**Enables stop_greq of the process tracking**
28		PROC_PRE_ULTRA_EN	**Enables pre_ultra of process tracking** If this bit is enabled, pre_ultra will be contolled by process tracking unit.
11:0		TRACK_WINDOW	**Tracking window** Unit: bclk_ck cycle

14011094 PROC_TRACK_CON_1 DMA Processing Tracking Control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									TARGET_CNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TARGET_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		TARGET_CNT	**Targets process count during a TRACK_WINDOW**

Bit(s)	Mnemonic	Name	Description
			It is s a 16.8 fix point number.

14011098 PROC_TRACK_CON_2 **DMA Processing Tracking Control 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									STOP_CNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STOP_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		STOP_CNT	If processing counter > STOP_CNT, stop issuing greq.

140110A0 WDMA_FLOW_CTRL_DBG **WDMA Debug Port of flow_ctrl** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_IN_REQ	WDMA_IN_ACK	WDMA_GREQ	WDMA_FIFO_FULL			WDMA_STATE									
Type	RU	RU	RU	RU			RU									
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
15	**WDMA_IN_REQ**	WDMA_IN_REQ	**WDMA input request** IN_REQ=1 means the previous engine is sending data to WDMA and waiting for response from WDMA.
14	**WDMA_IN_ACK**	WDMA_IN_ACK	**Acknowledges WDMA input** IN_ACK=1 means WDMA is ready for the next pixel and is waiting for the previous engine to send the next pixel.
13	**WDMA_GREQ**	WDMA_GREQ	**WDMA SMI request** GREQ=1 means that WDMA is sending out an SMI request but no response from LARB.
12	**WDMA_FIFO_FULL**	WDMA_FIFO_FULL	**WDMA FIFO status is full or not**
9:0	**WDMA_STATE**	WDMA_STATE	**WDMA state machine** Read the current status of WDMA here. 00_0000_0001: Idle state 00_0000_0010: Clear state 00_0000_0100: Prepare state 1 00_0000_1000: Prepare state 2 00_0001_0000: Data transmit state 00_0010_0000: EOF prepare state 00_0100_0000: SW reset prepare state

Bit(s)	Mnemonic	Name	Description
			00_1000_0000: EOF wait idle state 01_0000_0000: SW reset wait idle state 10_0000_0000: Frame completed state

140110A4 WDMA_EXEC_DBG — **WDMA Debug Port of Exec Count** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											WDMA_FRAME_COMPLETE_CNT					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											WDMA_FRAME_RUN_CNT					
Type											RU					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:16	CDBG	WDMA_FRAME_COMPLETE_CNT	**Debugging status of complete cnt** When WDMA completes one frame (not SW reset or EOF reset), this counter will increase.
5:0	EDBG	WDMA_FRAME_RUN_CNT	**Debugging status of exec cnt** When WDMA receives SOF signal (Start Of Frame) from the MUTEX, this counter will increase.

140110A8 WDMA_CT_DBG — **WDMA Debug Port of Input Counter** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			WDMA_INPUT_CNT_Y													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			WDMA_INPUT_CNT_X													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:16	WDMA_INPUT_CNT_Y	WDMA_INPUT_CNT_Y	**WDMA input counter in Y axis**
13:0	WDMA_INPUT_CNT_X	WDMA_INPUT_CNT_X	**WDMA input counter in X axis** How many pixels in a line are received by the WDMA. The total amount of received pixels is WDMA_INPUT_CNT_Y*SRC_W + WDMA_INPUT_CNT_X.

140110AC WDMA_SMI_TRAFFIC_DBG — **WDMA Debug Port for SMI Traffic** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_SMI_TRAFFIC															

Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_SMI_TRAFFIC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**WDMA_SMI_STATUS**	WDMA_SMI_TRAFFIC	**Traffic status between WDMA and SMI** This counter should be 0 while WDMA is being sw reset.

140110B0 WDMA_PROC_TRACK_DBG — WDMA Debug Port for Process Track 0 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_PROC_CNT_MAX															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_PROC_CNT_MAX															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**WDMA_PROC_TRACK_MAX**	WDMA_PROC_CNT_MAX	**Process tracking status counter max. value** Write this register to clear the counter.

140110B4 WDMA_PROC_TRACK_DBG_1 — WDMA Debug Port for Process Track 1 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_PROC_CNT_MIN															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_PROC_CNT_MIN															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**WDMA_PROC_TRACK_MIN**	WDMA_PROC_CNT_MIN	**Process tracking status counter min. value** Write this register to clear the counter.

140110B8 WDMA_DEBUG — WDMA Debug Port — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_STA_DEBUG															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_STA_DEBUG															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CDBG**	WDMA_STA_DEBUG	Trivil debugging status of WDMA

14011100 WDMA_DUMMY WDMA Dummy Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DUMMY**	WDMA_DUMMY	WDMA dummy register

14011E00 WDMA_DITHER_0 WDMA Dithering Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								crc_clr				crc_start				crc_cen
Type								RW				RW				RW
Reset								0				0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	frame_done_del											out_sel				start
Type	RW											RW				RW
Reset	0	0	0	0	0	0	0	0				0				0

Bit(s)	Mnemonic	Name	Description
24		crc_clr	Write 1 to clear CRC result.
20		crc_start	Write 1 to start CRC counting.
16		crc_cen	
15:8		frame_done_del	Frame done return delay
4		out_sel	
0		start	

14011E14 WDMA_DITHER_5 WDMA Dithering Control Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	w_demo															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		w_demo	Short line length

14011E18 WDMA_DITHER_6 WDMA Dithering Control Register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																wrap_mode
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	left_en		fphase_r	fphase_en			fphase						round_en	rdither_en	lfsr_en	edither_en
Type	RW		RW	RW			RW						RW	RW	RW	RW
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		wrap_mode	**Enales rounding for dithering function** When rounding method is used, both running order and error dispersion cannot be used.
15:14		left_en	**Enables left part of screen dither** 0: Dither runs at full screen. 1: Dither runs at left part of screen.
13		fphase_r	**Dither SubPixel addend**
12		fphase_en	**Enables running order dithering frame phase control**
9:4		fphase	**Running order dithering frame phase increment.** *Note:* *1. If ROUND_EN = 1, the output will only be rounding (no matter what RDITHER_EN and EDITHER_EN settings are).* *2. RDITHER_EN and EDITHER_EN can work together.*
3		round_en	**Enables rounding for dithering function** When rounding method is used, both running order and error dispersion cannot be used.
2		rdither_en	**Enables running order dithering** Running order dithering must be set when ROUND_EN is set to 0. Running order dithering can run with error dispersion when EDOTHER_EN is set to 1.
1		lfsr_en	**Enables LFSR-type dithering**
0		edither_en	**Enables error dispersion dithering** Error dispersion dithering must be set when ROUND_EN is set to 0. Running order dithering can run with error dispersion when RDITHER_EN is set to 1.

14011E1C WDMA_DITHER_7 — WDMA Dithering Control Register 7 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							drmo d_b				drmod_g				drmod_r	
Type							RW				RW				RW	
Reset							0	0			0	0			0	0

Bit(s)	Mnemonic	Name	Description
9:8		drmod_b	**Selects dither mode** 0: No dither 1: 12-bit dither to 10-bit 2: 12-bit dither to 8-bit 3: 12-bit dither to 6-bit
5:4		drmod_g	**Selects dither mode** 0: No dither 1: 12-bit dither to 10-bit 2: 12-bit dither to 8-bit 3: 12-bit dither to 6-bit
1:0		drmod_r	**Selects dither mode** 0: No dither 1: 12-bit dither to 10-bit 2: 12-bit dither to 8-bit 3: 12-bit dither to 6-bit

14011E20 WDMA_DITHER_8 — WDMA Dithering Control Register 8 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ink_ data _r									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ink
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
25:16		ink_data_r	Ink data for R
0		ink	Enables ink

14011E24 WDMA_DITHER_9 — WDMA Dithering Control Register 9 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ink_data_b									
Type							RW									

Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							ink_data_g									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25:16		ink_data_b	Ink data for B
9:0		ink_data_g	Ink data for G

14011E28 WDMA_DITHER_10 WDMA Dithering Control Register 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						fpha se_b it					fphase_se l				fphase_ct rl	
Type						RW					RW				RW	
Reset						0	0	0			0	0			0	0

Bit(s)	Mnemonic	Name	Description
10:8		fphase_bit	**fphase_bit XOR bus number** *Note: This function checks reg_fphase_sel.* Only 0, 1, 2, 4 and 6 are available. 0: No effect on fphase (XOR disabled)
5:4		fphase_sel	**fphase XOR function: fphase do self bit-wise xor** *Note: This function checks reg_fphase_sel. Only bit 2, bit 4 and bit 6 are available.* 0: Disable fphase XOR 1: Effect fphase[0]~[1] based on the value of reg_fphase_sel is 1 or 2. 2: Effect fphase[0]~[3] based on the value of reg_fphase_sel is 1, 2 or 4. 3: Effect fphase[0]~[5] based on the value of reg_fphase_sel is 1, 2, 4 or 6.
1:0		fphase_ctrl	**Selects fphase range to add with rdither table.** 00: 0~63 01: 0~16 10: 0~3

14011E2C WDMA_DITHER_11 WDMA Dithering Control Register 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			sub_ b				sub_ g				sub_r					subp ix_e n

Type			RW				RW				RW					RW
Reset			0	0			0	0			0	0				0

Bit(s)	Mnemonic	Name	Description
13:12		sub_b	**Dither SubPixel addend**
9:8		sub_g	**Dither SubPixel addend**
5:4		sub_r	**Dither SubPixel addend**
0		subpix_en	**Enables sub pix dither mode** 0: Pix dither mode 1: Sub pix dither mode

14011E30 WDMA_DITHER_12 WDMA Dithering Control Register 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	h_active															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											table_en					lsb_off
Type											RW					RW
Reset											0	0				0

Bit(s)	Mnemonic	Name	Description
31:16		h_active	**Active region of dither IP**
5:4		table_en	**Active bit of magic table for running order** 01: Phase active in bit 3 ~ bit 0 10: Phase active in bit 1 ~ bit 0 Others: Phase active in bit 5 ~ bit 0
0		lsb_off	**Turns off LSB for dither function**

14011E34 WDMA_DITHER_13 WDMA Dithering Control Register 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						rshi ft_b				rshift_g				rshift_r		
Type						RW				RW				RW		
Reset						0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
10:8		rshift_b	B right shift position after IP output
6:4		rshift_g	G right shift position after IP output
2:0		rshift_r	R right shift position after IP output

14011E38 WDMA_DITHER_14 WDMA Dithering Control Register 14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							debug_mode			diff_shift						testpin_en
Type							RW			RW						RW
Reset							0	0		0	0	0				0

Bit(s)	Mnemonic	Name	Description
9:8		debug_mode	1: Enables debugging mode
6:4		diff_shift	Debugging mode difference shift positions
0		testpin_en	Enables testpin input

14011E3C WDMA_DITHER_15 WDMA Dithering Control Register 15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		lsb_err_shift_r				ovflw_bit_r				add_lshift_r				input_rshift_r		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																new_bit_mode
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
30:28		lsb_err_shift_r	RED LSB error bit select
26:24		ovflw_bit_r	RED overflow bit select
22:20		add_lshift_r	RED addend left shift bits
18:16		input_rshift_r	RED input right shift bits
0		new_bit_mode	1: Enables modified test algorithm

14011E40 WDMA_DITHER_16 WDMA Dithering Control Register 16 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		lsb_err_shift_b				ovflw_bit_b				add_lshift_b				input_rshift_b		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		lsb_err_shift_g				ovflw_bit_g				add_lshift_g				input_rshift_g		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		lsb_err_shift_ b	GREEN LSB error bit select
26:24		ovflw_bit_b	GREEN overflow bit select
22:20		add_lshift_b	GREEN addend left shift bits
18:16		input_rshift_b	GREEN input right shift bits
14:12		lsb_err_shift_ g	BLUE LSB error bit select
10:8		ovflw_bit_g	BLUE overflow bit select
6:4		add_lshift_g	BLUE addend left shift bits
2:0		input_rshift_g	BLUE input right shift bits

14011E44 WDMA_DITHER_17 WDMA Dithering Control Register 17 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																crc_rdy
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crc_out															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		crc_rdy	CRC ready
15:0		crc_out	CRC result

14011F00 WDMA_DST_ADDR0 WDMA Destination Address 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Addresso															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Addresso															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	ADDR0	Addresso	**Destination address of image** There is no alignment restriction. For YV12/NV12/NV21 data format, address 0 means the destination of Y.

14011F04 WDMA_DST_ADDR1 WDMA Destination Address 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Address1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Address1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**Address1**	Address1	**U address for YV12 output** UV address for NV12/NV21 output

14011F08 WDMA_DST_ADDR2 WDMA Destination Address 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Address2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Address2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**Address2**	Address2	V address for YV12 output

Module name: DISP_WDMA1 Base address: (+14012000h)

Address	Name	Width	Register Function
14012000	**WDMA_INTEN**	32	WDMA Interrupt Enable
14012004	**WDMA_INTSTA**	32	WDMA Interrupt Status
14012008	**WDMA_EN**	32	WDMA Enable
1401200C	**WDMA_RST**	32	WDMA Reset
14012010	**WDMA_SMI_CON**	32	WDMA SMI Control
14012014	**WDMA_CFG**	32	WDMA Config Register
14012018	**WDMA_SRC_SIZE**	32	WDMA Source Size Register
1401201C	**WDMA_CLIP_SIZE**	32	WDMA Clip Size Register
14012020	**WDMA_CLIP_COORD**	32	WDMA Clip Coordinate Register
14012028	**WDMA_DST_W_IN_BYTE**	32	WDMA Destination Width in Byte
1401202C	**WDMA_ALPHA**	32	WDMA Alpha
14012038	**WDMA_BUF_CON1**	32	WDMA Buffer Control 1
1401203C	**WDMA_BUF_CON2**	32	WDMA Buffer Control 2
14012040	**WDMA_C00**	32	WDMA Matrix Coefficient
14012044	**WDMA_C02**	32	WDMA Matrix Coefficient
14012048	**WDMA_C10**	32	WDMA Matrix Coefficient
1401204C	**WDMA_C12**	32	WDMA Matrix Coefficient
14012050	**WDMA_C20**	32	WDMA Matrix Coefficient
14012054	**WDMA_C22**	32	WDMA Matrix Coefficient
14012058	**WDMA_PRE_ADD0**	32	WDMA Matrix Coefficient

Address	Name	Width	Register Function
1401205C	WDMA_PRE_ADD2	32	WDMA Matrix Coefficient
14012060	WDMA_POST_ADD0	32	WDMA Matrix Coefficient
14012064	WDMA_POST_ADD2	32	WDMA Matrix Coefficient
14012078	WDMA_DST_UV_PITCH	32	WDMA UV Destination Width in Byte
14012080	WDMA_DST_ADDR_OFFSET0	32	WDMA Destination Address Offset 0
14012084	WDMA_DST_ADDR_OFFSET1	32	WDMA Destination Address Offset 1
14012088	WDMA_DST_ADDR_OFFSET2	32	WDMA Destination Address Offset 2
14012090	PROC_TRACK_CON_0	32	DMA Processing Tracking Control 0
14012094	PROC_TRACK_CON_1	32	DMA Processing Tracking Control 1
14012098	PROC_TRACK_CON_2	32	DMA Processing Tracking Control 2
140120A0	WDMA_FLOW_CTRL_DBG	32	WDMA Debug Port of flow_ctrl
140120A4	WDMA_EXEC_DBG	32	WDMA Debug Port of Exec Count
140120A8	WDMA_CT_DBG	32	WDMA Debug Port of Input Counter
140120AC	WDMA_SMI_TRAFFIC_DBG	32	WDMA Debug Port for SMI Traffic
140120B0	WDMA_PROC_TRACK_DBG_0	32	WDMA Debug Port for Process Track 0
140120B4	WDMA_PROC_TRACK_DBG_1	32	WDMA Debug Port for Process Track 1
140120B8	WDMA_DEBUG	32	WDMA Debug Port
14012100	WDMA_DUMMY	32	WDMA Dummy Register
14012E00	WDMA_DITHER_0	32	WDMA Dithering Control Register 0
14012E14	WDMA_DITHER_5	32	WDMA Dithering Control Register 5
14012E18	WDMA_DITHER_6	32	WDMA Dithering Control Register 6
14012E1C	WDMA_DITHER_7	32	WDMA Dithering Control Register 7
14012E20	WDMA_DITHER_8	32	WDMA Dithering Control Register 8
14012E24	WDMA_DITHER_9	32	WDMA Dithering Control Register 9
14012E28	WDMA_DITHER_10	32	WDMA Dithering Control Register 10
14012E2C	WDMA_DITHER_11	32	WDMA Dithering Control Register 11
14012E30	WDMA_DITHER_12	32	WDMA Dithering Control Register 12
14012E34	WDMA_DITHER_13	32	WDMA Dithering Control Register 13
14012E38	WDMA_DITHER_14	32	WDMA Dithering Control Register 14
14012E3C	WDMA_DITHER_15	32	WDMA Dithering Control Register 15
14012E40	WDMA_DITHER_16	32	WDMA Dithering Control Register 16
14012E44	WDMA_DITHER_17	32	WDMA Dithering Control Register 17
14012F00	WDMA_DST_ADDR0	32	WDMA Destination Address 0
14012F04	WDMA_DST_ADDR1	32	WDMA Destination Address 1
14012F08	WDMA_DST_ADDR2	32	WDMA Destination Address 2

14012000 WDMA_INTEN WDMA Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															Frame_Underrun	Frame_Complete
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	**FUE**	Frame_Underrun	**Enables frame underrun interrupt** 0: Disable interrupt 1: Enable interrupt
0	**FCE**	Frame_Complete	**Enables frame completed interrupt** 0: Disable interrupt 1: Enable interrupt

14012004 WDMA_INTSTA **WDMA Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															Frame_Underrun	Frame_Complete
Type															A1	A1
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	**FU**	Frame_Underrun	**Incompletes one frame when WDMA receives EOF** SW writes this bit to clear IRQ. 0: WDMA idle or busy 1: WDMA incompletes one frame
0	**FC**	Frame_Complete	**Completes one frame before WDMA receives EOF** SW writes this bit to clear IRQ. 0: WDMA idle or busy 1: WDMA completes one frame

14012008 WDMA_EN **WDMA Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																Enable
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	EN	Enable	**Enables WDMA or not** 0: Disable WDMA 1: Enable WDMA

1401200C WDMA_RST WDMA Reset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																Soft_Reset
Type																Ao
Reset																0

Bit(s)	Mnemonic	Name	Description
0	RST	Soft_Reset	**Soft reset to WDMA** Write this bit to trigger soft reset. WDMA will reset itself when bus transaction is done. SW must keep polling bit 0 of register WDMA_FLOW_CTRL_DBG until it is 1 to determine if the reset flow is done. 0: Write: No effect; Read: Reset is done . 1: Write: Trigger reset; Read: Reset is on-going.

14012010 WDMA_SMI_CON WDMA SMI Control 02240007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					SMI_V_REPEAT_NUM				SMI_U_REPEAT_NUM				SMI_Y_REPEAT_NUM			
Type					RW				RW				RW			
Reset					0	0	1	0	0	0	1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Slow_Count								Slow_Level			Slow_Enable	Threshold			
Type	RW								RW			RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
27:24	V_NUM	SMI_V_REPEAT_NUM	**Number of continuous V SMI commands** Only takes effects when out_format=YV12/NV12/NV21.
23:20	U_NUM	SMI_U_REPEAT_NUM	**Number of continuous U SMI commands** Only takes effects when out_format=YV12/NV12/NV21.
19:16	Y_NUM	SMI_Y_REPEAT_N	**Number of continuous Y SMI commands**

Bit(s)	Mnemonic	Name	Description
		UM	Only takes effects when out_format=YV12/NV12/NV21.
15:8	**SC**	Slow_Count	**Slow-down counter of each write request** The actual slow-down count of each request is (slow_count*slow_level).
7:5	**SL**	Slow_Level	**Slow-down level of each write request** 0: slow_level=1 1: slow_level=2 2: slow_level=4 4: slow_level=8
4	**SE**	Slow_Enable	**Enables slow-down of each write request or not** 0: Disable slow-down 1: Enable slow-down
3:0	**TH**	Threshold	**Restricts max. burst length of each write request** Max. burst length: Threshold + 1

14012014 WDMA_CFG WDMA Config Register 03020000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_SEL				INT_MTX_SEL										UNI_CONFIG	SWAP
Type	RW				RW										RW	RW
Reset	0	0	0	0	0	0	1	1							1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DNSP_SEL		EXT_MTX_EN	VERTICAL_AVG	CT_EN	UV_SWAP	RGB_SWAP	BYTE_SWAP	Out_Format							
Type	RW		RW	RW	RW	RW	RW	RW	RW							
Reset	0		0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:28	**DEBUG_SEL**	DEBUG_SEL	**For WDMA debugging selection**
27:24	**INT_MTX_SEL**	INT_MTX_SEL	**Selects pre-defined color transformation coefficient** 4'b0000: RGB to JPEG 4'b0010: RGB to BT601 4'b0011: RGB to BT709 4'b0100: JPEG to RGB 4'b0110: BT601 to RGB 4'b0111: BT709 to RGB 4'b1000: JPEG to BT601 4'b1001: JPEG to BT709 4'b1010: BT601 to JPEG 4'b1011: BT709 to JPEG 4'b1100: BT709 to BT601 4'b1101: BT601 to BT709
17	**UNICON**	UNI_CONFIG	**Uses uniform config or not** Do not modify this bit. 0: Disable uniform config 1: Enable uniform config
16	**SWAP**	SWAP	**Enables swap function to translate the output data format** Translated output data format: RGB565 -> BGR565 RGB888 -> BGR888 RGBA8888 -> BGRA8888

Bit(s)	Mnemonic	Name	Description
			ARGB8888 -> ABGR8888 UYVY -> VYUY YUY2 -> YVYU IYUV -> YV12 NV12 -> NV21 0: Disable swap 1: Enable swap
15	**DNSP_SEL**	DNSP_SEL	**Selects YUV444 to YUV422 mode** 0: Drop odd pixel U/V 1: Apply [1 2 1] filter for U/V
13	**EXT_MTX_EN**	EXT_MTX_EN	**Enables color transformation external coefficients or not** For internal coefficient, use INT_MTX_SEL to select the pre-defined coefficients. For external coefficient, use register WDMA_C00 -> WDMA_POST_ADD. 0: Use internal coefficients for color transformation 1: Use External coefficients for color transformation
12	**V_AVG**	VERTICAL_AVG	**Enables vertical average or not** 0: Drop odd line pixels 1: Average in vertical while YUV444->YUV420
11	**CT_EN**	CT_EN	**Enables color transformation matrix or not** 0: Bypass color transformation matrix 1: Do color transformation
10	**UVS**	UV_SWAP	**Enables uv_swap or not** If the output format is UYVY (y1 v0 y0 u0), it will become (y1 u0 y0 v0) after UV swap. It takes no effect only when legacy mode and the output format is in RGB domain. 0: Disable uv swap 1: Enable uv swap
9	**RGBS**	RGB_SWAP	**Enables rgb_swap or not** If the output format is ARGB, it will become ABGR after RGB swap. It takes no effect only when legacy mode and the output format is in YUV domain. 0: Disable rgb swap 1: Enable rgb swap
8	**BYTES**	BYTE_SWAP	**Enables byte_swap or not** Takes no effect when output format is RGB565 or RGB888. If the output format is ARGB, it will become BGRA after byte swap. If the output format is UYVY(y1 v0 y0 u0), it will become (v0 y1 u0 y0) after byte swap. Only works in legacy mode. 0: Disable byte swap 1: Enable byte swap
7:4	**OF**	Out_Format	**Specifies output format of WDMA** 0: RGB565 1: RGB888 2: BGRA8888 3: ARGB8888 4: UYVY 5: YUY2 7: Y-only 8: IYUV (I420) 12: NV12

14012018 WDMA_SRC_SIZE **WDMA Source Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			Height													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			Width													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:16	**HGT**	Height	**Source height in pixels** Range: 0 ~ 2,047
13:0	**WTH**	Width	**Source width in pixels** Range: 0 ~ 2,047

1401201C WDMA_CLIP_SIZE **WDMA Clip Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			Height													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			Width													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:16	**HGT**	Height	**Clip height in pixels** Range: 0 ~ 2,047
13:0	**WTH**	Width	**Clip width in pixels** Range: 0 ~ 2,047

14012020 WDMA_CLIP_COORD **WDMA Clip Coordinate Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			Y_coord													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			X_coord													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:16	**CY**	Y_coord	**Y coordinate in pixels of clipped image** Range: 0 ~ 2,047

Bit(s)	Mnemonic	Name	Description
13:0	**CX**	X_coord	**X coordinate in pixels of clipped image** Range: 0 ~ 2,047

14012028 WDMA_DST_W_IN_BYTE **WDMA Destination Width in Byte** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dst_W_in_Byte															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**DWB**	Dst_W_in_Byte	**Destination width in bytes of each scan line** It is width*bpp. bpp: RGB565 -> 2, RGB888->3, ARGB->4, YV12->1, NV12->1, NV21->1

1401202C WDMA_ALPHA **WDMA Alpha** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	A_Sel															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									A_Value							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**ASEL**	A_Sel	**Selects A source from pixel alpha or specified alpha** 0: Select pixle alpha from OVL 1: Select specfied A value
7:0	**A**	A_Value	**Specified A value**

14012038 WDMA_BUF_CON1 **WDMA Buffer Control 1** **10100100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ultra_Enable	Pre_Ultra_Enable		Frame_End_Ultra				issue_req_th								
Type	RW	RW		RW				RW								
Reset	0	0		1				0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name								fifo_pseudo_size								
Type								RW								
Reset								1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**UE**	Ultra_Enable	**Enables ultra high request not**
30	**PUE**	Pre_Ultra_Enab le	**Enables pre-ultra high request**
28	**FEU**	Frame_End_Ultr a	**WDMA issues ultra high command at the end of the frame.**
24:16	**REQ_TH**	issue_req_th	**Threshold of data amount to release data from WDMA** WDMA starts sending data only when data amount in FIFO is larger than the set value.
8:0	**FIFO_SIZE**	fifo_pseudo_si ze	**Actually used FIFO entries** Keep it at default value. MDP_WDMA: 128. DISP_WDMA: 256.

1401203C WDMA_BUF_CON2 **WDMA Buffer Control 2** **10101010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ultra_th_high_ofs								pre_ultra_th_high_ofs							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ultra_th_low_ofs								pre_ultra_th_low							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**UL_H_OFFSET**	ultra_th_high_ ofs	**UH (ultra high threshold) = PUH + ultra_th_high_ofs** If FIFO size of WMDA > UH, WDMA will assert ultra high request.
23:16	**PUL_H_OFFSET**	pre_ultra_th_h igh_ofs	**PUH (pre_ultra high threshold) = UL + pre_ultra_th_high_ofs** If FIFO size of WMDA > PUH, WDMA will assert pre-ultra high request.
15:8	**UL_L_OFFSET**	ultra_th_low_o fs	**UL (ultra low threshold) = PUL + ultra_th_low_ofs** If FIFO size of WMDA < UL, WDMA will de-assert ultra high request.
7:0	**PUL_L_OFFSET**	pre_ultra_th_l ow	**PUL (pre_ultra low threshold) = pre_ultra_th_low** If FIFO size of WMDA < PUL, WDMA will de-assert pre-ultra high request.

14012040 WDMA_C00 **WDMA Matrix Coefficient** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C01												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C00												

Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	C01	C01	Matrix coefficient of C01
12:0	C00	C00	Matrix coefficient of C00

14012044 WDMA_C02 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C02												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0	C02	C02	Matrix coefficient of C02

14012048 WDMA_C10 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C11												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C10												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	C11	C11	Matrix coefficient of C11
12:0	C10	C10	Matrix coefficient of C10

1401204C WDMA_C12 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C12												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
12:0	**C12**	C12	Matrix coefficient of C12

14012050 WDMA_C20 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				C21												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C20												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**C21**	C21	Matrix coefficient of C21
12:0	**C20**	C20	Matrix coefficient of C20

14012054 WDMA_C22 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				C22												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0	**C22**	C22	Matrix coefficient of C22

14012058 WDMA_PRE_ADD0 WDMA Matrix Coefficient 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								PRE_ADD_1								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								PRE_ADD_0								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16	**PREADD1**	PRE_ADD_1	Matrix coefficient of pre add1
8:0	**PREADD0**	PRE_ADD_0	Matrix coefficient of pre add0

1401205C WDMA_PRE_ADD2 — **WDMA Matrix Coefficient** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								PRE_ADD_2								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0	**PREADD2**	PRE_ADD_2	Matrix coefficient of pre add2

14012060 WDMA_POST_ADD0 — **WDMA Matrix Coefficient** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								POST_ADD_1								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								POST_ADD_0								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16	**POSTADD1**	POST_ADD_1	Matrix coefficient of post add1
8:0	**POSTADD0**	POST_ADD_0	Matrix coefficient of post add0

14012064 WDMA_POST_ADD2 — **WDMA Matrix Coefficient** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								POST_ADD_2								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0	**POSTADD2**	POST_ADD_2	Matrix coefficient of post add2

14012078 WDMA_DST_UV_PITCH — **WDMA UV Destination Width in Byte** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UV_Dst_W_in_Byte															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**UV_Dst_W_in_Byte**	UV_Dst_W_in_By te	UV pitch for YV12/NV12/NV21 output

14012080 WDMA_DST_ADDR_OFFSET **WDMA Destination Address Offset 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					WDMA_Destination_Address_offseto											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_Destination_Address_offseto															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:0	**Address_offset 0**	WDMA_Destinati on_Address_off seto	**WDMA destination address offset 0** Final destination address = DST_ADDR + DST_ADDR_OFFSET

14012084 WDMA_DST_ADDR_OFFSET1 **WDMA Destination Address Offset 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					WDMA_Destination_Address_offset1											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_Destination_Address_offset1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:0	**Address_offset 1**	WDMA_Destinati on_Address_off set1	**WDMA destination address offset 1** U address offset for YV12 output; UV address offset for NV12/NV21 output

14012088 WDMA_DST_A **WDMA Destination Address** **00000000**

DDR_OFFSET2 **Offset 2**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					WDMA_Destination_Address_offset2											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_Destination_Address_offset2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:0	**Address_offset 2**	WDMA_Destination_Address_offset2	**WDMA destination address offset 2** V address offset for YV12 output

14012090 **PROC_TRACK_CON_0** **DMA Processing Tracking Control 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		IGNORE_INIT_LATENCY	STOP_GREQ_EN	PROC_PRE_ULTRA_EN												
Type		RW	RW	RW												
Reset		0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TRACK_WINDOW											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30		IGNORE_INIT_LATENCY	**Ignores initial latency from SOF to the first proc_one**
29		STOP_GREQ_EN	**Enables stop_greq of the process tracking**
28		PROC_PRE_ULTRA_EN	**Enables pre_ultra of process tracking** If this bit is enabled, pre_ultra will be contolled by process tracking unit.
11:0		TRACK_WINDOW	**Tracking window** Unit: bclk_ck cycle

14012094 **PROC_TRACK_CON_1** **DMA Processing Tracking Control 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									TARGET_CNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TARGET_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		TARGET_CNT	**Targets process count during a TRACK_WINDOW** It is s a 16.8 fix point number.

14012098 PROC_TRACK_CON_2 **DMA Processing Tracking Control 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									STOP_CNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STOP_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		STOP_CNT	If processing counter > STOP_CNT, stop issuing greq.

140120A0 WDMA_FLOW_CTRL_DBG **WDMA Debug Port of flow_ctrl** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_IN_REQ	WDMA_IN_ACK	WDMA_GREQ	WDMA_FIFO_FULL			WDMA_STATE									
Type	RU	RU	RU	RU			RU									
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
15	**WDMA_IN_REQ**	WDMA_IN_REQ	**WDMA input request** IN_REQ=1 means the previous engine is sending data to WDMA and waiting for response from WDMA.
14	**WDMA_IN_ACK**	WDMA_IN_ACK	**Acknowledges WDMA input** IN_ACK=1 means WDMA is ready for the next pixel and is waiting for the previous engine to send the next pixel.
13	**WDMA_GREQ**	WDMA_GREQ	**WDMA SMI request** GREQ=1 means that WDMA is sending out an SMI request but no response from LARB.
12	**WDMA_FIFO_FULL**	WDMA_FIFO_FULL	**WDMA FIFO status is full or not**
9:0	**WDMA_STATE**	WDMA_STATE	**WDMA state machine** Read the current status of WDMA here. 00_0000_0001: Idle state 00_0000_0010: Clear state 00_0000_0100: Prepare state 1 00_0000_1000: Prepare state 2 00_0001_0000: Data transmit state

Bit(s)	Mnemonic	Name	Description
			00_0010_0000: EOF prepare state 00_0100_0000: SW reset prepare state 00_1000_0000: EOF wait idle state 01_0000_0000: SW reset wait idle state 10_0000_0000: Frame completed state

140120A4 WDMA_EXEC_DBG **WDMA Debug Port of Exec Count** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											WDMA_FRAME_COMPLETE_CNT					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											WDMA_FRAME_RUN_CNT					
Type											RU					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:16	**CDBG**	WDMA_FRAME_COMPLETE_CNT	**Debugging status of complete cnt** When WDMA completes one frame (not SW reset or EOF reset), this counter will increase.
5:0	**EDBG**	WDMA_FRAME_RUN_CNT	**Debugging status of exec cnt** When WDMA receives SOF signal (Start Of Frame) from the MUTEX, this counter will increase.

140120A8 WDMA_CT_DBG **WDMA Debug Port of Input Counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			WDMA_INPUT_CNT_Y													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			WDMA_INPUT_CNT_X													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:16	**WDMA_INPUT_CNT_Y**	WDMA_INPUT_CNT_Y	**WDMA input counter in Y axis**
13:0	**WDMA_INPUT_CNT_X**	WDMA_INPUT_CNT_X	**WDMA input counter in X axis** How many pixels in a line are received by the WDMA. The total amount of received pixels is WDMA_INPUT_CNT_Y*SRC_W + WDMA_INPUT_CNT_X.

140120AC WDMA_SMI_TRAFFIC_DBG **WDMA Debug Port for SMI Traffic** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_SMI_TRAFFIC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_SMI_TRAFFIC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**WDMA_SMI_STATUS**	WDMA_SMI_TRAFFIC	**Traffic status between WDMA and SMI** This counter should be 0 while WDMA is being sw reset.

140120B0 WDMA_PROC_TRACK_DBG **WDMA Debug Port for Process Track 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_PROC_CNT_MAX															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_PROC_CNT_MAX															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**WDMA_PROC_TRACK_MAX**	WDMA_PROC_CNT_MAX	**Process tracking status counter max. value** Write this register to clear the counter.

140120B4 WDMA_PROC_TRACK_DBG_1 **WDMA Debug Port for Process Track 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_PROC_CNT_MIN															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_PROC_CNT_MIN															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**WDMA_PROC_TRACK_MIN**	WDMA_PROC_CNT_MIN	**Process tracking status counter min. value** Write this register to clear the counter.

140120B8 WDMA_DEBUG **WDMA Debug Port** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_STA_DEBUG															

Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_STA_DEBUG															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CDBG**	WDMA_STA_DEBUG	Trivil debugging status of WDMA

14012100 WDMA_DUMMY WDMA Dummy Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DUMMY**	WDMA_DUMMY	WDMA dummy register

14012E00 WDMA_DITHER_0 WDMA Dithering Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								crc_clr				crc_start				crc_cen
Type								RW				RW				RW
Reset								0				0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	frame_done_del											out_sel				start
Type	RW											RW				RW
Reset	0	0	0	0	0	0	0	0				0				0

Bit(s)	Mnemonic	Name	Description
24		crc_clr	Write 1 to clear CRC result.
20		crc_start	Write 1 to start CRC counting.
16		crc_cen	
15:8		frame_done_del	Frame done return delay
4		out_sel	
0		start	

14012E14 WDMA_DITHER_5 WDMA Dithering Control Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	w_demo															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		w_demo	Short line length

14012E18 WDMA_DITHER_6 **WDMA Dithering Control Register 6** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																wrap_mode
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	left_en		fphase_r	fphase_en			fphase						round_en	rdither_en	lfsr_en	edither_en
Type	RW		RW	RW			RW						RW	RW	RW	RW
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		wrap_mode	**Enales rounding for dithering function** When rounding method is used, both running order and error dispersion cannot be used.
15:14		left_en	**Enables left part of screen dither** 0: Dither runs at full screen. 1: Dither runs at left part of screen.
13		fphase_r	**Dither SubPixel addend**
12		fphase_en	**Enables running order dithering frame phase control**
9:4		fphase	**Running order dithering frame phase increment.** *Note:* *1. If ROUND_EN = 1, the output will only be rounding (no matter what RDITHER_EN and EDITHER_EN settings are).* *2. RDITHER_EN and EDITHER_EN can work together.*
3		round_en	**Enables rounding for dithering function** When rounding method is used, both running order and error dispersion cannot be used.
2		rdither_en	**Enables running order dithering** Running order dithering must be set when ROUND_EN is set to 0. Running order dithering can run with error dispersion when EDOTHER_EN is set to 1.
1		lfsr_en	**Enables LFSR-type dithering**
0		edither_en	**Enables error dispersion dithering** Error dispersion dithering must be set when ROUND_EN is set to 0. Running order dithering can run with error dispersion when RDITHER_EN is set to 1.

Bit(s)	Mnemonic	Name	Description

14012E1C WDMA_DITHER_7 WDMA Dithering Control Register 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							drmo d_b				drmod_g				drmod_r	
Type							RW				RW				RW	
Reset							0	0			0	0			0	0

Bit(s)	Mnemonic	Name	Description
9:8		drmod_b	**Selects dither mode** 0: No dither 1: 12-bit dither to 10-bit 2: 12-bit dither to 8-bit 3: 12-bit dither to 6-bit
5:4		drmod_g	**Selects dither mode** 0: No dither 1: 12-bit dither to 10-bit 2: 12-bit dither to 8-bit 3: 12-bit dither to 6-bit
1:0		drmod_r	**Selects dither mode** 0: No dither 1: 12-bit dither to 10-bit 2: 12-bit dither to 8-bit 3: 12-bit dither to 6-bit

14012E20 WDMA_DITHER_8 WDMA Dithering Control Register 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ink_ data _r									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ink
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
25:16		ink_data_r	Ink data for R
0		ink	Enables ink

14012E24 WDMA_DITHER_9 WDMA Dithering Control Register 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ink_data_b									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							ink_data_g									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25:16		ink_data_b	Ink data for B
9:0		ink_data_g	Ink data for G

14012E28 WDMA_DITHER_10 WDMA Dithering Control Register 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						fpha se_b it					fphase_se l				fphase_ct rl	
Type						RW					RW				RW	
Reset						0	0	0			0	0			0	0

Bit(s)	Mnemonic	Name	Description
10:8		fphase_bit	**fphase_bit XOR bus number** *Note: This function checks reg_fphase_sel.* Only 0, 1, 2, 4 and 6 are available. 0: No effect on fphase (XOR disabled)
5:4		fphase_sel	**fphase XOR function: fphase do self bit-wise xor** *Note: This function checks reg_fphase_sel. Only bit 2, bit 4 and bit 6 are available.* 0: Disable fphase XOR 1: Effect fphase[0]~[1] based on the value of reg_fphase_sel is 1 or 2. 2: Effect fphase[0]~[3] based on the value of reg_fphase_sel is 1, 2 or 4. 3: Effect fphase[0]~[5] based on the value of reg_fphase_sel is 1, 2, 4 or 6.
1:0		fphase_ctrl	**Selects fphase range to add with rdither table.** 00: 0~63 01: 0~16 10: 0~3

14012E2C WDMA_DITHER_11 WDMA Dithering Control Register 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			sub_ b				sub_ g				sub_r					subpix_en
Type			RW				RW				RW					RW
Reset			0	0			0	0			0	0				0

Bit(s)	Mnemonic	Name	Description
13:12		sub_b	**Dither SubPixel addend**
9:8		sub_g	**Dither SubPixel addend**
5:4		sub_r	**Dither SubPixel addend**
0		subpix_en	**Enables sub pix dither mode** 0: Pix dither mode 1: Sub pix dither mode

14012E30 WDMA_DITHER_12 WDMA Dithering Control Register 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	h_active															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											table_en					lsb_off
Type											RW					RW
Reset											0	0				0

Bit(s)	Mnemonic	Name	Description
31:16		h_active	**Active region of dither IP**
5:4		table_en	**Active bit of magic table for running order** 01: Phase active in bit 3 ~ bit 0 10: Phase active in bit 1 ~ bit 0 Others: Phase active in bit 5 ~ bit 0
0		lsb_off	**Turns off LSB for dither function**

14012E34 WDMA_DITHER_13 WDMA Dithering Control Register 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						rshi ft_b				rshift_g				rshift_r		
Type						RW				RW				RW		
Reset						0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
10:8		rshift_b	B right shift position after IP output
6:4		rshift_g	G right shift position after IP output
2:0		rshift_r	R right shift position after IP output

Bit(s)	Mnemonic	Name	Description

14012E38 WDMA_DITHER_14 WDMA Dithering Control Register 14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							debug_mode			diff_shift						testpin_en
Type							RW			RW						RW
Reset							0	0		0	0	0				0

Bit(s)	Mnemonic	Name	Description
9:8		debug_mode	1: Enables debugging mode
6:4		diff_shift	Debugging mode difference shift positions
0		testpin_en	Enables testpin input

14012E3C WDMA_DITHER_15 WDMA Dithering Control Register 15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		lsb_err_shift_r				ovflw_bit_r				add_lshift_r				input_rshift_r		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																new_bit_mode
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
30:28		lsb_err_shift_r	RED LSB error bit select
26:24		ovflw_bit_r	RED overflow bit select
22:20		add_lshift_r	RED addend left shift bits
18:16		input_rshift_r	RED input right shift bits
0		new_bit_mode	1: Enables modified test algorithm

14012E40 WDMA_DITHER_16 WDMA Dithering Control Register 16 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		lsb_err_shift_b				ovflw_bit_b				add_lshift_b				input_rshift_b		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		lsb_err_shift_g				ovflw_bit_g				add_lshift_g				input_rshift_g		

Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30:28		lsb_err_shift_ b	GREEN LSB error bit select
26:24		ovflw_bit_b	GREEN overflow bit select
22:20		add_lshift_b	GREEN addend left shift bits
18:16		input_rshift_b	GREEN input right shift bits
14:12		lsb_err_shift_ g	BLUE LSB error bit select
10:8		ovflw_bit_g	BLUE overflow bit select
6:4		add_lshift_g	BLUE addend left shift bits
2:0		input_rshift_g	BLUE input right shift bits

14012E44 WDMA_DITHER_17 — WDMA Dithering Control Register 17 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																crc_rdy
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crc_out															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		crc_rdy	CRC ready
15:0		crc_out	CRC result

14012F00 WDMA_DST_ADDR0 — WDMA Destination Address 0 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Addresso															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Addresso															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	ADDR0	Addresso	**Destination address of image** There is no alignment restriction. For YV12/NV12/NV21 data format, address 0 means the destination of Y.

14012F04 WDMA_DST_ADDR1 — WDMA Destination Address 1 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	Address1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Address1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**Address1**	Address1	**U address for YV12 output** UV address for NV12/NV21 output

14012F08 WDMA_DST_ADDR2 WDMA Destination Address 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Address2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Address2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**Address2**	Address2	V address for YV12 output

Module name: DISP_COLOR Base address: (+14013000h)
Module name: MDP_COLOR Base address: (+1400a000h)

Address	Name	Width	Register Function
14013400	DISP_COLOR_CFG_MAIN	32	Configuration
14013404	DISP_COLOR_PXL_CNT_MAIN	32	Pixel Counter
14013408	DISP_COLOR_LINE_CNT_MAIN	32	Line Counter
1401340C	DISP_COLOR_WIN_X_MAIN	32	Window X
14013410	DISP_COLOR_WIN_Y_MAIN	32	Window Y
14013418	DISP_COLOR_TIMING_DETECTION_0	32	Timing Detection 0
1401341C	DISP_COLOR_TIMING_DETECTION_1	32	Timing Detection 1
14013420	DISP_COLOR_DBG_CFG_MAIN	32	Debug Mode Config
14013428	DISP_COLOR_C_BOOST_MAIN	32	Chroma Boost
1401342C	DISP_COLOR_C_BOOST_MAIN_2	32	Chroma Boost 2

Address	Name	Width	Register Function
14013430	DISP_COLOR_LUMA_ADJ	32	Input Y Level Adjust
14013434	DISP_COLOR_G_PIC_ADJ_MAIN_1	32	Global Picture Adjustment
14013438	DISP_COLOR_G_PIC_ADJ_MAIN_2	32	Global Picture Adjustment
14013484	DISP_COLOR_POS_MAIN	32	Position X
14013488	DISP_COLOR_INK_DATA_MAIN	32	Ink Data Y
1401348C	DISP_COLOR_INK_DATA_MAIN_CR	32	Ink Data Cr
14013490	DISP_COLOR_CAP_IN_DATA_MAIN	32	Capture In Data Y
14013494	DISP_COLOR_CAP_IN_DATA_MAIN_CR	32	Capture In Data Cr
14013498	DISP_COLOR_CAP_OUT_DATA_MAIN	32	Capture Out Data Y
1401349C	DISP_COLOR_CAP_OUT_DATA_MAIN_CR	32	Capture Out Data Cr
140134A0	DISP_COLOR_Y_SLOPE_1_0_MAIN	32	Y Slope 1, 0
140134A4	DISP_COLOR_Y_SLOPE_3_2_MAIN	32	Y Slope 3, 2
140134A8	DISP_COLOR_Y_SLOPE_5_4_MAIN	32	Y Slope 5, 4
140134AC	DISP_COLOR_Y_SLOPE_7_6_MAIN	32	Y Slope 7, 6
140134B0	DISP_COLOR_Y_SLOPE_9_8_MAIN	32	Y Slope 9, 8
140134B4	DISP_COLOR_Y_SLOPE_11_10_MAIN	32	Y Slope 11, 10
140134B8	DISP_COLOR_Y_SLOPE_13_12_MAIN	32	Y Slope 13, 12
140134BC	DISP_COLOR_Y_SLOPE_15_14_MAIN	32	Y Slope 15, 14
14013620	DISP_COLOR_LOCAL_HUE_CD_0	32	Local Hue Cost Down 0
14013624	DISP_COLOR_LOCAL_HUE_CD_1	32	Local Hue Cost Down 1
14013628	DISP_COLOR_LOCAL_HUE_CD_2	32	Local Hue Cost Down 2
1401362C	DISP_COLOR_LOCAL_HUE_CD_3	32	Local Hue Cost Down 3
14013630	DISP_COLOR_LOCAL_HUE_CD_4	32	Local Hue Cost Down 4
14013740	DISP_COLOR_TWO_D_WINDOW_1	32	Two D Window 1
1401374C	DISP_COLOR_TWO_D_W1_RESULT	32	Two D Window 1 Result
14013768	DISP_COLOR_SAT_HIST_X_CFG_MAIN	32	Saturation Histogram Horizontal Range

Address	Name	Width	Register Function
1401376C	DISP_COLOR_SAT_HIST_Y_CFG_MAIN	32	Saturation Histogram Vertical Range
1401379C	DISP_COLOR_BWS_2	32	Black White Stretch 2
140137E0	DISP_COLOR_CRC_0	32	CRC_0
140137E4	DISP_COLOR_CRC_1	32	CRC_1
140137E8	DISP_COLOR_CRC_2	32	CRC_2
140137EC	DISP_COLOR_CRC_3	32	CRC_3
140137F0	DISP_COLOR_CRC_4	32	CRC_4
140137FC	DISP_COLOR_PARTIAL_SAT_GAIN1_0	32	Partial Sat Gain 1 from Hue Phase 0 to 3
14013800	DISP_COLOR_PARTIAL_SAT_GAIN1_1	32	Partial Sat Gain 1 from Hue Phase 4 to 7
14013804	DISP_COLOR_PARTIAL_SAT_GAIN1_2	32	Partial Sat Gain 1 from Hue Phase 8 to 11
14013808	DISP_COLOR_PARTIAL_SAT_GAIN1_3	32	Partial Sat Gain 1 from Hue Phase 12 to 15
1401380C	DISP_COLOR_PARTIAL_SAT_GAIN1_4	32	Partial Sat Gain 1 from Hue Phase 16 to 19
14013810	DISP_COLOR_PARTIAL_SAT_GAIN2_0	32	Partial Sat Gain 2 from Hue Phase 0 to 3
14013814	DISP_COLOR_PARTIAL_SAT_GAIN2_1	32	Partial Sat Gain 2 from Hue Phase 4 to 7
14013818	DISP_COLOR_PARTIAL_SAT_GAIN2_2	32	Partial Sat Gain 2 from Hue Phase 8 to 11
1401381C	DISP_COLOR_PARTIAL_SAT_GAIN2_3	32	Partial Sat Gain 2 from Hue Phase 12 to 15
14013820	DISP_COLOR_PARTIAL_SAT_GAIN2_4	32	Partial Sat Gain 2 from Hue Phase 16 to 19
14013824	DISP_COLOR_PARTIAL_SAT_GAIN3_0	32	Partial Sat Gain 3 from Hue Phase 0 to 3
14013828	DISP_COLOR_PARTIAL_SAT_GAIN3_1	32	Partial Sat Gain 3 from Hue Phase 4 to 7
1401382C	DISP_COLOR_PARTIAL_SAT_GAIN3_2	32	Partial Sat Gain 3 from Hue Phase 8 to 11
14013830	DISP_COLOR_PARTIAL_SAT_GAIN3_3	32	Partial Sat Gain 3 from Hue Phase 12 to 15
14013834	DISP_COLOR_PARTIAL_SAT_GAIN3_4	32	Partial Sat Gain 3 from Hue Phase 16 to 19
14013838	DISP_COLOR_PARTIAL_SAT_POINT1_0	32	Partial Sat Point 1 from Hue Phase 0 to 3
1401383C	DISP_COLOR_PARTIAL_SAT_POINT1_1	32	Partial Sat Point 1 from Hue Phase 4 to 7
14013840	DISP_COLOR_PARTIAL_SAT_POINT1_2	32	Partial Sat Point 1 from Hue Phase 8 to 11
14013844	DISP_COLOR_PAR	32	Partial Sat Point 1 from Hue Phase 12 to 15

Address	Name	Width	Register Function
	TIAL_SAT_POINT_1_3		
14013848	DISP_COLOR_PARTIAL_SAT_POINT_1_4	32	Partial Sat Point 1 from Hue Phase 16 to 19
1401384C	DISP_COLOR_PARTIAL_SAT_POINT_2_0	32	Partial Sat Point 2 from Hue Phase 0 to 3
14013850	DISP_COLOR_PARTIAL_SAT_POINT_2_1	32	Partial Sat Point 2 from Hue Phase 4 to 7
14013854	DISP_COLOR_PARTIAL_SAT_POINT_2_2	32	Partial Sat Point 2 from Hue Phase 8 to 11
14013858	DISP_COLOR_PARTIAL_SAT_POINT_2_3	32	Partial Sat Point 2 from Hue Phase 12 to 15
1401385C	DISP_COLOR_PARTIAL_SAT_POINT_2_4	32	Partial Sat Point 2 from Hue Phase 16 to 19
14013C00	DISP_COLOR_START	32	Configuration
14013C04	DISP_COLOR_INTEN	32	Interrupt Enable
14013C08	DISP_COLOR_INTSTA	32	Interrupt Status
14013C0C	DISP_COLOR_OUT_SEL	32	Output Bits Configuration
14013C10	DISP_COLOR_FRAME_DONE_DEL	32	Frame Done Delay Select
14013C14	DISP_COLOR_CRC	32	CRC Enable
14013C18	DISP_COLOR_SW_SCRATCH	32	Software Scratch
14013C28	DISP_COLOR_CK_ON	32	Clock Force on
14013C50	DISP_COLOR_INTERNAL_IP_WIDTH	32	Wrapper Internal IP Width
14013C54	DISP_COLOR_INTERNAL_IP_HEIGHT	32	Wrapper Internal IP Height
14013C60	DISP_COLOR_CM1_EN	32	Front Color Transform Enable
14013CA0	DISP_COLOR_CM2_EN	32	Back Color Transform Enable
14013CF0	DISP_COLOR_R0_CRC	32	Wrapper R0 CRC
14013CF4	DISP_COLOR_S_GAIN_BY_Y0_0	32	S Gain by Y0 from Hue Phase 0 to 3
14013CF8	DISP_COLOR_S_GAIN_BY_Y0_1	32	S Gain by Y0 from Hue Phase 4 to 7
14013CFC	DISP_COLOR_S_GAIN_BY_Y0_2	32	S Gain by Y0 from Hue Phase 8 to 11
14013D00	DISP_COLOR_S_GAIN_BY_Y0_3	32	S Gain by Y0 from Hue Phase 12 to 15
14013D04	DISP_COLOR_S_GAIN_BY_Y0_4	32	S Gain by Y0 from Hue Phase 16 to 19

Address	Name	Width	Register Function
14013D08	DISP_COLOR_S_GAIN_BY_Y64_0	32	S Gain by Y64 from Hue Phase 0 to 3
14013D0C	DISP_COLOR_S_GAIN_BY_Y64_1	32	S Gain by Y64 from Hue Phase 4 to 7
14013D10	DISP_COLOR_S_GAIN_BY_Y64_2	32	S Gain by Y64 from Hue Phase 8 to 11
14013D14	DISP_COLOR_S_GAIN_BY_Y64_3	32	S Gain by Y64 from Hue Phase 12 to 15
14013D18	DISP_COLOR_S_GAIN_BY_Y64_4	32	S Gain by Y64 from Hue Phase 16 to 19
14013D1C	DISP_COLOR_S_GAIN_BY_Y128_0	32	S Gain by Y128 from Hue Phase 0 to 3
14013D20	DISP_COLOR_S_GAIN_BY_Y128_1	32	S Gain by Y128 from Hue Phase 4 to 7
14013D24	DISP_COLOR_S_GAIN_BY_Y128_2	32	S Gain by Y128 from Hue Phase 8 to 11
14013D28	DISP_COLOR_S_GAIN_BY_Y128_3	32	S Gain by Y128 from Hue Phase 12 to 15
14013D2C	DISP_COLOR_S_GAIN_BY_Y128_4	32	S Gain by Y128 from Hue Phase 16 to 19
14013D30	DISP_COLOR_S_GAIN_BY_Y192_0	32	S Gain by Y192 from Hue Phase 0 to 3
14013D34	DISP_COLOR_S_GAIN_BY_Y192_1	32	S Gain by Y192 from Hue Phase 4 to 7
14013D38	DISP_COLOR_S_GAIN_BY_Y192_2	32	S Gain by Y192 from Hue Phase 8 to 11
14013D3C	DISP_COLOR_S_GAIN_BY_Y192_3	32	S Gain by Y192 from Hue Phase 12 to 15
14013D40	DISP_COLOR_S_GAIN_BY_Y192_4	32	S Gain by Y192 from Hue Phase 16 to 19
14013D44	DISP_COLOR_S_GAIN_BY_Y256_0	32	S Gain by Y256 from Hue Phase 0 to 3
14013D48	DISP_COLOR_S_GAIN_BY_Y256_1	32	S Gain by Y256 from Hue Phase 4 to 7
14013D4C	DISP_COLOR_S_GAIN_BY_Y256_2	32	S Gain by Y256 from Hue Phase 8 to 11
14013D50	DISP_COLOR_S_GAIN_BY_Y256_3	32	S Gain by Y256 from Hue Phase 12 to 15
14013D54	DISP_COLOR_S_GAIN_BY_Y256_4	32	S Gain by Y256 from Hue Phase 16 to 19
14013D58	DISP_COLOR_LSP_1	32	LSP Reg Group 1
14013D5C	DISP_COLOR_LSP_2	32	LSP Reg Group 2

14013400 DISP_COLOR_CFG_MAIN Configuration 00202080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									LSP_SAT_SRC	LSP_INK_EN	LSP_SAT_LIMIT	LSP_EN	c_pp _cm_ dbg_ sel			
Type									RW	RW	RW	RW	RW			

Reset									0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	S_GAIN_BY_Y_EN		SEQ_SEL					wide_gamut_en	ALLBP			HEBP	SEBP	YEBP	P2CBP	C2PBP
Type	RW		RW					RW	RW			RW	RW	RW	RW	RW
Reset	0		1					0	1			0	0	0	0	0

Bit(s)	Name	Description
23	LSP_SAT_SRC	**Selects ref sat of low sat protection** 0: Luma engine output sat (sat engine input sat) 1: C2P output sat (hue engine input sat)
22	LSP_INK_EN	**Enables low sat protection ink** 0: Disable 1: Normal function
21	LSP_SAT_LIMIT	**Sat limited by low sat protection** 0: Disable 1: Output S <= Input S
20	LSP_EN	**Enables low sat protection** 0: Disable 1: Normal function
19:16	c_pp_cm_dbg_sel	**Selects debug signals**
15	S_GAIN_BY_Y_EN	**Enables S gain by Y** 0: Disable 1: Normal function
13	SEQ_SEL	**Hue/Luma/Saturation engines sequence** 0: 65/95 sequence 1: 68/96 sequence
8	wide_gamut_en	**Enables wide gamut transformation**
7	ALLBP	**Bypasses all engines** 0: Normal function 1: Bypass
4	HEBP	**Bypasses hue engine** 0: Normal function 1: Bypass
3	SEBP	**Bypasses saturation engine** 0: Normal function 1: Bypass
2	YEBP	**Bypasses luma engine** 0: Normal function 1: Bypass
1	P2CBP	**Bypasses polar to Cartesian engine** 0: Normal function 1: bypass
0	C2PBP	**Bypasses Cartesian to polar engine** 0: Normal function 1: Bypass

14013404 DISP_COLOR_PXL_CNT_MAIN **Pixel Counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	H_CONT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	H_CONT	Current horizontal pixel counter

14013408 DISP_COLOR_LINE_CNT_MAIN Line Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	V_CONT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LINE_CONT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	V_CONT	Current vertical pixel counter
15:0	LINE_CONT	Current vertical line counter

1401340C DISP_COLOR_WIN_X_MAIN Window X FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WIN_X_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WIN_X_START															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	WIN_X_END	X end for processing window
15:0	WIN_X_START	X start for processing window

14013410 DISP_COLOR_WIN_Y_MAIN Window Y FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WIN_Y_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WIN_Y_START															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	WIN_Y_END	Y end for processing window
15:0	WIN_Y_START	Y start for processing window

14013418 DISP_COLOR_TIMING_DETECTION_0 Timing Detection 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	vtotal_cnt															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	htotal_cnt															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	vtotal_cnt	Information of input V total
15:0	htotal_cnt	Information of input H total

1401341C DISP_COLOR_TIMING_DETECTION_1 Timing Detection 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	vde_cnt															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hde_cnt															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	vde_cnt	Information of input V DE
15:0	hde_cnt	Information of input H DE

14013420 DISP_COLOR_DBG_CFG_MAIN Debug Mode Config 00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CR_INK_SHIFT		CB_INK_SHIFT		Y_INK_SHIFT		CR_INK_MODE			CB_INK_MODE			Y_INK_MODE		
Type		RW		RW		RW		RW			RW			RW		
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name					W1_INK_EN	CR_REPLACE	CB_REPLACE	Y_REPLACE				SPLIT_SWAP	SPLIT_EN	CAP_EN		INK_EN
Type					RW	RW	RW	RW				RW	RW	RW		RW
Reset					0	1	1	1				0	0	0		0

Bit(s)	Name	Description
30:29	CR_INK_SHIFT	**For Cr ink mode 4, 5, 6**
28:27	CB_INK_SHIFT	**For Cb ink mode 4, 5, 6**
26:25	Y_INK_SHIFT	**For Y ink mode 4, 5, 6**
24:22	CR_INK_MODE	**0: Single pixel ink mode** 1: Full screen ink mode 2: Ramp pattern 1 (00112233) 3: Ramp pattern 2 (02468) 4: Ramp pattern 3 (0X4,8X4) 5: Ramp pattern 4 (0X8,16X8) 6: Ramp pattern 5 (0X16, 32X16)
21:19	CB_INK_MODE	**0: Single pixel ink mode** 1: Full screen ink mode 2: Ramp pattern 1 (00112233) 3: Ramp pattern 2 (02468) 4: Ramp pattern 3 (0X4,8X4) 5: Ramp pattern 4 (0X8,16X8) 6: Ramp pattern 5 (0X16, 32X16)
18:16	Y_INK_MODE	**0: Single pixel ink mode** 1: Full screen ink mode 2: Ramp pattern 1 (00112233) 3: Ramp pattern 2 (02468) 4: Ramp pattern 3 (0X4,8X4) 5: Ramp pattern 4 (0X8,16X8) 6: Ramp pattern 5 (0X16, 32X16)
11	W1_INK_EN	**Enables ink for 2D counter 1**
10	CR_REPLACE	**0: Cr data not replaced in ink mode** 1: Cr data replaced
9	CB_REPLACE	**0: Cb data not replaced in ink mode** 1: Cb data replaced
8	Y_REPLACE	**0: Y data not replaced in ink mode** 1: Y data replaced
4	SPLIT_SWAP	**Enables window split or not** 0: Does not swap 1: Swap enable window
3	SPLIT_EN	**Enables split window for demo mode or not** 0: Process full window 1: Enable window split; range is defined in [26:16].
2	CAP_EN	**Enables data capture enable** The capture coordinate is defined in POS_X, POS_Y. 0: Disable 1: Enable
0	INK_EN	**Enables ink mode or not** 0: Disable 1: Enable

14013428 DISP_COLOR_C_BOOST_MAIN **Chroma Boost** **FF402080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NEW_CBOOST_LMT_U								NEW_CBOOST_LMT_L							
Type	RW								RW							

Reset	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			NEW_CBOOST_EN						CBOOST_GAIN							
Type			RW						RW							
Reset			1						1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	NEW_CBOOST_LMT_U	**Chroma boost gain upper bound**
23:16	NEW_CBOOST_LMT_L	**Chroma boost gain lower bound**
13	NEW_CBOOST_EN	**0: Disable new chroma boost** 1: Enable new chroma boost
7:0	CBOOST_GAIN	**128 denotes 1.0**

1401342C DISP_COLOR_C_BOOST_MAIN_2 **Chroma Boost 2** **80000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CBOO ST_Y CONS T														CBOOST_YOFFSET_SEL	
Type	RW														RW	
Reset	1	0	0	0	0	0	0	0							0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CBOOST_YOFFSET							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	CBOOST_YCONST	Y constant value of chroma boost
17:16	CBOOST_YOFFSET_SEL	Limit function of CBOOST_YOFFSET
7:0	CBOOST_YOFFSET	Y offset value of chroma boost

14013430 DISP_COLOR_LUMA_ADJ **Input Y Level Adjust** **0000FF40**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Y_SLOPE_LMT									Y_LEV_ADJ						
Type	RW									RW						
Reset	1	1	1	1	1	1	1	1		1	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	Y_SLOPE_LMT	**Limitation value of delta related to y slope, +- Y_SLOPE_LMT**
6:0	Y_LEV_ADJ	**Adjusts Y level before global contrast** 0x40: No adjustment

Bit(s)	Name	Description
		0x3F: Minus 1 before global contrast and brightness (will be added back after global contrast and brightness) 0x41: Plus 1 before global contrast and brightness (will be subtracted after global contrast and brightness)

14013434 DISP_COLOR_G_PIC_ADJ_MAIN_1 **Global Picture Adjustment** **04000080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						BRIGHTNESS										
Type						RW										
Reset						1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							CONTRAST									
Type							RW									
Reset							0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:16	BRIGHTNESS	**Adjusts global brightness value** Brightness = (value-1024)
9:0	CONTRAST	**Adjusts global contrast** 0: Multiply by 0.0 128: Multiply by 1.0 255: Multiply by 1.992

14013438 DISP_COLOR_G_PIC_ADJ_MAIN_2 **Global Picture Adjustment** **00000080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SATURATION									
Type							RW									
Reset							0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	SATURATION	**Adjusts global saturation** 0: Multiply by 0.0 128: Multiply by 1.0 255: Multiply by 1.992

14013484 DISP_COLOR_POS_MAIN **Position X** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	POS_Y															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	POS_X															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	POS_Y	Capture or ink Y coordinate
15:0	POS_X	Capture or ink X coordinate

14013488 DISP_COLOR_INK_DATA_MAIN — Ink Data Y — 020003FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							INK_DATA_CB									
Type							RW									
Reset							1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							INK_DATA_Y									
Type							RW									
Reset							1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
25:16	INK_DATA_CB	Cb value of ink data
9:0	INK_DATA_Y	Y value of ink data

1401348C DISP_COLOR_INK_DATA_MAIN_CR — Ink Data Cr — 00000200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							INK_DATA_CR									
Type							RW									
Reset							1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	INK_DATA_CR	Cr value of ink data

14013490 DISP_COLOR_CAP_IN_DATA_MAIN — Capture In Data Y — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name							CAP_IN_CB									
Type							RO									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							CAP_IN_Y									
Type							RO									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	CAP_IN_CB	Capture data of input Cb
9:0	CAP_IN_Y	Capture data of input Y

14013494 DISP_COLOR_CAP_IN_DATA_MAIN_CR Capture In Data Cr 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							CAP_IN_CR									
Type							RO									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	CAP_IN_CR	Capture data of input Cr

14013498 DISP_COLOR_CAP_OUT_DATA_MAIN Capture Out Data Y 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CAP_OUT_CB											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							CAP_OUT_Y									
Type							RO									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	CAP_OUT_CB	Capture data of output Cb
9:0	CAP_OUT_Y	Capture data of output Y

1401349C DISP_COLOR_CAP_OUT_DATA_MAIN_C Capture Out Data Cr 00000000

R

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CAP_OUT_CR												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	CAP_OUT_CR	Capture data of output Cr

140134A0 DISP_COLOR_Y_SLOPE_1_0_MAIN — Y Slope 1, 0 — 00800080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									Y_Slope_1							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									Y_Slope_0							
Type									RW							
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	Y_Slope_1	**Y slope 1** 255: 0.992 128: 0.0 0: -1.0
7:0	Y_Slope_0	**Y slope 0** 255: 0.992 128: 0.0 0: -1.0

140134A4 DISP_COLOR_Y_SLOPE_3_2_MAIN — Y Slope 3, 2 — 00800080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									Y_Slope_3							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									Y_Slope_2							
Type									RW							
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	Y_Slope_3	**Y slope 3**

Bit(s)	Name	Description
		255: 0.992 128: 0.0 0: -1.0
7:0	Y_Slope_2	**Y slope 2** 255: 0.992 128: 0.0 0: -1.0

140134A8 DISP_COLOR_Y_SLOPE_5_4_MAIN **Y Slope 5, 4** **00800080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									Y_Slope_5							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									Y_Slope_4							
Type									RW							
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	Y_Slope_5	**Y slope 5** 255: 0.992 128: 0.0 0: -1.0
7:0	Y_Slope_4	**Y slope 4** 255: 0.992 128: 0.0 0: -1.0

140134AC DISP_COLOR_Y_SLOPE_7_6_MAIN **Y Slope 7, 6** **00800080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									Y_Slope_7							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									Y_Slope_6							
Type									RW							
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	Y_Slope_7	**Y slope 7** 255: 0.992 128: 0.0 0: -1.0
7:0	Y_Slope_6	**Y slope 6** 255: 0.992 128: 0.0

Bit(s)	Name	Description
		0: -1.0

140134B0 DISP_COLOR_Y_SLOPE_98_MAIN **Y Slope 9, 8** **00800080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									Y_Slope_9							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									Y_Slope_8							
Type									RW							
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	Y_Slope_9	**Y slope 9** 255: 0.992 128: 0.0 0: -1.0
7:0	Y_Slope_8	**Y slope 8** 255: 0.992 128: 0.0 0: -1.0

140134B4 DISP_COLOR_Y_SLOPE_11_10_MAIN **Y Slope 11, 10** **00800080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									Y_Slope_11							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									Y_Slope_10							
Type									RW							
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	Y_Slope_11	**Y slope 11** 255: 0.992 128: 0.0 0: -1.0
7:0	Y_Slope_10	**Y slope 10** 255: 0.992 128: 0.0 0: -1.0

140134B8 DISP_COLOR_Y_SLOPE_1 **Y Slope 13, 12** **00800080**

3_12_MAIN

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									Y_Slope_13							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									Y_Slope_12							
Type									RW							
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	Y_Slope_13	**Y slope 13** 255: 0.992 128: 0.0 0: -1.0
7:0	Y_Slope_12	**Y slope 12** 255: 0.992 128: 0.0 0: -1.0

140134BC DISP_COLOR_Y_SLOPE_15_14_MAIN **Y Slope 15, 14** **00800080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									Y_Slope_15							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									Y_Slope_14							
Type									RW							
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	Y_Slope_15	**Y slope 15** 255: 0.992 128: 0.0 0: -1.0
7:0	Y_Slope_14	**Y slope 14** 255: 0.992 128: 0.0 0: -1.0

14013620 DISP_COLOR_LOCAL_HUE_CD_0 **Local Hue Cost Down 0** **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	hue_to_hue_3								hue_to_hue_2							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	hue_to_hue_1								hue_to_hue_0							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	hue_to_hue_3	0x01: -127 0x80: 0 0xFF: +127
23:16	hue_to_hue_2	0x01: -127 0x80: 0 0xFF: +127
15:8	hue_to_hue_1	0x01: -127 0x80: 0 0xFF: +127
7:0	hue_to_hue_0	0x01: -127 0x80: 0 0xFF: +127

14013624 DISP_COLOR_LOCAL_HUE_CD_1 Local Hue Cost Down 1 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	hue_to_hue_7								hue_to_hue_6							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hue_to_hue_5								hue_to_hue_4							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	hue_to_hue_7	0x01: -127 0x80: 0 0xFF: +127
23:16	hue_to_hue_6	0x01: -127 0x80: 0 0xFF: +127
15:8	hue_to_hue_5	0x01: -127 0x80: 0 0xFF: +127
7:0	hue_to_hue_4	0x01: -127 0x80: 0 0xFF: +127

14013628 DISP_COLOR_LOCAL_HUE_CD_2 Local Hue Cost Down 2 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	hue_to_hue_11								hue_to_hue_10							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hue_to_hue_9								hue_to_hue_8							

Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	hue_to_hue_11	0x01: -127 0x80: 0 0xFF: +127
23:16	hue_to_hue_10	0x01: -127 0x80: 0 0xFF: +127
15:8	hue_to_hue_9	0x01: -127 0x80: 0 0xFF: +127
7:0	hue_to_hue_8	0x01: -127 0x80: 0 0xFF: +127

1401362C DISP_COLOR_LOCAL_HUE_CD_3 Local Hue Cost Down 3 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	hue_to_hue_15								hue_to_hue_14							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hue_to_hue_13								hue_to_hue_12							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	hue_to_hue_15	0x01: -127 0x80: 0 0xFF: +127
23:16	hue_to_hue_14	0x01: -127 0x80: 0 0xFF: +127
15:8	hue_to_hue_13	0x01: -127 0x80: 0 0xFF: +127
7:0	hue_to_hue_12	0x01: -127 0x80: 0 0xFF: +127

14013630 DISP_COLOR_LOCAL_HUE_CD_4 Local Hue Cost Down 4 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	hue_to_hue_19								hue_to_hue_18							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hue_to_hue_17								hue_to_hue_16							
Type	RW								RW							

Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	hue_to_hue_19	0x01: -127 0x80: 0 0xFF: +127
23:16	hue_to_hue_18	0x01: -127 0x80: 0 0xFF: +127
15:8	hue_to_hue_17	0x01: -127 0x80: 0 0xFF: +127
7:0	hue_to_hue_16	0x01: -127 0x80: 0 0xFF: +127

14013740 DISP_COLOR_TWO_D_WINDOW_1 Two D Window 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	W1_SAT_UPPER								W1_SAT_LOWER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	W1_HUE_UPPER								W1_HUE_LOWER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	W1_SAT_UPPER	Saturation upper bound for accumulation
23:16	W1_SAT_LOWER	Saturation lower bound for accumulation
15:8	W1_HUE_UPPER	Hue upper bound for accumulation
7:0	W1_HUE_LOWER	Hue lower bound for accumulation

1401374C DISP_COLOR_TWO_D_W1_RESULT Two D Window 1 Result 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									W1_RESULT							
Type									RO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	W1_RESULT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	W1_RESULT	Result of window 1

14013768 DISP_COLOR_SAT_HIST_X_CFG_MAIN — Saturation Histogram Horizontal Range — FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SAT_WIN_X_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SAT_WIN_X_START															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SAT_WIN_X_END	**Saturation histogram window** X end position
15:0	SAT_WIN_X_START	**Saturation histogram window** X start position

1401376C DISP_COLOR_SAT_HIST_Y_CFG_MAIN — Saturation Histogram Vertical Range — FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SAT_WIN_Y_END															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SAT_WIN_Y_START															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SAT_WIN_Y_END	**Saturation histogram window** Y end position
15:0	SAT_WIN_Y_START	**Saturation histogram window** Y start position

1401379C DISP_COLOR_BWS_2 — Black White Stretch 2 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					PPMCM_ATPG_CT	PPMCM_ATPG_OB										
Type					RW	RW										
Reset					0	0										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
27	PPMCM_ATPG_CT	HW debug register
26	PPMCM_ATPG_OB	HW debug register

140137E0 DISP_COLOR_CRC_0 CRC_0 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													crc_src_sel			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crc_still_check_max								crc_non_still_cnt				crc_still_check_done	c_crc_still_check_trig	crc_l_en	crc_r_en
Type	RW								RO				RO	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit(s)	Name	Description
19:16	crc_src_sel	**Selects CRC source** 0: Color engine output 1: Channel delay output 2: c2p output 3: Hue output 4: Luma output 5: Sat output
15:8	crc_still_check_max	**Max. count of CRC still frame check**
7:4	crc_non_still_cnt	**Count status of CRC non still field/frame**
3	crc_still_check_done	**Ready status of CRC still frame check**
2	c_crc_still_check_trig	**Triggers CRC still frame check**
1	crc_l_en	**Enables CRC for left frame**
0	crc_r_en	**Enables CRC for right frame**

140137E4 DISP_COLOR_CRC_1 CRC_1 1FFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				crc_clip_h_end												
Type				RW												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				crc_clip_h_start												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	crc_clip_h_end	CRC calculation range: H end
12:0	crc_clip_h_start	CRC calculation range: H start

140137E8 DISP_COLOR_CRC_2 CRC_2 0FFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					crc_clip_v_end											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					crc_clip_v_start											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	crc_clip_v_end	CRC calculation range: V end
11:0	crc_clip_v_start	CRC calculation range: V start

140137EC DISP_COLOR_CRC_3 CRC_3 3FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			crc_y_mask										crc_c_mask			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crc_c_mask						crc_v_mask									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	crc_y_mask	Masks CRC for Y channel
19:10	crc_c_mask	Masks CRC for Cb channel
9:0	crc_v_mask	Masks CRC for Cr channel

140137F0 DISP_COLOR_CRC_4 CRC_4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	crc_result															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crc_result															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	crc_result	CRC result of one frame

140137FC DISP_COLOR_PARTIAL_S Partial Sat Gain 1 from Hue Phase 0 to 3 80808080

AT_GAIN1_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain1_hue_3								sat_gain1_hue_2							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain1_hue_1								sat_gain1_hue_0							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain1_hue_3	Partial Sat Gain1 in Hue Phase 3
23:16	sat_gain1_hue_2	Partial Sat Gain1 in Hue Phase 2
15:8	sat_gain1_hue_1	Partial Sat Gain1 in Hue Phase 1
7:0	sat_gain1_hue_0	Partial Sat Gain1 in Hue Phase 0

14013800 DISP_COLOR_PARTIAL_SAT_GAIN1_1 — **Partial Sat Gain 1 from Hue Phase 4 to 7** — **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain1_hue_7								sat_gain1_hue_6							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain1_hue_5								sat_gain1_hue_4							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain1_hue_7	Partial Sat Gain1 in Hue Phase 7
23:16	sat_gain1_hue_6	Partial Sat Gain1 in Hue Phase 6
15:8	sat_gain1_hue_5	Partial Sat Gain1 in Hue Phase 5
7:0	sat_gain1_hue_4	Partial Sat Gain1 in Hue Phase 4

14013804 DISP_COLOR_PARTIAL_SAT_GAIN1_2 — **Partial Sat Gain 1 from Hue Phase 8 to 11** — **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain1_hue_11								sat_gain1_hue_10							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain1_hue_9								sat_gain1_hue_8							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain1_hue_11	Partial Sat Gain1 in Hue Phase 11
23:16	sat_gain1_hue_10	Partial Sat Gain1 in Hue Phase 10
15:8	sat_gain1_hue_9	Partial Sat Gain1 in Hue Phase 9

Bit(s)	Name	Description
7:0	sat_gain1_hue_8	Partial Sat Gain1 in Hue Phase 8

14013808 DISP_COLOR_PARTIAL_SAT_GAIN1_3 **Partial Sat Gain 1 from Hue Phase 12 to 15** **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain1_hue_15								sat_gain1_hue_14							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain1_hue_13								sat_gain1_hue_12							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain1_hue_15	Partial Sat Gain1 in Hue Phase 15
23:16	sat_gain1_hue_14	Partial Sat Gain1 in Hue Phase 14
15:8	sat_gain1_hue_13	Partial Sat Gain1 in Hue Phase 13
7:0	sat_gain1_hue_12	Partial Sat Gain1 in Hue Phase 12

1401380C DISP_COLOR_PARTIAL_SAT_GAIN1_4 **Partial Sat Gain 1 from Hue Phase 16 to 19** **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain1_hue_19								sat_gain1_hue_18							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain1_hue_17								sat_gain1_hue_16							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain1_hue_19	Partial Sat Gain1 in Hue Phase 19
23:16	sat_gain1_hue_18	Partial Sat Gain1 in Hue Phase 18
15:8	sat_gain1_hue_17	Partial Sat Gain1 in Hue Phase 17
7:0	sat_gain1_hue_16	Partial Sat Gain1 in Hue Phase 16

14013810 DISP_COLOR_PARTIAL_SAT_GAIN2_0 **Partial Sat Gain 2 from Hue Phase 0 to 3** **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain2_hue_3								sat_gain2_hue_2							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain2_hue_1								sat_gain2_hue_0							
Type	RW								RW							

Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain2_hue_3	Partial Sat Gain2 in Hue Phase 3
23:16	sat_gain2_hue_2	Partial Sat Gain2 in Hue Phase 2
15:8	sat_gain2_hue_1	Partial Sat Gain2 in Hue Phase 1
7:0	sat_gain2_hue_0	Partial Sat Gain2 in Hue Phase 0

14013814 DISP_COLOR_PARTIAL_SAT_GAIN2_1 — Partial Sat Gain 2 from Hue Phase 4 to 7 — 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain2_hue_7								sat_gain2_hue_6							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain2_hue_5								sat_gain2_hue_4							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain2_hue_7	Partial Sat Gain2 in Hue Phase 7
23:16	sat_gain2_hue_6	Partial Sat Gain2 in Hue Phase 6
15:8	sat_gain2_hue_5	Partial Sat Gain2 in Hue Phase 5
7:0	sat_gain2_hue_4	Partial Sat Gain2 in Hue Phase 4

14013818 DISP_COLOR_PARTIAL_SAT_GAIN2_2 — Partial Sat Gain 2 from Hue Phase 8 to 11 — 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain2_hue_11								sat_gain2_hue_10							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain2_hue_9								sat_gain2_hue_8							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain2_hue_11	Partial Sat Gain2 in Hue Phase 11
23:16	sat_gain2_hue_10	Partial Sat Gain2 in Hue Phase 10
15:8	sat_gain2_hue_9	Partial Sat Gain2 in Hue Phase 9
7:0	sat_gain2_hue_8	Partial Sat Gain2 in Hue Phase 8

1401381C DISP_COLOR_PARTIAL_SAT_GAIN2_3 — Partial Sat Gain 2 from Hue Phase 12 to 15 — 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	sat_gain2_hue_15								sat_gain2_hue_14							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain2_hue_13								sat_gain2_hue_12							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain2_hue_15	Partial Sat Gain2 in Hue Phase 15
23:16	sat_gain2_hue_14	Partial Sat Gain2 in Hue Phase 14
15:8	sat_gain2_hue_13	Partial Sat Gain2 in Hue Phase 13
7:0	sat_gain2_hue_12	Partial Sat Gain2 in Hue Phase 12

14013820 DISP_COLOR_PARTIAL_SAT_GAIN2_4 — **Partial Sat Gain 2 from Hue Phase 16 to 19** — **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain2_hue_19								sat_gain2_hue_18							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain2_hue_17								sat_gain2_hue_16							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain2_hue_19	Partial Sat Gain2 in Hue Phase 19
23:16	sat_gain2_hue_18	Partial Sat Gain2 in Hue Phase 18
15:8	sat_gain2_hue_17	Partial Sat Gain2 in Hue Phase 17
7:0	sat_gain2_hue_16	Partial Sat Gain2 in Hue Phase 16

14013824 DISP_COLOR_PARTIAL_SAT_GAIN3_0 — **Partial Sat Gain 3 from Hue Phase 0 to 3** — **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain3_hue_3								sat_gain3_hue_2							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain3_hue_1								sat_gain3_hue_0							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain3_hue_3	Partial Sat Gain3 in Hue Phase 3
23:16	sat_gain3_hue_2	Partial Sat Gain3 in Hue Phase 2
15:8	sat_gain3_hue_1	Partial Sat Gain3 in Hue Phase 1
7:0	sat_gain3_hue_0	Partial Sat Gain3 in Hue Phase 0

14013828 DISP_COLOR_PARTIAL_SAT_GAIN3_1 — **Partial Sat Gain 3 from Hue Phase 4 to 7** — **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain3_hue_7								sat_gain3_hue_6							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain3_hue_5								sat_gain3_hue_4							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain3_hue_7	Partial Sat Gain3 in Hue Phase 7
23:16	sat_gain3_hue_6	Partial Sat Gain3 in Hue Phase 6
15:8	sat_gain3_hue_5	Partial Sat Gain3 in Hue Phase 5
7:0	sat_gain3_hue_4	Partial Sat Gain3 in Hue Phase 4

1401382C DISP_COLOR_PARTIAL_SAT_GAIN3_2 — **Partial Sat Gain 3 from Hue Phase 8 to 11** — **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain3_hue_11								sat_gain3_hue_10							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain3_hue_9								sat_gain3_hue_8							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain3_hue_11	Partial Sat Gain3 in Hue Phase 11
23:16	sat_gain3_hue_10	Partial Sat Gain3 in Hue Phase 10
15:8	sat_gain3_hue_9	Partial Sat Gain3 in Hue Phase 9
7:0	sat_gain3_hue_8	Partial Sat Gain3 in Hue Phase 8

14013830 DISP_COLOR_PARTIAL_SAT_GAIN3_3 — **Partial Sat Gain 3 from Hue Phase 12 to 15** — **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain3_hue_15								sat_gain3_hue_14							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain3_hue_13								sat_gain3_hue_12							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain3_hue_15	Partial Sat Gain3 in Hue Phase 15
23:16	sat_gain3_hue_14	Partial Sat Gain3 in Hue Phase 14
15:8	sat_gain3_hue_13	Partial Sat Gain3 in Hue Phase 13
7:0	sat_gain3_hue_12	Partial Sat Gain3 in Hue Phase 12

14013834 DISP_COLOR_PARTIAL_SAT_GAIN3_4 **Partial Sat Gain 3 from Hue Phase 16 to 19** **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_gain3_hue_19								sat_gain3_hue_18							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_gain3_hue_17								sat_gain3_hue_16							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	sat_gain3_hue_19	Partial Sat Gain3 in Hue Phase 19
23:16	sat_gain3_hue_18	Partial Sat Gain3 in Hue Phase 18
15:8	sat_gain3_hue_17	Partial Sat Gain3 in Hue Phase 17
7:0	sat_gain3_hue_16	Partial Sat Gain3 in Hue Phase 16

14013838 DISP_COLOR_PARTIAL_SAT_POINT1 **Partial Sat Point 1 from Hue Phase 0 to 3** **1E1E1E1E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_point1_hue_3								sat_point1_hue_2							
Type	RW								RW							
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_point1_hue_1								sat_point1_hue_0							
Type	RW								RW							
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0

Bit(s)	Name	Description
31:24	sat_point1_hue_3	Partial Sat Point1 in Hue Phase 3
23:16	sat_point1_hue_2	Partial Sat Point1 in Hue Phase 2
15:8	sat_point1_hue_1	Partial Sat Point1 in Hue Phase 1
7:0	sat_point1_hue_0	Partial Sat Point1 in Hue Phase 0

1401383C DISP_COLOR_PARTIAL_SAT_POINT1_1 **Partial Sat Point 1 from Hue Phase 4 to 7** **1E1E1E1E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_point1_hue_7								sat_point1_hue_6							
Type	RW								RW							

Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_point1_hue_5								sat_point1_hue_4							
Type	RW								RW							
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0

Bit(s)	Name	Description
31:24	sat_point1_hue_7	Partial Sat Point1 in Hue Phase 7
23:16	sat_point1_hue_6	Partial Sat Point1 in Hue Phase 6
15:8	sat_point1_hue_5	Partial Sat Point1 in Hue Phase 5
7:0	sat_point1_hue_4	Partial Sat Point1 in Hue Phase 4

14013840 DISP_COLOR_PARTIAL_SAT_POINT12 — **Partial Sat Point 1 from Hue Phase 8 to 11** — **1E1E1E1E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_point1_hue_11								sat_point1_hue_10							
Type	RW								RW							
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_point1_hue_9								sat_point1_hue_8							
Type	RW								RW							
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0

Bit(s)	Name	Description
31:24	sat_point1_hue_11	Partial Sat Point1 in Hue Phase 11
23:16	sat_point1_hue_10	Partial Sat Point1 in Hue Phase 10
15:8	sat_point1_hue_9	Partial Sat Point1 in Hue Phase 9
7:0	sat_point1_hue_8	Partial Sat Point1 in Hue Phase 8

14013844 DISP_COLOR_PARTIAL_SAT_POINT13 — **Partial Sat Point 1 from Hue Phase 12 to 15** — **1E1E1E1E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_point1_hue_15								sat_point1_hue_14							
Type	RW								RW							
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_point1_hue_13								sat_point1_hue_12							
Type	RW								RW							
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0

Bit(s)	Name	Description
31:24	sat_point1_hue_15	Partial Sat Point1 in Hue Phase 15
23:16	sat_point1_hue_14	Partial Sat Point1 in Hue Phase 14
15:8	sat_point1_hue_13	Partial Sat Point1 in Hue Phase 13
7:0	sat_point1_hue_12	Partial Sat Point1 in Hue Phase 12

14013848 DISP_COLOR_PARTIAL_SAT_POINT14 **Partial Sat Point 1 from Hue Phase 16 to 19** **1E1E1E1E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_point1_hue_19								sat_point1_hue_18							
Type	RW								RW							
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_point1_hue_17								sat_point1_hue_16							
Type	RW								RW							
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0

Bit(s)	Name	Description
31:24	sat_point1_hue_19	Partial Sat Point1 in Hue Phase 19
23:16	sat_point1_hue_18	Partial Sat Point1 in Hue Phase 18
15:8	sat_point1_hue_17	Partial Sat Point1 in Hue Phase 17
7:0	sat_point1_hue_16	Partial Sat Point1 in Hue Phase 16

1401384C DISP_COLOR_PARTIAL_SAT_POINT2 **Partial Sat Point 2 from Hue Phase 0 to 3** **3C3C3C3C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_point2_hue_3								sat_point2_hue_2							
Type	RW								RW							
Reset	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_point2_hue_1								sat_point2_hue_0							
Type	RW								RW							
Reset	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0

Bit(s)	Name	Description
31:24	sat_point2_hue_3	Partial Sat Point2 in Hue Phase 3
23:16	sat_point2_hue_2	Partial Sat Point2 in Hue Phase 2
15:8	sat_point2_hue_1	Partial Sat Point2 in Hue Phase 1
7:0	sat_point2_hue_0	Partial Sat Point2 in Hue Phase 0

14013850 DISP_COLOR_PARTIAL_SAT_POINT21 **Partial Sat Point 2 from Hue Phase 4 to 7** **3C3C3C3C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_point2_hue_7								sat_point2_hue_6							
Type	RW								RW							
Reset	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_point2_hue_5								sat_point2_hue_4							
Type	RW								RW							
Reset	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0

Bit(s)	Name	Description
31:24	sat_point2_hue_7	Partial Sat Point2 in Hue Phase 7
23:16	sat_point2_hue_6	Partial Sat Point2 in Hue Phase 6
15:8	sat_point2_hue_5	Partial Sat Point2 in Hue Phase 5
7:0	sat_point2_hue_4	Partial Sat Point2 in Hue Phase 4

14013854 DISP_COLOR_PARTIAL_SAT_POINT2_2 — **Partial Sat Point 2 from Hue Phase 8 to 11** — **3C3C3C3C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_point2_hue_11								sat_point2_hue_10							
Type	RW								RW							
Reset	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_point2_hue_9								sat_point2_hue_8							
Type	RW								RW							
Reset	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0

Bit(s)	Name	Description
31:24	sat_point2_hue_11	Partial Sat Point2 in Hue Phase 11
23:16	sat_point2_hue_10	Partial Sat Point2 in Hue Phase 10
15:8	sat_point2_hue_9	Partial Sat Point2 in Hue Phase 9
7:0	sat_point2_hue_8	Partial Sat Point2 in Hue Phase 8

14013858 DISP_COLOR_PARTIAL_SAT_POINT2_3 — **Partial Sat Point 2 from Hue Phase 12 to 15** — **3C3C3C3C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_point2_hue_15								sat_point2_hue_14							
Type	RW								RW							
Reset	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_point2_hue_13								sat_point2_hue_12							
Type	RW								RW							
Reset	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0

Bit(s)	Name	Description
31:24	sat_point2_hue_15	Partial Sat Point2 in Hue Phase 15
23:16	sat_point2_hue_14	Partial Sat Point2 in Hue Phase 14
15:8	sat_point2_hue_13	Partial Sat Point2 in Hue Phase 13
7:0	sat_point2_hue_12	Partial Sat Point2 in Hue Phase 12

1401385C DISP_COLOR_PARTIAL_SAT_POINT2_4 — **Partial Sat Point 2 from Hue Phase 16 to 19** — **3C3C3C3C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sat_point2_hue_19								sat_point2_hue_18							
Type	RW								RW							
Reset	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sat_point2_hue_17								sat_point2_hue_16							
Type	RW								RW							
Reset	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0

Bit(s)	Name	Description
31:24	sat_point2_hue_19	Partial Sat Point2 in Hue Phase 19
23:16	sat_point2_hue_18	Partial Sat Point2 in Hue Phase 18
15:8	sat_point2_hue_17	Partial Sat Point2 in Hue Phase 17
7:0	sat_point2_hue_16	Partial Sat Point2 in Hue Phase 16

14013C00 DISP_COLOR_START Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									disp_color_dbg_sel							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								disp_color_sw_rst_engine			stop_to_wdma	direct_yuv_bit_sel	disp_color_dbuf_vsync	disp_color_wrap_mode	disp_color_out_sel	disp_color_start
Type								RW			RW	RW	RW	RW	RW	RW
Reset								0			0	0	0	0	0	0

Bit(s)	Name	Description
23:16	disp_color_dbg_sel	Selects debug
8	disp_color_sw_rst_engine	Reset engine
5	stop_to_wdma	0: Normal path 1: Signal stop to WDMA
4	direct_yuv_bit_sel	0: MDP 10-bit YUV 1: DISP 8-bit YUV
3	disp_color_dbuf_vsync	Color engine shadow at vsync
2	disp_color_wrap_mode	Wrapper_mode
1	disp_color_out_sel	Selects output
0	disp_color_start	Start disp_color engine

14013C04 DISP_COLOR_INTEN Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														disp_color_i	disp_color_i	disp_color_i

														nten_fr_underrun	nten_fr_done	nten_fr_complete
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	disp_color_inten_fr_underrun	**Enables interrupt** frame_underrun
1	disp_color_inten_fr_done	**Enables interrupt** frame_done
0	disp_color_inten_fr_complete	**Enables interrupt** frame_complete

14013C08 DISP_COLOR_INTSTA **Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														disp_color_intsta_fr_underrun	disp_color_intsta_fr_done	disp_color_intsta_fr_complete
Type														RO	RO	RO
Reset														0	0	0

Bit(s)	Name	Description
2	disp_color_intsta_fr_underrun	**Interrupt status** Frame underrun
1	disp_color_intsta_fr_done	**Interrupt status** Frame done
0	disp_color_intsta_fr_complete	**Interrupt status** Frame completed

14013C0C DISP_COLOR_OUT_SEL **Output Bits Configuration** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						reg_chc_uv	reg_chc_round	reg_chc_sel		reg_chb_uv	reg_chb_round	reg_chb_sel		reg_cha_uv	reg_cha_round	reg_cha_sel
Type						RW	RW	RW		RW	RW	RW		RW	RW	RW
Reset						0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
10	reg_chc_uv	channel_c uv output
9	reg_chc_round	Rounds channel_c to 8 bits
8	reg_chc_sel	Selects channel_c 8-bit/10-bit
6	reg_chb_uv	channel_b uv output
5	reg_chb_round	Rounds channel_b to 8 bits
4	reg_chb_sel	Selects channel_b 8-bit/10-bit
2	reg_cha_uv	channel_a uv output
1	reg_cha_round	Rounds channel_a to 8 bits
0	reg_cha_sel	Selects channel_a 8-bit/10-bit

14013C10 DISP_COLOR_FRAME_DONE_DEL Frame Done Delay Select 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									disp_color_frame_done_del							
Type									RW							
Reset									0	0	0	1	0	0	0	0

Bit(s)	Name	Description
7:0	disp_color_frame_done_del	Selects frame done delay

14013C14 DISP_COLOR_CRC CRC Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														disp_color_crc_clr	disp_color_crc_start	disp_color_crc_cen
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	disp_color_crc_clr	Clears CRC
1	disp_color_crc_start	Starts CRC
0	disp_color_crc_cen	Enables CRC

14013C18 DISP_COLOR_SW_SCRATC Software Scratch 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	disp_color_sw_scratch															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	disp_color_sw_scratch															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	disp_color_sw_scratch	disp_color_sw_scratch

14013C28 DISP_COLOR_CK_ON — Clock Force on — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																disp_color_ck_on
Type																RW
Reset																0

Bit(s)	Name	Description
0	disp_color_ck_on	Forces clock on

14013C50 DISP_COLOR_INTERNAL_IP_WIDTH — Wrapper Internal IP Width — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			disp_color_internal_ip_width													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	disp_color_internal_ip_width	Wrapper internal IP width

14013C54 DISP_COLOR — Wrapper Internal IP Height — 00000000

_INTERNAL_IP_HEIGHT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			disp_color_internal_ip_height													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	disp_color_internal_ip_height	Wrapper internal IP height

14013C60 DISP_COLOR_CM1_EN **Front Color Transform Enable** **00000003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															disp_color_cm1_clip_en	disp_color_cm1_en
Type															RW	RW
Reset															1	1

Bit(s)	Name	Description
1	disp_color_cm1_clip_en	Front color transform enable of clipping for input RGB
0	disp_color_cm1_en	Enables front color transform

14013CA0 DISP_COLOR_CM2_EN **Back Color Transform Enable** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												disp_color_cm2_round_off		disp_color_cm2_clip_sel		disp_color_cm2_en
Type												RW		RW		RW
Reset												0		0	0	1

Bit(s)	Name	Description
4	disp_color_cm2_round_off	
2:1	disp_color_cm2_clip_sel	
0	disp_color_cm2_en	Enables back color transform

14013CF0 DISP_COLOR_R0_CRC — Wrapper R0 CRC — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															disp_color_engine_end	disp_color_crc_rdy_0
Type															RO	RO
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	disp_color_crc_out_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	disp_color_engine_end	Engine end
16	disp_color_crc_rdy_0	Wrapper R0 CRC RDY
15:0	disp_color_crc_out_0	Wrapper R0 CRC DATA

14013CF4 DISP_COLOR_S_GAIN_BY_Y0_0 — S Gain by Y0 from Hue Phase 0 to 3 — 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y0_hue_3								s_gain_y0_hue_2							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y0_hue_1								s_gain_y0_hue_0							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y0_hue_3	S Gain by Y0 in Hue Phase 3
23:16	s_gain_y0_hue_2	S Gain by Y0 in Hue Phase 2
15:8	s_gain_y0_hue_1	S Gain by Y0 in Hue Phase 1
7:0	s_gain_y0_hue_0	S Gain by Y0 in Hue Phase 0

14013CF8 DISP_COLOR_S_GAIN_BY_Y0_1 — S Gain by Y0 from Hue Phase 4 to 7 — 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y0_hue_7								s_gain_y0_hue_6							
Type	RW								RW							

Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_yo_hue_5								s_gain_yo_hue_4							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_yo_hue_7	S Gain by Yo in Hue Phase 7
23:16	s_gain_yo_hue_6	S Gain by Yo in Hue Phase 6
15:8	s_gain_yo_hue_5	S Gain by Yo in Hue Phase 5
7:0	s_gain_yo_hue_4	S Gain by Yo in Hue Phase 4

14013CFC DISP_COLOR_S_GAIN_BY_YO_2 — **S Gain by Yo from Hue Phase 8 to 11** — **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_yo_hue_11								s_gain_yo_hue_10							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_yo_hue_9								s_gain_yo_hue_8							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_yo_hue_11	S Gain by Yo in Hue Phase 11
23:16	s_gain_yo_hue_10	S Gain by Yo in Hue Phase 10
15:8	s_gain_yo_hue_9	S Gain by Yo in Hue Phase 9
7:0	s_gain_yo_hue_8	S Gain by Yo in Hue Phase 8

14013D00 DISP_COLOR_S_GAIN_BY_YO_3 — **S Gain by Yo from Hue Phase 12 to 15** — **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_yo_hue_15								s_gain_yo_hue_14							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_yo_hue_13								s_gain_yo_hue_12							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_yo_hue_15	S Gain by Yo in Hue Phase 15
23:16	s_gain_yo_hue_14	S Gain by Yo in Hue Phase 14
15:8	s_gain_yo_hue_13	S Gain by Yo in Hue Phase 13
7:0	s_gain_yo_hue_12	S Gain by Yo in Hue Phase 12

14013D04 DISP_COLOR — **S Gain by Yo from Hue Phase 16** — **80808080**

S_GAIN_BY_Y0_4 to 19

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y0_hue_19								s_gain_y0_hue_18							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y0_hue_17								s_gain_y0_hue_16							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y0_hue_19	S Gain by Y0 in Hue Phase 19
23:16	s_gain_y0_hue_18	S Gain by Y0 in Hue Phase 18
15:8	s_gain_y0_hue_17	S Gain by Y0 in Hue Phase 17
7:0	s_gain_y0_hue_16	S Gain by Y0 in Hue Phase 16

14013D08 DISP_COLOR_S_GAIN_BY_Y64_0 S Gain by Y64 from Hue Phase 0 to 3 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y64_hue_3								s_gain_y64_hue_2							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y64_hue_1								s_gain_y64_hue_0							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y64_hue_3	S Gain by Y64 in Hue Phase 3
23:16	s_gain_y64_hue_2	S Gain by Y64 in Hue Phase 2
15:8	s_gain_y64_hue_1	S Gain by Y64 in Hue Phase 1
7:0	s_gain_y64_hue_0	S Gain by Y64 in Hue Phase 0

14013D0C DISP_COLOR_S_GAIN_BY_Y64_1 S Gain by Y64 from Hue Phase 4 to 7 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y64_hue_7								s_gain_y64_hue_6							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y64_hue_5								s_gain_y64_hue_4							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y64_hue_7	S Gain by Y64 in Hue Phase 7
23:16	s_gain_y64_hue_6	S Gain by Y64 in Hue Phase 6

Bit(s)	Name	Description
15:8	s_gain_y64_hue_5	S Gain by Y64 in Hue Phase 5
7:0	s_gain_y64_hue_4	S Gain by Y64 in Hue Phase 4

14013D10 DISP_COLOR_S_GAIN_BY_Y64_2 — S Gain by Y64 from Hue Phase 8 to 11 — 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y64_hue_11								s_gain_y64_hue_10							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y64_hue_9								s_gain_y64_hue_8							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y64_hue_11	S Gain by Y64 in Hue Phase 11
23:16	s_gain_y64_hue_10	S Gain by Y64 in Hue Phase 10
15:8	s_gain_y64_hue_9	S Gain by Y64 in Hue Phase 9
7:0	s_gain_y64_hue_8	S Gain by Y64 in Hue Phase 8

14013D14 DISP_COLOR_S_GAIN_BY_Y64_3 — S Gain by Y64 from Hue Phase 12 to 15 — 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y64_hue_15								s_gain_y64_hue_14							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y64_hue_13								s_gain_y64_hue_12							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y64_hue_15	S Gain by Y64 in Hue Phase 15
23:16	s_gain_y64_hue_14	S Gain by Y64 in Hue Phase 14
15:8	s_gain_y64_hue_13	S Gain by Y64 in Hue Phase 13
7:0	s_gain_y64_hue_12	S Gain by Y64 in Hue Phase 12

14013D18 DISP_COLOR_S_GAIN_BY_Y64_4 — S Gain by Y64 from Hue Phase 16 to 19 — 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y64_hue_19								s_gain_y64_hue_18							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y64_hue_17								s_gain_y64_hue_16							

Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y64_hue_19	S Gain by Y64 in Hue Phase 19
23:16	s_gain_y64_hue_18	S Gain by Y64 in Hue Phase 18
15:8	s_gain_y64_hue_17	S Gain by Y64 in Hue Phase 17
7:0	s_gain_y64_hue_16	S Gain by Y64 in Hue Phase 16

14013D1C DISP_COLOR_S_GAIN_BY_Y128_0 — S Gain by Y128 from Hue Phase 0 to 3 — 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y128_hue_3								s_gain_y128_hue_2							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y128_hue_1								s_gain_y128_hue_0							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y128_hue_3	S Gain by Y128 in Hue Phase 3
23:16	s_gain_y128_hue_2	S Gain by Y128 in Hue Phase 2
15:8	s_gain_y128_hue_1	S Gain by Y128 in Hue Phase 1
7:0	s_gain_y128_hue_0	S Gain by Y128 in Hue Phase 0

14013D20 DISP_COLOR_S_GAIN_BY_Y128_1 — S Gain by Y128 from Hue Phase 4 to 7 — 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y128_hue_7								s_gain_y128_hue_6							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y128_hue_5								s_gain_y128_hue_4							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y128_hue_7	S Gain by Y128 in Hue Phase 7
23:16	s_gain_y128_hue_6	S Gain by Y128 in Hue Phase 6
15:8	s_gain_y128_hue_5	S Gain by Y128 in Hue Phase 5
7:0	s_gain_y128_hue_4	S Gain by Y128 in Hue Phase 4

14013D24 DISP_COLOR_S_GAIN_BY_Y128_2 — S Gain by Y128 from Hue Phase 8 to 11 — 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y128_hue_11								s_gain_y128_hue_10							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y128_hue_9								s_gain_y128_hue_8							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y128_hue_11	S Gain by Y128 in Hue Phase 11
23:16	s_gain_y128_hue_10	S Gain by Y128 in Hue Phase 10
15:8	s_gain_y128_hue_9	S Gain by Y128 in Hue Phase 9
7:0	s_gain_y128_hue_8	S Gain by Y128 in Hue Phase 8

14013D28 DISP_COLOR_S_GAIN_BY_Y128_3 — S Gain by Y128 from Hue Phase 12 to 15 — 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y128_hue_15								s_gain_y128_hue_14							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y128_hue_13								s_gain_y128_hue_12							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y128_hue_15	S Gain by Y128 in Hue Phase 15
23:16	s_gain_y128_hue_14	S Gain by Y128 in Hue Phase 14
15:8	s_gain_y128_hue_13	S Gain by Y128 in Hue Phase 13
7:0	s_gain_y128_hue_12	S Gain by Y128 in Hue Phase 12

14013D2C DISP_COLOR_S_GAIN_BY_Y128_4 — S Gain by Y128 from Hue Phase 16 to 19 — 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y128_hue_19								s_gain_y128_hue_18							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y128_hue_17								s_gain_y128_hue_16							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y128_hue_19	S Gain by Y128 in Hue Phase 19
23:16	s_gain_y128_hue_18	S Gain by Y128 in Hue Phase 18
15:8	s_gain_y128_hue_17	S Gain by Y128 in Hue Phase 17
7:0	s_gain_y128_hue_16	S Gain by Y128 in Hue Phase 16

Bit(s)	Name	Description

14013D30 DISP_COLOR_S_GAIN_BY_Y192_0 — **S Gain by Y192 from Hue Phase 0 to 3** — **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y192_hue_3								s_gain_y192_hue_2							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y192_hue_1								s_gain_y192_hue_0							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y192_hue_3	S Gain by Y192 in Hue Phase 3
23:16	s_gain_y192_hue_2	S Gain by Y192 in Hue Phase 2
15:8	s_gain_y192_hue_1	S Gain by Y192 in Hue Phase 1
7:0	s_gain_y192_hue_0	S Gain by Y192 in Hue Phase 0

14013D34 DISP_COLOR_S_GAIN_BY_Y192_1 — **S Gain by Y192 from Hue Phase 4 to 7** — **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y192_hue_7								s_gain_y192_hue_6							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y192_hue_5								s_gain_y192_hue_4							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y192_hue_7	S Gain by Y192 in Hue Phase 7
23:16	s_gain_y192_hue_6	S Gain by Y192 in Hue Phase 6
15:8	s_gain_y192_hue_5	S Gain by Y192 in Hue Phase 5
7:0	s_gain_y192_hue_4	S Gain by Y192 in Hue Phase 4

14013D38 DISP_COLOR_S_GAIN_BY_Y192_2 — **S Gain by Y192 from Hue Phase 8 to 11** — **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y192_hue_11								s_gain_y192_hue_10							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y192_hue_9								s_gain_y192_hue_8							
Type	RW								RW							

Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y192_hue_11	S Gain by Y192 in Hue Phase 11
23:16	s_gain_y192_hue_10	S Gain by Y192 in Hue Phase 10
15:8	s_gain_y192_hue_9	S Gain by Y192 in Hue Phase 9
7:0	s_gain_y192_hue_8	S Gain by Y192 in Hue Phase 8

14013D3C DISP_COLOR_S_GAIN_BY_Y192_3 — S Gain by Y192 from Hue Phase 12 to 15 — 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y192_hue_15								s_gain_y192_hue_14							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y192_hue_13								s_gain_y192_hue_12							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y192_hue_15	S Gain by Y192 in Hue Phase 15
23:16	s_gain_y192_hue_14	S Gain by Y192 in Hue Phase 14
15:8	s_gain_y192_hue_13	S Gain by Y192 in Hue Phase 13
7:0	s_gain_y192_hue_12	S Gain by Y192 in Hue Phase 12

14013D40 DISP_COLOR_S_GAIN_BY_Y192_4 — S Gain by Y192 from Hue Phase 16 to 19 — 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y192_hue_19								s_gain_y192_hue_18							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y192_hue_17								s_gain_y192_hue_16							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y192_hue_19	S Gain by Y192 in Hue Phase 19
23:16	s_gain_y192_hue_18	S Gain by Y192 in Hue Phase 18
15:8	s_gain_y192_hue_17	S Gain by Y192 in Hue Phase 17
7:0	s_gain_y192_hue_16	S Gain by Y192 in Hue Phase 16

14013D44 DISP_COLOR_S_GAIN_BY_Y256_0 — S Gain by Y256 from Hue Phase 0 to 3 — 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	s_gain_y256_hue_3								s_gain_y256_hue_2							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y256_hue_1								s_gain_y256_hue_0							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y256_hue_3	S Gain by Y256 in Hue Phase 3
23:16	s_gain_y256_hue_2	S Gain by Y256 in Hue Phase 2
15:8	s_gain_y256_hue_1	S Gain by Y256 in Hue Phase 1
7:0	s_gain_y256_hue_0	S Gain by Y256 in Hue Phase 0

14013D48 DISP_COLOR_S_GAIN_BY_Y256_1

S Gain by Y256 from Hue Phase 4 to 7 **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y256_hue_7								s_gain_y256_hue_6							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y256_hue_5								s_gain_y256_hue_4							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y256_hue_7	S Gain by Y256 in Hue Phase 7
23:16	s_gain_y256_hue_6	S Gain by Y256 in Hue Phase 6
15:8	s_gain_y256_hue_5	S Gain by Y256 in Hue Phase 5
7:0	s_gain_y256_hue_4	S Gain by Y256 in Hue Phase 4

14013D4C DISP_COLOR_S_GAIN_BY_Y256_2

S Gain by Y256 from Hue Phase 8 to 11 **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y256_hue_11								s_gain_y256_hue_10							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y256_hue_9								s_gain_y256_hue_8							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y256_hue_11	S Gain by Y256 in Hue Phase 11
23:16	s_gain_y256_hue_10	S Gain by Y256 in Hue Phase 10
15:8	s_gain_y256_hue_9	S Gain by Y256 in Hue Phase 9
7:0	s_gain_y256_hue_8	S Gain by Y256 in Hue Phase 8

14013D50 DISP_COLOR_S_GAIN_BY_Y256_3 — **S Gain by Y256 from Hue Phase 12 to 15** — **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y256_hue_15								s_gain_y256_hue_14							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y256_hue_13								s_gain_y256_hue_12							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y256_hue_15	S Gain by Y256 in Hue Phase 15
23:16	s_gain_y256_hue_14	S Gain by Y256 in Hue Phase 14
15:8	s_gain_y256_hue_13	S Gain by Y256 in Hue Phase 13
7:0	s_gain_y256_hue_12	S Gain by Y256 in Hue Phase 12

14013D54 DISP_COLOR_S_GAIN_BY_Y256_4 — **S Gain by Y256 from Hue Phase 16 to 19** — **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	s_gain_y256_hue_19								s_gain_y256_hue_18							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s_gain_y256_hue_17								s_gain_y256_hue_16							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	s_gain_y256_hue_19	S Gain by Y256 in Hue Phase 19
23:16	s_gain_y256_hue_18	S Gain by Y256 in Hue Phase 18
15:8	s_gain_y256_hue_17	S Gain by Y256 in Hue Phase 17
7:0	s_gain_y256_hue_16	S Gain by Y256 in Hue Phase 16

14013D58 DISP_COLOR_LSP_1 — **LSP Reg Group 1** — **14140380**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				lsp_lire_sth							lsp_lire_yth					
Type				RW							RW					
Reset				1	0	1	0	0	0	0	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lsp_lire_yth		lsp_lire_sslope							lsp_lire_yslope						
Type	RW		RW							RW						
Reset	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:22	lsp_lire_sth	Saturation threshold of low IRE range
21:14	lsp_lire_yth	Luma threshold of low IRE range
13:7	lsp_lire_sslope	Saturation transient slope of low IRE range
6:0	lsp_lire_yslope	Luma transient slope of low IRE range

14013D5C DISP_COLOR_LSP_2 LSP Reg Group 2 03D07F7F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			lsp_lsat_sslope							lsp_lsat_sth						
Type			RW							RW						
Reset			0	0	0	0	1	1	1	1	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		lsp_lsat_gain								lsp_lire_gain						
Type		RW								RW						
Reset		1	1	1	1	1	1	1		1	1	1	1	1	1	1

Bit(s)	Name	Description
29:23	lsp_lsat_sslope	**Saturation transient slope of low saturation range**
22:16	lsp_lsat_sth	**Saturation threshold of low saturation range**
14:8	lsp_lsat_gain	**LSP suppression gain in low saturation range** SatSrc = (Org_SatSrc*LSAT_GAIN)>>7
6:0	lsp_lire_gain	**LSP suppression gain in low IRE range** SatSrc = (Org_SatSrc*LIRE_GAIN)>>7

Module name: DISP_CCORR Base address: (+14014000h)

Address	Name	Width	Register Function
14014000	DISP_CCORR_EN	32	CCORR Enable Register
14014004	DISP_CCORR_RESET	32	CCORR Reset Register
14014008	DISP_CCORR_INTEN	32	CCORR Interrupt Enable Register
1401400C	DISP_CCORR_INTSTA	32	CCORR Interrupt Status Register
14014010	DISP_CCORR_STATUS	32	CCORR Status Register
14014020	DISP_CCORR_CFG	32	CCORR Configuration Register
14014024	DISP_CCORR_INPUT_COUNT	32	CCORR Input Count Register
14014028	DISP_CCORR_OUTPUT_COUNT	32	CCORR Output Count Register
1401402C	DISP_CCORR_CHKSUM	32	CCORR Checksum Register
14014030	DISP_CCORR_SIZE	32	CCORR Size Register
14014080	DISP_CCORR_COEF_0	32	CCORR Color Coefficient 0
14014084	DISP_CCORR_COEF_1	32	CCORR Color Coefficient 1
14014088	DISP_CCORR_COEF_2	32	CCORR Color Coefficient 2

Address	Name	Width	Register Function
1401408C	DISP_CCORR_COEF_3	32	CCORR Color Coefficient 3
14014090	DISP_CCORR_COEF_4	32	CCORR Color Coefficient 4
140140C0	DISP_CCORR_DUMMY_REG	32	CCORR Dummy Register

14014000 DISP_CCORR_EN CCORR Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CCORR_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	CCORR_EN	**Enables CCORR** 0: Disable 1: Enable

14014004 DISP_CCORR_RESET CCORR Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CCORR_RESET
Type																RW
Reset																0

Bit(s)	Name	Description
0	CCORR_RESET	**Software reset** 0: De-assert software reset 1: Assert software reset

14014008 DISP_CCORR_INTEN CCORR Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															OF_END_INT_EN	IF_END_INT_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	OF_END_INT_EN	**Enables output frame end interrupt** 0: Disable 1: Enable
0	IF_END_INT_EN	**Enables input frame end interrupt** 0: Disable 1: Enable

1401400C DISP_CCORR_INTSTA **CCORR Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															OF_END_INT	IF_END_INT
Type															OTHER	OTHER
Reset															0	0

Bit(s)	Name	Description
1	OF_END_INT	**Output frame end interrupt status** 1: Output frame end (write 0 to clear)
0	IF_END_INT	**Input frame end interrupt status** 1: Input frame end (write 0 to clear)

14014010 DISP_CCORR_STATUS **CCORR Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					HANDSHAKE											
Type					RU											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HANDSHAKE														OF_UNFINISH	IF_UNFINISH
Type	RU														OTHER	OTHER
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
27:4	HANDSHAKE	**Handshake signals for debugging**

Bit(s)	Name	Description
1	OF_UNFINISH	**Output frame unfinished but EOF arrives** 0: Normal 1: Output frame unfinished (write 0 to clear)
0	IF_UNFINISH	**Input frame unfinished but EOF arrives** 0: Normal 1: Input frame unfinished (write 0 to clear)

14014020 DISP_CCORR_CFG **CCORR Configuration Register** **00000100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CHKSUM_SEL		CHKSUM_EN												
Type		RW		RW												
Reset		0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								HG_STALL_CG_ON						CCORR_GAMMA_OFF	CCORR_ENGINE_EN	RELAY_MODE
Type								RW						RW	RW	RW
Reset								1						0	0	0

Bit(s)	Name	Description
30:29	CHKSUM_SEL	**Selects checksum source** 0: Output 1: Input
28	CHKSUM_EN	**Enables checksum** 0: Disable 1: Enable
8	HG_STALL_CG_ON	**Stalls hg clock during stall** 0: Disable 1: Enable
2	CCORR_GAMMA_OFF	**Enables color correction without Gamma** 0: Disable 1: Enable
1	CCORR_ENGINE_EN	**Enables color correction** 0: Disable 1: Enable
0	RELAY_MODE	**Switches to RELAY mode** 0: Disable 1: Enable

14014024 DISP_CCORR_INPUT_COUNT **CCORR Input Count Register** **00010001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				INP_LINE_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name				INP_PIX_CNT													
Type				RU													
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28:16	INP_LINE_CNT	Input frame line counter
12:0	INP_PIX_CNT	Input frame pixel counter

14014028 DISP_CCORR_OUTPUT_COUNT CCORR Output Count Register 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				OUTP_LINE_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OUTP_PIX_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28:16	OUTP_LINE_CNT	Output frame line counter
12:0	OUTP_PIX_CNT	Output frame pixel counter

1401402C DISP_CCORR_CHKSUM CCORR Checksum Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			CHKSUM													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKSUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:0	CHKSUM	Checksum

14014030 DISP_CCORR_SIZE CCORR Size Register 01E00320

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				HSIZE												
Type				RW												
Reset				0	0	0	0	1	1	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VSIZE												

Type				RW												
Reset				0	0	0	1	1	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
28:16	HSIZE	Active width
12:0	VSIZE	Active height

14014080 DISP_CCORR_COEF_0 CCORR Color Coefficient 0 04000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CCORR_C00											
Type					RW											
Reset					0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CCORR_C01											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	CCORR_C00	Color coefficient C00
11:0	CCORR_C01	Color coefficient C01

14014084 DISP_CCORR_COEF_1 CCORR Color Coefficient 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CCORR_C02											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CCORR_C10											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	CCORR_C02	Color coefficient C02
11:0	CCORR_C10	Color coefficient C10

14014088 DISP_CCORR_COEF_2 CCORR Color Coefficient 2 04000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CCORR_C11											
Type					RW											
Reset					0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CCORR_C12											
Type					RW											

Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	CCORR_C11	Color coefficient C11
11:0	CCORR_C12	Color coefficient C12

1401408C DISP_CCORR_COEF_3 CCORR Color Coefficient 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CCORR_C20											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CCORR_C21											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	CCORR_C20	Color coefficient C20
11:0	CCORR_C21	Color coefficient C21

14014090 DISP_CCORR_COEF_4 CCORR Color Coefficient 4 04000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CCOR R_C2 2											
Type					RW											
Reset					0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
27:16	CCORR_C22	Color coefficient C22

140140C0 DISP_CCORR_DUMMY_REG CCORR Dummy Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY_REG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY_REG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DUMMY_REG	Dummy register

Module name: DISP_AAL Base address: (+14015000h)

Address	Name	Width	Register Function
14015000	DISP_AAL_EN	32	AAL Enable Register
14015004	DISP_AAL_RESET	32	AAL Reset Register
14015008	DISP_AAL_INTEN	32	AAL Interrupt Enable Register
1401500C	DISP_AAL_INTSTA	32	AAL Interrupt Status Register
14015010	DISP_AAL_STATUS	32	AAL Status Register
14015020	DISP_AAL_CFG	32	AAL Configuration Register
14015024	DISP_AAL_INPUT_COUNT	32	AAL Input Count Register
14015028	DISP_AAL_OUTPUT_COUNT	32	AAL Output Count Register
1401502C	DISP_AAL_CHKSUM	32	AAL Checksum Register
14015030	DISP_AAL_SIZE	32	AAL Size Register
140150C0	DISP_AAL_DUMMY_REG	32	AAL Dummy Register
140150FC	DISP_AAL_ATPG	32	DISP_AAL_ATPG
14015204	DISP_AAL_MAX_HIST_CONFIG_00	32	Configuration
1401520C	DISP_AAL_CABC_00	32	Configuration
14015214	DISP_AAL_CABC_02	32	Configuration
1401521C	DISP_AAL_CABC_04	32	Configuration
14015224	DISP_AAL_STATUS_00	32	Configuration
14015228	DISP_AAL_STATUS_01	32	Configuration
1401522C	DISP_AAL_STATUS_02	32	Configuration
14015230	DISP_AAL_STATUS_03	32	Configuration
14015234	DISP_AAL_STATUS_04	32	Configuration
14015238	DISP_AAL_STATUS_05	32	Configuration
1401523C	DISP_AAL_STATUS_06	32	Configuration
14015240	DISP_AAL_STATUS_07	32	Configuration
14015244	DISP_AAL_STATUS_08	32	Configuration
14015248	DISP_AAL_STATUS_09	32	Configuration
1401524C	DISP_AAL_STATUS_10	32	Configuration

Address	Name	Width	Register Function
14015250	DISP_AAL_STATUS_11	32	Configuration
14015254	DISP_AAL_STATUS_12	32	Configuration
14015258	DISP_AAL_STATUS_13	32	Configuration
1401525C	DISP_AAL_STATUS_14	32	Configuration
14015260	DISP_AAL_STATUS_15	32	Configuration
14015264	DISP_AAL_STATUS_16	32	Configuration
14015268	DISP_AAL_STATUS_17	32	Configuration
1401526C	DISP_AAL_STATUS_18	32	Configuration
14015270	DISP_AAL_STATUS_19	32	Configuration
14015274	DISP_AAL_STATUS_20	32	Configuration
14015278	DISP_AAL_STATUS_21	32	Configuration
1401527C	DISP_AAL_STATUS_22	32	Configuration
14015280	DISP_AAL_STATUS_23	32	Configuration
14015284	DISP_AAL_STATUS_24	32	Configuration
14015288	DISP_AAL_STATUS_25	32	Configuration
1401528C	DISP_AAL_STATUS_26	32	Configuration
14015290	DISP_AAL_STATUS_27	32	Configuration
14015294	DISP_AAL_STATUS_28	32	Configuration
14015298	DISP_AAL_STATUS_29	32	Configuration
1401529C	DISP_AAL_STATUS_30	32	Configuration
140152A0	DISP_AAL_STATUS_31	32	Configuration
140152A4	DISP_AAL_STATUS_32	32	Configuration
14015358	DISP_AAL_DRE_FLT_FORCE_00	32	Configuration
1401535C	DISP_AAL_DRE_FLT_FORCE_01	32	Configuration
14015360	DISP_AAL_DRE_FLT_FORCE_02	32	Configuration
14015364	DISP_AAL_DRE_FLT_FORCE_03	32	Configuration
14015368	DISP_AAL_DRE_FLT_FORCE_04	32	Configuration

Address	Name	Width	Register Function
1401536C	DISP_AAL_DRE_FLT_FORCE_05	32	Configuration
14015370	DISP_AAL_DRE_FLT_FORCE_06	32	Configuration
14015374	DISP_AAL_DRE_FLT_FORCE_07	32	Configuration
14015378	DISP_AAL_DRE_FLT_FORCE_08	32	Configuration
1401537C	DISP_AAL_DRE_FLT_FORCE_09	32	Configuration
14015380	DISP_AAL_DRE_FLT_FORCE_10	32	Configuration
140153B0	DISP_AAL_DRE_MAPPING_00	32	Configuration
1401540C	DISP_AAL_CABC_GAINLMT_TBL_00	32	Configuration
14015410	DISP_AAL_CABC_GAINLMT_TBL_01	32	Configuration
14015414	DISP_AAL_CABC_GAINLMT_TBL_02	32	Configuration
14015418	DISP_AAL_CABC_GAINLMT_TBL_03	32	Configuration
1401541C	DISP_AAL_CABC_GAINLMT_TBL_04	32	Configuration
14015420	DISP_AAL_CABC_GAINLMT_TBL_05	32	Configuration
14015424	DISP_AAL_CABC_GAINLMT_TBL_06	32	Configuration
14015428	DISP_AAL_CABC_GAINLMT_TBL_07	32	Configuration
1401542C	DISP_AAL_CABC_GAINLMT_TBL_08	32	Configuration
14015430	DISP_AAL_CABC_GAINLMT_TBL_09	32	Configuration
14015434	DISP_AAL_CABC_GAINLMT_TBL_10	32	Configuration
14015440	DISP_AAL_DBG_CFG_MAIN	32	DISP_AAL_DBG_CFG_MAIN
14015444	DISP_AAL_WIN_X_MAIN	32	DISP_AAL_WIN_X_MAIN
14015448	DISP_AAL_WIN_Y_MAIN	32	DISP_AAL_WIN_Y_MAIN

14015000 DISP_AAL_EN AAL Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																AAL_EN
Type																RW

Reset																0

Bit(s)	Name	Description
0	AAL_EN	

14015004 DISP_AAL_RESET AAL Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																AAL_RESET
Type																RW
Reset																0

Bit(s)	Name	Description
0	AAL_RESET	

14015008 DISP_AAL_INTEN AAL Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															OF_END_INT_EN	IF_END_INT_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	OF_END_INT_EN	
0	IF_END_INT_EN	

1401500C DISP_AAL_INTSTA AAL Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															OF_END_INT	IF_END_INT
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	OF_END_INT	
0	IF_END_INT	

14015010 DISP_AAL_STATUS AAL Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					HANDSHAKE											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HANDSHAKE														OF_UNFINISH	IF_UNFINISH
Type	RO														RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
27:4	HANDSHAKE	
1	OF_UNFINISH	
0	IF_UNFINISH	

14015020 DISP_AAL_CFG AAL Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CHKSUM_SEL		CHKSUM_EN												
Type		RW		RW												
Reset		0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												AAL_CG_DISABLE	AAL_HIST_LOCK	AAL_HIST_EN	AAL_ENGINE_EN	RELAY_MODE
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
30:29	CHKSUM_SEL	
28	CHKSUM_EN	
4	AAL_CG_DISABLE	
3	AAL_HIST_LOCK	
2	AAL_HIST_EN	
1	AAL_ENGINE_EN	
0	RELAY_MODE	

14015024 DISP_AAL_INPUT_COUNT AAL Input Count Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				INP_LINE_CNT												

Type				RO													
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name				INP_PIX_CNT													
Type				RO													
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	INP_LINE_CNT	
12:0	INP_PIX_CNT	

14015028 DISP_AAL_OUTPUT_COUNT AAL Output Count Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				OUTP_LINE_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OUTP_PIX_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	OUTP_LINE_CNT	
12:0	OUTP_PIX_CNT	

1401502C DISP_AAL_CHKSUM AAL Checksum Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						CHKSUM										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKSUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	CHKSUM	

14015030 DISP_AAL_SIZE AAL Size Register 01E00320

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				HSIZE												
Type				RW												
Reset				0	0	0	0	1	1	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VSIZE												
Type				RW												

Reset				0	0	0	1	1	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
28:16	HSIZE	
12:0	VSIZE	

140150C0 DISP_AAL_DUMMY_REG AAL Dummy Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY_REG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY_REG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DUMMY_REG	

140150FC DISP_AAL_ATPG DISP_AAL_ATPG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															aal_atpg_ct	aal_atpg_ob
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	aal_atpg_ct	
0	aal_atpg_ob	

14015204 DISP_AAL_MAX_HIST_CONFIG_00 Configuration 00080000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													maxhist_rgb_weight			
Type													RW			
Reset													1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
19:16	maxhist_rgb_weight	

Bit(s)	Name	Description

1401520C DISP_AAL_CABC_00 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	cabc_en															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31	cabc_en	

14015214 DISP_AAL_CABC_02 Configuration 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							cabc_fltgain_force									
Type							RW									
Reset							0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	cabc_fltgain_force	

1401521C DISP_AAL_CABC_04 Configuration 07FFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	cabc_ink					cabc_out_b_force									cabc_out_g_force	
Type	RW					RW									RW	
Reset	0					1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cabc_out_g_force							cabc_out_r_force								
Type	RW							RW								
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	cabc_ink	
26:18	cabc_out_b_force	
17:9	cabc_out_g_force	
8:0	cabc_out_r_force	

14015224 DISP_AAL_STATUS_00 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_00					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_00															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_00	

14015228 DISP_AAL_STATUS_01 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_01					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_01															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_01	

1401522C DISP_AAL_STATUS_02 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_02					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_02															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_02	

14015230 DISP_AAL_STATUS_03 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_03					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_03															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_03	

14015234 DISP_AAL_STATUS_04 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_04					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_04															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_04	

14015238 DISP_AAL_STATUS_05 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_05					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_05															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_05	

1401523C DISP_AAL_STATUS_06 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_06					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_06															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_06	

14015240 DISP_AAL_STATUS_07 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name											max_hist_07					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_07															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_07	

14015244 DISP_AAL_STATUS_08 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_08					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_08															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_08	

14015248 DISP_AAL_STATUS_09 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_09					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_09															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_09	

1401524C DISP_AAL_STATUS_10 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_10					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_10															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_10	

14015250 DISP_AAL_STATUS_11 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_11					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_11															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_11	

14015254 DISP_AAL_STATUS_12 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_12					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_12															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_12	

14015258 DISP_AAL_STATUS_13 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_13					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_13															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_13	

1401525C DISP_AAL_STATUS_14 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_14					
Type											RO					

Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_14															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_14	

14015260 DISP_AAL_STATUS_15 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_15					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_15															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_15	

14015264 DISP_AAL_STATUS_16 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_16					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_16															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_16	

14015268 DISP_AAL_STATUS_17 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_17					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_17															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_17	

Bit(s)	Name	Description

1401526C DISP_AAL_STATUS_18 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_18					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_18															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_18	

14015270 DISP_AAL_STATUS_19 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_19					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_19															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_19	

14015274 DISP_AAL_STATUS_20 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_20					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_20															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_20	

14015278 DISP_AAL_STATUS_21 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_21					
Type											RO					
Reset											0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_21															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_21	

1401527C DISP_AAL_STATUS_22 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_22					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_22															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_22	

14015280 DISP_AAL_STATUS_23 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_23					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_23															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_23	

14015284 DISP_AAL_STATUS_24 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_24					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_24															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_24	

14015288 DISP_AAL_STATUS_25 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_25					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_25															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_25	

1401528C DISP_AAL_STATUS_26 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_26					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_26															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_26	

14015290 DISP_AAL_STATUS_27 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_27					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_27															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_27	

14015294 DISP_AAL_STATUS_28 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_28					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_28															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_28	

14015298 DISP_AAL_STATUS_29 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_29					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_29															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_29	

1401529C DISP_AAL_STATUS_30 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_30					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_30															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_30	

140152A0 DISP_AAL_STATUS_31 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_31					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_31															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_31	

140152A4 DISP_AAL_STATUS_32 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											max_hist_32					
Type											RO					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_hist_32															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	max_hist_32	

14015358 DISP_AAL_DRE_FLT_FORCE_00 Configuration **00100100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									dre_gain_flt_1_force							
Type									RW							
Reset									0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dre_gain_flt_1_fo rce				dre_gain_flt_0_force											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:12	dre_gain_flt_1_force	
11:0	dre_gain_flt_0_force	

1401535C DISP_AAL_DRE_FLT_FORCE_01 Configuration **00100100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										dre_gain_flt_3_force						
Type										RW						
Reset										0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dre_gain_flt_3_fo rce				dre_gain_flt_2_force											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
22:12	dre_gain_flt_3_force	
11:0	dre_gain_flt_2_force	

14015360 DISP_AAL_DRE_FLT_FORCE_02 Configuration **00080100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											dre_gain_flt_5_force					
Type											RW					
Reset											0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dre_gain_flt_5_force					dre_gain_flt_4_force										

Type	RW					RW										
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:11	dre_gain_flt_5_force	
10:0	dre_gain_flt_4_force	

14015364 DISP_AAL_DRE_FLT_FORCE_03 Configuration 20080100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		dre_gain_flt_8_force										dre_gain_flt_7_force				
Type		RW										RW				
Reset		0	1	0	0	0	0	0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dre_gain_flt_7_force					dre_gain_flt_6_force										
Type	RW					RW										
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:21	dre_gain_flt_8_force	
20:11	dre_gain_flt_7_force	
10:0	dre_gain_flt_6_force	

14015368 DISP_AAL_DRE_FLT_FORCE_04 Configuration 10040100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			dre_gain_flt_11_force										dre_gain_flt_10_force			
Type			RW										RW			
Reset			0	1	0	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dre_gain_flt_10_force						dre_gain_flt_9_force									
Type	RW						RW									
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:20	dre_gain_flt_11_force	
19:10	dre_gain_flt_10_force	
9:0	dre_gain_flt_9_force	

1401536C DISP_AAL_DRE_FLT_FORCE_05 Configuration 10040100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			dre_gain_flt_14_force										dre_gain_flt_13_force			
Type			RW										RW			
Reset			0	1	0	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dre_gain_flt_13_force						dre_gain_flt_12_force									
Type	RW						RW									
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
29:20	dre_gain_flt_14_force	
19:10	dre_gain_flt_13_force	
9:0	dre_gain_flt_12_force	

14015370 DISP_AAL_DRE_FLT_FORCE_06 Configuration **10040100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			dre_gain_flt_17_force										dre_gain_flt_16_force			
Type			RW										RW			
Reset			0	1	0	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dre_gain_flt_16_force						dre_gain_flt_15_force									
Type	RW						RW									
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:20	dre_gain_flt_17_force	
19:10	dre_gain_flt_16_force	
9:0	dre_gain_flt_15_force	

14015374 DISP_AAL_DRE_FLT_FORCE_07 Configuration **04020100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						dre_gain_flt_20_force									dre_gain_flt_19_force	
Type						RW									RW	
Reset						1	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dre_gain_flt_19_force							dre_gain_flt_18_force								
Type	RW							RW								
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:18	dre_gain_flt_20_force	
17:9	dre_gain_flt_19_force	
8:0	dre_gain_flt_18_force	

14015378 DISP_AAL_DRE_FLT_FORCE_08 Configuration **04020100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						dre_gain_flt_23_force									dre_gain_flt_22_force	
Type						RW									RW	
Reset						1	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dre_gain_flt_22_force							dre_gain_flt_21_force								
Type	RW							RW								
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:18	dre_gain_flt_23_force	

Bit(s)	Name	Description
17:9	dre_gain_flt_22_force	
8:0	dre_gain_flt_21_force	

1401537C DISP_AAL_DRE_FLT_FORCE_09 Configuration 04020100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						dre_gain_flt_26_force									dre_gain_flt_25_force	
Type						RW									RW	
Reset						1	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dre_gain_flt_25_force							dre_gain_flt_24_force								
Type	RW							RW								
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:18	dre_gain_flt_26_force	
17:9	dre_gain_flt_25_force	
8:0	dre_gain_flt_24_force	

14015380 DISP_AAL_DRE_FLT_FORCE_10 Configuration 00020100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															dre_gain_flt_28_force	
Type															RW	
Reset															1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dre_gain_flt_28_force							dre_gain_flt_27_force								
Type	RW							RW								
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:9	dre_gain_flt_28_force	
8:0	dre_gain_flt_27_force	

140153B0 DISP_AAL_DRE_MAPPING_00 Configuration 00000018

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												dre_map_bypass	dre_map_rgb_weight			
Type												RW	RW			
Reset												1	1	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
4	dre_map_bypass	
3:0	dre_map_rgb_weight	

1401540C DISP_AAL_CABC_GAINLMT_TBL_00 Configuration 3FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			cabc_gainlmt_02										cabc_gainlmt_01			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cabc_gainlmt_01						cabc_gainlmt_00									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	cabc_gainlmt_02	
19:10	cabc_gainlmt_01	
9:0	cabc_gainlmt_00	

14015410 DISP_AAL_CABC_GAINLMT_TBL_01 Configuration 3FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			cabc_gainlmt_05										cabc_gainlmt_04			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cabc_gainlmt_04						cabc_gainlmt_03									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	cabc_gainlmt_05	
19:10	cabc_gainlmt_04	
9:0	cabc_gainlmt_03	

14015414 DISP_AAL_CABC_GAINLMT_TBL_02 Configuration 3FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			cabc_gainlmt_08										cabc_gainlmt_07			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cabc_gainlmt_07						cabc_gainlmt_06									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	cabc_gainlmt_08	
19:10	cabc_gainlmt_07	
9:0	cabc_gainlmt_06	

Bit(s)	Name	Description

14015418 DISP_AAL_CABC_GAINLMT_TBL_03 Configuration 3FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			cabc_gainlmt_11										cabc_gainlmt_10			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cabc_gainlmt_10						cabc_gainlmt_09									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	cabc_gainlmt_11	
19:10	cabc_gainlmt_10	
9:0	cabc_gainlmt_09	

1401541C DISP_AAL_CABC_GAINLMT_TBL_04 Configuration 3FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			cabc_gainlmt_14										cabc_gainlmt_13			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cabc_gainlmt_13						cabc_gainlmt_12									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	cabc_gainlmt_14	
19:10	cabc_gainlmt_13	
9:0	cabc_gainlmt_12	

14015420 DISP_AAL_CABC_GAINLMT_TBL_05 Configuration 3FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			cabc_gainlmt_17										cabc_gainlmt_16			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cabc_gainlmt_16						cabc_gainlmt_15									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	cabc_gainlmt_17	
19:10	cabc_gainlmt_16	
9:0	cabc_gainlmt_15	

14015424 DISP_AAL_CABC_GAINLMT_TBL_06 Configuration 3FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			cabc_gainlmt_20										cabc_gainlmt_19			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cabc_gainlmt_19						cabc_gainlmt_18									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	cabc_gainlmt_20	
19:10	cabc_gainlmt_19	
9:0	cabc_gainlmt_18	

14015428 DISP_AAL_CABC_GAINLMT_TBL_07 Configuration 3FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			cabc_gainlmt_23										cabc_gainlmt_22			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cabc_gainlmt_22						cabc_gainlmt_21									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	cabc_gainlmt_23	
19:10	cabc_gainlmt_22	
9:0	cabc_gainlmt_21	

1401542C DISP_AAL_CABC_GAINLMT_TBL_08 Configuration 3FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			cabc_gainlmt_26										cabc_gainlmt_25			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cabc_gainlmt_25						cabc_gainlmt_24									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	cabc_gainlmt_26	
19:10	cabc_gainlmt_25	
9:0	cabc_gainlmt_24	

14015430 DISP_AAL_CABC_GAINLMT_TBL_09 Configuration 3FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			cabc_gainlmt_29										cabc_gainlmt_28			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cabc_gainlmt_28						cabc_gainlmt_27									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	cabc_gainlmt_29	
19:10	cabc_gainlmt_28	
9:0	cabc_gainlmt_27	

14015434 DISP_AAL_CABC_GAINLMT_TBL_10 Configuration 3FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			cabc_gainlmt_32										cabc_gainlmt_31			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cabc_gainlmt_31						cabc_gainlmt_30									
Type	RW						RW									
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
29:20	cabc_gainlmt_32	
19:10	cabc_gainlmt_31	
9:0	cabc_gainlmt_30	

14015440 DISP_AAL_DBG_CFG_MAIN DISP_AAL_DBG_CFG_MAIN 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															split_swap	split_en
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	split_swap	**Swaps DRE demo window or not** 0: Does not swap 1: Swap demo window
0	split_en	**Splits DRE demo window or not** 0: Process whole window 1: Split demo window

14015444 DISP_AAL_WIN_X_MAIN DISP_AAL_WIN_X_MAIN 1FFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				win_x_end												
Type				RW												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				win_x_start												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	win_x_end	**X end for DRE processing window**
12:0	win_x_start	**X start for DRE processing window**

14015448 DISP_AAL_WIN_Y_MAIN DISP_AAL_WIN_Y_MAIN 1FFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				win_y_end												
Type				RW												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				win_y_start												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	win_y_end	Y end for DRE processing window
12:0	win_y_start	Y start for DRE processing window

Module name: DISP_GAMMA Base address: (+14016000h)

Address	Name	Width	Register Function
14016000	**DISP_GAMMA_EN**	32	GAMMA Enable Register
14016004	**DISP_GAMMA_RESET**	32	GAMMA Reset Register
14016008	**DISP_GAMMA_INTEN**	32	GAMMA Interrupt Enable Register
1401600C	**DISP_GAMMA_INTSTA**	32	GAMMA Interrupt Status Register
14016010	**DISP_GAMMA_STATUS**	32	GAMMA Status Register
14016020	**DISP_GAMMA_CFG**	32	GAMMA Configuration Register
14016024	**DISP_GAMMA_INPUT_COUNT**	32	GAMMA Input Count Register
14016028	**DISP_GAMMA_OUTPUT_COUNT**	32	GAMMA Output Count Register
1401602C	**DISP_GAMMA_CHKSUM**	32	GAMMA Checksum Register
14016030	**DISP_GAMMA_SIZE**	32	GAMMA Size Register
140160C0	**DISP_GAMMA_DUM**	32	GAMMA Dummy Register

Address	Name	Width	Register Function
	MY_REG		
14016700~ 14016efc	**DISP_GAMMA_LUT [n] (n=0~511)**	32	GAMMA LUT Entries

14016000 DISP_GAMMA_EN GAMMA Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																GAMMA_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	GAMMA_EN	**Enables GAMMA** 0: Disable 1: Enable

14016004 DISP_GAMMA_RESET GAMMA Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																GAMMA_RESET
Type																RW
Reset																0

Bit(s)	Name	Description
0	GAMMA_RESET	**Software reset** 0: De-assert software reset 1: Assert software reset

14016008 DISP_GAMMA_INTEN GAMMA Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															OF_END_INT_EN	IF_END_INT_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	OF_END_INT_EN	**Enables output frame end interrupt** 0: Disable 1: Enable
0	IF_END_INT_EN	**Enables input frame end interrupt** 0: Disable 1: Enable

1401600C DISP_GAMMA_INTSTA **GAMMA Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															OF_END_INT	IF_END_INT
Type															OTHER	OTHER
Reset															0	0

Bit(s)	Name	Description
1	OF_END_INT	**Output frame end interrupt status** 1: Output frame end (write 0 to clear)
0	IF_END_INT	**Input frame end interrupt status** 1: Input frame end (write 0 to clear)

14016010 DISP_GAMMA_STATUS **GAMMA Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													HANDSHAKE			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HANDSHAKE														OF_UNFINISH	IF_UNFINISH
Type	RU														OTHER	OTHER
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
19:4	HANDSHAKE	**Handshake signals for debugging**
1	OF_UNFINISH	**Output frame unfinished but EOF arrives**

Bit(s)	Name	Description
0	IF_UNFINISH	0: Normal 1: Output frame unfinished (write 0 to clear) **Input frame unfinished but EOF arrives** 0: Normal 1: Input frame unfinished (write 0 to clear)

14016020 DISP_GAMMA_CFG **GAMMA Configuration Register** **00000100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CHKSUM_SEL		CHKSUM_EN												
Type		RW		RW												
Reset		0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								STALL_CG_ON							GAMMA_LUT_EN	RELAY_MODE
Type								RW							RW	RW
Reset								1							0	0

Bit(s)	Name	Description
30:29	CHKSUM_SEL	**Selects checksum source** 0: Output 1: Input
28	CHKSUM_EN	**Enables checksum** 0: Disable 1: Enable
8	STALL_CG_ON	**Enable CG for pipeline stall** 0: Disable 1: Enable
1	GAMMA_LUT_EN	**Enables gamma table** 0: Disable 1: Enable
0	RELAY_MODE	**Switches to RELAY mode** 0: Disable 1: Enable

14016024 DISP_GAMMA_INPUT_COUNT **GAMMA Input Count Register** **00010001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				INP_LINE_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				INP_PIX_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28:16	INP_LINE_CNT	Input frame line counter
12:0	INP_PIX_CNT	Input frame pixel counter

14016028 DISP_GAMMA_OUTPUT_COUNT GAMMA Output Count Register 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				OUTP_LINE_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OUTP_PIX_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28:16	OUTP_LINE_CNT	Output frame line counter
12:0	OUTP_PIX_CNT	Output frame pixel counter

1401602C DISP_GAMMA_CHKSUM GAMMA Checksum Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			CHKSUM													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKSUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:0	CHKSUM	Checksum

14016030 DISP_GAMMA_SIZE GAMMA Size Register 01E00320

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				HSIZE												
Type				RW												
Reset				0	0	0	0	1	1	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VSIZE												
Type				RW												
Reset				0	0	0	1	1	0	0	1	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
28:16	HSIZE	Active width
12:0	VSIZE	Active height

140160C0 DISP_GAMMA_DUMMY_REG GAMMA Dummy Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY_REG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY_REG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DUMMY_REG	Dummy register

14016700~14016EFC DISP_GAMMA_LUT[n](n=0~511) GAMMA LUT Entries 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			GAMMA_LUT_R										GAMMA_LUT_G			
Type			RW										RW			
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAMMA_LUT_G						GAMMA_LUT_B									
Type	RW						RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:20	GAMMA_LUT_R	9-bit to 10-bit gamma correction for R channel
19:10	GAMMA_LUT_G	9-bit to 10-bit gamma correction for G channel
9:0	GAMMA_LUT_B	9-bit to 10-bit gamma correction for B channel

Module name: DISP_DITHER Base address: (+14018000h)

Address	Name	Width	Register Function
14018000	DISP_DITHER_EN	32	DITHER Enable Register
14018004	DISP_DITHER_RESET	32	DITHER Reset Register
14018008	DISP_DITHER_INTEN	32	DITHER Interrupt Enable Register
1401800C	DISP_DITHER_INTSTA	32	DITHER Interrupt Status Register
14018010	DISP_DITHER_STATUS	32	DITHER Status Register
14018020	DISP_DITHER_CFG	32	DITHER Configuration Register

Address	Name	Width	Register Function
14018024	DISP_DITHER_INPUT_COUNT	32	DITHER Input Count Register
14018028	DISP_DITHER_OUTPUT_COUNT	32	DITHER Output Count Register
1401802C	DISP_DITHER_CHKSUM	32	DITHER Checksum Register
14018030	DISP_DITHER_SIZE	32	DITHER Size Register
140180C0	DISP_DITHER_DUMMY_REG	32	DITHER Dummy Register
14018100	DISP_DITHER_0	32	DITHER Dither Setting 0
14018114	DISP_DITHER_5	32	DITHER Dither Setting 5
14018118	DISP_DITHER_6	32	DITHER Dither Setting 6
1401811C	DISP_DITHER_7	32	DITHER Dither Setting 7
14018120	DISP_DITHER_8	32	DITHER Dither Setting 8
14018124	DISP_DITHER_9	32	DITHER Dither Setting 9
14018128	DISP_DITHER_10	32	DITHER Dither Setting 10
1401812C	DISP_DITHER_11	32	DITHER Dither Setting 11
14018130	DISP_DITHER_12	32	DITHER Dither Setting 12
14018134	DISP_DITHER_13	32	DITHER Dither Setting 13
14018138	DISP_DITHER_14	32	DITHER Dither Setting 14
1401813C	DISP_DITHER_15	32	DITHER Dither Setting 15
14018140	DISP_DITHER_16	32	DITHER Dither Setting 16
14018144	DISP_DITHER_17	32	DITHER Dither Setting 17

14018000 DISP_DITHER_EN **DITHER Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DITHER_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	DITHER_EN	**Enables DITHER** 0: Disable 1: Enable

14018004 DISP_DITHER_RESET **DITHER Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DITHER_RESET
Type																RW
Reset																0

Bit(s)	Name	Description
0	DITHER_RESET	**Software reset** 0: De-assert software reset 1: Assert software reset

14018008 DISP_DITHER_INTEN **DITHER Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															OF_END_INT_EN	IF_END_INT_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	OF_END_INT_EN	**Enables output frame end interrupt** 0: Disable 1: Enable
0	IF_END_INT_EN	**Enables input frame end interrupt** 0: Disable 1: Enable

1401800C DISP_DITHER_INTSTA **DITHER Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															OF_END_INT	IF_END_INT
Type															OTHER	OTHER
Reset															0	0

Bit(s)	Name	Description
1	OF_END_INT	**Output frame end interrupt status**

Bit(s)	Name	Description
		1: Output frame end (write 0 to clear)
0	IF_END_INT	**Input frame end interrupt status** 1: Input frame end (write 0 to clear)

14018010 DISP_DITHER_STATUS **DITHER Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													HANDSHAKE			
Type													RU			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HANDSHAKE														OF_UNFINISH	IF_UNFINISH
Type	RU														OTHER	OTHER
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
19:4	HANDSHAKE	**Handshake signals for debugging**
1	OF_UNFINISH	**Output frame unfinished but EOF arrives** 0: Normal 1: Output frame unfinished (write 0 to clear)
0	IF_UNFINISH	**Input frame unfinished but EOF arrives** 0: Normal 1: Input frame unfinished (write 0 to clear)

14018020 DISP_DITHER_CFG **DITHER Configuration Register** **00000100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CHKSUM_SEL		CHKSUM_EN												
Type		RW		RW												
Reset		0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							MODULE_STALL_CG_ON	SUB_MODULE_STALL_CG_ON							DITHER_ENGINE_EN	RELAY_MODE
Type							RW	RW							RW	RW
Reset							0	1							0	0

Bit(s)	Name	Description
30:29	CHKSUM_SEL	**Selects checksum source** 0: Output 1: Input 2: After dithering
28	CHKSUM_EN	**Enables checksum** 0: Disable

Bit(s)	Name	Description
		1: Enable
9	MODULE_STALL_CG_ON	**Stall CG on module level** 0: Disable 1: Enable
8	SUB_MODULE_STALL_CG_ON	**Stall CG on submodule level** 0: Disable 1: Enable
1	DITHER_ENGINE_EN	**Enables dithering** 0: Disable 1: Enable
0	RELAY_MODE	**Switches to RELAY mode** 0: Disable 1: Enable

14018024 DISP_DITHER_INPUT_COUNT **DITHER Input Count Register** **00010001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				INP_LINE_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				INP_PIX_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28:16	INP_LINE_CNT	Input frame line counter
12:0	INP_PIX_CNT	Input frame pixel counter

14018028 DISP_DITHER_OUTPUT_COUNT **DITHER Output Count Register** **00010001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				OUTP_LINE_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OUTP_PIX_CNT												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28:16	OUTP_LINE_CNT	Output frame line counter
12:0	OUTP_PIX_CNT	Output frame pixel counter

1401802C DISP_DITHE **DITHER Checksum Register** **00000000**

R_CHKSUM

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			CHKSUM													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKSUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:0	CHKSUM	Checksum

14018030 DISP_DITHER_SIZE DITHER Size Register 01E00320

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				HSIZE												
Type				RW												
Reset				0	0	0	0	1	1	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VSIZE												
Type				RW												
Reset				0	0	0	1	1	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
28:16	HSIZE	Active width
12:0	VSIZE	Active height

140180C0 DISP_DITHER_DUMMY_REG DITHER Dummy Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY_REG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY_REG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DUMMY_REG	Dummy register

14018100 DISP_DITHER_0 DITHER Dither Setting 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name								crc_clr				crc_start				crc_cen
Type								RW				RW				RW
Reset								0				0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	frame_done_del											out_sel				
Type	RW											RW				
Reset	0	0	0	0	0	0	0	0				0				

Bit(s)	Name	Description
24	crc_clr	**Write 1 to clear CRC result.**
20	crc_start	**Write 1 to start CRC counting.**
16	crc_cen	**Enables CRC engine CG** 0: Disable 1: Enable
15:8	frame_done_del	**Frame done return delay**
4	out_sel	**Selects dither output** 0: Through dither 1: Bypass dither

14018114 DISP_DITHER_5 DITHER Dither Setting 5 000000F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	w_demo															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
15:0	w_demo	Short line length

14018118 DISP_DITHER_6 DITHER Dither Setting 6 00003004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																wrap_mode
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	left_en		fphase_r	fphase_en			fphase						round_en	rdither_en	lfsr_en	edither_en
Type	RW		RW	RW			RW						RW	RW	RW	RW
Reset	0	0	1	1			0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
16	wrap_mode	**Enables 2-channel mode** 0: Disable 1: Enable
15:14	left_en	**Enables left part of screen dither** 0: Dither run at full screen 1: Dither run at left part of screen
13	fphase_r	
12	fphase_en	**Enables running order dither frame phase control**
9:4	fphase	**Running order dither frame phase increment.** *Note:* *1. If ROUND_EN = 1, the output will only be rounded (no matter what RDITHER_EN and EDITHER_EN settings are).* *2. RDITHER_EN and EDITHER_EN can work together.*
3	round_en	**Enables rounding for dither function** When rounding method is used, both running order and error dispersion cannot be used.
2	rdither_en	**Enables running order dither** Running order dither must be set when ROUND_EN is set to 0. Running order dither can run with error dispersion when EDOTHER_EN is set to 1.
1	lfsr_en	**Enables LFSR-type dither**
0	edither_en	**Enables error dispersion dither** Error dispersion dither must be set when ROUND_EN is set to 0. Running order dither can run with error dispersion when RDITHER_EN is set to 1.

1401811C DISP_DITHER_7 DITHER Dither Setting 7 00000111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							drmo d_b				drmod_g				drmod_r	
Type							RW				RW				RW	
Reset							0	1			0	1			0	1

Bit(s)	Name	Description
9:8	drmod_b	**Selects dither mode for B channel** 0: No dither 1: 10-bit dither to 8-bit 2: 10-bit dither to 6-bit 3: 10-bit dither to 4-bit
5:4	drmod_g	**Selects dither mode for G channel** 0: No dither 1: 10-bit dither to 8-bit 2: 10-bit dither to 6-bit 3: 10-bit dither to 4-bit
1:0	drmod_r	**Selects dither mode for R channel** 0: No dither 1: 10-bit dither to 8-bit 2: 10-bit dither to 6-bit 3: 10-bit dither to 4-bit

14018120 DISP_DITHER_8 DITHER Dither Setting 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ink_data_r									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ink
Type																RW
Reset																0

Bit(s)	Name	Description
25:16	ink_data_r	Ink data for R
0	ink	Enables ink

14018124 DISP_DITHER_9 DITHER Dither Setting 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ink_data_b									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							ink_data_g									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	ink_data_b	Ink data for B
9:0	ink_data_g	Ink data for G

14018128 DISP_DITHER_10 DITHER Dither Setting 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						fpha se_b it					fphase_se l				fphase_ct rl	
Type						RW					RW				RW	
Reset						0	0	0			0	0			0	0

Bit(s)	Name	Description
10:8	fphase_bit	**fphase_bit XOR bus number** *Note: This function checks reg_fphase_sel.* Only 0, 1, 2, 4 and 6 are available. 0: No effect on fphase (XOR disabled)
5:4	fphase_sel	**fphase XOR function: fphase does self bit-wise xor.**

Bit(s)	Name	Description
		Note: This function checks reg_fphase_sel. Only bit 2, bit 4 and bit 6 are available. 0: Disable fphase XOR 1: Effect fphase[0]~[1] based on the value of reg_fphase_sel is 1 or 2 2: Effect fphase[0]~[3] based on the value of reg_fphase_sel is 1, 2 or 4 3: Effect fphase[0]~[5] based on the value of reg_fphase_sel is 1, 2, 4 or 6
1:0	fphase_ctrl	**Selects fphase range add with rdither table** 00: 0~63 01: 0~16 10: 0~3

1401812C DISP_DITHER_11 DITHER Dither Setting 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			sub_b				sub_g				sub_r					subpix_en
Type			RW				RW				RW					RW
Reset			0	0			0	0			0	0				0

Bit(s)	Name	Description
13:12	sub_b	
9:8	sub_g	
5:4	sub_r	
0	subpix_en	**Enables sub-pixel dither mode** 0: Disable 1: Enable

14018130 DISP_DITHER_12 DITHER Dither Setting 12 00000011

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	h_active															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											table_en					lsb_off
Type											RW					RW
Reset											0	1				1

Bit(s)	Name	Description
31:16	h_active	**Reserved**
5:4	table_en	**Active bit of magic table for running order** 01: Phase active in bit3 ~ bit0 10: Phase active in bit1 ~ bit0

Bit(s)	Name	Description
		Others: Phase active in bit5 ~ bit0
0	lsb_off	**Turns off LSB for dither function**

14018134 DISP_DITHER_13 DITHER Dither Setting 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						rshift_b				rshift_g				rshift_r		
Type						RW				RW				RW		
Reset						0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
10:8	rshift_b	
6:4	rshift_g	
2:0	rshift_r	

14018138 DISP_DITHER_14 DITHER Dither Setting 14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							debug_mode			diff_shift						testpin_en
Type							RW			RW						RW
Reset							0	0		0	0	0				0

Bit(s)	Name	Description
9:8	debug_mode	**Enables debugging mode** 0: Disable 1: Enable
6:4	diff_shift	**Debugging mode difference shift positions**
0	testpin_en	**Enables testpin input**

1401813C DISP_DITHER_15 DITHER Dither Setting 15 20200001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		lsb_err_shift_r				ovflw_bit_r				add_lshift_r				input_rshift_r		
Type		RW				RW				RW				RW		
Reset		0	1	0		0	0	0		0	1	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																new_

																bit_mode
Type																RW
Reset																1

Bit(s)	Name	Description
30:28	lsb_err_shift_r	**Selects RED LSB error bit**
26:24	ovflw_bit_r	**Selects RED overflow bit**
22:20	add_lshift_r	
18:16	input_rshift_r	
0	new_bit_mode	**Enables modified test algorithm** 0: Disable 1: Enable

14018140 DISP_DITHER_16 DITHER Dither Setting 16 20202020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		lsb_err_shift_b				ovflw_bit_b				add_lshift_b				input_rshift_b		
Type		RW				RW				RW				RW		
Reset		0	1	0		0	0	0		0	1	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		lsb_err_shift_g				ovflw_bit_g				add_lshift_g				input_rshift_g		
Type		RW				RW				RW				RW		
Reset		0	1	0		0	0	0		0	1	0		0	0	0

Bit(s)	Name	Description
30:28	lsb_err_shift_b	Selects GREEN LSB error bit
26:24	ovflw_bit_b	Selects GREEN overflow bit
22:20	add_lshift_b	
18:16	input_rshift_b	
14:12	lsb_err_shift_g	Selects BLUE LSB error bit
10:8	ovflw_bit_g	Selects BLUE overflow bit
6:4	add_lshift_g	BLUE addend left shift bits
2:0	input_rshift_g	BLUE input right shift bits

14018144 DISP_DITHER_17 DITHER Dither Setting 17 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																crc_rdy
Type																RU
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crc_out															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	crc_rdy	CRC ready
15:0	crc_out	CRC result

4.2 DISPLAY PWM Generator

Module name: DISP_PWM Base address: (+1100f000h)

Address	Name	Width	Register Function
1100F000	DISP_PWM_EN	32	PWM Enable
1100F004	DISP_PWM_RST	32	PWM Reset
1100F008	DISP_PWM_COMMIT	32	PWM Commit
1100F010	DISP_PWM_CON_0	32	PWM Control 0
1100F014	DISP_PWM_CON_1	32	PWM Control 1
1100F018	DISP_PWM_GRADUAL	32	PWM Gradual Control
1100F01C	DISP_PWM_GRADUAL_RO	32	PWM Gradual Control Output
1100F020	DISP_PWM_DEBUG	32	PWM Debug Register
1100F030	DISP_PWM_DUMMY	32	PWM Dummy Register

1100F000 DISP_PWM_EN PWM Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																PWM_EN
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		PWM_EN	Enables PWM or not

1100F004 DISP_PWM_RST PWM Reset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																PWM_RST
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		PWM_RST	SW resets PWM

1100F008 DISP_PWM_COMMIT PWM Commit 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																PWM_COMMIT
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		PWM_COMMIT	Commits shadow register values to working registers

1100F010 DISP_PWM_CON_0 PWM Control 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							PWM_ CLKD IV									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									PWM_DONT_UPDATE	TE_EDGE_SEL	PWM_UPDATE_SEL		PWM_FRAME_SYNC	PWM_POLARITY		PWM_AUTO_MODE
Type									RW	RW	RW		RW	RW		RW
Reset									0	0	0	0	0	0		0

Bit(s)	Mnemonic	Name	Description
25:16		PWM_CLKDIV	**Selects PWM clock division** PWM clock frequency = 26MHz/(PWM_CLKDIV + 1)
7		PWM_DONT_UPDATE	**Disables PWM setting update** 0: PWM setting can be normally updated. 1: PWM setting cannot be updated.
6		TE_EDGE_SEL	**Selects TE edge** 0: Rising edge 1: Falling edge
5:4		PWM_UPDATE_SEL	**Selects PWM setting update source** 00: PWM setting is updated by mutex SOF. 01: PWM setting is updated by DSI internal TE. 10: PWM setting is updated by DSI external TE. 11: PWM setting is updated by DBI external TE.
3		PWM_FRAME_SYNC	**PWM waveform frame synchronization** 0: PWM waveform is free-run. 1: PWM waveform rising edge is synchronized with SOF.
2		PWM_POLARITY	**PWM waveform polarity** 0: Default=0; duty = high level/period 1: Default=1; duty = low level/period
0		PWM_AUTO_MODE	**PWM generator auto mode**

Bit(s)	Mnemonic	Name	Description
			0: Manual mode (defined by DISP_PWM_CON_1) 1: Auto mode (from BLS)

1100F014 DISP_PWM_CON_1 PWM Control 1 000003FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				PWM_HIGH_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PWM_PERIOD											
Type					RW											
Reset					0	0	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
28:16		PWM_HIGH_WIDTH	**PWM high width = PWM_HIGH_WIDTH + 1** Unit: clk Only for manual mode.
11:0		PWM_PERIOD	**PWM period = PWM_PERIOD + 1 (unit: clk)** (Only for manual mode)

1100F018 DISP_PWM_GRADUAL PWM Gradual Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PWM_GRADUAL_STEP							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			PWM_GRADUAL_FRAME													PWM_GRADUAL_EN
Type			RW													RW
Reset			0	0	0	0	0	0								0

Bit(s)	Mnemonic	Name	Description
23:16		PWM_GRADUAL_STEP	**PWM duty gradual step** PWM_GRADUAL_STEP needs to be > 0.
13:8		PWM_GRADUAL_FRAME	**PWM duty gradual frame** PWM duty updates every (PWM_GRADUAL_FRAME + 1) frames.
0		PWM_GRADUAL_EN	**Enables PWM duty gradual**

1100F01C DISP_PWM_GRADUAL_RO PWM Gradual Control Output 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PWM_HIGH_WIDTH_GRAD												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0		PWM_HIGH_WIDTH_GRAD	PWM high width after gradual control

1100F020 DISP_PWM_DEBUG **PWM Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PWM_DOUBLE_BUFFER_DIS	DOUBLE_BUFFER_DIS
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1		PWM_DOUBLE_BUFFER_DIS	Disables PWM setting double buffer
0		DOUBLE_BUFFER_DIS	Disables register double buffer

1100F030 DISP_PWM_DUMMY **PWM Dummy Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		DUMMY	Reserved

4.3 DPI (Digital Parallel Interface)

Module name: DISP_DPI Base address: (+1401e000h)

Address	Name	Width	Register Function
1401E000	DPI_EN	32	DPI Enable Register
1401E004	DPI_RST	32	DPI Software Reset Register
1401E008	DPI_INTEN	32	DPI IRQ Enable Register
1401E00C	DPI_INTSTA	32	DPI IRQ Status Register
1401E010	DPI_CON	32	DPI Control Register
1401E014	DPI_OUTPUT_SETTING	32	DPI Output Stage Setting Register
1401E018	DPI_SIZE	32	DPI Size Register
1401E01C	DPI_DDR_SETTING	32	DPI DDR Register
1401E020	DPI_TGEN_HWIDTH	32	DPI Timing Generator Horizontal Sync Pulse Width Control Register
1401E024	DPI_TGEN_HPORCH	32	DPI Timing Generator Horizontal Front/Back Porch Control Register
1401E028	DPI_TGEN_VWIDTH	32	DPI Timing Generator Vertical Sync Pulse Width Control Register
1401E02C	DPI_TGEN_VPORCH	32	DPI Timing Generator Vertical Front/Back Porch Control Register
1401E030	DPI_BG_HCNTL	32	DPI Background Horizontal Control Register
1401E034	DPI_BG_VCNTL	32	DPI Background Vertical Control Register
1401E038	DPI_BG_COLOR	32	DPI Background Color Register
1401E03C	DPI_FIFO_CTL	32	DPI FIFO CTL
1401E040	DPI_STATUS	32	DPI Status Register
1401E044	DPI_TMODE	32	DPI Test Mode Register
1401E048	DPI_CHKSUM	32	DPI Checksum Register
1401E04C	DPI_DCM	32	DPI DCM Register
1401E050	DPI_DUMMY	32	
1401E054	DPI_GPIO_MODE	32	DPI Output Control Signal Has Two GPIO Output Select
1401E068	DPI_TGEN_VWIDTH_LEVEN	32	DPI Timing Generator Vertical Sync Pulse Width Control Register (Left Frame, Even Field)
1401E06C	DPI_TGEN_VPORCH_LEVEN	32	DPI Timing Generator Vertical Front/Back Porch Control Register (Left Frame, Even Field)
1401E070	DPI_TGEN_VWIDTH_RODD	32	DPI Timing Generator Vertical Sync Pulse Width Control Register (Right Frame, Odd Field)
1401E074	DPI_TGEN_VPORCH_RODD	32	DPI Timing Generator Vertical Front/Back Porch Control Register (Right Frame, Odd Field)
1401E078	DPI_TGEN_VWIDTH_REVEN	32	DPI Timing Generator Vertical Sync Pulse Width Control Register (Right Frame, Even Field)
1401E07C	DPI_TGEN_VPORCH_REVEN	32	DPI Timing Generator Vertical Front/Back Porch Control Register (Right Frame, Even Field)
1401E080	DPI_ESAV_VTIM_LODD	32	EAV/SAV V Timing Control Register (Left ODD Frame)
1401E084	DPI_ESAV_VTIM_LEVEN	32	EAV/SAV V Timing Control Register (Left EVEN Frame)
1401E088	DPI_ESAV_VTIM_RODD	32	EAV/SAV V Timing Control Register (Right ODD Frame)
1401E08C	DPI_ESAV_VTIM_REVEN	32	EAV/SAV V Timing Control Register (Right EVEN Frame)

Address	Name	Width	Register Function
1401E090	DPI_ESAV_FTIM	32	EAV/SAV F Timing Control Register
1401E094	DPI_CLPF_SETTING	32	Chroma Low-Pass Filter Setting Register
1401E098	DPI_Y_LIMIT	32	Y (G) Channel Limit Setting Register
1401E09C	DPI_C_LIMIT	32	C (R, B) Channel Limit Setting Register
1401E0A0	DPI_YUV422_SETTING	32	YUV444 To YUV422 Transform Setting Register
1401E0A4	DPI_EMBSYNC_SETTING	32	Embedded Sync Setting Register
1401E0A8	DPI_ESAV_CODE_SET0	32	
1401E0AC	DPI_ESAV_CODE_SET1	32	
1401E0B0	DPI_BLANK_CODE_SET	32	
1401E0B4	DPI_MATRIX_SET	32	
1401E0B8	DPI_MATRIX_COEF_00	32	
1401E0BC	DPI_MATRIX_COEF_02	32	
1401E0C0	DPI_MATRIX_COEF_11	32	
1401E0C4	DPI_MATRIX_COEF_20	32	
1401E0C8	DPI_MATRIX_COEF_22	32	
1401E0CC	DPI_MATRIX_IN_OFFSET_0	32	
1401E0D0	DPI_MATRIX_IN_OFFSET_2	32	
1401E0D4	DPI_MATRIX_OUT_OFFSET_0	32	
1401E0D8	DPI_MATRIX_OUT_OFFSET_2	32	
1401E0E0	DPI_MUTEX_VSYNC_SETTING	32	
1401E0E4	DPI_SHEUDO_REG_UPDATE	32	Sheudo Register Update Time Register
1401E0E8	DPI_INTERNAL_CG_CON	32	Internal Clock Gated Configuration
1401EF00	DPI_PATTERN	32	DPI Internal Pattern Register

1401E000 DPI_EN — DPI Enable Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**EN**	EN	**Turns on/off DPI controller** 0: DPI controller off 1: DPI controller on

1401E004 DPI_RST **DPI Software Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**RST**
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**RST**	RST	**Resets DPI controller or not** 0: Release DPI reset 1: Assert DPI reset

1401E008 DPI_INTEN **DPI IRQ Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**INT_UNDERFLOW_EN**	**INT_VDE_EN**	**INT_VSYNC_EN**
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	**INT_UNDERFLOW_EN**	INT_UNDERFLOW_EN	**If FIFO is underflow, an interrupt request will be generated.** 0: Disable 1: Enable
1	**INT_VDE_EN**	INT_VDE_EN	**If VDE is activated, an interrupt request will be generated.** 0: Disable 1: Enable
0	**INT_VSYNC_EN**	INT_VSYNC_EN	**If VSYNC is activated, an interrupt request will be generated.** 0: Disable 1: Enable

1401E00C DPI_INTSTA **DPI IRQ Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INTSTA_UNDERFLOW	INTSTA_VDE_EN	INTSTA_VSYNC_EN
Type														A1	A1	A1
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	**INTSTA_UNDERFLOW**	INTSTA_UNDERFLOW	**If FIFO is underflow, an interrupt request will be generated.** SW can only write 0 to clear the interrupt. Writing 1 is ineffective.
1	**INTSTA_VDE_EN**	INTSTA_VDE_EN	**If VDE falling edge, an interrupt request will be generated.** SW can only write 0 to clear the interrupt. Writing 1 is ineffective.
0	**INTSTA_VSYNC_EN**	INTSTA_VSYNC_EN	**If VSYNC is activated, an interrupt request will be generated.** SW can only write 0 to clear the interrupt. Writing 1 is ineffective.

1401E010 DPI_CON **DPI Control Register** **00030000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FAKE_DE_REVEN	FAKE_DE_RODD	FAKE_DE_LEVEN	FAKE_DE_LODD	VS_REVEN_EN	VS_RODD_EN	VS_LEVEN_EN	VS_LODD_EN
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIXREP							EMBSYNC_EN		MATRIX_EN	YUV422_EN	CLPF_EN	TDFP_EN	INTL_EN	IN_RB_SWAP	BG_ENABLE
Type	RW							RW		RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0				0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23	**FAKE_DE_REVEN**	FAKE_DE_REVEN	**Fake DE for REVEN frame**
22	**FAKE_DE_RODD**	FAKE_DE_RODD	**Fake DE for RODD frame**
21	**FAKE_DE_LEVEN**	FAKE_DE_LEVEN	**Fake DE for LEVEN frame**
20	**FAKE_DE_LODD**	FAKE_DE_LODD	**Fake DE for LODD frame**
19	**VS_REVEN_EN**	VS_REVEN_EN	**VS_EN for REVEN frame**
18	**VS_RODD_EN**	VS_RODD_EN	**VS_EN for RODD frame**
17	**VS_LEVEN_EN**	VS_LEVEN_EN	**VS_EN for LEVEN frame**
16	**VS_LODD_EN**	VS_LODD_EN	**VS_EN for LODD frame**
15:12	**PIXREP**	PIXREP	
8	**EMBSYNC_EN**	EMBSYNC_EN	**Enables embeded sync**
6	**MATRIX_EN**	MATRIX_EN	**Enables color space conversion**
5	**YUV422_EN**	YUV422_EN	**Enables YUV444-to-422**
4	**CLPF_EN**	CLPF_EN	**Enables chroma low pass filter**
3	**TDFP_EN**	TDFP_EN	**Enables 3D frame packet**

Bit(s)	Mnemonic	Name	Description
			0: Disable 3D frame packing 1: Enable 3D frame packing
2	**INTL_EN**	INTL_EN	**Enables interlace** 0: Progressive mode 1: Interlace mode
1	**IN_RB_SWAP**	IN_RB_SWAP	**Swaps input RB channel** 0: RGB 1: BGR
0	**BG_ENABLE**	BG_ENABLE	**Enables frame** 0: No background frame 1: Background frame

1401E014 DPI_OUTPUT_SETTING **DPI Output Stage Setting Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										YC_MAP			OUT_BIT		EDGE_SEL	DPI_OEN_OFF
Type										RW			RW		RW	RW
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CK_POL	VSYNC_POL	HSYNC_POL	DE_POL		VS_MASK	HS_MASK	DE_MASK		R_MASK	G_MASK	B_MASK	BIT_SWAP	CH_SWAP		
Type	RW	RW	RW	RW		RW	RW	RW		RW	RW	RW	RW	RW		
Reset	0	0	0	0		0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
22:20	**YC_MAP**	YC_MAP	**YUV422 bit mapping** 0XX: {R[7:4],G[7:4],B[7:4]} (or {Cr[7:4],Y[7:4],Cb[7:4]}) 100: {C[11:4],Y[11:4],C[3:0],Y[3:0]} 101: {Y[11:4],C[11:4],Y[3:0],C[3:0]} 110: {C[11:0],Y[11:0]} 111: {Y[11:0],C[11:0]}
19:18	**OUT_BIT**	OUT_BIT	**Output bit number** 00: 8 bits 01: 10 bits 10: 12 bits 11: 12 bits
17	**DUAL_EDGE_SEL**	EDGE_SEL	**Selects output dual edge** 0: First edge: {R[7:0], G[7:4]} Second edge: {G[3:0], B[7:0]} 1: First edge: {G[3:0], B[7:0]} Second edge: {R[7:0], G[7:4]}
16	**DPI_OEN_OFF**	DPI_OEN_OFF	**Turns off DPI output enabling** 0: Does not turn off 1: Turn off
15	**DPI_CK_POL**	CK_POL	
14	**VSYNC_POL**	VSYNC_POL	**Vsync polarity** 0: Negative 1: Positive
13	**HSYNC_POL**	HSYNC_POL	**Hsync polarity** 0: Negative

Bit(s)	Mnemonic	Name	Description
			1: Positive
12	**DE_POL**	DE_POL	**Data enabling polarity** 0: Positive 1: Negative
10	**VS_MASK**	VS_MASK	**Controls Vsync mask** 0: Enable Vsync 1: Mask Vsync
9	**HS_MASK**	HS_MASK	**Controls Hsync mask** 0: Enable Hsync 1: Mask Hsync
8	**DE_MASK**	DE_MASK	**Controls DE mask** 0: Enable DE 1: Mask DE
6	**R_MASK**	R_MASK	**Controls R channel mask** 0: Enable R channel 1: Mask R channel
5	**G_MASK**	G_MASK	**Controls G channel mask** 0: Enable G channel 1: Mask G channel
4	**B_MASK**	B_MASK	**Controls B channel mask** 0: Enable B channel 1: Mask B channel
3	**OUT_BIT_SWAP**	BIT_SWAP	**Inverts output bit order**
2:0	**OUT_CH_SWAP**	CH_SWAP	**Swaps output channel** 000: RGB 001: GBR 010: BRG 011: RBG 100: GRB 101: BGR

1401E018 DPI_SIZE **DPI Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				HSIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**VSIZE**	VSIZE	DPI vertical size
12:0	**HSIZE**	HSIZE	DPI horizontal size

1401E01C DPI_DDR_SETTING **DPI DDR Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DDR_PAD_MODE			DDR_WIDTH		DATA_THROT	DDR_4PHASE	DDR_SEL	DDR_EN
Type								RW			RW		RW	RW	RW	RW
Reset								0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8	**DDR_PAD_MODE**	DDR_PAD_MODE	**DPI dual edge padding mode** 0: Padding by MSB 1: Padding by 0's
5:4	**DDR_WIDTH**	DDR_WIDTH	**DPI dual edge output width** 0: RGB888 DDR (12 bits) 1: RGB101010 DDR (15 bits) 2: RGB121212 DDR (18 bits) 3: RGB161616 DDR (24 bits)
3	**DATA_THROT**	DATA_THROT	
2	**DDR_4PHASE**	DDR_4PHASE	**DPI dual edge central align clock**
1	**DDR_SEL**	DDR_SEL	**Selects DPI dual edge output**
0	**DDR_EN**	DDR_EN	**Enables DPI dual edge**

1401E020 DPI_TGEN_HWIDTH — DPI Timing Generator Horizontal Sync Pulse Width Control Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					HPW											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0	**HPW**	HPW	**Horizontal sync pulse width** Unit: Pixel. Must be > 0.

1401E024 DPI_TGEN_HPORCH — DPI Timing Generator Horizontal Front/Back Porch Control Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					HFP											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					HBP											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**HFP**	HFP	**Horizontal front porch width** Unit: Pixel. Must be > 0.
11:0	**HBP**	HBP	**Horizontal back porch width** Unit: Pixel. Must be > 0.

1401E028 DPI_TGEN_VWIDTH — **DPI Timing Generator Vertical Sync Pulse Width Control Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																VPW_HALF
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					VPW											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**VPW_HALF**	VPW_HALF	**Controls vertical sync pulse width (left frame, even field)** 0: VS puls width aligned to HS puls 1: VS puls width shifts 0.5 lines.
11:0	**VPW**	VPW	**Vertical sync pulse width (left frame, odd field)** Unit: Line. Must be > 0.

1401E02C DPI_TGEN_VPORCH — **DPI Timing Generator Vertical Front/Back Porch Control Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VFP											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					VBP											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**VFP**	VFP	**Vertical front porch width (left frame, odd field)** Unit: Line. Must be > 0.
11:0	**VBP**	VBP	**Vertical back porch width (left frame, odd field)** Unit: Line. Must be > 0.

1401E030 DPI_BG_HCNTL — **DPI Background Horizontal Control Register** — **00010001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				BG_LEFT												

Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				BG_RIGHT												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
28:16	**BG_LEFT**	BG_LEFT	DPI frame boundary left
12:0	**BG_RIGHT**	BG_RIGHT	DPI frame boundary right

1401E034 DPI_BG_VCNTL **DPI Background Vertical Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				BG_TOP												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				BG_BOT												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**BG_TOP**	BG_TOP	DPI frame boundary top
12:0	**BG_BOT**	BG_BOT	DPI frame boundary bottom

1401E038 DPI_BG_COLOR **DPI Background Color Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BG_R							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BG_G								BG_B							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:16	**BG_R**	BG_R	DPI background color R
15:8	**BG_G**	BG_G	DPI background color G
7:0	**BG_B**	BG_B	DPI background color B

1401E03C DPI_FIFO_CTL **DPI FIFO CTL** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								FIFO_RST_SEL				FIFO_VALID_SET				
Type								RW				RW				
Reset								0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8	**FIFO_RST_SEL**	FIFO_RST_SEL	DPI FIFO control
4:0	**FIFO_VALID_SET**	FIFO_VALID_SET	DPI FIFO control

1401E040 DPI_STATUS DPI Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											TDLR	FIELD			OUTEN	DPI_BUSY
Type											RU	RU			RU	RU
Reset											0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				V_COUNTER												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21	**TDLR**	TDLR	3DLR signal
20	**FIELD**	FIELD	Field signal
17	**OUTEN**	OUTEN	Output pad of DPI signals is enabled to output.
16	**DPI_BUSY**	DPI_BUSY	DPI is busy.
12:0	**V_COUNTER**	V_COUNTER	Line counter

1401E044 DPI_TMODE DPI Test Mode Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DPI_OEN_ON
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**DPI_OEN_ON**	DPI_OEN_ON	**Turns on DPI output enable** Only takes effect when DPI_OEN_OFF = 0.

1401E048 DPI_CHKSUM DPI Checksum Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DPI_CHKSUM_EN	DPI_CHKSUM_READY							DPI_CHKSUM							
Type	WO	RU							RU							
Reset	0	0							0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DPI_CHKSUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**DPI_CHKSUM_EN**	DPI_CHKSUM_EN	**Enables DPI checksum** 0: Disable 1: Enable
30	**DPI_CHKSUM_RDY**	DPI_CHKSUM_READY	**DPI checksum ready**
23:0	**DPI_CHKSUM**	DPI_CHKSUM	**DPI checksum**

1401E04C DPI_DCM DPI DCM Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																PIXELPLL_CK_DCM_EN
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**PIXELPLL_CK_DCM_EN**	PIXELPLL_CK_DCM_EN	**Enables pixelpll_ck_dcm** 0: Disable 1: Enable

1401E050 DPI_DUMMY 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DPI_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DPI_DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DPI_DUMMY**	DPI_DUMMY	

Bit(s)	Mnemonic	Name	Description

1401E054 DPI_GPIO_MODE — **DPI Output Control Signal Has Two GPIO Output Select** — **00000003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**DPI_GPIO_EN**	
Type															RW	
Reset															1	1

Bit(s)	Mnemonic	Name	Description
1:0	**DPI_GPIO_EN**	DPI_GPIO_EN	**Enables 1st or 2nd group of DPI GPIO** 2'b11: Enable both 1st and 2nd DPI GPIO output 2'b10: Enable 2nd group of DPI GPIO output 2'b01: Enable 1st group of DPI GPIO output 2'b00: Disable

1401E068 DPI_TGEN_VWIDTH_LEVEN — **DPI Timing Generator Vertical Sync Pulse Width Control Register (Left Frame, Even Field)** — **00010000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**VPW_HALF_LEVEN**
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**VPW_LEVEN**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**VPW_HALF_LEVEN**	VPW_HALF_LEVEN	**Controls vertical sync pulse width (left frame, even field)** 0: LEVEN VS puls width aligned to HS puls 1: LEVEN VS puls width shifts 0.5 lines.
11:0	**VPW_LEVEN**	VPW_LEVEN	**Vertical sync pulse width (left frame, even field)** Unit: Line. Must be > 0.

1401E06C DPI_TGEN_VPORCH_LEVEN — **DPI Timing Generator Vertical Front/Back Porch Control Register (Left Frame, Even** — **00000000**

Field)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VFP_LEVEN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					VBP_LEVEN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**VFP_LEVEN**	VFP_LEVEN	**Vertical front porch width (left frame, even field)** Unit: Line. Must be > 0.
11:0	**VBP_LEVEN**	VBP_LEVEN	**Vertical back porch width (left frame, even field)** Unit: Line. Must be > 0.

1401E070 DPI_TGEN_V_WIDTH_RODD — **DPI Timing Generator Vertical Sync Pulse Width Control Register (Right Frame, Odd Field)** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																VPW_HALF_RODD
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					VPW_RODD											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**VPW_HALF_RODD**	VPW_HALF_RODD	**Controls vertical sync pulse width (right frame, odd field)** 0: RODD VS puls width aligned to HS puls 1: RODD VS puls width shifts 0.5 lines.
11:0	**VPW_RODD**	VPW_RODD	**Vertical sync pulse width (right frame, odd field)** Unit: Line. Must be > 0.

1401E074 DPI_TGEN_V_PORCH_RODD — **DPI Timing Generator Vertical Front/Back Porch Control Register (Right Frame, Odd Field)** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VFP_RODD											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					VBP_RODD											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**VFP_RODD**	VFP_RODD	**Vertical front porch width (right frame, odd field)** Unit: Line. Must be > 0.
11:0	**VBP_RODD**	VBP_RODD	**Vertical back porch width (right frame, odd field)** Unit: Line. Must be > 0.

1401E078 DPI_TGEN_VWIDTH_REVEN — DPI Timing Generator Vertical Sync Pulse Width Control Register (Right Frame, Even Field) — 00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																VPW_HALF_REVEN
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					VPW_REVEN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**VPW_HALF_REVEN**	VPW_HALF_REVEN	**Controls vertical sync pulse width (right frame, even field)** 0: REVEN VS puls width aligned to HS puls 1: REVEN VS puls width shifts 0.5 lines.
11:0	**VPW_REVEN**	VPW_REVEN	**Vertical sync pulse width (right frame, even field)** Unit: Line. Must be > 0.

1401E07C DPI_TGEN_VPORCH_REVEN — DPI Timing Generator Vertical Front/Back Porch Control Register (Right Frame, Even Field) — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VFP_REVEN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					VBP_REVEN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**VFP_REVEN**	VFP_REVEN	**Vertical front porch width (right frame, even field)** Unit: Line. Must be > 0.
11:0	**VBP_REVEN**	VBP_REVEN	**Vertical back porch width (right frame, even field)** Unit: Line. Must be > 0.

1401E080 DPI_ESAV_VTIM_LODD **EAV/SAV V Timing Control Register (Left ODD Frame)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					ESAV_VWID_LODD											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ESAV_VOFST_LODD											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**ESAV_VWID_LODD**	ESAV_VWID_LODD	**EAV/SAV V width (left frame, odd field)** Unit: Line
11:0	**ESAV_VOFST_LODD**	ESAV_VOFST_LOD D	**Enables EAV/SAV V offset from the end of data (left frame, odd field)** Unit: Line

1401E084 DPI_ESAV_VTIM_LEVEN **EAV/SAV V Timing Control Register (Left EVEN Frame)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					ESAV_VWID_LEVEN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ESAV_VOFST_LEVEN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**ESAV_VWID_LEVEN**	ESAV_VWID_LEVE N	**EAV/SAV V width (left frame, even field)** Unit: Line
11:0	**ESAV_VOFST_LEVEN**	ESAV_VOFST_LEV EN	**Enables EAV/SAV V offset from the end of data (left frame, even field)** Unit: Line

1401E088 DPI_ESAV_VTIM_RODD **EAV/SAV V Timing Control Register (Right ODD Frame)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					ESAV_VWID_RODD											
Type					RW											

Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ESAV_VOFST_RODD											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**ESAV_VWID_RODD**	ESAV_VWID_RODD	**EAV/SAV V width (right frame, odd field)** Unit: Line
11:0	**ESAV_VOFST_RODD**	ESAV_VOFST_ROD D	**Enables EAV/SAV V offset from the end of data (right frame, odd field)** Unit: Line

1401E08C DPI_ESAV_VTIM_REVEN **EAV/SAV V Timing Control Register (Right EVEN Frame)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					ESAV_VWID_REVEN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ESAV_VOFST_REVEN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**ESAV_VWID_REVEN**	ESAV_VWID_REVE N	**EAV/SAV V width (right frame, even field)** Unit: Line
11:0	**ESAV_VOFST_REVEN**	ESAV_VOFST_REV EN	**Enables EAV/SAV V offset from the end of data (right frame, even field)** Unit: Line

1401E090 DPI_ESAV_FTIM **EAV/SAV F Timing Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					ESAV_FOFST_EVEN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ESAV_FOFST_ODD											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**ESAV_FOFST_EVEN**	ESAV_FOFST_EVE N	**Enables EAV/SAV F offset from the end of data (even field)** Unit: Line
11:0	**ESAV_FOFST_ODD**	ESAV_FOFST_ODD	**Enables EAV/SAV F offset from the end of data (odd field)** Unit: Line

1401E094 DPI_CLPF_SETTING Chroma Low-Pass Filter Setting Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												ROUND_EN			CLPF_TYPE	
Type												RW			RW	
Reset												0			0	0

Bit(s)	Mnemonic	Name	Description
4	**ROUND_EN**	ROUND_EN	**Enables chroma LPF output rounding** 0: Disable rounding 1: Enable rounding
1:0	**CLPF_TYPE**	CLPF_TYPE	**Chroma LPF type** 00: out = 1/2*(in + in_d1) 01: out = 1/2*(in_d1 + in_d2) 10: out = 1/4*(in + 2*in_d1 + in_d2) 11: out = 1/4*(in + 2*in_d1 + in_d2)

1401E098 DPI_Y_LIMIT Y (G) Channel Limit Setting Register 0FFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					Y_LIMIT_TOP											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					Y_LIMIT_BOT											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**Y_LIMIT_TOP**	Y_LIMIT_TOP	Y (G) chnnel value top limit
11:0	**Y_LIMIT_BOT**	Y_LIMIT_BOT	Y (G) chnnel value bottom limit

1401E09C DPI_C_LIMIT C (R, B) Channel Limit Setting Register 0FFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					C_LIMIT_TOP											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					C_LIMIT_BOT											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**C_LIMIT_TOP**	C_LIMIT_TOP	C (R,B) chnnel value top limit
11:0	**C_LIMIT_BOT**	C_LIMIT_BOT	C (R,B) chnnel value bottom limit

1401E0A0 DPI_YUV422_SETTING YUV444 To YUV422 Transform Setting Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DE_DELSEL	Y_DELSEL	CB_DELSEL	CR_DELSEL				UV_SWAP
Type									RW	RW	RW	RW				RW
Reset									0	0	0	0				0

Bit(s)	Mnemonic	Name	Description
7	**DE_DELSEL**	DE_DELSEL	**Selects data enable and control signal deley** 0: Delay 0T 1: Delay 1T
6	**Y_DELSEL**	Y_DELSEL	**Selects Y channel delay** 0: Delay 0T 1: Delay 1T
5	**CB_DELSEL**	CB_DELSEL	**Selects Cb channel delay** 0: Delay 0T 1: Delay 1T
4	**CR_DELSEL**	CR_DELSEL	**Selects Cr channel delay** 0: Delay 0T 1: Delay 1T
0	**UV_SWAP**	UV_SWAP	**Swaps Cb, Cr channel** 0: CbCr 1: CrCb

1401E0A4 DPI_EMBSYNC_SETTING Embedded Sync Setting Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																EMBSYNC_OPT
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		VS_OUT_SEL						ESAV_CODE_MAN		ESAV_H_INV	ESAV_V_INV	ESAV_F_INV		EMBSYNC_B_CB_EN	EMBSYNC_G_Y_EN	EMBSYNC_R_CR_EN
Type		RW						RW		RW	RW	RW		RW	RW	RW
Reset		0	0	0				0		0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
16	**EMBSYNC_OPT**	EMBSYNC_OPT	
14:12	**VS_OSEL**	VS_OUT_SEL	**Selects vsync output** 000: Vsync of timing generator 100: ESAV_V 101: ESAV_F 110: Hsync aligned ESAV_V 111: Hsync aligned ESAV_F
8	**ESAV_CODE_MAN**	ESAV_CODE_MAN	**EAV/SAV code definition** 0: Use default EAV/SAV definition 1: Use manual code defined by 0xA0~0xA4
6	**ESAV_H_INV**	ESAV_H_INV	**Inverts H bit**
5	**ESAV_V_INV**	ESAV_V_INV	**Inverts V bit**
4	**ESAV_F_INV**	ESAV_F_INV	**Inverts F bit**
2	**EMBSYNC_B_CB_EN**	EMBSYNC_B_CB_EN	**Embedded sync in Cb (B) channel**
1	**EMBSYNC_G_Y_EN**	EMBSYNC_G_Y_EN	**Embedded sync in Y (G) channel**
0	**EMBSYNC_R_CR_EN**	EMBSYNC_R_CR_EN	**Embedded sync in Cr (R) channel**

1401E0A8 DPI_ESAV_CODE_SET0 **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					ESAV_CODE1											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ESAV_CODE0											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:16	**ESAV_CODE1**	ESAV_CODE1	EAV/SAV manual code 1
11:0	**ESAV_CODE0**	ESAV_CODE0	EAV/SAV manual code 0

1401E0AC DPI_ESAV_CODE_SET1 **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																ESAV_CODE3_MSB
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ESAV_CODE2											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**ESAV_CODE3_MSB**	ESAV_CODE3_MSB	EAV/SAV manual code 3 (bit 7)

Bit(s)	Mnemonic	Name	Description
11:0	**ESAV_CODE2**	ESAV_CODE2	EAV/SAV manual code 2

1401E0B0 DPI_BLANK_CODE_SET **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							BLANK_PAD_OPT	BLANK_CODE_EN	BLANK_B							
Type							RW	RW	RW							
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLANK_G								BLANK_R							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25	**BLANK_PAD_OPT**	BLANK_PAD_OPT	
24	**BLANK_CODE_EN**	BLANK_CODE_EN	
23:16	**BLANK_B**	BLANK_B	
15:8	**BLANK_G**	BLANK_G	
7:0	**BLANK_R**	BLANK_R	

1401E0B4 DPI_MATRIX_SET **00000203**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				EXT_MATRIX_EN			MATRIX_BIT					INT_MATRIX_SEL				
Type				RW			RW					RW				
Reset				0			1	0				0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
12	**EXT_MATRIX_EN**	EXT_MATRIX_EN	
9:8	**MATRIX_BIT**	MATRIX_BIT	
4:0	**INT_MATRIX_SEL**	INT_MATRIX_SEL	**Selects internal matrix coefficients** 0: RGB_TO_JPEG 1: RGB_TO_FULL709 2: RGB_TO_BT601 3: RGB_TO_BT709 4: JPEG_TO_RGB 5: FULL709_TO_RGB 6: BT601_TO_RGB 7: BT709_TO_RGB 8: JPEG_TO_BT601

Bit(s)	Mnemonic	Name	Description
			9: JPEG_TO_BT709 10: BT601_TO_JPEG 11: BT709_TO_JPEG 12:BT709_TO_BT601 13: BT601_TO_BT709 20: JPEG_TO_CERGB 21: FULL709_TO_CERGB 22: BT601_TO_CERGB 23: BT709_TO_CERGB 28: RGB_TO_CERGB Default: Bypass

1401E0B8 DPI_MATRIX_COEF_00 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MATRIX_COEF_01												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MATRIX_COEF_00												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	MATRIX_COEF_01	MATRIX_COEF_01	Color matrix coefficient 01
12:0	MATRIX_COEF_00	MATRIX_COEF_00	Color matrix coefficient 00

1401E0BC DPI_MATRIX_COEF_02 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MATRIX_COEF_10												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MATRIX_COEF_02												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	MATRIX_COEF_10	MATRIX_COEF_10	Color matrix coefficient 10
12:0	MATRIX_COEF_02	MATRIX_COEF_02	Color matrix coefficient 02

1401E0C0 DPI_MATRIX_COEF_11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MATRIX_COEF_12												

Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MATRIX_COEF_11												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**MATRIX_COEF_12**	MATRIX_COEF_12	Color matrix coefficient 12
12:0	**MATRIX_COEF_11**	MATRIX_COEF_11	Color matrix coefficient 11

1401E0C4 DPI_MATRIX_COEF_20 **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MATRIX_COEF_21												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MATRIX_COEF_20												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:16	**MATRIX_COEF_21**	MATRIX_COEF_21	Color matrix coefficient 21
12:0	**MATRIX_COEF_20**	MATRIX_COEF_20	Color matrix coefficient 20

1401E0C8 DPI_MATRIX_COEF_22 **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MATRIX_COEF_22												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0	**MATRIX_COEF_22**	MATRIX_COEF_22	Color matrix coefficient 22

1401E0CC DPI_MATRIX_IN_OFFSET_0 **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								MATRIX_IN _OFFSET_1								
Type								RW								

Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MATRIX_IN_OFFSET_0								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16	**MATRIX_IN_OFFSET_1**	MATRIX_IN_OFFSET_1	Color matrix input offset 1
8:0	**MATRIX_IN_OFFSET_0**	MATRIX_IN_OFFSET_0	Color matrix input offset 0

1401E0D0 DPI_MATRIX_IN_OFFSET_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MATRIX_IN_OFFSET_2								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0	**MATRIX_IN_OFFSET_2**	MATRIX_IN_OFFSET_2	Color matrix input offset 2

1401E0D4 DPI_MATRIX_OUT_OFFSET_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								MATRIX_OU T_OFFSET_ 1								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MATRIX_OUT_OFFSET_0								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:16	**MATRIX_IN_OFFSET_1**	MATRIX_OUT_OFFSET_1	Color matrix output offset 1
8:0	**MATRIX_IN_OFFSET_0**	MATRIX_OUT_OFFSET_0	Color matrix output offset 0

1401E0D8 DPI_MATRIX 00000000

_OUT_OFFSET_2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MATRIX_OUT_OFFSET_2								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0	**MATRIX_IN_OFFSET_2**	MATRIX_OUT_OFFSET_2	Color matrix output offset 2

1401E0E0 DPI_MUTEX_VSYNC_SETTING **00000010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MUTEX_VSYNC_SEL															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					MUTEX_VSYNC_DELAY_LINE_NUM											
Type					RW											
Reset					0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**DPI_MUTEX_VSYNC_SEL**	MUTEX_VSYNC_SEL	**Selects MUTEX_VSYNC** 0: Original vsync 1: Delayed vsync
11:0	**DPI_MUTEX_VSYNC_DELAY_LINE_NUM**	MUTEX_VSYNC_DELAY_LINE_NUM	**MUTEX_VSYNC_DELAY_LINE_NUM**

1401E0E4 DPI_SHEUDO_REG_UPDATE **Sheudo Register Update Time Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								SHEUDO_REG_UPDATE_SEL								
Type								RW								
Reset								0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
8:0	**DPI_PSEUDO_REG_UPDATE_SEL**	SHEUDO_REG_UPDATE_SEL	**PSEUDO_REG_UPDATE_SEL** 000_000_001: hfp&vfp 000_000_010: hpw&vfp 000_000_100: hbp&vfp 000_001_000: hfp&vpw 000_010_000: hpw&vpw 000_100_000: hbp&vpw 001_000_000: hfp&vbp 010_000_000: hpw&vbp 100_000_000: hbp&vbp

1401E0E8 DPI_INTERNAL_CG_CON **Internal Clock Gated Configuration** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									PAT_CG_EN	CHKSUM_CG_EN	YUV422_CG_EN	ASYNC_FIFO_BCLK_CG_EN	REG_CG_EN	CLPF_CG_EN	MATRIX_CG_EN	EMBSYNC_CG_EN
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7		PAT_CG_EN	**PAT_CG_EN** 0: Internal CG gated 1: Disable internal CG gated
6	**DPI_CHKSUM_CG_EN**	CHKSUM_CG_EN	**CHKSUM_CG_EN** 0: Internal CG gated 1: Disable internal CG gated
5	**DPI_YUV422_CG_EN**	YUV422_CG_EN	**YUV422_CG_EN** 0: Internal CG gated 1: Disable internal CG gated
4	**DPI_ASYNC_FIFO_BCLK_CG_EN**	ASYNC_FIFO_BCLK_CG_EN	**ASYNC_FIFO_BCLK_CG_EN** 0: Internal CG gated 1: Disable internal CG gated
3	**DPI_REG_CG_EN**	REG_CG_EN	**REG_CG_EN** 0: Internal CG gated 1: Disable internal CG gated
2	**DPI_CLPF_CG_EN**	CLPF_CG_EN	**CLPF_CG_EN** 0: Internal CG gated 1: Disable internal CG gated
1	**DPI_MATRIX_CG_EN**	MATRIX_CG_EN	**MATRIX_CG_EN** 0: Internal CG gated 1: Disable internal CG gated
0	**DPI_EMBSYNC_CG_EN**	EMBSYNC_CG_EN	**EMBSYNC_CG_EN** 0: Internal CG gated 1: Disable internal CG gated

1401EF00 DPI_PATTERN **DPI Internal Pattern Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PAT_R_MAN								PAT_G_MAN							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAT_B_MAN									PAT_SEL						PAT_EN
Type	RW									RW						RW
Reset	0	0	0	0	0	0	0	0		0	0	0				0

Bit(s)	Mnemonic	Name	Description
31:24	**DPI_PAT_B**	PAT_R_MAN	**User defined color (red)**
23:16	**DPI_PAT_G**	PAT_G_MAN	**User defined color (green)**
15:8	**DPI_PAT_R**	PAT_B_MAN	**User defined color (blue)**
6:4	**DPI_PAT_SEL**	PAT_SEL	**Selects internal pattern** 000: 256 vertical gray 001: 64 vertical gray 010: 256 horizontal gray 011: 64 horizontal gray 100: Color bar 101: User defined color 110: Frame border 111: Dot morei
0	**PAT_EN**	PAT_EN	**Enables internal pattern**

4.4 Display Serial Interface

Module name: DISP_DSI0 Base address: (+1401c000h)

Address	Name	Width	Register Function
1401C000	DSI_START	32	DSI Start Register
1401C004	DSI_STATUS	32	DSI Status Register
1401C008	DSI_INTEN	32	DSI Interrupt Enable Register
1401C00C	DSI_INTSTA	32	DSI Interrupt Status Register
1401C010	DSI_COM_CON	32	DSI Common Control Register
1401C014	DSI_MODE_CON	32	DSI Mode Control Register
1401C018	DSI_TXRX_CON	32	DSI TX RX Control Register
1401C01C	DSI_PSCON	32	DSI Pixel Stream Control Register
1401C020	DSI_VSA_NL	32	DSI Vertical Sync Active Register
1401C024	DSI_VBP_NL	32	DSI Vertical Back Porch Register
1401C028	DSI_VFP_NL	32	DSI Vertical Front Porch Register
1401C02C	DSI_VACT_NL	32	DSI Vertical Active Register
1401C030	DSI_LFR_CON	32	DSI Low Frame Rate Control Register
1401C034	DSI_LFR_STA	32	DSI Low Frame Rate Status Register
1401C050	DSI_HSA_WC	32	DSI Horizontal Sync Active Word Count Register
1401C054	DSI_HBP_WC	32	DSI Horizontal Back Porch Word Count Register
1401C058	DSI_HFP_WC	32	DSI Horizontal Front Porch Word Count Register
1401C05C	DSI_BLLP_WC	32	DSI Horizontal Blanking or Low Power Mode Word Count Register
1401C060	DSI_CMDQ_CON	32	DSI Command Queue Control Register
1401C064	DSI_HSTX_CKLP_WC	32	DSI HSTX Clock Low-power Mode Word Count Register
1401C068	DSI_HSTX_CKLP_WC_AUTO_RESULT	32	DSI HSTX Clock Low-power Mode Automatic Calculation result
1401C074	DSI_RX_DATA03	32	DSI Receive Packet Data Byte 0 ~ 3 Register
1401C078	DSI_RX_DATA47	32	DSI Receive Packet Data Byte 4 ~ 7 Register
1401C07C	DSI_RX_DATA8B	32	DSI Receive Packet Data Byte 8 ~ 11 Register
1401C080	DSI_RX_DATAC	32	DSI Receive Packet Data Byte 12 ~ 15 Register
1401C084	DSI_RX_RACK	32	DSI Read Data Acknowledge Register
1401C088	DSI_RX_TRIG_ST A	32	DSI Receiver Status Register
1401C090	DSI_MEM_CONTI	32	DSI Memory Continue Command Register
1401C094	DSI_FRM_BC	32	DSI Frame Byte Count Register
1401C098	DSI_V3D_CON	32	DSI Vsync 3D Control Register
1401C0A0	DSI_TIME_CON0	32	DSI Timing Control 0 Register
1401C0A4	DSI_TIME_CON1	32	DSI Timing Control 1 Register
1401C100	DSI_PHY_LCPAT	32	DSI PHY Lane Clock Pattern Register
1401C104	DSI_PHY_LCCON	32	DSI PHY Lane Clock Control Register
1401C108	DSI_PHY_LD0CON	32	DSI PHY Lane 0 Control Register
1401C10C	DSI_PHY_SYNCON	32	DSI PHY Sync Control Register
1401C110	DSI_PHY_TIMCON 0	32	DSI PHY Timing Control 0 Register
1401C114	DSI_PHY_TIMCON 1	32	DSI PHY Timing Control 1 Register
1401C118	DSI_PHY_TIMCON 2	32	DSI PHY Timing Control 2 Register
1401C11C	DSI_PHY_TIMCON 3	32	DSI PHY Timing Control 3 Register
1401C130	DSI_VM_CMD_CON	32	DSI Video Mode Command Packet Control Register

Address	Name	Width	Register Function
1401C134	DSI_VM_CMD_DATA0	32	DSI Video Mode Command Packet Data Byte 0~3 Register
1401C138	DSI_VM_CMD_DATA4	32	DSI Video Mode Command Packet Data Byte 4~7 Register
1401C13C	DSI_VM_CMD_DATA8	32	DSI Video Mode Command Packet Data Byte 8~11 Register
1401C140	DSI_VM_CMD_DATAC	32	DSI Video Mode Command Packet Data Byte 12~15 Register
1401C144	DSI_CKSM_OUT	32	DSI Checksum Output
1401C148	DSI_STATE_DBG0	32	DSI State Machine Debug 0
1401C14C	DSI_STATE_DBG1	32	DSI State Machine Debug 1
1401C150	DSI_STATE_DBG2	32	DSI State Machine Debug 2
1401C154	DSI_STATE_DBG3	32	DSI State Machine Debug 3
1401C158	DSI_STATE_DBG4	32	DSI State Machine Debug 4
1401C15C	DSI_STATE_DBG5	32	DSI State Machine Debug 5
1401C160	DSI_STATE_DBG6	32	DSI State Machine Debug 6
1401C164	DSI_STATE_DBG7	32	DSI State Machine Debug 7
1401C168	DSI_STATE_DBG8	32	DSI State Machine Debug 8
1401C16C	DSI_STATE_DBG9	32	DSI State Machine Debug 9
1401C170	DSI_DEBUG_SEL	32	DSI Debug Output Selection
1401C174	DSI_RESERVED	32	Reserved Register
1401C178	DSI_BIST_PATTERN	32	DSI Bist Pattern Register
1401C17C	DSI_BIST_CON	32	DSI Bist Control Register
1401C180	DSI_VM_CMD_DATA10	32	DSI Video Mode Command Packet Data Byte 16~19 Register
1401C184	DSI_VM_CMD_DATA14	32	DSI Video Mode Command Packet Data Byte 20~23 Register
1401C188	DSI_VM_CMD_DATA18	32	DSI Video Mode Command Packet Data Byte 24~27 Register
1401C18C	DSI_VM_CMD_DATA1C	32	DSI Video Mode Command Packet Data Byte 28~31 Register
1401C200~1401c3fc	DSI_CMDQ[n] (n=0~127)	32	DSI Command Queue

1401C000 DSI_START **DSI Start Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																VM_CMD_START
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												SKEWCAL_START		SLEEPOUT_START		DSI_START
Type												RW		RW		RW
Reset												0		0		0

Bit(s)	Name	Description

Bit(s)	Name	Description
16	VM_CMD_START	**Starts DSI VM command transmission** Set up this bit to start command transmission in video mode. This bit is only available when VM_CMD_EN = 1. 0: No effect 1: Start
4	SKEWCAL_START	**DSI skew calibration operation** Set this bit to start de-skew calibration process for RX. This bit is only available when DSI_BUSY = 0 0: No effect 1: Start
2	SLEEPOUT_START	**DSI sleep-out operation** Set up this bit to wake up DSI from ULPS mode. This bit is only available when SLEEP_MODE = 1. 0: No effect 1: Start
0	DSI_START	**Starts DSI controller operation** Set up this bit to start DSI control. 0: No effect 1: Start

1401C004 DSI_STATUS **DSI Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CONTENTION_ERR	FALSE_CTRL_ERR	ESC_SYNC_ERR	ESC_ENTRY_ERR			BUFFER_UNDERRUN	
Type									RU	RU	RU	RU			RU	
Reset									0	0	0	0			0	

Bit(s)	Name	Description
7	CONTENTION_ERR	**Contention error** This error indicates a contention error happened during transmission
6	FALSE_CTRL_ERR	**False control error** This error indicates a LP-Rqst is not followed by a valid escape or turnaround sequence, or a HS-Rqst is not correctly followed by a bridge state from RX
5	ESC_SYNC_ERR	**Escape mode sync error** This error indicates the last bit of a transmission does not match a byte boundary
4	ESC_ENTRY_ERR	**Escape mode entry error** This error indicates an invalid escape entry command from RX
1	BUFFER_UNDERRUN	**Buffer underrun error** This error indicates the DSI throughput exceeds data throughput and makes invalid data transmission

1401C008 DSI_INTEN **DSI Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SKEWCAL_DONE_INT_EN	VM_VFP_STR_INT_EN	VM_VACT_STR_INT_EN	VM_VBP_STR_INT_EN	TE_TIMEOUT_INT_EN	SLEEPOUT_DONE_INT_EN	VM_CMD_DONE_INT_EN	FRAME_DONE_INT_EN	VM_DONE_INT_EN	TE_RDY_INT_EN	CMD_DONE_INT_EN	LPRX_RD_RDY_INT_EN
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	SKEWCAL_DONE_INT_EN	**Skew-calibration done interrupt** This interrupt will be issued when skew-calibration process started by SKEWCAL_START is done 0: Disable 1: Enable
10	VM_VFP_STR_INT_EN	**Video mode VFP period start interrupt** This interrupt will be issued when VFP period start during video mode transmission 0: Disable 1: Enable
9	VM_VACT_STR_INT_EN	**Video mode VACT period start interrupt** This interrupt will be issued when VACT period start during video mode transmission 0: Disable 1: Enable
8	VM_VBP_STR_INT_EN	**Video mode VBP period start interrupt** This interrupt will be issued when VBP period start during video mode transmission 0: Disable 1: Enable
7	TE_TIMEOUT_INT_EN	**TE timeout interrupt** This interrupt will be issued when the wait time of TE signal exceeds SW-configured threshold 0: Disable 1: Enable
6	SLEEPOUT_DONE_INT_EN	**Enables ULPS sleep-out interrupt** The interrupt will be issued when ULPS sleep out procedure is completed 0: Disable 1: Enable
5	VM_CMD_DONE_INT_EN	**Enables DSI video mode command packet transmission interrupt** This interrupt will be issued when command packet transmission during video mode is completed 0: Disable 1: Enable
4	FRAME_DONE_INT_EN	**Frame done interrupt** This interrupt will be issued when the frame transmission is done, both for video and command mode 0: Disable 1: Enable
3	VM_DONE_INT_EN	**Enables DSI video mode finished interrupt** This interrupt will be issued when video mode transmission is finished 0: Disable 1: Enable
2	TE_RDY_INT_EN	**DSI TE ready interrupt**

Bit(s)	Name	Description
		This interrupt will be issued when either BTA TE or external TE is received 0: Disable 1: Enable
1	CMD_DONE_INT_EN	**Enables DSI command mode finished interrupt** This interrupt will be issued when all commands set in command queue are executed 0: Disable 1: Enable
0	LPRX_RD_RDY_INT_EN	**Enables RX data-ready interrupt** This interrupt will be issued when RX data are received through read commands. It is recommended to enable this interrupt to receive data because the read response may be overwritten if another read command exists. An RACK operation should be set after reading data to allow HW continue execution 0: Disable 1: Enable

1401C00C DSI_INTSTA DSI Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSI_BUSY															
Type	RU															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SKEWCAL_DONE_INT_FLAG	VM_VFP_STR_INT_FLAG	VM_VACT_STR_INT_FLAG	VM_VBP_STR_INT_FLAG	TE_TIMEOUT_INT_FLAG	SLEEPOUT_DONE_INT_FLAG	VM_CMD_DONE_INT_FLAG	FRAME_DONE_INT_FLAG	VM_DONE_INT_FLAG	TE_RDY_INT_FLAG	CMD_DONE_INT_FLAG	LPRX_RD_RDY_INT_FLAG
Type					A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	DSI_BUSY	**DSI busy status** 0: Idle 1: Busy
11	SKEWCAL_DONE_INT_FLAG	**Skew-calibration done interrupt status** 0: Clear interrupt 1: No effect
10	VM_VFP_STR_INT_FLAG	**Video mode VFP period start interrupt status** 0: Clear interrupt 1: No effect
9	VM_VACT_STR_INT_FLAG	**Video mode VACT period start interrupt status** 0: Clear interrupt 1: No effect
8	VM_VBP_STR_INT_FLAG	**Video mode VBP period start interrupt status** 0: Clear interrupt 1: No effect
7	TE_TIMEOUT_INT_FLAG	**TE time-out interrupt status** 0: Clear interrupt 1: No effect
6	SLEEPOUT_DONE_INT_FLAG	**ULPS sleep-out done interrupt status.** 0: Clear interrupt

Bit(s)	Name	Description
		1: No effect
5	VM_CMD_DONE_INT_FLAG	**DSI video mode command packet transmission interrupt status** 0: Clear interrupt 1: No effect
4	FRAME_DONE_INT_FLAG	**Frame done interrupt status** 0: Clear interrupt 1: No effect
3	VM_DONE_INT_FLAG	**DSI video mode finish interrupt status** 0: Clear interrupt 1: No effect
2	TE_RDY_INT_FLAG	**DSI TE ready interrupt status** 0: Clear interrupt 1: No effect
1	CMD_DONE_INT_FLAG	**DSI command mode finish interrupt status** 0: Clear interrupt 1: No effect
0	LPRX_RD_RDY_INT_FLAG	**RX data-ready interrupt status** 0: Clear interrupt 1: No effect

1401C010 DSI_COM_CON **DSI Common Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												DSI_DUAL_EN		DPHY_RESET		DSI_RESET
Type												RW		RW		RW
Reset												0		0		0

Bit(s)	Name	Description
4	DSI_DUAL_EN	**Enables DSI dual module** Enable this bit to start dual-DSI display simultaneously. 0: Disable dual start 1: Enable dual start
2	DPHY_RESET	**DIG_MIPI_TX software reset** 0: De-assert software reset 1: Assert software reset
0	DSI_RESET	**DSI module software reset** 0: De-assert software reset 1: Assert software reset

1401C014 DSI_MODE_CON **DSI Mode Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												SLEEP_MODE	C2V_SWITCH_O	V2C_SWITCH_O	MIX_MODE	FRAME_MODE

													N	N		
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															MODE_CON	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
20	SLEEP_MODE	**DSI sleep mode for ULPS wake-up operation** This mode is used during wake-up stage to leave ULPS. Set this bit to 1 before setting LANE_NUM to enable output data lane to LP-00; then set up SLEEPOUT_START to start the ULPS-exit process. 0: Disable 1: Enable
19	C2V_SWITCH_ON	**DSI auto-switch from command mode to video mode.** Set up this bit to wait for last TE and start video mode when running in command mode with TE 0: Disable 1: Enable
18	V2C_SWITCH_ON	**DSI auto-switch from video mode to command mode** Set up this bit to send last vsync and switch to command idle when running in video mode 0: Disable 1: Assert
17	MIX_MODE	**Mixed mode for command / video transmission.** Set up this bit to allow command packets in command queue transmitted after every VFP period in video mode 0: Disable 1: Enable
16	FRAME_MODE	**Single frame mode for video mode** Set up this bit to make DSI return to idle after each frame transmitted in video mode. 0: Disable 1: Enable
1:0	MODE_CON	**DSI mode control** Set DSI_EN = 1 when changing this register 0: Command mode 1: Sync-pulse video mode 2: Sync-event video mode 3: Burst video mode

1401C018 DSI_TXRX_CON DSI TX RX Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				LP_ONLY_VBLK	RGB_PKT_CNT				EXT_TE_TIME_VM				TE_TIMEOUT_CHK_EN	TE_WITH_CMD_EN	TYPE1_BTA_SEL	HSTX_CKLP_EN
Type				RW	RW				RW				RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RTN_SIZE				TE_AUTO_SYNC	EXT_TE_EDGE_	EXT_TE_EN	TE_FREERUN	HSTX_BLLP_EN	HSTX_DIS_EOT	LANE_NUM				VC_NUM	

						SEL											
Type	RW				RW	RW	RW	RW	RW	RW	RW				RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
28	LP_ONLY_VBLK	**Only enter LP mode at V-blanking while enable** 0: Disable 1: Enable
27:24	RGB_PKT_CNT	**Reverved counter target value for multi-packet in DE period, do not use in this version.**
23:20	EXT_TE_TIME_VM	**External TE timeout for video mode, unit: frame**
19	TE_TIMEOUT_CHK_EN	**Enables TE time-out check mechanism** Enable this bit to turn on DSI TE and external TE time-out check mechansim based on wait time of TE_TIMEOUT. 0: Disable 1: Enable
18	TE_WITH_CMD_EN	**In the tradition design, TE command excutes 'bus turnaround' and ignores other settings in the same command column. Combine the TE bit and other commands if this bit is asserted.** 0: Disable 1: Enable
17	TYPE1_BTA_SEL	**Selects TYPE1 BTA machenism** 0: TYPE1 BTA by frame 1: TYPE1 BTA by packet
16	HSTX_CKLP_EN	**Enables non-continuous clock lane** 0: Disable 1: Enable
15:12	MAX_RTN_SIZE	**Maximum return packet size** This register constrains maximum return packet that the slave side will send back to the host. It takes effect after the host sends 'Set Maximum Return Packet Size' packet to slave.
11	TE_AUTO_SYNC	**Enables TE auto-sync** Turn-on this register to automatically receive TE signals when command mode is idle. This bit is useful in command mode only. 0: Disable TE auto sync 1: Enable TE auto sync
10	EXT_TE_EDGE_SEL	**Selects trigger edge type of external TE** 0: Rising edge 1: Falling edge
9	EXT_TE_EN	**Enables external TE signal** This bit should be set to receive external TE if LPTE pin is used as external TE pin 0: Disable 1: Enable
8	TE_FREERUN	**TE free-run mode** If disabled, SW needs to wait for TE, write RACK and re-trigger DSI_START for the next transmission. If enabled, HW will detect TE and automatically to start the next transmission until it is disabled 0: Disable free-run mode 1: Enable free-run mode
7	HSTX_BLLP_EN	**Enables null packet transfer in BLLP.** 0: Disable 1: Enable
6	HSTX_DIS_EOT	**Disables end of transmission packet.** 0: Enable EoTp 1: Disable EoTp

Bit(s)	Name	Description
5:2	LANE_NUM	**Lane number** Set up this bit to turn on PRE_OE to enable lane circuit. 4'b0000: Disable all lanes 4'b0001: Enable 1 lane 4'b0011: Enable 2 lanes 4'b0111: Enable 3 lanes 4'b1111: Enable 4 lanes
1:0	VC_NUM	**Virtual channel parameter in video mode.**

1401C01C DSI_PSCON **DSI Pixel Stream Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							BYTE_SWAP	RGB_SWAP							DSI_PS_SEL	
Type							RW	RW							RW	
Reset							0	0							0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DSI_PS_WC													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25	BYTE_SWAP	**Selects byte order** For RGB565 type, it select to swap bytes between MSB and LSB. For other stream typs, this bit is not used. 0: Normal case 1: Byte order change
24	RGB_SWAP	**Selects order of RGB** For all color types, it changes the color order in format of RGB or BGR. 0: Normal case 1: R/B order change
17:16	DSI_PS_SEL	**Selects pixel stream type** 0: Packed pixel stream with 16-bit RGB 5-6-5 format 1: Packed pixel stream with 18-bit RGB 6-6-6 format 2: Loosely pixel stream with 24-bit RGB 6-6-6 format 3: Packed pixel stream with 24-bit RGB 8-8-8 format
13:0	DSI_PS_WC	**Word count of long packet in valid pixel data duration** Unit: Byte This value must be (H_SIZE*BPP). Take the QVGA display as an example, the value of PS_WC is (240*3) = 720 in decimal.

1401C020 DSI_VSA_NL **DSI Vertical Sync Active Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					VSA_NL											

Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	VSA_NL	**Vertical sync active duration** Unit: Line

1401C024 DSI_VBP_NL — DSI Vertical Back Porch Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					VBP_NL											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	VBP_NL	**Vertical back porch duration** Unit: Line

1401C028 DSI_VFP_NL — DSI Vertical Front Porch Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					VFP_NL											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	VFP_NL	**Vertical front porch duration** Unit: Line

1401C02C DSI_VACT_NL — DSI Vertical Active Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					VACT_NL											
Type					RW											

Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	VACT_NL	**Vertical active duration** Configures frame height of pixels in video mode and command mode.

1401C030 DSI_LFR_CON **DSI Low Frame Rate Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DSI_LFR_SKIP_NUM							DSI_LFR_VSE_DIS	DSI_LFR_UPDATE	DSI_LFR_EN	DSI_LFR_TYPE		DSI_LFR_MODE	
Type			RW							RW	RW	RW	RW		RW	
Reset			0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
13:8	DSI_LFR_SKIP_NUM	**Low frame rate skip frame number** Configure this register to control the number of frames to skip in LFR static mode.
6	DSI_LFR_VSE_DIS	**Disables low frame rate VSE** Set this bit to 1 to disable Vsync End packet transmission when low frame rate type is vsync only. 0: Enable VSE packet 1: Disable VSE packet
5	DSI_LFR_UPDATE	**Low frame rate update in dynamic mode** Set this bit from 0 to 1 to send one normal frame in LFR dynamic mode. In both modes, updating frames will reset the skip frame counter. 0: No effect 1: Update frame
4	DSI_LFR_EN	**Enables low frame rate** Set this bit to 1 to enable LFR (Low Frame Rate) mode. 0: Disable 1: Enable
3:2	DSI_LFR_TYPE	**Low frame rate transmission type** Selects packet types to be transmitted in skip frame 0: LP mode (no transmission) 1: Vsync only 2: Hsync only 3: Vsync + Hsync
1:0	DSI_LFR_MODE	**Low frame rate mode** Selects which mode is used for LFR control. Static mode allows DSI to send one normal frame per skip frames based on DSI_LFR_SKIP_NUM autometically, and dynamic mode allows software to control when to send normal frame manually. 0: Disable 1: Static mode 2: Dynamic mode 3: Both

Bit(s)	Name	Description

1401C034 DSI_LFR_STA **DSI Low Frame Rate Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DSI_LFR_SKIP_STA			DSI_LFR_SKIP_CNT					
Type								RU			RU					
Reset								0			0	0	0	0	0	0

Bit(s)	Name	Description
8	DSI_LFR_SKIP_STA	**Low frame rate skip frame status** 0: Normal frame 1: Skip frame
5:0	DSI_LFR_SKIP_CNT	**Low frame rate skip frame counter** Shows current frame count of skip frames in static mode

1401C050 DSI_HSA_WC **DSI Horizontal Sync Active Word Count Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DSI_HSA_WC											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	DSI_HSA_WC	**Word count of horizontal sync active duration** Follow the program sequence and configure sync pulse mode.

1401C054 DSI_HBP_WC **DSI Horizontal Back Porch Word Count Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DSI_HBP_WC											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	DSI_HBP_WC	**Word count of horizontal sync back porch duration** Follow the program sequence and configure all video mode.

1401C058 DSI_HFP_WC **DSI Horizontal Front Porch Word Count Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DSI_HFP_WC											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	DSI_HFP_WC	**Word count of horizontal sync front porch duration** Follow the program sequence and configure all video mode.

1401C05C DSI_BLLP_WC **DSI Horizontal Blanking or Low Power Mode Word Count Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DSI_BLLP_WC											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	DSI_BLLP_WC	**Word count of horizontal blanking or low power mode duration** Follow the program sequence and configure burst mode.

1401C060 DSI_CMDQ_CON **DSI Command Queue Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CMDQ_SIZE							
Type									RW							

Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	CMDQ_SIZE	**Number of commands in command queue** Range: 1 ~ 127

1401C064 DSI_HSTX_CKLP_WC **DSI HSTX Clock Low-power Mode Word Count Register** **00010000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																HSTX_CKLP_WC_AUTO
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HSTX_CKLP_WC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
16	HSTX_CKLP_WC_AUTO	**Automatic calculation for HSTX_CKLP_WC**
15:2	HSTX_CKLP_WC	**Word count of non-continuous clock lane counter** Sets up HSTX clock low-power period when HSTX_CKLP_EN = 1. Refer to programming guide for details on the usage.

1401C068 DSI_HSTX_CKLP_WC_AUTO_RESULT **DSI HSTX Clock Low-power Mode Automatic Calculation result** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HSTX_CKLP_WC_AUTO_RESULT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	HSTX_CKLP_WC_AUTO_RESULT	DSI HSTX Clock Low-power Mode Automatic Calculation result

1401C074 DSI_RX_DATA03 **DSI Receive Packet Data Byte 0 ~ 3 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BYTE3								BYTE2							
Type	RO								RO							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE1								BYTE0							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	BYTE3	RX read data buffer byte 3
23:16	BYTE2	RX read data buffer byte 2
15:8	BYTE1	RX read data buffer byte 1
7:0	BYTE0	RX read data buffer byte 0

1401C078 DSI_RX_DATA47 DSI Receive Packet Data Byte 4 ~ 7 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BYTE7								BYTE6							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE5								BYTE4							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	BYTE7	RX read data buffer byte 7
23:16	BYTE6	RX read data buffer byte 6
15:8	BYTE5	RX read data buffer byte 5
7:0	BYTE4	RX read data buffer byte 4

1401C07C DSI_RX_DATA8B DSI Receive Packet Data Byte 8 ~ 11 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BYTEB								BYTEA							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE9								BYTE8							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	BYTEB	RX read data buffer byte 11
23:16	BYTEA	RX read data buffer byte 10
15:8	BYTE9	RX read data buffer byte 9
7:0	BYTE8	RX read data buffer byte 8

1401C080 DSI_RX_DATAAC DSI Receive Packet Data Byte 12 ~ 15 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BYTEF								BYTEE							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTED								BYTEC							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	BYTEF	RX read data buffer byte 15
23:16	BYTEE	RX read data buffer byte 14
15:8	BYTED	RX read data buffer byte 13
7:0	BYTEC	RX read data buffer byte 12

1401C084 DSI_RX_RACK — DSI Read Data Acknowledge Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RACK_BYPASS	RACK
Type															RW	W1C
Reset															0	0

Bit(s)	Name	Description
1	RACK_BYPASS	**Enables RX read acknowledge bypass** Set this bit to enable to ignore RACK from SW and continue next commands 1: Does not check RACK 0: Check RACK
0	RACK	**Acknowledges RX read** When a read command is executed and read data are received completely, the LPRX_RD_RDY interrupt will be issued. After read from the RX_DATA buffer, set up this bit to continue to the next command. 1: Acknowledge 0: No effect

1401C088 DSI_RX_TRIG_STA — DSI Receiver Status Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_POINTER					RX_LPDT	DIRECTION	RX_ULPS	RX_TRIG_3	RX_TRIG_2	RX_TRIG_1	RX_TRIG_0

Type					RU					RU	RU	RU	RU	RU	RU	RU
Reset					0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
11:8	RX_POINTER	**RX data count**
6	RX_LPDT	**RX low power data transmission state**
5	DIRECTION	**Escape turnaround direction** Current bus direction of Data Lane 0. If set to 1, there will be reverse direction transmission on Data Lane0 in Low Power mode. Otherwise, it will be a forward direction transmission. 1: Reverse direction 0: Forward direction
4	RX_ULPS	**RX ULPS (Ultra-low power state)** Entry pattern is 00011110
3	RX_TRIG_3	**Reserved by DSI specification.** Entry pattern is 10100000
2	RX_TRIG_2	**Acknowledge.** Entry pattern is 00100001
1	RX_TRIG_1	**TE.** Entry pattern is 01011101
0	RX_TRIG_0	**Remote application reset.** Entry pattern is 01100010

1401C090 DSI_MEM_CONTI DSI Memory Continue Command Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DSI_RWMEM_CONTI															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DSI_RWMEM_CONTI	Read/Write memory continue command.

1401C094 DSI_FRM_BC DSI Frame Byte Count Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												DSI_FRM_BC				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DSI_FRM_BC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	DSI_FRM_BC	**Frame buffer byte count** The total number of byte is expected to be read for type3 command.

1401C098 DSI_V3D_CON DSI Vsync 3D Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								V3D_EN			V3D_LR	V3D_VSYNC	V3D_FMT		V3D_MODE	
Type								RW			RW	RW	RW		RW	
Reset								0			0	0	0	0	0	0

Bit(s)	Name	Description
8	V3D_EN	Enables 3D control payload to be present in video mode VSS packet
5	V3D_LR	3D left/right order
4	V3D_VSYNC	Enables the second VSYNC between images on the left and right
3:2	V3D_FMT	3D image format
1:0	V3D_MODE	3D mode on/off, display orientation

1401C0A0 DSI_TIME_CON0 DSI Timing Control 0 Register 00060080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SKEWCAL_PRD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ULPS_WAKEUP_PRD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SKEWCAL_PRD	**Skew calibration period** Cycle count for skew-calibration period defined in DPHY 1.2 spec to continuously send out calibration patterns. Total time = (SKEWCAL_PRD*1024*DSI clock cycle time) Default value: 45us under 130MHz DSI byte clock
15:0	ULPS_WAKEUP_PRD	**ULPS wakeup period** Cycle count for ultra-low power state (ULPS) wake-up during ULPS-exit sequence. Total wait time = (ULPS_WAKEUP_PRD*1024*DSI clock cycle time) Default value: 1ms under 130MHz DSI byte clock

1401C0A4 DSI_TIME_CON1 DSI Timing Control 1 Register 000A2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PREFETCH_EN	PREFETCH_TIME														
Type	RW	RW														

Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TE_TIMEOUT_PRD															
Type	RW															
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PREFETCH_EN	**Prefetch enable for GCE to get DSI SOF prior to DE start.** 0: Disable 1: Enable
30:16	PREFETCH_TIME	**Prefetch pulse time**
15:0	TE_TIMEOUT_PRD	**TE time-out check period** Cycle count to check TE time-out and issue time-out interrupt when waiting for TE signal. Total wait time = (TE_TIMEOUT_PRD*16384*DSI clock cycle time) Default value: 1sec under 130MHz DSI byte clock

1401C100 DSI_PHY_LCPAT DSI PHY Lane Clock Pattern Register 00000055

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LC_HSTX_CK_PAT							
Type									RW							
Reset									0	1	0	1	0	1	0	1

Bit(s)	Name	Description
7:0	LC_HSTX_CK_PAT	**Clock lane HSTX clock pattern** Configure this field to generate HSTX clock pattern and change polarity. Default: Rising edge pulse first

1401C104 DSI_PHY_LCCON DSI PHY Lane Clock Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														LC_WAKEUP_EN	LC_ULPM_EN	LC_HSTX_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	LC_WAKEUP_EN	**Enables clock lane wake-up** Make the clock lane wake-up from ultra-low power mode. Make sure DSI_EN = 1 when setting this register

Bit(s)	Name	Description
1	LC_ULPM_EN	**Enables clock lane ULPS** Make the clock lane go to ultra-low power mode. Make sure DSI_EN = 1 when setup this register
0	LC_HSTX_EN	**Enables clock lane HS mode** Start clock lane high speed transmission.

1401C108 DSI_PHY_LD0CON DSI PHY Lane 0 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												Lo_RX_FILTER_EN	LX_ULPM_AS_Lo	Lo_WAKEUP_EN	Lo_ULPM_EN	Lo_RM_TRIG_EN
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	Lo_RX_FILTER_EN	**Enables data lane 0 RX glitch filter** If the MIPI RX signal from peripheral is not stable, set up this bit to filter the signal glitches
3	LX_ULPM_AS_Lo	**Enables data lane 1/2/3 ULPS mode** Set up this bit to make data lane 1/2/3 enter ULPS accompanied by data lane 0.
2	Lo_WAKEUP_EN	**Enables data lane 0 wake-up** Make the data lane 0 wake-up from ultra-low power mode.
1	Lo_ULPM_EN	**Enables data lane 0 ULPS** Make the data lane 0 go to ultra-low power mode.
0	Lo_RM_TRIG_EN	**Enables data lane 0 remote application trigger** Send application trigger to slave side.

1401C10C DSI_PHY_SYNCON DSI PHY Sync Control Register 000000B8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								HS_DB_SYNC_EN	HS_SKEWCAL_PAT							
Type								RW	RW							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HS_SYNC_CODE2								HS_SYNC_CODE							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0

Bit(s)	Name	Description
24	HS_DB_SYNC_EN	**Enables HSTX double-byte sync code** Set this bit to 1 if 16-bit sync code is to be sent. The LSB is HS_SYNC_CODE; the MSB is HS_SYNC_CODE2.

Bit(s)	Name	Description
23:16	HS_SKEWCAL_PAT	**HSTX skew calibration pattern** Set up this bit to transmit continuous pattern code for skew calibration.
15:8	HS_SYNC_CODE2	**HSTX sync code 2** If a sync code with 16-bit length is sent, fill out this field.
7:0	HS_SYNC_CODE	**HSTX sync code** Sync code byte sent for high-speed transmission

1401C110 DSI_PHY_TIMCON0 DSI PHY Timing Control 0 Register 14140A0A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DA_HS_TRAIL								DA_HS_ZERO							
Type	RW								RW							
Reset	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_HS_PREP								LPX							
Type	RW								RW							
Reset	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
31:24	DA_HS_TRAIL	Control for timing parameter: T_HS-Trail
23:16	DA_HS_ZERO	Control for timing parameter: T_HS-Zero
15:8	DA_HS_PREP	Control for timing parameter: T_HS-Prepare
7:0	LPX	Control for timing parameter: T_LPX

1401C114 DSI_PHY_TIMCON1 DSI PHY Timing Control 1 Register 0E1A1632

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DA_HS_EXIT								TA_GET							
Type	RW								RW							
Reset	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TA_SURE								TA_GO							
Type	RW								RW							
Reset	0	0	0	1	0	1	1	0	0	0	1	1	0	0	1	0

Bit(s)	Name	Description
31:24	DA_HS_EXIT	Control for timing parameter: T_HS-Exit for data lane
23:16	TA_GET	Control for timing parameter: T_TA-Get
15:8	TA_SURE	Control for timing parameter: T_TA-Sure
7:0	TA_GO	Control for timing parameter: T_TA-Go

1401C118 DSI_PHY_TIMCON2 DSI PHY Timing Control 2 Register 14140100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLK_HS_TRAIL								CLK_HS_ZERO							
Type	RW								RW							
Reset	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	DA_HS_SYNC								CONT_DET							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	CLK_HS_TRAIL	Control for timing parameter: T_CLK-Trail
23:16	CLK_HS_ZERO	Control for timing parameter: T_CLK-Zero
15:8	DA_HS_SYNC	Control for timing parameter: T_HS-Sync
7:0	CONT_DET	Control for contention detection cycle

1401C11C DSI_PHY_TIMCON3 **DSI PHY Timing Control 3 Register** **000E0E0A**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CLK_HS_EXIT							
Type									RW							
Reset									0	0	0	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_HS_POST								CLK_HS_PREP							
Type	RW								RW							
Reset	0	0	0	0	1	1	1	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
23:16	CLK_HS_EXIT	Control for timing parameter: T_HS-Exit for clock lane
15:8	CLK_HS_POST	Control for timing parameter: T_CLK-Post
7:0	CLK_HS_PREP	Control for timing parameter: T_CLK-Prepare

1401C130 DSI_VM_CMD_CON **DSI Video Mode Command Packet Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CM_DATA_1								CM_DATA_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CM_DATA_ID										TS_VFP_EN	TS_VBP_EN	TS_VSA_EN	TIME_SEL	LONG_PKT	VM_CMD_EN
Type	RW										RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
31:24	CM_DATA_1	**Command packet data byte 1** If short packet, the byte will be used as DATA 1. If long packet, this registers should be 0 because word count should be less than 16 bytes.
23:16	CM_DATA_0	**Command packet data byte 0** If short packet, the byte will be used as DATA 0. If long packet, this registers should be used as Word Count 0 for long packet
15:8	CM_DATA_ID	**Command packet data ID** *Note: The packet data ID should contain both data type and VC.*
5	TS_VFP_EN	**Command packet is allowable in VFP period** 0: Disable

Bit(s)	Name	Description
		1: Enable
4	TS_VBP_EN	**Command packet is allowable in VBP period** 0: Disable 1: Enable
3	TS_VSA_EN	**Command packet is allowable in VSA period** 0: Disable 1: Enable
2	TIME_SEL	**Timing interval for transmission** Allowable timing interval for command transmission in BLLP period. Select RGB if the HBP interval length is shorter than long packet length to be sent. 0: HBP timing interval 1: RGB timing interval
1	LONG_PKT	**Command packet type** 0: Short packet 1: Long packet
0	VM_CMD_EN	**Enables video mode command packet transmission** 0: Disable 1: Enable

1401C134 DSI_VM_CMD_DATA0 — DSI Video Mode Command Packet Data Byte 0~3 Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD	**Command packet word** Command packet data byte 0~3 of long packet for video mode transmission

1401C138 DSI_VM_CMD_DATA4 — DSI Video Mode Command Packet Data Byte 4~7 Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD	**Command packet word** Command packet data byte 4~7 of long packet for video mode transmission

Bit(s)	Name	Description

1401C13C DSI_VM_CMD_DATA8 — DSI Video Mode Command Packet Data Byte 8~11 Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD	**Command packet word** Command packet data byte 8~11 of long packet for video mode transmission

1401C140 DSI_VM_CMD_DATAC — DSI Video Mode Command Packet Data Byte 12~15 Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD	**Command packet word** Command packet data byte 12~15 of long packet for video mode transmission

1401C144 DSI_CKSM_OUT — DSI Checksum Output — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACC_CHKSUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PKT_CHKSUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ACC_CHKSUM	**Accumulated packet checksum** Checksum value of sequentially accumulated packets for System

Bit(s)	Name	Description
15:0	PKT_CHKSUM	Level Test (SLT) **Transmitted packet checksum** Checksum value of the last transmitted packet for System Level Test (SLT)

1401C148 DSI_STATE_DBG0 DSI State Machine Debug 0 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												DPHY_HS_TX_STATE_C				
Type												RU				
Reset												0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DPHY_CTL_STATE_C								
Type								RU								
Reset								0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
20:16	DPHY_HS_TX_STATE_C	DSI DPHY clock lane HSTX state monitor
8:0	DPHY_CTL_STATE_C	DSI DPHY clock lane control state monitor

1401C14C DSI_STATE_DBG1 DSI State Machine Debug 1 01010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DPHY_ESC_STATE_0											DPHY_HS_TX_STATE_0				
Type	RU											RU				
Reset	0	0	0	0	0	0	0	1				0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DPHY_CTL_STATE_0														
Type		RU														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:24	DPHY_ESC_STATE_0	DSI DPHY Data Lane 0 escape state monitor
20:16	DPHY_HS_TX_STATE_0	DSI DPHY Data Lane 0 HSTX state monitor
14:0	DPHY_CTL_STATE_0	DSI DPHY Data Lane 0 control state monitor

1401C150 DSI_STATE_DBG2 DSI State Machine Debug 2 01010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DPHY_TA_R2T_STATE								DPHY_TA_T2R_STATE				
Type				RU								RU				
Reset				0	0	0	0	1				0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							DPHY_RX_ESC_STATE									
Type							RU									
Reset							0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28:24	DPHY_TA_R2T_STATE	DSI DPHY Data Lane 0 turnaround RX to TX state monitor
20:16	DPHY_TA_T2R_STATE	DSI DPHY Data Lane 0 turnaround TX to RX state monitor
9:0	DPHY_RX_ESC_STATE	DSI DPHY Data Lane 0 LPRX escape state monitor

1401C154 DSI_STATE_DBG3 **DSI State Machine Debug 3** **01010101**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DPHY_HS_TX_STATE_2								DPHY_CTL_STATE_2				
Type				RU								RU				
Reset				0	0	0	0	1				0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DPHY_HS_TX_STATE_1								DPHY_CTL_STATE_1				
Type				RU								RU				
Reset				0	0	0	0	1				0	0	0	0	1

Bit(s)	Name	Description
28:24	DPHY_HS_TX_STATE_2	DSI DPHY Data Lane 2 HSTX state monitor
20:16	DPHY_CTL_STATE_2	DSI DPHY Data Lane 2 control state monitor
12:8	DPHY_HS_TX_STATE_1	DSI DPHY Data Lane 1 HSTX state monitor
4:0	DPHY_CTL_STATE_1	DSI DPHY Data Lane 1 control state monitor

1401C158 DSI_STATE_DBG4 **DSI State Machine Debug 4** **00000101**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DPHY_HS_TX_STATE_3								DPHY_CTL_STATE_3				
Type				RU								RU				
Reset				0	0	0	0	1				0	0	0	0	1

Bit(s)	Name	Description
12:8	DPHY_HS_TX_STATE_3	DSI DPHY Data Lane 3 HSTX state monitor
4:0	DPHY_CTL_STATE_3	DSI DPHY Data Lane 3 control state monitor

1401C15C DSI_STATE_DBG5 **DSI State Machine Debug 5** **10000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WAKE UP_STATE															TIMER_BUSY
Type	RU															RU
Reset	0	0	0	1												0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	TIMER_COUNTER															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	WAKEUP_STATE	DSI sleep-out state monitor
16	TIMER_BUSY	DSI sleep mode/TE time-out timer busy status
15:0	TIMER_COUNTER	DSI sleep mode/TE time-out timer counter

1401C160 DSI_STATE_DBG6 — DSI State Machine Debug 6 — 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										CMDQ_STATE						
Type										RU						
Reset										0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CMCTL_STATE														
Type		RU														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
22:16	CMDQ_STATE	DSI command queue state monitor
14:0	CMCTL_STATE	DSI command control state monitor

1401C164 DSI_STATE_DBG7 — DSI State Machine Debug 7 — 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VSA_PERIOD	VBP_PERIOD	VACT_PERIOD	VFP_PERIOD		VMCTL_STATE										
Type	RU	RU	RU	RU		RU										
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15	VSA_PERIOD	DSI video mode VSA indication
14	VBP_PERIOD	DSI video mode VBP indication
13	VACT_PERIOD	DSI video mode VACT indication
12	VFP_PERIOD	DSI video mode VFP indication
10:0	VMCTL_STATE	DSI video mode control state monitor

1401C168 DSI_STATE_DBG8 — DSI State Machine Debug 8 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			WORD_COUNTER													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	WORD_COUNTER	DSI packet word count monitor

1401C16C DSI_STATE_DBG9 — DSI State Machine Debug 9 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											LINE_COUNTER					
Type											RU					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LINE_COUNTER															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:0	LINE_COUNTER	DSI packet line count monitor

1401C170 DSI_DEBUG_SEL — DSI Debug Output Selection — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								CHKSUM_REC_EN				DEBUG_OUT_SEL				
Type								RW				RW				
Reset								0				0	0	0	0	0

Bit(s)	Name	Description
8	CHKSUM_REC_EN	**Enables checksum record** Set this bit to enable checksum record circuit to obtain PKT_CHKSUM and ACC_CHKSUM in DSI_CKSM_OUT register.
4:0	DEBUG_OUT_SEL	**Selects DSI debug out** This register selects which group of internal signal is sent to debug output port. It is only for hardware debug purpose and not described here.

1401C174 DSI_RESERV — Reserved Register — FFF00000

ED

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSI_RESERVED															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DSI_RESERVED															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DSI_RESERVED	DSI reserved register for HW usage

1401C178 DSI_BIST_PATTERN — DSI Bist Pattern Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BIST_PATTERN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIST_PATTERN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BIST_PATTERN	DSI BIST test register for HW verification

1401C17C DSI_BIST_CON — DSI Bist Control Register — 00200000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BIST_TIMI ING							
Type									RW							
Reset									0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					BIST_LANE_NUM					SELF_PAT_MODE		BIST_HS_FREE	BIST_SPECIFIED_PATTERN	BIST_FIX_PATTERN	BIST_ENABLE	BIST_MODE
Type					RW					RW		RW	RW	RW	RW	RW
Reset					0	0	0	0		0		0	0	0	0	0

Bit(s)	Name	Description
23:16	BIST_TIMIING	**BIST timing control for MIPI signal**
11:8	BIST_LANE_NUM	**BIST lane number** 4'b0000: Disable all lanes 4'b0001: Enable 1 lane 4'b0011: Enable 2 lanes 4'b0111: Enable 3 lanes

Bit(s)	Name	Description
		4'b1111: Enable 4 lanes
6	SELF_PAT_MODE	**Enables the self-pattern test mode to show built-in pattens according to configuration of BIST_PATTERN value** 0: Disable 1: Enable
4	BIST_HS_FREE	**Enables BIST free run test** 0: Normal mode 1: Free-run mode
3	BIST_SPECIFIED_PATTERN	**Enables BIST specified pattern** 0: Not specified pattern 1: Specified pattern
2	BIST_FIX_PATTERN	**Enables BIST fix pattern** 0: Not fix pattern 1: Fix pattern
1	BIST_ENABLE	**Start BIST mode** 0: No effect 1: Trigger
0	BIST_MODE	**Enables BIST mode** 0: Disable 1: Enable

1401C180 DSI_VM_CMD_DATA10 — DSI Video Mode Command Packet Data Byte 16~19 Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD	**Command packet word** Command packet data byte 16~19 of long packet for video mode transmission

1401C184 DSI_VM_CMD_DATA14 — DSI Video Mode Command Packet Data Byte 20~23 Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD	**Command packet word**

Bit(s)	Name	Description
		Command packet data byte 20~23 of long packet for video mode transmission

1401C188 DSI_VM_CMD_DATA18 DSI Video Mode Command Packet Data Byte 24~27 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD	**Command packet word** Command packet data byte 24~27 of long packet for video mode transmission

1401C18C DSI_VM_CMD_DATA1C DSI Video Mode Command Packet Data Byte 28~31 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD	**Command packet word** Command packet data byte 28~31 of long packet for video mode transmission

1401C200~1401C3FC DSI_CMDQ[n](n=0~127) DSI Command Queue 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA_1								DATA_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_ID								RESV		TE	CL	HS	BTA	TYPE	
Type	RW								RW		RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
31:24	DATA_1	**Data byte 1 of command**
23:16	DATA_0	**Data byte 0 of command**
15:8	DATA_ID	**Data ID of command**
7:6	RESV	**Reserved**
5	TE	**Enables internal or external TE** 0: Disable 1: Enable
4	CL	**Selects DCS byte** 0: 1-byte DCS 1: 2-byte DCS
3	HS	**Enables high-speed transmission** 0: LPTX transmission 1: HSTX transmission
2	BTA	**Enables BTA** 0: Disable 1: Enable
1:0	TYPE	**Command types** 0: Type-0 command 1: Type-1 command 2: Type-2 command 3: Type-3 command

4.5 JPEG Encoder

Module name: jpgenc Base address: (+17003000h)

Address	Name	Width	Register Function
17003100	JPGENC_RSTB	32	JPEG Encoder Reset Register
17003104	JPGENC_CTRL	32	JPEG Encoder Control Register
17003108	JPGENC_QUALITY	32	JPEG Encoder Quality Setting Register
1700310C	JPGENC_BLK_NUM	32	JPEG Encoder Total Block Number Register
17003110	JPGENC_BLK_CNT	32	JPEG Encoder Current Block Count Register
1700311C	JPGENC_INT_STS	32	JPEG Encoder Interrupt Status Register
17003120	JPGENC_DST_ADDR0	32	JPEG Encoder Destination Address 0 Register
17003124	JPGENC_DMA_ADDR0	32	JPEG Encoder Write Address 0 Register
17003128	JPGENC_STALL_ADDR0	32	JPEG Encoder Stall Address 0 Register
17003138	JPGENC_OFFSET_ADDR	32	JPEG Encoder Offset Address Register
1700313C	JPGENC_CURR_DMA_ADDR	32	JPEG Encoder Current Write Address Register
17003150	JPGENC_RST_MCU_NUM	32	JPEG Encoder Restart MCU Number Register
17003154	JPGENC_IMG_SIZE	32	JPEG Encoder Image Size Register
17003160	JPGENC_DEBUG_INFO0	32	JPEG Encoder Debug Information 0 Register
17003164	JPGENC_DEBUG_INFO1	32	JPEG Encoder Debug Information 1 Register
17003168	JPGENC_TOTAL_CYCLE	32	JPEG Encoder performance Counter Register
1700316C	JPGENC_BYTE_OFFSET_MASK	32	JPEG Encoder Destination Address Offset Mask Register
17003170	JPGENC_SRC_LUMA_ADDR	32	JPEG Encoder Luma Source Data Base Address Register
17003174	JPGENC_SRC_CHROMA_ADDR	32	JPEG Encoder Chroma Source Data Base Address Register
17003178	JPGENC_STRIDE	32	JPEG Encoder Memory Stride Register
1700317C	JPGENC_IMG_STRIDE	32	JPEG Encoder Image Stride Width Register
17003200	JPGENC_RDMA_CHKSUM	32	JPEG Encoder RDMA Checksum
17003204	JPGENC_BSDMA_CHKSUM	32	JPEG Encoder BSDMA Checksum
17003300	JPGENC_DCM_CTRL	32	JPEG Encoder DCM Control Register
17003318	JPGENC_ULTRA_THRES	32	JPEG Encoder Ultra Threshold Control Register
1700331C	JPGENC_LATENCY_THRES	32	JPEG Encoder Latency Threshold Control Register
17003400	JPGENC_IRQ_EN	32	JPEG Encoder IRQ Enable Control Register

17003100 JPGENC_RST JPEG Encoder Reset Register 00000001

B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RSTB
Type																RW
Reset																1

Bit(s)	Name	Description
0	RSTB	**Resets JPEG encoder's active-low** After resetting the JPEG encoder, the bit of RSTB should be re-assigned to 1. Note: Reset the JPEG encoder before encoding each new image. If resetting the encoder during encoding is required, follow the soft reset mechanism. Hard reset may cause unexpected SMI behavior. 0: Reset mode 1: Normal mode

17003104 JPGENC_CTRL JPEG Encoder Control Register 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				ULTRA_CTRL												
Type				RW												
Reset				0	0	0	0									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RST_MARK					JPG	YUV		INT_EN		EN
Type						RW					RW	RW		RW		RW
Reset						0					0	0	0	1		0

Bit(s)	Name	Description
28:25	ULTRA_CTRL	**Controls JPEG SMI port ultra option enable** Set it to 1 to enable the corresponding option bit[28]: RDMA GULTRA bit[27]: RDMA GPREULTRA bit]26]: BSDMA GULTRA bit[25]: BSDMA GPREULTRA
10	RST_MARK	**Restarts interval encoding process enable** JPEG encoder inserts restart marker based on JPGENC_RST_MCU_NUM. JPGENC_RST_MCU_NUM should be bigger than 0. 0: Disable 1: Enable
5	JPG	**JPEG or JFIF/EXIF** If JFIF/EXIF format is enabled, the JPEG encoder will not write out SOI marker (start from 0xffd8) but write out from DQT maker (start from 0xffdb). Software program can fill the JFIF/EXIF content above the DQT marker to finish one JFIF/EXIF JPEG file. 0: JPEG mode 1: JFIF/EXIF
4:3	YUV	**YUV format**

Bit(s)	Name	Description
		0: YUV422 (YUYV) 1: YUV422 (YVYU) 2: YUV420 (NV12) 3: YUV420 (NV21)
2	INT_EN	**Enables interrupt** 0: Disable 1: Enable
0	EN	**Trigger signal to enable the JPEG encoder.** This bit is cleared by hardware after encoding is done. For software reset, this bit should be set to 0 first.

17003108 JPGENC_QUALITY JPEG Encoder Quality Setting Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												QT			QUALITY	
Type												RW			RW	
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:2	QT	**Quantization table setting for frame 1 (only works in continuous shooting mode)** 00: High quality table 01: Good quality table 10: Fair quality table 11: Low quality table
1:0	QUALITY	**Quantization level setting for frame 1 (only works in continuous shooting mode)** 00: Low, only for high and good quality quantization table 01: Fair 10: Good 11: High

1700310C JPGENC_BLK_NUM JPEG Encoder Total Block Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						BLK_NUM										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLK_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:0	BLK_NUM	**Total 8x8 block number.**

Bit(s)	Name	Description
		Min. value: 4 (Image with block number smaller than 4 cannot be encoded, which is the hardware limitation) *Note: The dummy 8x8 block must be considered in BLK_NUM. For example, for a 162x128 YUV420 JPEG file, the block number setting should be 527.*

17003110 JPGENC_BLK_CNT **JPEG Encoder Current Block Count Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RD_RLE					BLK_CNT										
Type	RW					RO										
Reset	0					0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLK_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RD_RLE	**Read RLE current 8x8 block count control** 0: FDCT current block count 1: RLE current block count
26:0	BLK_CNT	**Current encoded 8x8 block number**

1700311C JPGENC_INT_STS **JPEG Encoder Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												ERROR			STALL	ENCODE_DONE
Type												RW			RW	RW
Reset												0			0	0

Bit(s)	Name	Description
4	ERROR	**Shows if codec selection is accessed by video encoder when JPGENC is working**
1	STALL	**Stall interrupt** Indicates that encoding operation is reaching the memory bound configured by software and entering stall condition. Set this bit to 0 after reading and reset hardware to start another encoding process.
0	ENCODE_DONE	**Done interrupt** Indicates that encoding operation is done. Set it to 0 after reading.

17003120 JPGENC_DST **JPEG Encoder Destination** **00000000**

_ADDR0 Address 0 Register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEST_ADDR0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEST_ADDR0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	DEST_ADDR0	**JPEG encoder destination address setting 0** Should be 16-byte aligned.

17003124 JPGENC_DMA_ADDR0 JPEG Encoder Write Address 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_ADDR0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_ADDR0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DMA_ADDR0	**JPEG encoder current written address setting 0** This address information will be updated after every one burst write command is finished.

17003128 JPGENC_STALL_ADDR0 JPEG Encoder Stall Address 0 Register 000000F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STALL_ADDR0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STALL_ADDR0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	1	1	1				

Bit(s)	Name	Description
31:4	STALL_ADDR0	**JPEG encoder stall address setting 0** The stall address should be 16-byte aligned and set to bigger than the actual upper bound by one burst command (128 bytes). Whenever the stall address is reached, the JPEG encoder stalls and issues an interrupt to software. The software can discard the uncompleted file by simply resetting the JPEG encoder to cancel the encode operation. JPGENC_STALL_ADDR should be bigger than JPGENC_DEST_ADDR by at least 624 bytes to guarantee that the

Bit(s)	Name	Description
		header of the JPEG file can be completely written into memory. *Note: JPG_ENC_STALL_ADDR should not be smaller than JPG_ENC_DEST_ADDR; otherwise stall condition will occur.*

17003138 JPGENC_OFFSET_ADDR JPEG Encoder Offset Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFFSET_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
15:4	OFFSET_ADDR	**JPEG encoder offset address** This address should be 16-byte aligned. OFFSET_ADDR should be set to 0 if this function is not needed. *Note: OFFSET_ADDR is set before starting encoding process only to offset the destination address for the application such as EXIF mode.*

1700313C JPGENC_CURR_DMA_ADDR JPEG Encoder Current Write Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CURR_DMA_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CURR_DMA_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CURR_DMA_ADDR	Current DMA address during encoding

17003150 JPGENC_RST_MCU_NUM JPEG Encoder Restart MCU Number Register 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RST_MCU_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
15:0	RST_MCU_NUM	**JPEG encoder restart interval** If re-start marker is enabled, JPEG encoder will insert one re-start marker whenever the defined MCU number is enabled. For example, to insert one re-start marker every N MCUs, RST_MCU_MUN should be programmed to N. *Note: RST_MCU_NUM should be bigger than 0 if the restart marker insertion is enabled.*

17003154 JPGENC_IMG_SIZE JPEG Encoder Image Size Register 0A200798

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	XSIZE															
Type	RW															
Reset	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	YSIZE															
Type	RW															
Reset	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	0

Bit(s)	Name	Description
31:16	XSIZE	Width of current image
15:0	YSIZE	Height of current image

17003160 JPGENC_DEBUG_INFO0 JPEG Encoder Debug Information 0 Register 00022000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							PXL_VLD	DMA_REQ							VLC_EPY	END_IMG
Type							RO	RO							RO	RO
Reset							0	0							1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			GMC_IDLE	HEAD								GREQ	ENC_STATE			
Type			RO	RO								RO	RO			
Reset			1	0								0	0	0	0	0

Bit(s)	Name	Description
25	PXL_VLD	**Date valid indicator from JPEG DMA** 0: Idle 1: Valid
24	DMA_REQ	**Request status between JPEG encoder and JPEG DMA** 0: Idle 1: Active
17	VLC_EPY	**Empty status of VLC buffer** 0: Not empty 1: Empty
16	END_IMG	**Frame end indicator** 0: Not in frame end 1: Process the last block data of the current frame
13	GMC_IDLE	**Status of GMC port for JPEG encoder**

Bit(s)	Name	Description
		0: Active 1: Idle
12	HEAD	**Header generation indicator** 0: JPEG encoder is not generating header stream. 1: JPEG encoder is generating header stream.
4	GREQ	**Memory access status** 0: Active 1: Idle
3:0	ENC_STATE	**FSM status of JPEG encoder** 0: IDLE 1: INIT 2: START_HEADER 3: HEADER_GEN 4: WAIT_FST_FDCT 5: TRANS_COEFF 6: WAIT_RLE 7: WAIT_FDCT 8: WAIT_DONE 9: WAIT_ENC_DONE 10: WAIT_FST_FDCT_RDY 11: STOP_BLK 12: WAIT_TO_IDLE

17003164 JPGENC_DEBUG_INFO1 JPEG Encoder Debug Information 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLE_CYCLE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLE_CYCLE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RLE_CYCLE_CNT	Process cycle of Huffman encoding

17003168 JPGENC_TOTAL_CYCLE JPEG Encoder performance Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TOTAL_CYCLE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOTAL_CYCLE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TOTAL_CYCLE	Total cycle count of JPEG encoder

1700316C JPGENC_BYTE_OFFSET_MASK — **JPEG Encoder Destination Address Offset Mask Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE_OFFSET_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BYTE_OFFSET_MASK	**Actual destination address = Destination address + offset address + destination address offset mask** Bit 4~15 are reserved for future use. 0: No offset 1~15: Offset byte from the 16-byte aligned destination address setting

17003170 JPGENC_SRC_LUMA_ADDR — **JPEG Encoder Luma Source Data Base Address Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LUMA_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUMA_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	LUMA_BASE	**LUMA source data base address** YUV422: Memory base address of image data YUV420: Memory base address of luma image data

17003174 JPGENC_SRC_CHROMA_ADDR — **JPEG Encoder Chroma Source Data Base Address Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHROMA_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHROMA_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	CHROMA_BASE	**CHROMA source data base address** YUV422: Not used YUV420: Memory base address of chroma image data

17003178 JPGENC_STRIDE **JPEG Encoder Memory Stride Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STRIDE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
15:4	STRIDE	**JPEG encoder memory stride register** Should be 128-byte aligned.

1700317C JPGENC_IMG_STRIDE **JPEG Encoder Image Stride Width Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STRIDE_IMG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
15:4	STRIDE_IMG	**JPEG encoder image stride register** Should be MCU alignment. For YUV422, it is 32-byte alignment. For YUV420, it is 16-byte alignment.

17003200 JPGENC_RDMA_CHKSUM **JPEG Encoder RDMA Checksum** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA_CHKSUM															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA_CHKSUM															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	RDMA_CHKSUM	Checksum

17003204 JPGENC_BSDMA_CHKSUM **JPEG Encoder BSDMA Checksum** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BSDMA_CHKSUM															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSDMA_CHKSUM															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	BSDMA_CHKSUM	Checksum

17003300 JPGENC_DCM_CTRL **JPEG Encoder DCM Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																STATUS
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DISABLE
Type																RW
Reset																0

Bit(s)	Name	Description
16	STATUS	0: JPGENC clock is off. 1: JPGENC clock is on.
0	DISABLE	0: Enable JPGENC DCM (default) 1: Disable JPGENC DCM

17003318 JPGENC_ULTRA_THRES **JPEG Encoder Ultra Threshold Control Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA_ULTRA_THRES								RDMA_PREULTRA_THRES							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSDMA_ULTRA_THRES								BSDMA_PREULTRA_THRES							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description

Bit(s)	Name	Description
31:24	RDMA_ULTRA_THRES	**Sets up RDMA gultra threshold** Useful if the corresponding ultra enable bit is set.
23:16	RDMA_PREULTRA_THRES	**Sets up RDMA gpreultra threshold** Useful if the corresponding preultra enable bit is set.
15:8	BSDMA_ULTRA_THRES	**Sets up BSDMA gultra threshold** Useful if the corresponding ultra enable bit is set.
7:0	BSDMA_PREULTRA_THRES	**Sets up BSDMA gpreultra threshold** Useful if the corresponding preultra enable bit is set.

1700331C JPGENC_LATENCY_THRES **JPEG Encoder Latency Threshold Control Register** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDMA_LATENCY_EN	BSDMA_LATENCY_EN														
Type	RW	RW														
Reset	0	0														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDMA_LATENCY_THRES								BSDMA_LATENCY_THRES							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	RDMA_LATENCY_EN	Set it to 1 to enable RDMA latency request control.
30	BSDMA_LATENCY_EN	Set it to 1 to enable BSDMA latency requset control.
15:8	RDMA_LATENCY_THRES	Sets up RDMA latency threshold
7:0	BSDMA_LATENCY_THRES	Sets up BSDMA latency threshold

17003400 JPGENC_IRQ_EN **JPEG Encoder IRQ Enable Control Register** **00000007**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CMDQ_EN															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														IRQ_EN		
Type														WO		
Reset														1	1	1

Bit(s)	Name	Description
31	CMDQ_EN	**Set it to 1 to enable frame done signal to command queue.**
2:0	IRQ_EN	**Set it to 1 to enable each IRQ status** bit[0]: Error bit[1]: Stall bit[2]: Encoding done When using command queue, set bit[2] to 0.

4.6 JPEG Decoder

Module name: jpgdec Base address: (+17004000h)

Address	Name	Width	Register Function
17004090	JPGDEC_RESET	32	JPEG Decoder Reset Register
170040F8	JPGDEC_BRZ_FACTOR	32	JPEG Decode Block ReSize Factor
170040FC	JPGDEC_DU_NUM	32	JPEG Decode DU Number for Each Component
1700412C	JPGDEC_DCT_DEBUG	32	JPEG Decoder Debug Register
17004130	JPGDEC_CHKSUM0	32	JPEG Decoder Checksum 0
17004134	JPGDEC_CHKSUM1	32	JPEG Decoder Checksum 1
17004140	JPGDEC_DEST_ADDR0_Y	32	JPEG Decode Y Base Address
17004144	JPGDEC_DEST_ADDR0_U	32	JPEG Decode U Base Address
17004148	JPGDEC_DEST_ADDR0_V	32	JPEG Decode V Base Address
1700414C	JPGDEC_DEST_ADDR1_Y	32	JPEG Decode Y Base Address
17004150	JPGDEC_DEST_ADDR1_U	32	JPEG Decode U Base Address
17004154	JPGDEC_DEST_ADDR1_V	32	JPEG Decode V Base Address
17004158	JPGDEC_STRIDE_Y	32	JPEG Decode Y Plane Memory Stride
1700415C	JPGDEC_STRIDE_UV	32	JPEG Decode U or V Plane Memory Stride
17004160	JPGDEC_IMG_STRIDE_Y	32	JPEG Decode Y Plane Image Stride
17004164	JPGDEC_IMG_STRIDE_UV	32	JPEG Decode U or V Plane Image Stride
1700416C	JPGDEC_WDMA_CTRL	32	JPEG Decoder WDMA Control
17004170	JPGDEC_PAUSE_MCU_NUM	32	JPEG Decoder Pause MCU Index
1700417C	JPGDEC_OPERATION_MODE	32	JPEG Decoder Operation Mode
17004180	JPGDEC_DEBUG0	32	JPEG Decoder Debug Register
17004184	JPGDEC_DEBUG1	32	JPEG Decoder Debug Register
17004188	JPGDEC_DEBUG2	32	JPEG Decoder Debug Register
1700418C	JPGDEC_DEBUG3	32	JPEG Decoder Debug Register
17004200	JPGDEC_FILE_ADDR	32	JPEG Decoder File Address Register
1700420C	JPGDEC_COMP_ID	32	JPEG Decoder Component ID Register
17004210	JPGDEC_TOTAL_MCU_NUM	32	JPEG Decoder Total MCU Number Register
17004224	JPGDEC_COMP0_DATA_UNIT_NUM	32	JPEG Decoder Component 0's Data Unit Number Register
1700423C	JPGDEC_DU_CTRL	32	JPEG Decoder Control Register
17004240	JPGDEC_TRIG	32	JPEG Decoder Trigger Register
17004248	JPGDEC_FILE_BRP	32	JPEG Decoder Breakpoint Address Register
1700424C	JPGDEC_FILE_TO	32	JPEG Decoder File Size Register

Address	Name	Width	Register Function
	TAL_SIZE		
17004270	JPGDEC_QT_ID	32	JPEG Decoder Quantization Table ID Register
17004274	JPGDEC_INTERRUPT_STATUS	32	JPEG Decoder Interrupt Status Register
17004278	JPGDEC_STATUS	32	JPEG Decoder FSM Status Register
17004294	JPGDEC_MCU_CNT	32	JPEG VLD Decoded MCU Count Register
17004300	JPGDEC_DCM_CTRL	32	JPEG Decoder DCM Control Register
17004304	JPGDEC_SMI_DEBUG0	32	JPEG Decoder Debug Register
17004308	JPGDEC_SMI_DEBUG1	32	JPEG Decoder Debug Register
1700430C	JPGDEC_SMI_DEBUG2	32	JPEG Decoder Debug Register
17004310	JPGDEC_SMI_DEBUG3	32	JPEG Decoder Debug Register
17004318	JPGDEC_ULTRA_THRES	32	JPEG Decoder Ultra Threshold Control Register
1700431C	JPGDEC_IRQ_EN	32	JPEG Decoder IRQ Enable Control Register
1700432C	JPGENC_LATENCY_THRES	32	JPEG Decoder Latency Threshold Control Register

17004090 JPGDEC_RESET JPEG Decoder Reset Register 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RSTB				
Type												RW				
Reset												1				

Bit(s)	Name	Description
4	RSTB	**JPEG decoder's active-low reset (write only)** After resetting the JPEG decoder, the bit of RSTB should be re-assigned to 1. *Note: Reset the JPEG decoder before decoding each new image. If resetting the decoder during decoding is required, follow the soft reset mechanism. Hard reset may cause unexpected SMI behavior.* 0: Reset mode 1: Normal mode

170040F8 JPGDEC_BRZ_FACTOR JPEG Decode Block ReSize Factor 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			BRZ_FACTOR_UV_V				BRZ_FACTOR_UV_H				BRZ_FACTOR_Y_V				BRZ_FACTOR_Y_H	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0

Bit(s)	Name	Description
13:12	BRZ_FACTOR_UV_V	**Vertical block resize factor for chroma** 2'b00: No resize 2'b01: 1/2 resize horizontally and vertically 2'b10: 1/4 resize horizontally and vertically 2'b11: 1/8 resize horizontally and vertically
9:8	BRZ_FACTOR_UV_H	**Horizontal block resize factor for chroma** 2'b00: No resize 2'b01: 1/2 resize horizontally and vertically 2'b10: 1/4 resize horizontally and vertically 2'b11: 1/8 resize horizontally and vertically
5:4	BRZ_FACTOR_Y_V	**Vertical block resize factor for luma** 2'b00: No resize 2'b01: 1/2 resize horizontally and vertically 2'b10: 1/4 resize horizontally and vertically 2'b11: 1/8 resize horizontally and vertically
1:0	BRZ_FACTOR_Y_H	**Horizontal block resize factor for luma** 2'b00: No resize 2'b01: 1/2 resize horizontally and vertically 2'b10: 1/4 resize horizontally and vertically 2'b11: 1/8 resize horizontally and vertically

170040FC JPGDEC_DU_NUM — **JPEG Decode DU Number for Each Component** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					H_SAMP_0		V_SAMP_0		H_SAMP_1		V_SAMP_1		H_SAMP_2		V_SAMP_2	
Type					RW		RW		RW		RW		RW		RW	
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:10	H_SAMP_0	**Horizontal sampling factor of the 1st component, Y** 2'b00: Sampling factor = 1 2'b01: Sampling factor = 2 2'b10: Invalid 2'b11: Sampling factor = 4
9:8	V_SAMP_0	**Vertical sampling factor of the 1st component, Y** 2'b00: Sampling factor = 1 2'b01: Sampling factor = 2 2'b10: Invalid 2'b11: Sampling factor = 4
7:6	H_SAMP_1	**Horizontal sampling factor of the 2nd component, U** 2'b00: Sampling factor = 1

Bit(s)	Name	Description
		2'b01: Sampling factor = 2 2'b10: Invalid 2'b11: Sampling factor = 4
5:4	V_SAMP_1	**Vertical sampling factor of the 2nd component, U** 2'b00: Sampling factor = 1 2'b01: Sampling factor = 2 2'b10: Invalid 2'b11: Sampling factor = 4
3:2	H_SAMP_2	**Horizontal sampling factor of the 3rd component, V** 2'b00: Sampling factor = 1 2'b01: Sampling factor = 2 2'b10: Invalid 2'b11: Sampling factor = 4
1:0	V_SAMP_2	**Vertical sampling factor of the 3rd component, V** 2'b00: Sampling factor = 1 2'b01: Sampling factor = 2 2'b10: Invalid 2'b11: Sampling factor = 4

1700412C JPGDEC_DCT_DEBUG **JPEG Decoder Debug Register** **00000013**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																ERR
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						STATUS0							STATUS1			
Type						RO							RO			
Reset						0	0	0	0	0	0	1	0	0	1	1

Bit(s)	Name	Description
16	ERR	Indicates if there is VLD error
10:4	STATUS0	DCT core status
3:0	STATUS1	DCT buffer status

17004130 JPGDEC_CHKSUM0 **JPEG Decoder Checksum 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKSUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKSUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CHKSUM	BSDMA checksum register

17004134 JPGDEC_CHKSUM1 JPEG Decoder Checksum 1 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKSUM															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKSUM															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	CHKSUM	WDMA checksum register

17004140 JPGDEC_DEST_ADDR0_Y JPEG Decode Y Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEST_ADDR0_Y															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEST_ADDR0_Y															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEST_ADDR0_Y	**First base address of Y component** Should be 16-byte aligned.

17004144 JPGDEC_DEST_ADDR0_U JPEG Decode U Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEST_ADDR0_U															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEST_ADDR0_U															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEST_ADDR0_U	**First base address of U component** Should be 16-byte aligned.

17004148 JPGDEC_DEST_ADDR0_V JPEG Decode V Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEST_ADDRo_V															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEST_ADDRo_V															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEST_ADDRo_V	**First base address of V component** Should be 16-byte aligned.

1700414C JPGDEC_DEST_ADDR1_Y JPEG Decode Y Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEST_ADDR1_Y															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEST_ADDR1_Y															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEST_ADDR1_Y	**Second base address of Y component** Should be 16-byte aligned. Only used for JPGDEC/GDMA direct couple mode.

17004150 JPGDEC_DEST_ADDR1_U JPEG Decode U Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEST_ADDR1_U															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEST_ADDR1_U															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEST_ADDR1_U	**Second base address of U component** Should be 16-byte aligned. Only used for JPGDEC/GDMA direct couple mode.

17004154 JPGDEC_DEST_ADDR1_V JPEG Decode V Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	DEST_ADDR1_V															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEST_ADDR1_V															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEST_ADDR1_V	**Second base address of V component** Should be 16-byte aligned. Only used for JPGDEC/GDMA direct couple mode.

17004158 JPGDEC_STRIDE_Y **JPEG Decode Y Plane Memory Stride** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				STRIDE_Y												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	STRIDE_Y	**Memory stride of Y component** Should be 16-bytes aligned. Larger than Image_stride_Y = (image_width_Y+15)/16*16. *Note: Only useful in GDMA direct couple mode. Should be equal to image stride in other modes.*

1700415C JPGDEC_STRIDE_UV **JPEG Decode U or V Plane Memory Stride** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				STRIDE_UV												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	STRIDE_UV	**Memory stride of U and V component** Should be 16-bytes aligned. Larger than Image_stride_UV = (image_width_UV+15)/16*16. *Note: Only useful in GDMA direct couple mode. Should be equal to image stride in other modes.*

17004160 JPGDEC_IMG_STRIDE_Y **JPEG Decode Y Plane Image Stride** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				IMG_STRIDE_Y												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	IMG_STRIDE_Y	**Image stride of Y component** Should be 16-bytes aligned. Image_stride_Y = (image_width_Y+15)/16*16

17004164 JPGDEC_IMG_STRIDE_UV **JPEG Decode U or V Plane Image Stride** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				IMG_STRIDE_UV												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	IMG_STRIDE_UV	**Image stride of U and V component** Should be 16-bytes aligned. Image_stride_UV = (image_width_UV+15)/16*16

1700416C JPGDEC_WDMA_CTRL **JPEG Decoder WDMA Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									NUM_MCU_PER_GROUP							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		NUM_GROUP_MCU							NUM_MCU_LAST_GROUP							
Type		RW							RW							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	NUM_MCU_PER_GROUP	**Sets up the number of MCU in each MCU group except for that of last MCU group for write DMA control** NUM_MCU_PER_GROUP = 128/(Y pixel width in one MCU) - 1

Bit(s)	Name	Description
		Here the Y pixel number in one MCU corresponds to that after format conversion and resizing.
14:8	NUM_GROUP_MCU	**Sets up the number of MCU group for write DMA control** NUM_GROUP_MCU = (number of MCU per MCU row + number of MCU per MCU group - 1/number of MCU per MCU group) - 1
7:0	NUM_MCU_LAST_GROUP	**Sets up the number of MCU in last MCU group for write DMA control** NUM_MCU_LAST_GROUP = (Y pixel width in last MCU group)/(Y pixel width in one MCU) - 1. Here the Y pixel number in one MCU corresponds to that after format conversion and resizing.

17004170 JPGDEC_PAUSE_MCU_NUM **JPEG Decoder Pause MCU Index** **03FFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							PAUSE_MCU_NUM									
Type							RW									
Reset							1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAUSE_MCU_NUM															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
25:0	PAUSE_MCU_NUM	**Sets up pause MCU index for pause/resume mode** If stop MCU index is N in this pause/resume interaction, set this value to N-1; N should be the MCU index of MCU row end.

1700417C JPGDEC_OPERATION_MODE **JPEG Decoder Operation Mode** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					ULTRA_CTRL											ERR_DET_DISABLE
Type					RW											RW
Reset					0	0	0	0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RST_INVALID_SKIP							OP_MODE	
Type								RW							RW	
Reset								0							0	0

Bit(s)	Name	Description
27:24	ULTRA_CTRL	**Controls JPEG SMI port ultra option enable** Set it to 1 to enable the corresponding option. bit[27]: WDMA GULTRA

Bit(s)	Name	Description
		bit[26]: WDMA GPREULTRA bit]25]: BSDMA GULTRA bit[24]: BSDMA GPREULTRA
16	ERR_DET_DISABLE	**Disables error detection feature** Set it to 0 to disable error detection.
8	RST_INVALID_SKIP	**Skip invalid restart marker detection** Set it to 1 to skip invalid restart marker detection if necessary.
1:0	OP_MODE	**Sets up JPEG decoder operation mode** 2'b00: Normal mode (full frame mode) 2'b01: Direct couple mode 2'b10: Pause/resume mode 2'b11: Reserved

17004180 JPGDEC_DEBUG0 JPEG Decoder Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				JPGDEC_READY0				JPGDEC_READY1				GDMA_BUSY0				GDMA_BUSY1
Type				RO				RO				RO				RO
Reset				0				0				0				0

Bit(s)	Name	Description
12	JPGDEC_READY0	Debugging information for direct couple mode
8	JPGDEC_READY1	Debugging information for direct couple mode
4	GDMA_BUSY0	Debugging information for direct couple mode
0	GDMA_BUSY1	Debugging information for direct couple mode

17004184 JPGDEC_DEBUG1 JPEG Decoder Debug Register 00000080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GWRSP_CNT_INT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			GWRSP_CNT_INT_OVERFLOW		WDMA_DEBUG				WDMA_BUFFER_STATE				WDMA_MAIN_STATE			
Type			RO		RO				RO				RO			
Reset			0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	GWRSP_CNT_INT	JPEG decoder debugging information
13:12	GWRSP_CNT_INT_OVERFLOW	JPEG decoder debugging information
11:8	WDMA_DEBUG	JPEG decoder debugging information
7:4	WDMA_BUFFER_STATE	JPEG decoder debugging information

Bit(s)	Name	Description
3:0	WDMA_MAIN_STATE	JPEG decoder debugging information

17004188 JPGDEC_DEBUG2 JPEG Decoder Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GWRSP_CNT_SMI															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GWRSP_CNT_SMI															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GWRSP_CNT_SMI	JPEG decoder debugging information

1700418C JPGDEC_DEBUG3 JPEG Decoder Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				EARLY_EOI				INVALID_RST				INVALID_CODE				BLK_OVERFLOW
Type				RO				RO				RO				RO
Reset				0				0				0				0

Bit(s)	Name	Description
12	EARLY_EOI	Debugging information for error detection
8	INVALID_RST	Debugging information for error detection
4	INVALID_CODE	Debugging information for error detection
0	BLK_OVERFLOW	Debugging information for error detection

17004200 JPGDEC_FILE_ADDR JPEG Decoder File Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FILE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FILE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	FILE_ADDR	**JPEG file starting address** This address must be 16-byte aligned. This register's content will be changed by hardware if JPEG decoder has been started. The contents represent the address that has been read. It is suggested that the starting address be set to the location of DQT marker (oxffdb) in the beginning of decoding one JPEG file. Some dummy data (0xff) can be inserted before the JPEG file to help meet the limitation of 16-byte alignment. When the function of breakpoint is enabled, one JPEG file can be divided into several sections and loaded to the memory for decoding individually. In every end of a section, the software should re-program this file address to the start address of the next file section. Any dummy data is not allowed to be inserted in the file content. *Note: Due to DCM implementation, this register can be read only when DCM is disabled.*

1700420C JPGDEC_COMP_ID **JPEG Decoder Component ID Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMP0_ID								COMP1_ID							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMP2_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Name	Description
31:24	COMP0_ID	**1st component (Y) ID extracted from SOF marker** Note: This register should be written before read; otherwise, the return value will be meaningless.
23:16	COMP1_ID	**2nd component (U) ID extracted from SOF marker** Note: This register should be written before read; otherwise, the return value will be meaningless.
15:8	COMP2_ID	**3rd component (V) ID extracted from SOF marker** Note: This register should be written before read; otherwise, the return value will be meaningless.

17004210 JPGDEC_TOTAL_MCU_NUM **JPEG Decoder Total MCU Number Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TOTAL_MCU_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOTAL_MCU_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TOTAL_MCU_NUM	**Total MCU number to be decoded.**

Bit(s)	Name	Description
		If the MCU number is N, program (N-1) into this register. *Note: This register should be written before read; otherwise, the return value will be meaningless.*

17004224 JPGDEC_COMPo_DATA_UNIT_NUM **JPEG Decoder Component 0's Data Unit Number Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMPo_DATA_UNIT_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMPo_DATA_UNIT_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COMPo_DATA_UNIT_NUM	**Component o data unit count** Only effective in grayscale mode. Contains the 8x8 data unit number of the first component in non-interleaved scans. If the data unit number is N, program (N-1) into this register. *Note: This register should be written before read; otherwise, the return value will be meaningless.*

1700423C JPGDEC_DU_CTRL **JPEG Decoder Control Register** **3FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GRAY	GMC_EN	DU_9			DU_8			DU_7			DU_6			DU_5	
Type	RW	RW	RW			RW			RW			RW			RW	
Reset	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DU_5	DU_4			DU_3			DU_2			DU_1			DU_0		
Type	RW	RW			RW			RW			RW			RW		
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	GRAY	**Grayscale mode indicator** 0: Not grayscale 1: Grayscale
30	GMC_EN	**Enables signal for GMC activity** Should be set to 1 before trigger JPEG decoder *Note: Due to DCM implementation, this register can be read only when DCM is disabled.* 0: Disable 1: Enable
29:27	DU_9	**10th data unit component category in MCU** *Note: Due to DCM implementation, this register can be read only when DCM is disabled.* 3'b100: Data unit is Y component. 3'b101: Data unit is U component.

Bit(s)	Name	Description
		3'b110: Data unit is V component. 3'b111: Not used in current frame Others: Invalid
26:24	DU_8	**9th data unit component category in MCU** *Note: Due to DCM implementation, this register can be read only when DCM is disabled.* 3'b100: Data unit is Y component. 3'b101: Data unit is U component. 3'b110: Data unit is V component. 3'b111: Not used in current frame Others: Invalid
23:21	DU_7	**8th data unit component category in MCU** *Note: Due to DCM implementation, this register can be read only when DCM is disabled.* 3'b100: Data unit is Y component. 3'b101: Data unit is U component. 3'b110: Data unit is V component. 3'b111: Not used in current frame Others: Invalid
20:18	DU_6	**7th data unit component category in MCU** *Note: Due to DCM implementation, this register can be read only when DCM is disabled.* 3'b100: Data unit is Y component. 3'b101: Data unit is U component. 3'b110: Data unit is V component. 3'b111: Not used in current frame Others: Invalid
17:15	DU_5	**6th data unit component category in MCU** *Note: Due to DCM implementation, this register can be read only when DCM is disabled.* 3'b100: Data unit is Y component. 3'b101: Data unit is U component. 3'b110: Data unit is V component. 3'b111: Not used in current frame Others: Invalid
14:12	DU_4	**5th data unit component category in MCU** *Note: Due to DCM implementation, this register can be read only when DCM is disabled.* 3'b100: Data unit is Y component. 3'b101: Data unit is U component. 3'b110: Data unit is V component. 3'b111: Not used in current frame Others: Invalid
11:9	DU_3	**4th data unit component category in MCU** *Note: Due to DCM implementation, this register can be read only when DCM is disabled.* 3'b100: Data unit is Y component. 3'b101: Data unit is U component. 3'b110: Data unit is V component. 3'b111: Not used in current frame Others: Invalid
8:6	DU_2	**3rd data unit component category in MCU** *Note: Due to DCM implementation, this register can be read only when DCM is disabled.* 3'b100: Data unit is Y component. 3'b101: Data unit is U component. 3'b110: Data unit is V component.

Bit(s)	Name	Description
		3'b111: Not used in current frame Others: Invalid
5:3	DU_1	**2nd data unit component category in MCU** *Note: Due to DCM implementation, this register can be read only when DCM is disabled.* 3'b100: Data unit is Y component. 3'b101: Data unit is U component. 3'b110: Data unit is V component. 3'b111: Not used in current frame Others: Invalid
2:0	DU_0	**1st data unit component category in MCU** *Note: Due to DCM implementation, this register can be read only when DCM is disabled.* 3'b100: Data unit is Y component. 3'b101: Data unit is U component. 3'b110: Data unit is V component. 3'b111: Not used in current frame Others: Invalid

17004240 JPGDEC_TRIG JPEG Decoder Trigger Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TRIG
Type																WO
Reset																0

Bit(s)	Name	Description
0	TRIG	Write to start JPEG decoder.

17004248 JPGDEC_FILE_BRP JPEG Decoder Breakpoint Address Register FFFFFFF0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	JPEG_FILE_BRP_ADDR															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	JPEG_FILE_BRP_ADDR															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1				

Bit(s)	Name	Description
31:4	JPEG_FILE_BRP_ADDR	**JPGDEC_FILE_BRP stands for 16-byte aligned breakpoint address that hardware will stall once the breakpoint address is encountered.** The data in the current breakpoint address will not be parsed for

Bit(s)	Name	Description
		decoding. This control register provides a solution for software to swap internal memory content with the external memory in case the JPEG source file is too big for the internal memory to store at a time. A breakpoint interrupt will fire when the hardware DMA address hits the breakpoint address. The software can refill the residue bitstream and follow the procedure below to restart the JPEG decoder. 1. Write new breakpoint address to JPGDEC_FILE_BRP register. 2. Write new destination address to JPEG_DEC_FILE_ADDR register. 3. Write JPG_DEC_TRIG register to trigger the decoder.

1700424C JPGDEC_FILE_TOTAL_SIZE **JPEG Decoder File Size Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	JPEG_FILE_TOTAL_SIZE															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	JPEG_FILE_TOTAL_SIZE															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	JPEG_FILE_TOTAL_SIZE	**Size slightly larger than the JPEG source file size in bytes for error file detection** The hardware will fire a file overflow interrupt and stall if this size of bitstream has been read in. *Note: The total size of file must be a multiple of 128 (including initial dummy data). If the total size is not divisible by 128, increase the size value until it is.*

17004270 JPGDEC_QT_ID **JPEG Decoder Quantization Table ID Register** **00000011**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					COMP0_QT_ID				COMP1_QT_ID				COMP2_QT_ID			
Type					RW				RW				RW			
Reset					0	0	0	0	0	0	0	1	0	0	0	1

Bit(s)	Name	Description
11:8	COMP0_QT_ID	Quantization table ID of Y component directly extracted from SOF marker
7:4	COMP1_QT_ID	Quantization table ID of U component directly extracted from SOF marker
3:0	COMP2_QT_ID	Quantization table ID of V component directly extracted from SOF marker

Bit(s)	Name	Description

17004274 JPGDEC_INTERRUPT_STATUS **JPEG Decoder Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ_TYPE															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ERR_IRQ	PAUSE_IRQ		OVFL_IRQ	BRP_IRQ	EOF_IRQ
Type											RW	RW		RW	RW	RW
Reset											0	0		0	0	0

Bit(s)	Name	Description
31	IRQ_TYPE	**IRQ type** 0: Write-clear mode 1: Read-clear mode (if read-clear mode is enabled, this bit must be always set to 1)
5	ERR_IRQ	**Set it to 1 by error interrupt; write 1 to clear interrupt signal (write-clear mode).**
4	PAUSE_IRQ	**Set it to 1 by pause interrupt; write 1 to clear interrupt signal (write-clear mode).**
2	OVFL_IRQ	**Set it to 1 by file overflow interrupt; write 1 to clear interrupt signal (write-clear mode).**
1	BRP_IRQ	**Set it to 1 by breakpoint interrupt; write 1 to clear interrupt signal (write-clear mode).**
0	EOF_IRQ	**Set it to 1 by end of file interrupt; write 1 to clear interrupt signal (write-clear mode).**

17004278 JPGDEC_STATUS **JPEG Decoder FSM Status Register** **88011000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GREQ_EN	FOS	BRPS	EOFS	GMC_IDLE	JPEG_DEC_STATE			HUFF_DEC_STATE					MARKER_PARSER_STATE		
Type	RO	RO	RO	RO	RO	RO			RO					RO		
Reset	1	0	0	0	1	0	0	0	0	0	0	0		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SOS_PARSER_STATE						DHT_PARSER_STATE				DQT_PARSER_STATE		DATA_UNIT_STATE			
Type	RO						RO				RO		RO			
Reset	0	0	0	1			0	0			0	0	0	0	0	0

Bit(s)	Name	Description
31	GREQ_EN	**Indicator for greq port**
30	FOS	**Set it to 1 in overflow condition.**
29	BRPS	**Set it to 1 in breakpoint condition.**
28	EOFS	**Set it to 1 in EOI condition.**
27	GMC_IDLE	**Status of GMC port for JPEG decoder** 0: Active

Bit(s)	Name	Description
		1: Idle
26:24	JPEG_DEC_STATE	**State of JPEG decoder** 0: IDLE 1: DMA_LOAD 2: MARKER_PARSER 3: HUFFMAN_DECODE 4: RST_SRCH 5: RELOAD_PROGR_COEFF 6: WAIT_FOR_IDCT
23:20	HUFF_DEC_STATE	**State of Huffman decoding** 0: IDLE 1: RELOAD_SCAN_START_ADDR 2: RELOAD_EOB_RUN 3: BYPASS_DATA 4: RELOAD_CTRL 5: READ_COEFF 6: HUFF_ADDR_LOGICAL 7: HUFF_ADDR_PHYSICAL 8: EOB_RUN_GEN 9: AMP_CAL A: WAIT_COEFF B: SAVE_SCAN_START_ADDR C: SAVE_EOB_RUN D: SAVE_CTRL E: WAIT_FOR_IDCT
18:16	MARKER_PARSER_STATE	**State of marker parser** 1: SRCH_0xFF 2: MARKER_TYPE_IDEN 3: MARKER_LEN_HIGH 4: MARKER_LEN_LOW 5: MARKER_MISC_INFO_DEC
15:12	SOS_PARSER_STATE	**State of SOS parser** 1: NS 2: COMP_SPEC 3: SS_FIELD 4: SE_FIELD 5: AH_AL_FIELD
9:8	DHT_PARSER_STATE	**State of DHT parser** 0: TC_TH 1:HUFF_SYM_LENGTH 2: HUFF_VAL_COLLECT 3: WRITE_HUFF_VAL
5:4	DQT_PARSER_STATE	**State of DQT parser** 0: PQ_TQ 1: READ_COEFF 2: PROGR_COEFF 3: WRITE_COEFF
3:0	DATA_UNIT_STATE	**State of process data unit** 0: DU0 1: DU1 2: DU2 3: DU3 4: DU4 5: DU5 6: DU6

Bit(s)	Name	Description
		7: DU7 8: DU8 9: DU9

17004294 JPGDEC_MCU_CNT **JPEG VLD Decoded MCU Count Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												MCU_CNT				
Type												RO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MCU_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	MCU_CNT	MCU counts decoded by VLD

17004300 JPGDEC_DCM_CTRL **JPEG Decoder DCM Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																STATUS
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DISABLE
Type																RW
Reset																0

Bit(s)	Name	Description
16	STATUS	0: JPGDEC clock is off 1: JPGDEC clock is on
0	DISABLE	0: Enable JPGDEC DCM (default) 1: Disable JPGDEC DCM

17004304 JPGDEC_SMI_DEBUG0 **JPEG Decoder Debug Register** **10000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG0															
Type	RO															
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG0	JPEG decoder debugging information

17004308 JPGDEC_SMI_DEBUG1 JPEG Decoder Debug Register 10000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG1															
Type	RO															
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG1	JPEG decoder debugging information

1700430C JPGDEC_SMI_DEBUG2 JPEG Decoder Debug Register 02300000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG2															
Type	RO															
Reset	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG2	JPEG decoder debugging information

17004310 JPGDEC_SMI_DEBUG3 JPEG Decoder Debug Register 00040000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG3	JPEG decoder debugging information

17004318 JPGDEC_ULTRA_THRES — **JPEG Decoder Ultra Threshold Control Register** — **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_ULTRA_THRES								WDMA_PREULTRA_THRES							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSDMA_ULTRA_THRES								BSDMA_PREULTRA_THRES							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	WDMA_ULTRA_THRES	**Sets up WDMA gultra threshold** Useful if the corresponding ultra enable bit is set.
23:16	WDMA_PREULTRA_THRES	**Sets up WDMA gpreultra threshold** Useful if the corresponding preultra enable bit is set.
15:8	BSDMA_ULTRA_THRES	**Sets up BSDMA gultra threshold** Useful if the corresponding ultra enable bit is set.
7:0	BSDMA_PREULTRA_THRES	**Sets up BSDMA gpreultra threshold** Useful if the corresponding preultra enable bit is set.

1700431C JPGDEC_IRQ_EN — **JPEG Decoder IRQ Enable Control Register** — **0000017F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CMDQ_EN															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DEBUG_APP_FLAG	DEBUG_BRP_FLAG	IRQ_INT_EN						
Type								RW	RW	RW						
Reset								1	0	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	CMDQ_EN	**Set it to 0 to disable command queue frame done.**
8	DEBUG_APP_FLAG	**Set it to 1 to trun on.**
7	DEBUG_BRP_FLAG	**Set it to 1 to trun on.**
6:0	IRQ_INT_EN	**Enables IRQ** bit[6]: Reserved bit[5]: Enable error detection interrupt bit[4]: Enable decoding pause interrupt bit[2]: Enable overflow interrupt bit[1]: Enable break point interrupt bit[0]: Enable EOF interrupt Note: When not using command queue, set all IRQ enable to 1. When using command queue, set error detection/overflow/breakpoint to 1 and others to 0.

1700432C JPGENC_LATENCY_THRES — **JPEG Decoder Latency Threshold Control Register** — **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA_LATENCY_EN	BSDMA_LATENCY_EN														
Type	RW	RW														
Reset	0	0														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA_LATENCY_THRES								BSDMA_LATENCY_THRES							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	WDMA_LATENCY_EN	
30	BSDMA_LATENCY_EN	
15:8	WDMA_LATENCY_THRES	
7:0	BSDMA_LATENCY_THRES	

4.7 Video Decoder

Module name: VDEC_GCON Base address: (+16000000h)

Address	Name	Width	Register Function
16000000	VDEC_CKEN_SET	32	Clock Enable (Power On) Register (CG Off)
16000004	VDEC_CKEN_CLR	32	Clock Disable (Power Down) Register (CG On)
16000008	VDEC_LARB1_CKEN_SET	32	Clock Enable (Power On) Register (CG Off)
1600000C	VDEC_LARB1_CKEN_CLR	32	Clock Disable (Power Down) Register (CG On)
16000010	VDEC_RESETB	32	Sub-system Reset Control Register
16000014	LARB_RESTB	32	SMI Local Arbiter Reset Control Register
16000018	VDEC_DCM_CON	32	Sub-system DCM Off
1600001C	VDEC_SRAM_CFG	32	Sub-system SRAM Config Register
16000024	SMI_LARB_CFG	32	SMI Larbiter Config Register
16000028	VDEC_BIST_MODE_CFG0	32	VDEC Core MBIST Mode Control Register 0
1600002C	VDEC_BIST_RSTB_CFG	32	VDEC Core MBIST Reset Control Register
16000030	VDEC_BIST_DEBUG_CFG	32	VDEC Core MBIST Debug Control Register
16000034	VDEC_BIST_HOLDB_CFG0	32	VDEC Core MBIST holdb Control Register 0
16000038	VDEC_BIST_BG_CFG	32	VDEC Core MBIST Background Control Register
1600003C	VDEC_BIST_DONE_CFG0	32	VDEC Core MBIST Done Monitor 0
16000040	VDEC_BIST_FAIL_CFG0	32	VDEC Core MBIST Done Failure Status Monitor 0
16000044	VDEC_BIST_FAIL_CFG1	32	VDEC Core MBIST Done Failure Status Monitor 1
160000C0	VDEC_BIST_FAIL_CFG2	32	VDEC Core MBIST Done Failure Status Monitor 2
16000048	VDEC_BIST_MODE_CFG1	32	VDEC Core MBIST Mode Control Register 1
1600004C	VDEC_BIST_HOLDB_CFG1	32	VDEC Core MBIST holdb Control Register 1
16000050	VDEC_BIST_DONE_CFG1	32	VDEC Core MBIST Done Monitor 1
16000054	VDEC_MBIST_BSEL_CFG1	32	VDEC Core MBIST BSEL Config 1
16000058	VDEC_MBIST_BSEL_CFG2	32	VDEC Core MBIST BSEL Config 2
1600005C	VDEC_MBIST_BSEL_CFG3	32	VDEC Core MBIST BSEL Config 3
16000060	VDEC_MBIST_BSEL_CFG4	32	VDEC Core MBIST BSEL Config 4
16000064	VDEC_MBIST_BSEL_CFG5	32	VDEC Core MBIST BSEL Config 5
16000068	VDEC_MBIST_BSEL_CFG6	32	VDEC Core MBIST BSEL Config 6
1600006C	VDEC_MBIST_BSEL_CFG7	32	VDEC Core MBIST BSEL Config 7

Address	Name	Width	Register Function
16000070	VDEC_MBIST_BSEL_CFG8	32	VDEC Core MBIST BSEL Config 8
16000074	VDEC_MBIST_BSEL_CFG9	32	VDEC Core MBIST BSEL Config 9
16000078	VDEC_MBIST_BSEL_CFG10	32	VDEC Core MBIST BSEL Config 10
1600007C	VDEC_MBIST_BSEL_CFG11	32	VDEC Core MBIST BSEL Config 11
16000080	VDEC_MBIST_BSEL_CFG12	32	VDEC Core MBIST BSEL Config 12
16000084	VDEC_MBIST_BSEL_CFG13	32	VDEC Core MBIST BSEL Config 13
16000088	VDEC_MBIST_BSEL_CFG14	32	VDEC Core MBIST BSEL Config 14
1600008C	VDEC_MBIST_BSEL_CFG15	32	VDEC Core MBIST BSEL Config 15
16000090	VDEC_MBIST_BSEL_CFG16	32	VDEC Core MBIST BSEL Config 16
16000094	VDEC_MBIST_BSEL_CFG17	32	VDEC Core MBIST BSEL Config 17
16000098	VDEC_MBIST_BSEL_CFG18	32	VDEC Core MBIST BSEL Config 18
1600009C	VDEC_MBIST_BSEL_CFG19	32	VDEC Core MBIST BSEL Config 19
160000A0	VDEC_MBIST_BSEL_CFG20	32	VDEC Core MBIST BSEL Config 20
160000A4	VDEC_MBIST_BSEL_CFG21	32	VDEC Core MBIST BSEL Config 21
160000A8	VDEC_MBIST_BSEL_CFG22	32	VDEC Core MBIST BSEL Config 22
160000AC	VDEC_MBIST_BSEL_CFG23	32	VDEC Core MBIST BSEL Config 23
160000B0	VDEC_MBIST_BSEL_CFG24	32	VDEC Core MBIST BSEL Config 24
160000B4	VDEC_MBIST_BSEL_CFG25	32	VDEC Core MBIST BSEL Config 25
160000B8	VDEC_MBIST_BSEL_CFG26	32	VDEC Core MBIST BSEL Config 26
160000BC	VDEC_MBIST_BSEL_CFG27	32	VDEC Core MBIST BSEL Config 27
160000C4	VDEC_MBIST_BSEL_CFG28	32	VDEC Core MBIST BSEL Config 28
160000F0	VDEC_BIST_SCAN_SEL_CFG	32	VDEC BIST Scan SEL Config
160000F4	VDEC_BIST_FAIL_SEL_CFG	32	VDEC BIST Fail SEL Config
16000104	VDEC_EMI_SYS_MODE_CFG	32	VDEC SMI SYS Mode Config
1600010C	VDEC_AXI_ASIF_CFG0	32	VDEC AXI ASIG CONFIG0 Register
16000110	VDEC_AXI_ASIF_CFG1	32	VDEC AXI ASIG CONFIG1 Register
16000114	VDEC_EMI_PDN_CTRL	32	VDEC EMI Power Down Control Register

Address	Name	Width	Register Function
16000118	MEMOFF_DLY_RSTB_CON	32	MEMOFF DLY RESET BAR Control Register
1600011C	VDEC_CBIP_CFG	32	VDEC CBIP Control Register
16000120	VDEC_CBIP_MON	32	VDEC CBIP Monitor Register

16000000 VDEC_CKEN_SET **Clock Enable (Power On) Register (CG Off)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								VDEC_CKEN_ENG				VDEC_ACTIVE				VDEC_CKEN
Type								RU				RW				RW
Reset								0				0				0

Bit(s)	Name	Description
8	VDEC_CKEN_ENG	0: No effect 1: Enable clock
4	VDEC_ACTIVE	
0	VDEC_CKEN	0: No effect 1: Enable clock

16000004 VDEC_CKEN_CLR **Clock Disable (Power Down) Register (CG On)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								VDEC_CKEN_ENG				VDEC_ACTIVE_CLR				VDEC_PDN
Type								RU				RW				RW
Reset								0				0				0

Bit(s)	Name	Description
8	VDEC_CKEN_ENG	0: No effect 1: Enable clock
4	VDEC_ACTIVE_CLR	
0	VDEC_PDN	0: No effect 1: Disable clock

16000008 VDEC_LARB1_CKEN_SET **Clock Enable (Power On) Register (CG Off)** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																LARB1_CKEN
Type																RW
Reset																1

Bit(s)	Name	Description
0	LARB1_CKEN	0: No effect 1: Enable clock

1600000C VDEC_LARB1_CKEN_CLR **Clock Disable (Power Down) Register (CG On)** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																LARB1_PDN
Type																RW
Reset																1

Bit(s)	Name	Description
0	LARB1_PDN	0: No effect 1: Disable clock

16000010 VDEC_RESETB **Sub-system Reset Control Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VDEC_RESETB
Type																RW
Reset																1

Bit(s)	Name	Description
0	VDEC_RESETB	0: Reset the entire VDEC system (including MBIST registers)

Bit(s)	Name	Description
		(Reset is low active. Remember to set it back to 1 for VDEC sub-system to work again.) 1: Does nothing to reset net

16000014 LARB_RESTB **SMI Local Arbiter Reset Control Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																LARB_RESTB
Type																RW
Reset																1

Bit(s)	Name	Description
0	LARB_RESTB	0: Reset the entire LARB1 system 1: Does nothing to reset net

16000018 VDEC_DCM_CON **Sub-system DCM Off** **00000010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												vdec_dec_err_dcm_off				vdec_hw_dcm_off
Type												RW				RW
Reset												1				0

Bit(s)	Name	Description
4	vdec_dec_err_dcm_off	0: ERR_DCM on 1: ERR_DCM off
0	vdec_hw_dcm_off	0: DCM on 1: DCM off

1600001C VDEC_SRAM_CFG **Sub-system SRAM Config Register** **0AAAAAAA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					s_hvt_b512m16_del sel				s_hvt_b64m4_s_del sel				s_hvt_b64m4_delse l			
Type					RW				RW				RW			

Reset					1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	t_rvt_b512m1_dels el				s_hvt_b512m4_dels el				s_hvt_b512m2_dels el				s_hvt_b512m2_l_de lsel			
Type	RW				RW				RW				RW			
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Name	Description
27:24	s_hvt_b512m16_delsel	Configures SRAM DELSEL
23:20	s_hvt_b64m4_s_delsel	Configures SRAM DELSEL
19:16	s_hvt_b64m4_delsel	Configures SRAM DELSEL
15:12	t_rvt_b512m1_delsel	Configures SRAM DELSEL
11:8	s_hvt_b512m4_delsel	Configures SRAM DELSEL
7:4	s_hvt_b512m2_delsel	Configures SRAM DELSEL
3:0	s_hvt_b512m2_l_delsel	Configures SRAM DELSEL

16000024 SMI_LARB_CFG — **SMI Larbiter Config Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																smi_larb_stall_cfg
Type																RW
Reset																0

Bit(s)	Name	Description
0	smi_larb_stall_cfg	smi_larb_stall_cfg

16000028 VDEC_BIST_MODE_CFG0 — **VDEC Core MBIST Mode Control Register 0** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VDEC_BIST_MODE_CFG0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDEC_BIST_MODE_CFG0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VDEC_BIST_MODE_CFG0	vdec_bist_mode_cfg0

1600002C VDEC_BIST_RSTB_CFG — **VDEC Core MBIST Reset Control Register** — **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VDEC_BIST_RSTB_CFG
Type																RW
Reset																1

Bit(s)	Name	Description
0	VDEC_BIST_RSTB_CFG	MBIST resetb

16000030 VDEC_BIST_DEBUG_CFG — **VDEC Core MBIST Debug Control Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VDEC_BIST_DEBUG_CFG
Type																RW
Reset																0

Bit(s)	Name	Description
0	VDEC_BIST_DEBUG_CFG	Debugs MBIST

16000034 VDEC_BIST_HOLDB_CFGo — **VDEC Core MBIST holdb Control Register o** — **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VDEC_BIST_HOLDB_CFGo															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDEC_BIST_HOLDB_CFGo															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	VDEC_BIST_HOLDB_CFGo	vdec_bist_bist_holdb_cfgo

16000038 VDEC_BIST_ — **VDEC Core MBIST Background** — **00000000**

BG_CFG **Control Register**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														VDEC_BIST_BG_CFG		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	VDEC_BIST_BG_CFG	MBIST background

1600003C **VDEC_BIST_DONE_CFG0** **VDEC Core MBIST Done Monitor 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VDEC_BIST_DONE_CFG0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDEC_BIST_DONE_CFG0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VDEC_BIST_DONE_CFG0	vdec_bist_done_cfg0

16000040 **VDEC_BIST_FAIL_CFG0** **VDEC Core MBIST Done Failure Status Monitor 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VDEC_BIST_FAIL_CFG0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDEC_BIST_FAIL_CFG0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VDEC_BIST_FAIL_CFG0	vdec_bist_fail_cfg0

16000044 **VDEC_BIST_FAIL_CFG1** **VDEC Core MBIST Done Failure Status Monitor 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VDEC_BIST_FAIL_CFG1															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDEC_BIST_FAIL_CFG1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VDEC_BIST_FAIL_CFG1	vdec_bist_fail_cfg1

160000C0 VDEC_BIST_FAIL_CFG2 — VDEC Core MBIST Done Failure Status Monitor 2 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			VDEC_BIST_FAIL_CFG2													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDEC_BIST_FAIL_CFG2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:0	VDEC_BIST_FAIL_CFG2	vdec_bist_fail_cfg2

16000048 VDEC_BIST_MODE_CFG1 — VDEC Core MBIST Mode Control Register 1 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												VDEC_BIST_MODE_CFG1				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	VDEC_BIST_MODE_CFG1	vdec_bist_mode_cfg1

1600004C VDEC_BIST_HOLDB_CFG1 — VDEC Core MBIST holdb Control Register 1 — 000003FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							VDEC_BIST_HOLDB_CFG1									
Type							RW									

Reset							1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
9:0	VDEC_BIST_HOLDB_CFG1	VDEC_BIST_HOLDB_CFG1

16000050 VDEC_BIST_DONE_CFG1 **VDEC Core MBIST Done Monitor 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							VDEC_BIST_DONE_CFG1									
Type							RU									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	VDEC_BIST_DONE_CFG1	VDEC_BIST_DONE_CFG1

16000054 VDEC_MBIST_BSEL_CFG1 **VDEC Core MBIST BSEL Config 1** **000001FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								mc_hiu_ext2_mbist_bsel								
Type								RW								
Reset								1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
8:0	mc_hiu_ext2_mbist_bsel	mc_hiu_ext2_mbist_bsel

16000058 VDEC_MBIST_BSEL_CFG2 **VDEC Core MBIST BSEL Config 2** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mc_hiu_mbist_bsel															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description

Bit(s)	Name	Description
15:0	mc_hiu_mbist_bsel	mc_hiu_mbist_bsel

1600005C VDEC_MBIST_BSEL_CFG3 **VDEC Core MBIST BSEL Config 3** **003FFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											mc_ibuf2_mbist_bsel					
Type											RW					
Reset											1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mc_ibuf2_mbist_bsel					mc_ibuf_mbist_bsel										
Type	RW					RW										
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
21:11	mc_ibuf2_mbist_bsel	mc_ibuf2_mbist_bsel
10:0	mc_ibuf_mbist_bsel	mc_ibuf_mbist_bsel

16000060 VDEC_MBIST_BSEL_CFG4 **VDEC Core MBIST BSEL Config 4** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mc_qiu_mbist_bsel															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	mc_qiu_mbist_bsel	mc_qiu_mbist_bsel

16000064 VDEC_MBIST_BSEL_CFG5 **VDEC Core MBIST BSEL Config 5** **00000007**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														mc_risc_sram_mbist_bsel		
Type														RW		
Reset														1	1	1

Bit(s)	Name	Description
2:0	mc_risc_sram_mbist_bsel	mc_risc_sram_mbist_bsel

16000068 VDEC_MBIST_BSEL_CFG6 VDEC Core MBIST BSEL Config 6 0000007F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										mc_wp_tbl_mbist_bsel						
Type										RW						
Reset										1	1	1	1	1	1	1

Bit(s)	Name	Description
6:0	mc_wp_tbl_mbist_bsel	mc_wp_tbl_mbist_bsel

1600006C VDEC_MBIST_BSEL_CFG7 VDEC Core MBIST BSEL Config 7 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													vdec_avc_it_tm_mbist_bsel			
Type													RW			
Reset													1	1	1	1

Bit(s)	Name	Description
3:0	vdec_avc_it_tm_mbist_bsel	vdec_avc_it_tm_mbist_bsel

16000070 VDEC_MBIST_BSEL_CFG8 VDEC Core MBIST BSEL Config 8 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									vdec_ds_mix_deblocking_sram_mbist _bsel							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	vdec_ds_mix_deblocking_sram_mbist_bsel	vdec_ds_mix_deblocking_sram_mbist_bsel

16000074 VDEC_MBIST VDEC Core MBIST BSEL Config 000000FF

_BSEL_CFG9 9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									vdec_ds_mix_vld_sram_mbist_bsel							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	vdec_ds_mix_vld_sram_mbist_bsel	vdec_ds_mix_vld_sram_mbist_bsel

16000078 VDEC_MBIST_BSEL_CFG10 VDEC Core MBIST BSEL Config 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									vdec_hevc_it_tm_mbist_bsel							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	vdec_hevc_it_tm_mbist_bsel	vdec_hevc_it_tm_mbist_bsel

1600007C VDEC_MBIST_BSEL_CFG11 VDEC Core MBIST BSEL Config 0000001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												vdec_lat_coef_buf_mbist_bsel				
Type												RW				
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:0	vdec_lat_coef_buf_mbist_bsel	vdec_lat_coef_buf_mbist_bsel

16000080 VDEC_MBIST VDEC Core MBIST BSEL Config 00000007

_BSEL_CFG12

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														vdec_mc_nbm_idxq_mbist_bsel		
Type														RW		
Reset														1	1	1

Bit(s)	Name	Description
2:0	vdec_mc_nbm_idxq_mbist_bsel	vdec_mc_nbm_idxq_mbist_bsel

16000084 VDEC_MBIST_BSEL_CFG13 VDEC Core MBIST BSEL Config 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													vdec_mc_nbm_map_rec_mbist_bsel			
Type													RW			
Reset													1	1	1	1

Bit(s)	Name	Description
3:0	vdec_mc_nbm_map_rec_mbist_bsel	vdec_mc_nbm_map_rec_mbist_bsel

16000088 VDEC_MBIST_BSEL_CFG14 VDEC Core MBIST BSEL Config 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdec_mc_nbm_sram_mbist_bsel															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	vdec_mc_nbm_sram_mbist_bsel	vdec_mc_nbm_sram_mbist_bsel

1600008C VDEC_MBIST_BSEL_CFG15 **VDEC Core MBIST BSEL Config 15** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdec_mc_pp_reorder_mbist_bsel															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	vdec_mc_pp_reorder_mbist_bsel	vdec_mc_pp_reorder_mbist_bsel

16000090 VDEC_MBIST_BSEL_CFG16 **VDEC Core MBIST BSEL Config 16** **0000007F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										vdec_mv_list_sram_mbist_bsel						
Type										RW						
Reset										1	1	1	1	1	1	1

Bit(s)	Name	Description
6:0	vdec_mv_list_sram_mbist_bsel	vdec_mv_list_sram_mbist_bsel

16000094 VDEC_MBIST_BSEL_CFG17 **VDEC Core MBIST BSEL Config 17** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdec_pp_sram_c_mbist_bsel															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	vdec_pp_sram_c_mbist_bsel	vdec_pp_sram_c_mbist_bsel

Bit(s)	Name	Description

16000098 VDEC_MBIST_BSEL_CFG18 **VDEC Core MBIST BSEL Config 18** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdec_pp_sram_y_mbist_bsel															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	vdec_pp_sram_y_mbist_bsel	vdec_pp_sram_y_mbist_bsel

1600009C VDEC_MBIST_BSEL_CFG19 **VDEC Core MBIST BSEL Config 19** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdec_mv_wbuf_sram_mbsit_bsel															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	vdec_mv_wbuf_sram_mbsit_bsel	vdec_mv_wbuf_sram_mbsit_bsel

160000A0 VDEC_MBIST_BSEL_CFG2 **VDEC Core MBIST BSEL Config 20** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdec_pp_out_buf_mbist_bsel															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	vdec_pp_out_buf_mbist_bsel	vdec_pp_out_buf_mbist_bsel

Bit(s)	Name	Description

160000A4 VDEC_MBIST_BSEL_CFG21 VDEC Core MBIST BSEL Config 21 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									vdec_vld_errmap_mbist_bsel							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	vdec_vld_errmap_mbist_bsel	vdec_vld_errmap_mbist_bsel

160000A8 VDEC_MBIST_BSEL_CFG22 VDEC Core MBIST BSEL Config 22 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdec_ufo_dec_buf_mbist_bsel															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	vdec_ufo_dec_buf_mbist_bsel	vdec_ufo_dec_buf_mbist_bsel

160000AC VDEC_MBIST_BSEL_CFG23 VDEC Core MBIST BSEL Config 23 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdec_ufo_enc_buf_mbist_bsel															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	vdec_ufo_enc_buf_mbist_bsel	vdec_ufo_enc_buf_mbist_bsel

160000B0 VDEC_MBIST_BSEL_CFG24 **VDEC Core MBIST BSEL Config 24** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdec_vld_avc_cabac_context_sram_mbist_bsel															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	vdec_vld_avc_cabac_context_sram_mbist_bsel	vdec_vld_avc_cabac_context_sram_mbist_bsel

160000B4 VDEC_MBIST_BSEL_CFG25 **VDEC Core MBIST BSEL Config 25** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdec_vld_bus_int_unit_sram_mbist_bsel															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	vdec_vld_bus_int_unit_sram_mbist_bsel	vdec_vld_bus_int_unit_sram_mbist_bsel

160000B8 VDEC_MBIST_BSEL_CFG26 **VDEC Core MBIST BSEL Config 26** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdec_vld_ctx_sram_mbist_bsel															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	vdec_vld_ctx_sram_mbist_bsel	vdec_vld_ctx_sram_mbist_bsel

160000BC VDEC_MBIST_BSEL_CFG27 — **VDEC Core MBIST BSEL Config 27** — **00000003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**vdec_vld_hevc_is_ext_sram_mbsit_bsel**	
Type															RW	
Reset															1	1

Bit(s)	Name	Description
1:0	vdec_vld_hevc_is_ext_sram_mbsit_bsel	vdec_vld_hevc_is_ext_sram_mbsit_bsel

160000C4 VDEC_MBIST_BSEL_CFG28 — **VDEC Core MBIST BSEL Config 28** — **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**vdec_vld_hevc_is_sram_mbist_bsel**							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	vdec_vld_hevc_is_sram_mbist_bsel	vdec_vld_hevc_is_sram_mbist_bsel

160000F0 VDEC_BIST_SCAN_SEL_CFG — **VDEC BIST Scan SEL Config** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										mbist_scan_select_cfg						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	mbist_scan_select_cfg	No use

160000F4 VDEC_BIST_FAIL_SEL_CFG — VDEC BIST Fail SEL Config — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										mbist_fail_select_cfg						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	mbist_fail_select_cfg	Selects mbist fail

16000104 VDEC_EMI_SYS_MODE_CFG — VDEC SMI SYS Mode Config — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								smi_sys_mode_cfg								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	smi_sys_mode_cfg	**Configures EMI/SYS selection** 0: Select EMI path 1: Select SYSRAM path

1600010C VDEC_AXI_ASIF_CFG0 — VDEC AXI ASIG CONFIG0 Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	axi_asif_cfg_reg_wd															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	axi_asif_cfg_reg_wd															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	axi_asif_cfg_reg_wd	larb1_ax_asif config regsiter for write

16000110 VDEC_AXI_ASIF_CFG1 — VDEC AXI ASIG CONFIG1 Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	axi_asif_cfg_reg_rd															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	axi_asif_cfg_reg_rd															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	axi_asif_cfg_reg_rd	larb1_ax_asif config regsiter for read

16000114 VDEC_EMI_PDN_CTRL — VDEC EMI Power Down Control Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																disable_emi_power_down_ctrl
Type																RW
Reset																0

Bit(s)	Name	Description
0	disable_emi_power_down_ctrl	Disables vdec_req for emi_power_down_ctrl

16000118 MEMOFF_DLY_RSTB_CON — MEMOFF DLY RESET BAR Control Register — 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																memoff_dly_cken_rstb
Type																RW
Reset																1

Bit(s)	Name	Description
0	memoff_dly_cken_rstb	Reset for memoff_dly module

1600011C VDEC_CBIP_CFG — VDEC CBIP Control Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																vdec_single_en
Type																RW
Reset																0

Bit(s)	Name	Description
0	vdec_single_en	CBIP control register

16000120 VDEC_CBIP_MON — VDEC CBIP Monitor Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															vdec_cbip_s2p_idle	vdec_cbip_s2s_idle
Type															RU	RU
Reset															0	0

Bit(s)	Name	Description
1	vdec_cbip_s2p_idle	vdec_cbip_s2p_idle
0	vdec_cbip_s2s_idle	vdec_cbip_s2s_idle

4.8 H.264/HEVC Video Encoder

Module name: VENC_dcm_cg Base address: (+17002000h)

Address	Name	Width	Register Function
170020EC	VENC_CE	32	VIDEO_CE
170020F4	VENC_CLK_DCM_CTRL	32	VIDEO_CLK_DCM_CTRL
170020FC	VENC_CLK_CG_CTRL	32	VIDEO_CLK_CG_CTRL

170020EC VENC_CE VIDEO_CE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CE
Type																RW
Reset																0

Bit(s)	Name	Description
0	CE	**Enables VENC chip** 1'b1: Aall VENC internal registers can be written and operated. 1'b0: VENC is stall and no data can be read from local bus decoder except MMR.

170020F4 VENC_CLK_DCM_CTRL VIDEO_CLK_DCM_CTRL 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DCM_STATUS															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CLK_DCM_CTRL
Type																RW
Reset																1

Bit(s)	Name	Description
31	DCM_STATUS	**Use 1-bit to enable VENC DCM mechanism** 1'b0 : Disable DCM management (All clock source will work at all time.) 1'b1 : Sequencer will trun off internal venc clock when frame encoding is finished.
0	CLK_DCM_CTRL	**Use 1-bit to enable VENC DCM mechanism** 1'b0 : Disable DCM management (All clock source will work at all time.) 1'b1 : Sequencer will trun off internal venc clock when frame

Bit(s)	Name	Description
		encoding is finished.

170020FC VENC_CLK_CG_CTRL **VIDEO_CLK_CG_CTRL** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLK_CG_CTRL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_CG_CTRL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	CLK_CG_CTRL	**Use 1-bit to enable VENC internal gated clock mechanism** 1'b0 : Disable gated clock (All clock source will work at all time.) 1'b1 : Sequencer will trun off specific clock when the corresponding engine is not under operation.

4.9 MFG

Module name: MFG_TOP Base address: (+13000000h)

Address	Name	Width	Register Function
13000000	MFG_CG_CON	32	MFG Clock Gating Register
13000004	MFG_CG_SET	32	MFG Clock Gating Set Register
13000008	MFG_CG_CLR	32	MFG Clock Gating Clear Register
1300000C	MFG_RESET	32	MFG Reset Register
13000010	MFG_DCM_CON_0	32	MFG DCM Control Register 0
13000014	MFG_APB_DEBUG	32	MFG APB Debug Register
13000018	MFG_APB_DEBUG2	32	MFG APB Debug 2 Register
1300001C	MFG_ASYNC_CON	32	MFG ASYNC_SEL Register
13000020	MFG_SRAM_DELSEL_00	32	MFG_SRAM_DELSEL_00
13000024	MFG_SRAM_DELSEL_01	32	MFG_SRAM_DELSEL_01
13000028	MFG_SRAM_DELSEL_02	32	MFG_SRAM_DELSEL_02
1300002C	MFG_SRAM_DELSEL_03	32	MFG_SRAM_DELSEL_03
13000030	MFG_SRAM_DELSEL_04	32	MFG_SRAM_DELSEL_04
13000034	MFG_SRAM_DELSEL_05	32	MFG_SRAM_DELSEL_05
13000038	MFG_SRAM_DELSEL_06	32	MFG_SRAM_DELSEL_06
1300003C	MFG_SRAM_DELSEL_07	32	MFG_SRAM_DELSEL_07
13000040	MFG_SRAM_DELSEL_08	32	MFG_SRAM_DELSEL_08
13000044	MFG_SRAM_DELSEL_09	32	MFG_SRAM_DELSEL_09
13000048	MFG_SRAM_DELSEL_10	32	MFG_SRAM_DELSEL_10
1300004C	MFG_SRAM_DELSEL_11	32	MFG_SRAM_DELSEL_11
13000050	MFG_SRAM_DELSEL_12	32	MFG_SRAM_DELSEL_12
13000054	MFG_SRAM_DELSEL_13	32	MFG_SRAM_DELSEL_13
13000058	MFG_SRAM_DELSEL_14	32	MFG_SRAM_DELSEL_14
1300005C	MFG_SRAM_DELSEL_15	32	MFG_SRAM_DELSEL_15
13000060	MFG_SRAM_DELSEL_16	32	MFG_SRAM_DELSEL_16
13000064	MFG_SRAM_DELSEL_17	32	MFG_SRAM_DELSEL_17
130000A8	MFG_MBIST_DBG_CON	32	MFG MBIST Debug Register
130000AC	MFG_MBIST_BG	32	MFG MBIST Background Register
130000B0	MFG_GLOBAL_CON	32	MFG Global Control Register
130000B4	MFG_MBIST_HOLD	32	MFG MBIST Holdb Control Register

Address	Name	Width	Register Function
	B		
130000C0	MFG_MBIST_BSEL_0	32	MFG MBIST BSEL Register 0
13000124	MFG_MBIST_DONE_FAIL	32	MFG MBIST Done and Fail Register
13000130	MFG_TIMESTAMP	32	MFG IP Timestamp Register
13000134	MFG_BARRIERDISABLE	32	MFG IP Barrier Disable Register
13000180	MFG_DEBUG_SEL	32	MFG Debug Select Register
13000184	MFG_DEBUG_A	32	MFG Debug Register A
13000188	MFG_DEBUG_B	32	MFG Debug Register B
13000250	MFG_MBIST_MODE_00	32	MFG_MBIST_MODE_00
13000254	MFG_MBIST_MODE_01	32	MFG_MBIST_MODE_01
13000258	MFG_MBIST_MODE_02	32	MFG_MBIST_MODE_02
1300025C	MFG_MBIST_MODE_03	32	MFG_MBIST_MODE_03
13000260	MFG_MBIST_MODE_04	32	MFG_MBIST_MODE_04
13000264	MFG_MBIST_MODE_05	32	MFG_MBIST_MODE_05
13000268	MFG_MBIST_MODE_06	32	MFG_MBIST_MODE_06
1300026C	MFG_MBIST_MODE_07	32	MFG_MBIST_MODE_07
13000270	MFG_MBIST_MODE_08	32	MFG_MBIST_MODE_08
13000274	MFG_MBIST_MODE_09	32	MFG_MBIST_MODE_09
13000278	MFG_MBIST_MODE_10	32	MFG_MBIST_MODE_10
1300027C	MFG_MBIST_MODE_11	32	MFG_MBIST_MODE_11
13000280	MFG_MBIST_MODE_12	32	MFG_MBIST_MODE_12
13000284	MFG_MBIST_MODE_13	32	MFG_MBIST_MODE_13
13000288	MFG_MBIST_MODE_14	32	MFG_MBIST_MODE_14
1300028C	MFG_MBIST_MODE_15	32	MFG_MBIST_MODE_15
13000290	MFG_MBIST_MODE_16	32	MFG_MBIST_MODE_16
13000294	MFG_MBIST_MODE_17	32	MFG_MBIST_MODE_17
13000298	MFG_MBIST_MODE_18	32	MFG_MBIST_MODE_18
1300029C	MFG_MBIST_MODE_19	32	MFG_MBIST_MODE_19
130002A0	MFG_MBIST_MODE_20	32	MFG_MBIST_MODE_20
130002A4	MFG_MBIST_MODE	32	MFG_MBIST_MODE_21

Address	Name	Width	Register Function
	_21		
130002D0	MFG_MBIST_DONE_00	32	MFG_MBIST_DONE_00
130002D4	MFG_MBIST_DONE_01	32	MFG_MBIST_DONE_01
130002D8	MFG_MBIST_DONE_02	32	MFG_MBIST_DONE_02
130002DC	MFG_MBIST_DONE_03	32	MFG_MBIST_DONE_03
130002E0	MFG_MBIST_DONE_04	32	MFG_MBIST_DONE_04
130002E4	MFG_MBIST_DONE_05	32	MFG_MBIST_DONE_05
130002E8	MFG_MBIST_DONE_06	32	MFG_MBIST_DONE_06
130002EC	MFG_MBIST_DONE_07	32	MFG_MBIST_DONE_07
130002F0	MFG_MBIST_DONE_08	32	MFG_MBIST_DONE_08
130002F4	MFG_MBIST_DONE_09	32	MFG_MBIST_DONE_09
130002F8	MFG_MBIST_DONE_10	32	MFG_MBIST_DONE_10
130002FC	MFG_MBIST_DONE_11	32	MFG_MBIST_DONE_11
13000300	MFG_MBIST_DONE_12	32	MFG_MBIST_DONE_12
13000304	MFG_MBIST_DONE_13	32	MFG_MBIST_DONE_13
13000308	MFG_MBIST_DONE_14	32	MFG_MBIST_DONE_14
1300030C	MFG_MBIST_DONE_15	32	MFG_MBIST_DONE_15
13000310	MFG_MBIST_DONE_16	32	MFG_MBIST_DONE_16
13000314	MFG_MBIST_DONE_17	32	MFG_MBIST_DONE_17
13000318	MFG_MBIST_DONE_18	32	MFG_MBIST_DONE_18
1300031C	MFG_MBIST_DONE_19	32	MFG_MBIST_DONE_19
13000320	MFG_MBIST_DONE_20	32	MFG_MBIST_DONE_20
13000324	MFG_MBIST_DONE_21	32	MFG_MBIST_DONE_21
13000350	MFG_MBIST_FAIL_00	32	MFG_MBIST_FAIL_00
13000354	MFG_MBIST_FAIL_01	32	MFG_MBIST_FAIL_01
13000358	MFG_MBIST_FAIL_02	32	MFG_MBIST_FAIL_02
1300035C	MFG_MBIST_FAIL_03	32	MFG_MBIST_FAIL_03
13000360	MFG_MBIST_FAIL	32	MFG_MBIST_FAIL_04

Address	Name	Width	Register Function
	_04		
13000364	MFG_MBIST_FAIL_05	32	MFG_MBIST_FAIL_05
13000368	MFG_MBIST_FAIL_06	32	MFG_MBIST_FAIL_06
1300036C	MFG_MBIST_FAIL_07	32	MFG_MBIST_FAIL_07
13000370	MFG_MBIST_FAIL_08	32	MFG_MBIST_FAIL_08
13000374	MFG_MBIST_FAIL_09	32	MFG_MBIST_FAIL_09
13000378	MFG_MBIST_FAIL_10	32	MFG_MBIST_FAIL_10
1300037C	MFG_MBIST_FAIL_11	32	MFG_MBIST_FAIL_11
13000380	MFG_MBIST_FAIL_12	32	MFG_MBIST_FAIL_12
13000384	MFG_MBIST_FAIL_13	32	MFG_MBIST_FAIL_13
13000388	MFG_MBIST_FAIL_14	32	MFG_MBIST_FAIL_14
1300038C	MFG_MBIST_FAIL_15	32	MFG_MBIST_FAIL_15
13000390	MFG_MBIST_FAIL_16	32	MFG_MBIST_FAIL_16
13000394	MFG_MBIST_FAIL_17	32	MFG_MBIST_FAIL_17
13000398	MFG_MBIST_FAIL_18	32	MFG_MBIST_FAIL_18
1300039C	MFG_MBIST_FAIL_19	32	MFG_MBIST_FAIL_19
130003A0	MFG_MBIST_FAIL_20	32	MFG_MBIST_FAIL_20
130003A4	MFG_MBIST_FAIL_21	32	MFG_MBIST_FAIL_21
130003A8	MFG_MBIST_FAIL_22	32	MFG_MBIST_FAIL_22
130003AC	MFG_MBIST_FAIL_23	32	MFG_MBIST_FAIL_23
130003B0	MFG_MBIST_FAIL_24	32	MFG_MBIST_FAIL_24
130003B4	MFG_MBIST_FAIL_25	32	MFG_MBIST_FAIL_25
130003B8	MFG_MBIST_FAIL_26	32	MFG_MBIST_FAIL_26
130003BC	MFG_MBIST_FAIL_27	32	MFG_MBIST_FAIL_27
130003C0	MFG_MBIST_FAIL_28	32	MFG_MBIST_FAIL_28
130003C4	MFG_MBIST_FAIL_29	32	MFG_MBIST_FAIL_29
130003C8	MFG_MBIST_FAIL_30	32	MFG_MBIST_FAIL_30
130003CC	MFG_MBIST_FAIL	32	MFG_MBIST_FAIL_31

Address	Name	Width	Register Function
	_31		
130003D0	MFG_MBIST_FAIL_32	32	MFG_MBIST_FAIL_32
130003E0	MFG_PERF_EN_00	32	MFG_PERF_EN_00
130003E4	MFG_PERF_EN_01	32	MFG_PERF_EN_01
130003E8	MFG_PERF_EN_02	32	MFG_PERF_EN_02
130003EC	MFG_PERF_EN_03	32	MFG_PERF_EN_03
130003F0	MFG_PERF_EN_04	32	MFG_PERF_EN_04
13000460	MFG_OCP_DCM_CON	32	MFG_OCP_DCM_CON

13000000 MFG_CG_CON **MFG Clock Gating Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BG3D_PDN
Type																RU
Reset																0

Bit(s)	Mnemonic	Name	Description
0		BG3D_PDN	**Controls 3D core clock gating** 0: Turn on 3D core clock 1: Turn off 3D core clock

13000004 MFG_CG_SET **MFG Clock Gating Set Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BG3D_SET
Type																WO
Reset																0

Bit(s)	Mnemonic	Name	Description
0		BG3D_SET	Turns off 3D core clock

13000008 MFG_CG_CLR **MFG Clock Gating Clear Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BG3D_CLR
Type																WO
Reset																0

Bit(s)	Mnemonic	Name	Description
0		BG3D_CLR	Turns on 3D core clock

1300000C MFG_RESET **MFG Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															AXI_RESET	G3D_RESET
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1		AXI_RESET	Resets 3D software
0		G3D_RESET	Resets AXI async

13000010 MFG_DCM_CON_0 **MFG DCM Control Register 0** **0000C03F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															BG3D_DCM_ALL_IDLE_OPT	BG3D_ASYNC_FREE_RUN
Type															RW	RW
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BG3D_DCM_EN	BG3D_DBC_EN	BG3D_FSEL							BG3D_DBC_CNT						
Type	RW	RW	RW							RW						
Reset	1	1	0	0	0	0	0	0		0	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
17		BG3D_DCM_ALL_IDLE_OPT	**Option for DCM all idle**
16		BG3D_ASYNC_FREE_RUN	**Forces AXI async interface to turn on**
15		BG3D_DCM_EN	**Enables core clock DCM**

Bit(s)	Mnemonic	Name	Description
14		BG3D_DBC_EN	**Enables core clock debounce DCM**
13:8		BG3D_FSEL	**Selects core clock frequency** 100000: Divide by 1 010000: Divide by 2 001000: Divide by 4 000100: Divide by 8 000010: Divide by 16 000001: Divide by 32 000000: Divide by 64
6:0		BG3D_DBC_CNT	**Debounce counter**

13000014 MFG_APB_DEBUG **MFG APB Debug Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_ADDR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERR_TIMEOUT															ERR_FLAG_EN
Type	RU															RW
Reset	0															0

Bit(s)	Mnemonic	Name	Description
31:16		ERR_ADDR	APB error address
15		ERR_TIMEOUT	APB error timeout ocurrs
0		ERR_FLAG_EN	Enables APB error flag

13000018 MFG_APB_DEBUG2 **MFG APB Debug 2 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DFP_ERR_ADDR											
Type					RU											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DFP_ERR_TIMEOUT															DFP_CLK_104M_EN
Type	RU															RW
Reset	0															0

Bit(s)	Mnemonic	Name	Description
27:16		DFP_ERR_ADDR	**DFP APB error address**
15		DFP_ERR_TIMEOUT	**DFP APB error timeout ocurrs**
0		DFP_CLK_104M_EN	**DFP 52MHz/104MHz clock selection** 0: DFP uses 52MHz clock 1: DFP uses 104MHz clock

Bit(s)	Mnemonic	Name	Description

1300001C MFG_ASYNC_CON **MFG ASYNC_SEL Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MEM_REG_AR_FCTRL_EN
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MEM_DEPTH_VALUE										MEM_SLV_SEL		MEM_MST_SEL	
Type			RW										RW		RW	
Reset			0	0	0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		MEM_REG_AR_FCTRL_EN	**Enables AXI async IP FCTRL**
13:8		MEM_DEPTH_VALUE	**AXI async IP depth value**
3:2		MEM_SLV_SEL	**Selects async-FIFO depth** 00: Sync delay 1T 01: Sync delay 2T 10: Sync delay 3T 11: Sync delay 3T
1:0		MEM_MST_SEL	**Selects async-FIFO depth** 00: Sync delay 1T 01: Sync delay 2T 10: Sync delay 3T 11: Sync delay 3T

13000020 MFG_SRAM_DELSEL_00 **MFG_SRAM_DELSEL_00** **0000000A**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													MFG_SRAM_DELSEL_GLOBAL			
Type													RW			
Reset													1	0	1	0

Bit(s)	Mnemonic	Name	Description
3:0		MFG_SRAM_DELSEL_GLOBAL	MFG_SRAM_DELSEL for Mali Global

13000024 MFG_SRAM_D **MFG_SRAM_DELSEL_01** **00000AAA**

ELSEL_01

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					MFG_SRAM_DELSEL_CG											
Type					RW											
Reset					1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
11:0		MFG_SRAM_DELSEL_CG	MFG_SRAM_DELSEL for Mali Core Group

13000028 MFG_SRAM_DELSEL_02 MFG_SRAM_DELSEL_02 000000AA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MFG_SRAM_DELSEL_SCo							
Type									RW							
Reset									1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0		MFG_SRAM_DELSEL_SCo	MFG_SRAM_DELSEL for Mali Shader Coreo

1300002C MFG_SRAM_DELSEL_03 MFG_SRAM_DELSEL_03 000000AA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MFG_SRAM_DELSEL_SCo_ARITH							
Type									RW							
Reset									1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0		MFG_SRAM_DELSEL_SCo_ARITH	MFG_SRAM_DELSEL for Mali Shader Coreo ARITH

13000030 MFG_SRAM_DELSEL_04 MFG_SRAM_DELSEL_04 0000000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													MFG_SRAM_DELSEL_SCo_LS			
Type													RW			
Reset													1	0	1	0

Bit(s)	Mnemonic	Name	Description
3:0		MFG_SRAM_DELSEL_SCo_LS	MFG_SRAM_DELSEL for Mali Shader Coreo LS

13000034 MFG_SRAM_DELSEL_05 MFG_SRAM_DELSEL_05 000000AA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MFG_SRAM_DELSEL_SCo_TEX							
Type									RW							
Reset									1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0		MFG_SRAM_DELSEL_SCo_TEX	MFG_SRAM_DELSEL for Mali Shader Coreo TEX

13000038 MFG_SRAM_DELSEL_06 MFG_SRAM_DELSEL_06 000000AA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MFG_SRAM_DELSEL_SC1							
Type									RW							
Reset									1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0		MFG_SRAM_DELSEL_SC1	MFG_SRAM_DELSEL for Mali Shader Core1

1300003C MFG_SRAM_DELSEL_07 MFG_SRAM_DELSEL_07 000000AA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MFG_SRAM_DELSEL_SC1_ARITH							
Type									RW							
Reset									1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0		MFG_SRAM_DELSEL_SC1_ARITH	MFG_SRAM_DELSEL for Mali Shader Core1 ARITH

13000040 MFG_SRAM_DELSEL_08 **MFG_SRAM_DELSEL_08** **0000000A**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													MFG_SRAM_DELSEL_SC1_LS			
Type													RW			
Reset													1	0	1	0

Bit(s)	Mnemonic	Name	Description
3:0		MFG_SRAM_DELSEL_SC1_LS	MFG_SRAM_DELSEL for Mali Shader Core1 LS

13000044 MFG_SRAM_DELSEL_09 **MFG_SRAM_DELSEL_09** **000000AA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MFG_SRAM_DELSEL_SC1_TEX							
Type									RW							
Reset									1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0		MFG_SRAM_DELSEL_SC1_TEX	MFG_SRAM_DELSEL for Mali Shader Core1 TEX

13000048 MFG_SRAM_DELSEL_10 **MFG_SRAM_DELSEL_10** **000000AA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MFG_SRAM_DELSEL_SC2							
Type									RW							
Reset									1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0		MFG_SRAM_DELSEL_SC2	MFG_SRAM_DELSEL for Mali Shader Core2

1300004C MFG_SRAM_DELSEL_11 MFG_SRAM_DELSEL_11 000000AA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MFG_SRAM_DELSEL_SC2_ARITH							
Type									RW							
Reset									1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0		MFG_SRAM_DELSEL_SC2_ARITH	MFG_SRAM_DELSEL for Mali Shader Core2 ARITH

13000050 MFG_SRAM_DELSEL_12 MFG_SRAM_DELSEL_12 0000000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													MFG_SRAM_DELSEL_SC2_LS			
Type													RW			
Reset													1	0	1	0

Bit(s)	Mnemonic	Name	Description
3:0		MFG_SRAM_DELSEL_SC2_LS	MFG_SRAM_DELSEL for Mali Shader Core2 LS

13000054 MFG_SRAM_DELSEL_13 MFG_SRAM_DELSEL_13 000000AA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MFG_SRAM_DELSEL_SC2_TEX							
Type									RW							
Reset									1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0		MFG_SRAM_DELSEL_SC2_TEX	MFG_SRAM_DELSEL for Mali Shader Core2 TEX

13000058 MFG_SRAM_DELSEL_14 **MFG_SRAM_DELSEL_14** **000000AA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MFG_SRAM_DELSEL_SC3							
Type									RW							
Reset									1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0		MFG_SRAM_DELSEL_SC3	MFG_SRAM_DELSEL for Mali Shader Core3

1300005C MFG_SRAM_DELSEL_15 **MFG_SRAM_DELSEL_15** **000000AA**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MFG_SRAM_DELSEL_SC3_ARITH							
Type									RW							
Reset									1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0		MFG_SRAM_DELSEL_SC3_ARITH	MFG_SRAM_DELSEL for Mali Shader Core3 ARITH

13000060 MFG_SRAM_DELSEL_16 **MFG_SRAM_DELSEL_16** **0000000A**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													MFG_SRAM_DELSEL_SC3_LS			
Type													RW			
Reset													1	0	1	0

Bit(s)	Mnemonic	Name	Description
3:0		MFG_SRAM_DELSEL_SC3_LS	MFG_SRAM_DELSEL for Mali Shader Core3 LS

13000064 MFG_SRAM_DELSEL_17 MFG_SRAM_DELSEL_17 000000AA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MFG_SRAM_DELSEL_SC3_TEX							
Type									RW							
Reset									1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0		MFG_SRAM_DELSEL_SC3_TEX	MFG_SRAM_DELSEL for Mali Shader Core3 TEX

130000A8 MFG_MBIST_DBG_CON MFG MBIST Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											MBIST_DONE_SEL					
Type											RW					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					MBIST_FAIL_SEL											MBIST_DBG_EN
Type					RW											RW
Reset					0	0	0	0	0	0	0	0				0

Bit(s)	Mnemonic	Name	Description
21:16		MBIST_DONE_SEL	**Selects MBIST done bus** When this register is set to i, MBIST_DONE_MUX = MBIST_DONE[i] will output to DEBUG.
11:4		MBIST_FAIL_SEL	**Selects MBIST fail bus** When this register is set to i, MBIST_FAIL_MUX = MBIST_FAIL[i] will output to DEBUG.
0		MBIST_DBG_EN	**Enables MBIST debugging for SRAM with diagnosis circuit**

Bit(s)	Mnemonic	Name	Description

130000AC MFG_MBIST_BG — **MFG MBIST Background Register** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														MBIST_BG		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0		MBIST_BG	Selects MBIST background

130000B0 MFG_GLOBAL_CON — **MFG Global Control Register** — **00000003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PSEL_M_GLOBAL_CON_OPT	PSEL_S_GLOBAL_CON_OPT
Type															RW	RW
Reset															1	1

Bit(s)	Mnemonic	Name	Description
1		PSEL_M_GLOBAL_CON_OPT	Option for Master PSEL Global control
0		PSEL_S_GLOBAL_CON_OPT	Option for Slave PSEL Global control

130000B4 MFG_MBIST_HOLDB — **MFG MBIST Holdb Control Register** — **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MBSIT_HOLDB_CON

Type																RW
Reset																1

Bit(s)	Mnemonic	Name	Description
0		MBSIT_HOLDB_CO N	MBIST holdb register 1 for mali SRAM

130000C0 MFG_MBIST_BSEL_0 **MFG MBIST BSEL Register 0** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MBIST_BSEL_0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
15:0		MBIST_BSEL_0	MFG MBIST BSEL register for Mali SRAM

13000124 MFG_MBIST_DONE_FAIL **MFG MBIST Done and Fail Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															MFG_MBIST_FAIL_OR_ALL_X	MFG_MBIST_DONE_AND_ALL_X1
Type															RU	RU
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1		MFG_MBIST_FAIL _OR_ALL_X	MBIST FAIL is OR'ed to one signal
0		MFG_MBIST_DONE _AND_ALL_X1	MBIST DONE is AND'ed to one signal

13000130 MFG_TIMESTAMP **MFG IP Timestamp Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TOP_TSVALUEB_EN
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		TOP_TSVALUEB_E N	Enables Mali Timestamp

13000134 MFG_BARRIERDISABLE MFG IP Barrier Disable Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MALI_T760_BARRIERDISABLE
Type																RW
Reset																1

Bit(s)	Mnemonic	Name	Description
0		MALI_T760_BARR IERDISABLE	Disables ACE barrier

13000180 MFG_DEBUG_SEL MFG Debug Select Register 00000108

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MFG_CRC_CLR				MFG_DEBUG_SEL				
Type								RW				RW				
Reset								1				0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
8		MFG_CRC_CLR	**Clears GPU CRC**
4:0		MFG_DEBUG_SEL	**Selects MFG debugging signals** 5'h0: MBIST 5'h1: IRQ 5'h3: MISC

Bit(s)	Mnemonic	Name	Description

13000184 MFG_DEBUG_A **MFG Debug Register A** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_DEBUG_A															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_DEBUG_A															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_DEBUG_A	MFG DEBUG OUT signals

13000188 MFG_DEBUG_B **MFG Debug Register B** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_DEBUG_B															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_DEBUG_B															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_DEBUG_B	Reserved

13000250 MFG_MBIST_MODE_00 **MFG_MBIST_MODE_00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MBIST_RSTB															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MFG_MBIST_MODE_00
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
31		MBIST_RSTB	Resets MBIST
0		MFG_MBIST_MODE_00	Enables MBIST mode for Mali Global SRAM

13000254 MFG_MBIST_MODE_01 MFG_MBIST_MODE_01 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						MFG_MBIST_MODE_01										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_MODE_01															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26:0		MFG_MBIST_MODE_01	Enables MBIST mode for Mali Core Group SRAM

13000258 MFG_MBIST_MODE_02 MFG_MBIST_MODE_02 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MFG_MBIST_MODE_02												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_MODE_02															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:0		MFG_MBIST_MODE_02	Enables MBIST mode for Mali Shader Core0 SRAM

1300025C MFG_MBIST_MODE_03 MFG_MBIST_MODE_03 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_MODE_03															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_MODE_03															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_MODE_03	Enables MBIST mode for Mali Shader Core0 ARITH0 SRAM

13000260 MFG_MBIST_MODE_04 MFG_MBIST_MODE_04 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MFG_MBIST_MODE_04						
Type											RW						
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		MFG_MBIST_MODE_04	Enables MBIST mode for Mali Shader Core0 ARITH1 SRAM

13000264 MFG_MBIST_MODE_05 MFG_MBIST_MODE_05 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												MFG_MBIST_MODE_05				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_MODE_05															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		MFG_MBIST_MODE_05	Enables MBIST mode for Mali Shader Core0 LS SRAM

13000268 MFG_MBIST_MODE_06 MFG_MBIST_MODE_06 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MFG_MBIST_MODE_06												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_MODE_06															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:0		MFG_MBIST_MODE	Enables MBIST mode for Mali Shader Core0 TEX

Bit(s)	Mnemonic	Name	Description
		_06	SRAM

1300026C MFG_MBIST_MODE_07 MFG_MBIST_MODE_07 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MFG_MBIST_MODE_07												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_MODE_07															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:0		MFG_MBIST_MODE_07	Enables MBIST mode for Mali Shader Core1 SRAM

13000270 MFG_MBIST_MODE_08 MFG_MBIST_MODE_08 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_MODE_08															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_MODE_08															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_MODE_08	Enables MBIST mode for Mali Shader Core1 ARITH0 SRAM

13000274 MFG_MBIST_MODE_09 MFG_MBIST_MODE_09 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MFG_MBIST_MODE_09					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		MFG_MBIST_MODE_09	Enables MBIST mode for Mali Shader Core1 ARITH1 SRAM

Bit(s)	Mnemonic	Name	Description

13000278 MFG_MBIST_MODE_10 MFG_MBIST_MODE_10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												MFG_MBIST_MODE_10				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_MODE_10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		MFG_MBIST_MODE_10	Enables MBIST mode for Mali Shader Core1 LS SRAM

1300027C MFG_MBIST_MODE_11 MFG_MBIST_MODE_11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MFG_MBIST_MODE_11												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_MODE_11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:0		MFG_MBIST_MODE_11	Enables MBIST mode for Mali Shader Core1 TEX SRAM

13000280 MFG_MBIST_MODE_12 MFG_MBIST_MODE_12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MFG_MBIST_MODE_12												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_MODE_12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:0		MFG_MBIST_MODE_12	Enables MBIST mode for Mali Shader Core2 SRAM

13000284 MFG_MBIST_MODE_13 **MFG_MBIST_MODE_13** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_MODE_13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_MODE_13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_MODE_13	Enables MBIST mode for Mali Shader Core2 ARITH0 SRAM

13000288 MFG_MBIST_MODE_14 **MFG_MBIST_MODE_14** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MFG_MBIST_MODE_14					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		MFG_MBIST_MODE_14	Enables MBIST mode for Mali Shader Core2 ARITH1 SRAM

1300028C MFG_MBIST_MODE_15 **MFG_MBIST_MODE_15** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												MFG_MBIST_MODE_15				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_MODE_15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		MFG_MBIST_MODE_15	Enables MBIST mode for Mali Shader Core2 LS SRAM

13000290 MFG_MBIST **MFG_MBIST_MODE_16** **00000000**

MODE_16

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MFG_MBIST_MODE_16												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_MODE_16															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:0		MFG_MBIST_MODE_16	Enables MBIST mode for Mali Shader Core2 TEX SRAM

13000294 MFG_MBIST_MODE_17 MFG_MBIST_MODE_17 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MFG_MBIST_MODE_17												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_MODE_17															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:0		MFG_MBIST_MODE_17	Enables MBIST mode for Mali Shader Core3 SRAM

13000298 MFG_MBIST_MODE_18 MFG_MBIST_MODE_18 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_MODE_18															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_MODE_18															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_MODE_18	Enables MBIST mode for Mali Shader Core3 ARITH0 SRAM

1300029C MFG_MBIST_MODE_19 MFG_MBIST_MODE_19 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MFG_MBIST_MODE_19					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		MFG_MBIST_MODE_19	Enables MBIST mode for Mali Shader Core3 ARITH1 SRAM

130002A0 MFG_MBIST_MODE_20 — MFG_MBIST_MODE_20 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												MFG_MBIST_MODE_20				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_MODE_20															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		MFG_MBIST_MODE_20	Enables MBIST mode for Mali Shader Core3 LS SRAM

130002A4 MFG_MBIST_MODE_21 — MFG_MBIST_MODE_21 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MFG_MBIST_MODE_21												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_MODE_21															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:0		MFG_MBIST_MODE_21	Enables MBIST mode for Mali Shader Core3 TEX SRAM

130002D0 MFG_MBIST_DONE_00 — MFG_MBIST_DONE_00 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MFG_MBIST_DONE_00
Type																RU
Reset																0

Bit(s)	Mnemonic	Name	Description
0		MFG_MBIST_DONE_00	MBIST done for Mali Global

130002D4 MFG_MBIST_DONE_01 MFG_MBIST_DONE_01 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						MFG_MBIST_DONE_01										
Type						RU										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_DONE_01															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26:0		MFG_MBIST_DONE_01	MBIST done for Mali Core Group

130002D8 MFG_MBIST_DONE_02 MFG_MBIST_DONE_02 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MFG_MBIST_DONE_02												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_DONE_02															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:0		MFG_MBIST_DONE_02	MBIST done for Mali Shader Core0

130002DC MFG_MBIST_DONE_03 MFG_MBIST_DONE_03 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	MFG_MBIST_DONE_03															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_DONE_03															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_DONE_03	MBIST done for Mali Shader Core0 ARITH0

130002E0 MFG_MBIST_DONE_04 **MFG_MBIST_DONE_04** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MFG_MBIST_DONE_04						
Type											RU					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		MFG_MBIST_DONE_04	MBIST done for Mali Shader Core0 ARITH1

130002E4 MFG_MBIST_DONE_05 **MFG_MBIST_DONE_05** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												MFG_MBIST_DONE_05				
Type												RU				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_DONE_05															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		MFG_MBIST_DONE_05	MBIST done for Mali Shader Core0 LS

130002E8 MFG_MBIST_DONE_06 **MFG_MBIST_DONE_06** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MFG_MBIST_DONE_06												
Type				RU												

Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_DONE_06															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:0		MFG_MBIST_DONE_06	MBIST done for Mali Shader Core0 TEX

130002EC MFG_MBIST_DONE_07 MFG_MBIST_DONE_07 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MFG_MBIST_DONE_07												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_DONE_07															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:0		MFG_MBIST_DONE_07	MBIST done for Mali Shader Core1

130002F0 MFG_MBIST_DONE_08 MFG_MBIST_DONE_08 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_DONE_08															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_DONE_08															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_DONE_08	MBIST done for Mali Shader Core1 ARITH0

130002F4 MFG_MBIST_DONE_09 MFG_MBIST_DONE_09 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name											MFG_MBIST_DONE_09					
Type											RU					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		MFG_MBIST_DONE_09	MBIST done for Mali Shader Core1 ARITH1

130002F8 MFG_MBIST_DONE_10 **MFG_MBIST_DONE_10** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												MFG_MBIST_DONE_10				
Type												RU				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_DONE_10															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		MFG_MBIST_DONE_10	MBIST done for Mali Shader Core1 LS

130002FC MFG_MBIST_DONE_11 **MFG_MBIST_DONE_11** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MFG_MBIST_DONE_11												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_DONE_11															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:0		MFG_MBIST_DONE_11	MBIST done for Mali Shader Core1 TEX

13000300 MFG_MBIST_DONE_12 **MFG_MBIST_DONE_12** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MFG_MBIST_DONE_12												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_DONE_12															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:0		MFG_MBIST_DONE_12	MBIST done for Mali Shader Core2

13000304 MFG_MBIST_DONE_13 MFG_MBIST_DONE_13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_DONE_13															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_DONE_13															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_DONE_13	MBIST done for Mali Shader Core2 ARITH0

13000308 MFG_MBIST_DONE_14 MFG_MBIST_DONE_14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MFG_MBIST_DONE_14					
Type											RU					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		MFG_MBIST_DONE_14	MBIST done for Mali Shader Core2 ARITH1

1300030C MFG_MBIST_DONE_15 MFG_MBIST_DONE_15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												MFG_MBIST_DONE_15				
Type												RU				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_DONE_15															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		MFG_MBIST_DONE_15	MBIST done for Mali Shader Core2 LS

13000310 MFG_MBIST_DONE_16 MFG_MBIST_DONE_16 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MFG_MBIST_DONE_16												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_DONE_16															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:0		MFG_MBIST_DONE_16	MBIST done for Mali Shader Core2 TEX

13000314 MFG_MBIST_DONE_17 MFG_MBIST_DONE_17 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MFG_MBIST_DONE_17												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_DONE_17															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:0		MFG_MBIST_DONE_17	MBIST done for Mali Shader Core3

13000318 MFG_MBIST_DONE_18 MFG_MBIST_DONE_18 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_DONE_18															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_DONE_18															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_DONE	MBIST done for Mali Shader Core3 ARITH0

Bit(s)	Mnemonic	Name	Description
		_18	

1300031C MFG_MBIST_DONE_19 **MFG_MBIST_DONE_19** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MFG_MBIST_DONE_19					
Type											RU					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		MFG_MBIST_DONE_19	MBIST done for Mali Shader Core3 ARITH1

13000320 MFG_MBIST_DONE_20 **MFG_MBIST_DONE_20** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												MFG_MBIST_DONE_20				
Type												RU				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_DONE_20															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		MFG_MBIST_DONE_20	MBIST done for Mali Shader Core3 LS

13000324 MFG_MBIST_DONE_21 **MFG_MBIST_DONE_21** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				MFG_MBIST_DONE_21												
Type				RU												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_DONE_21															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:0		MFG_MBIST_DONE_21	MBIST done for Mali Shader Core3 TEX

Bit(s)	Mnemonic	Name	Description

13000350 MFG_MBIST_FAIL_00 **MFG_MBIST_FAIL_00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															MFG_MBIST_FAIL_00	
Type															RU	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0		MFG_MBIST_FAIL_00	MBIST fail for Mali Global

13000354 MFG_MBIST_FAIL_01 **MFG_MBIST_FAIL_01** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_FAIL_01															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_FAIL_01															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_FAIL_01	MBIST fail for Mali Core Group

13000358 MFG_MBIST_FAIL_02 **MFG_MBIST_FAIL_02** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_FAIL_02															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_FAIL_02															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_FAIL_02	MBIST fail for Mali Core Group

Bit(s)	Mnemonic	Name	Description

1300035C MFG_MBIST_FAIL_03 **MFG_MBIST_FAIL_03** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_FAIL_03															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_FAIL_03															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_FAIL_03	MBIST fail for Mali Core Group

13000360 MFG_MBIST_FAIL_04 **MFG_MBIST_FAIL_04** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					MFG_MBIST_FAIL_04											
Type					RU											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0		MFG_MBIST_FAIL_04	MBIST fail for Mali Core **Group**

13000364 MFG_MBIST_FAIL_05 **MFG_MBIST_FAIL_05** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_FAIL_05															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_FAIL_05															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_FAIL_05	MBIST fail for Mali Shader Coreo

13000368 MFG_MBIST_FAIL_06 **MFG_MBIST_FAIL_06** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MFG_MBIST_FAIL_06								
Type								RU								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		MFG_MBIST_FAIL_06	MBIST fail for Mali Shader Core0

1300036C MFG_MBIST_FAIL_07 **MFG_MBIST_FAIL_07** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_FAIL_07															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_FAIL_07															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_FAIL_07	MBIST fail for Mali Shader Core0 ARITH0

13000370 MFG_MBIST_FAIL_08 **MFG_MBIST_FAIL_08** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MFG_MBIST_FAIL_08					
Type											RU					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		MFG_MBIST_FAIL_08	MBIST fail for Mali Shader Core0 ARITH1

13000374 MFG_MBIST_FAIL_09 MFG_MBIST_FAIL_09 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									MFG_MBIST_FAIL_09							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_FAIL_09															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		MFG_MBIST_FAIL_09	MBIST fail for Mali Shader Core0 LS

13000378 MFG_MBIST_FAIL_10 MFG_MBIST_FAIL_10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_FAIL_10															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_FAIL_10															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_FAIL_10	MBIST fail for Mali Shader Core0 TEX0

1300037C MFG_MBIST_FAIL_11 MFG_MBIST_FAIL_11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															MFG_MBIST_FAIL_11	
Type															RU	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0		MFG_MBIST_FAIL_11	MBIST fail for Mali Shader Core0 TEX1

13000380 MFG_MBIST_FAIL_12 MFG_MBIST_FAIL_12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_FAIL_12															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_FAIL_12															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_FAIL_12	MBIST fail for Mali Shader Core1

13000384 MFG_MBIST_FAIL_13 **MFG_MBIST_FAIL_13** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MFG_MBIST_FAIL_13								
Type								RU								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		MFG_MBIST_FAIL_13	MBIST fail for Mali Shader Core1

13000388 MFG_MBIST_FAIL_14 **MFG_MBIST_FAIL_14** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_FAIL_14															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_FAIL_14															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_FAIL_14	MBIST fail for Mali Shader Core1 ARITH0

1300038C MFG_MBIST_FAIL_15 **MFG_MBIST_FAIL_15** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MFG_MBIST_FAIL_15					
Type											RU					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		MFG_MBIST_FAIL _15	MBIST fail for Mali Shader Core1 ARITH1

13000390 MFG_MBIST_FAIL_16 **MFG_MBIST_FAIL_16** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									MFG_MBIST_FAIL_16							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_FAIL_16															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		MFG_MBIST_FAIL _16	MBIST fail for Mali Shader Core1 LS

13000394 MFG_MBIST_FAIL_17 **MFG_MBIST_FAIL_17** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_FAIL_17															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_FAIL_17															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_FAIL _17	MBIST fail for Mali Shader Core1 TEX0

13000398 MFG_MBIST_FAIL_18 **MFG_MBIST_FAIL_18** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name															MFG_MBIST_FAIL_18	
Type															RU	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0		MFG_MBIST_FAIL_18	MBIST fail for Mali Shader Core1 TEX1

1300039C MFG_MBIST_FAIL_19 MFG_MBIST_FAIL_19 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_FAIL_19															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_FAIL_19															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_FAIL_19	MBIST fail for Mali Shader Core2

130003A0 MFG_MBIST_FAIL_20 MFG_MBIST_FAIL_20 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MFG_MBIST_FAIL_20								
Type								RU								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		MFG_MBIST_FAIL_20	MBIST fail for Mali Shader Core2

130003A4 MFG_MBIST_FAIL_21 MFG_MBIST_FAIL_21 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_FAIL_21															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_FAIL_21															

Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_FAIL_21	MBIST fail for Mali Shader Core2 ARITH0

130003A8 MFG_MBIST_FAIL_22 MFG_MBIST_FAIL_22 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MFG_MBIST_FAIL_22					
Type											RU					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		MFG_MBIST_FAIL_22	MBIST fail for Mali Shader Core2 ARITH1

130003AC MFG_MBIST_FAIL_23 MFG_MBIST_FAIL_23 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									MFG_MBIST_FAIL_23							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_FAIL_23															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		MFG_MBIST_FAIL_23	MBIST fail for Mali Shader Core2 LS

130003B0 MFG_MBIST_FAIL_24 MFG_MBIST_FAIL_24 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_FAIL_24															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_FAIL_24															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_FAIL_24	MBIST fail for Mali Shader Core2 TEX0

130003B4 MFG_MBIST_FAIL_25 **MFG_MBIST_FAIL_25** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															MFG_MBIST_FAIL_25	
Type															RU	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0		MFG_MBIST_FAIL_25	MBIST fail for Mali Shader Core2 TEX1

130003B8 MFG_MBIST_FAIL_26 **MFG_MBIST_FAIL_26** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_FAIL_26															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_FAIL_26															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_FAIL_26	MBIST fail for Mali Shader Core3

130003BC MFG_MBIST_FAIL_27 **MFG_MBIST_FAIL_27** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MFG_MBIST_FAIL_27								
Type								RU								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8:0		MFG_MBIST_FAIL_27	MBIST fail for Mali Shader Core3

130003C0 MFG_MBIST_FAIL_28 **MFG_MBIST_FAIL_28** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_FAIL_28															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_FAIL_28															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_FAIL_28	MBIST fail for Mali Shader Core3 ARITH0

130003C4 MFG_MBIST_FAIL_29 **MFG_MBIST_FAIL_29** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MFG_MBIST_FAIL_29					
Type											RU					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		MFG_MBIST_FAIL_29	MBIST fail for Mali Shader Core3 ARITH1

130003C8 MFG_MBIST_FAIL_30 **MFG_MBIST_FAIL_30** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									MFG_MBIST_FAIL_30							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_FAIL_30															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		MFG_MBIST_FAIL	MBIST fail for Mali Shader Core3 LS

Bit(s)	Mnemonic	Name	Description
		_30	

130003CC MFG_MBIST_FAIL_31 — MFG_MBIST_FAIL_31 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MFG_MBIST_FAIL_31															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_MBIST_FAIL_31															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MFG_MBIST_FAIL_31	MBIST fail for Mali Shader Core3 TEX0

130003D0 MFG_MBIST_FAIL_32 — MFG_MBIST_FAIL_32 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															MFG_MBIST_FAIL_32	
Type															RU	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0		MFG_MBIST_FAIL_32	MBIST fail for Mali Shader Core3 TEX1

130003E0 MFG_PERF_EN_00 — MFG_PERF_EN_00 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							MFG_PERF_EN_00									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
9:0		MFG_PERF_EN_00	

Bit(s)	Mnemonic	Name	Description

130003E4 MFG_PERF_EN_01 MFG_PERF_EN_01 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								MFG_PERF_EN_01								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_PERF_EN_01															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:0		MFG_PERF_EN_01	

130003E8 MFG_PERF_EN_02 MFG_PERF_EN_02 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								MFG_PERF_EN_02								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_PERF_EN_02															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:0		MFG_PERF_EN_02	

130003EC MFG_PERF_EN_03 MFG_PERF_EN_03 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								MFG_PERF_EN_03								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_PERF_EN_03															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:0		MFG_PERF_EN_03	

130003F0 MFG_PERF_EN_04 MFG_PERF_EN_04 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								MFG_PERF_EN_04								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MFG_PERF_EN_04															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24:0		MFG_PERF_EN_04	

13000460 MFG_OCP_DCM_CON MFG_OCP_DCM_CON 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MFG_OCP_DCM_CON
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		MFG_OCP_DCM_CON	Enable OCP DCM

4.10 SENINF_TOP (Sensor Interface)

Module name: seninf_top Base address: (+1a040000h)

Address	Name	Width	Register Function
1A040000	SENINF_TOP_CTRL	32	SENINF Top Control Register
1A040004	SENINF_TOP_CMODEL_PAR	32	SENINF Top C model Register
1A040008	SENINF_TOP_MUX_CTRL	32	SENINF Top Mux Control Register
1A040010	SENINF_TOP_CAM_MUX_CTRL	32	SENINF Top Cam Mux Control Register
1A040014	SENINF_TOP_N3D_A_CTL	32	SENINF Top N3D_A Control Register
1A040018	SENINF_TOP_N3D_B_CTL	32	SENINF Top N3D_B Control Register

1A040000 SENINF_TOP_CTRL SENINF Top Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		SENINF_TOP_DBG_SEL														SENINF_TOP_N3D_SW_RST
Type		RW														RW
Reset		0	0	0												0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SENINF2_PCLK_EN	SENINF1_PCLK_EN	SENINF2_PCLK_SEL	SENINF1_PCLK_SEL								
Type					RW	RW	RW	RW								
Reset					0	0	0	0								

Bit(s)	Name	Description
30:28	SENINF_TOP_DBG_SEL	0: SENINF1 1: SENINF2 2: SENINF3 3: SENINF4 4: SENINF5
16	SENINF_TOP_N3D_SW_RST	**N3D software reset, active high** 0: De-assert reset 1: Assert reset
11	SENINF2_PCLK_EN	**Enables parallel sensor clock** 0: Gated 1: Not gated
10	SENINF1_PCLK_EN	**Enables parallel sensor clock** 0: Gated 1: Not gated
9	SENINF2_PCLK_SEL	**Selects parallel sensor clock** 0: pclk 1: mclk
8	SENINF1_PCLK_SEL	**Selects parallel sensor clock**

Bit(s)	Name	Description
		0: pclk 1: mclk

1A040004 SENINF_TOP_CMODEL_PAR — SENINF Top C model Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SENINF4_FORMAT			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF3_FORMAT				SENINF2_FORMAT				SENINF1_FORMAT				SENINF4_EN	SENINF3_EN	SENINF2_EN	SENINF1_EN
Type	RW				RW				RW				RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:16	SENINF4_FORMAT	
15:12	SENINF3_FORMAT	
11:8	SENINF2_FORMAT	
7:4	SENINF1_FORMAT	
3	SENINF4_EN	
2	SENINF3_EN	
1	SENINF2_EN	
0	SENINF1_EN	

1A040008 SENINF_TOP_MUX_CTRL — SENINF Top Mux Control Register — 00043210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF8_MUX_SRC_SEL				SENINF7_MUX_SRC_SEL				SENINF6_MUX_SRC_SEL				SENINF5_MUX_SRC_SEL			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF4_MUX_SRC_SEL				SENINF3_MUX_SRC_SEL				SENINF2_MUX_SRC_SEL				SENINF1_MUX_SRC_SEL			
Type	RW				RW				RW				RW			
Reset	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:28	SENINF8_MUX_SRC_SEL	0: SENINF1 1: SENINF2 2: SENINF3 3: SENINF4 4: SENINF5
27:24	SENINF7_MUX_SRC_SEL	0: SENINF1 1: SENINF2 2: SENINF3 3: SENINF4 4: SENINF5

Bit(s)	Name	Description
23:20	SENINF6_MUX_SRC_SEL	0: SENINF1 1: SENINF2 2: SENINF3 3: SENINF4 4: SENINF5
19:16	SENINF5_MUX_SRC_SEL	0: SENINF1 1: SENINF2 2: SENINF3 3: SENINF4 4: SENINF5
15:12	SENINF4_MUX_SRC_SEL	0: SENINF1 1: SENINF2 2: SENINF3 3: SENINF4 4: SENINF5
11:8	SENINF3_MUX_SRC_SEL	0: SENINF1 1: SENINF2 2: SENINF3 3: SENINF4 4: SENINF5
7:4	SENINF2_MUX_SRC_SEL	0: SENINF1 1: SENINF2 2: SENINF3 3: SENINF4 4: SENINF5
3:0	SENINF1_MUX_SRC_SEL	0: SENINF1 1: SENINF2 2: SENINF3 3: SENINF4 4: SENINF5

1A040010 SENINF_TOP_CAM_MUX_CTRL **SENINF Top Cam Mux Control Register** **76543210**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_CAM7_MUX_SRC_SEL				SENINF_CAM6_MUX_SRC_SEL				SENINF_CAM5_MUX_SRC_SEL				SENINF_CAM4_MUX_SRC_SEL			
Type	RW				RW				RW				RW			
Reset	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_CAM3_MUX_SRC_SEL				SENINF_CAM2_MUX_SRC_SEL				SENINF_CAM1_MUX_SRC_SEL				SENINF_CAM0_MUX_SRC_SEL			
Type	RW				RW				RW				RW			
Reset	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:28	SENINF_CAM7_MUX_SRC_SEL	0: seninf1_mux 1: seninf2_mux 2: seninf3_mux 3: seninf4_mux 4: seninf5_mux 5: seninf6_mux 6: seninf7_mux

Bit(s)	Name	Description
		7: seninf8_mux
27:24	SENINF_CAM6_MUX_SRC_SEL	0: seninf1_mux 1: seninf2_mux 2: seninf3_mux 3: seninf4_mux 4: seninf5_mux 5: seninf6_mux 6: seninf7_mux 7: seninf8_mux
23:20	SENINF_CAM5_MUX_SRC_SEL	0: seninf1_mux 1: seninf2_mux 2: seninf3_mux 3: seninf4_mux 4: seninf5_mux 5: seninf6_mux 6: seninf7_mux 7: seninf8_mux
19:16	SENINF_CAM4_MUX_SRC_SEL	0: seninf1_mux 1: seninf2_mux 2: seninf3_mux 3: seninf4_mux 4: seninf5_mux 5: seninf6_mux 6: seninf7_mux 7: seninf8_mux
15:12	SENINF_CAM3_MUX_SRC_SEL	0: seninf1_mux 1: seninf2_mux 2: seninf3_mux 3: seninf4_mux 4: seninf5_mux 5: seninf6_mux 6: seninf7_mux 7: seninf8_mux
11:8	SENINF_CAM2_MUX_SRC_SEL	0: seninf1_mux 1: seninf2_mux 2: seninf3_mux 3: seninf4_mux 4: seninf5_mux 5: seninf6_mux 6: seninf7_mux 7: seninf8_mux
7:4	SENINF_CAM1_MUX_SRC_SEL	0: seninf1_mux 1: seninf2_mux 2: seninf3_mux 3: seninf4_mux 4: seninf5_mux 5: seninf6_mux 6: seninf7_mux 7: seninf8_mux
3:0	SENINF_CAM0_MUX_SRC_SEL	0: seninf1_mux 1: seninf2_mux 2: seninf3_mux 3: seninf4_mux 4: seninf5_mux 5: seninf6_mux

Bit(s)	Name	Description
		6: seninf7_mux 7: seninf8_mux

1A040014 SENINF_TOP_N3D_A_CTL **SENINF Top N3D_A Control Register** **00001100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		SENINF_N3D_S2_SEN_VSYNC_SRC_SEL_A				SENINF_N3D_S2_SEN_PCLK_SRC_SEL_A				SENINF_N3D_S1_SEN_VSYNC_SRC_SEL_A				SENINF_N3D_S1_SEN_PCLK_SRC_SEL_A		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	0		0	0	0

Bit(s)	Name	Description
14:12	SENINF_N3D_S2_SEN_VSYNC_SRC_SEL_A	0: seninf1_mux 1: seninf2_mux 2: seninf3_mux 3: seninf4_mux 4: seninf5_mux 5: seninf6_mux 6: seninf7_mux 7: seninf8_mux
10:8	SENINF_N3D_S2_SEN_PCLK_SRC_SEL_A	0: seninf1_mux 1: seninf2_mux 2: seninf3_mux 3: seninf4_mux 4: seninf5_mux 5: seninf6_mux 6: seninf7_mux 7: seninf8_mux
6:4	SENINF_N3D_S1_SEN_VSYNC_SRC_SEL_A	0: seninf1_mux 1: seninf2_mux 2: seninf3_mux 3: seninf4_mux 4: seninf5_mux 5: seninf6_mux 6: seninf7_mux 7: seninf8_mux
2:0	SENINF_N3D_S1_SEN_PCLK_SRC_SEL_A	0: seninf1_mux 1: seninf2_mux 2: seninf3_mux 3: seninf4_mux 4: seninf5_mux 5: seninf6_mux 6: seninf7_mux 7: seninf8_mux

1A040018 SENINF_TOP_N3D_B_CTL **SENINF Top N3D_B Control Register** **00001100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		SENINF_N3D_S2_SEN_VSYNC_SRC_SEL_B				SENINF_N3D_S2_SEN_PCLK_SRC_SEL_B				SENINF_N3D_S1_SEN_VSYNC_SRC_SEL_B				SENINF_N3D_S1_SEN_PCLK_SRC_SEL_B		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	0		0	0	0

Bit(s)	Name	Description
14:12	SENINF_N3D_S2_SEN_VSYNC_SRC_SEL_B	0: seninf1_mux 1: seninf2_mux 2: seninf3_mux 3: seninf4_mux 4: seninf5_mux 5: seninf6_mux 6: seninf7_mux 7: seninf8_mux
10:8	SENINF_N3D_S2_SEN_PCLK_SRC_SEL_B	0: seninf1_mux 1: seninf2_mux 2: seninf3_mux 3: seninf4_mux 4: seninf5_mux 5: seninf6_mux 6: seninf7_mux 7: seninf8_mux
6:4	SENINF_N3D_S1_SEN_VSYNC_SRC_SEL_B	0: seninf1_mux 1: seninf2_mux 2: seninf3_mux 3: seninf4_mux 4: seninf5_mux 5: seninf6_mux 6: seninf7_mux 7: seninf8_mux
2:0	SENINF_N3D_S1_SEN_PCLK_SRC_SEL_B	0: seninf1_mux 1: seninf2_mux 2: seninf3_mux 3: seninf4_mux 4: seninf5_mux 5: seninf6_mux 6: seninf7_mux 7: seninf8_mux

Module name: mipi_rx_ana Base address: (+10217000h)

Address	Name	Width	Register Function
10217000	MIPI_RX_ANA00_CSI0A	32	2D1C Global Control
10217004	MIPI_RX_ANA04_CSI0A	32	2D1C Global Control

Address	Name	Width	Register Function
10217008	MIPI_RX_ANA08_CSI0A	32	High Speed Termination Control
1021700C	MIPI_RX_ANA0C_CSI0A	32	High Speed Termination Control
10217010	MIPI_RX_ANA10_CSI0A	32	Bandgap Voltage for Delay Line Calibration
10217014	MIPI_RX_ANA14_CSI0A	32	Bandgap Voltage for Delay Line Calibration
10217018	MIPI_RX_ANA18_CSI0A	32	HS AMP Control
1021701C	MIPI_RX_ANA1C_CSI0A	32	HS AMP Control
10217020	MIPI_RX_ANA20_CSI0A	32	HS AMP Control
10217024	MIPI_RX_ANA24_CSI0A	32	DPHY Deserializer Control
10217028	MIPI_RX_ANA28_CSI0A	32	CPHY CDR Control
1021702C	MIPI_RX_ANA2C_CSI0A	32	CPHY CDR Control
10217030	MIPI_RX_ANA30_CSI0A	32	CPHY CDR Control
10217034	MIPI_RX_ANA34_CSI0A	32	CPHY CDR Control
10217038	MIPI_RX_ANA38_CSI0A	32	CPHY CDR Control
1021703C	MIPI_RX_ANA3C_CSI0A	32	CPHY CDR Control
10217040	MIPI_RX_ANA40_CSI0A	32	GPI Control
10217044	MIPI_RX_ANA44_CSI0A	32	GPI Control
10217048	MIPI_RX_ANA48_CSI0A	32	RGS
1021704C	MIPI_RX_ANA4C_CSI0A	32	DEBUG
10217050	MIPI_RX_ANA50_CSI0A	32	DEBUG
10217054	MIPI_RX_ANA54_CSI0A	32	DEBUG
10217058	MIPI_RX_ANA58_CSI0A	32	DEBUG
1021705C	MIPI_RX_ANA5C_CSI0A	32	DEBUG
10217060	MIPI_RX_ANA60_CSI0A	32	DEBUG
10217064	MIPI_RX_ANA64_CSI0A	32	DEBUG
10217068	MIPI_RX_ANA68_CSI0A	32	DEBUG
1021706C	MIPI_RX_ANA6C_CSI0A	32	DEBUG
10217070	MIPI_RX_ANA70_CSI0A	32	DEBUG

Address	Name	Width	Register Function
10217074	MIPI_RX_ANA74_CSI0A	32	DEBUG
10217078	MIPI_RX_ANA78_CSI0A	32	DEBUG
1021707C	MIPI_RX_ANA7C_CSI0A	32	DEBUG
10217080	MIPI_RX_WRAPPER80_CSI0A	32	WRAPPER
10217084	MIPI_RX_WRAPPER84_CSI0A	32	WRAPPER
10217088	MIPI_RX_WRAPPER88_CSI0A	32	WRAPPER
1021708C	MIPI_RX_WRAPPER8C_CSI0A	32	WRAPPER
10217090	MIPI_RX_WRAPPER90_CSI0A	32	WRAPPER
10217094	MIPI_RX_WRAPPER94_CSI0A	32	WRAPPER
10217098	MIPI_RX_WRAPPER98_CSI0A	32	WRAPPER
1021709C	MIPI_RX_WRAPPER9C_CSI0A	32	WRAPPER
10217200	MIPI_RX_ANA00_CSI0B	32	2D1C Global Control
10217204	MIPI_RX_ANA04_CSI0B	32	2D1C Global Control
10217208	MIPI_RX_ANA08_CSI0B	32	High Speed Termination Control
1021720C	MIPI_RX_ANA0C_CSI0B	32	High Speed Termination Control
10217210	MIPI_RX_ANA10_CSI0B	32	Bandgap Voltage for Delay Line Calibration
10217214	MIPI_RX_ANA14_CSI0B	32	Bandgap Voltage for Delay Line Calibration
10217218	MIPI_RX_ANA18_CSI0B	32	HS AMP Control
1021721C	MIPI_RX_ANA1C_CSI0B	32	HS AMP Control
10217220	MIPI_RX_ANA20_CSI0B	32	HS AMP Control
10217224	MIPI_RX_ANA24_CSI0B	32	DPHY Deserializer Control
10217228	MIPI_RX_ANA28_CSI0B	32	CPHY CDR Control
1021722C	MIPI_RX_ANA2C_CSI0B	32	CPHY CDR Control
10217230	MIPI_RX_ANA30_CSI0B	32	CPHY CDR Control
10217234	MIPI_RX_ANA34_CSI0B	32	CPHY CDR Control
10217238	MIPI_RX_ANA38_CSI0B	32	CPHY CDR Control
1021723C	MIPI_RX_ANA3C_CSI0B	32	CPHY CDR Control

Address	Name	Width	Register Function
10217240	MIPI_RX_ANA40_CSI0B	32	GPI Control
10217244	MIPI_RX_ANA44_CSI0B	32	GPI Control
10217248	MIPI_RX_ANA48_CSI0B	32	RGS
1021724C	MIPI_RX_ANA4C_CSI0B	32	DEBUG
10217250	MIPI_RX_ANA50_CSI0B	32	DEBUG
10217254	MIPI_RX_ANA54_CSI0B	32	DEBUG
10217258	MIPI_RX_ANA58_CSI0B	32	DEBUG
1021725C	MIPI_RX_ANA5C_CSI0B	32	DEBUG
10217260	MIPI_RX_ANA60_CSI0B	32	DEBUG
10217264	MIPI_RX_ANA64_CSI0B	32	DEBUG
10217268	MIPI_RX_ANA68_CSI0B	32	DEBUG
1021726C	MIPI_RX_ANA6C_CSI0B	32	DEBUG
10217270	MIPI_RX_ANA70_CSI0B	32	DEBUG
10217274	MIPI_RX_ANA74_CSI0B	32	DEBUG
10217278	MIPI_RX_ANA78_CSI0B	32	DEBUG
1021727C	MIPI_RX_ANA7C_CSI0B	32	DEBUG
10217280	MIPI_RX_WRAPPER80_CSI0B	32	WRAPPER
10217284	MIPI_RX_WRAPPER84_CSI0B	32	WRAPPER
10217288	MIPI_RX_WRAPPER88_CSI0B	32	WRAPPER
1021728C	MIPI_RX_WRAPPER8C_CSI0B	32	WRAPPER
10217290	MIPI_RX_WRAPPER90_CSI0B	32	WRAPPER
10217294	MIPI_RX_WRAPPER94_CSI0B	32	WRAPPER
10217298	MIPI_RX_WRAPPER98_CSI0B	32	WRAPPER
1021729C	MIPI_RX_WRAPPER9C_CSI0B	32	WRAPPER
10217400	MIPI_RX_ANA00_CSI1A	32	2D1C Global Control
10217404	MIPI_RX_ANA04_CSI1A	32	2D1C Global Control
10217408	MIPI_RX_ANA08_CSI1A	32	High Speed Termination Control

Address	Name	Width	Register Function
1021740C	MIPI_RX_ANA0C_CSI1A	32	High Speed Termination Control
10217410	MIPI_RX_ANA10_CSI1A	32	Bandgap Voltage for Delay Line Calibration
10217414	MIPI_RX_ANA14_CSI1A	32	Bandgap Voltage for Delay Line Calibration
10217418	MIPI_RX_ANA18_CSI1A	32	HS AMP Control
1021741C	MIPI_RX_ANA1C_CSI1A	32	HS AMP Control
10217420	MIPI_RX_ANA20_CSI1A	32	HS AMP Control
10217424	MIPI_RX_ANA24_CSI1A	32	DPHY Deserializer Control
10217428	MIPI_RX_ANA28_CSI1A	32	CPHY CDR Control
1021742C	MIPI_RX_ANA2C_CSI1A	32	CPHY CDR Control
10217430	MIPI_RX_ANA30_CSI1A	32	CPHY CDR Control
10217434	MIPI_RX_ANA34_CSI1A	32	CPHY CDR Control
10217438	MIPI_RX_ANA38_CSI1A	32	CPHY CDR Control
1021743C	MIPI_RX_ANA3C_CSI1A	32	CPHY CDR Control
10217440	MIPI_RX_ANA40_CSI1A	32	GPI Control
10217444	MIPI_RX_ANA44_CSI1A	32	GPI Control
10217448	MIPI_RX_ANA48_CSI1A	32	RGS
1021744C	MIPI_RX_ANA4C_CSI1A	32	DEBUG
10217450	MIPI_RX_ANA50_CSI1A	32	DEBUG
10217454	MIPI_RX_ANA54_CSI1A	32	DEBUG
10217458	MIPI_RX_ANA58_CSI1A	32	DEBUG
1021745C	MIPI_RX_ANA5C_CSI1A	32	DEBUG
10217460	MIPI_RX_ANA60_CSI1A	32	DEBUG
10217464	MIPI_RX_ANA64_CSI1A	32	DEBUG
10217468	MIPI_RX_ANA68_CSI1A	32	DEBUG
1021746C	MIPI_RX_ANA6C_CSI1A	32	DEBUG
10217470	MIPI_RX_ANA70_CSI1A	32	DEBUG
10217474	MIPI_RX_ANA74_CSI1A	32	DEBUG

Address	Name	Width	Register Function
10217478	MIPI_RX_ANA78_CSI1A	32	DEBUG
1021747C	MIPI_RX_ANA7C_CSI1A	32	DEBUG
10217480	MIPI_RX_WRAPPER80_CSI1A	32	WRAPPER
10217484	MIPI_RX_WRAPPER84_CSI1A	32	WRAPPER
10217488	MIPI_RX_WRAPPER88_CSI1A	32	WRAPPER
1021748C	MIPI_RX_WRAPPER8C_CSI1A	32	WRAPPER
10217490	MIPI_RX_WRAPPER90_CSI1A	32	WRAPPER
10217494	MIPI_RX_WRAPPER94_CSI1A	32	WRAPPER
10217498	MIPI_RX_WRAPPER98_CSI1A	32	WRAPPER
1021749C	MIPI_RX_WRAPPER9C_CSI1A	32	WRAPPER
10217600	MIPI_RX_ANA00_CSI1B	32	2D1C Global Control
10217604	MIPI_RX_ANA04_CSI1B	32	2D1C Global Control
10217608	MIPI_RX_ANA08_CSI1B	32	High Speed Termination Control
1021760C	MIPI_RX_ANA0C_CSI1B	32	High Speed Termination Control
10217610	MIPI_RX_ANA10_CSI1B	32	Bandgap Voltage for Delay Line Calibration
10217614	MIPI_RX_ANA14_CSI1B	32	Bandgap Voltage for Delay Line Calibration
10217618	MIPI_RX_ANA18_CSI1B	32	HS AMP Control
1021761C	MIPI_RX_ANA1C_CSI1B	32	HS AMP Control
10217620	MIPI_RX_ANA20_CSI1B	32	HS AMP Control
10217624	MIPI_RX_ANA24_CSI1B	32	DPHY Deserializer Control
10217628	MIPI_RX_ANA28_CSI1B	32	CPHY CDR Control
1021762C	MIPI_RX_ANA2C_CSI1B	32	CPHY CDR Control
10217630	MIPI_RX_ANA30_CSI1B	32	CPHY CDR Control
10217634	MIPI_RX_ANA34_CSI1B	32	CPHY CDR Control
10217638	MIPI_RX_ANA38_CSI1B	32	CPHY CDR Control
1021763C	MIPI_RX_ANA3C_CSI1B	32	CPHY CDR Control
10217640	MIPI_RX_ANA40_CSI1B	32	GPI Control

Address	Name	Width	Register Function
10217644	MIPI_RX_ANA44_CSI1B	32	GPI Control
10217648	MIPI_RX_ANA48_CSI1B	32	RGS
1021764C	MIPI_RX_ANA4C_CSI1B	32	DEBUG
10217650	MIPI_RX_ANA50_CSI1B	32	DEBUG
10217654	MIPI_RX_ANA54_CSI1B	32	DEBUG
10217658	MIPI_RX_ANA58_CSI1B	32	DEBUG
1021765C	MIPI_RX_ANA5C_CSI1B	32	DEBUG
10217660	MIPI_RX_ANA60_CSI1B	32	DEBUG
10217664	MIPI_RX_ANA64_CSI1B	32	DEBUG
10217668	MIPI_RX_ANA68_CSI1B	32	DEBUG
1021766C	MIPI_RX_ANA6C_CSI1B	32	DEBUG
10217670	MIPI_RX_ANA70_CSI1B	32	DEBUG
10217674	MIPI_RX_ANA74_CSI1B	32	DEBUG
10217678	MIPI_RX_ANA78_CSI1B	32	DEBUG
1021767C	MIPI_RX_ANA7C_CSI1B	32	DEBUG
10217680	MIPI_RX_WRAPPER80_CSI1B	32	WRAPPER
10217684	MIPI_RX_WRAPPER84_CSI1B	32	WRAPPER
10217688	MIPI_RX_WRAPPER88_CSI1B	32	WRAPPER
1021768C	MIPI_RX_WRAPPER8C_CSI1B	32	WRAPPER
10217690	MIPI_RX_WRAPPER90_CSI1B	32	WRAPPER
10217694	MIPI_RX_WRAPPER94_CSI1B	32	WRAPPER
10217698	MIPI_RX_WRAPPER98_CSI1B	32	WRAPPER
1021769C	MIPI_RX_WRAPPER9C_CSI1B	32	WRAPPER
10217800	MIPI_RX_ANA00_CSI2	32	2D1C Global Control
10217804	MIPI_RX_ANA04_CSI2	32	2D1C Global Control
10217808	MIPI_RX_ANA08_CSI2	32	High Speed Termination Control
1021780C	MIPI_RX_ANA0C_CSI2	32	High Speed Termination Control

Address	Name	Width	Register Function
10217810	MIPI_RX_ANA10_CSI2	32	Bandgap Voltage for Delay Line Calibration
10217814	MIPI_RX_ANA14_CSI2	32	Bandgap Voltage for Delay Line Calibration
10217818	MIPI_RX_ANA18_CSI2	32	HS AMP Control
1021781C	MIPI_RX_ANA1C_CSI2	32	HS AMP Control
10217820	MIPI_RX_ANA20_CSI2	32	HS AMP Control
10217824	MIPI_RX_ANA24_CSI2	32	DPHY Deserializer Control
10217828	MIPI_RX_ANA28_CSI2	32	CPHY CDR Control
1021782C	MIPI_RX_ANA2C_CSI2	32	CPHY CDR Control
10217830	MIPI_RX_ANA30_CSI2	32	CPHY CDR Control
10217834	MIPI_RX_ANA34_CSI2	32	CPHY CDR Control
10217838	MIPI_RX_ANA38_CSI2	32	CPHY CDR Control
1021783C	MIPI_RX_ANA3C_CSI2	32	CPHY CDR Control
10217840	MIPI_RX_ANA40_CSI2	32	GPI Control
10217844	MIPI_RX_ANA44_CSI2	32	GPI Control
10217848	MIPI_RX_ANA48_CSI2	32	RGS
1021784C	MIPI_RX_ANA4C_CSI2	32	DEBUG
10217850	MIPI_RX_ANA50_CSI2	32	DEBUG
10217854	MIPI_RX_ANA54_CSI2	32	DEBUG
10217858	MIPI_RX_ANA58_CSI2	32	DEBUG
1021785C	MIPI_RX_ANA5C_CSI2	32	DEBUG
10217860	MIPI_RX_ANA60_CSI2	32	DEBUG
10217864	MIPI_RX_ANA64_CSI2	32	DEBUG
10217868	MIPI_RX_ANA68_CSI2	32	DEBUG
1021786C	MIPI_RX_ANA6C_CSI2	32	DEBUG
10217870	MIPI_RX_ANA70_CSI2	32	DEBUG
10217874	MIPI_RX_ANA74_CSI2	32	DEBUG
10217878	MIPI_RX_ANA78_CSI2	32	DEBUG

Address	Name	Width	Register Function
1021787C	MIPI_RX_ANA7C_CSI2	32	DEBUG
10217880	MIPI_RX_WRAPPER80_CSI2	32	WRAPPER
10217884	MIPI_RX_WRAPPER84_CSI2	32	WRAPPER
10217888	MIPI_RX_WRAPPER88_CSI2	32	WRAPPER
1021788C	MIPI_RX_WRAPPER8C_CSI2	32	WRAPPER
10217890	MIPI_RX_WRAPPER90_CSI2	32	WRAPPER
10217894	MIPI_RX_WRAPPER94_CSI2	32	WRAPPER
10217898	MIPI_RX_WRAPPER98_CSI2	32	WRAPPER
1021789C	MIPI_RX_WRAPPER9C_CSI2	32	WRAPPER

10217000 MIPI_RX_ANA00_CSI0A 2D1C Global Control 00000492

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_CSI_DPHY_L2_CKSEL	RG_CSI_DPHY_L2_CKMODE_EN	RG_CSI_DPHY_L2_BYPASS_SYNC	RG_CSI_DPHY_L1_CKSEL	RG_CSI_DPHY_L1_CKMODE_EN	RG_CSI_DPHY_L1_BYPASS_SYNC	RG_CSI_DPHY_L0_CKSEL	RG_CSI_DPHY_L0_CKMODE_EN	RG_CSI_DPHY_L0_BYPASS_SYNC	RG_CSI_BG_CORE_EN	RG_CSI_BG_LPF_EN	RG_CSI_HSAMP_PROTECT_EN	RG_CSI_CPHY_EN
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	1	0	0	1	0	0	1	0	0	1	0

Bit(s)	Name	Description
12	RG_CSI_DPHY_L2_CKSEL	**Data Mode** [NORMAL]1'b0: Sample data by Local Clock [NORMAL]1'b1: Sample data by Common Clock CK Mode [NORMAL]1'b0: Connect to Local Clock [NORMAL]1'b1: Connect to Common Clock
11	RG_CSI_DPHY_L2_CKMODE_EN	**[NORMAL]1'b0: Data Mode** [NORMAL]1'b1: CK Mode
10	RG_CSI_DPHY_L2_BYPASS_SYNC	**Bypass or Sync Mode Selection** [NORMAL]1'b0: Sync Mode [NORMAL]1'b1: Bypass Mode
9	RG_CSI_DPHY_L1_CKSEL	**Data Mode** [NORMAL]1'b0: Sample data by Local Clock [NORMAL]1'b1: Sample data by Common Clock CK Mode [NORMAL]1'b0: Connect to Local Clock [NORMAL]1'b1: Connect to Common Clock

Bit(s)	Name	Description
8	RG_CSI_DPHY_L1_CKMODE_EN	**[NORMAL]1'b0: Data Mode** [NORMAL]1'b1: CK Mode
7	RG_CSI_DPHY_L1_BYPASS_SYNC	**Bypass or Sync Mode Selection** [NORMAL]1'b0: Sync Mode [NORMAL]1'b1: Bypass Mode
6	RG_CSI_DPHY_L0_CKSEL	**Data Mode** [NORMAL]1'b0: Sample data by Local Clock [NORMAL]1'b1: Sample data by Common Clock CK Mode [NORMAL]1'b0: Connect to Local Clock [NORMAL]1'b1: Connect to Common Clock
5	RG_CSI_DPHY_L0_CKMODE_EN	**[NORMAL]1'b0: Data Mode** [NORMAL]1'b1: CK Mode
4	RG_CSI_DPHY_L0_BYPASS_SYNC	**Bypass or Sync Mode Selection** [NORMAL]1'b0: Sync Mode [NORMAL]1'b1: Bypass Mode
3	RG_CSI_BG_CORE_EN	**[NORMAL]1'b0: Bandgap Disable** [NORMAL]1'b1: Bandgap Enable
2	RG_CSI_BG_LPF_EN	**[NORMAL]1'b0: Bandgap low pass filter Disable** [NORMAL]1'b1: Bandgap low pass filter Enable
1	RG_CSI_HSAMP_PROTECT_EN	**HSAMP Protection** [NORMAL]1'b0: Disable [NORMAL]1'b1: Enable
0	RG_CSI_CPHY_EN	**1'b0: DPHY Mode** 1'b1: CPHY Mode

10217004 MIPI_RX_AN_A04_CSI0A 2D1C Global Control 00084444

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CSI_FORCE_HSRT_EN	RG_CSI_BG_MON_VREF_SEL								RG_CSI_BG_VREF_SEL			
Type				RW	RW								RW			
Reset				0	0	0	0	0					1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI_BG_HSDET_VTL_SEL				RG_CSI_BG_HSDET_VTH_SEL				RG_CSI_BG_LPRX_VTL_SEL				RG_CSI_BG_LPRX_VTH_SEL		
Type		RW				RW				RW				RW		
Reset		1	0	0		1	0	0		1	0	0		1	0	0

Bit(s)	Name	Description
28	RG_CSI_FORCE_HSRT_EN	**Force HSRT Enable to do FT calibration and eFuse**
27:24	RG_CSI_BG_MON_VREF_SEL	**Monitor Selection**
19:16	RG_CSI_BG_VREF_SEL	**HSAMP LDO Reference Voltage** Default 0.9V
14:12	RG_CSI_BG_HSDET_VTL_SEL	**HSDET VTH Selection** Default 0.12V
10:8	RG_CSI_BG_HSDET_VTH_SEL	**HSDET VTH Selection** Default 0.15V
6:4	RG_CSI_BG_LPRX_VTL_SEL	**LPRX VTL Selection** Default 0.70V
2:0	RG_CSI_BG_LPRX_VTH_SEL	**LPRX VTH Selection** Default 0.75V

10217008 MIPI_RX_ANA08_CSI0A High Speed Termination Control 10101010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CSI_L1N_T1A_HSRT_CODE								RG_CSI_L1P_T0C_HSRT_CODE				
Type				RW								RW				
Reset				1	0	0	0	0				1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_CSI_L0N_T0B_HSRT_CODE								RG_CSI_L0P_T0A_HSRT_CODE				
Type				RW								RW				
Reset				1	0	0	0	0				1	0	0	0	0

Bit(s)	Name	Description
28:24	RG_CSI_L1N_T1A_HSRT_CODE	**Termination code** 8000hm/(8+N) Requires Calibration & Efuse on FT
20:16	RG_CSI_L1P_T0C_HSRT_CODE	**Termination code** 8000hm/(8+N) Requires Calibration & Efuse on FT
12:8	RG_CSI_L0N_T0B_HSRT_CODE	**Termination code** 8000hm/(8+N) Requires Calibration & Efuse on FT
4:0	RG_CSI_L0P_T0A_HSRT_CODE	**Termination code** 8000hm/(8+N) Requires Calibration & Efuse on FT

1021700C MIPI_RX_ANA0C_CSI0A High Speed Termination Control 00001010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_CSI_L2N_T1C_HSRT_CODE								RG_CSI_L2P_T1B_HSRT_CODE				
Type				RW								RW				
Reset				1	0	0	0	0				1	0	0	0	0

Bit(s)	Name	Description
12:8	RG_CSI_L2N_T1C_HSRT_CODE	**Termination code** 8000hm/(8+N) Requires Calibration & Efuse on FT
4:0	RG_CSI_L2P_T1B_HSRT_CODE	**Termination code** 8000hm/(8+N) Requires Calibration & Efuse on FT

10217010 MIPI_RX_ANA10_CSI0A Bandgap Voltage for Delay Line Calibration 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RG_CSI_CPHY_To_VREF_SEL						RG_CSI_CPHY_To_CDR_DELAYCAL_RSTB	RG_CSI_CPHY_To_CDR_DELAYCAL_EN	RG_CSI_DPHY_L2_VREF_SEL						RG_CSI_DPHY_L2_DELAYCAL_RSTB	RG_CSI_DPHY_L2_DELAYCAL_EN
Type	RW						RW	RW	RW						RW	RW
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_DPHY_L1_VREF_SEL						RG_CSI_DPHY_L1_DELAYCAL_RSTB	RG_CSI_DPHY_L1_DELAYCAL_EN	RG_CSI_DPHY_Lo_VREF_SEL						RG_CSI_DPHY_Lo_DELAYCAL_RSTB	RG_CSI_DPHY_Lo_DELAYCAL_EN
Type	RW						RW	RW	RW						RW	RW
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:26	RG_CSI_CPHY_To_VREF_SEL	**Do Delay Line Reference Voltage** Requires Software Calibration
25	RG_CSI_CPHY_To_CDR_DELAYCAL_RSTB	**TRIOo Delay Line Calibration Reset Bar**
24	RG_CSI_CPHY_To_CDR_DELAYCAL_EN	**TRIOo Delay Line Calibration Enable**
23:18	RG_CSI_DPHY_L2_VREF_SEL	**Do Delay Line Reference Voltage** Requires Software Calibration
17	RG_CSI_DPHY_L2_DELAYCAL_RSTB	**D1 Delay Line Calibration Reset Bar**
16	RG_CSI_DPHY_L2_DELAYCAL_EN	**D1 Delay Line Calibration Enable**
15:10	RG_CSI_DPHY_L1_VREF_SEL	**Do Delay Line Reference Voltage** Requires Software Calibration
9	RG_CSI_DPHY_L1_DELAYCAL_RSTB	**CK Delay Line Calibration Reset Bar**
8	RG_CSI_DPHY_L1_DELAYCAL_EN	**CK Delay Line Calibration Enable**
7:2	RG_CSI_DPHY_Lo_VREF_SEL	**Do Delay Line Reference Voltage** Requires Software Calibration
1	RG_CSI_DPHY_Lo_DELAYCAL_RSTB	**Do Delay Line Calibration Reset Bar**
0	RG_CSI_DPHY_Lo_DELAYCAL_EN	**Do Delay Line Calibration Enable**

10217014 MIPI_RX_ANA14_CSIoA **Bandgap Voltage for Delay Line Calibration** **00000080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSI_CPHY_T1_VREF_SEL						RG_CSI_CPHY_T1_CDR_D	RG_CSI_CPHY_T1_CDR_D

															ELAY CAL_ RSTB	ELAY CAL_ EN
Type									RW						RW	RW
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSI_CPHY_T1_VREF_SEL	**D0 Delay Line Reference Voltage** Requires Software Calibration
1	RG_CSI_CPHY_T1_CDR_DELAYCAL_RSTB	**TRIO1 Delay Line Calibration Reset Bar**
0	RG_CSI_CPHY_T1_CDR_DELAYCAL_EN	**TRIO1 Delay Line Calibration Enable**

10217018 MIPI_RX_ANA18_CSI0A **HS AMP Control** **88008800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_XX_ToCA_HSAMP_SRB				RG_CSI_XX_ToCA_HSAMP_SRA				RG_CSI_XX_ToCA_HSAMP_BW		RG_CSI_XX_ToCA_HSAMP_IS		RG_CSI_XX_ToCA_HSAMP_SCB	RG_CSI_XX_ToCA_HSAMP_SCA	RG_CSI_XX_ToCA_HSAMP_LPBK_TEST_EN	RG_CSI_XX_ToCA_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_Lo_ToAB_HSAMP_SRB				RG_CSI_Lo_ToAB_HSAMP_SRA				RG_CSI_Lo_ToAB_HSAMP_BW		RG_CSI_Lo_ToAB_HSA MP_IS		RG_CSI_Lo_ToAB_HSAMP_SCB	RG_CSI_Lo_ToAB_HSAMP_SCA	RG_CSI_Lo_ToAB_HSAMP_LPBK_TEST_EN	RG_CSI_Lo_ToAB_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	RG_CSI_XX_ToCA_HSAMP_SRB	
27:24	RG_CSI_XX_ToCA_HSAMP_SRA	
23:22	RG_CSI_XX_ToCA_HSAMP_BW	
21:20	RG_CSI_XX_ToCA_HSAMP_IS	
19	RG_CSI_XX_ToCA_HSAMP_SCB	
18	RG_CSI_XX_ToCA_HSAMP_SCA	
17	RG_CSI_XX_ToCA_HSAMP_LPBK_TEST_EN	
16	RG_CSI_XX_ToCA_HSAMP_MON_EN	
15:12	RG_CSI_Lo_ToAB_HSAMP_SRB	
11:8	RG_CSI_Lo_ToAB_HSAMP_SRA	
7:6	RG_CSI_Lo_ToAB_HSAMP_BW	
5:4	RG_CSI_Lo_ToAB_HSAMP_IS	
3	RG_CSI_Lo_ToAB_HSAMP_SCB	
2	RG_CSI_Lo_ToAB_HSAMP_SCA	

Bit(s)	Name	Description
1	RG_CSI_Lo_ToAB_HSAMP_LPBK_TEST_EN	
0	RG_CSI_Lo_ToAB_HSAMP_MON_EN	

1021701C **MIPI_RX_ANA1C_CSIoA** **HS AMP Control** **88008800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_L1_T1AB_HSAMP_SRB				RG_CSI_L1_T1AB_HSAMP_SRA				RG_CSI_L1_T1AB_HSAMP_BW		RG_CSI_L1_T1AB_HSAMP_IS		RG_CSI_L1_T1AB_HSAMP_SCB	RG_CSI_L1_T1AB_HSAMP_SCA	RG_CSI_L1_T1AB_HSAMP_LPBK_TEST_EN	RG_CSI_L1_T1AB_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_XX_ToBC_HSAMP_SRB				RG_CSI_XX_ToBC_HSAMP_SRA				RG_CSI_XX_ToBC_HSAMP_BW		RG_CSI_XX_ToBC_HSAMP_IS		RG_CSI_XX_ToBC_HSAMP_SCB	RG_CSI_XX_ToBC_HSAMP_SCA	RG_CSI_XX_ToBC_HSAMP_LPBK_TEST_EN	RG_CSI_XX_ToBC_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	RG_CSI_L1_T1AB_HSAMP_SRB	
27:24	RG_CSI_L1_T1AB_HSAMP_SRA	
23:22	RG_CSI_L1_T1AB_HSAMP_BW	
21:20	RG_CSI_L1_T1AB_HSAMP_IS	
19	RG_CSI_L1_T1AB_HSAMP_SCB	
18	RG_CSI_L1_T1AB_HSAMP_SCA	
17	RG_CSI_L1_T1AB_HSAMP_LPBK_TEST_EN	
16	RG_CSI_L1_T1AB_HSAMP_MON_EN	
15:12	RG_CSI_XX_ToBC_HSAMP_SRB	
11:8	RG_CSI_XX_ToBC_HSAMP_SRA	
7:6	RG_CSI_XX_ToBC_HSAMP_BW	
5:4	RG_CSI_XX_ToBC_HSAMP_IS	
3	RG_CSI_XX_ToBC_HSAMP_SCB	
2	RG_CSI_XX_ToBC_HSAMP_SCA	
1	RG_CSI_XX_ToBC_HSAMP_LPBK_TEST_EN	
0	RG_CSI_XX_ToBC_HSAMP_MON_EN	

10217020 **MIPI_RX_ANA20_CSIoA** **HS AMP Control** **88008800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_L2_T1BC_HSAMP_SRB				RG_CSI_L2_T1BC_HSAMP_SRA				RG_CSI_L2_T1BC_HSAMP_BW		RG_CSI_L2_T1BC_HSAMP_IS		RG_CSI_L2_T1BC_HSAMP_SCB	RG_CSI_L2_T1BC_HSAMP_SCA	RG_CSI_L2_T1BC_HSAMP_LPBK_TEST_EN	RG_CSI_L2_T1BC_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_XX_T1CA_HSAMP_SRB				RG_CSI_XX_T1CA_HSAMP_SRA				RG_CSI_XX_T1CA_HSAMP_BW		RG_CSI_XX_T1CA_HSAMP_IS		RG_CSI_XX_T1CA_HSAMP_SCB	RG_CSI_XX_T1CA_HSAMP_SCA	RG_CSI_XX_T1CA_HSAMP_LPBK_TEST_EN	RG_CSI_XX_T1CA_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	RG_CSI_L2_T1BC_HSAMP_SRB	
27:24	RG_CSI_L2_T1BC_HSAMP_SRA	
23:22	RG_CSI_L2_T1BC_HSAMP_BW	
21:20	RG_CSI_L2_T1BC_HSAMP_IS	
19	RG_CSI_L2_T1BC_HSAMP_SCB	
18	RG_CSI_L2_T1BC_HSAMP_SCA	
17	RG_CSI_L2_T1BC_HSAMP_LPBK_TEST_EN	
16	RG_CSI_L2_T1BC_HSAMP_MON_EN	
15:12	RG_CSI_XX_T1CA_HSAMP_SRB	
11:8	RG_CSI_XX_T1CA_HSAMP_SRA	
7:6	RG_CSI_XX_T1CA_HSAMP_BW	
5:4	RG_CSI_XX_T1CA_HSAMP_IS	
3	RG_CSI_XX_T1CA_HSAMP_SCB	
2	RG_CSI_XX_T1CA_HSAMP_SCA	
1	RG_CSI_XX_T1CA_HSAMP_LPBK_TEST_EN	
0	RG_CSI_XX_T1CA_HSAMP_MON_EN	

10217024 MIPI_RX_ANA24_CSI0A **DPHY Deserializer Control** **0F000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_RESERVE											RG_CSI_DPHY_L2_SYNC_EDGE_SEL		RG_CSI_DPHY_L2_FORCE_SYNC		RG_CSI_DPHY_L2_BYPASS_BYTECK_INVERT
Type	RW											RW		RW		RW

Reset	0	0	0	0	1	1	1	1				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_DPHY_L2_BYTECK_INVERT		RG_CSI_DPHY_L1_SYNC_EDGE_SEL		RG_CSI_DPHY_L1_FORCE_SYNC		RG_CSI_DPHY_L1_BYPASS_BYTECK_INVERT	RG_CSI_DPHY_L1_BYTECK_INVERT			RG_CSI_DPHY_Lo_SYNC_EDGE_SEL		RG_CSI_DPHY_Lo_FORCE_SYNC		RG_CSI_DPHY_Lo_BYPASS_BYTECK_INVERT	RG_CSI_DPHY_Lo_BYTECK_INVERT
Type	RW		RW		RW		RW	RW			RW		RW		RW	RW
Reset	0		0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RG_CSI_RESERVE	
20:19	RG_CSI_DPHY_L2_SYNC_EDGE_SEL	
18:17	RG_CSI_DPHY_L2_FORCE_SYNC	
16	RG_CSI_DPHY_L2_BYPASS_BYTECK_INVERT	
15	RG_CSI_DPHY_L2_BYTECK_INVERT	
13:12	RG_CSI_DPHY_L1_SYNC_EDGE_SEL	
11:10	RG_CSI_DPHY_L1_FORCE_SYNC	
9	RG_CSI_DPHY_L1_BYPASS_BYTECK_INVERT	
8	RG_CSI_DPHY_L1_BYTECK_INVERT	
5:4	RG_CSI_DPHY_Lo_SYNC_EDGE_SEL	
3:2	RG_CSI_DPHY_Lo_FORCE_SYNC	
1	RG_CSI_DPHY_Lo_BYPASS_BYTECK_INVERT	
0	RG_CSI_DPHY_Lo_BYTECK_INVERT	

10217028 MIPI_RX_ANA28_CSI0A **CPHY CDR Control** **0000888F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CSI_CPHY_To_CDR_EARLY_CODE					RG_CSI_CPHY_To_CDR_INIT_CODE							RG_CSI_CPHY_To_CDR_MANUAL_EN
Type				RW					RW							RW
Reset				0	0	0	0	0	0	0	0	0	0			0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_To_CDR_CA_WIDTH			RG_CSI_CPHY_To_CDR_BC_WIDTH			RG_CSI_CPHY_To_CDR_AB_WIDTH						RG_CSI_CPHY_To_CDR_LPF_CTRL		RG_CSI_CPHY_To_CDR_AUTOLOAD_EN	RG_CSI_CPHY_To_CDR_DIRECT_EN

Type	RW				RW				RW				RW		RW	RW
Reset	1	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1

Bit(s)	Name	Description
28:24	RG_CSI_CPHY_To_CDR_EARLY_CODE	
23:19	RG_CSI_CPHY_To_CDR_INIT_CODE	
16	RG_CSI_CPHY_To_CDR_MANUAL_EN	
15:12	RG_CSI_CPHY_To_CDR_CA_WIDTH	Filter out coding jitter
11:8	RG_CSI_CPHY_To_CDR_BC_WIDTH	Filter out coding jitter
7:4	RG_CSI_CPHY_To_CDR_AB_WIDTH	Filter out coding jitter
3:2	RG_CSI_CPHY_To_CDR_LPF_CTRL	
1	RG_CSI_CPHY_To_CDR_AUTOLOAD_EN	
0	RG_CSI_CPHY_To_CDR_DIRECT_EN	Direct Sample Mode Enable

1021702C MIPI_RX_ANA2C_CSI0A CPHY CDR Control 00002000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI_CPHY_To_DEBUG_EN	RG_CSI_CPHY_To_BIST_EN	RG_CSI_CPHY_To_BIST_AB											
Type			RW	RW	RW											
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_To_BIST_AB		RG_CSI_CPHY_To_HSDET_SEL					RG_CSI_CPHY_To_FORCE_INIT	RG_CSI_CPHY_To_SYNC_INIT_SEL	RG_CSI_CPHY_To_SYMCK_INVERT		RG_CSI_CPHY_To_CDR_LATE_CODE				
Type	RW		RW					RW	RW	RW		RW				
Reset	0	0	1	0				0	0	0		0	0	0	0	0

Bit(s)	Name	Description
29	RG_CSI_CPHY_To_DEBUG_EN	
28	RG_CSI_CPHY_To_BIST_EN	
27:14	RG_CSI_CPHY_To_BIST_AB	
13:12	RG_CSI_CPHY_To_HSDET_SEL	
8	RG_CSI_CPHY_To_FORCE_INIT	[NORMAL]1'b0: Self [NORMAL]1'b1: DA
7	RG_CSI_CPHY_To_SYNC_INIT_SEL	[NORMAL]1'b0: Self [NORMAL]1'b1: DA
6	RG_CSI_CPHY_To_SYMCK_INVERT	
4:0	RG_CSI_CPHY_To_CDR_LATE_C	

Bit(s)	Name	Description
	ODE	

10217030 MIPI_RX_AN A30_CSI0A **CPHY CDR Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI_CPHY_To_BIST_CA													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_To_DEBUG_SEL		RG_CSI_CPHY_To_BIST_BC													
Type	RW		RW													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	RG_CSI_CPHY_To_BIST_CA	
15:14	RG_CSI_CPHY_To_DEBUG_SEL	
13:0	RG_CSI_CPHY_To_BIST_BC	

10217034 MIPI_RX_AN A34_CSI0A **CPHY CDR Control** **0000888F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CSI_CPHY_T1_CDR_EARLY_CODE					RG_CSI_CPHY_T1_CDR_INIT_CODE							RG_CSI_CPHY_T1_CDR_MANUAL_EN
Type				RW					RW							RW
Reset				0	0	0	0	0	0	0	0	0	0			0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_T1_CDR_CA_WIDTH			RG_CSI_CPHY_T1_CDR_BC_WIDTH					RG_CSI_CPHY_T1_CDR_AB_WIDTH				RG_CSI_CPHY_T1_CDR_LPF_CTRL		RG_CSI_CPHY_T1_CDR_AUTOLOAD_EN	RG_CSI_CPHY_T1_CDR_DIRECT_EN
Type	RW			RW					RW				RW		RW	RW
Reset	1	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1

Bit(s)	Name	Description
28:24	RG_CSI_CPHY_T1_CDR_EARLY_CODE	
23:19	RG_CSI_CPHY_T1_CDR_INIT_CODE	
16	RG_CSI_CPHY_T1_CDR_MANUAL_EN	
15:12	RG_CSI_CPHY_T1_CDR_CA_WIDTH	Filter out coding jitter

Bit(s)	Name	Description
11:8	RG_CSI_CPHY_T1_CDR_BC_WIDTH	Filter out coding jitter
7:4	RG_CSI_CPHY_T1_CDR_AB_WIDTH	Filter out coding jitter
3:2	RG_CSI_CPHY_T1_CDR_LPF_CTRL	
1	RG_CSI_CPHY_T1_CDR_AUTOLOAD_EN	
0	RG_CSI_CPHY_T1_CDR_DIRECT_EN	Direct Sample Mode Enable

10217038 MIPI_RX_ANA38_CSI0A CPHY CDR Control 00002000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI_CPHY_T1_DEBUG_EN	RG_CSI_CPHY_T1_BIST_EN	RG_CSI_CPHY_T1_BIST_AB											
Type			RW	RW	RW											
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_T1_BIST_AB		RG_CSI_CPHY_T1_HSDET_SEL					RG_CSI_CPHY_T1_FORCE_INIT	RG_CSI_CPHY_T1_SYNC_INIT_SEL	RG_CSI_CPHY_T1_SYMCK_INVERT		RG_CSI_CPHY_T1_CDR_LATE_CODE				
Type	RW		RW					RW	RW	RW		RW				
Reset	0	0	1	0				0	0	0		0	0	0	0	0

Bit(s)	Name	Description
29	RG_CSI_CPHY_T1_DEBUG_EN	
28	RG_CSI_CPHY_T1_BIST_EN	
27:14	RG_CSI_CPHY_T1_BIST_AB	
13:12	RG_CSI_CPHY_T1_HSDET_SEL	
8	RG_CSI_CPHY_T1_FORCE_INIT	[NORMAL]1'b0: Self [NORMAL]1'b1: DA
7	RG_CSI_CPHY_T1_SYNC_INIT_SEL	[NORMAL]1'b0: Self [NORMAL]1'b1: DA
6	RG_CSI_CPHY_T1_SYMCK_INVERT	
4:0	RG_CSI_CPHY_T1_CDR_LATE_CODE	

1021703C MIPI_RX_ANA3C_CSI0A CPHY CDR Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI_CPHY_T1_BIST_CA													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RG_CSI_CPHY_T1_DEBUG_SEL		RG_CSI_CPHY_T1_BIST_BC													
Type	RW		RW													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	RG_CSI_CPHY_T1_BIST_CA	
15:14	RG_CSI_CPHY_T1_DEBUG_SEL	
13:0	RG_CSI_CPHY_T1_BIST_BC	

10217040 MIPI_RX_ANA40_CSI0A GPI Control 40404040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_CSI_L1N_GPI_G	RG_CSI_L1N_GPI_RDSEL		RG_CSI_L1N_GPI_PD	RG_CSI_L1N_GPI_PU	RG_CSI_L1N_GPI_SMT	RG_CSI_L1N_GPI_IES		RG_CSI_L1P_GPI_G	RG_CSI_L1P_GPI_RDSEL		RG_CSI_L1P_GPI_PD	RG_CSI_L1P_GPI_PU	RG_CSI_L1P_GPI_SMT	RG_CSI_L1P_GPI_IES
Type		RW	RW		RW	RW	RW	RW		RW	RW		RW	RW	RW	RW
Reset		1	0	0	0	0	0	0		1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI_L0N_GPI_G	RG_CSI_L0N_GPI_RDSEL		RG_CSI_L0N_GPI_PD	RG_CSI_L0N_GPI_PU	RG_CSI_L0N_GPI_SMT	RG_CSI_L0N_GPI_IES		RG_CSI_L0P_GPI_G	RG_CSI_L0P_GPI_RDSEL		RG_CSI_L0P_GPI_PD	RG_CSI_L0P_GPI_PU	RG_CSI_L0P_GPI_SMT	RG_CSI_L0P_GPI_IES
Type		RW	RW		RW	RW	RW	RW		RW	RW		RW	RW	RW	RW
Reset		1	0	0	0	0	0	0		1	0	0	0	0	0	0

Bit(s)	Name	Description
30	RG_CSI_L1N_GPI_G	**RX Input Control Gating**
29:28	RG_CSI_L1N_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
27	RG_CSI_L1N_GPI_PD	**75K pull-down resistor control. High activiate.**
26	RG_CSI_L1N_GPI_PU	**75K pull-up resistor control. High activiate.**
25	RG_CSI_L1N_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
24	RG_CSI_L1N_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.
22	RG_CSI_L1P_GPI_G	**RX Input Control Gating**
21:20	RG_CSI_L1P_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable

Bit(s)	Name	Description
		Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
19	RG_CSI_L1P_GPI_PD	**75K pull-down resistor control. High activiate.**
18	RG_CSI_L1P_GPI_PU	**75K pull-up resistor control. High activiate.**
17	RG_CSI_L1P_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
16	RG_CSI_L1P_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.
14	RG_CSI_L0N_GPI_G	**RX Input Control Gating**
13:12	RG_CSI_L0N_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
11	RG_CSI_L0N_GPI_PD	**75K pull-down resistor control. High activiate.**
10	RG_CSI_L0N_GPI_PU	**75K pull-up resistor control. High activiate.**
9	RG_CSI_L0N_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
8	RG_CSI_L0N_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.
6	RG_CSI_L0P_GPI_G	**RX Input Control Gating**
5:4	RG_CSI_L0P_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
3	RG_CSI_L0P_GPI_PD	**75K pull-down resistor control. High activiate.**
2	RG_CSI_L0P_GPI_PU	**75K pull-up resistor control. High activiate.**
1	RG_CSI_L0P_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
0	RG_CSI_L0P_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.

10217044 MIPI_RX_AN_A44_CSI0A GPI Control 00004040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI_L2N_GPI_G	RG_CSI_L2N_GPI_RDSEL		RG_CSI_L2N_GPI_PD	RG_CSI_L2N_GPI_PU	RG_CSI_L2N_GPI_SMT	RG_CSI_L2N_GPI_IES		RG_CSI_L2P_GPI_G	RG_CSI_L2P_GPI_RDSEL		RG_CSI_L2P_GPI_PD	RG_CSI_L2P_GPI_PU	RG_CSI_L2P_GPI_SMT	RG_CSI_L2P_GPI_IES
Type		RW	RW		RW	RW	RW	RW		RW	RW		RW	RW	RW	RW
Reset		1	0	0	0	0	0	0		1	0	0	0	0	0	0

Bit(s)	Name	Description
14	RG_CSI_L2N_GPI_G	**RX Input Control Gating**
13:12	RG_CSI_L2N_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
11	RG_CSI_L2N_GPI_PD	**75K pull-down resistor control. High activiate.**
10	RG_CSI_L2N_GPI_PU	**75K pull-up resistor control. High activiate.**
9	RG_CSI_L2N_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
8	RG_CSI_L2N_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.
6	RG_CSI_L2P_GPI_G	**RX Input Control Gating**
5:4	RG_CSI_L2P_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
3	RG_CSI_L2P_GPI_PD	**75K pull-down resistor control. High activiate.**
2	RG_CSI_L2P_GPI_PU	**75K pull-up resistor control. High activiate.**
1	RG_CSI_L2P_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
0	RG_CSI_L2P_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.

10217048 MIPI_RX_ANA48_CSI0A RGS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AD_CSI_CPHY_T1_DEBUG_OUT	AD_CSI_CPHY_T1_BIST_CHECK_OU	AD_CSI_CPHY_T0_DEBUG_OUT	AD_CSI_CPHY_T0_BIST_CHECK_OU	AD_CSI_L2N_GPI_OUT	AD_CSI_L2P_GPI_OUT	AD_CSI_L1N_GPI_OUT	AD_CSI_L1P_GPI_OUT	AD_CSI_L0N_GPI_OUT	AD_CSI_L0P_GPI_OUT

								T		T						
Type							RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RGS_CSI_CPHY_T1_CDR_CODE								RGS_CSI_CPHY_To_CDR_CODE				
Type				RU								RU				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
25	AD_CSI_CPHY_T1_DEBUG_OUT	
24	AD_CSI_CPHY_T1_BIST_CHECK_OUT	
23	AD_CSI_CPHY_To_DEBUG_OUT	
22	AD_CSI_CPHY_To_BIST_CHECK_OUT	
21	AD_CSI_L2N_GPI_OUT	
20	AD_CSI_L2P_GPI_OUT	
19	AD_CSI_L1N_GPI_OUT	
18	AD_CSI_L1P_GPI_OUT	
17	AD_CSI_LoN_GPI_OUT	
16	AD_CSI_LoP_GPI_OUT	
12:8	RGS_CSI_CPHY_T1_CDR_CODE	
4:0	RGS_CSI_CPHY_To_CDR_CODE	

1021704C MIPI_RX_AN A4C_CSIoA **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DA_CSI_CDPHY_L2N_T1C_HSRT_EN	DA_CSI_CDPHY_L2P_T1B_HSRT_EN	DA_CSI_CDPHY_L1N_T1A_HSRT_EN	DA_CSI_CDPHY_L1P_ToC_HSRT_EN	DA_CSI_CDPHY_LoN_ToB_HSRT_EN	DA_CSI_CDPHY_LoP_ToA_HSRT_EN	AD_CSI_DPHY_L2N_HSDET_OUT	DA_CSI_DPHY_L2N_HSDET_RSTB	AD_CSI_DPHY_L2P_HSDET_OUT	DA_CSI_DPHY_L2P_HSDET_RSTB	AD_CSI_DPHY_L1N_HSDET_OUT	DA_CSI_DPHY_L1N_HSDET_RSTB	AD_CSI_DPHY_L1P_HSDET_OUT	DA_CSI_DPHY_L1P_HSDET_RSTB
Type			RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AD_CSI_DPHY_LoN_HSDET_OUT	DA_CSI_DPHY_LoN_HSDET_RSTB	AD_CSI_DPHY_LoP_HSDET_OUT	DA_CSI_DPHY_LoP_HSDET_RSTB	AD_CSI_CDPHY_L2N_T1C_LPRX_OUT	DA_CSI_CDPHY_L2N_T1C_LPRX_EN	AD_CSI_CDPHY_L2P_T1B_LPRX_OUT	DA_CSI_CDPHY_L2P_T1B_LPRX_EN	AD_CSI_CDPHY_L1N_T1A_LPRX_OUT	DA_CSI_CDPHY_L1N_T1A_LPRX_EN	AD_CSI_CDPHY_L1P_ToC_LPRX_OUT	DA_CSI_CDPHY_L1P_ToC_LPRX_EN	AD_CSI_CDPHY_LoN_ToB_LPRX_OUT	DA_CSI_CDPHY_LoN_ToB_LPRX_EN	AD_CSI_CDPHY_LoP_ToA_LPRX_OUT	DA_CSI_CDPHY_LoP_ToA_LPRX_EN
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29	DA_CSI_CDPHY_L2N_T1C_HSRT_EN	
28	DA_CSI_CDPHY_L2P_T1B_HSRT_EN	
27	DA_CSI_CDPHY_L1N_T1A_HSRT_EN	
26	DA_CSI_CDPHY_L1P_ToC_HSRT	

Bit(s)	Name	Description
	_EN	
25	DA_CSI_CDPHY_L0N_T0B_HSRT_EN	
24	DA_CSI_CDPHY_L0P_T0A_HSRT_EN	
23	AD_CSI_DPHY_L2N_HSDET_OUT	
22	DA_CSI_DPHY_L2N_HSDET_RSTB	
21	AD_CSI_DPHY_L2P_HSDET_OUT	
20	DA_CSI_DPHY_L2P_HSDET_RSTB	
19	AD_CSI_DPHY_L1N_HSDET_OUT	
18	DA_CSI_DPHY_L1N_HSDET_RSTB	
17	AD_CSI_DPHY_L1P_HSDET_OUT	
16	DA_CSI_DPHY_L1P_HSDET_RSTB	
15	AD_CSI_DPHY_L0N_HSDET_OUT	
14	DA_CSI_DPHY_L0N_HSDET_RSTB	
13	AD_CSI_DPHY_L0P_HSDET_OUT	
12	DA_CSI_DPHY_L0P_HSDET_RSTB	
11	AD_CSI_CDPHY_L2N_T1C_LPRX_OUT	
10	DA_CSI_CDPHY_L2N_T1C_LPRX_EN	
9	AD_CSI_CDPHY_L2P_T1B_LPRX_OUT	
8	DA_CSI_CDPHY_L2P_T1B_LPRX_EN	
7	AD_CSI_CDPHY_L1N_T1A_LPRX_OUT	
6	DA_CSI_CDPHY_L1N_T1A_LPRX_EN	
5	AD_CSI_CDPHY_L1P_T0C_LPRX_OUT	
4	DA_CSI_CDPHY_L1P_T0C_LPRX_EN	
3	AD_CSI_CDPHY_L0N_T0B_LPRX_OUT	
2	DA_CSI_CDPHY_L0N_T0B_LPRX_EN	
1	AD_CSI_CDPHY_L0P_T0A_LPRX_OUT	
0	DA_CSI_CDPHY_L0P_T0A_LPRX_EN	

10217050 MIPI_RX_ANA50_CSI0A **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AD_CSI_CPHY_ToCA_HSAMP_OS_CK	AD_CSI_CPHY_ToCA_HSAMP_OS_OUT	DA_CSI_CPHY_ToCA_HSAMP_OS_CODE					DA_CSI_CPHY_ToCA_HSAMP_OS_CAL_EN	DA_CSI_CPHY_ToCA_HSAMP_OS_APPLY	DA_CSI_CPHY_ToCA_HSAMP_EN

Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							AD_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CK	AD_CSI_CDPHY_Lo_ToAB_HSAMP_OS_OUT	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CODE					DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CAL_EN	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_APPLY	DA_CSI_CDPHY_Lo_ToAB_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25	AD_CSI_CPHY_ToCA_HSAMP_OS_CK	
24	AD_CSI_CPHY_ToCA_HSAMP_OS_OUT	
23:19	DA_CSI_CPHY_ToCA_HSAMP_OS_CODE	
18	DA_CSI_CPHY_ToCA_HSAMP_OS_CAL_EN	
17	DA_CSI_CPHY_ToCA_HSAMP_OS_APPLY	
16	DA_CSI_CPHY_ToCA_HSAMP_EN	
9	AD_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CK	
8	AD_CSI_CDPHY_Lo_ToAB_HSAMP_OS_OUT	
7:3	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CODE	
2	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CAL_EN	
1	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_APPLY	
0	DA_CSI_CDPHY_Lo_ToAB_HSAMP_EN	

10217054 MIPI_RX_AN A54_CSI0A DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AD_CSI_CDPHY_L1_T1AB_HSAMP_OS_CK	AD_CSI_CDPHY_L1_T1AB_HSAMP_OS_OUT	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_CODE					DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_CAL_EN	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_APPLY	DA_CSI_CDPHY_L1_T1AB_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							AD_CSI_CPHY_ToBC	AD_CSI_CPHY_ToBC	DA_CSI_CPHY_ToBC_HSAMP_OS_CODE					DA_CSI_CPHY_ToBC	DA_CSI_CPHY_ToBC	DA_CSI_CPHY_ToBC

							_HSAMP_OS_CK	_HSAMP_OS_OUT						_HSAMP_OS_CAL_EN	_HSAMP_OS_APPLY	_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25	AD_CSI_CDPHY_L1_T1AB_HSAMP_OS_CK	
24	AD_CSI_CDPHY_L1_T1AB_HSAMP_OS_OUT	
23:19	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_CODE	
18	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_CAL_EN	
17	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_APPLY	
16	DA_CSI_CDPHY_L1_T1AB_HSAMP_EN	
9	AD_CSI_CPHY_ToBC_HSAMP_OS_CK	
8	AD_CSI_CPHY_ToBC_HSAMP_OS_OUT	
7:3	DA_CSI_CPHY_ToBC_HSAMP_OS_CODE	
2	DA_CSI_CPHY_ToBC_HSAMP_OS_CAL_EN	
1	DA_CSI_CPHY_ToBC_HSAMP_OS_APPLY	
0	DA_CSI_CPHY_ToBC_HSAMP_EN	

10217058 MIPI_RX_AN A58_CSI0A **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AD_CSI_CDPHY_L2_T1BC_HSAMP_OS_CK	AD_CSI_CDPHY_L2_T1BC_HSAMP_OS_OUT	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_CODE					DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_CAL_EN	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_APPLY	DA_CSI_CDPHY_L2_T1BC_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							AD_CSI_CPHY_T1CA_HSAMP_OS_CK	AD_CSI_CPHY_T1CA_HSAMP_OS_OUT	DA_CSI_CPHY_T1CA_HSAMP_OS_CODE					DA_CSI_CPHY_T1CA_HSAMP_OS_CAL_EN	DA_CSI_CPHY_T1CA_HSAMP_OS_APPLY	DA_CSI_CPHY_T1CA_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25	AD_CSI_CDPHY_L2_T1BC_HSAMP_OS_CK	
24	AD_CSI_CDPHY_L2_T1BC_HSAMP_OS_OUT	
23:19	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_CODE	
18	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_CAL_EN	
17	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_APPLY	
16	DA_CSI_CDPHY_L2_T1BC_HSAMP_EN	
9	AD_CSI_CPHY_T1CA_HSAMP_OS_CK	
8	AD_CSI_CPHY_T1CA_HSAMP_OS_OUT	
7:3	DA_CSI_CPHY_T1CA_HSAMP_OS_CODE	
2	DA_CSI_CPHY_T1CA_HSAMP_OS_CAL_EN	
1	DA_CSI_CPHY_T1CA_HSAMP_OS_APPLY	
0	DA_CSI_CPHY_T1CA_HSAMP_EN	

1021705C MIPI_RX_ANA5C_CSI0A **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSI_DPHY_Lo_DELAY_CODE							AD_CSI_DPHY_Lo_BYPASS_BYTE_DATA							
Type		RU							RU							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_DPHY_Lo_DELAY_APPLY	DA_CSI_DPHY_Lo_DELAY_EN	AD_CSI_DPHY_Lo_BYPASS_BYTE_CK	AD_CSI_DPHY_Lo_SYNC_DETECT	AD_CSI_DPHY_Lo_BYTE_DATA								AD_CSI_DPHY_Lo_BYTE_CK	DA_CSI_DPHY_Lo_DES_SYNC_INIT	DA_CSI_DPHY_Lo_DES_EN	DA_CSI_DPHY_Lo_SAMP_EN
Type	RU	RU	RU	RU	RU								RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	DA_CSI_DPHY_Lo_DELAY_CODE	
23:16	AD_CSI_DPHY_Lo_BYPASS_BYTE_DATA	
15	DA_CSI_DPHY_Lo_DELAY_APPLY	
14	DA_CSI_DPHY_Lo_DELAY_EN	
13	AD_CSI_DPHY_Lo_BYPASS_BYTE_CK	
12	AD_CSI_DPHY_Lo_SYNC_DETECT	
11:4	AD_CSI_DPHY_Lo_BYTE_DATA	
3	AD_CSI_DPHY_Lo_BYTE_CK	
2	DA_CSI_DPHY_Lo_DES_SYNC_INIT	

Bit(s)	Name	Description
1	DA_CSI_DPHY_L0_DES_EN	
0	DA_CSI_DPHY_L0_SAMP_EN	

10217060 MIPI_RX_AN_A60_CSI0A DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSI_DPHY_L1_DELAY_CODE							AD_CSI_DPHY_L1_BYPASS_BYTE_DATA							
Type		RU							RU							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_DPHY_L1_DELAY_APPLY	DA_CSI_DPHY_L1_DELAY_EN	AD_CSI_DPHY_L1_BYPASS_BYTE_CK	AD_CSI_DPHY_L1_SYNC_DETECT	AD_CSI_DPHY_L1_BYTE_DATA								AD_CSI_DPHY_L1_BYTE_CK	DA_CSI_DPHY_L1_DES_SYNC_INIT	DA_CSI_DPHY_L1_DES_EN	DA_CSI_DPHY_L1_SAMP_EN
Type	RU	RU	RU	RU	RU								RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	DA_CSI_DPHY_L1_DELAY_CODE	
23:16	AD_CSI_DPHY_L1_BYPASS_BYTE_DATA	
15	DA_CSI_DPHY_L1_DELAY_APPLY	
14	DA_CSI_DPHY_L1_DELAY_EN	
13	AD_CSI_DPHY_L1_BYPASS_BYTE_CK	
12	AD_CSI_DPHY_L1_SYNC_DETECT	
11:4	AD_CSI_DPHY_L1_BYTE_DATA	
3	AD_CSI_DPHY_L1_BYTE_CK	
2	DA_CSI_DPHY_L1_DES_SYNC_INIT	
1	DA_CSI_DPHY_L1_DES_EN	
0	DA_CSI_DPHY_L1_SAMP_EN	

10217064 MIPI_RX_AN_A64_CSI0A DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSI_DPHY_L2_DELAY_CODE							AD_CSI_DPHY_L2_BYPASS_BYTE_DATA							
Type		RU							RU							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_DPHY_L2_DELAY_APPLY	DA_CSI_DPHY_L2_DELAY_EN	AD_CSI_DPHY_L2_BYPASS_BYTE_CK	AD_CSI_DPHY_L2_SYNC_DETECT	AD_CSI_DPHY_L2_BYTE_DATA								AD_CSI_DPHY_L2_BYTE_CK	DA_CSI_DPHY_L2_DES_SYNC_INIT	DA_CSI_DPHY_L2_DES_EN	DA_CSI_DPHY_L2_SAMP_EN

Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	DA_CSI_DPHY_L2_DELAY_CODE	
23:16	AD_CSI_DPHY_L2_BYPASS_BYTE_DATA	
15	DA_CSI_DPHY_L2_DELAY_APPLY	
14	DA_CSI_DPHY_L2_DELAY_EN	
13	AD_CSI_DPHY_L2_BYPASS_BYTE_CK	
12	AD_CSI_DPHY_L2_SYNC_DETECT	
11:4	AD_CSI_DPHY_L2_BYTE_DATA	
3	AD_CSI_DPHY_L2_BYTE_CK	
2	DA_CSI_DPHY_L2_DES_SYNC_INIT	
1	DA_CSI_DPHY_L2_DES_EN	
0	DA_CSI_DPHY_L2_SAMP_EN	

10217068 MIPI_RX_ANA68_CSI0A **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AD_CSI_CPHY_To_HSDET_OUT	DA_CSI_CPHY_To_SYNC_INIT
Type															RU	RU
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_CPHY_To_DES_EN	DA_CSI_CPHY_To_CDR_EN	AD_CSI_CPHY_To_AB													
Type	RU	RU	RU													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	AD_CSI_CPHY_To_HSDET_OUT	
16	DA_CSI_CPHY_To_SYNC_INIT	
15	DA_CSI_CPHY_To_DES_EN	
14	DA_CSI_CPHY_To_CDR_EN	
13:0	AD_CSI_CPHY_To_AB	

1021706C MIPI_RX_ANA6C_CSI0A **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AD_CSI_CPHY_To_BC													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	AD_CSI_CPHY_To_BC	

10217070 MIPI_RX_AN A70_CSI0A **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AD_CSI_CPHY_To_CA													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	AD_CSI_CPHY_To_CA	

10217074 MIPI_RX_AN A74_CSI0A **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AD_CSI_CPHY_T1_HSDET_OUT	DA_CSI_CPHY_T1_SYNC_INIT
Type															RU	RU
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_CPHY_T1_DES_EN	DA_CSI_CPHY_T1_CDR_EN	AD_CSI_CPHY_T1_AB													
Type	RU	RU	RU													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	AD_CSI_CPHY_T1_HSDET_OUT	
16	DA_CSI_CPHY_T1_SYNC_INIT	
15	DA_CSI_CPHY_T1_DES_EN	
14	DA_CSI_CPHY_T1_CDR_EN	
13:0	AD_CSI_CPHY_T1_AB	

10217078 MIPI_RX_ANA78_CSI0A **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AD_CSI_CPHY_T1_BC													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	AD_CSI_CPHY_T1_BC	

1021707C MIPI_RX_ANA7C_CSI0A **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AD_CSI_CPHY_T1_CA													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	AD_CSI_CPHY_T1_CA	

10217080 MIPI_RX_WRAPPER80_CSI0A **WRAPPER** **04000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CSR_CSI0_DPHY_MUX			CSR_SW_RST				CSR_CSI1_CPHY_RST_MODE		CSR_CSI1_DPHY_RST_MODE		CSR_CSI0_CPHY_RST_MODE		CSR_CSI0_DPHY_RST_MODE	
Type		RW			RW				RW		RW		RW		RW	
Reset		0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_CSI_MON_MUX								CSR_CSI_MODE				CSR_CSI1_DPHY_MUX		CSR_HSDET_MODE	CSR_CSI_CLK_MON
Type	RW								RW				RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:28	CSR_CSI0_DPHY_MUX	
27:24	CSR_SW_RST	

Bit(s)	Name	Description
23:22	CSR_CSI1_CPHY_RST_MODE	0: sync init 1: hsrx_en 2: sw rst 3: hw rst
21:20	CSR_CSI1_DPHY_RST_MODE	0: sync init 1: hsrx_en 2: sw rst 3: hw rst
19:18	CSR_CSI0_CPHY_RST_MODE	0: sync init 1: hsrx_en 2: sw rst 3: hw rst
17:16	CSR_CSI0_DPHY_RST_MODE	0: sync init 1: hsrx_en 2: sw rst 3: hw rst
15:8	CSR_CSI_MON_MUX	
7:4	CSR_CSI_MODE	0:4 lane 1:2/2l lane 2:cphy 4:cphy/2 lane
3:2	CSR_CSI1_DPHY_MUX	
1	CSR_HSDET_MODE	0:dn 1:dp
0	CSR_CSI_CLK_MON	Enable Clock monitor

10217084 MIPI_RX_WRAPPER84_CSI0A WRAPPER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI_DEBUG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI_DEBUG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSI_DEBUG_OUT	

10217088 MIPI_RX_WRAPPER88_CSI0A WRAPPER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_MODE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_MODE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_MODE_0	

1021708C MIPI_RX_WRAPPER8C_CSIoA **WRAPPER** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_MODE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_MODE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_MODE_1	

10217090 MIPI_RX_WRAPPER90_CSIoA **WRAPPER** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_MODE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_MODE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_MODE_2	

10217094 MIPI_RX_WRAPPER94_CSIoA **WRAPPER** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_VALUE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_VALUE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
31:0	CSR_SW_VALUE_0	

10217098 MIPI_RX_WRAPPER98_CSI0A WRAPPER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_VALUE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_VALUE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_VALUE_1	

1021709C MIPI_RX_WRAPPER9C_CSI0A WRAPPER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_VALUE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_VALUE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_VALUE_2	

10217200 MIPI_RX_ANA00_CSI0B 2D1C Global Control 00000492

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_CSI_DPHY_L2_CKSEL	RG_CSI_DPHY_L2_CKMODE_EN	RG_CSI_DPHY_L2_BYPASS_SYNC	RG_CSI_DPHY_L1_CKSEL	RG_CSI_DPHY_L1_CKMODE_EN	RG_CSI_DPHY_L1_BYPASS_SYNC	RG_CSI_DPHY_L0_CKSEL	RG_CSI_DPHY_L0_CKMODE_EN	RG_CSI_DPHY_L0_BYPASS_SYNC	RG_CSI_BG_CORE_EN	RG_CSI_BG_LPF_EN	RG_CSI_HSAMP_PROTECT_EN	RG_CSI_CPHY_EN
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	1	0	0	1	0	0	1	0	0	1	0

Bit(s)	Name	Description
12	RG_CSI_DPHY_L2_CKSEL	**Data Mode** [NORMAL]1'b0: Sample data by Local Clock [NORMAL]1'b1: Sample data by Common Clock CK Mode [NORMAL]1'b0: Connect to Local Clock [NORMAL]1'b1: Connect to Common Clock
11	RG_CSI_DPHY_L2_CKMODE_EN	**[NORMAL]1'b0: Data Mode** [NORMAL]1'b1: CK Mode
10	RG_CSI_DPHY_L2_BYPASS_SYNC	**Bypass or Sync Mode Selection** [NORMAL]1'b0: Sync Mode [NORMAL]1'b1: Bypass Mode
9	RG_CSI_DPHY_L1_CKSEL	**Data Mode** [NORMAL]1'b0: Sample data by Local Clock [NORMAL]1'b1: Sample data by Common Clock CK Mode [NORMAL]1'b0: Connect to Local Clock [NORMAL]1'b1: Connect to Common Clock
8	RG_CSI_DPHY_L1_CKMODE_EN	**[NORMAL]1'b0: Data Mode** [NORMAL]1'b1: CK Mode
7	RG_CSI_DPHY_L1_BYPASS_SYNC	**Bypass or Sync Mode Selection** [NORMAL]1'b0: Sync Mode [NORMAL]1'b1: Bypass Mode
6	RG_CSI_DPHY_L0_CKSEL	**Data Mode** [NORMAL]1'b0: Sample data by Local Clock [NORMAL]1'b1: Sample data by Common Clock CK Mode [NORMAL]1'b0: Connect to Local Clock [NORMAL]1'b1: Connect to Common Clock
5	RG_CSI_DPHY_L0_CKMODE_EN	**[NORMAL]1'b0: Data Mode** [NORMAL]1'b1: CK Mode
4	RG_CSI_DPHY_L0_BYPASS_SYNC	**Bypass or Sync Mode Selection** [NORMAL]1'b0: Sync Mode [NORMAL]1'b1: Bypass Mode
3	RG_CSI_BG_CORE_EN	**[NORMAL]1'b0: Bandgap Disable** [NORMAL]1'b1: Bandgap Enable
2	RG_CSI_BG_LPF_EN	**[NORMAL]1'b0: Bandgap low pass filter Disable** [NORMAL]1'b1: Bandgap low pass filter Enable
1	RG_CSI_HSAMP_PROTECT_EN	**HSAMP Protection** [NORMAL]1'b0: Disable [NORMAL]1'b1: Enable
0	RG_CSI_CPHY_EN	**1'b0: DPHY Mode** 1'b1: CPHY Mode

10217204 MIPI_RX_AN_A04_CSI0B 2D1C Global Control 00084444

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CSI_FORCE_HSRT_EN	RG_CSI_BG_VREF_SEL								RG_CSI_BG_VREF_SEL			
Type				RW	RW								RW			
Reset				0	0	0	0	0					1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI_BG_HSDET_VTL_SEL				RG_CSI_BG_HSDET_VTH_SEL				RG_CSI_BG_LPRX_VTL_SEL				RG_CSI_BG_LPRX_VTH_SEL		

Type		RW				RW				RW				RW		
Reset		1	0	0		1	0	0		1	0	0		1	0	0

Bit(s)	Name	Description
28	RG_CSI_FORCE_HSRT_EN	**Force HSRT Enable to do FT calibration and eFuse**
27:24	RG_CSI_BG_MON_VREF_SEL	**Monitor Selection**
19:16	RG_CSI_BG_VREF_SEL	**HSAMP LDO Reference Voltage** Default 0.9V
14:12	RG_CSI_BG_HSDET_VTL_SEL	**HSDET VTH Selection** Default 0.12V
10:8	RG_CSI_BG_HSDET_VTH_SEL	**HSDET VTH Selection** Default 0.15V
6:4	RG_CSI_BG_LPRX_VTL_SEL	**LPRX VTL Selection** Default 0.70V
2:0	RG_CSI_BG_LPRX_VTH_SEL	**LPRX VTH Selection** Default 0.75V

10217208 MIPI_RX_AN_A08_CSI0B High Speed Termination Control 10101010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CSI_L1N_T1A_HSRT_CODE								RG_CSI_L1P_T0C_HSRT_CODE				
Type				RW								RW				
Reset				1	0	0	0	0				1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_CSI_L0N_T0B_HSRT_CODE								RG_CSI_L0P_T0A_HSRT_CODE				
Type				RW								RW				
Reset				1	0	0	0	0				1	0	0	0	0

Bit(s)	Name	Description
28:24	RG_CSI_L1N_T1A_HSRT_CODE	**Termination code** 800ohm/(8+N) Requires Calibration & Efuse on FT
20:16	RG_CSI_L1P_T0C_HSRT_CODE	**Termination code** 800ohm/(8+N) Requires Calibration & Efuse on FT
12:8	RG_CSI_L0N_T0B_HSRT_CODE	**Termination code** 800ohm/(8+N) Requires Calibration & Efuse on FT
4:0	RG_CSI_L0P_T0A_HSRT_CODE	**Termination code** 800ohm/(8+N) Requires Calibration & Efuse on FT

1021720C MIPI_RX_AN_A0C_CSI0B High Speed Termination Control 00001010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_CSI_L2N_T1C_HSR								RG_CSI_L2P_T1B_HSRT_C				

				T_CODE								ODE				
Type				RW								RW				
Reset				1	0	0	0	0				1	0	0	0	0

Bit(s)	Name	Description
12:8	RG_CSI_L2N_T1C_HSRT_CODE	**Termination code** 800ohm/(8+N) Requires Calibration & Efuse on FT
4:0	RG_CSI_L2P_T1B_HSRT_CODE	**Termination code** 800ohm/(8+N) Requires Calibration & Efuse on FT

10217210 MIPI_RX_AN_A10_CSI0B **Bandgap Voltage for Delay Line Calibration** **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_CPHY_T0_VREF_SEL						RG_CSI_CPHY_T0_CDR_DELAYCAL_RSTB	RG_CSI_CPHY_T0_CDR_DELAYCAL_EN	RG_CSI_DPHY_L2_VREF_SEL						RG_CSI_DPHY_L2_DELAYCAL_RSTB	RG_CSI_DPHY_L2_DELAYCAL_EN
Type	RW						RW	RW	RW						RW	RW
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_DPHY_L1_VREF_SEL						RG_CSI_DPHY_L1_DELAYCAL_RSTB	RG_CSI_DPHY_L1_DELAYCAL_EN	RG_CSI_DPHY_L0_VREF_SEL						RG_CSI_DPHY_L0_DELAYCAL_RSTB	RG_CSI_DPHY_L0_DELAYCAL_EN
Type	RW						RW	RW	RW						RW	RW
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:26	RG_CSI_CPHY_T0_VREF_SEL	**D0 Delay Line Reference Voltage** Requires Software Calibration
25	RG_CSI_CPHY_T0_CDR_DELAYCAL_RSTB	**TRIO0 Delay Line Calibration Reset Bar**
24	RG_CSI_CPHY_T0_CDR_DELAYCAL_EN	**TRIO0 Delay Line Calibration Enable**
23:18	RG_CSI_DPHY_L2_VREF_SEL	**D0 Delay Line Reference Voltage** Requires Software Calibration
17	RG_CSI_DPHY_L2_DELAYCAL_RSTB	**D1 Delay Line Calibration Reset Bar**
16	RG_CSI_DPHY_L2_DELAYCAL_EN	**D1 Delay Line Calibration Enable**
15:10	RG_CSI_DPHY_L1_VREF_SEL	**D0 Delay Line Reference Voltage** Requires Software Calibration
9	RG_CSI_DPHY_L1_DELAYCAL_RSTB	**CK Delay Line Calibration Reset Bar**
8	RG_CSI_DPHY_L1_DELAYCAL_EN	**CK Delay Line Calibration Enable**
7:2	RG_CSI_DPHY_L0_VREF_SEL	**D0 Delay Line Reference Voltage** Requires Software Calibration
1	RG_CSI_DPHY_L0_DELAYCAL_R	**D0 Delay Line Calibration Reset Bar**

Bit(s)	Name	Description
0	STB RG_CSI_DPHY_Lo_DELAYCAL_EN	**Do Delay Line Calibration Enable**

10217214 MIPI_RX_ANA14_CSIoB **Bandgap Voltage for Delay Line Calibration** **00000080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSI_CPHY_T1_VREF_SEL						RG_CSI_CPHY_T1_CDR_DELAYCAL_RSTB	RG_CSI_CPHY_T1_CDR_DELAYCAL_EN
Type									RW						RW	RW
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSI_CPHY_T1_VREF_SEL	**Do Delay Line Reference Voltage** Requires Software Calibration
1	RG_CSI_CPHY_T1_CDR_DELAYCAL_RSTB	**TRIO1 Delay Line Calibration Reset Bar**
0	RG_CSI_CPHY_T1_CDR_DELAYCAL_EN	**TRIO1 Delay Line Calibration Enable**

10217218 MIPI_RX_ANA18_CSIoB **HS AMP Control** **88008800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_XX_ToCA_HSAMP_SRB				RG_CSI_XX_ToCA_HSAMP_SRA				RG_CSI_XX_ToCA_HSAMP_BW		RG_CSI_XX_ToCA_HSAMP_IS		RG_CSI_XX_ToCA_HSAMP_SCB	RG_CSI_XX_ToCA_HSAMP_SCA	RG_CSI_XX_ToCA_HSAMP_LPBK_TEST_EN	RG_CSI_XX_ToCA_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_Lo_ToAB_HSAMP_SRB				RG_CSI_Lo_ToAB_HSAMP_SRA				RG_CSI_Lo_ToAB_HSAMP_BW		RG_CSI_Lo_ToAB_HSA MP_IS		RG_CSI_Lo_ToAB_HSAMP_SCB	RG_CSI_Lo_ToAB_HSAMP_SCA	RG_CSI_Lo_ToAB_HSAMP_LPBK_TEST_EN	RG_CSI_Lo_ToAB_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW

Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	RG_CSI_XX_ToCA_HSAMP_SRB	
27:24	RG_CSI_XX_ToCA_HSAMP_SRA	
23:22	RG_CSI_XX_ToCA_HSAMP_BW	
21:20	RG_CSI_XX_ToCA_HSAMP_IS	
19	RG_CSI_XX_ToCA_HSAMP_SCB	
18	RG_CSI_XX_ToCA_HSAMP_SCA	
17	RG_CSI_XX_ToCA_HSAMP_LPBK_TEST_EN	
16	RG_CSI_XX_ToCA_HSAMP_MON_EN	
15:12	RG_CSI_Lo_ToAB_HSAMP_SRB	
11:8	RG_CSI_Lo_ToAB_HSAMP_SRA	
7:6	RG_CSI_Lo_ToAB_HSAMP_BW	
5:4	RG_CSI_Lo_ToAB_HSAMP_IS	
3	RG_CSI_Lo_ToAB_HSAMP_SCB	
2	RG_CSI_Lo_ToAB_HSAMP_SCA	
1	RG_CSI_Lo_ToAB_HSAMP_LPBK_TEST_EN	
0	RG_CSI_Lo_ToAB_HSAMP_MON_EN	

1021721C MIPI_RX_ANA1C_CSI0B HS AMP Control 88008800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_L1_T1AB_HSAMP_SRB				RG_CSI_L1_T1AB_HSAMP_SRA				RG_CSI_L1_T1AB_HSAMP_BW		RG_CSI_L1_T1AB_HSAMP_IS		RG_CSI_L1_T1AB_HSAMP_SCB	RG_CSI_L1_T1AB_HSAMP_SCA	RG_CSI_L1_T1AB_HSAMP_LPBK_TEST_EN	RG_CSI_L1_T1AB_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_XX_ToBC_HSAMP_SRB				RG_CSI_XX_ToBC_HSAMP_SRA				RG_CSI_XX_ToBC_HSAMP_BW		RG_CSI_XX_ToBC_HSAMP_IS		RG_CSI_XX_ToBC_HSAMP_SCB	RG_CSI_XX_ToBC_HSAMP_SCA	RG_CSI_XX_ToBC_HSAMP_LPBK_TEST_EN	RG_CSI_XX_ToBC_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	RG_CSI_L1_T1AB_HSAMP_SRB	
27:24	RG_CSI_L1_T1AB_HSAMP_SRA	
23:22	RG_CSI_L1_T1AB_HSAMP_BW	
21:20	RG_CSI_L1_T1AB_HSAMP_IS	
19	RG_CSI_L1_T1AB_HSAMP_SCB	
18	RG_CSI_L1_T1AB_HSAMP_SCA	

Bit(s)	Name	Description
17	RG_CSI_L1_T1AB_HSAMP_LPBK_TEST_EN	
16	RG_CSI_L1_T1AB_HSAMP_MON_EN	
15:12	RG_CSI_XX_T0BC_HSAMP_SRB	
11:8	RG_CSI_XX_T0BC_HSAMP_SRA	
7:6	RG_CSI_XX_T0BC_HSAMP_BW	
5:4	RG_CSI_XX_T0BC_HSAMP_IS	
3	RG_CSI_XX_T0BC_HSAMP_SCB	
2	RG_CSI_XX_T0BC_HSAMP_SCA	
1	RG_CSI_XX_T0BC_HSAMP_LPBK_TEST_EN	
0	RG_CSI_XX_T0BC_HSAMP_MON_EN	

10217220 MIPI_RX_AN_A20_CSI0B HS AMP Control 88008800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_L2_T1BC_HSAMP_SRB				RG_CSI_L2_T1BC_HSAMP_SRA				RG_CSI_L2_T1BC_HSAMP_BW		RG_CSI_L2_T1BC_HSAMP_IS		RG_CSI_L2_T1BC_HSAMP_SCB	RG_CSI_L2_T1BC_HSAMP_SCA	RG_CSI_L2_T1BC_HSAMP_LPBK_TEST_EN	RG_CSI_L2_T1BC_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_XX_T1CA_HSAMP_SRB				RG_CSI_XX_T1CA_HSAMP_SRA				RG_CSI_XX_T1CA_HSAMP_BW		RG_CSI_XX_T1CA_HSAMP_IS		RG_CSI_XX_T1CA_HSAMP_SCB	RG_CSI_XX_T1CA_HSAMP_SCA	RG_CSI_XX_T1CA_HSAMP_LPBK_TEST_EN	RG_CSI_XX_T1CA_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	RG_CSI_L2_T1BC_HSAMP_SRB	
27:24	RG_CSI_L2_T1BC_HSAMP_SRA	
23:22	RG_CSI_L2_T1BC_HSAMP_BW	
21:20	RG_CSI_L2_T1BC_HSAMP_IS	
19	RG_CSI_L2_T1BC_HSAMP_SCB	
18	RG_CSI_L2_T1BC_HSAMP_SCA	
17	RG_CSI_L2_T1BC_HSAMP_LPBK_TEST_EN	
16	RG_CSI_L2_T1BC_HSAMP_MON_EN	
15:12	RG_CSI_XX_T1CA_HSAMP_SRB	
11:8	RG_CSI_XX_T1CA_HSAMP_SRA	
7:6	RG_CSI_XX_T1CA_HSAMP_BW	
5:4	RG_CSI_XX_T1CA_HSAMP_IS	
3	RG_CSI_XX_T1CA_HSAMP_SCB	

Bit(s)	Name	Description
2	RG_CSI_XX_T1CA_HSAMP_SCA	
1	RG_CSI_XX_T1CA_HSAMP_LPBK_TEST_EN	
0	RG_CSI_XX_T1CA_HSAMP_MON_EN	

10217224 MIPI_RX_AN_A24_CSI0B DPHY Deserializer Control 0F000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_RESERVE											RG_CSI_DPHY_L2_SYNC_EDGE_SEL		RG_CSI_DPHY_L2_FORCE_SYNC		RG_CSI_DPHY_L2_BYPASS_BYTECK_INVERT
Type	RW											RW		RW		RW
Reset	0	0	0	0	1	1	1	1				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_DPHY_L2_BYTECK_INVERT		RG_CSI_DPHY_L1_SYNC_EDGE_SEL		RG_CSI_DPHY_L1_FORCE_SYNC		RG_CSI_DPHY_L1_BYPASS_BYTECK_INVERT	RG_CSI_DPHY_L1_BYTECK_INVERT			RG_CSI_DPHY_L0_SYNC_EDGE_SEL		RG_CSI_DPHY_L0_FORCE_SYNC		RG_CSI_DPHY_L0_BYPASS_BYTECK_INVERT	RG_CSI_DPHY_L0_BYTECK_INVERT
Type	RW		RW		RW		RW	RW			RW		RW		RW	RW
Reset	0		0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RG_CSI_RESERVE	
20:19	RG_CSI_DPHY_L2_SYNC_EDGE_SEL	
18:17	RG_CSI_DPHY_L2_FORCE_SYNC	
16	RG_CSI_DPHY_L2_BYPASS_BYTECK_INVERT	
15	RG_CSI_DPHY_L2_BYTECK_INVERT	
13:12	RG_CSI_DPHY_L1_SYNC_EDGE_SEL	
11:10	RG_CSI_DPHY_L1_FORCE_SYNC	
9	RG_CSI_DPHY_L1_BYPASS_BYTECK_INVERT	
8	RG_CSI_DPHY_L1_BYTECK_INVERT	
5:4	RG_CSI_DPHY_L0_SYNC_EDGE_SEL	
3:2	RG_CSI_DPHY_L0_FORCE_SYNC	
1	RG_CSI_DPHY_L0_BYPASS_BYTECK_INVERT	
0	RG_CSI_DPHY_L0_BYTECK_INVERT	

10217228 MIPI_RX_ANA28_CSI0B **CPHY CDR Control** **0000888F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CSI_CPHY_To_CDR_EARLY_CODE					RG_CSI_CPHY_To_CDR_INIT_CODE							RG_CSI_CPHY_To_CDR_MANUAL_EN
Type				RW					RW							RW
Reset				0	0	0	0	0	0	0	0	0	0			0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_To_CDR_CA_WIDTH				RG_CSI_CPHY_To_CDR_BC_WIDTH				RG_CSI_CPHY_To_CDR_AB_WIDTH				RG_CSI_CPHY_To_CDR_LPF_CTRL		RG_CSI_CPHY_To_CDR_AUTOLOAD_EN	RG_CSI_CPHY_To_CDR_DIRECT_EN
Type	RW				RW				RW				RW		RW	RW
Reset	1	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1

Bit(s)	Name	Description
28:24	RG_CSI_CPHY_To_CDR_EARLY_CODE	
23:19	RG_CSI_CPHY_To_CDR_INIT_CODE	
16	RG_CSI_CPHY_To_CDR_MANUAL_EN	
15:12	RG_CSI_CPHY_To_CDR_CA_WIDTH	Filter out coding jitter
11:8	RG_CSI_CPHY_To_CDR_BC_WIDTH	Filter out coding jitter
7:4	RG_CSI_CPHY_To_CDR_AB_WIDTH	Filter out coding jitter
3:2	RG_CSI_CPHY_To_CDR_LPF_CTRL	
1	RG_CSI_CPHY_To_CDR_AUTOLOAD_EN	
0	RG_CSI_CPHY_To_CDR_DIRECT_EN	Direct Sample Mode Enable

1021722C MIPI_RX_ANA2C_CSI0B **CPHY CDR Control** **00002000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI_CPHY_To_DEBUG_EN	RG_CSI_CPHY_To_BIST_EN	RG_CSI_CPHY_To_BIST_AB											
Type			RW	RW	RW											
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RG_CSI_CPHY_To_BIST_AB		RG_CSI_CPHY_To_HSDET_SEL					RG_CSI_CPHY_To_FORCE_INIT	RG_CSI_CPHY_To_SYNC_INIT_SEL	RG_CSI_CPHY_To_SYMCK_INVERT		RG_CSI_CPHY_To_CDR_LATE_CODE				
Type	RW		RW					RW	RW	RW		RW				
Reset	0	0	1	0				0	0	0		0	0	0	0	0

Bit(s)	Name	Description
29	RG_CSI_CPHY_To_DEBUG_EN	
28	RG_CSI_CPHY_To_BIST_EN	
27:14	RG_CSI_CPHY_To_BIST_AB	
13:12	RG_CSI_CPHY_To_HSDET_SEL	
8	RG_CSI_CPHY_To_FORCE_INIT	[NORMAL]1'b0: Self [NORMAL]1'b1: DA
7	RG_CSI_CPHY_To_SYNC_INIT_SEL	[NORMAL]1'b0: Self [NORMAL]1'b1: DA
6	RG_CSI_CPHY_To_SYMCK_INVERT	
4:0	RG_CSI_CPHY_To_CDR_LATE_CODE	

10217230 MIPI_RX_AN_A30_CSI0B CPHY CDR Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI_CPHY_To_BIST_CA													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_To_DEBUG_SEL		RG_CSI_CPHY_To_BIST_BC													
Type	RW		RW													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	RG_CSI_CPHY_To_BIST_CA	
15:14	RG_CSI_CPHY_To_DEBUG_SEL	
13:0	RG_CSI_CPHY_To_BIST_BC	

10217234 MIPI_RX_AN_A34_CSI0B CPHY CDR Control 0000888F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CSI_CPHY_T1_CDR_EARLY_CODE					RG_CSI_CPHY_T1_CDR_INIT_CODE							RG_CSI_CPHY_T1_CDR_MANUAL_EN
Type				RW					RW							RW
Reset				0	0	0	0	0	0	0	0	0	0			0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_T1_CDR_CA_WIDTH				RG_CSI_CPHY_T1_CDR_BC_WIDTH				RG_CSI_CPHY_T1_CDR_AB_WIDTH				RG_CSI_CPHY_T1_CDR_LPF_CTRL		RG_CSI_CPHY_T1_CDR_AUTOLOAD_EN	RG_CSI_CPHY_T1_CDR_DIRECT_EN
Type	RW				RW				RW				RW		RW	RW
Reset	1	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1

Bit(s)	Name	Description
28:24	RG_CSI_CPHY_T1_CDR_EARLY_CODE	
23:19	RG_CSI_CPHY_T1_CDR_INIT_CODE	
16	RG_CSI_CPHY_T1_CDR_MANUAL_EN	
15:12	RG_CSI_CPHY_T1_CDR_CA_WIDTH	Filter out coding jitter
11:8	RG_CSI_CPHY_T1_CDR_BC_WIDTH	Filter out coding jitter
7:4	RG_CSI_CPHY_T1_CDR_AB_WIDTH	Filter out coding jitter
3:2	RG_CSI_CPHY_T1_CDR_LPF_CTRL	
1	RG_CSI_CPHY_T1_CDR_AUTOLOAD_EN	
0	RG_CSI_CPHY_T1_CDR_DIRECT_EN	Direct Sample Mode Enable

10217238 MIPI_RX_AN A38_CSI0B CPHY CDR Control 00002000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI_CPHY_T1_DEBUG_EN	RG_CSI_CPHY_T1_BIST_EN	RG_CSI_CPHY_T1_BIST_AB											
Type			RW	RW	RW											
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_T1_BIST_AB		RG_CSI_CPHY_T1_HSDET_SEL					RG_CSI_CPHY_T1_FORCE_INIT	RG_CSI_CPHY_T1_SYNC_INIT_SEL	RG_CSI_CPHY_T1_SYMCK_INVERT		RG_CSI_CPHY_T1_CDR_LATE_CODE				
Type	RW		RW					RW	RW	RW		RW				
Reset	0	0	1	0				0	0	0		0	0	0	0	0

Bit(s)	Name	Description
29	RG_CSI_CPHY_T1_DEBUG_EN	
28	RG_CSI_CPHY_T1_BIST_EN	
27:14	RG_CSI_CPHY_T1_BIST_AB	

Bit(s)	Name	Description
13:12	RG_CSI_CPHY_T1_HSDET_SEL	
8	RG_CSI_CPHY_T1_FORCE_INIT	[NORMAL]1'b0: Self [NORMAL]1'b1: DA
7	RG_CSI_CPHY_T1_SYNC_INIT_SEL	[NORMAL]1'b0: Self [NORMAL]1'b1: DA
6	RG_CSI_CPHY_T1_SYMCK_INVERT	
4:0	RG_CSI_CPHY_T1_CDR_LATE_CODE	

1021723C MIPI_RX_ANA3C_CSI0B **CPHY CDR Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI_CPHY_T1_BIST_CA													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_T1_DEBUG_SEL		RG_CSI_CPHY_T1_BIST_BC													
Type	RW		RW													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	RG_CSI_CPHY_T1_BIST_CA	
15:14	RG_CSI_CPHY_T1_DEBUG_SEL	
13:0	RG_CSI_CPHY_T1_BIST_BC	

10217240 MIPI_RX_ANA40_CSI0B **GPI Control** **40404040**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_CSI_L1N_GPI_G	RG_CSI_L1N_GPI_RDSEL		RG_CSI_L1N_GPI_PD	RG_CSI_L1N_GPI_PU	RG_CSI_L1N_GPI_SMT	RG_CSI_L1N_GPI_IES		RG_CSI_L1P_GPI_G	RG_CSI_L1P_GPI_RDSEL		RG_CSI_L1P_GPI_PD	RG_CSI_L1P_GPI_PU	RG_CSI_L1P_GPI_SMT	RG_CSI_L1P_GPI_IES
Type		RW	RW		RW	RW	RW	RW		RW	RW		RW	RW	RW	RW
Reset		1	0	0	0	0	0	0		1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI_LoN_GPI_G	RG_CSI_LoN_GPI_RDSEL		RG_CSI_LoN_GPI_PD	RG_CSI_LoN_GPI_PU	RG_CSI_LoN_GPI_SMT	RG_CSI_LoN_GPI_IES		RG_CSI_LoP_GPI_G	RG_CSI_LoP_GPI_RDSEL		RG_CSI_LoP_GPI_PD	RG_CSI_LoP_GPI_PU	RG_CSI_LoP_GPI_SMT	RG_CSI_LoP_GPI_IES
Type		RW	RW		RW	RW	RW	RW		RW	RW		RW	RW	RW	RW
Reset		1	0	0	0	0	0	0		1	0	0	0	0	0	0

Bit(s)	Name	Description
30	RG_CSI_L1N_GPI_G	**RX Input Control Gating**
29:28	RG_CSI_L1N_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment)

Bit(s)	Name	Description
		RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
27	RG_CSI_L1N_GPI_PD	**75K pull-down resistor control. High activiate.**
26	RG_CSI_L1N_GPI_PU	**75K pull-up resistor control. High activiate.**
25	RG_CSI_L1N_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
24	RG_CSI_L1N_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.
22	RG_CSI_L1P_GPI_G	**RX Input Control Gating**
21:20	RG_CSI_L1P_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
19	RG_CSI_L1P_GPI_PD	**75K pull-down resistor control. High activiate.**
18	RG_CSI_L1P_GPI_PU	**75K pull-up resistor control. High activiate.**
17	RG_CSI_L1P_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
16	RG_CSI_L1P_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.
14	RG_CSI_L0N_GPI_G	**RX Input Control Gating**
13:12	RG_CSI_L0N_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
11	RG_CSI_L0N_GPI_PD	**75K pull-down resistor control. High activiate.**
10	RG_CSI_L0N_GPI_PU	**75K pull-up resistor control. High activiate.**
9	RG_CSI_L0N_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
8	RG_CSI_L0N_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.
6	RG_CSI_L0P_GPI_G	**RX Input Control Gating**
5:4	RG_CSI_L0P_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting:

Bit(s)	Name	Description
		1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
3	RG_CSI_L0P_GPI_PD	**75K pull-down resistor control. High activiate.**
2	RG_CSI_L0P_GPI_PU	**75K pull-up resistor control. High activiate.**
1	RG_CSI_L0P_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
0	RG_CSI_L0P_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.

10217244 MIPI_RX_ANA44_CSI0B GPI Control 00004040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI_L2N_GPI_G	RG_CSI_L2N_GPI_RDSEL		RG_CSI_L2N_GPI_PD	RG_CSI_L2N_GPI_PU	RG_CSI_L2N_GPI_SMT	RG_CSI_L2N_GPI_IES		RG_CSI_L2P_GPI_G	RG_CSI_L2P_GPI_RDSEL		RG_CSI_L2P_GPI_PD	RG_CSI_L2P_GPI_PU	RG_CSI_L2P_GPI_SMT	RG_CSI_L2P_GPI_IES
Type		RW	RW		RW	RW	RW	RW		RW	RW		RW	RW	RW	RW
Reset		1	0	0	0	0	0	0		1	0	0	0	0	0	0

Bit(s)	Name	Description
14	RG_CSI_L2N_GPI_G	**RX Input Control Gating**
13:12	RG_CSI_L2N_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
11	RG_CSI_L2N_GPI_PD	**75K pull-down resistor control. High activiate.**
10	RG_CSI_L2N_GPI_PU	**75K pull-up resistor control. High activiate.**
9	RG_CSI_L2N_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
8	RG_CSI_L2N_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.
6	RG_CSI_L2P_GPI_G	**RX Input Control Gating**
5:4	RG_CSI_L2P_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00]

Bit(s)	Name	Description
		1.2V: RDSEL[1:0]=[11]
3	RG_CSI_L2P_GPI_PD	**75K pull-down resistor control. High activiate.**
2	RG_CSI_L2P_GPI_PU	**75K pull-up resistor control. High activiate.**
1	RG_CSI_L2P_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
0	RG_CSI_L2P_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.

10217248 MIPI_RX_ANA48_CSI0B RGS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AD_CSI_CPHY_T1_DEBUG_OUT	AD_CSI_CPHY_T1_BIST_CHECK_OUT	AD_CSI_CPHY_T0_DEBUG_OUT	AD_CSI_CPHY_T0_BIST_CHECK_OUT	AD_CSI_L2N_GPI_OUT	AD_CSI_L2P_GPI_OUT	AD_CSI_L1N_GPI_OUT	AD_CSI_L1P_GPI_OUT	AD_CSI_L0N_GPI_OUT	AD_CSI_L0P_GPI_OUT
Type							RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RGS_CSI_CPHY_T1_CDR_CODE								RGS_CSI_CPHY_T0_CDR_CODE				
Type				RU								RU				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
25	AD_CSI_CPHY_T1_DEBUG_OUT	
24	AD_CSI_CPHY_T1_BIST_CHECK_OUT	
23	AD_CSI_CPHY_T0_DEBUG_OUT	
22	AD_CSI_CPHY_T0_BIST_CHECK_OUT	
21	AD_CSI_L2N_GPI_OUT	
20	AD_CSI_L2P_GPI_OUT	
19	AD_CSI_L1N_GPI_OUT	
18	AD_CSI_L1P_GPI_OUT	
17	AD_CSI_L0N_GPI_OUT	
16	AD_CSI_L0P_GPI_OUT	
12:8	RGS_CSI_CPHY_T1_CDR_CODE	
4:0	RGS_CSI_CPHY_T0_CDR_CODE	

1021724C MIPI_RX_ANA4C_CSI0B DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DA_CSI_CDPHY_L2N_T1C_HSR	DA_CSI_CDPHY_L2P_T1B_HSR	DA_CSI_CDPHY_L1N_T1A_HSR	DA_CSI_CDPHY_L1P_T0C_HSR	DA_CSI_CDPHY_L0N_T0B_HSR	DA_CSI_CDPHY_L0P_T0A_HSR	AD_CSI_DPHY_L2N_HSDET_OUT	DA_CSI_DPHY_L2N_HSDET_RS	AD_CSI_DPHY_L2P_HSDET_OUT	DA_CSI_DPHY_L2P_HSDET_RS	AD_CSI_DPHY_L1N_HSDET_OUT	DA_CSI_DPHY_L1N_HSDET_RS	AD_CSI_DPHY_L1P_HSDET_OUT	DA_CSI_DPHY_L1P_HSDET_RS

			T_EN	T_EN	T_EN	T_EN	T_EN	T_EN	T	TB	T	TB	T	TB	T	TB
Type			RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AD_CSI_DPHY_LoN_HSDET_OUT	DA_CSI_DPHY_LoN_HSDET_RSTB	AD_CSI_DPHY_LoP_HSDET_OUT	DA_CSI_DPHY_LoP_HSDET_RSTB	AD_CSI_CDPHY_L2N_T1C_LPRX_OUT	DA_CSI_CDPHY_L2N_T1C_LPRX_EN	AD_CSI_CDPHY_L2P_T1B_LPRX_OUT	DA_CSI_CDPHY_L2P_T1B_LPRX_EN	AD_CSI_CDPHY_L1N_T1A_LPRX_OUT	DA_CSI_CDPHY_L1N_T1A_LPRX_EN	AD_CSI_CDPHY_L1P_ToC_LPRX_OUT	DA_CSI_CDPHY_L1P_ToC_LPRX_EN	AD_CSI_CDPHY_LoN_ToB_LPRX_OUT	DA_CSI_CDPHY_LoN_ToB_LPRX_EN	AD_CSI_CDPHY_LoP_ToA_LPRX_OUT	DA_CSI_CDPHY_LoP_ToA_LPRX_EN
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29	DA_CSI_CDPHY_L2N_T1C_HSRT_EN	
28	DA_CSI_CDPHY_L2P_T1B_HSRT_EN	
27	DA_CSI_CDPHY_L1N_T1A_HSRT_EN	
26	DA_CSI_CDPHY_L1P_ToC_HSRT_EN	
25	DA_CSI_CDPHY_LoN_ToB_HSRT_EN	
24	DA_CSI_CDPHY_LoP_ToA_HSRT_EN	
23	AD_CSI_DPHY_L2N_HSDET_OUT	
22	DA_CSI_DPHY_L2N_HSDET_RSTB	
21	AD_CSI_DPHY_L2P_HSDET_OUT	
20	DA_CSI_DPHY_L2P_HSDET_RSTB	
19	AD_CSI_DPHY_L1N_HSDET_OUT	
18	DA_CSI_DPHY_L1N_HSDET_RSTB	
17	AD_CSI_DPHY_L1P_HSDET_OUT	
16	DA_CSI_DPHY_L1P_HSDET_RSTB	
15	AD_CSI_DPHY_LoN_HSDET_OUT	
14	DA_CSI_DPHY_LoN_HSDET_RSTB	
13	AD_CSI_DPHY_LoP_HSDET_OUT	
12	DA_CSI_DPHY_LoP_HSDET_RSTB	
11	AD_CSI_CDPHY_L2N_T1C_LPRX_OUT	
10	DA_CSI_CDPHY_L2N_T1C_LPRX_EN	
9	AD_CSI_CDPHY_L2P_T1B_LPRX_OUT	
8	DA_CSI_CDPHY_L2P_T1B_LPRX_EN	
7	AD_CSI_CDPHY_L1N_T1A_LPRX_OUT	
6	DA_CSI_CDPHY_L1N_T1A_LPRX_EN	
5	AD_CSI_CDPHY_L1P_ToC_LPRX_OUT	
4	DA_CSI_CDPHY_L1P_ToC_LPRX_EN	

Bit(s)	Name	Description
3	AD_CSI_CDPHY_LoN_ToB_LPRX_OUT	
2	DA_CSI_CDPHY_LoN_ToB_LPRX_EN	
1	AD_CSI_CDPHY_LoP_ToA_LPRX_OUT	
0	DA_CSI_CDPHY_LoP_ToA_LPRX_EN	

10217250 MIPI_RX_AN_A50_CSI0B **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AD_CSI_CPHY_ToCA_HSAMP_OS_CK	AD_CSI_CPHY_ToCA_HSAMP_OS_OUT	DA_CSI_CPHY_ToCA_HSAMP_OS_CODE					DA_CSI_CPHY_ToCA_HSAMP_OS_CAL_EN	DA_CSI_CPHY_ToCA_HSAMP_OS_APPLY	DA_CSI_CPHY_ToCA_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							AD_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CK	AD_CSI_CDPHY_Lo_ToAB_HSAMP_OS_OUT	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CODE					DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CAL_EN	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_APPLY	DA_CSI_CDPHY_Lo_ToAB_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25	AD_CSI_CPHY_ToCA_HSAMP_OS_CK	
24	AD_CSI_CPHY_ToCA_HSAMP_OS_OUT	
23:19	DA_CSI_CPHY_ToCA_HSAMP_OS_CODE	
18	DA_CSI_CPHY_ToCA_HSAMP_OS_CAL_EN	
17	DA_CSI_CPHY_ToCA_HSAMP_OS_APPLY	
16	DA_CSI_CPHY_ToCA_HSAMP_EN	
9	AD_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CK	
8	AD_CSI_CDPHY_Lo_ToAB_HSAMP_OS_OUT	
7:3	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CODE	
2	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CAL_EN	
1	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_APPLY	
0	DA_CSI_CDPHY_Lo_ToAB_HSAM	

Bit(s)	Name	Description
	P_EN	

10217254 MIPI_RX_ANA54_CSI0B **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AD_CSI_CDPHY_L1_T1AB_HSAMP_OS_CK	AD_CSI_CDPHY_L1_T1AB_HSAMP_OS_OUT	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_CODE					DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_CAL_EN	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_APPLY	DA_CSI_CDPHY_L1_T1AB_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							AD_CSI_CPHY_ToBC_HSAMP_OS_CK	AD_CSI_CPHY_ToBC_HSAMP_OS_OUT	DA_CSI_CPHY_ToBC_HSAMP_OS_CODE					DA_CSI_CPHY_ToBC_HSAMP_OS_CAL_EN	DA_CSI_CPHY_ToBC_HSAMP_OS_APPLY	DA_CSI_CPHY_ToBC_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25	AD_CSI_CDPHY_L1_T1AB_HSAMP_OS_CK	
24	AD_CSI_CDPHY_L1_T1AB_HSAMP_OS_OUT	
23:19	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_CODE	
18	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_CAL_EN	
17	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_APPLY	
16	DA_CSI_CDPHY_L1_T1AB_HSAMP_EN	
9	AD_CSI_CPHY_ToBC_HSAMP_OS_CK	
8	AD_CSI_CPHY_ToBC_HSAMP_OS_OUT	
7:3	DA_CSI_CPHY_ToBC_HSAMP_OS_CODE	
2	DA_CSI_CPHY_ToBC_HSAMP_OS_CAL_EN	
1	DA_CSI_CPHY_ToBC_HSAMP_OS_APPLY	
0	DA_CSI_CPHY_ToBC_HSAMP_EN	

10217258 MIPI_RX_ANA58_CSI0B **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AD_CSI_CDPHY_L2_T1BC_HSAMP_OS_CK	AD_CSI_CDPHY_L2_T1BC_HSAMP_OS_OUT	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_CODE					DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_CAL_EN	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_APPLY	DA_CSI_CDPHY_L2_T1BC_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							AD_CSI_CPHY_T1CA_HSAMP_OS_CK	AD_CSI_CPHY_T1CA_HSAMP_OS_OUT	DA_CSI_CPHY_T1CA_HSAMP_OS_CODE					DA_CSI_CPHY_T1CA_HSAMP_OS_CAL_EN	DA_CSI_CPHY_T1CA_HSAMP_OS_APPLY	DA_CSI_CPHY_T1CA_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25	AD_CSI_CDPHY_L2_T1BC_HSAMP_OS_CK	
24	AD_CSI_CDPHY_L2_T1BC_HSAMP_OS_OUT	
23:19	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_CODE	
18	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_CAL_EN	
17	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_APPLY	
16	DA_CSI_CDPHY_L2_T1BC_HSAMP_EN	
9	AD_CSI_CPHY_T1CA_HSAMP_OS_CK	
8	AD_CSI_CPHY_T1CA_HSAMP_OS_OUT	
7:3	DA_CSI_CPHY_T1CA_HSAMP_OS_CODE	
2	DA_CSI_CPHY_T1CA_HSAMP_OS_CAL_EN	
1	DA_CSI_CPHY_T1CA_HSAMP_OS_APPLY	
0	DA_CSI_CPHY_T1CA_HSAMP_EN	

1021725C MIPI_RX_AN_A5C_CSI0B **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSI_DPHY_Lo_DELAY_CODE							AD_CSI_DPHY_Lo_BYPASS_BYTE_DATA							
Type		RU							RU							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_D	DA_CSI_D	AD_CSI_D	AD_CSI_D	AD_CSI_DPHY_Lo_BYTE_DATA								AD_CSI_D	DA_CSI_D	DA_CSI_D	DA_CSI_D

	PHY_Lo_DELAY_APPLY	PHY_Lo_DELAY_EN	PHY_Lo_BYPASS_BYTE_CK	PHY_Lo_SYNC_DETECT									PHY_Lo_BYTE_CK	PHY_Lo_DES_SYNC_INIT	PHY_Lo_DES_EN	PHY_Lo_SAMP_EN
Type	RU	RU	RU	RU	RU								RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	DA_CSI_DPHY_Lo_DELAY_CODE	
23:16	AD_CSI_DPHY_Lo_BYPASS_BYTE_DATA	
15	DA_CSI_DPHY_Lo_DELAY_APPLY	
14	DA_CSI_DPHY_Lo_DELAY_EN	
13	AD_CSI_DPHY_Lo_BYPASS_BYTE_CK	
12	AD_CSI_DPHY_Lo_SYNC_DETECT	
11:4	AD_CSI_DPHY_Lo_BYTE_DATA	
3	AD_CSI_DPHY_Lo_BYTE_CK	
2	DA_CSI_DPHY_Lo_DES_SYNC_INIT	
1	DA_CSI_DPHY_Lo_DES_EN	
0	DA_CSI_DPHY_Lo_SAMP_EN	

10217260 MIPI_RX_AN_A60_CSIoB **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSI_DPHY_L1_DELAY_CODE							AD_CSI_DPHY_L1_BYPASS_BYTE_DATA							
Type		RU							RU							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_DPHY_L1_DELAY_APPLY	DA_CSI_DPHY_L1_DELAY_EN	AD_CSI_DPHY_L1_BYPASS_BYTE_CK	AD_CSI_DPHY_L1_SYNC_DETECT	AD_CSI_DPHY_L1_BYTE_DATA								AD_CSI_DPHY_L1_BYTE_CK	DA_CSI_DPHY_L1_DES_SYNC_INIT	DA_CSI_DPHY_L1_DES_EN	DA_CSI_DPHY_L1_SAMP_EN
Type	RU	RU	RU	RU	RU								RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	DA_CSI_DPHY_L1_DELAY_CODE	
23:16	AD_CSI_DPHY_L1_BYPASS_BYTE_DATA	
15	DA_CSI_DPHY_L1_DELAY_APPLY	
14	DA_CSI_DPHY_L1_DELAY_EN	
13	AD_CSI_DPHY_L1_BYPASS_BYTE_CK	
12	AD_CSI_DPHY_L1_SYNC_DETECT	
11:4	AD_CSI_DPHY_L1_BYTE_DATA	

Bit(s)	Name	Description
3	AD_CSI_DPHY_L1_BYTE_CK	
2	DA_CSI_DPHY_L1_DES_SYNC_INIT	
1	DA_CSI_DPHY_L1_DES_EN	
0	DA_CSI_DPHY_L1_SAMP_EN	

10217264 MIPI_RX_AN A64_CSI0B DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSI_DPHY_L2_DELAY_CODE							AD_CSI_DPHY_L2_BYPASS_BYTE_DATA							
Type		RU							RU							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_DPHY_L2_DELAY_APPLY	DA_CSI_DPHY_L2_DELAY_EN	AD_CSI_DPHY_L2_BYPASS_BYTE_CK	AD_CSI_DPHY_L2_SYNC_DETECT	AD_CSI_DPHY_L2_BYTE_DATA								AD_CSI_DPHY_L2_BYTE_CK	DA_CSI_DPHY_L2_DES_SYNC_INIT	DA_CSI_DPHY_L2_DES_EN	DA_CSI_DPHY_L2_SAMP_EN
Type	RU	RU	RU	RU	RU								RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	DA_CSI_DPHY_L2_DELAY_CODE	
23:16	AD_CSI_DPHY_L2_BYPASS_BYTE_DATA	
15	DA_CSI_DPHY_L2_DELAY_APPLY	
14	DA_CSI_DPHY_L2_DELAY_EN	
13	AD_CSI_DPHY_L2_BYPASS_BYTE_CK	
12	AD_CSI_DPHY_L2_SYNC_DETECT	
11:4	AD_CSI_DPHY_L2_BYTE_DATA	
3	AD_CSI_DPHY_L2_BYTE_CK	
2	DA_CSI_DPHY_L2_DES_SYNC_INIT	
1	DA_CSI_DPHY_L2_DES_EN	
0	DA_CSI_DPHY_L2_SAMP_EN	

10217268 MIPI_RX_AN A68_CSI0B DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AD_CSI_CPHY_To_HSDET_OUT	DA_CSI_CPHY_To_SYNC_INIT
Type															RU	RU
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	DA_CSI_CPHY_To_DES_EN	DA_CSI_CPHY_To_CDR_EN	AD_CSI_CPHY_To_AB													
Type	RU	RU	RU													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	AD_CSI_CPHY_To_HSDET_OUT	
16	DA_CSI_CPHY_To_SYNC_INIT	
15	DA_CSI_CPHY_To_DES_EN	
14	DA_CSI_CPHY_To_CDR_EN	
13:0	AD_CSI_CPHY_To_AB	

1021726C MIPI_RX_ANA6C_CSI0B DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AD_CSI_CPHY_To_BC													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	AD_CSI_CPHY_To_BC	

10217270 MIPI_RX_ANA70_CSI0B DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AD_CSI_CPHY_To_CA													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	AD_CSI_CPHY_To_CA	

10217274 MIPI_RX_ANA74_CSI0B DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AD_C	DA_C

															SI_CPHY_T1_HSDET_OUT	SI_CPHY_T1_SYNC_INIT
Type															RU	RU
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_CPHY_T1_DES_EN	DA_CSI_CPHY_T1_CDR_EN	AD_CSI_CPHY_T1_AB													
Type	RU	RU	RU													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	AD_CSI_CPHY_T1_HSDET_OUT	
16	DA_CSI_CPHY_T1_SYNC_INIT	
15	DA_CSI_CPHY_T1_DES_EN	
14	DA_CSI_CPHY_T1_CDR_EN	
13:0	AD_CSI_CPHY_T1_AB	

10217278 MIPI_RX_ANA78_CSI0B **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AD_CSI_CPHY_T1_BC													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	AD_CSI_CPHY_T1_BC	

1021727C MIPI_RX_ANA7C_CSI0B **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AD_CSI_CPHY_T1_CA													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	AD_CSI_CPHY_T1_CA	

Bit(s)	Name	Description

10217280 MIPI_RX_WRAPPER80_CSIoB WRAPPER 04000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CSR_CSIo_DPHY_MUX			CSR_SW_RST				CSR_CSI1_CPHY_RST_MODE		CSR_CSI1_DPHY_RST_MODE		CSR_CSIo_CPHY_RST_MODE		CSR_CSIo_DPHY_RST_MODE	
Type		RW			RW				RW		RW		RW		RW	
Reset		0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_CSI_MON_MUX								CSR_CSI_MODE				CSR_CSI1_DPHY_MUX		CSR_HSDET_MODE	CSR_CSI_CLK_MON
Type	RW								RW				RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:28	CSR_CSIo_DPHY_MUX	
27:24	CSR_SW_RST	
23:22	CSR_CSI1_CPHY_RST_MODE	0: sync init 1: hsrx_en 2: sw rst 3: hw rst
21:20	CSR_CSI1_DPHY_RST_MODE	0: sync init 1: hsrx_en 2: sw rst 3: hw rst
19:18	CSR_CSIo_CPHY_RST_MODE	0: sync init 1: hsrx_en 2: sw rst 3: hw rst
17:16	CSR_CSIo_DPHY_RST_MODE	0: sync init 1: hsrx_en 2: sw rst 3: hw rst
15:8	CSR_CSI_MON_MUX	
7:4	CSR_CSI_MODE	0:4 lane 1:2/2l lane 2:cphy 4:cphy/2 lane
3:2	CSR_CSI1_DPHY_MUX	
1	CSR_HSDET_MODE	0:dn 1:dp
0	CSR_CSI_CLK_MON	Enable Clock monitor

10217284 MIPI_RX_WRAPPER84_CSIoB WRAPPER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI_DEBUG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI_DEBUG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSI_DEBUG_OUT	

10217288 MIPI_RX_WRAPPER88_CSIoB WRAPPER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_MODE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_MODE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_MODE_0	

1021728C MIPI_RX_WRAPPER8C_CSIoB WRAPPER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_MODE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_MODE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_MODE_1	

10217290 MIPI_RX_WRAPPER90_CSIoB WRAPPER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_MODE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_MODE_2															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_MODE_2	

10217294 MIPI_RX_WRAPPER94_CSIoB WRAPPER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_VALUE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_VALUE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_VALUE_0	

10217298 MIPI_RX_WRAPPER98_CSIoB WRAPPER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_VALUE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_VALUE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_VALUE_1	

1021729C MIPI_RX_WRAPPER9C_CSIoB WRAPPER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_VALUE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_VALUE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_VALUE_2	

10217400 MIPI_RX_AN A00_CSI1A 2D1C Global Control 00000492

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_CSI_DPHY_L2_CKSEL	RG_CSI_DPHY_L2_CKMODE_EN	RG_CSI_DPHY_L2_BYPASS_SYNC	RG_CSI_DPHY_L1_CKSEL	RG_CSI_DPHY_L1_CKMODE_EN	RG_CSI_DPHY_L1_BYPASS_SYNC	RG_CSI_DPHY_Lo_CKSEL	RG_CSI_DPHY_Lo_CKMODE_EN	RG_CSI_DPHY_Lo_BYPASS_SYNC	RG_CSI_BG_CORE_EN	RG_CSI_BG_LPF_EN	RG_CSI_HSAMP_PROTECT_EN	RG_CSI_CPHY_EN
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	1	0	0	1	0	0	1	0	0	1	0

Bit(s)	Name	Description
12	RG_CSI_DPHY_L2_CKSEL	**Data Mode** [NORMAL]1'b0: Sample data by Local Clock [NORMAL]1'b1: Sample data by Common Clock CK Mode [NORMAL]1'b0: Connect to Local Clock [NORMAL]1'b1: Connect to Common Clock
11	RG_CSI_DPHY_L2_CKMODE_EN	**[NORMAL]1'b0: Data Mode** [NORMAL]1'b1: CK Mode
10	RG_CSI_DPHY_L2_BYPASS_SYNC	**Bypass or Sync Mode Selection** [NORMAL]1'b0: Sync Mode [NORMAL]1'b1: Bypass Mode
9	RG_CSI_DPHY_L1_CKSEL	**Data Mode** [NORMAL]1'b0: Sample data by Local Clock [NORMAL]1'b1: Sample data by Common Clock CK Mode [NORMAL]1'b0: Connect to Local Clock [NORMAL]1'b1: Connect to Common Clock
8	RG_CSI_DPHY_L1_CKMODE_EN	**[NORMAL]1'b0: Data Mode** [NORMAL]1'b1: CK Mode
7	RG_CSI_DPHY_L1_BYPASS_SYNC	**Bypass or Sync Mode Selection** [NORMAL]1'b0: Sync Mode [NORMAL]1'b1: Bypass Mode
6	RG_CSI_DPHY_Lo_CKSEL	**Data Mode** [NORMAL]1'b0: Sample data by Local Clock [NORMAL]1'b1: Sample data by Common Clock CK Mode [NORMAL]1'b0: Connect to Local Clock [NORMAL]1'b1: Connect to Common Clock
5	RG_CSI_DPHY_Lo_CKMODE_EN	**[NORMAL]1'b0: Data Mode** [NORMAL]1'b1: CK Mode
4	RG_CSI_DPHY_Lo_BYPASS_SYNC	**Bypass or Sync Mode Selection** [NORMAL]1'b0: Sync Mode [NORMAL]1'b1: Bypass Mode
3	RG_CSI_BG_CORE_EN	**[NORMAL]1'b0: Bandgap Disable** [NORMAL]1'b1: Bandgap Enable

Bit(s)	Name	Description
2	RG_CSI_BG_LPF_EN	**[NORMAL]1'b0: Bandgap low pass filter Disable** [NORMAL]1'b1: Bandgap low pass filter Enable
1	RG_CSI_HSAMP_PROTECT_EN	**HSAMP Protection** [NORMAL]1'b0: Disable [NORMAL]1'b1: Enable
0	RG_CSI_CPHY_EN	**1'b0: DPHY Mode** 1'b1: CPHY Mode

10217404 MIPI_RX_AN A04_CSI1A 2D1C Global Control 00084444

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CSI_FORCE_HSRT_EN	RG_CSI_BG_MON_VREF_SEL								RG_CSI_BG_VREF_SEL			
Type				RW	RW								RW			
Reset				0	0	0	0	0					1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI_BG_HSDET_VTL_SEL				RG_CSI_BG_HSDET_VTH_SEL				RG_CSI_BG_LPRX_VTL_SEL				RG_CSI_BG_LPRX_VTH_SEL		
Type		RW				RW				RW				RW		
Reset		1	0	0		1	0	0		1	0	0		1	0	0

Bit(s)	Name	Description
28	RG_CSI_FORCE_HSRT_EN	**Force HSRT Enable to do FT calibration and eFuse**
27:24	RG_CSI_BG_MON_VREF_SEL	**Monitor Selection**
19:16	RG_CSI_BG_VREF_SEL	**HSAMP LDO Reference Voltage** Default 0.9V
14:12	RG_CSI_BG_HSDET_VTL_SEL	**HSDET VTH Selection** Default 0.12V
10:8	RG_CSI_BG_HSDET_VTH_SEL	**HSDET VTH Selection** Default 0.15V
6:4	RG_CSI_BG_LPRX_VTL_SEL	**LPRX VTL Selection** Default 0.70V
2:0	RG_CSI_BG_LPRX_VTH_SEL	**LPRX VTH Selection** Default 0.75V

10217408 MIPI_RX_AN A08_CSI1A High Speed Termination Control 10101010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CSI_L1N_T1A_HSRT_CODE								RG_CSI_L1P_ToC_HSRT_CODE				
Type				RW								RW				
Reset				1	0	0	0	0				1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_CSI_LoN_ToB_HSRT_CODE								RG_CSI_LoP_ToA_HSRT_CODE				
Type				RW								RW				
Reset				1	0	0	0	0				1	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
28:24	RG_CSI_L1N_T1A_HSRT_CODE	**Termination code** 8000hm/(8+N) Requires Calibration & Efuse on FT
20:16	RG_CSI_L1P_T0C_HSRT_CODE	**Termination code** 8000hm/(8+N) Requires Calibration & Efuse on FT
12:8	RG_CSI_L0N_T0B_HSRT_CODE	**Termination code** 8000hm/(8+N) Requires Calibration & Efuse on FT
4:0	RG_CSI_L0P_T0A_HSRT_CODE	**Termination code** 8000hm/(8+N) Requires Calibration & Efuse on FT

1021740C MIPI_RX_AN_A0C_CSI1A **High Speed Termination Control** **00001010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_CSI_L2N_T1C_HSRT_CODE								RG_CSI_L2P_T1B_HSRT_CODE				
Type				RW								RW				
Reset				1	0	0	0	0				1	0	0	0	0

Bit(s)	Name	Description
12:8	RG_CSI_L2N_T1C_HSRT_CODE	**Termination code** 8000hm/(8+N) Requires Calibration & Efuse on FT
4:0	RG_CSI_L2P_T1B_HSRT_CODE	**Termination code** 8000hm/(8+N) Requires Calibration & Efuse on FT

10217410 MIPI_RX_AN_A10_CSI1A **Bandgap Voltage for Delay Line Calibration** **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_CPHY_T0_VREF_SEL						RG_CSI_CPHY_T0_CDR_DELAY_CAL_RSTB	RG_CSI_CPHY_T0_CDR_DELAY_CAL_EN	RG_CSI_DPHY_L2_VREF_SEL						RG_CSI_DPHY_L2_DELAY_CAL_RSTB	RG_CSI_DPHY_L2_DELAY_CAL_EN
Type	RW						RW	RW	RW						RW	RW
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_DPHY_L1_VREF_SEL						RG_CSI_DPHY_L1_DELAY_CAL_RSTB	RG_CSI_DPHY_L1_DELAY_CAL_EN	RG_CSI_DPHY_L0_VREF_SEL						RG_CSI_DPHY_L0_DELAY_CAL_RSTB	RG_CSI_DPHY_L0_DELAY_CAL_EN

Type	RW						RW	RW	RW						RW	RW
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:26	RG_CSI_CPHY_T0_VREF_SEL	**D0 Delay Line Reference Voltage** Requires Software Calibration
25	RG_CSI_CPHY_T0_CDR_DELAYCAL_RSTB	**TRIO0 Delay Line Calibration Reset Bar**
24	RG_CSI_CPHY_T0_CDR_DELAYCAL_EN	**TRIO0 Delay Line Calibration Enable**
23:18	RG_CSI_DPHY_L2_VREF_SEL	**D0 Delay Line Reference Voltage** Requires Software Calibration
17	RG_CSI_DPHY_L2_DELAYCAL_RSTB	**D1 Delay Line Calibration Reset Bar**
16	RG_CSI_DPHY_L2_DELAYCAL_EN	**D1 Delay Line Calibration Enable**
15:10	RG_CSI_DPHY_L1_VREF_SEL	**D0 Delay Line Reference Voltage** Requires Software Calibration
9	RG_CSI_DPHY_L1_DELAYCAL_RSTB	**CK Delay Line Calibration Reset Bar**
8	RG_CSI_DPHY_L1_DELAYCAL_EN	**CK Delay Line Calibration Enable**
7:2	RG_CSI_DPHY_L0_VREF_SEL	**D0 Delay Line Reference Voltage** Requires Software Calibration
1	RG_CSI_DPHY_L0_DELAYCAL_RSTB	**D0 Delay Line Calibration Reset Bar**
0	RG_CSI_DPHY_L0_DELAYCAL_EN	**D0 Delay Line Calibration Enable**

10217414 MIPI_RX_ANA14_CSI1A **Bandgap Voltage for Delay Line Calibration** **00000080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**RG_CSI_CPHY_T1_VREF_SEL**						**RG_CSI_CPHY_T1_CDR_DELAYCAL_RSTB**	**RG_CSI_CPHY_T1_CDR_DELAYCAL_EN**
Type									RW						RW	RW
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSI_CPHY_T1_VREF_SEL	**D0 Delay Line Reference Voltage** Requires Software Calibration
1	RG_CSI_CPHY_T1_CDR_DELAYCAL_RSTB	**TRIO1 Delay Line Calibration Reset Bar**
0	RG_CSI_CPHY_T1_CDR_DELAYCAL_EN	**TRIO1 Delay Line Calibration Enable**

10217418 MIPI_RX_ANA18_CSI1A HS AMP Control 88008800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_XX_ToCA_HSAMP_SRB				RG_CSI_XX_ToCA_HSAMP_SRA				RG_CSI_XX_ToCA_HSAMP_BW		RG_CSI_XX_ToCA_HSAMP_IS		RG_CSI_XX_ToCA_HSAMP_SCB	RG_CSI_XX_ToCA_HSAMP_SCA	RG_CSI_XX_ToCA_HSAMP_LPBK_TEST_EN	RG_CSI_XX_ToCA_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_Lo_ToAB_HSAMP_SRB				RG_CSI_Lo_ToAB_HSAMP_SRA				RG_CSI_Lo_ToAB_HSAMP_BW		RG_CSI_Lo_ToAB_HSA MP_IS		RG_CSI_Lo_ToAB_HSAMP_SCB	RG_CSI_Lo_ToAB_HSAMP_SCA	RG_CSI_Lo_ToAB_HSAMP_LPBK_TEST_EN	RG_CSI_Lo_ToAB_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	RG_CSI_XX_ToCA_HSAMP_SRB	
27:24	RG_CSI_XX_ToCA_HSAMP_SRA	
23:22	RG_CSI_XX_ToCA_HSAMP_BW	
21:20	RG_CSI_XX_ToCA_HSAMP_IS	
19	RG_CSI_XX_ToCA_HSAMP_SCB	
18	RG_CSI_XX_ToCA_HSAMP_SCA	
17	RG_CSI_XX_ToCA_HSAMP_LPBK_TEST_EN	
16	RG_CSI_XX_ToCA_HSAMP_MON_EN	
15:12	RG_CSI_Lo_ToAB_HSAMP_SRB	
11:8	RG_CSI_Lo_ToAB_HSAMP_SRA	
7:6	RG_CSI_Lo_ToAB_HSAMP_BW	
5:4	RG_CSI_Lo_ToAB_HSAMP_IS	
3	RG_CSI_Lo_ToAB_HSAMP_SCB	
2	RG_CSI_Lo_ToAB_HSAMP_SCA	
1	RG_CSI_Lo_ToAB_HSAMP_LPBK_TEST_EN	
0	RG_CSI_Lo_ToAB_HSAMP_MON_EN	

1021741C MIPI_RX_ANA1C_CSI1A HS AMP Control 88008800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_L1_T1AB_HSAMP_SRB				RG_CSI_L1_T1AB_HSAMP_SRA				RG_CSI_L1_T1AB_HSAMP_BW		RG_CSI_L1_T1AB_HSAMP_IS		RG_CSI_L1_T1AB_HSAMP_SCB	RG_CSI_L1_T1AB_HSAMP_SCA	RG_CSI_L1_T1AB_HSAMP_LPBK_TEST_E	RG_CSI_L1_T1AB_HSAMP_MON_EN

															N	
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_XX_ToBC_HSAMP_SRB				RG_CSI_XX_ToBC_HSAMP_SRA				RG_CSI_XX_ToBC_HSAMP_BW		RG_CSI_XX_ToBC_HSAMP_IS		RG_CSI_XX_ToBC_HSAMP_SCB	RG_CSI_XX_ToBC_HSAMP_SCA	RG_CSI_XX_ToBC_HSAMP_LPBK_TEST_EN	RG_CSI_XX_ToBC_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	RG_CSI_L1_T1AB_HSAMP_SRB	
27:24	RG_CSI_L1_T1AB_HSAMP_SRA	
23:22	RG_CSI_L1_T1AB_HSAMP_BW	
21:20	RG_CSI_L1_T1AB_HSAMP_IS	
19	RG_CSI_L1_T1AB_HSAMP_SCB	
18	RG_CSI_L1_T1AB_HSAMP_SCA	
17	RG_CSI_L1_T1AB_HSAMP_LPBK_TEST_EN	
16	RG_CSI_L1_T1AB_HSAMP_MON_EN	
15:12	RG_CSI_XX_ToBC_HSAMP_SRB	
11:8	RG_CSI_XX_ToBC_HSAMP_SRA	
7:6	RG_CSI_XX_ToBC_HSAMP_BW	
5:4	RG_CSI_XX_ToBC_HSAMP_IS	
3	RG_CSI_XX_ToBC_HSAMP_SCB	
2	RG_CSI_XX_ToBC_HSAMP_SCA	
1	RG_CSI_XX_ToBC_HSAMP_LPBK_TEST_EN	
0	RG_CSI_XX_ToBC_HSAMP_MON_EN	

10217420 MIPI_RX_AN A20_CSI1A **HS AMP Control** **88008800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_L2_T1BC_HSAMP_SRB				RG_CSI_L2_T1BC_HSAMP_SRA				RG_CSI_L2_T1BC_HSAMP_BW		RG_CSI_L2_T1BC_HSAMP_IS		RG_CSI_L2_T1BC_HSAMP_SCB	RG_CSI_L2_T1BC_HSAMP_SCA	RG_CSI_L2_T1BC_HSAMP_LPBK_TEST_EN	RG_CSI_L2_T1BC_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_XX_T1CA_HSAMP_SRB				RG_CSI_XX_T1CA_HSAMP_SRA				RG_CSI_XX_T1CA_HSAMP_BW		RG_CSI_XX_T1CA_HSAMP_IS		RG_CSI_XX_T1CA_HSAMP_SCB	RG_CSI_XX_T1CA_HSAMP_SCA	RG_CSI_XX_T1CA_HSAMP_LPBK_TE	RG_CSI_XX_T1CA_HSAMP_MON_EN

															ST_EN	
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	RG_CSI_L2_T1BC_HSAMP_SRB	
27:24	RG_CSI_L2_T1BC_HSAMP_SRA	
23:22	RG_CSI_L2_T1BC_HSAMP_BW	
21:20	RG_CSI_L2_T1BC_HSAMP_IS	
19	RG_CSI_L2_T1BC_HSAMP_SCB	
18	RG_CSI_L2_T1BC_HSAMP_SCA	
17	RG_CSI_L2_T1BC_HSAMP_LPBK_TEST_EN	
16	RG_CSI_L2_T1BC_HSAMP_MON_EN	
15:12	RG_CSI_XX_T1CA_HSAMP_SRB	
11:8	RG_CSI_XX_T1CA_HSAMP_SRA	
7:6	RG_CSI_XX_T1CA_HSAMP_BW	
5:4	RG_CSI_XX_T1CA_HSAMP_IS	
3	RG_CSI_XX_T1CA_HSAMP_SCB	
2	RG_CSI_XX_T1CA_HSAMP_SCA	
1	RG_CSI_XX_T1CA_HSAMP_LPBK_TEST_EN	
0	RG_CSI_XX_T1CA_HSAMP_MON_EN	

10217424 MIPI_RX_ANA24_CSI1A **DPHY Deserializer Control** **0F000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_RESERVE											RG_CSI_DPHY_L2_SYNC_EDGE_SEL		RG_CSI_DPHY_L2_FORCE_SYNC		RG_CSI_DPHY_L2_BYPASS_BYTECK_INVERT
Type	RW											RW		RW		RW
Reset	0	0	0	0	1	1	1	1				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_DPHY_L2_BYTECK_INVERT		RG_CSI_DPHY_L1_SYNC_EDGE_SEL		RG_CSI_DPHY_L1_FORCE_SYNC		RG_CSI_DPHY_L1_BYPASS_BYTECK_INVERT	RG_CSI_DPHY_L1_BYTECK_INVERT			RG_CSI_DPHY_L0_SYNC_EDGE_SEL		RG_CSI_DPHY_L0_FORCE_SYNC		RG_CSI_DPHY_L0_BYPASS_BYTECK_INVERT	RG_CSI_DPHY_L0_BYTECK_INVERT
Type	RW		RW		RW		RW	RW			RW		RW		RW	RW
Reset	0		0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RG_CSI_RESERVE	
20:19	RG_CSI_DPHY_L2_SYNC_EDGE_SEL	

Bit(s)	Name	Description
18:17	RG_CSI_DPHY_L2_FORCE_SYNC	
16	RG_CSI_DPHY_L2_BYPASS_BYTECK_INVERT	
15	RG_CSI_DPHY_L2_BYTECK_INVERT	
13:12	RG_CSI_DPHY_L1_SYNC_EDGE_SEL	
11:10	RG_CSI_DPHY_L1_FORCE_SYNC	
9	RG_CSI_DPHY_L1_BYPASS_BYTECK_INVERT	
8	RG_CSI_DPHY_L1_BYTECK_INVERT	
5:4	RG_CSI_DPHY_L0_SYNC_EDGE_SEL	
3:2	RG_CSI_DPHY_L0_FORCE_SYNC	
1	RG_CSI_DPHY_L0_BYPASS_BYTECK_INVERT	
0	RG_CSI_DPHY_L0_BYTECK_INVERT	

10217428 MIPI_RX_AN A28_CSI1A **CPHY CDR Control** **0000888F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CSI_CPHY_To_CDR_EARLY_CODE					RG_CSI_CPHY_To_CDR_INIT_CODE							RG_CSI_CPHY_To_CDR_MANUAL_EN
Type				RW					RW							RW
Reset				0	0	0	0	0	0	0	0	0	0			0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_To_CDR_CA_WIDTH				RG_CSI_CPHY_To_CDR_BC_WIDTH				RG_CSI_CPHY_To_CDR_AB_WIDTH				RG_CSI_CPHY_To_CDR_LPF_CTRL		RG_CSI_CPHY_To_CDR_AUTOLOAD_EN	RG_CSI_CPHY_To_CDR_DIRECT_EN
Type	RW				RW				RW				RW		RW	RW
Reset	1	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1

Bit(s)	Name	Description
28:24	RG_CSI_CPHY_To_CDR_EARLY_CODE	
23:19	RG_CSI_CPHY_To_CDR_INIT_CODE	
16	RG_CSI_CPHY_To_CDR_MANUAL_EN	
15:12	RG_CSI_CPHY_To_CDR_CA_WIDTH	Filter out coding jitter
11:8	RG_CSI_CPHY_To_CDR_BC_WIDTH	Filter out coding jitter
7:4	RG_CSI_CPHY_To_CDR_AB_WIDTH	Filter out coding jitter
3:2	RG_CSI_CPHY_To_CDR_LPF_CT	

Bit(s)	Name	Description
	RL	
1	RG_CSI_CPHY_To_CDR_AUTOLOAD_EN	
0	RG_CSI_CPHY_To_CDR_DIRECT_EN	Direct Sample Mode Enable

1021742C MIPI_RX_ANA2C_CSI1A **CPHY CDR Control** **00002000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI_CPHY_To_DEBUG_EN	RG_CSI_CPHY_To_BIST_EN	RG_CSI_CPHY_To_BIST_AB											
Type			RW	RW	RW											
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_To_BIST_AB		RG_CSI_CPHY_To_HSDET_SEL					RG_CSI_CPHY_To_FORCE_INIT	RG_CSI_CPHY_To_SYNC_INIT_SEL	RG_CSI_CPHY_To_SYMCK_INVERT		RG_CSI_CPHY_To_CDR_LATE_CODE				
Type	RW		RW					RW	RW	RW		RW				
Reset	0	0	1	0				0	0	0		0	0	0	0	0

Bit(s)	Name	Description
29	RG_CSI_CPHY_To_DEBUG_EN	
28	RG_CSI_CPHY_To_BIST_EN	
27:14	RG_CSI_CPHY_To_BIST_AB	
13:12	RG_CSI_CPHY_To_HSDET_SEL	
8	RG_CSI_CPHY_To_FORCE_INIT	[NORMAL]1'b0: Self [NORMAL]1'b1: DA
7	RG_CSI_CPHY_To_SYNC_INIT_SEL	[NORMAL]1'b0: Self [NORMAL]1'b1: DA
6	RG_CSI_CPHY_To_SYMCK_INVERT	
4:0	RG_CSI_CPHY_To_CDR_LATE_CODE	

10217430 MIPI_RX_ANA30_CSI1A **CPHY CDR Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI_CPHY_To_BIST_CA													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_To_DEBUG_SEL		RG_CSI_CPHY_To_BIST_BC													
Type	RW		RW													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	RG_CSI_CPHY_To_BIST_CA	
15:14	RG_CSI_CPHY_To_DEBUG_SEL	
13:0	RG_CSI_CPHY_To_BIST_BC	

10217434 MIPI_RX_ANA34_CSI1A CPHY CDR Control 0000888F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CSI_CPHY_T1_CDR_EARLY_CODE					RG_CSI_CPHY_T1_CDR_INIT_CODE							RG_CSI_CPHY_T1_CDR_MANUAL_EN
Type				RW					RW							RW
Reset				0	0	0	0	0	0	0	0	0	0			0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_T1_CDR_CA_WIDTH				RG_CSI_CPHY_T1_CDR_BC_WIDTH				RG_CSI_CPHY_T1_CDR_AB_WIDTH				RG_CSI_CPHY_T1_CDR_LPF_CTRL		RG_CSI_CPHY_T1_CDR_AUTOLOAD_EN	RG_CSI_CPHY_T1_CDR_DIRECT_EN
Type	RW				RW				RW				RW		RW	RW
Reset	1	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1

Bit(s)	Name	Description
28:24	RG_CSI_CPHY_T1_CDR_EARLY_CODE	
23:19	RG_CSI_CPHY_T1_CDR_INIT_CODE	
16	RG_CSI_CPHY_T1_CDR_MANUAL_EN	
15:12	RG_CSI_CPHY_T1_CDR_CA_WIDTH	Filter out coding jitter
11:8	RG_CSI_CPHY_T1_CDR_BC_WIDTH	Filter out coding jitter
7:4	RG_CSI_CPHY_T1_CDR_AB_WIDTH	Filter out coding jitter
3:2	RG_CSI_CPHY_T1_CDR_LPF_CTRL	
1	RG_CSI_CPHY_T1_CDR_AUTOLOAD_EN	
0	RG_CSI_CPHY_T1_CDR_DIRECT_EN	Direct Sample Mode Enable

10217438 MIPI_RX_ANA38_CSI1A CPHY CDR Control 00002000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI_CPHY_	RG_CSI_CPHY_	RG_CSI_CPHY_T1_BIST_AB											

			T1_DEBUG_EN	T1_BIST_EN												
Type			RW	RW	RW											
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_T1_BIST_AB		RG_CSI_CPHY_T1_HSDET_SEL					RG_CSI_CPHY_T1_FORCE_INIT	RG_CSI_CPHY_T1_SYNC_INIT_SEL	RG_CSI_CPHY_T1_SYMCK_INVERT		RG_CSI_CPHY_T1_CDR_LATE_CODE				
Type	RW		RW					RW	RW	RW		RW				
Reset	0	0	1	0				0	0	0		0	0	0	0	0

Bit(s)	Name	Description
29	RG_CSI_CPHY_T1_DEBUG_EN	
28	RG_CSI_CPHY_T1_BIST_EN	
27:14	RG_CSI_CPHY_T1_BIST_AB	
13:12	RG_CSI_CPHY_T1_HSDET_SEL	
8	RG_CSI_CPHY_T1_FORCE_INIT	[NORMAL]1'b0: Self [NORMAL]1'b1: DA
7	RG_CSI_CPHY_T1_SYNC_INIT_SEL	[NORMAL]1'b0: Self [NORMAL]1'b1: DA
6	RG_CSI_CPHY_T1_SYMCK_INVERT	
4:0	RG_CSI_CPHY_T1_CDR_LATE_CODE	

1021743C MIPI_RX_ANA3C_CSI1A — CPHY CDR Control — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI_CPHY_T1_BIST_CA													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_T1_DEBUG_SEL		RG_CSI_CPHY_T1_BIST_BC													
Type	RW		RW													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	RG_CSI_CPHY_T1_BIST_CA	
15:14	RG_CSI_CPHY_T1_DEBUG_SEL	
13:0	RG_CSI_CPHY_T1_BIST_BC	

10217440 MIPI_RX_ANA40_CSI1A — GPI Control — 40404040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_CSI_L1N_G	RG_CSI_L1N_GPI_RDSEL		RG_CSI_L1N_G	RG_CSI_L1N_G	RG_CSI_L1N_G	RG_CSI_L1N_G		RG_CSI_L1P_G	RG_CSI_L1P_GPI_RDSEL		RG_CSI_L1P_G	RG_CSI_L1P_G	RG_CSI_L1P_G	RG_CSI_L1P_G

		PI_G			PI_PD	PI_PU	PI_SMT	PI_IES		PI_G			PI_PD	PI_PU	PI_SMT	PI_IES
Type		RW	RW		RW	RW	RW	RW		RW	RW		RW	RW	RW	RW
Reset		1	0	0	0	0	0	0		1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI_LoN_GPI_G	RG_CSI_LoN_GPI_RDSEL		RG_CSI_LoN_GPI_PD	RG_CSI_LoN_GPI_PU	RG_CSI_LoN_GPI_SMT	RG_CSI_LoN_GPI_IES		RG_CSI_LoP_GPI_G	RG_CSI_LoP_GPI_RDSEL		RG_CSI_LoP_GPI_PD	RG_CSI_LoP_GPI_PU	RG_CSI_LoP_GPI_SMT	RG_CSI_LoP_GPI_IES
Type		RW	RW		RW	RW	RW	RW		RW	RW		RW	RW	RW	RW
Reset		1	0	0	0	0	0	0		1	0	0	0	0	0	0

Bit(s)	Name	Description
30	RG_CSI_L1N_GPI_G	**RX Input Control Gating**
29:28	RG_CSI_L1N_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
27	RG_CSI_L1N_GPI_PD	**75K pull-down resistor control. High activiate.**
26	RG_CSI_L1N_GPI_PU	**75K pull-up resistor control. High activiate.**
25	RG_CSI_L1N_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
24	RG_CSI_L1N_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.
22	RG_CSI_L1P_GPI_G	**RX Input Control Gating**
21:20	RG_CSI_L1P_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
19	RG_CSI_L1P_GPI_PD	**75K pull-down resistor control. High activiate.**
18	RG_CSI_L1P_GPI_PU	**75K pull-up resistor control. High activiate.**
17	RG_CSI_L1P_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
16	RG_CSI_L1P_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.
14	RG_CSI_LoN_GPI_G	**RX Input Control Gating**
13:12	RG_CSI_LoN_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00]

Bit(s)	Name	Description
		1.2V: RDSEL[1:0]=[11]
11	RG_CSI_L0N_GPI_PD	**75K pull-down resistor control. High activiate.**
10	RG_CSI_L0N_GPI_PU	**75K pull-up resistor control. High activiate.**
9	RG_CSI_L0N_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
8	RG_CSI_L0N_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.
6	RG_CSI_L0P_GPI_G	**RX Input Control Gating**
5:4	RG_CSI_L0P_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
3	RG_CSI_L0P_GPI_PD	**75K pull-down resistor control. High activiate.**
2	RG_CSI_L0P_GPI_PU	**75K pull-up resistor control. High activiate.**
1	RG_CSI_L0P_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
0	RG_CSI_L0P_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.

10217444 MIPI_RX_AN_A44_CSI1A GPI Control 00004040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI_L2N_GPI_G	RG_CSI_L2N_GPI_RDSEL		RG_CSI_L2N_GPI_PD	RG_CSI_L2N_GPI_PU	RG_CSI_L2N_GPI_SMT	RG_CSI_L2N_GPI_IES		RG_CSI_L2P_GPI_G	RG_CSI_L2P_GPI_RDSEL		RG_CSI_L2P_GPI_PD	RG_CSI_L2P_GPI_PU	RG_CSI_L2P_GPI_SMT	RG_CSI_L2P_GPI_IES
Type		RW	RW		RW	RW	RW	RW		RW	RW		RW	RW	RW	RW
Reset		1	0	0	0	0	0	0		1	0	0	0	0	0	0

Bit(s)	Name	Description
14	RG_CSI_L2N_GPI_G	**RX Input Control Gating**
13:12	RG_CSI_L2N_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]

Bit(s)	Name	Description
11	RG_CSI_L2N_GPI_PD	**75K pull-down resistor control. High activiate.**
10	RG_CSI_L2N_GPI_PU	**75K pull-up resistor control. High activiate.**
9	RG_CSI_L2N_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
8	RG_CSI_L2N_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.
6	RG_CSI_L2P_GPI_G	**RX Input Control Gating**
5:4	RG_CSI_L2P_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
3	RG_CSI_L2P_GPI_PD	**75K pull-down resistor control. High activiate.**
2	RG_CSI_L2P_GPI_PU	**75K pull-up resistor control. High activiate.**
1	RG_CSI_L2P_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
0	RG_CSI_L2P_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.

10217448 MIPI_RX_AN A48_CSI1A RGS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AD_CSI_CPHY_T1_DEBUG_OUT	AD_CSI_CPHY_T1_BIST_CHECK_OUT	AD_CSI_CPHY_To_DEBUG_OUT	AD_CSI_CPHY_To_BIST_CHECK_OUT	AD_CSI_L2N_GPI_OUT	AD_CSI_L2P_GPI_OUT	AD_CSI_L1N_GPI_OUT	AD_CSI_L1P_GPI_OUT	AD_CSI_L0N_GPI_OUT	AD_CSI_L0P_GPI_OUT
Type							RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RGS_CSI_CPHY_T1_CDR_CODE								RGS_CSI_CPHY_To_CDR_CODE				
Type				RU								RU				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
25	AD_CSI_CPHY_T1_DEBUG_OUT	
24	AD_CSI_CPHY_T1_BIST_CHECK_OUT	
23	AD_CSI_CPHY_To_DEBUG_OUT	
22	AD_CSI_CPHY_To_BIST_CHECK_OUT	
21	AD_CSI_L2N_GPI_OUT	
20	AD_CSI_L2P_GPI_OUT	

Bit(s)	Name	Description
19	AD_CSI_L1N_GPI_OUT	
18	AD_CSI_L1P_GPI_OUT	
17	AD_CSI_L0N_GPI_OUT	
16	AD_CSI_L0P_GPI_OUT	
12:8	RGS_CSI_CPHY_T1_CDR_CODE	
4:0	RGS_CSI_CPHY_T0_CDR_CODE	

1021744C **MIPI_RX_AN A4C_CSI1A** **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DA_CSI_CDPHY_L2N_T1C_HSRT_EN	DA_CSI_CDPHY_L2P_T1B_HSRT_EN	DA_CSI_CDPHY_L1N_T1A_HSRT_EN	DA_CSI_CDPHY_L1P_T0C_HSRT_EN	DA_CSI_CDPHY_L0N_T0B_HSRT_EN	DA_CSI_CDPHY_L0P_T0A_HSRT_EN	AD_CSI_DPHY_L2N_HSDET_OUT	DA_CSI_DPHY_L2N_HSDET_RSTB	AD_CSI_DPHY_L2P_HSDET_OUT	DA_CSI_DPHY_L2P_HSDET_RSTB	AD_CSI_DPHY_L1N_HSDET_OUT	DA_CSI_DPHY_L1N_HSDET_RSTB	AD_CSI_DPHY_L1P_HSDET_OUT	DA_CSI_DPHY_L1P_HSDET_RSTB
Type			RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AD_CSI_DPHY_L0N_HSDET_OUT	DA_CSI_DPHY_L0N_HSDET_RSTB	AD_CSI_DPHY_L0P_HSDET_OUT	DA_CSI_DPHY_L0P_HSDET_RSTB	AD_CSI_CDPHY_L2N_T1C_LPRX_OUT	DA_CSI_CDPHY_L2N_T1C_LPRX_EN	AD_CSI_CDPHY_L2P_T1B_LPRX_OUT	DA_CSI_CDPHY_L2P_T1B_LPRX_EN	AD_CSI_CDPHY_L1N_T1A_LPRX_OUT	DA_CSI_CDPHY_L1N_T1A_LPRX_EN	AD_CSI_CDPHY_L1P_T0C_LPRX_OUT	DA_CSI_CDPHY_L1P_T0C_LPRX_EN	AD_CSI_CDPHY_L0N_T0B_LPRX_OUT	DA_CSI_CDPHY_L0N_T0B_LPRX_EN	AD_CSI_CDPHY_L0P_T0A_LPRX_OUT	DA_CSI_CDPHY_L0P_T0A_LPRX_EN
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29	DA_CSI_CDPHY_L2N_T1C_HSRT_EN	
28	DA_CSI_CDPHY_L2P_T1B_HSRT_EN	
27	DA_CSI_CDPHY_L1N_T1A_HSRT_EN	
26	DA_CSI_CDPHY_L1P_T0C_HSRT_EN	
25	DA_CSI_CDPHY_L0N_T0B_HSRT_EN	
24	DA_CSI_CDPHY_L0P_T0A_HSRT_EN	
23	AD_CSI_DPHY_L2N_HSDET_OUT	
22	DA_CSI_DPHY_L2N_HSDET_RSTB	
21	AD_CSI_DPHY_L2P_HSDET_OUT	
20	DA_CSI_DPHY_L2P_HSDET_RSTB	
19	AD_CSI_DPHY_L1N_HSDET_OUT	
18	DA_CSI_DPHY_L1N_HSDET_RSTB	
17	AD_CSI_DPHY_L1P_HSDET_OUT	
16	DA_CSI_DPHY_L1P_HSDET_RSTB	

Bit(s)	Name	Description
15	AD_CSI_DPHY_L0N_HSDET_OUT	
14	DA_CSI_DPHY_L0N_HSDET_RSTB	
13	AD_CSI_DPHY_L0P_HSDET_OUT	
12	DA_CSI_DPHY_L0P_HSDET_RSTB	
11	AD_CSI_CDPHY_L2N_T1C_LPRX_OUT	
10	DA_CSI_CDPHY_L2N_T1C_LPRX_EN	
9	AD_CSI_CDPHY_L2P_T1B_LPRX_OUT	
8	DA_CSI_CDPHY_L2P_T1B_LPRX_EN	
7	AD_CSI_CDPHY_L1N_T1A_LPRX_OUT	
6	DA_CSI_CDPHY_L1N_T1A_LPRX_EN	
5	AD_CSI_CDPHY_L1P_T0C_LPRX_OUT	
4	DA_CSI_CDPHY_L1P_T0C_LPRX_EN	
3	AD_CSI_CDPHY_L0N_T0B_LPRX_OUT	
2	DA_CSI_CDPHY_L0N_T0B_LPRX_EN	
1	AD_CSI_CDPHY_L0P_T0A_LPRX_OUT	
0	DA_CSI_CDPHY_L0P_T0A_LPRX_EN	

10217450 MIPI_RX_AN A50_CSI1A **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AD_CSI_CPHY_ToCA_HSAMP_OS_CK	AD_CSI_CPHY_ToCA_HSAMP_OS_OUT	DA_CSI_CPHY_ToCA_HSAMP_OS_CODE					DA_CSI_CPHY_ToCA_HSAMP_OS_CAL_EN	DA_CSI_CPHY_ToCA_HSAMP_OS_APPLY	DA_CSI_CPHY_ToCA_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							AD_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CK	AD_CSI_CDPHY_Lo_ToAB_HSAMP_OS_OUT	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CODE					DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CAL_EN	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_APPLY	DA_CSI_CDPHY_Lo_ToAB_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
25	AD_CSI_CPHY_ToCA_HSAMP_OS_CK	
24	AD_CSI_CPHY_ToCA_HSAMP_OS_OUT	
23:19	DA_CSI_CPHY_ToCA_HSAMP_OS_CODE	
18	DA_CSI_CPHY_ToCA_HSAMP_OS_CAL_EN	
17	DA_CSI_CPHY_ToCA_HSAMP_OS_APPLY	
16	DA_CSI_CPHY_ToCA_HSAMP_EN	
9	AD_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CK	
8	AD_CSI_CDPHY_Lo_ToAB_HSAMP_OS_OUT	
7:3	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CODE	
2	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CAL_EN	
1	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_APPLY	
0	DA_CSI_CDPHY_Lo_ToAB_HSAMP_EN	

10217454 MIPI_RX_AN A54_CSI1A **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AD_CSI_CDPHY_L1_T1AB_HSAMP_OS_CK	AD_CSI_CDPHY_L1_T1AB_HSAMP_OS_OUT	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_CODE					DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_CAL_EN	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_APPLY	DA_CSI_CDPHY_L1_T1AB_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							AD_CSI_CPHY_ToBC_HSAMP_OS_CK	AD_CSI_CPHY_ToBC_HSAMP_OS_OUT	DA_CSI_CPHY_ToBC_HSAMP_OS_CODE					DA_CSI_CPHY_ToBC_HSAMP_OS_CAL_EN	DA_CSI_CPHY_ToBC_HSAMP_OS_APPLY	DA_CSI_CPHY_ToBC_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25	AD_CSI_CDPHY_L1_T1AB_HSAMP_OS_CK	
24	AD_CSI_CDPHY_L1_T1AB_HSAMP_OS_OUT	
23:19	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_CODE	
18	DA_CSI_CDPHY_L1_T1AB_HSAM	

Bit(s)	Name	Description
	P_OS_CAL_EN	
17	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_APPLY	
16	DA_CSI_CDPHY_L1_T1AB_HSAMP_EN	
9	AD_CSI_CPHY_T0BC_HSAMP_OS_CK	
8	AD_CSI_CPHY_T0BC_HSAMP_OS_OUT	
7:3	DA_CSI_CPHY_T0BC_HSAMP_OS_CODE	
2	DA_CSI_CPHY_T0BC_HSAMP_OS_CAL_EN	
1	DA_CSI_CPHY_T0BC_HSAMP_OS_APPLY	
0	DA_CSI_CPHY_T0BC_HSAMP_EN	

10217458 MIPI_RX_ANA58_CSI1A **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AD_CSI_CDPHY_L2_T1BC_HSAMP_OS_CK	AD_CSI_CDPHY_L2_T1BC_HSAMP_OS_OUT	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_CODE					DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_CAL_EN	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_APPLY	DA_CSI_CDPHY_L2_T1BC_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							AD_CSI_CPHY_T1CA_HSAMP_OS_CK	AD_CSI_CPHY_T1CA_HSAMP_OS_OUT	DA_CSI_CPHY_T1CA_HSAMP_OS_CODE					DA_CSI_CPHY_T1CA_HSAMP_OS_CAL_EN	DA_CSI_CPHY_T1CA_HSAMP_OS_APPLY	DA_CSI_CPHY_T1CA_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25	AD_CSI_CDPHY_L2_T1BC_HSAMP_OS_CK	
24	AD_CSI_CDPHY_L2_T1BC_HSAMP_OS_OUT	
23:19	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_CODE	
18	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_CAL_EN	
17	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_APPLY	
16	DA_CSI_CDPHY_L2_T1BC_HSAMP_EN	
9	AD_CSI_CPHY_T1CA_HSAMP_OS_CK	

Bit(s)	Name	Description
8	AD_CSI_CPHY_T1CA_HSAMP_OS_OUT	
7:3	DA_CSI_CPHY_T1CA_HSAMP_OS_CODE	
2	DA_CSI_CPHY_T1CA_HSAMP_OS_CAL_EN	
1	DA_CSI_CPHY_T1CA_HSAMP_OS_APPLY	
0	DA_CSI_CPHY_T1CA_HSAMP_EN	

1021745C MIPI_RX_ANA5C_CSI1A **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSI_DPHY_Lo_DELAY_CODE							AD_CSI_DPHY_Lo_BYPASS_BYTE_DATA							
Type		RU							RU							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_DPHY_Lo_DELAY_APPLY	DA_CSI_DPHY_Lo_DELAY_EN	AD_CSI_DPHY_Lo_BYPASS_BYTE_CK	AD_CSI_DPHY_Lo_SYNC_DETECT	AD_CSI_DPHY_Lo_BYTE_DATA								AD_CSI_DPHY_Lo_BYTE_CK	DA_CSI_DPHY_Lo_DES_SYNC_INIT	DA_CSI_DPHY_Lo_DES_EN	DA_CSI_DPHY_Lo_SAMP_EN
Type	RU	RU	RU	RU	RU								RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	DA_CSI_DPHY_Lo_DELAY_CODE	
23:16	AD_CSI_DPHY_Lo_BYPASS_BYTE_DATA	
15	DA_CSI_DPHY_Lo_DELAY_APPLY	
14	DA_CSI_DPHY_Lo_DELAY_EN	
13	AD_CSI_DPHY_Lo_BYPASS_BYTE_CK	
12	AD_CSI_DPHY_Lo_SYNC_DETECT	
11:4	AD_CSI_DPHY_Lo_BYTE_DATA	
3	AD_CSI_DPHY_Lo_BYTE_CK	
2	DA_CSI_DPHY_Lo_DES_SYNC_INIT	
1	DA_CSI_DPHY_Lo_DES_EN	
0	DA_CSI_DPHY_Lo_SAMP_EN	

10217460 MIPI_RX_ANA60_CSI1A **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSI_DPHY_L1_DELAY_CODE							AD_CSI_DPHY_L1_BYPASS_BYTE_DATA							
Type		RU							RU							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	DA_CSI_DPHY_L1_DELAY_APPLY	DA_CSI_DPHY_L1_DELAY_EN	AD_CSI_DPHY_L1_BYPASS_BYTE_CK	AD_CSI_DPHY_L1_SYNC_DETECT	AD_CSI_DPHY_L1_BYTE_DATA								AD_CSI_DPHY_L1_BYTE_CK	DA_CSI_DPHY_L1_DES_SYNC_INIT	DA_CSI_DPHY_L1_DES_EN	DA_CSI_DPHY_L1_SAMP_EN
Type	RU	RU	RU	RU	RU								RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	DA_CSI_DPHY_L1_DELAY_CODE	
23:16	AD_CSI_DPHY_L1_BYPASS_BYTE_DATA	
15	DA_CSI_DPHY_L1_DELAY_APPLY	
14	DA_CSI_DPHY_L1_DELAY_EN	
13	AD_CSI_DPHY_L1_BYPASS_BYTE_CK	
12	AD_CSI_DPHY_L1_SYNC_DETECT	
11:4	AD_CSI_DPHY_L1_BYTE_DATA	
3	AD_CSI_DPHY_L1_BYTE_CK	
2	DA_CSI_DPHY_L1_DES_SYNC_INIT	
1	DA_CSI_DPHY_L1_DES_EN	
0	DA_CSI_DPHY_L1_SAMP_EN	

10217464 MIPI_RX_ANA64_CSI1A DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSI_DPHY_L2_DELAY_CODE							AD_CSI_DPHY_L2_BYPASS_BYTE_DATA							
Type		RU							RU							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_DPHY_L2_DELAY_APPLY	DA_CSI_DPHY_L2_DELAY_EN	AD_CSI_DPHY_L2_BYPASS_BYTE_CK	AD_CSI_DPHY_L2_SYNC_DETECT	AD_CSI_DPHY_L2_BYTE_DATA								AD_CSI_DPHY_L2_BYTE_CK	DA_CSI_DPHY_L2_DES_SYNC_INIT	DA_CSI_DPHY_L2_DES_EN	DA_CSI_DPHY_L2_SAMP_EN
Type	RU	RU	RU	RU	RU								RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	DA_CSI_DPHY_L2_DELAY_CODE	
23:16	AD_CSI_DPHY_L2_BYPASS_BYTE_DATA	
15	DA_CSI_DPHY_L2_DELAY_APPLY	
14	DA_CSI_DPHY_L2_DELAY_EN	
13	AD_CSI_DPHY_L2_BYPASS_BYTE_CK	
12	AD_CSI_DPHY_L2_SYNC_DETECT	

Bit(s)	Name	Description
11:4	AD_CSI_DPHY_L2_BYTE_DATA	
3	AD_CSI_DPHY_L2_BYTE_CK	
2	DA_CSI_DPHY_L2_DES_SYNC_INIT	
1	DA_CSI_DPHY_L2_DES_EN	
0	DA_CSI_DPHY_L2_SAMP_EN	

10217468 MIPI_RX_AN A68_CSI1A **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AD_CSI_CPHY_To_HSDET_OUT	DA_CSI_CPHY_To_SYNC_INIT
Type															RU	RU
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_CPHY_To_DES_EN	DA_CSI_CPHY_To_CDR_EN	AD_CSI_CPHY_To_AB													
Type	RU	RU	RU													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	AD_CSI_CPHY_To_HSDET_OUT	
16	DA_CSI_CPHY_To_SYNC_INIT	
15	DA_CSI_CPHY_To_DES_EN	
14	DA_CSI_CPHY_To_CDR_EN	
13:0	AD_CSI_CPHY_To_AB	

1021746C MIPI_RX_AN A6C_CSI1A **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AD_CSI_CPHY_To_BC													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	AD_CSI_CPHY_To_BC	

10217470 MIPI_RX_AN **DEBUG** **00000000**

A70_CSI1A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AD_CSI_CPHY_To_CA													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	AD_CSI_CPHY_To_CA	

10217474 MIPI_RX_AN A74_CSI1A DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AD_CSI_CPHY_T1_HSDET_OUT	DA_CSI_CPHY_T1_SYNC_INIT
Type															RU	RU
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_CPHY_T1_DES_EN	DA_CSI_CPHY_T1_CDR_EN	AD_CSI_CPHY_T1_AB													
Type	RU	RU	RU													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	AD_CSI_CPHY_T1_HSDET_OUT	
16	DA_CSI_CPHY_T1_SYNC_INIT	
15	DA_CSI_CPHY_T1_DES_EN	
14	DA_CSI_CPHY_T1_CDR_EN	
13:0	AD_CSI_CPHY_T1_AB	

10217478 MIPI_RX_AN A78_CSI1A DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AD_CSI_CPHY_T1_BC													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	AD_CSI_CPHY_T1_BC	

1021747C MIPI_RX_ANA7C_CSI1A DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AD_CSI_CPHY_T1_CA													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	AD_CSI_CPHY_T1_CA	

10217480 MIPI_RX_WRAPPER80_CSI1A WRAPPER 04000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CSR_CSIo_DPHY_MUX			CSR_SW_RST				CSR_CSI1_CPHY_RST_MODE		CSR_CSI1_DPHY_RST_MODE		CSR_CSIo_CPHY_RST_MODE		CSR_CSIo_DPHY_RST_MODE	
Type		RW			RW				RW		RW		RW		RW	
Reset		0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_CSI_MON_MUX								CSR_CSI_MODE				CSR_CSI1_DPHY_MUX		CSR_HSDET_MODE	CSR_CSI_CLK_MON
Type	RW								RW				RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:28	CSR_CSIo_DPHY_MUX	
27:24	CSR_SW_RST	
23:22	CSR_CSI1_CPHY_RST_MODE	0: sync init 1: hsrx_en 2: sw rst 3: hw rst
21:20	CSR_CSI1_DPHY_RST_MODE	0: sync init 1: hsrx_en 2: sw rst 3: hw rst
19:18	CSR_CSIo_CPHY_RST_MODE	0: sync init 1: hsrx_en 2: sw rst 3: hw rst
17:16	CSR_CSIo_DPHY_RST_MODE	0: sync init 1: hsrx_en

Bit(s)	Name	Description
		2: sw rst 3: hw rst
15:8	CSR_CSI_MON_MUX	
7:4	CSR_CSI_MODE	0:4 lane 1:2/2l lane 2:cphy 4:cphy/2 lane
3:2	CSR_CSI1_DPHY_MUX	
1	CSR_HSDET_MODE	0: dn 1: dp
0	CSR_CSI_CLK_MON	Enable Clock monitor

10217484 MIPI_RX_WRAPPER84_CSI1A WRAPPER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI_DEBUG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI_DEBUG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSI_DEBUG_OUT	

10217488 MIPI_RX_WRAPPER88_CSI1A WRAPPER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_MODE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_MODE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_MODE_0	

1021748C MIPI_RX_WRAPPER8C_CSI1A WRAPPER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_MODE_1															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_MODE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_MODE_1	

10217490 MIPI_RX_WRAPPER90_CSI1A **WRAPPER** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_MODE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_MODE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_MODE_2	

10217494 MIPI_RX_WRAPPER94_CSI1A **WRAPPER** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_VALUE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_VALUE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_VALUE_0	

10217498 MIPI_RX_WRAPPER98_CSI1A **WRAPPER** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_VALUE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	CSR_SW_VALUE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_VALUE_1	

1021749C MIPI_RX_WRAPPER9C_CSI1A WRAPPER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_VALUE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_VALUE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_VALUE_2	

10217600 MIPI_RX_ANA00_CSI1B 2D1C Global Control 00000492

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_CSI_DPHY_L2_CKSEL	RG_CSI_DPHY_L2_CKMODE_EN	RG_CSI_DPHY_L2_BYPASS_SYNC	RG_CSI_DPHY_L1_CKSEL	RG_CSI_DPHY_L1_CKMODE_EN	RG_CSI_DPHY_L1_BYPASS_SYNC	RG_CSI_DPHY_L0_CKSEL	RG_CSI_DPHY_L0_CKMODE_EN	RG_CSI_DPHY_L0_BYPASS_SYNC	RG_CSI_BG_CORE_EN	RG_CSI_BG_LPF_EN	RG_CSI_HSAMP_PROTECT_EN	RG_CSI_CPHY_EN
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	1	0	0	1	0	0	1	0	0	1	0

Bit(s)	Name	Description
12	RG_CSI_DPHY_L2_CKSEL	**Data Mode** [NORMAL]1'b0: Sample data by Local Clock [NORMAL]1'b1: Sample data by Common Clock CK Mode [NORMAL]1'b0: Connect to Local Clock [NORMAL]1'b1: Connect to Common Clock
11	RG_CSI_DPHY_L2_CKMODE_EN	**[NORMAL]1'b0: Data Mode** [NORMAL]1'b1: CK Mode
10	RG_CSI_DPHY_L2_BYPASS_SYNC	**Bypass or Sync Mode Selection** [NORMAL]1'b0: Sync Mode [NORMAL]1'b1: Bypass Mode
9	RG_CSI_DPHY_L1_CKSEL	**Data Mode**

Bit(s)	Name	Description
		[NORMAL]1'b0: Sample data by Local Clock [NORMAL]1'b1: Sample data by Common Clock
		CK Mode [NORMAL]1'b0: Connect to Local Clock [NORMAL]1'b1: Connect to Common Clock
8	RG_CSI_DPHY_L1_CKMODE_EN	**[NORMAL]1'b0: Data Mode** [NORMAL]1'b1: CK Mode
7	RG_CSI_DPHY_L1_BYPASS_SYNC	**Bypass or Sync Mode Selection** [NORMAL]1'b0: Sync Mode [NORMAL]1'b1: Bypass Mode
6	RG_CSI_DPHY_L0_CKSEL	**Data Mode** [NORMAL]1'b0: Sample data by Local Clock [NORMAL]1'b1: Sample data by Common Clock
		CK Mode [NORMAL]1'b0: Connect to Local Clock [NORMAL]1'b1: Connect to Common Clock
5	RG_CSI_DPHY_L0_CKMODE_EN	**[NORMAL]1'b0: Data Mode** [NORMAL]1'b1: CK Mode
4	RG_CSI_DPHY_L0_BYPASS_SYNC	**Bypass or Sync Mode Selection** [NORMAL]1'b0: Sync Mode [NORMAL]1'b1: Bypass Mode
3	RG_CSI_BG_CORE_EN	**[NORMAL]1'b0: Bandgap Disable** [NORMAL]1'b1: Bandgap Enable
2	RG_CSI_BG_LPF_EN	**[NORMAL]1'b0: Bandgap low pass filter Disable** [NORMAL]1'b1: Bandgap low pass filter Enable
1	RG_CSI_HSAMP_PROTECT_EN	**HSAMP Protection** [NORMAL]1'b0: Disable [NORMAL]1'b1: Enable
0	RG_CSI_CPHY_EN	**1'b0: DPHY Mode** 1'b1: CPHY Mode

10217604 MIPI_RX_AN_A04_CSI1B 2D1C Global Control 00084444

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CSI_FORCE_HSRT_EN	RG_CSI_BG_MON_VREF_SEL								RG_CSI_BG_VREF_SEL			
Type				RW	RW								RW			
Reset				0	0	0	0	0					1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI_BG_HSDET_VTL_SEL				RG_CSI_BG_HSDET_VTH_SEL				RG_CSI_BG_LPRX_VTL_SEL				RG_CSI_BG_LPRX_VTH_SEL		
Type		RW				RW				RW				RW		
Reset		1	0	0		1	0	0		1	0	0		1	0	0

Bit(s)	Name	Description
28	RG_CSI_FORCE_HSRT_EN	**Force HSRT Enable to do FT calibration and eFuse**
27:24	RG_CSI_BG_MON_VREF_SEL	**Monitor Selection**
19:16	RG_CSI_BG_VREF_SEL	**HSAMP LDO Reference Voltage** Default 0.9V
14:12	RG_CSI_BG_HSDET_VTL_SEL	**HSDET VTH Selection** Default 0.12V
10:8	RG_CSI_BG_HSDET_VTH_SEL	**HSDET VTH Selection** Default 0.15V

Bit(s)	Name	Description
6:4	RG_CSI_BG_LPRX_VTL_SEL	**LPRX VTL Selection** Default 0.70V
2:0	RG_CSI_BG_LPRX_VTH_SEL	**LPRX VTH Selection** Default 0.75V

10217608 MIPI_RX_AN_A08_CSI1B High Speed Termination Control 10101010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CSI_L1N_T1A_HSRT_CODE								RG_CSI_L1P_T0C_HSRT_CODE				
Type				RW								RW				
Reset				1	0	0	0	0				1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_CSI_L0N_T0B_HSRT_CODE								RG_CSI_L0P_T0A_HSRT_CODE				
Type				RW								RW				
Reset				1	0	0	0	0				1	0	0	0	0

Bit(s)	Name	Description
28:24	RG_CSI_L1N_T1A_HSRT_CODE	**Termination code** 800ohm/(8+N) Requires Calibration & Efuse on FT
20:16	RG_CSI_L1P_T0C_HSRT_CODE	**Termination code** 800ohm/(8+N) Requires Calibration & Efuse on FT
12:8	RG_CSI_L0N_T0B_HSRT_CODE	**Termination code** 800ohm/(8+N) Requires Calibration & Efuse on FT
4:0	RG_CSI_L0P_T0A_HSRT_CODE	**Termination code** 800ohm/(8+N) Requires Calibration & Efuse on FT

1021760C MIPI_RX_AN_A0C_CSI1B High Speed Termination Control 00001010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_CSI_L2N_T1C_HSRT_CODE								RG_CSI_L2P_T1B_HSRT_CODE				
Type				RW								RW				
Reset				1	0	0	0	0				1	0	0	0	0

Bit(s)	Name	Description
12:8	RG_CSI_L2N_T1C_HSRT_CODE	**Termination code** 800ohm/(8+N) Requires Calibration & Efuse on FT
4:0	RG_CSI_L2P_T1B_HSRT_CODE	**Termination code** 800ohm/(8+N) Requires Calibration & Efuse on FT

Bit(s)	Name	Description

10217610 MIPI_RX_AN A10_CSI1B **Bandgap Voltage for Delay Line Calibration** **80808080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_CPHY_To_VREF_SEL						RG_CSI_CPHY_To_CDR_DELAYCAL_RSTB	RG_CSI_CPHY_To_CDR_DELAYCAL_EN	RG_CSI_DPHY_L2_VREF_SEL						RG_CSI_DPHY_L2_DELAYCAL_RSTB	RG_CSI_DPHY_L2_DELAYCAL_EN
Type	RW						RW	RW	RW						RW	RW
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_DPHY_L1_VREF_SEL						RG_CSI_DPHY_L1_DELAYCAL_RSTB	RG_CSI_DPHY_L1_DELAYCAL_EN	RG_CSI_DPHY_Lo_VREF_SEL						RG_CSI_DPHY_Lo_DELAYCAL_RSTB	RG_CSI_DPHY_Lo_DELAYCAL_EN
Type	RW						RW	RW	RW						RW	RW
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:26	RG_CSI_CPHY_To_VREF_SEL	**Do Delay Line Reference Voltage** Requires Software Calibration
25	RG_CSI_CPHY_To_CDR_DELAYCAL_RSTB	**TRIOo Delay Line Calibration Reset Bar**
24	RG_CSI_CPHY_To_CDR_DELAYCAL_EN	**TRIOo Delay Line Calibration Enable**
23:18	RG_CSI_DPHY_L2_VREF_SEL	**Do Delay Line Reference Voltage** Requires Software Calibration
17	RG_CSI_DPHY_L2_DELAYCAL_RSTB	**D1 Delay Line Calibration Reset Bar**
16	RG_CSI_DPHY_L2_DELAYCAL_EN	**D1 Delay Line Calibration Enable**
15:10	RG_CSI_DPHY_L1_VREF_SEL	**Do Delay Line Reference Voltage** Requires Software Calibration
9	RG_CSI_DPHY_L1_DELAYCAL_RSTB	**CK Delay Line Calibration Reset Bar**
8	RG_CSI_DPHY_L1_DELAYCAL_EN	**CK Delay Line Calibration Enable**
7:2	RG_CSI_DPHY_Lo_VREF_SEL	**Do Delay Line Reference Voltage** Requires Software Calibration
1	RG_CSI_DPHY_Lo_DELAYCAL_RSTB	**Do Delay Line Calibration Reset Bar**
0	RG_CSI_DPHY_Lo_DELAYCAL_EN	**Do Delay Line Calibration Enable**

10217614 MIPI_RX_AN A14_CSI1B **Bandgap Voltage for Delay Line Calibration** **00000080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSI_CPHY_T1_VREF_SEL						RG_CSI_CPHY_T1_CDR_DELAYCAL_RSTB	RG_CSI_CPHY_T1_CDR_DELAYCAL_EN
Type									RW						RW	RW
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSI_CPHY_T1_VREF_SEL	**D0 Delay Line Reference Voltage** Requires Software Calibration
1	RG_CSI_CPHY_T1_CDR_DELAYCAL_RSTB	**TRIO1 Delay Line Calibration Reset Bar**
0	RG_CSI_CPHY_T1_CDR_DELAYCAL_EN	**TRIO1 Delay Line Calibration Enable**

10217618 MIPI_RX_ANA18_CSI1B HS AMP Control 88008800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_XX_ToCA_HSAMP_SRB				RG_CSI_XX_ToCA_HSAMP_SRA				RG_CSI_XX_ToCA_HSAMP_BW		RG_CSI_XX_ToCA_HSAMP_IS		RG_CSI_XX_ToCA_HSAMP_SCB	RG_CSI_XX_ToCA_HSAMP_SCA	RG_CSI_XX_ToCA_HSAMP_LPBK_TEST_EN	RG_CSI_XX_ToCA_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_Lo_ToAB_HSAMP_SRB				RG_CSI_Lo_ToAB_HSAMP_SRA				RG_CSI_Lo_ToAB_HSAMP_BW		RG_CSI_Lo_ToAB_HSA MP_IS		RG_CSI_Lo_ToAB_HSAMP_SCB	RG_CSI_Lo_ToAB_HSAMP_SCA	RG_CSI_Lo_ToAB_HSAMP_LPBK_TEST_EN	RG_CSI_Lo_ToAB_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	RG_CSI_XX_ToCA_HSAMP_SRB	
27:24	RG_CSI_XX_ToCA_HSAMP_SRA	
23:22	RG_CSI_XX_ToCA_HSAMP_BW	
21:20	RG_CSI_XX_ToCA_HSAMP_IS	
19	RG_CSI_XX_ToCA_HSAMP_SCB	
18	RG_CSI_XX_ToCA_HSAMP_SCA	
17	RG_CSI_XX_ToCA_HSAMP_LPBK_TEST_EN	

Bit(s)	Name	Description
16	RG_CSI_XX_ToCA_HSAMP_MON_EN	
15:12	RG_CSI_Lo_ToAB_HSAMP_SRB	
11:8	RG_CSI_Lo_ToAB_HSAMP_SRA	
7:6	RG_CSI_Lo_ToAB_HSAMP_BW	
5:4	RG_CSI_Lo_ToAB_HSAMP_IS	
3	RG_CSI_Lo_ToAB_HSAMP_SCB	
2	RG_CSI_Lo_ToAB_HSAMP_SCA	
1	RG_CSI_Lo_ToAB_HSAMP_LPBK_TEST_EN	
0	RG_CSI_Lo_ToAB_HSAMP_MON_EN	

1021761C MIPI_RX_ANA1C_CSI1B HS AMP Control 88008800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_L1_T1AB_HSAMP_SRB				RG_CSI_L1_T1AB_HSAMP_SRA				RG_CSI_L1_T1AB_HSAMP_BW		RG_CSI_L1_T1AB_HSAMP_IS		RG_CSI_L1_T1AB_HSAMP_SCB	RG_CSI_L1_T1AB_HSAMP_SCA	RG_CSI_L1_T1AB_HSAMP_LPBK_TEST_EN	RG_CSI_L1_T1AB_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_XX_ToBC_HSAMP_SRB				RG_CSI_XX_ToBC_HSAMP_SRA				RG_CSI_XX_ToBC_HSAMP_BW		RG_CSI_XX_ToBC_HSAMP_IS		RG_CSI_XX_ToBC_HSAMP_SCB	RG_CSI_XX_ToBC_HSAMP_SCA	RG_CSI_XX_ToBC_HSAMP_LPBK_TEST_EN	RG_CSI_XX_ToBC_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	RG_CSI_L1_T1AB_HSAMP_SRB	
27:24	RG_CSI_L1_T1AB_HSAMP_SRA	
23:22	RG_CSI_L1_T1AB_HSAMP_BW	
21:20	RG_CSI_L1_T1AB_HSAMP_IS	
19	RG_CSI_L1_T1AB_HSAMP_SCB	
18	RG_CSI_L1_T1AB_HSAMP_SCA	
17	RG_CSI_L1_T1AB_HSAMP_LPBK_TEST_EN	
16	RG_CSI_L1_T1AB_HSAMP_MON_EN	
15:12	RG_CSI_XX_ToBC_HSAMP_SRB	
11:8	RG_CSI_XX_ToBC_HSAMP_SRA	
7:6	RG_CSI_XX_ToBC_HSAMP_BW	
5:4	RG_CSI_XX_ToBC_HSAMP_IS	
3	RG_CSI_XX_ToBC_HSAMP_SCB	
2	RG_CSI_XX_ToBC_HSAMP_SCA	
1	RG_CSI_XX_ToBC_HSAMP_LPBK	

Bit(s)	Name	Description
0	_TEST_EN RG_CSI_XX_ToBC_HSAMP_MON_ EN	

10217620 MIPI_RX_AN A20_CSI1B HS AMP Control 88008800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_L2_T1BC_HSAMP_SRB				RG_CSI_L2_T1BC_HSAMP_SRA				RG_CSI_L2_T1BC_HSAMP_BW		RG_CSI_L2_T1BC_HSAMP_IS		RG_CSI_L2_T1BC_HSAMP_SCB	RG_CSI_L2_T1BC_HSAMP_SCA	RG_CSI_L2_T1BC_HSAMP_LPBK_TEST_EN	RG_CSI_L2_T1BC_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_XX_T1CA_HSAMP_SRB				RG_CSI_XX_T1CA_HSAMP_SRA				RG_CSI_XX_T1CA_HSAMP_BW		RG_CSI_XX_T1CA_HSAMP_IS		RG_CSI_XX_T1CA_HSAMP_SCB	RG_CSI_XX_T1CA_HSAMP_SCA	RG_CSI_XX_T1CA_HSAMP_LPBK_TEST_EN	RG_CSI_XX_T1CA_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	RG_CSI_L2_T1BC_HSAMP_SRB	
27:24	RG_CSI_L2_T1BC_HSAMP_SRA	
23:22	RG_CSI_L2_T1BC_HSAMP_BW	
21:20	RG_CSI_L2_T1BC_HSAMP_IS	
19	RG_CSI_L2_T1BC_HSAMP_SCB	
18	RG_CSI_L2_T1BC_HSAMP_SCA	
17	RG_CSI_L2_T1BC_HSAMP_LPBK_TEST_EN	
16	RG_CSI_L2_T1BC_HSAMP_MON_EN	
15:12	RG_CSI_XX_T1CA_HSAMP_SRB	
11:8	RG_CSI_XX_T1CA_HSAMP_SRA	
7:6	RG_CSI_XX_T1CA_HSAMP_BW	
5:4	RG_CSI_XX_T1CA_HSAMP_IS	
3	RG_CSI_XX_T1CA_HSAMP_SCB	
2	RG_CSI_XX_T1CA_HSAMP_SCA	
1	RG_CSI_XX_T1CA_HSAMP_LPBK_TEST_EN	
0	RG_CSI_XX_T1CA_HSAMP_MON_EN	

10217624 MIPI_RX_AN A24_CSI1B DPHY Deserializer Control 0F000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RG_CSI_RESERVE											RG_CSI_DPHY_L2_SYNC_EDGE_SEL		RG_CSI_DPHY_L2_FORCE_SYNC		RG_CSI_DPHY_L2_BYPASS_BYTECK_INVERT
Type	RW											RW		RW		RW
Reset	0	0	0	0	1	1	1	1				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_DPHY_L2_BYTECK_INVERT		RG_CSI_DPHY_L1_SYNC_EDGE_SEL		RG_CSI_DPHY_L1_FORCE_SYNC		RG_CSI_DPHY_L1_BYPASS_BYTECK_INVERT	RG_CSI_DPHY_L1_BYTECK_INVERT			RG_CSI_DPHY_L0_SYNC_EDGE_SEL		RG_CSI_DPHY_L0_FORCE_SYNC		RG_CSI_DPHY_L0_BYPASS_BYTECK_INVERT	RG_CSI_DPHY_L0_BYTECK_INVERT
Type	RW		RW		RW		RW	RW			RW		RW		RW	RW
Reset	0		0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RG_CSI_RESERVE	
20:19	RG_CSI_DPHY_L2_SYNC_EDGE_SEL	
18:17	RG_CSI_DPHY_L2_FORCE_SYNC	
16	RG_CSI_DPHY_L2_BYPASS_BYTECK_INVERT	
15	RG_CSI_DPHY_L2_BYTECK_INVERT	
13:12	RG_CSI_DPHY_L1_SYNC_EDGE_SEL	
11:10	RG_CSI_DPHY_L1_FORCE_SYNC	
9	RG_CSI_DPHY_L1_BYPASS_BYTECK_INVERT	
8	RG_CSI_DPHY_L1_BYTECK_INVERT	
5:4	RG_CSI_DPHY_L0_SYNC_EDGE_SEL	
3:2	RG_CSI_DPHY_L0_FORCE_SYNC	
1	RG_CSI_DPHY_L0_BYPASS_BYTECK_INVERT	
0	RG_CSI_DPHY_L0_BYTECK_INVERT	

10217628 MIPI_RX_ANA28_CSI1B CPHY CDR Control 0000888F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CSI_CPHY_To_CDR_EARLY_CODE					RG_CSI_CPHY_To_CDR_INIT_CODE							RG_CSI_CPHY_To_CDR_MANUAL_EN
Type				RW					RW							RW

Reset				0	0	0	0	0	0	0	0	0	0			0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_To_CDR_CA_WIDTH				RG_CSI_CPHY_To_CDR_BC_WIDTH				RG_CSI_CPHY_To_CDR_AB_WIDTH				RG_CSI_CPHY_To_CDR_LPF_CTRL		RG_CSI_CPHY_To_CDR_AUTOLOAD_EN	RG_CSI_CPHY_To_CDR_DIRECT_EN
Type	RW				RW				RW				RW		RW	RW
Reset	1	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1

Bit(s)	Name	Description
28:24	RG_CSI_CPHY_To_CDR_EARLY_CODE	
23:19	RG_CSI_CPHY_To_CDR_INIT_CODE	
16	RG_CSI_CPHY_To_CDR_MANUAL_EN	
15:12	RG_CSI_CPHY_To_CDR_CA_WIDTH	Filter out coding jitter
11:8	RG_CSI_CPHY_To_CDR_BC_WIDTH	Filter out coding jitter
7:4	RG_CSI_CPHY_To_CDR_AB_WIDTH	Filter out coding jitter
3:2	RG_CSI_CPHY_To_CDR_LPF_CTRL	
1	RG_CSI_CPHY_To_CDR_AUTOLOAD_EN	
0	RG_CSI_CPHY_To_CDR_DIRECT_EN	Direct Sample Mode Enable

1021762C MIPI_RX_ANA2C_CSI1B **CPHY CDR Control** **00002000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI_CPHY_To_DEBUG_EN	RG_CSI_CPHY_To_BIST_EN	RG_CSI_CPHY_To_BIST_AB											
Type			RW	RW	RW											
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_To_BIST_AB		RG_CSI_CPHY_To_HSDET_SEL					RG_CSI_CPHY_To_FORCE_INIT	RG_CSI_CPHY_To_SYNC_INIT_SEL	RG_CSI_CPHY_To_SYMCK_INVERT		RG_CSI_CPHY_To_CDR_LATE_CODE				
Type	RW		RW					RW	RW	RW		RW				
Reset	0	0	1	0				0	0	0		0	0	0	0	0

Bit(s)	Name	Description
29	RG_CSI_CPHY_To_DEBUG_EN	
28	RG_CSI_CPHY_To_BIST_EN	

Bit(s)	Name	Description
27:14	RG_CSI_CPHY_T0_BIST_AB	
13:12	RG_CSI_CPHY_T0_HSDET_SEL	
8	RG_CSI_CPHY_T0_FORCE_INIT	[NORMAL]1'b0: Self [NORMAL]1'b1: DA
7	RG_CSI_CPHY_T0_SYNC_INIT_SEL	[NORMAL]1'b0: Self [NORMAL]1'b1: DA
6	RG_CSI_CPHY_T0_SYMCK_INVERT	
4:0	RG_CSI_CPHY_T0_CDR_LATE_CODE	

10217630 MIPI_RX_AN A30_CSI1B CPHY CDR Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI_CPHY_T0_BIST_CA													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_T0_DEBUG_SEL		RG_CSI_CPHY_T0_BIST_BC													
Type	RW		RW													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	RG_CSI_CPHY_T0_BIST_CA	
15:14	RG_CSI_CPHY_T0_DEBUG_SEL	
13:0	RG_CSI_CPHY_T0_BIST_BC	

10217634 MIPI_RX_AN A34_CSI1B CPHY CDR Control 0000888F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CSI_CPHY_T1_CDR_EARLY_CODE					RG_CSI_CPHY_T1_CDR_INIT_CODE							RG_CSI_CPHY_T1_CDR_MANUAL_EN
Type				RW					RW							RW
Reset				0	0	0	0	0	0	0	0	0	0			0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_T1_CDR_CA_WIDTH			RG_CSI_CPHY_T1_CDR_BC_WIDTH					RG_CSI_CPHY_T1_CDR_AB_WIDTH				RG_CSI_CPHY_T1_CDR_LPF_CTRL		RG_CSI_CPHY_T1_CDR_AUTOLOAD_EN	RG_CSI_CPHY_T1_CDR_DIRECT_EN
Type	RW			RW					RW				RW		RW	RW
Reset	1	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1

Bit(s)	Name	Description
28:24	RG_CSI_CPHY_T1_CDR_EARLY_CODE	
23:19	RG_CSI_CPHY_T1_CDR_INIT_CODE	
16	RG_CSI_CPHY_T1_CDR_MANUAL_EN	
15:12	RG_CSI_CPHY_T1_CDR_CA_WIDTH	Filter out coding jitter
11:8	RG_CSI_CPHY_T1_CDR_BC_WIDTH	Filter out coding jitter
7:4	RG_CSI_CPHY_T1_CDR_AB_WIDTH	Filter out coding jitter
3:2	RG_CSI_CPHY_T1_CDR_LPF_CTRL	
1	RG_CSI_CPHY_T1_CDR_AUTOLOAD_EN	
0	RG_CSI_CPHY_T1_CDR_DIRECT_EN	Direct Sample Mode Enable

10217638 MIPI_RX_AN A38_CSI1B CPHY CDR Control 00002000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI_CPHY_T1_DEBUG_EN	RG_CSI_CPHY_T1_BIST_EN	RG_CSI_CPHY_T1_BIST_AB											
Type			RW	RW	RW											
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_T1_BIST_AB		RG_CSI_CPHY_T1_HSDET_SEL					RG_CSI_CPHY_T1_FORCE_INIT	RG_CSI_CPHY_T1_SYNC_INIT_SEL	RG_CSI_CPHY_T1_SYMCK_INVERT		RG_CSI_CPHY_T1_CDR_LATE_CODE				
Type	RW		RW					RW	RW	RW		RW				
Reset	0	0	1	0				0	0	0		0	0	0	0	0

Bit(s)	Name	Description
29	RG_CSI_CPHY_T1_DEBUG_EN	
28	RG_CSI_CPHY_T1_BIST_EN	
27:14	RG_CSI_CPHY_T1_BIST_AB	
13:12	RG_CSI_CPHY_T1_HSDET_SEL	
8	RG_CSI_CPHY_T1_FORCE_INIT	[NORMAL]1'b0: Self [NORMAL]1'b1: DA
7	RG_CSI_CPHY_T1_SYNC_INIT_SEL	[NORMAL]1'b0: Self [NORMAL]1'b1: DA
6	RG_CSI_CPHY_T1_SYMCK_INVERT	
4:0	RG_CSI_CPHY_T1_CDR_LATE_CODE	

1021763C MIPI_RX_ANA3C_CSI1B **CPHY CDR Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI_CPHY_T1_BIST_CA													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_T1_DEBUG_SEL		RG_CSI_CPHY_T1_BIST_BC													
Type	RW		RW													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	RG_CSI_CPHY_T1_BIST_CA	
15:14	RG_CSI_CPHY_T1_DEBUG_SEL	
13:0	RG_CSI_CPHY_T1_BIST_BC	

10217640 MIPI_RX_ANA40_CSI1B **GPI Control** **40404040**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_CSI_L1N_GPI_G	RG_CSI_L1N_GPI_RDSEL		RG_CSI_L1N_GPI_PD	RG_CSI_L1N_GPI_PU	RG_CSI_L1N_GPI_SMT	RG_CSI_L1N_GPI_IES		RG_CSI_L1P_GPI_G	RG_CSI_L1P_GPI_RDSEL		RG_CSI_L1P_GPI_PD	RG_CSI_L1P_GPI_PU	RG_CSI_L1P_GPI_SMT	RG_CSI_L1P_GPI_IES
Type		RW	RW		RW	RW	RW	RW		RW	RW		RW	RW	RW	RW
Reset		1	0	0	0	0	0	0		1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI_LoN_GPI_G	RG_CSI_LoN_GPI_RDSEL		RG_CSI_LoN_GPI_PD	RG_CSI_LoN_GPI_PU	RG_CSI_LoN_GPI_SMT	RG_CSI_LoN_GPI_IES		RG_CSI_LoP_GPI_G	RG_CSI_LoP_GPI_RDSEL		RG_CSI_LoP_GPI_PD	RG_CSI_LoP_GPI_PU	RG_CSI_LoP_GPI_SMT	RG_CSI_LoP_GPI_IES
Type		RW	RW		RW	RW	RW	RW		RW	RW		RW	RW	RW	RW
Reset		1	0	0	0	0	0	0		1	0	0	0	0	0	0

Bit(s)	Name	Description
30	RG_CSI_L1N_GPI_G	**RX Input Control Gating**
29:28	RG_CSI_L1N_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
27	RG_CSI_L1N_GPI_PD	**75K pull-down resistor control. High activiate.**
26	RG_CSI_L1N_GPI_PU	**75K pull-up resistor control. High activiate.**
25	RG_CSI_L1N_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
24	RG_CSI_L1N_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO

Bit(s)	Name	Description
		power domain.
22	RG_CSI_L1P_GPI_G	**RX Input Control Gating**
21:20	RG_CSI_L1P_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
19	RG_CSI_L1P_GPI_PD	**75K pull-down resistor control. High activiate.**
18	RG_CSI_L1P_GPI_PU	**75K pull-up resistor control. High activiate.**
17	RG_CSI_L1P_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
16	RG_CSI_L1P_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.
14	RG_CSI_L0N_GPI_G	**RX Input Control Gating**
13:12	RG_CSI_L0N_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
11	RG_CSI_L0N_GPI_PD	**75K pull-down resistor control. High activiate.**
10	RG_CSI_L0N_GPI_PU	**75K pull-up resistor control. High activiate.**
9	RG_CSI_L0N_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
8	RG_CSI_L0N_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.
6	RG_CSI_L0P_GPI_G	**RX Input Control Gating**
5:4	RG_CSI_L0P_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
3	RG_CSI_L0P_GPI_PD	**75K pull-down resistor control. High activiate.**
2	RG_CSI_L0P_GPI_PU	**75K pull-up resistor control. High activiate.**
1	RG_CSI_L0P_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
0	RG_CSI_L0P_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.

10217644 MIPI_RX_ANA44_CSI1B GPI Control 00004040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI_L2N_GPI_G	RG_CSI_L2N_GPI_RDSEL		RG_CSI_L2N_GPI_PD	RG_CSI_L2N_GPI_PU	RG_CSI_L2N_GPI_SMT	RG_CSI_L2N_GPI_IES		RG_CSI_L2P_GPI_G	RG_CSI_L2P_GPI_RDSEL		RG_CSI_L2P_GPI_PD	RG_CSI_L2P_GPI_PU	RG_CSI_L2P_GPI_SMT	RG_CSI_L2P_GPI_IES
Type		RW	RW		RW	RW	RW	RW		RW	RW		RW	RW	RW	RW
Reset		1	0	0	0	0	0	0		1	0	0	0	0	0	0

Bit(s)	Name	Description
14	RG_CSI_L2N_GPI_G	**RX Input Control Gating**
13:12	RG_CSI_L2N_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
11	RG_CSI_L2N_GPI_PD	**75K pull-down resistor control. High activiate.**
10	RG_CSI_L2N_GPI_PU	**75K pull-up resistor control. High activiate.**
9	RG_CSI_L2N_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
8	RG_CSI_L2N_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.
6	RG_CSI_L2P_GPI_G	**RX Input Control Gating**
5:4	RG_CSI_L2P_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
3	RG_CSI_L2P_GPI_PD	**75K pull-down resistor control. High activiate.**
2	RG_CSI_L2P_GPI_PU	**75K pull-up resistor control. High activiate.**
1	RG_CSI_L2P_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
0	RG_CSI_L2P_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.

10217648 MIPI_RX_ANA48_CSI1B RGS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AD_CSI_CPHY_T1_DEBUG_OUT	AD_CSI_CPHY_T1_BIST_CHECK_OUT	AD_CSI_CPHY_To_DEBUG_OUT	AD_CSI_CPHY_To_BIST_CHECK_OUT	AD_CSI_L2N_GPI_OUT	AD_CSI_L2P_GPI_OUT	AD_CSI_L1N_GPI_OUT	AD_CSI_L1P_GPI_OUT	AD_CSI_L0N_GPI_OUT	AD_CSI_L0P_GPI_OUT
Type							RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RGS_CSI_CPHY_T1_CDR_CODE								RGS_CSI_CPHY_To_CDR_CODE				
Type				RU								RU				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
25	AD_CSI_CPHY_T1_DEBUG_OUT	
24	AD_CSI_CPHY_T1_BIST_CHECK_OUT	
23	AD_CSI_CPHY_To_DEBUG_OUT	
22	AD_CSI_CPHY_To_BIST_CHECK_OUT	
21	AD_CSI_L2N_GPI_OUT	
20	AD_CSI_L2P_GPI_OUT	
19	AD_CSI_L1N_GPI_OUT	
18	AD_CSI_L1P_GPI_OUT	
17	AD_CSI_L0N_GPI_OUT	
16	AD_CSI_L0P_GPI_OUT	
12:8	RGS_CSI_CPHY_T1_CDR_CODE	
4:0	RGS_CSI_CPHY_To_CDR_CODE	

1021764C MIPI_RX_AN A4C_CSI1B DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DA_CSI_CDPHY_L2N_T1C_HSRT_EN	DA_CSI_CDPHY_L2P_T1B_HSRT_EN	DA_CSI_CDPHY_L1N_T1A_HSRT_EN	DA_CSI_CDPHY_L1P_T0C_HSRT_EN	DA_CSI_CDPHY_L0N_T0B_HSRT_EN	DA_CSI_CDPHY_L0P_T0A_HSRT_EN	AD_CSI_DPHY_L2N_HSDET_OUT	DA_CSI_DPHY_L2N_HSDET_RSTB	AD_CSI_DPHY_L2P_HSDET_OUT	DA_CSI_DPHY_L2P_HSDET_RSTB	AD_CSI_DPHY_L1N_HSDET_OUT	DA_CSI_DPHY_L1N_HSDET_RSTB	AD_CSI_DPHY_L1P_HSDET_OUT	DA_CSI_DPHY_L1P_HSDET_RSTB
Type			RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AD_CSI_DPHY_L0N_HSDET_OUT	DA_CSI_DPHY_L0N_HSDET_RSTB	AD_CSI_DPHY_L0P_HSDET_OUT	DA_CSI_DPHY_L0P_HSDET_RSTB	AD_CSI_CDPHY_L2N_T1C_LPRX_OUT	DA_CSI_CDPHY_L2N_T1C_LPRX_EN	AD_CSI_CDPHY_L2P_T1B_LPRX_OUT	DA_CSI_CDPHY_L2P_T1B_LPRX_EN	AD_CSI_CDPHY_L1N_T1A_LPRX_OUT	DA_CSI_CDPHY_L1N_T1A_LPRX_EN	AD_CSI_CDPHY_L1P_T0C_LPRX_OUT	DA_CSI_CDPHY_L1P_T0C_LPRX_EN	AD_CSI_CDPHY_L0N_T0B_LPRX_OUT	DA_CSI_CDPHY_L0N_T0B_LPRX_EN	AD_CSI_CDPHY_L0P_T0A_LPRX_OUT	DA_CSI_CDPHY_L0P_T0A_LPRX_EN
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
29	DA_CSI_CDPHY_L2N_T1C_HSRT_EN	
28	DA_CSI_CDPHY_L2P_T1B_HSRT_EN	
27	DA_CSI_CDPHY_L1N_T1A_HSRT_EN	
26	DA_CSI_CDPHY_L1P_T0C_HSRT_EN	
25	DA_CSI_CDPHY_L0N_T0B_HSRT_EN	
24	DA_CSI_CDPHY_L0P_T0A_HSRT_EN	
23	AD_CSI_DPHY_L2N_HSDET_OUT	
22	DA_CSI_DPHY_L2N_HSDET_RSTB	
21	AD_CSI_DPHY_L2P_HSDET_OUT	
20	DA_CSI_DPHY_L2P_HSDET_RSTB	
19	AD_CSI_DPHY_L1N_HSDET_OUT	
18	DA_CSI_DPHY_L1N_HSDET_RSTB	
17	AD_CSI_DPHY_L1P_HSDET_OUT	
16	DA_CSI_DPHY_L1P_HSDET_RSTB	
15	AD_CSI_DPHY_L0N_HSDET_OUT	
14	DA_CSI_DPHY_L0N_HSDET_RSTB	
13	AD_CSI_DPHY_L0P_HSDET_OUT	
12	DA_CSI_DPHY_L0P_HSDET_RSTB	
11	AD_CSI_CDPHY_L2N_T1C_LPRX_OUT	
10	DA_CSI_CDPHY_L2N_T1C_LPRX_EN	
9	AD_CSI_CDPHY_L2P_T1B_LPRX_OUT	
8	DA_CSI_CDPHY_L2P_T1B_LPRX_EN	
7	AD_CSI_CDPHY_L1N_T1A_LPRX_OUT	
6	DA_CSI_CDPHY_L1N_T1A_LPRX_EN	
5	AD_CSI_CDPHY_L1P_T0C_LPRX_OUT	
4	DA_CSI_CDPHY_L1P_T0C_LPRX_EN	
3	AD_CSI_CDPHY_L0N_T0B_LPRX_OUT	
2	DA_CSI_CDPHY_L0N_T0B_LPRX_EN	
1	AD_CSI_CDPHY_L0P_T0A_LPRX_OUT	
0	DA_CSI_CDPHY_L0P_T0A_LPRX_EN	

10217650 MIPI_RX_ANA50_CSI1B **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name							AD_CSI_CPHY_ToCA_HSAMP_OS_CK	AD_CSI_CPHY_ToCA_HSAMP_OS_OUT	DA_CSI_CPHY_ToCA_HSAMP_OS_CODE					DA_CSI_CPHY_ToCA_HSAMP_OS_CAL_EN	DA_CSI_CPHY_ToCA_HSAMP_OS_APPLY	DA_CSI_CPHY_ToCA_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							AD_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CK	AD_CSI_CDPHY_Lo_ToAB_HSAMP_OS_OUT	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CODE					DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CAL_EN	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_APPLY	DA_CSI_CDPHY_Lo_ToAB_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25	AD_CSI_CPHY_ToCA_HSAMP_OS_CK	
24	AD_CSI_CPHY_ToCA_HSAMP_OS_OUT	
23:19	DA_CSI_CPHY_ToCA_HSAMP_OS_CODE	
18	DA_CSI_CPHY_ToCA_HSAMP_OS_CAL_EN	
17	DA_CSI_CPHY_ToCA_HSAMP_OS_APPLY	
16	DA_CSI_CPHY_ToCA_HSAMP_EN	
9	AD_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CK	
8	AD_CSI_CDPHY_Lo_ToAB_HSAMP_OS_OUT	
7:3	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CODE	
2	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CAL_EN	
1	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_APPLY	
0	DA_CSI_CDPHY_Lo_ToAB_HSAMP_EN	

10217654 MIPI_RX_AN A54_CSI1B **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AD_CSI_CDPHY_L1_T1AB_HSAMP_OS_CK	AD_CSI_CDPHY_L1_T1AB_HSAMP_OS_OUT	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_CODE					DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_CAL_EN	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_APPLY	DA_CSI_CDPHY_L1_T1AB_HSAMP_EN

Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							AD_CSI_CPHY_ToBC_HSAMP_OS_CK	AD_CSI_CPHY_ToBC_HSAMP_OS_OUT	DA_CSI_CPHY_ToBC_HSAMP_OS_CODE					DA_CSI_CPHY_ToBC_HSAMP_OS_CAL_EN	DA_CSI_CPHY_ToBC_HSAMP_OS_APPLY	DA_CSI_CPHY_ToBC_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25	AD_CSI_CDPHY_L1_T1AB_HSAMP_OS_CK	
24	AD_CSI_CDPHY_L1_T1AB_HSAMP_OS_OUT	
23:19	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_CODE	
18	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_CAL_EN	
17	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_APPLY	
16	DA_CSI_CDPHY_L1_T1AB_HSAMP_EN	
9	AD_CSI_CPHY_ToBC_HSAMP_OS_CK	
8	AD_CSI_CPHY_ToBC_HSAMP_OS_OUT	
7:3	DA_CSI_CPHY_ToBC_HSAMP_OS_CODE	
2	DA_CSI_CPHY_ToBC_HSAMP_OS_CAL_EN	
1	DA_CSI_CPHY_ToBC_HSAMP_OS_APPLY	
0	DA_CSI_CPHY_ToBC_HSAMP_EN	

10217658 MIPI_RX_ANA58_CSI1B **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AD_CSI_CDPHY_L2_T1BC_HSAMP_OS_CK	AD_CSI_CDPHY_L2_T1BC_HSAMP_OS_OUT	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_CODE					DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_CAL_EN	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_APPLY	DA_CSI_CDPHY_L2_T1BC_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							AD_CSI_CPHY_T1CA_HSA	AD_CSI_CPHY_T1CA_HSA	DA_CSI_CPHY_T1CA_HSAMP_OS_CODE					DA_CSI_CPHY_T1CA_HSA	DA_CSI_CPHY_T1CA_HSA	DA_CSI_CPHY_T1CA_HSA

							MP_OS_CK	MP_OS_OUT						MP_OS_CAL_EN	MP_OS_APPLY	MP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25	AD_CSI_CDPHY_L2_T1BC_HSAMP_OS_CK	
24	AD_CSI_CDPHY_L2_T1BC_HSAMP_OS_OUT	
23:19	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_CODE	
18	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_CAL_EN	
17	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_APPLY	
16	DA_CSI_CDPHY_L2_T1BC_HSAMP_EN	
9	AD_CSI_CPHY_T1CA_HSAMP_OS_CK	
8	AD_CSI_CPHY_T1CA_HSAMP_OS_OUT	
7:3	DA_CSI_CPHY_T1CA_HSAMP_OS_CODE	
2	DA_CSI_CPHY_T1CA_HSAMP_OS_CAL_EN	
1	DA_CSI_CPHY_T1CA_HSAMP_OS_APPLY	
0	DA_CSI_CPHY_T1CA_HSAMP_EN	

1021765C MIPI_RX_ANA5C_CSI1B **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSI_DPHY_Lo_DELAY_CODE							AD_CSI_DPHY_Lo_BYPASS_BYTE_DATA							
Type		RU							RU							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_DPHY_Lo_DELAY_APPLY	DA_CSI_DPHY_Lo_DELAY_EN	AD_CSI_DPHY_Lo_BYPASS_BYTE_CK	AD_CSI_DPHY_Lo_SYNC_DETECT	AD_CSI_DPHY_Lo_BYTE_DATA								AD_CSI_DPHY_Lo_BYTE_CK	DA_CSI_DPHY_Lo_DES_SYNC_INIT	DA_CSI_DPHY_Lo_DES_EN	DA_CSI_DPHY_Lo_SAMP_EN
Type	RU	RU	RU	RU	RU								RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	DA_CSI_DPHY_Lo_DELAY_CODE	
23:16	AD_CSI_DPHY_Lo_BYPASS_BYTE_DATA	
15	DA_CSI_DPHY_Lo_DELAY_APPLY	
14	DA_CSI_DPHY_Lo_DELAY_EN	
13	AD_CSI_DPHY_Lo_BYPASS_BYT	

Bit(s)	Name	Description
	E_CK	
12	AD_CSI_DPHY_L0_SYNC_DETECT	
11:4	AD_CSI_DPHY_L0_BYTE_DATA	
3	AD_CSI_DPHY_L0_BYTE_CK	
2	DA_CSI_DPHY_L0_DES_SYNC_INIT	
1	DA_CSI_DPHY_L0_DES_EN	
0	DA_CSI_DPHY_L0_SAMP_EN	

10217660 MIPI_RX_AN A60_CSI1B **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSI_DPHY_L1_DELAY_CODE							AD_CSI_DPHY_L1_BYPASS_BYTE_DATA							
Type		RU							RU							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_DPHY_L1_DELAY_APPLY	DA_CSI_DPHY_L1_DELAY_EN	AD_CSI_DPHY_L1_BYPASS_BYTE_CK	AD_CSI_DPHY_L1_SYNC_DETECT	AD_CSI_DPHY_L1_BYTE_DATA								AD_CSI_DPHY_L1_BYTE_CK	DA_CSI_DPHY_L1_DES_SYNC_INIT	DA_CSI_DPHY_L1_DES_EN	DA_CSI_DPHY_L1_SAMP_EN
Type	RU	RU	RU	RU	RU								RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	DA_CSI_DPHY_L1_DELAY_CODE	
23:16	AD_CSI_DPHY_L1_BYPASS_BYTE_DATA	
15	DA_CSI_DPHY_L1_DELAY_APPLY	
14	DA_CSI_DPHY_L1_DELAY_EN	
13	AD_CSI_DPHY_L1_BYPASS_BYTE_CK	
12	AD_CSI_DPHY_L1_SYNC_DETECT	
11:4	AD_CSI_DPHY_L1_BYTE_DATA	
3	AD_CSI_DPHY_L1_BYTE_CK	
2	DA_CSI_DPHY_L1_DES_SYNC_INIT	
1	DA_CSI_DPHY_L1_DES_EN	
0	DA_CSI_DPHY_L1_SAMP_EN	

10217664 MIPI_RX_AN A64_CSI1B **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSI_DPHY_L2_DELAY_CODE							AD_CSI_DPHY_L2_BYPASS_BYTE_DATA							
Type		RU							RU							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	DA_CSI_DPHY_L2_DELAY_APPLY	DA_CSI_DPHY_L2_DELAY_EN	AD_CSI_DPHY_L2_BYPASS_BYTE_CK	AD_CSI_DPHY_L2_SYNC_DETECT	AD_CSI_DPHY_L2_BYTE_DATA								AD_CSI_DPHY_L2_BYTE_CK	DA_CSI_DPHY_L2_DES_SYNC_INIT	DA_CSI_DPHY_L2_DES_EN	DA_CSI_DPHY_L2_SAMP_EN
Type	RU	RU	RU	RU	RU								RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	DA_CSI_DPHY_L2_DELAY_CODE	
23:16	AD_CSI_DPHY_L2_BYPASS_BYTE_DATA	
15	DA_CSI_DPHY_L2_DELAY_APPLY	
14	DA_CSI_DPHY_L2_DELAY_EN	
13	AD_CSI_DPHY_L2_BYPASS_BYTE_CK	
12	AD_CSI_DPHY_L2_SYNC_DETECT	
11:4	AD_CSI_DPHY_L2_BYTE_DATA	
3	AD_CSI_DPHY_L2_BYTE_CK	
2	DA_CSI_DPHY_L2_DES_SYNC_INIT	
1	DA_CSI_DPHY_L2_DES_EN	
0	DA_CSI_DPHY_L2_SAMP_EN	

10217668 MIPI_RX_ANA68_CSI1B **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AD_CSI_CPHY_To_HSDET_OUT	DA_CSI_CPHY_To_SYNC_INIT
Type															RU	RU
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_CPHY_To_DES_EN	DA_CSI_CPHY_To_CDR_EN	AD_CSI_CPHY_To_AB													
Type	RU	RU	RU													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	AD_CSI_CPHY_To_HSDET_OUT	
16	DA_CSI_CPHY_To_SYNC_INIT	
15	DA_CSI_CPHY_To_DES_EN	
14	DA_CSI_CPHY_To_CDR_EN	
13:0	AD_CSI_CPHY_To_AB	

1021766C MIPI_RX_ANA6C_CSI1B DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AD_CSI_CPHY_To_BC													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	AD_CSI_CPHY_To_BC	

10217670 MIPI_RX_ANA70_CSI1B DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AD_CSI_CPHY_To_CA													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	AD_CSI_CPHY_To_CA	

10217674 MIPI_RX_ANA74_CSI1B DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AD_CSI_CPHY_T1_HSDET_OUT	DA_CSI_CPHY_T1_SYNC_INIT
Type															RU	RU
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_CPHY_T1_DES_EN	DA_CSI_CPHY_T1_CDR_EN	AD_CSI_CPHY_T1_AB													
Type	RU	RU	RU													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
17	AD_CSI_CPHY_T1_HSDET_OUT	
16	DA_CSI_CPHY_T1_SYNC_INIT	
15	DA_CSI_CPHY_T1_DES_EN	
14	DA_CSI_CPHY_T1_CDR_EN	
13:0	AD_CSI_CPHY_T1_AB	

10217678 MIPI_RX_ANA78_CSI1B DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AD_CSI_CPHY_T1_BC													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	AD_CSI_CPHY_T1_BC	

1021767C MIPI_RX_ANA7C_CSI1B DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AD_CSI_CPHY_T1_CA													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	AD_CSI_CPHY_T1_CA	

10217680 MIPI_RX_WRAPPER80_CSI1B WRAPPER 04000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CSR_CSIo_DPHY_MUX			CSR_SW_RST				CSR_CSI1_CPHY_RST_MODE		CSR_CSI1_DPHY_RST_MODE		CSR_CSIo_CPHY_RST_MODE		CSR_CSIo_DPHY_RST_MODE	
Type		RW			RW				RW		RW		RW		RW	
Reset		0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_CSI_MON_MUX								CSR_CSI_MODE				CSR_CSI1_DPHY_MUX		CSR_HSDET_MO	CSR_CSI_CLK_

															DE	MON
Type	RW								RW				RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:28	CSR_CSI0_DPHY_MUX	
27:24	CSR_SW_RST	
23:22	CSR_CSI1_CPHY_RST_MODE	0: sync init 1: hsrx_en 2: sw rst 3: hw rst
21:20	CSR_CSI1_DPHY_RST_MODE	0: sync init 1: hsrx_en 2: sw rst 3: hw rst
19:18	CSR_CSI0_CPHY_RST_MODE	0: sync init 1: hsrx_en 2: sw rst 3: hw rst
17:16	CSR_CSI0_DPHY_RST_MODE	0: sync init 1: hsrx_en 2: sw rst 3: hw rst
15:8	CSR_CSI_MON_MUX	
7:4	CSR_CSI_MODE	0:4 lane 1:2/2l lane 2:cphy 4:cphy/2 lane
3:2	CSR_CSI1_DPHY_MUX	
1	CSR_HSDET_MODE	0:dn 1:dp
0	CSR_CSI_CLK_MON	Enable Clock monitor

10217684 MIPI_RX_WRAPPER84_CSI1B WRAPPER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI_DEBUG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI_DEBUG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSI_DEBUG_OUT	

10217688 MIPI_RX_WRAPPER88_CSI1B WRAPPER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_MODE_0															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_MODE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_MODE_0	

1021768C MIPI_RX_WRAPPER8C_CSI1B **WRAPPER** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_MODE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_MODE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_MODE_1	

10217690 MIPI_RX_WRAPPER90_CSI1B **WRAPPER** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_MODE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_MODE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_MODE_2	

10217694 MIPI_RX_WRAPPER94_CSI1B **WRAPPER** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_VALUE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_VALUE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_VALUE_0	

10217698 MIPI_RX_WRAPPER98_CSI1B **WRAPPER** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_VALUE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_VALUE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_VALUE_1	

1021769C MIPI_RX_WRAPPER9C_CSI1B **WRAPPER** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_VALUE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_VALUE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_VALUE_2	

10217800 MIPI_RX_ANA00_CSI2 **2D1C Global Control** **00000492**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_CSI_DPHY_	RG_CSI_DPHY_	RG_CSI_DPHY_	RG_CSI_DPHY_	RG_CSI_DPHY_	RG_CSI_DPHY_	RG_CSI_DPHY_	RG_CSI_DPHY_	RG_CSI_DPHY_	RG_CSI_BG_CO	RG_CSI_BG_LP	RG_CSI_HSAMP	RG_CSI_CPHY_

				L2_CKSEL	L2_CKMODE_EN	L2_BYPASS_SYNC	L1_CKSEL	L1_CKMODE_EN	L1_BYPASS_SYNC	L0_CKSEL	L0_CKMODE_EN	L0_BYPASS_SYNC	RE_EN	F_EN	_PROTECT_EN	EN
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	1	0	0	1	0	0	1	0	0	1	0

Bit(s)	Name	Description
12	RG_CSI_DPHY_L2_CKSEL	**Data Mode** [NORMAL]1'b0: Sample data by Local Clock [NORMAL]1'b1: Sample data by Common Clock CK Mode [NORMAL]1'b0: Connect to Local Clock [NORMAL]1'b1: Connect to Common Clock
11	RG_CSI_DPHY_L2_CKMODE_EN	**[NORMAL]1'b0: Data Mode** [NORMAL]1'b1: CK Mode
10	RG_CSI_DPHY_L2_BYPASS_SYNC	**Bypass or Sync Mode Selection** [NORMAL]1'b0: Sync Mode [NORMAL]1'b1: Bypass Mode
9	RG_CSI_DPHY_L1_CKSEL	**Data Mode** [NORMAL]1'b0: Sample data by Local Clock [NORMAL]1'b1: Sample data by Common Clock CK Mode [NORMAL]1'b0: Connect to Local Clock [NORMAL]1'b1: Connect to Common Clock
8	RG_CSI_DPHY_L1_CKMODE_EN	**[NORMAL]1'b0: Data Mode** [NORMAL]1'b1: CK Mode
7	RG_CSI_DPHY_L1_BYPASS_SYNC	**Bypass or Sync Mode Selection** [NORMAL]1'b0: Sync Mode [NORMAL]1'b1: Bypass Mode
6	RG_CSI_DPHY_L0_CKSEL	**Data Mode** [NORMAL]1'b0: Sample data by Local Clock [NORMAL]1'b1: Sample data by Common Clock CK Mode [NORMAL]1'b0: Connect to Local Clock [NORMAL]1'b1: Connect to Common Clock
5	RG_CSI_DPHY_L0_CKMODE_EN	**[NORMAL]1'b0: Data Mode** [NORMAL]1'b1: CK Mode
4	RG_CSI_DPHY_L0_BYPASS_SYNC	**Bypass or Sync Mode Selection** [NORMAL]1'b0: Sync Mode [NORMAL]1'b1: Bypass Mode
3	RG_CSI_BG_CORE_EN	**[NORMAL]1'b0: Bandgap Disable** [NORMAL]1'b1: Bandgap Enable
2	RG_CSI_BG_LPF_EN	**[NORMAL]1'b0: Bandgap low pass filter Disable** [NORMAL]1'b1: Bandgap low pass filter Enable
1	RG_CSI_HSAMP_PROTECT_EN	**HSAMP Protection** [NORMAL]1'b0: Disable [NORMAL]1'b1: Enable
0	RG_CSI_CPHY_EN	**1'b0: DPHY Mode** 1'b1: CPHY Mode

10217804 MIPI_RX_AN A04_CSI2 2D1C Global Control 00084444

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CSI_FORCE_HSRT_EN	RG_CSI_BG_VREF_SEL								RG_CSI_BG_VREF_SEL			

Type				RW	RW								RW			
Reset				0	0	0	0	0					1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI_BG_HSDET_VTL_SEL				RG_CSI_BG_HSDET_VTH_SEL				RG_CSI_BG_LPRX_VTL_SEL				RG_CSI_BG_LPRX_VTH_SEL		
Type		RW				RW				RW				RW		
Reset		1	0	0		1	0	0		1	0	0		1	0	0

Bit(s)	Name	Description
28	RG_CSI_FORCE_HSRT_EN	**Force HSRT Enable to do FT calibration and eFuse**
27:24	RG_CSI_BG_MON_VREF_SEL	**Monitor Selection**
19:16	RG_CSI_BG_VREF_SEL	**HSAMP LDO Reference Voltage** Default 0.9V
14:12	RG_CSI_BG_HSDET_VTL_SEL	**HSDET VTH Selection** Default 0.12V
10:8	RG_CSI_BG_HSDET_VTH_SEL	**HSDET VTH Selection** Default 0.15V
6:4	RG_CSI_BG_LPRX_VTL_SEL	**LPRX VTL Selection** Default 0.70V
2:0	RG_CSI_BG_LPRX_VTH_SEL	**LPRX VTH Selection** Default 0.75V

10217808 MIPI_RX_AN_A08_CSI2 High Speed Termination Control 10101010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CSI_L1N_T1A_HSRT_CODE								RG_CSI_L1P_T0C_HSRT_CODE				
Type				RW								RW				
Reset				1	0	0	0	0				1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_CSI_L0N_T0B_HSRT_CODE								RG_CSI_L0P_T0A_HSRT_CODE				
Type				RW								RW				
Reset				1	0	0	0	0				1	0	0	0	0

Bit(s)	Name	Description
28:24	RG_CSI_L1N_T1A_HSRT_CODE	**Termination code** 800ohm/(8+N) Requires Calibration & Efuse on FT
20:16	RG_CSI_L1P_T0C_HSRT_CODE	**Termination code** 800ohm/(8+N) Requires Calibration & Efuse on FT
12:8	RG_CSI_L0N_T0B_HSRT_CODE	**Termination code** 800ohm/(8+N) Requires Calibration & Efuse on FT
4:0	RG_CSI_L0P_T0A_HSRT_CODE	**Termination code** 800ohm/(8+N) Requires Calibration & Efuse on FT

1021780C MIPI_RX_AN_A0C_CSI2 High Speed Termination Control 00001010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_CSI_L2 N_T1C_HSRT_CODE								RG_CSI_L2P_T1B_HSRT_CODE				
Type				RW								RW				
Reset				1	0	0	0	0				1	0	0	0	0

Bit(s)	Name	Description
12:8	RG_CSI_L2N_T1C_HSRT_CODE	**Termination code** 800ohm/(8+N) Requires Calibration & Efuse on FT
4:0	RG_CSI_L2P_T1B_HSRT_CODE	**Termination code** 800ohm/(8+N) Requires Calibration & Efuse on FT

10217810 MIPI_RX_AN_A10_CSI2 Bandgap Voltage for Delay Line Calibration 80808080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_CPHY_To_VREF_SEL						RG_CSI_CPHY_To_CDR_DELAYCAL_RSTB	RG_CSI_CPHY_To_CDR_DELAYCAL_EN	RG_CSI_DPHY_L2_VREF_SEL						RG_CSI_DPHY_L2_DELAYCAL_RSTB	RG_CSI_DPHY_L2_DELAYCAL_EN
Type	RW						RW	RW	RW						RW	RW
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_DPHY_L1_VREF_SEL						RG_CSI_DPHY_L1_DELAYCAL_RSTB	RG_CSI_DPHY_L1_DELAYCAL_EN	RG_CSI_DPHY_Lo_VREF_SEL						RG_CSI_DPHY_Lo_DELAYCAL_RSTB	RG_CSI_DPHY_Lo_DELAYCAL_EN
Type	RW						RW	RW	RW						RW	RW
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:26	RG_CSI_CPHY_To_VREF_SEL	**Do Delay Line Reference Voltage** Requires Software Calibration
25	RG_CSI_CPHY_To_CDR_DELAYCAL_RSTB	**TRIOo Delay Line Calibration Reset Bar**
24	RG_CSI_CPHY_To_CDR_DELAYCAL_EN	**TRIOo Delay Line Calibration Enable**
23:18	RG_CSI_DPHY_L2_VREF_SEL	**Do Delay Line Reference Voltage** Requires Software Calibration
17	RG_CSI_DPHY_L2_DELAYCAL_RSTB	**D1 Delay Line Calibration Reset Bar**
16	RG_CSI_DPHY_L2_DELAYCAL_EN	**D1 Delay Line Calibration Enable**
15:10	RG_CSI_DPHY_L1_VREF_SEL	**Do Delay Line Reference Voltage** Requires Software Calibration
9	RG_CSI_DPHY_L1_DELAYCAL_R	**CK Delay Line Calibration Reset Bar**

Bit(s)	Name	Description
	STB	
8	RG_CSI_DPHY_L1_DELAYCAL_EN	**CK Delay Line Calibration Enable**
7:2	RG_CSI_DPHY_L0_VREF_SEL	**D0 Delay Line Reference Voltage** Requires Software Calibration
1	RG_CSI_DPHY_L0_DELAYCAL_RSTB	**D0 Delay Line Calibration Reset Bar**
0	RG_CSI_DPHY_L0_DELAYCAL_EN	**D0 Delay Line Calibration Enable**

10217814 MIPI_RX_ANA14_CSI2 **Bandgap Voltage for Delay Line Calibration** **00000080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSI_CPHY_T1_VREF_SEL						RG_CSI_CPHY_T1_CDR_DELAYCAL_RSTB	RG_CSI_CPHY_T1_CDR_DELAYCAL_EN
Type									RW						RW	RW
Reset									1	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSI_CPHY_T1_VREF_SEL	**D0 Delay Line Reference Voltage** Requires Software Calibration
1	RG_CSI_CPHY_T1_CDR_DELAYCAL_RSTB	**TRIO1 Delay Line Calibration Reset Bar**
0	RG_CSI_CPHY_T1_CDR_DELAYCAL_EN	**TRIO1 Delay Line Calibration Enable**

10217818 MIPI_RX_ANA18_CSI2 **HS AMP Control** **88008800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_XX_ToCA_HSAMP_SRB				RG_CSI_XX_ToCA_HSAMP_SRA				RG_CSI_XX_ToCA_HSAMP_BW		RG_CSI_XX_ToCA_HSAMP_IS		RG_CSI_XX_ToCA_HSAMP_SCB	RG_CSI_XX_ToCA_HSAMP_SCA	RG_CSI_XX_ToCA_HSAMP_LPBK_TEST_EN	RG_CSI_XX_ToCA_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_Lo_ToAB_HSAMP_SRB				RG_CSI_Lo_ToAB_HSAMP_SRA				RG_CSI_Lo_ToAB_HSAMP_BW		RG_CSI_Lo_ToAB_HSA MP_IS		RG_CSI_Lo_ToAB_H	RG_CSI_Lo_ToAB_H	RG_CSI_Lo_ToAB_H	RG_CSI_Lo_ToAB_H

													SAMP_SCB	SAMP_SCA	SAMP_LPBK_TEST_EN	SAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	RG_CSI_XX_ToCA_HSAMP_SRB	
27:24	RG_CSI_XX_ToCA_HSAMP_SRA	
23:22	RG_CSI_XX_ToCA_HSAMP_BW	
21:20	RG_CSI_XX_ToCA_HSAMP_IS	
19	RG_CSI_XX_ToCA_HSAMP_SCB	
18	RG_CSI_XX_ToCA_HSAMP_SCA	
17	RG_CSI_XX_ToCA_HSAMP_LPBK_TEST_EN	
16	RG_CSI_XX_ToCA_HSAMP_MON_EN	
15:12	RG_CSI_Lo_ToAB_HSAMP_SRB	
11:8	RG_CSI_Lo_ToAB_HSAMP_SRA	
7:6	RG_CSI_Lo_ToAB_HSAMP_BW	
5:4	RG_CSI_Lo_ToAB_HSAMP_IS	
3	RG_CSI_Lo_ToAB_HSAMP_SCB	
2	RG_CSI_Lo_ToAB_HSAMP_SCA	
1	RG_CSI_Lo_ToAB_HSAMP_LPBK_TEST_EN	
0	RG_CSI_Lo_ToAB_HSAMP_MON_EN	

1021781C MIPI_RX_ANA1C_CSI2 HS AMP Control 88008800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_L1_T1AB_HSAMP_SRB				RG_CSI_L1_T1AB_HSAMP_SRA				RG_CSI_L1_T1AB_HSAMP_BW		RG_CSI_L1_T1AB_HSAMP_IS		RG_CSI_L1_T1AB_HSAMP_SCB	RG_CSI_L1_T1AB_HSAMP_SCA	RG_CSI_L1_T1AB_HSAMP_LPBK_TEST_EN	RG_CSI_L1_T1AB_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_XX_ToBC_HSAMP_SRB				RG_CSI_XX_ToBC_HSAMP_SRA				RG_CSI_XX_ToBC_HSAMP_BW		RG_CSI_XX_ToBC_HSAMP_IS		RG_CSI_XX_ToBC_HSAMP_SCB	RG_CSI_XX_ToBC_HSAMP_SCA	RG_CSI_XX_ToBC_HSAMP_LPBK_TEST_EN	RG_CSI_XX_ToBC_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	RG_CSI_L1_T1AB_HSAMP_SRB	

Bit(s)	Name	Description
27:24	RG_CSI_L1_T1AB_HSAMP_SRA	
23:22	RG_CSI_L1_T1AB_HSAMP_BW	
21:20	RG_CSI_L1_T1AB_HSAMP_IS	
19	RG_CSI_L1_T1AB_HSAMP_SCB	
18	RG_CSI_L1_T1AB_HSAMP_SCA	
17	RG_CSI_L1_T1AB_HSAMP_LPBK_TEST_EN	
16	RG_CSI_L1_T1AB_HSAMP_MON_EN	
15:12	RG_CSI_XX_T0BC_HSAMP_SRB	
11:8	RG_CSI_XX_T0BC_HSAMP_SRA	
7:6	RG_CSI_XX_T0BC_HSAMP_BW	
5:4	RG_CSI_XX_T0BC_HSAMP_IS	
3	RG_CSI_XX_T0BC_HSAMP_SCB	
2	RG_CSI_XX_T0BC_HSAMP_SCA	
1	RG_CSI_XX_T0BC_HSAMP_LPBK_TEST_EN	
0	RG_CSI_XX_T0BC_HSAMP_MON_EN	

10217820 MIPI_RX_AN A20_CSI2 HS AMP Control 88008800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_L2_T1BC_HSAMP_SRB				RG_CSI_L2_T1BC_HSAMP_SRA				RG_CSI_L2_T1BC_HSAMP_BW		RG_CSI_L2_T1BC_HSAMP_IS		RG_CSI_L2_T1BC_HSAMP_SCB	RG_CSI_L2_T1BC_HSAMP_SCA	RG_CSI_L2_T1BC_HSAMP_LPBK_TEST_EN	RG_CSI_L2_T1BC_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_XX_T1CA_HSAMP_SRB				RG_CSI_XX_T1CA_HSAMP_SRA				RG_CSI_XX_T1CA_HSAMP_BW		RG_CSI_XX_T1CA_HSAMP_IS		RG_CSI_XX_T1CA_HSAMP_SCB	RG_CSI_XX_T1CA_HSAMP_SCA	RG_CSI_XX_T1CA_HSAMP_LPBK_TEST_EN	RG_CSI_XX_T1CA_HSAMP_MON_EN
Type	RW				RW				RW		RW		RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	RG_CSI_L2_T1BC_HSAMP_SRB	
27:24	RG_CSI_L2_T1BC_HSAMP_SRA	
23:22	RG_CSI_L2_T1BC_HSAMP_BW	
21:20	RG_CSI_L2_T1BC_HSAMP_IS	
19	RG_CSI_L2_T1BC_HSAMP_SCB	
18	RG_CSI_L2_T1BC_HSAMP_SCA	
17	RG_CSI_L2_T1BC_HSAMP_LPBK_TEST_EN	
16	RG_CSI_L2_T1BC_HSAMP_MON_EN	

Bit(s)	Name	Description
15:12	RG_CSI_XX_T1CA_HSAMP_SRB	
11:8	RG_CSI_XX_T1CA_HSAMP_SRA	
7:6	RG_CSI_XX_T1CA_HSAMP_BW	
5:4	RG_CSI_XX_T1CA_HSAMP_IS	
3	RG_CSI_XX_T1CA_HSAMP_SCB	
2	RG_CSI_XX_T1CA_HSAMP_SCA	
1	RG_CSI_XX_T1CA_HSAMP_LPBK_TEST_EN	
0	RG_CSI_XX_T1CA_HSAMP_MON_EN	

10217824 MIPI_RX_AN A24_CSI2 DPHY Deserializer Control 0F000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI_RESERVE											RG_CSI_DPHY_L2_SYNC_EDGE_SEL		RG_CSI_DPHY_L2_FORCE_SYNC		RG_CSI_DPHY_L2_BYPASS_BYTECK_INVERT
Type	RW											RW		RW		RW
Reset	0	0	0	0	1	1	1	1				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_DPHY_L2_BYTECK_INVERT		RG_CSI_DPHY_L1_SYNC_EDGE_SEL		RG_CSI_DPHY_L1_FORCE_SYNC		RG_CSI_DPHY_L1_BYPASS_BYTECK_INVERT	RG_CSI_DPHY_L1_BYTECK_INVERT			RG_CSI_DPHY_L0_SYNC_EDGE_SEL		RG_CSI_DPHY_L0_FORCE_SYNC		RG_CSI_DPHY_L0_BYPASS_BYTECK_INVERT	RG_CSI_DPHY_L0_BYTECK_INVERT
Type	RW		RW		RW		RW	RW			RW		RW		RW	RW
Reset	0		0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RG_CSI_RESERVE	
20:19	RG_CSI_DPHY_L2_SYNC_EDGE_SEL	
18:17	RG_CSI_DPHY_L2_FORCE_SYNC	
16	RG_CSI_DPHY_L2_BYPASS_BYTECK_INVERT	
15	RG_CSI_DPHY_L2_BYTECK_INVERT	
13:12	RG_CSI_DPHY_L1_SYNC_EDGE_SEL	
11:10	RG_CSI_DPHY_L1_FORCE_SYNC	
9	RG_CSI_DPHY_L1_BYPASS_BYTECK_INVERT	
8	RG_CSI_DPHY_L1_BYTECK_INVERT	
5:4	RG_CSI_DPHY_L0_SYNC_EDGE_SEL	
3:2	RG_CSI_DPHY_L0_FORCE_SYNC	
1	RG_CSI_DPHY_L0_BYPASS_BYT	

Bit(s)	Name	Description
0	ECK_INVERT RG_CSI_DPHY_Lo_BYTECK_INVERT	

10217828 MIPI_RX_ANA28_CSI2 CPHY CDR Control 0000888F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CSI_CPHY_To_CDR_EARLY_CODE					RG_CSI_CPHY_To_CDR_INIT_CODE							RG_CSI_CPHY_To_CDR_MANUAL_EN
Type				RW					RW							RW
Reset				0	0	0	0	0	0	0	0	0	0			0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_To_CDR_CA_WIDTH				RG_CSI_CPHY_To_CDR_BC_WIDTH				RG_CSI_CPHY_To_CDR_AB_WIDTH				RG_CSI_CPHY_To_CDR_LPF_CTRL		RG_CSI_CPHY_To_CDR_AUTOLOAD_EN	RG_CSI_CPHY_To_CDR_DIRECT_EN
Type	RW				RW				RW				RW		RW	RW
Reset	1	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1

Bit(s)	Name	Description
28:24	RG_CSI_CPHY_To_CDR_EARLY_CODE	
23:19	RG_CSI_CPHY_To_CDR_INIT_CODE	
16	RG_CSI_CPHY_To_CDR_MANUAL_EN	
15:12	RG_CSI_CPHY_To_CDR_CA_WIDTH	Filter out coding jitter
11:8	RG_CSI_CPHY_To_CDR_BC_WIDTH	Filter out coding jitter
7:4	RG_CSI_CPHY_To_CDR_AB_WIDTH	Filter out coding jitter
3:2	RG_CSI_CPHY_To_CDR_LPF_CTRL	
1	RG_CSI_CPHY_To_CDR_AUTOLOAD_EN	
0	RG_CSI_CPHY_To_CDR_DIRECT_EN	Direct Sample Mode Enable

1021782C MIPI_RX_ANA2C_CSI2 CPHY CDR Control 00002000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI_CPHY_To_D	RG_CSI_CPHY_To_B	RG_CSI_CPHY_To_BIST_AB											

			EBUG_EN	IST_EN												
Type			RW	RW	RW											
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_To_BIST_AB		RG_CSI_CPHY_To_HSDET_SEL					RG_CSI_CPHY_To_FORCE_INIT	RG_CSI_CPHY_To_SYNC_INIT_SEL	RG_CSI_CPHY_To_SYMCK_INVERT		RG_CSI_CPHY_To_CDR_LATE_CODE				
Type	RW		RW					RW	RW	RW		RW				
Reset	0	0	1	0				0	0	0		0	0	0	0	0

Bit(s)	Name	Description
29	RG_CSI_CPHY_To_DEBUG_EN	
28	RG_CSI_CPHY_To_BIST_EN	
27:14	RG_CSI_CPHY_To_BIST_AB	
13:12	RG_CSI_CPHY_To_HSDET_SEL	
8	RG_CSI_CPHY_To_FORCE_INIT	[NORMAL]1'b0: Self [NORMAL]1'b1: DA
7	RG_CSI_CPHY_To_SYNC_INIT_SEL	[NORMAL]1'b0: Self [NORMAL]1'b1: DA
6	RG_CSI_CPHY_To_SYMCK_INVERT	
4:0	RG_CSI_CPHY_To_CDR_LATE_CODE	

10217830 MIPI_RX_ANA30_CSI2 CPHY CDR Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI_CPHY_To_BIST_CA													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_To_DEBUG_SEL		RG_CSI_CPHY_To_BIST_BC													
Type	RW		RW													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	RG_CSI_CPHY_To_BIST_CA	
15:14	RG_CSI_CPHY_To_DEBUG_SEL	
13:0	RG_CSI_CPHY_To_BIST_BC	

10217834 MIPI_RX_ANA34_CSI2 CPHY CDR Control 0000888F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_CSI_CPHY_T1_CDR_EARLY_CODE					RG_CSI_CPHY_T1_CDR_INIT_CODE							RG_CSI_CPHY_T1_C

																DR_MANUAL_EN
Type				RW					RW							RW
Reset				0	0	0	0	0	0	0	0	0	0			0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_T1_CDR_CA_WIDTH				RG_CSI_CPHY_T1_CDR_BC_WIDTH				RG_CSI_CPHY_T1_CDR_AB_WIDTH				RG_CSI_CPHY_T1_CDR_LPF_CTRL		RG_CSI_CPHY_T1_CDR_AUTOLOAD_EN	RG_CSI_CPHY_T1_CDR_DIRECT_EN
Type	RW				RW				RW				RW		RW	RW
Reset	1	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1

Bit(s)	Name	Description
28:24	RG_CSI_CPHY_T1_CDR_EARLY_CODE	
23:19	RG_CSI_CPHY_T1_CDR_INIT_CODE	
16	RG_CSI_CPHY_T1_CDR_MANUAL_EN	
15:12	RG_CSI_CPHY_T1_CDR_CA_WIDTH	Filter out coding jitter
11:8	RG_CSI_CPHY_T1_CDR_BC_WIDTH	Filter out coding jitter
7:4	RG_CSI_CPHY_T1_CDR_AB_WIDTH	Filter out coding jitter
3:2	RG_CSI_CPHY_T1_CDR_LPF_CTRL	
1	RG_CSI_CPHY_T1_CDR_AUTOLOAD_EN	
0	RG_CSI_CPHY_T1_CDR_DIRECT_EN	Direct Sample Mode Enable

10217838 MIPI_RX_ANA38_CSI2 **CPHY CDR Control** **00002000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI_CPHY_T1_DEBUG_EN	RG_CSI_CPHY_T1_BIST_EN	RG_CSI_CPHY_T1_BIST_AB											
Type			RW	RW	RW											
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_T1_BIST_AB		RG_CSI_CPHY_T1_HSDET_SEL					RG_CSI_CPHY_T1_FORCE_INIT	RG_CSI_CPHY_T1_SYNC_INIT_SEL	RG_CSI_CPHY_T1_SYMCK_INVERT		RG_CSI_CPHY_T1_CDR_LATE_CODE				
Type	RW		RW					RW	RW	RW		RW				
Reset	0	0	1	0				0	0	0		0	0	0	0	0

Bit(s)	Name	Description
29	RG_CSI_CPHY_T1_DEBUG_EN	
28	RG_CSI_CPHY_T1_BIST_EN	
27:14	RG_CSI_CPHY_T1_BIST_AB	
13:12	RG_CSI_CPHY_T1_HSDET_SEL	
8	RG_CSI_CPHY_T1_FORCE_INIT	[NORMAL]1'b0: Self [NORMAL]1'b1: DA
7	RG_CSI_CPHY_T1_SYNC_INIT_SEL	[NORMAL]1'b0: Self [NORMAL]1'b1: DA
6	RG_CSI_CPHY_T1_SYMCK_INVERT	
4:0	RG_CSI_CPHY_T1_CDR_LATE_CODE	

1021783C MIPI_RX_ANA3C_CSI2 CPHY CDR Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RG_CSI_CPHY_T1_BIST_CA													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI_CPHY_T1_DEBUG_SEL		RG_CSI_CPHY_T1_BIST_BC													
Type	RW		RW													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	RG_CSI_CPHY_T1_BIST_CA	
15:14	RG_CSI_CPHY_T1_DEBUG_SEL	
13:0	RG_CSI_CPHY_T1_BIST_BC	

10217840 MIPI_RX_ANA40_CSI2 GPI Control 40404040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_CSI_L1N_GPI_G	RG_CSI_L1N_GPI_RDSEL		RG_CSI_L1N_GPI_PD	RG_CSI_L1N_GPI_PU	RG_CSI_L1N_GPI_SMT	RG_CSI_L1N_GPI_IES		RG_CSI_L1P_GPI_G	RG_CSI_L1P_GPI_RDSEL		RG_CSI_L1P_GPI_PD	RG_CSI_L1P_GPI_PU	RG_CSI_L1P_GPI_SMT	RG_CSI_L1P_GPI_IES
Type		RW	RW		RW	RW	RW	RW		RW	RW		RW	RW	RW	RW
Reset		1	0	0	0	0	0	0		1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI_LoN_GPI_G	RG_CSI_LoN_GPI_RDSEL		RG_CSI_LoN_GPI_PD	RG_CSI_LoN_GPI_PU	RG_CSI_LoN_GPI_SMT	RG_CSI_LoN_GPI_IES		RG_CSI_LoP_GPI_G	RG_CSI_LoP_GPI_RDSEL		RG_CSI_LoP_GPI_PD	RG_CSI_LoP_GPI_PU	RG_CSI_LoP_GPI_SMT	RG_CSI_LoP_GPI_IES
Type		RW	RW		RW	RW	RW	RW		RW	RW		RW	RW	RW	RW
Reset		1	0	0	0	0	0	0		1	0	0	0	0	0	0

Bit(s)	Name	Description
30	RG_CSI_L1N_GPI_G	**RX Input Control Gating**

Bit(s)	Name	Description
29:28	RG_CSI_L1N_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
27	RG_CSI_L1N_GPI_PD	**75K pull-down resistor control. High activiate.**
26	RG_CSI_L1N_GPI_PU	**75K pull-up resistor control. High activiate.**
25	RG_CSI_L1N_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
24	RG_CSI_L1N_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.
22	RG_CSI_L1P_GPI_G	**RX Input Control Gating**
21:20	RG_CSI_L1P_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
19	RG_CSI_L1P_GPI_PD	**75K pull-down resistor control. High activiate.**
18	RG_CSI_L1P_GPI_PU	**75K pull-up resistor control. High activiate.**
17	RG_CSI_L1P_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
16	RG_CSI_L1P_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.
14	RG_CSI_L0N_GPI_G	**RX Input Control Gating**
13:12	RG_CSI_L0N_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
11	RG_CSI_L0N_GPI_PD	**75K pull-down resistor control. High activiate.**
10	RG_CSI_L0N_GPI_PU	**75K pull-up resistor control. High activiate.**
9	RG_CSI_L0N_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
8	RG_CSI_L0N_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.
6	RG_CSI_L0P_GPI_G	**RX Input Control Gating**
5:4	RG_CSI_L0P_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse

Bit(s)	Name	Description
		width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
3	RG_CSI_L0P_GPI_PD	**75K pull-down resistor control. High activiate.**
2	RG_CSI_L0P_GPI_PU	**75K pull-up resistor control. High activiate.**
1	RG_CSI_L0P_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
0	RG_CSI_L0P_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.

10217844 MIPI_RX_AN A44_CSI2 **GPI Control** **00004040**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI_L2N_GPI_G	RG_CSI_L2N_GPI_RDSEL		RG_CSI_L2N_GPI_PD	RG_CSI_L2N_GPI_PU	RG_CSI_L2N_GPI_SMT	RG_CSI_L2N_GPI_IES		RG_CSI_L2P_GPI_G	RG_CSI_L2P_GPI_RDSEL		RG_CSI_L2P_GPI_PD	RG_CSI_L2P_GPI_PU	RG_CSI_L2P_GPI_SMT	RG_CSI_L2P_GPI_IES
Type		RW	RW		RW	RW	RW	RW		RW	RW		RW	RW	RW	RW
Reset		1	0	0	0	0	0	0		1	0	0	0	0	0	0

Bit(s)	Name	Description
14	RG_CSI_L2N_GPI_G	**RX Input Control Gating**
13:12	RG_CSI_L2N_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment) Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
11	RG_CSI_L2N_GPI_PD	**75K pull-down resistor control. High activiate.**
10	RG_CSI_L2N_GPI_PU	**75K pull-up resistor control. High activiate.**
9	RG_CSI_L2N_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
8	RG_CSI_L2N_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.
6	RG_CSI_L2P_GPI_G	**RX Input Control Gating**
5:4	RG_CSI_L2P_GPI_RDSEL	**RX duty select** RDSEL[0]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[1]: Level shifter duty low when asserted (low pulse width adjustment)

Bit(s)	Name	Description
		Register programmable Default setting: 1.8V: RDSEL[1:0]=[00] 1.2V: RDSEL[1:0]=[11]
3	RG_CSI_L2P_GPI_PD	**75K pull-down resistor control. High activiate.**
2	RG_CSI_L2P_GPI_PU	**75K pull-up resistor control. High activiate.**
1	RG_CSI_L2P_GPI_SMT	**RX input buffer schmit trigger hysteresis control enable. High asserted.** SMT=1, Schmit Trigger enable
0	RG_CSI_L2P_GPI_IES	**RX input buffer enable. High asserted. Datapath: from IO to O. IES=0, O=0** For Vio turn-off applicatons, IES=0 prevent leakage in VDDIO power domain.

10217848 MIPI_RX_AN A48_CSI2 **RGS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AD_CSI_CPHY_T1_DEBUG_OUT	AD_CSI_CPHY_T1_BIST_CHECK_OUT	AD_CSI_CPHY_To_DEBUG_OUT	AD_CSI_CPHY_To_BIST_CHECK_OUT	AD_CSI_L2N_GPI_OUT	AD_CSI_L2P_GPI_OUT	AD_CSI_L1N_GPI_OUT	AD_CSI_L1P_GPI_OUT	AD_CSI_L0N_GPI_OUT	AD_CSI_L0P_GPI_OUT
Type							RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RGS_CSI_CPHY_T1_CDR_CODE								RGS_CSI_CPHY_To_CDR_CODE				
Type				RU								RU				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
25	AD_CSI_CPHY_T1_DEBUG_OUT	
24	AD_CSI_CPHY_T1_BIST_CHECK_OUT	
23	AD_CSI_CPHY_To_DEBUG_OUT	
22	AD_CSI_CPHY_To_BIST_CHECK_OUT	
21	AD_CSI_L2N_GPI_OUT	
20	AD_CSI_L2P_GPI_OUT	
19	AD_CSI_L1N_GPI_OUT	
18	AD_CSI_L1P_GPI_OUT	
17	AD_CSI_L0N_GPI_OUT	
16	AD_CSI_L0P_GPI_OUT	
12:8	RGS_CSI_CPHY_T1_CDR_CODE	
4:0	RGS_CSI_CPHY_To_CDR_CODE	

1021784C MIPI_RX_AN A4C_CSI2 **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DA_CSI_C	DA_CSI_C	DA_CSI_C	DA_CSI_C	DA_CSI_C	DA_CSI_C	AD_CSI_D	DA_CSI_D	AD_CSI_D	DA_CSI_D	AD_CSI_D	DA_CSI_D	AD_CSI_D	DA_CSI_D

			DPHY_L2N_T1C_HSRT_EN	DPHY_L2P_T1B_HSRT_EN	DPHY_L1N_T1A_HSRT_EN	DPHY_L1P_T0C_HSRT_EN	DPHY_L0N_T0B_HSRT_EN	DPHY_L0P_T0A_HSRT_EN	PHY_L2N_HSDET_OUT	PHY_L2N_HSDET_RSTB	PHY_L2P_HSDET_OUT	PHY_L2P_HSDET_RSTB	PHY_L1N_HSDET_OUT	PHY_L1N_HSDET_RSTB	PHY_L1P_HSDET_OUT	PHY_L1P_HSDET_RSTB
Type			RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AD_CSI_DPHY_L0N_HSDET_OUT	DA_CSI_DPHY_L0N_HSDET_RSTB	AD_CSI_DPHY_L0P_HSDET_OUT	DA_CSI_DPHY_L0P_HSDET_RSTB	AD_CSI_CDPHY_L2N_T1C_LPRX_OUT	DA_CSI_CDPHY_L2N_T1C_LPRX_EN	AD_CSI_CDPHY_L2P_T1B_LPRX_OUT	DA_CSI_CDPHY_L2P_T1B_LPRX_EN	AD_CSI_CDPHY_L1N_T1A_LPRX_OUT	DA_CSI_CDPHY_L1N_T1A_LPRX_EN	AD_CSI_CDPHY_L1P_T0C_LPRX_OUT	DA_CSI_CDPHY_L1P_T0C_LPRX_EN	AD_CSI_CDPHY_L0N_T0B_LPRX_OUT	DA_CSI_CDPHY_L0N_T0B_LPRX_EN	AD_CSI_CDPHY_L0P_T0A_LPRX_OUT	DA_CSI_CDPHY_L0P_T0A_LPRX_EN
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29	DA_CSI_CDPHY_L2N_T1C_HSRT_EN	
28	DA_CSI_CDPHY_L2P_T1B_HSRT_EN	
27	DA_CSI_CDPHY_L1N_T1A_HSRT_EN	
26	DA_CSI_CDPHY_L1P_T0C_HSRT_EN	
25	DA_CSI_CDPHY_L0N_T0B_HSRT_EN	
24	DA_CSI_CDPHY_L0P_T0A_HSRT_EN	
23	AD_CSI_DPHY_L2N_HSDET_OUT	
22	DA_CSI_DPHY_L2N_HSDET_RSTB	
21	AD_CSI_DPHY_L2P_HSDET_OUT	
20	DA_CSI_DPHY_L2P_HSDET_RSTB	
19	AD_CSI_DPHY_L1N_HSDET_OUT	
18	DA_CSI_DPHY_L1N_HSDET_RSTB	
17	AD_CSI_DPHY_L1P_HSDET_OUT	
16	DA_CSI_DPHY_L1P_HSDET_RSTB	
15	AD_CSI_DPHY_L0N_HSDET_OUT	
14	DA_CSI_DPHY_L0N_HSDET_RSTB	
13	AD_CSI_DPHY_L0P_HSDET_OUT	
12	DA_CSI_DPHY_L0P_HSDET_RSTB	
11	AD_CSI_CDPHY_L2N_T1C_LPRX_OUT	
10	DA_CSI_CDPHY_L2N_T1C_LPRX_EN	
9	AD_CSI_CDPHY_L2P_T1B_LPRX_OUT	
8	DA_CSI_CDPHY_L2P_T1B_LPRX_EN	
7	AD_CSI_CDPHY_L1N_T1A_LPRX_OUT	
6	DA_CSI_CDPHY_L1N_T1A_LPRX	

Bit(s)	Name	Description
	_EN	
5	AD_CSI_CDPHY_L1P_ToC_LPRX_OUT	
4	DA_CSI_CDPHY_L1P_ToC_LPRX_EN	
3	AD_CSI_CDPHY_LoN_ToB_LPRX_OUT	
2	DA_CSI_CDPHY_LoN_ToB_LPRX_EN	
1	AD_CSI_CDPHY_LoP_ToA_LPRX_OUT	
0	DA_CSI_CDPHY_LoP_ToA_LPRX_EN	

10217850 MIPI_RX_AN A50_CSI2 **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AD_CSI_CPHY_ToCA_HSAMP_OS_CK	AD_CSI_CPHY_ToCA_HSAMP_OS_OUT	DA_CSI_CPHY_ToCA_HSAMP_OS_CODE					DA_CSI_CPHY_ToCA_HSAMP_OS_CAL_EN	DA_CSI_CPHY_ToCA_HSAMP_OS_APPLY	DA_CSI_CPHY_ToCA_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							AD_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CK	AD_CSI_CDPHY_Lo_ToAB_HSAMP_OS_OUT	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CODE					DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CAL_EN	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_APPLY	DA_CSI_CDPHY_Lo_ToAB_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25	AD_CSI_CPHY_ToCA_HSAMP_OS_CK	
24	AD_CSI_CPHY_ToCA_HSAMP_OS_OUT	
23:19	DA_CSI_CPHY_ToCA_HSAMP_OS_CODE	
18	DA_CSI_CPHY_ToCA_HSAMP_OS_CAL_EN	
17	DA_CSI_CPHY_ToCA_HSAMP_OS_APPLY	
16	DA_CSI_CPHY_ToCA_HSAMP_EN	
9	AD_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CK	
8	AD_CSI_CDPHY_Lo_ToAB_HSAMP_OS_OUT	
7:3	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CODE	

Bit(s)	Name	Description
2	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_CAL_EN	
1	DA_CSI_CDPHY_Lo_ToAB_HSAMP_OS_APPLY	
0	DA_CSI_CDPHY_Lo_ToAB_HSAMP_EN	

10217854 MIPI_RX_ANA54_CSI2 **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AD_CSI_CDPHY_L1_T1AB_HSAMP_OS_CK	AD_CSI_CDPHY_L1_T1AB_HSAMP_OS_OUT	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_CODE					DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_CAL_EN	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_APPLY	DA_CSI_CDPHY_L1_T1AB_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							AD_CSI_CPHY_ToBC_HSAMP_OS_CK	AD_CSI_CPHY_ToBC_HSAMP_OS_OUT	DA_CSI_CPHY_ToBC_HSAMP_OS_CODE					DA_CSI_CPHY_ToBC_HSAMP_OS_CAL_EN	DA_CSI_CPHY_ToBC_HSAMP_OS_APPLY	DA_CSI_CPHY_ToBC_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25	AD_CSI_CDPHY_L1_T1AB_HSAMP_OS_CK	
24	AD_CSI_CDPHY_L1_T1AB_HSAMP_OS_OUT	
23:19	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_CODE	
18	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_CAL_EN	
17	DA_CSI_CDPHY_L1_T1AB_HSAMP_OS_APPLY	
16	DA_CSI_CDPHY_L1_T1AB_HSAMP_EN	
9	AD_CSI_CPHY_ToBC_HSAMP_OS_CK	
8	AD_CSI_CPHY_ToBC_HSAMP_OS_OUT	
7:3	DA_CSI_CPHY_ToBC_HSAMP_OS_CODE	
2	DA_CSI_CPHY_ToBC_HSAMP_OS_CAL_EN	
1	DA_CSI_CPHY_ToBC_HSAMP_OS_APPLY	
0	DA_CSI_CPHY_ToBC_HSAMP_EN	

Bit(s)	Name	Description

10217858 MIPI_RX_AN A58_CSI2 **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							AD_CSI_CDPHY_L2_T1BC_HSAMP_OS_CK	AD_CSI_CDPHY_L2_T1BC_HSAMP_OS_OUT	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_CODE					DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_CAL_EN	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_APPLY	DA_CSI_CDPHY_L2_T1BC_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							AD_CSI_CPHY_T1CA_HSAMP_OS_CK	AD_CSI_CPHY_T1CA_HSAMP_OS_OUT	DA_CSI_CPHY_T1CA_HSAMP_OS_CODE					DA_CSI_CPHY_T1CA_HSAMP_OS_CAL_EN	DA_CSI_CPHY_T1CA_HSAMP_OS_APPLY	DA_CSI_CPHY_T1CA_HSAMP_EN
Type							RU	RU	RU					RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25	AD_CSI_CDPHY_L2_T1BC_HSAMP_OS_CK	
24	AD_CSI_CDPHY_L2_T1BC_HSAMP_OS_OUT	
23:19	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_CODE	
18	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_CAL_EN	
17	DA_CSI_CDPHY_L2_T1BC_HSAMP_OS_APPLY	
16	DA_CSI_CDPHY_L2_T1BC_HSAMP_EN	
9	AD_CSI_CPHY_T1CA_HSAMP_OS_CK	
8	AD_CSI_CPHY_T1CA_HSAMP_OS_OUT	
7:3	DA_CSI_CPHY_T1CA_HSAMP_OS_CODE	
2	DA_CSI_CPHY_T1CA_HSAMP_OS_CAL_EN	
1	DA_CSI_CPHY_T1CA_HSAMP_OS_APPLY	
0	DA_CSI_CPHY_T1CA_HSAMP_EN	

1021785C MIPI_RX_AN A5C_CSI2 **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name		DA_CSI_DPHY_Lo_DELAY_CODE							AD_CSI_DPHY_Lo_BYPASS_BYTE_DATA							
Type		RU							RU							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_DPHY_Lo_DELAY_APPLY	DA_CSI_DPHY_Lo_DELAY_EN	AD_CSI_DPHY_Lo_BYPASS_BYTE_CK	AD_CSI_DPHY_Lo_SYNC_DETECT	AD_CSI_DPHY_Lo_BYTE_DATA								AD_CSI_DPHY_Lo_BYTE_CK	DA_CSI_DPHY_Lo_DES_SYNC_INIT	DA_CSI_DPHY_Lo_DES_EN	DA_CSI_DPHY_Lo_SAMP_EN
Type	RU	RU	RU	RU	RU								RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	DA_CSI_DPHY_Lo_DELAY_CODE	
23:16	AD_CSI_DPHY_Lo_BYPASS_BYTE_DATA	
15	DA_CSI_DPHY_Lo_DELAY_APPLY	
14	DA_CSI_DPHY_Lo_DELAY_EN	
13	AD_CSI_DPHY_Lo_BYPASS_BYTE_CK	
12	AD_CSI_DPHY_Lo_SYNC_DETECT	
11:4	AD_CSI_DPHY_Lo_BYTE_DATA	
3	AD_CSI_DPHY_Lo_BYTE_CK	
2	DA_CSI_DPHY_Lo_DES_SYNC_INIT	
1	DA_CSI_DPHY_Lo_DES_EN	
0	DA_CSI_DPHY_Lo_SAMP_EN	

10217860 MIPI_RX_AN_A60_CSI2 **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSI_DPHY_L1_DELAY_CODE							AD_CSI_DPHY_L1_BYPASS_BYTE_DATA							
Type		RU							RU							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_DPHY_L1_DELAY_APPLY	DA_CSI_DPHY_L1_DELAY_EN	AD_CSI_DPHY_L1_BYPASS_BYTE_CK	AD_CSI_DPHY_L1_SYNC_DETECT	AD_CSI_DPHY_L1_BYTE_DATA								AD_CSI_DPHY_L1_BYTE_CK	DA_CSI_DPHY_L1_DES_SYNC_INIT	DA_CSI_DPHY_L1_DES_EN	DA_CSI_DPHY_L1_SAMP_EN
Type	RU	RU	RU	RU	RU								RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	DA_CSI_DPHY_L1_DELAY_CODE	
23:16	AD_CSI_DPHY_L1_BYPASS_BYTE_DATA	
15	DA_CSI_DPHY_L1_DELAY_APPLY	

Bit(s)	Name	Description
14	DA_CSI_DPHY_L1_DELAY_EN	
13	AD_CSI_DPHY_L1_BYPASS_BYTE_CK	
12	AD_CSI_DPHY_L1_SYNC_DETECT	
11:4	AD_CSI_DPHY_L1_BYTE_DATA	
3	AD_CSI_DPHY_L1_BYTE_CK	
2	DA_CSI_DPHY_L1_DES_SYNC_INIT	
1	DA_CSI_DPHY_L1_DES_EN	
0	DA_CSI_DPHY_L1_SAMP_EN	

10217864 MIPI_RX_ANA64_CSI2 **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSI_DPHY_L2_DELAY_CODE							AD_CSI_DPHY_L2_BYPASS_BYTE_DATA							
Type		RU							RU							
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_DPHY_L2_DELAY_APPLY	DA_CSI_DPHY_L2_DELAY_EN	AD_CSI_DPHY_L2_BYPASS_BYTE_CK	AD_CSI_DPHY_L2_SYNC_DETECT	AD_CSI_DPHY_L2_BYTE_DATA								AD_CSI_DPHY_L2_BYTE_CK	DA_CSI_DPHY_L2_DES_SYNC_INIT	DA_CSI_DPHY_L2_DES_EN	DA_CSI_DPHY_L2_SAMP_EN
Type	RU	RU	RU	RU	RU								RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	DA_CSI_DPHY_L2_DELAY_CODE	
23:16	AD_CSI_DPHY_L2_BYPASS_BYTE_DATA	
15	DA_CSI_DPHY_L2_DELAY_APPLY	
14	DA_CSI_DPHY_L2_DELAY_EN	
13	AD_CSI_DPHY_L2_BYPASS_BYTE_CK	
12	AD_CSI_DPHY_L2_SYNC_DETECT	
11:4	AD_CSI_DPHY_L2_BYTE_DATA	
3	AD_CSI_DPHY_L2_BYTE_CK	
2	DA_CSI_DPHY_L2_DES_SYNC_INIT	
1	DA_CSI_DPHY_L2_DES_EN	
0	DA_CSI_DPHY_L2_SAMP_EN	

10217868 MIPI_RX_ANA68_CSI2 **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AD_CSI_CPHY_	DA_CSI_CPHY_

															To_HSDET_OUT	To_SYNC_INIT
Type															RU	RU
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_CPHY_To_DES_EN	DA_CSI_CPHY_To_CDR_EN	AD_CSI_CPHY_To_AB													
Type	RU	RU	RU													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	AD_CSI_CPHY_To_HSDET_OUT	
16	DA_CSI_CPHY_To_SYNC_INIT	
15	DA_CSI_CPHY_To_DES_EN	
14	DA_CSI_CPHY_To_CDR_EN	
13:0	AD_CSI_CPHY_To_AB	

1021786C MIPI_RX_ANA6C_CSI2 **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AD_CSI_CPHY_To_BC													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	AD_CSI_CPHY_To_BC	

10217870 MIPI_RX_ANA70_CSI2 **DEBUG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AD_CSI_CPHY_To_CA													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	AD_CSI_CPHY_To_CA	

10217874 MIPI_RX_ANA74_CSI2 DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AD_CSI_CPHY_T1_HSDET_OUT	DA_CSI_CPHY_T1_SYNC_INIT
Type															RU	RU
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CSI_CPHY_T1_DES_EN	DA_CSI_CPHY_T1_CDR_EN	AD_CSI_CPHY_T1_AB													
Type	RU	RU	RU													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	AD_CSI_CPHY_T1_HSDET_OUT	
16	DA_CSI_CPHY_T1_SYNC_INIT	
15	DA_CSI_CPHY_T1_DES_EN	
14	DA_CSI_CPHY_T1_CDR_EN	
13:0	AD_CSI_CPHY_T1_AB	

10217878 MIPI_RX_ANA78_CSI2 DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AD_CSI_CPHY_T1_BC													
Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	AD_CSI_CPHY_T1_BC	

1021787C MIPI_RX_ANA7C_CSI2 DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			AD_CSI_CPHY_T1_CA													

Type			RU													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	AD_CSI_CPHY_T1_CA	

10217880 MIPI_RX_WRAPPER80_CSI2 WRAPPER 04000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CSR_CSI0_DPHY_MUX			CSR_SW_RST				CSR_CSI1_CPHY_RST_MODE		CSR_CSI1_DPHY_RST_MODE		CSR_CSI0_CPHY_RST_MODE		CSR_CSI0_DPHY_RST_MODE	
Type		RW			RW				RW		RW		RW		RW	
Reset		0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_CSI_MON_MUX								CSR_CSI_MODE				CSR_CSI1_DPHY_MUX		CSR_HSDET_MODE	CSR_CSI_CLK_MON
Type	RW								RW				RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:28	CSR_CSI0_DPHY_MUX	
27:24	CSR_SW_RST	
23:22	CSR_CSI1_CPHY_RST_MODE	0: sync init 1: hsrx_en 2: sw rst 3: hw rst
21:20	CSR_CSI1_DPHY_RST_MODE	0: sync init 1: hsrx_en 2: sw rst 3: hw rst
19:18	CSR_CSI0_CPHY_RST_MODE	0: sync init 1: hsrx_en 2: sw rst 3: hw rst
17:16	CSR_CSI0_DPHY_RST_MODE	0: sync init 1: hsrx_en 2: sw rst 3: hw rst
15:8	CSR_CSI_MON_MUX	
7:4	CSR_CSI_MODE	0:4 lane 1:2/2l lane 2:cphy 4:cphy/2 lane
3:2	CSR_CSI1_DPHY_MUX	
1	CSR_HSDET_MODE	0:dn 1:dp
0	CSR_CSI_CLK_MON	Enable Clock monitor

10217884 MIPI_RX_WRAPPER84_CSI WRAPPER 00000000

I2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI_DEBUG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI_DEBUG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSI_DEBUG_OUT	

10217888 MIPI_RX_WRAPPER88_CSI2 **WRAPPER** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_MODE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_MODE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_MODE_0	

1021788C MIPI_RX_WRAPPER8C_CSI2 **WRAPPER** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_MODE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_MODE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_MODE_1	

10217890 MIPI_RX_WRAPPER90_CSI2 **WRAPPER** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	CSR_SW_MODE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_MODE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_MODE_2	

10217894 MIPI_RX_WRAPPER94_CSI2 WRAPPER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_VALUE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_VALUE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_VALUE_0	

10217898 MIPI_RX_WRAPPER98_CSI2 WRAPPER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_VALUE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_VALUE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_VALUE_1	

1021789C MIPI_RX_WRAPPER9C_CSI2 WRAPPER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR_SW_VALUE_2															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR_SW_VALUE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSR_SW_VALUE_2	

Module name: mipi_tx_config Base address: (+10215000h)

Address	Name	Width	Register Function
10215000	DSI_CON	32	DSI Configuration Register
10215004	DSI_CLOCK_LANE	32	DSI Clock Lane Configuration Register
10215008	DSI_DATA_LANE_0	32	DSI Data Lane 0 Configuration Register
1021500C	DSI_DATA_LANE_1	32	DSI Data Lane 1 Configuration Register
10215010	DSI_DATA_LANE_2	32	DSI Data Lane 2 Configuration Register
10215014	DSI_DATA_LANE_3	32	DSI Data Lane 3 Configuration Register
10215040	DSI_TOP_CON	32	DSI Top Configuration Register
10215044	DSI_BG_CON	32	DSI BG Configuration Register
10215050	DSI_PLL_CON0	32	DSI PLL Configuration 0 Register
10215054	DSI_PLL_CON1	32	DSI PLL Configuration 1 Register
10215058	DSI_PLL_CON2	32	DSI PLL Configuration 2 Register
1021505C	DSI_PLL_CON3	32	DSI PLL Configuration 3 Register
10215060	DSI_PLL_CHG	32	DSI PLL Charge Register
10215064	DSI_PLL_TOP	32	DSI PLL Top Register
10215068	DSI_PLL_PWR	32	DSI PLL Power Control Register
10215070	DSI_GPI_CON0	32	DSI GPI Control 0 Register
10215074	DSI_GPI_CON1	32	DSI GPI Control 1 Register
10215078	DSI_GPI_CON2	32	DSI GPI Control 1 Register
1021507C	DSI_PHY_SEL	32	DSI MIPI TX PHY Lane Swap Selection
10215080	DSI_SW_CTRL_EN	32	DSI Software Control Enable Register
10215084	DSI_SW_CTRL_CON0	32	DSI Software Control Configuration Register 0
10215088	DSI_SW_CTRL_CON1	32	DSI Software Control Configuration Register 1
1021508C	DSI_SW_CTRL_CON2	32	DSI Software Control Configuration Register 0
10215090	DSI_DBG_CON	32	DSI Debug Control Register
10215094	DSI_DBG_OUT	32	DSI Debug Out Register
10215098	DSI_APB_ASYNC_STA	32	DSI APB Async Status Register
10215200	DSI_HS_BIST_CON	32	CSI HS BIST Configuration
10215204	DSI_HS_BIST_PAT	32	CSI HS BIST Pattern

10215000 DSI_CON DSI Configuration Register 00001040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name											RG_DSI_BIST_2D5G_PRESERVE 0					
Type											RW					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_DSI_BIST_DATA_SEL	RG_DSI_BIST_2D5G_SEL	RG_DSI_BIST_2D5G_EN	RG_DSI_DSICLK_FREQ_SEL	RG_DSI_PHYCLK_SEL		RG_DSI_CKG_IMINUS	RG_DSI_CKG_IPLUS	RG_DSI_LDO_VOD_EN	RG_DSI_LDO_LPF_EN	RG_DSI_LD_IDX_SEL		RG_DSI_BCLK_SEL		RG_DSI_CKG_LDOOUT_EN	RG_DSI_LDOCORE_EN
Type	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW		RW		RW	RW
Reset	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:16		RG_DSI_BIST_2D5G_PRESERVE0	**Reserved**
15		RG_DSI_BIST_DATA_SEL	**Selects for CSI BIST path**
14		RG_DSI_BIST_2D5G_SEL	**Selects analog 2D5G**
13		RG_DSI_BIST_2D5G_EN	**Enables analog 2D5G**
12		RG_DSI_DSICLK_FREQ_SEL	**Selects frequency of DSICLK** 1'b0: 2X of PHYCLK 1'b1: 1X of PHYCLK
11:10		RG_DSI_PHYCLK_SEL	**Selects phase of DSI PHYCLK** 2'b00: Align with BCLK 2'b01: Align with BCLKQ 2'b10: Align with BCLKB 2'b11: Align with BCLKQB
9		RG_DSI_CKG_IMINUS	**Decreases bias current for DSI clock generator** 1'b00: Normal 1'b01: -10%
8		RG_DSI_CKG_IPLUS	**Increases bias current for DSI clock generator** 1'b00: Normal 1'b01: +10%
7		RG_DSI_LDO_VOD_EN	**Enables voltage offset for DSI LDOs** 1'b0: Disable, LDO output 1.0V 1'b1: Enable, LDO output 1.1V
6		RG_DSI_LDO_LPF_EN	**Enables low-pass filter for DSI LDOs** 1'b0: Disable low-pass filter 1'b1: Enable low-pass filter
5:4		RG_DSI_LD_IDX_SEL	**Selects phase of DSI LD_IDX** 2'b00: Align with CKQ 2'b01: Align with CKB 2'b10: Align with CKQB 2'b11: Align with CK
3:2		RG_DSI_BCLK_SEL	**Selects phase of DSI byte clock** 2'b00: Align with CK 2'b01: Align with CKQ 2'b10: Align with CKB 2'b11: Align with CKQB
1		RG_DSI_CKG_LDOOUT_EN	**Enables LDO output for DSI clock generator** 1'b0: Disable 1'b1: Enable
0		RG_DSI_LDOCORE_EN	**Enables bias current for DSI LDOs** 1'b0: Disable 1'b1: Enable

Bit(s)	Mnemonic	Name	Description

10215004 DSI_CLOCK_LANE **DSI Clock Lane Configuration Register** **00000802**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_DSI_LNTC_RT_CODE						RG_DSI_LNTC_EO_SWAP	RG_DSI_LNTC_PN_SWAP	RG_DSI_LNTC_IMINUS	RG_DSI_LNTC_IPLUS	RG_DSI_LNTC_CKLANE_EN	RG_DSI_LNTC_LDOOUT_EN
Type					RW						RW	RW	RW	RW	RW	RW
Reset					1	0	0	0			0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
11:8		RG_DSI_LNTC_RT_CODE	**DSI clock lane HS impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
5		RG_DSI_LNTC_EO_SWAP	**Swaps even and odd bits for DSI clock lane** 1'b0: Normal 1'b1: Swap the even and odd bits for clock lane
4		RG_DSI_LNTC_PN_SWAP	**Swaps P/N pins for DSI clock lane** 1'b0: Normal 1'b1: Swap output P/N for clock lane
3		RG_DSI_LNTC_IMINUS	**Decreases bias current for DSI clock Lane** 1'b00: Normal 1'b01: -10%
2		RG_DSI_LNTC_IPLUS	**Increases bias current for DSI clock Lane** 1'b00: Normal 1'b01: +10%
1		RG_DSI_LNTC_CKLANE_EN	**Selects clock source for clock lane** 1'b0: In phase clock for data lane 1'b1: Quadrature phase clock for clock lane
0		RG_DSI_LNTC_LDOOUT_EN	**Enables LDO output for DSI clock lane** 1'b0: Disable 1'b1: Enable

10215008 DSI_DATA_LANE_0 **DSI Data Lane 0 Configuration Register** **00000800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_DSI_LNTo_RT_CODE						RG_DSI_LNTo_EO_SWAP	RG_DSI_LNTo_PN_SWAP	RG_DSI_LNTo_IMINUS	RG_DSI_LNTo_IPLUS	RG_DSI_LNTo_CKLANE_E	RG_DSI_LNTo_LDOOUT_E

															N	N
Type					RW						RW	RW	RW	RW	RW	RW
Reset					1	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:8		RG_DSI_LNT0_RT_CODE	**DSI Data Lane 0 HS impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
5		RG_DSI_LNT0_EO_SWAP	**Swaps even and odd bits for DSI Data Lane 0** 1'b0: Normal 1'b1: Swap even and odd bits for Data Lane 0
4		RG_DSI_LNT0_PN_SWAP	**Swaps P/N pins for DSI Data Lane 0** 1'b0: Normal 1'b1: Swap output P/N for Data Lane 0
3		RG_DSI_LNT0_IMINUS	**Decreases bias current for DSI Data Lane 0** 1'b00: Normal 1'b01: -10%
2		RG_DSI_LNT0_IP LUS	**Increases bias current for DSI Data Lane 0** 1'b00: Normal 1'b01: +10%
1		RG_DSI_LNT0_CK LANE_EN	**Select clock source for DSI Data Lane 0** 1'b0: In phase clock for data lane 1'b1: Quadrature phase clock for clock lane
0		RG_DSI_LNT0_LD OOUT_EN	**Enables LDO output for DSI Data Lane 0** 1'b0: Disable 1'b1: Enable

1021500C DSI_DATA_LANE_1 **DSI Data Lane 1 Configuration Register** **00000800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_DSI_LNT1_RT_CODE						RG_DSI_LNT1_EO_SWAP	RG_DSI_LNT1_PN_SWAP	RG_DSI_LNT1_IMINUS	RG_DSI_LNT1_IPLUS	RG_DSI_LNT1_CKLANE_EN	RG_DSI_LNT1_LDOOUT_EN
Type					RW						RW	RW	RW	RW	RW	RW
Reset					1	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:8		RG_DSI_LNT1_RT_CODE	**DSI Data Lane 1 HS impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
5		RG_DSI_LNT1_EO_SWAP	**Swaps even and odd bits for DSI Data Lane 1** 1'b0: Normal 1'b1: Swap even and odd bits for Data Lane 1
4		RG_DSI_LNT1_PN_SWAP	**Swaps P/N pins for DSI Data Lane 1** 1'b0: Normal 1'b1: Swap output P/N for Data Lane 1
3		RG_DSI_LNT1_IMINUS	**Decreases bias current for DSI Data Lane 1** 1'b00: Normal

Bit(s)	Mnemonic	Name	Description
			1'b01: -10%
2		RG_DSI_LNT1_IP LUS	**Increases bias current for DSI Data Lane 1** 1'b00: Normal 1'b01: +10%
1		RG_DSI_LNT1_CK LANE_EN	**Selects clock source for DSI Data Lane 1** 1'b0: In phase clock for data lane 1'b1: Quadrature phase clock for clock lane
0		RG_DSI_LNT1_LD OOUT_EN	**Enables LDO output for DSI Data Lane 1** 1'b0: Disable 1'b1: Enable

10215010 DSI_DATA_LANE_2 DSI Data Lane 2 Configuration Register 00000800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_DSI_LNT2_RT_CODE						RG_DSI_LNT2_EO_SWAP	RG_DSI_LNT2_PN_SWAP	RG_DSI_LNT2_IMINUS	RG_DSI_LNT2_IPLUS	RG_DSI_LNT2_CKLANE_EN	RG_DSI_LNT2_LDOOUT_EN
Type					RW						RW	RW	RW	RW	RW	RW
Reset					1	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:8		RG_DSI_LNT2_RT _CODE	**DSI Data Lane 2 HS impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
5		RG_DSI_LNT2_EO _SWAP	**Swaps even and odd bits for DSI Data Lane 2** 1'b0: Normal 1'b1: Swap even and odd bits for Data Lane 2
4		RG_DSI_LNT2_PN _SWAP	**Swaps P/N pins for DSI Data Lane 2** 1'b0: Normal 1'b1: Swap output P/N for Data Lane 2
3		RG_DSI_LNT2_IM INUS	**Decreases bias current for DSI Data Lane 2** 1'b00: Normal 1'b01: -10%
2		RG_DSI_LNT2_IP LUS	**Increases bias current for DSI Data Lane 2** 1'b00: Normal 1'b01: +10%
1		RG_DSI_LNT2_CK LANE_EN	**Selects clock source for DSI Data Lane 2** 1'b0: In phase clock for data lane 1'b1: Quadrature phase clock for clock lane
0		RG_DSI_LNT2_LD OOUT_EN	**Enables LDO output for DSI Data Lane 2** 1'b0: Disable 1'b1: Enable

10215014 DSI_DATA_LANE_3 DSI Data Lane 3 Configuration Register 00000800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_DSI_LNT3_RT_CODE						RG_DSI_LNT3_EO_SWAP	RG_DSI_LNT3_PN_SWAP	RG_DSI_LNT3_IMINUS	RG_DSI_LNT3_IPLUS	RG_DSI_LNT3_CKLANE_EN	RG_DSI_LNT3_LDOOUT_EN
Type					RW						RW	RW	RW	RW	RW	RW
Reset					1	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:8		RG_DSI_LNT3_RT_CODE	**DSI Data Lane 3 HS impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
5		RG_DSI_LNT3_EO_SWAP	**Swaps even and odd bits for DSI Data Lane 3** 1'b0: Normal 1'b1: Swap even and odd bits for Data Lane 3
4		RG_DSI_LNT3_PN_SWAP	**Swaps P/N pins for DSI Data Lane 3** 1'b0: Normal 1'b1: Swap the output P/N for Data Lane 3
3		RG_DSI_LNT3_IMINUS	**Decreases bias current for DSI Data Lane 3** 1'b00: Normal 1'b01: -10%
2		RG_DSI_LNT3_IPLUS	**Increases bias current for DSI Data Lane 3** 1'b00: Normal 1'b01: +10%
1		RG_DSI_LNT3_CKLANE_EN	**Selects clock source for DSI Data Lane 3** 1'b0: In phase clock for data lane 1'b1: Quadrature phase clock for clock lane
0		RG_DSI_LNT3_LDOOUT_EN	**Enables the LDO output for DSI Data Lane 3** 1'b0: Disable 1'b1: Enable

10215040 DSI_TOP_CON — DSI Top Configuration Register — 0000F800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_DSI_PRESERVE1				RG_DSI_PAD_TIE_LOW_EN	RG_DSI_LNT_AIO_SEL			RG_DSI_PRESERVE0				RG_DSI_LNT_TESTMODE_EN			
Type	RW				RW	RW			RW				RW			
Reset	1	1	1	1	1	0	0	0	0	0	0	0	0			

Bit(s)	Mnemonic	Name	Description
15:12		RG_DSI_PRESERVE1	**DSI preserved registers**

Bit(s)	Mnemonic	Name	Description
11		RG_DSI_PAD_TIE_LOW_EN	**Enables tie-low resistors for DSI 10 pads** 1'b0: Floating or depends on line driver. 1'b1: Tie to ground with 20k ohm resistors
10:8		RG_DSI_LNT_AIO_SEL	**Selects analog debug output** 3'b000: Output VREF 0.2V 3'b001: Output VREF 0.32V 3'b010: Output VREF 0.4V 3'b011: Output VREF 0.72V 3'b100: Output VREF 0.86V 3'b101: Output VREF 1.2V 3'b110: Output VCCK09 3'b111: Output PLL_TST
7:4		RG_DSI_PRESERV E0	**DSI preserved registers**
3		RG_DSI_LNT_TESTMODE_EN	**Enables analog test mode in DSI** 1'b0: Disable 1'b1: Enable

10215044 DSI_BG_CON DSI BG Configuration Register 01249240

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								RG_DSI_V03_SEL			RG_DSI_V035_SEL			RG_DSI_V07_SEL		
Type								RW			RW			RW		
Reset								1	0	0	1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_DSI_V075_SEL			RG_DSI_V04_SEL			RG_DSI_V10_SEL			RG_DSI_V12_SEL						RG_DSI_BG_CORE_EN
Type	RW			RW			RW			RW						RW
Reset	1	0	0	1	0	0	1	0	0	1	0	0				0

Bit(s)	Mnemonic	Name	Description
24:22		RG_DSI_V03_SEL	**Selects 0.3V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
21:19		RG_DSI_V035_SEL	**Selects 0.35V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
18:16		RG_DSI_V07_SEL	**Selects 0.7V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
15:13		RG_DSI_V075_SEL	**Selects 0.75V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
12:10		RG_DSI_V04_SEL	**Selects 0.4V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
9:7		RG_DSI_V10_SEL	**Selects AVDD10 output voltage**

Bit(s)	Mnemonic	Name	Description
			3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
6:4		RG_DSI_V12_SEL	**Selects 1.2V output voltage** 3'b0000: Minimum voltage 3'b0100: Typical voltage 3'b0111: Maximum voltage
0		RG_DSI_BG_CORE_EN	**Enables R-string for reference voltage** 1'b0: Power off 1'b1: Enable R-string voltages

10215050 DSI_PLL_CON0 **DSI PLL Configuration 0 Register** **F0002010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_DSI_MPPLL_PRESERV_E1				RG_DSI_MPPLL_PRESERV_E0											
Type	RW				RW											
Reset	1	1	1	1	0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_DSI_MPPLL_PLLOUT_EN	RG_DSI_MPPLL_S2QDIV		RG_DSI_MPPLL_VOD_EN		RG_DSI_MPPLL_MONREF_EN	RG_DSI_MPPLL_MONVC_EN		RG_DSI_MPPLL_POSDIV			RG_DSI_MPPLL_PREDIV			RG_DSI_MPPLL_PLL_EN
Type		RW	RW		RW		RW	RW		RW			RW			RW
Reset		0	1	0	0		0	0		0	0	1	0	0		0

Bit(s)	Mnemonic	Name	Description
31:28		RG_DSI_MPPLL_PRESERVE1	**DSI MPPLL preserved registers**
27:24		RG_DSI_MPPLL_PRESERVE0	**DSI MPPLL preserved registers**
14		RG_DSI_MPPLL_PLLOUT_EN	**Enables PLL output for LVDS** 1'b0: Disable 1'b1: Enable
13:12		RG_DSI_MPPLL_S2QDIV	**Selects divisor for the quadrature phase divider** 2'b00: Gate the output to ground 2'b01: Divided by 2 2'b1x: Divided by 4
11		RG_DSI_MPPLL_VOD_EN	**Overdrive LDO** 1'b0: Disable 1'b1: Enable
9		RG_DSI_MPPLL_MONREF_EN	**Monitor PLL reference clock** 1'b0: Disable 1'b1: Enable
8		RG_DSI_MPPLL_MONVC_EN	**Monitor VCO controlled voltage** 1'b0: Disable 1'b1: Enable
6:4		RG_DSI_MPPLL_POSDIV	**PLL post divide ratio** 3'b000: /1 3'b001: /2 3'b010: /4 3'b011: /8 3'b100: /16

Bit(s)	Mnemonic	Name	Description
			Others: Clock gating
3:2		RG_DSI_MPPLL_PREDIV	**Pre divide ratio** 2'b00: /1 2'b01: /2 2'b1x: /4
0		RG_DSI_MPPLL_PLL_EN	**Enables MIPI PLL** 1'b0: Power down 1'b1: Enable

10215054 DSI_PLL_CON1 **DSI PLL Configuration 1 Register** **00000003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_DSI_MPPLL_ SDM_SSC_PRD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_DSI_MPPLL_SDM_SSC_EN	RG_DSI_MPPLL_SDM_SSC_PH_INIT	RG_DSI_MPPLL_SDM_FRA_EN
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Mnemonic	Name	Description
31:16		RG_DSI_MPPLL_SDM_SSC_PRD	**SDM SSC period** 16'd0: Min. 16'd65536: Max.
2		RG_DSI_MPPLL_SDM_SSC_EN	**Enables SDM SSC** 1'b0: Disable 1'b1: Enable
1		RG_DSI_MPPLL_SDM_SSC_PH_INIT	**Initializes SDM SSC phase** 1'b0: Upward 1'b1: Downward
0		RG_DSI_MPPLL_SDM_FRA_EN	**Enables SDM PLL fractional mode** 1'b0: Integer mode 1'b1: Fractional mode

10215058 DSI_PLL_CON2 **DSI PLL Configuration 2 Register** **50000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_DSI_MPPLL_SDM_PCW														
Type		RW														
Reset		1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_DSI_MPPLL_SDM_PCW															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		RG_DSI_MPPLL_SDM_PCW	**Feedback divide ratio** 8-bit integer + 24-bit fractional

1021505C DSI_PLL_CON3 **DSI PLL Configuration 3 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_DSI_MPPLL_SDM_SSC_DELTA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_DSI_MPPLL_SDM_SSC_DELTA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		RG_DSI_MPPLL_SDM_SSC_DELTA	**SDM SSC amplitude** 16'do: Min. 16'd65536: Max.
15:0		RG_DSI_MPPLL_SDM_SSC_DELTA1	**SDM SSC amplitude 1** 16'do: Min. 16'd65536: Max.

10215060 DSI_PLL_CHG **DSI PLL Charge Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_DSI_MPPLL_SDM_PCW_CHG
Type																RW
Reset																1

Bit(s)	Mnemonic	Name	Description
0		RG_DSI_MPPLL_SDM_PCW_CHG	Trigger signal to update divide ratio of feedback divider

10215064 DSI_PLL_TOP **DSI PLL Top Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_DSI_MPPLL_TSTSEL		RG_DSI_MPPLL_TSTCK_EN	RG_DSI_MPPLL_TST_EN
Type													RW		RW	RW
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:2		RG_DSI_MPPLL_TSTSEL	**Selects MIPI PLL test mode** [0]: Used for RG_DSI_MPPLL_MONCK_EN [1]: Not used
1		RG_DSI_MPPLL_TSTCK_EN	**Enables MIPI PLL test clock** 1'b0: Disable 1'b1: Enable
0		RG_DSI_MPPLL_TST_EN	**Enables MIPI PLL test** 1'b0: Disable 1'b1: Enable

10215068 DSI_PLL_PWR DSI PLL Power Control Register 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								AD_DSI_MPPLL_SDM_PWR_ACK							DA_DSI_MPPLL_SDM_ISO_EN	DA_DSI_MPPLL_SDM_PWR_ON
Type								RU							RW	RW
Reset								0							1	0

Bit(s)	Mnemonic	Name	Description
8		AD_DSI_MPPLL_SDM_PWR_ACK	**Acknowledges PLL power-on** 1'b0: No effect 1'b1: Power-on ack
1		DA_DSI_MPPLL_SDM_ISO_EN	**Enables PLL isolation** 1'b0: Disable 1'b1: Enable
0		DA_DSI_MPPLL_SDM_PWR_ON	**Controls PLL power-on** 1'b0: Power-off 1'b1: Power-on

10215070 DSI_GPI_CON DSI GPI Control 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							RG_DSI_G	RG_DSI_G	RG_DSI_G	RG_DSI_G	RG_DSI_G	RG_DSI_G	RG_DSI_G	RG_DSI_G	RG_DSI_G	RG_DSI_G

							PI9_SMT	PI8_SMT	PI7_SMT	PI6_SMT	PI5_SMT	PI4_SMT	PI3_SMT	PI2_SMT	PI1_SMT	PI0_SMT
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_DSI_GPI9_IES	RG_DSI_GPI8_IES	RG_DSI_GPI7_IES	RG_DSI_GPI6_IES	RG_DSI_GPI5_IES	RG_DSI_GPI4_IES	RG_DSI_GPI3_IES	RG_DSI_GPI2_IES	RG_DSI_GPI1_IES	RG_DSI_GPI0_IES
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25		RG_DSI_GPI9_SMT	**DSI GPI9 Schmitt trigger for PAD_TDN3** 1'b0: Disable 1'b1: Enable
24		RG_DSI_GPI8_SMT	**DSI GPI8 Schmitt trigger for PAD_TDP3** 1'b0: Disable 1'b1: Enable
23		RG_DSI_GPI7_SMT	**DSI GPI7 Schmitt trigger for PAD_TDN2** 1'b0: Disable 1'b1: Enable
22		RG_DSI_GPI6_SMT	**DSI GPI6 Schmitt trigger for PAD_TDP2** 1'b0: Disable 1'b1: Enable
21		RG_DSI_GPI5_SMT	**DSI GPI5 Schmitt trigger for PAD_TCN** 1'b0: Disable 1'b1: Enable
20		RG_DSI_GPI4_SMT	**DSI GPI4 Schmitt trigger for PAD_TCP** 1'b0: Disable 1'b1: Enable
19		RG_DSI_GPI3_SMT	**DSI GPI3 Schmitt trigger for PAD_TDN1** 1'b0: Disable 1'b1: Enable
18		RG_DSI_GPI2_SMT	**DSI GPI2 Schmitt trigger for PAD_TDP1** 1'b0: Disable 1'b1: Enable
17		RG_DSI_GPI1_SMT	**DSI GPI1 Schmitt trigger for PAD_TDN0** 1'b0: Disable 1'b1: Enable
16		RG_DSI_GPI0_SMT	**DSI GPI0 Schmitt trigger for PAD_TDP0** 1'b0: Disable 1'b1: Enable
9		RG_DSI_GPI9_IES	**Enables DSI GPI9 input buffer for PAD_TDN3** 1'b0: Disable 1'b1: Enable
8		RG_DSI_GPI8_IES	**Enables DSI GPI8 input buffer for PAD_TDP3** 1'b0: Disable 1'b1: Enable
7		RG_DSI_GPI7_IES	**Enables DSI GPI7 input buffer for PAD_TDN2** 1'b0: Disable 1'b1: Enable
6		RG_DSI_GPI6_IES	**Enables DSI GPI6 input buffer for PAD_TDP2** 1'b0: Disable 1'b1: Enable
5		RG_DSI_GPI5_IES	**Enables DSI GPI5 input buffer for PAD_TCN**

Bit(s)	Mnemonic	Name	Description
			1'b0: Disable 1'b1: Enable
4		RG_DSI_GPI4_IE S	**Enables DSI GPI4 input buffer for PAD_TCP** 1'b0: Disable 1'b1: Enable
3		RG_DSI_GPI3_IE S	**Enables DSI GPI3 input buffer for PAD_TDN1** 1'b0: Disable 1'b1: Enable
2		RG_DSI_GPI2_IE S	**Enables DSI GPI2 input buffer for PAD_TDP1** 1'b0: Disable 1'b1: Enable
1		RG_DSI_GPI1_IE S	**Enables DSI GPI1 input buffer for PAD_TDN0** 1'b0: Disable 1'b1: Enable
0		RG_DSI_GPI0_IE S	**Enables DSI GPI0 input buffer for PAD_TDP0** 1'b0: Disable 1'b1: Enable

10215074 DSI_GPI_CON1 **DSI GPI Control 1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							RG_DSI_GPI9_PD	RG_DSI_GPI8_PD	RG_DSI_GPI7_PD	RG_DSI_GPI6_PD	RG_DSI_GPI5_PD	RG_DSI_GPI4_PD	RG_DSI_GPI3_PD	RG_DSI_GPI2_PD	RG_DSI_GPI1_PD	RG_DSI_GPI0_PD
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_DSI_GPI9_PU	RG_DSI_GPI8_PU	RG_DSI_GPI7_PU	RG_DSI_GPI6_PU	RG_DSI_GPI5_PU	RG_DSI_GPI4_PU	RG_DSI_GPI3_PU	RG_DSI_GPI2_PU	RG_DSI_GPI1_PU	RG_DSI_GPI0_PU
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25		RG_DSI_GPI9_PD	**DSI GPI9 pull-down control for PAD_TDN3** 1'b0: Disable 1'b1: Enable
24		RG_DSI_GPI8_PD	**DSI GPI8 pull-down control for PAD_TDP3** 1'b0: Disable 1'b1: Enable
23		RG_DSI_GPI7_PD	**DSI GPI7 pull-down control for PAD_TDN2** 1'b0: Disable 1'b1: Enable
22		RG_DSI_GPI6_PD	**DSI GPI6 pull-down control for PAD_TDP2** 1'b0: Disable 1'b1: Enable
21		RG_DSI_GPI5_PD	**DSI GPI5 pull-down control for PAD_TCN** 1'b0: Disable 1'b1: Enable
20		RG_DSI_GPI4_PD	**DSI GPI4 pull-down control for PAD_TCP** 1'b0: Disable

Bit(s)	Mnemonic	Name	Description
			1'b1: Enable
19		RG_DSI_GPI3_PD	**DSI GPI3 pull-down control for PAD_TDN1** 1'b0: Disable 1'b1: Enable
18		RG_DSI_GPI2_PD	**DSI GPI2 pull-down control for PAD_TDP1** 1'b0: Disable 1'b1: Enable
17		RG_DSI_GPI1_PD	**DSI GPI1 pull-down control for PAD_TDN0** 1'b0: Disable 1'b1: Enable
16		RG_DSI_GPI0_PD	**DSI GPI0 pull-down control for PAD_TDP0** 1'b0: Disable 1'b1: Enable
9		RG_DSI_GPI9_PU	**DSI GPI9 pull-up control for PAD_TDN3** 1'b0: Disable 1'b1: Enable
8		RG_DSI_GPI8_PU	**DSI GPI8 pull-up control for PAD_TDP3** 1'b0: Disable 1'b1: Enable
7		RG_DSI_GPI7_PU	**DSI GPI7 pull-up control for PAD_TDN2** 1'b0: Disable 1'b1: Enable
6		RG_DSI_GPI6_PU	**DSI GPI6 pull-up control for PAD_TDP2** 1'b0: Disable 1'b1: Enable
5		RG_DSI_GPI5_PU	**DSI GPI5 pull-up control for PAD_TCN** 1'b0: Disable 1'b1: Enable
4		RG_DSI_GPI4_PU	**DSI GPI4 pull-up control for PAD_TCP** 1'b0: Disable 1'b1: Enable
3		RG_DSI_GPI3_PU	**DSI GPI3 pull-up control for PAD_TDN1** 1'b0: Disable 1'b1: Enable
2		RG_DSI_GPI2_PU	**DSI GPI2 pull-up control for PAD_TDP1** 1'b0: Disable 1'b1: Enable
1		RG_DSI_GPI1_PU	**DSI GPI1 pull-up control for PAD_TDN0** 1'b0: Disable 1'b1: Enable
0		RG_DSI_GPI0_PU	**DSI GPI0 pull-up control for PAD_TDP0** 1'b0: Disable 1'b1: Enable

10215078 DSI_GPI_CON2 **DSI GPI Control 1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													RG_DSI_GPI9_RDSEL		RG_DSI_GPI8_RDSEL	
Type													RW		RW	
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_DSI_GP		RG_DSI_GP		RG_DSI_GP		RG_DSI_GP		RG_DSI_GP		RG_DSI_GP		RG_DSI_GP		RG_DSI_GP	

	I7_RDSEL		I6_RDSEL		I5_RDSEL		I4_RDSEL		I3_RDSEL		I2_RDSEL		I1_RDSEL		I0_RDSEL	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:18		RG_DSI_GPI9_RD SEL	**Selects DSI GPI9 RX duty for PAD_TDN3** 1'b0: Disable 1'b1: Enable
17:16		RG_DSI_GPI8_RD SEL	**Selects DSI GPI8 RX duty for PAD_TDP3** 1'b0: Disable 1'b1: Enable
15:14		RG_DSI_GPI7_RD SEL	**Selects DSI GPI7 RX duty for PAD_TDN2** 1'b0: Disable 1'b1: Enable
13:12		RG_DSI_GPI6_RD SEL	**Selects DSI GPI6 RX duty for PAD_TDP2** 1'b0: Disable 1'b1: Enable
11:10		RG_DSI_GPI5_RD SEL	**Selects DSI GPI5 RX duty for PAD_TCN** 1'b0: Disable 1'b1: Enable
9:8		RG_DSI_GPI4_RD SEL	**Selects DSI GPI4 RX duty for PAD_TCP** 1'b0: Disable 1'b1: Enable
7:6		RG_DSI_GPI3_RD SEL	**Selects DSI GPI3 RX duty for PAD_TDN1** 1'b0: Disable 1'b1: Enable
5:4		RG_DSI_GPI2_RD SEL	**Selects DSI GPI2 RX duty for PAD_TDP1** 1'b0: Disable 1'b1: Enable
3:2		RG_DSI_GPI1_RD SEL	**Selects DSI GPI1 RX duty for PAD_TDN0** 1'b0: Disable 1'b1: Enable
1:0		RG_DSI_GPI0_RD SEL	**Selects DSI GPI0 RX duty for PAD_TDP0** 1'b0: Disable 1'b1: Enable

1021507C DSI_PHY_SEL **DSI MIPI TX PHY Lane Swap Selection** **00043210**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										MIPI_TX_LPRX_SEL				MIPI_TX_PHYC_SEL		
Type										RW				RW		
Reset										0	0	0		1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		MIPI_TX_PHY3_SEL				MIPI_TX_PHY2_SEL				MIPI_TX_PHY1_SEL				MIPI_TX_PHY0_SEL		
Type		RW				RW				RW				RW		
Reset		0	1	1		0	1	0		0	0	1		0	0	0

Bit(s)	Mnemonic	Name	Description
22:20		MIPI_TX_LPRX_SEL	**Selects MIPI TX PHY Lane RX**
18:16		MIPI_TX_PHYC_SEL	**Selects MIPI TX PHY Lane CK**
14:12		MIPI_TX_PHY3_SEL	**Selects MIPI TX PHY Lane 3**
10:8		MIPI_TX_PHY2_SEL	**Selects MIPI TX PHY Lane 2**
6:4		MIPI_TX_PHY1_SEL	**Selects MIPI TX PHY Lane 1**

Bit(s)	Mnemonic	Name	Description
2:0		MIPI_TX_PHY0_SEL	**Selects MIPI TX PHY Lane 0** 3'd0: DSI lane 0 3'd1: DSI lane 1 3'd2: DSI lane 2 3'd3: DSI lane 3 3'd4: DSI lane CK

10215080 DSI_SW_CTRL_EN **DSI Software Control Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MIPI_TX_SW_CTRL_EN
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		MIPI_TX_SW_CTRL_EN	**Enables DSI software control** 1'b0: Disable 1'b1: Enable

10215084 DSI_SW_CTRL_CON0 **DSI Software Control Configuration Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIPI_TX_SW_LNTC_HSTX_DATA								MIPI_TX_SW_LNTC_LPRX_EN	MIPI_TX_SW_LNTC_HSTX_RDY	MIPI_TX_SW_LNTC_HSTX_OE	MIPI_TX_SW_LNTC_HSTX_PRE_OE	MIPI_TX_SW_LNTC_LPTX_DN	MIPI_TX_SW_LNTC_LPTX_DP	MIPI_TX_SW_LNTC_LPTX_OE	MIPI_TX_SW_LNTC_LPTX_PRE_OE
Type	RW								RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8		MIPI_TX_SW_LNTC_HSTX_DATA	DSI CK Lane HSTX data
7		MIPI_TX_SW_LNTC_LPRX_EN	Enables DSI CK Lane LPRX
6		MIPI_TX_SW_LNTC_HSTX_RDY	DSI CK Lane HSTX ready
5		MIPI_TX_SW_LNT	DSI CK Lane HSTX OE

Bit(s)	Mnemonic	Name	Description
4		C_HSTX_OE MIPI_TX_SW_LNTC_HSTX_PRE_OE	DSI CK Lane HSTX Pre OE
3		MIPI_TX_SW_LNTC_LPTX_DN	DSI CK Lane LPTX DN
2		MIPI_TX_SW_LNTC_LPTX_DP	DSI CK Lane LPTX DP
1		MIPI_TX_SW_LNTC_LPTX_OE	DSI CK Lane LPTX OE
0		MIPI_TX_SW_LNTC_LPTX_PRE_OE	DSI CK Lane LPTX Pre OE

10215088 DSI_SW_CTRL_CON1 **DSI Software Control Configuration Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIPI_TX_SW_LNT3_LPRX_EN	MIPI_TX_SW_LNT3_HSTX_RDY	MIPI_TX_SW_LNT3_HSTX_OE	MIPI_TX_SW_LNT3_HSTX_PRE_OE	MIPI_TX_SW_LNT3_LPTX_DN	MIPI_TX_SW_LNT3_LPTX_DP	MIPI_TX_SW_LNT3_LPTX_OE	MIPI_TX_SW_LNT3_LPTX_PRE_OE	MIPI_TX_SW_LNT2_LPRX_EN	MIPI_TX_SW_LNT2_HSTX_RDY	MIPI_TX_SW_LNT2_HSTX_OE	MIPI_TX_SW_LNT2_HSTX_PRE_OE	MIPI_TX_SW_LNT2_LPTX_DN	MIPI_TX_SW_LNT2_LPTX_DP	MIPI_TX_SW_LNT2_LPTX_OE	MIPI_TX_SW_LNT2_LPTX_PRE_OE
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIPI_TX_SW_LNT1_LPRX_EN	MIPI_TX_SW_LNT1_HSTX_RDY	MIPI_TX_SW_LNT1_HSTX_OE	MIPI_TX_SW_LNT1_HSTX_PRE_OE	MIPI_TX_SW_LNT1_LPTX_DN	MIPI_TX_SW_LNT1_LPTX_DP	MIPI_TX_SW_LNT1_LPTX_OE	MIPI_TX_SW_LNT1_LPTX_PRE_OE	MIPI_TX_SW_LNT0_LPRX_EN	MIPI_TX_SW_LNT0_HSTX_RDY	MIPI_TX_SW_LNT0_HSTX_OE	MIPI_TX_SW_LNT0_HSTX_PRE_OE	MIPI_TX_SW_LNT0_LPTX_DN	MIPI_TX_SW_LNT0_LPTX_DP	MIPI_TX_SW_LNT0_LPTX_OE	MIPI_TX_SW_LNT0_LPTX_PRE_OE
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		MIPI_TX_SW_LNT3_LPRX_EN	Enables DSI Data Lane 3 LPRX
30		MIPI_TX_SW_LNT3_HSTX_RDY	DSI Data Lane 3 HSTX ready
29		MIPI_TX_SW_LNT3_HSTX_OE	DSI Data Lane 3 HSTX OE
28		MIPI_TX_SW_LNT3_HSTX_PRE_OE	DSI Data Lane 3 HSTX Pre OE
27		MIPI_TX_SW_LNT3_LPTX_DN	DSI Data Lane 3 LPTX DN
26		MIPI_TX_SW_LNT3_LPTX_DP	DSI Data Lane 3 LPTX DP
25		MIPI_TX_SW_LNT3_LPTX_OE	DSI Data Lane 3 LPTX OE
24		MIPI_TX_SW_LNT3_LPTX_PRE_OE	DSI Data Lane 3 LPTX Pre OE
23		MIPI_TX_SW_LNT2_LPRX_EN	Enables DSI Data Lane 2 LPRX
22		MIPI_TX_SW_LNT2_HSTX_RDY	DSI Data Lane 2 HSTX ready
21		MIPI_TX_SW_LNT2_HSTX_OE	DSI Data Lane 2 HSTX OE

Bit(s)	Mnemonic	Name	Description
20		MIPI_TX_SW_LNT2_HSTX_PRE_OE	DSI Data Lane 2 HSTX Pre OE
19		MIPI_TX_SW_LNT2_LPTX_DN	DSI Data Lane 2 LPTX DN
18		MIPI_TX_SW_LNT2_LPTX_DP	DSI Data Lane 2 LPTX DP
17		MIPI_TX_SW_LNT2_LPTX_OE	DSI Data Lane 2 LPTX OE
16		MIPI_TX_SW_LNT2_LPTX_PRE_OE	DSI Data Lane 2 LPTX Pre OE
15		MIPI_TX_SW_LNT1_LPRX_EN	Enables DSI Data Lane 1 LPRX
14		MIPI_TX_SW_LNT1_HSTX_RDY	DSI Data Lane 1 HSTX ready
13		MIPI_TX_SW_LNT1_HSTX_OE	DSI Data Lane 1 HSTX OE
12		MIPI_TX_SW_LNT1_HSTX_PRE_OE	DSI Data Lane 1 HSTX Pre OE
11		MIPI_TX_SW_LNT1_LPTX_DN	DSI Data Lane 1 LPTX DN
10		MIPI_TX_SW_LNT1_LPTX_DP	DSI Data Lane 1 LPTX DP
9		MIPI_TX_SW_LNT1_LPTX_OE	DSI Data Lane 1 LPTX OE
8		MIPI_TX_SW_LNT1_LPTX_PRE_OE	DSI Data Lane 1 LPTX Pre OE
7		MIPI_TX_SW_LNT0_LPRX_EN	Enables DSI Data Lane 0 LPRX
6		MIPI_TX_SW_LNT0_HSTX_RDY	DSI Data Lane 0 HSTX ready
5		MIPI_TX_SW_LNT0_HSTX_OE	DSI Data Lane 0 HSTX OE
4		MIPI_TX_SW_LNT0_HSTX_PRE_OE	DSI Data Lane 0 HSTX Pre OE
3		MIPI_TX_SW_LNT0_LPTX_DN	DSI Data Lane 0 LPTX DN
2		MIPI_TX_SW_LNT0_LPTX_DP	DSI Data Lane 0 LPTX DP
1		MIPI_TX_SW_LNT0_LPTX_OE	DSI Data Lane 0 LPTX OE
0		MIPI_TX_SW_LNT0_LPTX_PRE_OE	DSI Data Lane 0 LPTX Pre OE

1021508C DSI_SW_CTRL_CON2 — **DSI Software Control Configuration Register 0** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**MIPI_TX_SW_LNTD_HSTX_DATA**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
7:0		MIPI_TX_SW_LNTD_HSTX_DATA	DSI Data Lane 0~3 HSTX data

10215090 DSI_DBG_CON DSI Debug Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MIPI_TX_TST_CK_OUT_SEL	MIPI_TX_TST_CK_OUT_EN		MIPI_TX_GPIO_MODE_EN	MIPI_TX_DBG_OUT_EN	MIPI_TX_DBG_SEL			
Type								RW	RW		RW	RW	RW			
Reset								0	0		0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8		MIPI_TX_TST_CK_OUT_SEL	Selects MIPI clocks to frequency meter
7		MIPI_TX_TST_CK_OUT_EN	Enables MIPI clock output to frequency meter
5		MIPI_TX_GPIO_MODE_EN	Enables GPIO of MIPI TX pads
4		MIPI_TX_DBG_OUT_EN	Enables debug output of MIPI probe bus
3:0		MIPI_TX_DBG_SEL	Selects debug mux of MIPI debug bus

10215094 DSI_DBG_OUT DSI Debug Out Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIPI_TX_DBG_OUT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIPI_TX_DBG_OUT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MIPI_TX_DBG_OUT	MIPI debug bus out status

10215098 DSI_APB_ASYNC_STA DSI APB Async Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						MIPI_TX_APB_ASYNC_ERR_ADDR										MIPI_TX_APB_ASYNC_ERR
Type						RO										RO
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
10:1		MIPI_TX_APB_ASYNC_ERR_ADDR	MIPI APB async error address
0		MIPI_TX_APB_ASYNC_ERR	MIPI APB async error status

10215200 DSI_HS_BIST_CON CSI HS BIST Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														TX_HS_BIST_RDY_SEL		
Type														RW		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TX_HS_BIST_TM_ZERO								TX_HS_BIST_MODE		TX_HS_BIST_SKEW_MODE	TX_HS_BIST_LANE_NUM			
Type		RW								RW		RW	RW			
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
18:16		TX_HS_BIST_RDY_SEL	
14:8		TX_HS_BIST_TM_ZERO	
6:5		TX_HS_BIST_MODE	Selects BIST mode
4		TX_HS_BIST_SKEW_MODE	Selects skew mode
3:0		TX_HS_BIST_LANE_NUM	CSI BIST lane number

10215204 DSI_HS_BIST_PAT CSI HS BIST Pattern 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_HS_BIST_PAT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_HS_BIST_PAT															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		TX_HS_BIST_PAT	CSI BIST pattern

Module name: mipi_tx_config1 Base address: (+1021e000h)

Address	Name	Width	Register Function
1021E000	DSI_CON	32	DSI Configuration Register
1021E004	DSI_CLOCK_LANE	32	DSI Clock Lane Configuration Register
1021E008	DSI_DATA_LANE_0	32	DSI Data Lane 0 Configuration Register
1021E00C	DSI_DATA_LANE_1	32	DSI Data Lane 1 Configuration Register
1021E010	DSI_DATA_LANE_2	32	DSI Data Lane 2 Configuration Register
1021E014	DSI_DATA_LANE_3	32	DSI Data Lane 3 Configuration Register
1021E040	DSI_TOP_CON	32	DSI Top Configuration Register
1021E044	DSI_BG_CON	32	DSI BG Configuration Register
1021E050	DSI_PLL_CON0	32	DSI PLL Configuration 0 Register
1021E054	DSI_PLL_CON1	32	DSI PLL Configuration 1 Register
1021E058	DSI_PLL_CON2	32	DSI PLL Configuration 2 Register
1021E05C	DSI_PLL_CON3	32	DSI PLL Configuration 3 Register
1021E060	DSI_PLL_CHG	32	DSI PLL Charge Register
1021E064	DSI_PLL_TOP	32	DSI PLL Top Register
1021E068	DSI_PLL_PWR	32	DSI PLL Power Control Register
1021E070	DSI_GPI_CON0	32	DSI GPI Control 0 Register
1021E074	DSI_GPI_CON1	32	DSI GPI Control 1 Register
1021E078	DSI_GPI_CON2	32	DSI GPI Control 1 Register
1021E07C	DSI_PHY_SEL	32	DSI MIPI TX PHY Lane Swap Selection
1021E080	DSI_SW_CTRL_EN	32	DSI Software Control Enable Register
1021E084	DSI_SW_CTRL_CON0	32	DSI Software Control Configuration Register 0
1021E088	DSI_SW_CTRL_CON1	32	DSI Software Control Configuration Register 1
1021E08C	DSI_SW_CTRL_CON2	32	DSI Software Control Configuration Register 0
1021E090	DSI_DBG_CON	32	DSI Debug Control Register
1021E094	DSI_DBG_OUT	32	DSI Debug Out Register
1021E098	DSI_APB_ASYNC_STA	32	DSI APB Async Status Register
1021E200	DSI_HS_BIST_CON	32	CSI HS BIST Configuration
1021E204	DSI_HS_BIST_PAT	32	CSI HS BIST Pattern

1021E000 DSI_CON DSI Configuration Register 00001040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											RG_DSI_BIST_2D5G_PRESERVE 0					
Type											RW					
Reset											0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_DSI_BIST_DATA_SEL	RG_DSI_BIST_2D5G_SEL	RG_DSI_BIST_2D5G_EN	RG_DSI_DSICLK_FREQ_SEL	RG_DSI_PHYCLK_SEL		RG_DSI_CKG_IMINUS	RG_DSI_CKG_IPLUS	RG_DSI_LDO_VOD_EN	RG_DSI_LDO_LPF_EN	RG_DSI_LD_IDX_SEL		RG_DSI_BCLK_SEL		RG_DSI_CKG_LDOOUT_EN	RG_DSI_LDOCORE_EN
Type	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW		RW		RW	RW
Reset	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:16		RG_DSI_BIST_2D5G_PRESERVE0	**Reserved**
15		RG_DSI_BIST_DATA_SEL	**Selects for CSI BIST path**
14		RG_DSI_BIST_2D5G_SEL	**Selects analog 2D5G**
13		RG_DSI_BIST_2D5G_EN	**Enables analog 2D5G**
12		RG_DSI_DSICLK_FREQ_SEL	**Selects frequency of DSICLK** 1'b0: 2X of PHYCLK 1'b1: 1X of PHYCLK
11:10		RG_DSI_PHYCLK_SEL	**Selects phase of DSI PHYCLK** 2'b00: Align with BCLK 2'b01: Align with BCLKQ 2'b10: Align with BCLKB 2'b11: Align with BCLKQB
9		RG_DSI_CKG_IMINUS	**Decreases bias current for DSI clock generator** 1'b00: Normal 1'b01: -10%
8		RG_DSI_CKG_IPLUS	**Increases bias current for DSI clock generator** 1'b00: Normal 1'b01: +10%
7		RG_DSI_LDO_VOD_EN	**Enables voltage offset for DSI LDOs** 1'b0: Disable, LDO output 1.0V 1'b1: Enable, LDO output 1.1V
6		RG_DSI_LDO_LPF_EN	**Enables low-pass filter for DSI LDOs** 1'b0: Disable low-pass filter 1'b1: Enable low-pass filter
5:4		RG_DSI_LD_IDX_SEL	**Selects phase of DSI LD_IDX** 2'b00: Align with CKQ 2'b01: Align with CKB 2'b10: Align with CKQB 2'b11: Align with CK
3:2		RG_DSI_BCLK_SEL	**Selects phase of DSI byte clock** 2'b00: Align with CK 2'b01: Align with CKQ 2'b10: Align with CKB 2'b11: Align with CKQB
1		RG_DSI_CKG_LDOOUT_EN	**Enables LDO output for DSI clock generator** 1'b0: Disable 1'b1: Enable
0		RG_DSI_LDOCORE_EN	**Enables bias current for DSI LDOs** 1'b0: Disable 1'b1: Enable

1021E004 DSI_CLOCK DSI Clock Lane Configuration 00000802

LANE **Register**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_DSI_LNTC_RT_CODE						RG_DSI_LNTC_EO_SWAP	RG_DSI_LNTC_PN_SWAP	RG_DSI_LNTC_IMINUS	RG_DSI_LNTC_IPLUS	RG_DSI_LNTC_CKLANE_EN	RG_DSI_LNTC_LDOOUT_EN
Type					RW						RW	RW	RW	RW	RW	RW
Reset					1	0	0	0			0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
11:8		RG_DSI_LNTC_RT_CODE	**DSI clock lane HS impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
5		RG_DSI_LNTC_EO_SWAP	**Swaps even and odd bits for DSI clock lane** 1'b0: Normal 1'b1: Swap the even and odd bits for clock lane
4		RG_DSI_LNTC_PN_SWAP	**Swaps P/N pins for DSI clock lane** 1'b0: Normal 1'b1: Swap output P/N for clock lane
3		RG_DSI_LNTC_IMINUS	**Decreases bias current for DSI clock lane** 1'b00: Normal 1'b01: -10%
2		RG_DSI_LNTC_IPLUS	**Increases bias current for DSI clock lane** 1'b00: Normal 1'b01: +10%
1		RG_DSI_LNTC_CKLANE_EN	**Selects clock source for clock lane** 1'b0: In phase clock for data lane 1'b1: Quadrature phase clock for clock lane
0		RG_DSI_LNTC_LDOOUT_EN	**Enables LDO output for DSI clock lane** 1'b0: Disable 1'b1: Enable

1021E008 DSI_DATA_LANE_0 **DSI Data Lane 0 Configuration Register** **00000800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_DSI_LNTo_RT_CODE						RG_DSI_LNTo_EO_SWAP	RG_DSI_LNTo_PN_SWAP	RG_DSI_LNTo_IMINUS	RG_DSI_LNTo_IPLUS	RG_DSI_LNTo_CKLANE_EN	RG_DSI_LNTo_LDOOUT_EN
Type					RW						RW	RW	RW	RW	RW	RW
Reset					1	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
11:8		RG_DSI_LNT0_RT_CODE	**DSI Data Lane 0 HS impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
5		RG_DSI_LNT0_EO_SWAP	**Swaps even and odd bits for DSI Data Lane 0** 1'b0: Normal 1'b1: Swap even and odd bits for Data Lane 0
4		RG_DSI_LNT0_PN_SWAP	**Swaps P/N pins for DSI Data Lane 0** 1'b0: Normal 1'b1: Swap output P/N for Data Lane 0
3		RG_DSI_LNT0_IMINUS	**Decreases bias current for DSI Data Lane 0** 1'b00: Normal 1'b01: -10%
2		RG_DSI_LNT0_IP LUS	**Increases bias current for DSI Data Lane 0** 1'b00: Normal 1'b01: +10%
1		RG_DSI_LNT0_CK LANE_EN	**Select clock source for DSI Data Lane 0** 1'b0: In phase clock for data lane 1'b1: Quadrature phase clock for clock lane
0		RG_DSI_LNT0_LD OOUT_EN	**Enables LDO output for DSI Data Lane 0** 1'b0: Disable 1'b1: Enable

1021E00C DSI_DATA_LANE_1 **DSI Data Lane 1 Configuration Register** **00000800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_DSI_LNT1_RT_CODE						RG_DSI_LNT1_EO_SWAP	RG_DSI_LNT1_PN_SWAP	RG_DSI_LNT1_IMINUS	RG_DSI_LNT1_IPLUS	RG_DSI_LNT1_CKLANE_EN	RG_DSI_LNT1_LDOOUT_EN
Type					RW						RW	RW	RW	RW	RW	RW
Reset					1	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:8		RG_DSI_LNT1_RT_CODE	**DSI Data Lane 1 HS impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
5		RG_DSI_LNT1_EO_SWAP	**Swaps even and odd bits for DSI Data Lane 1** 1'b0: Normal 1'b1: Swap even and odd bits for Data Lane 1
4		RG_DSI_LNT1_PN_SWAP	**Swaps P/N pins for DSI Data Lane 1** 1'b0: Normal 1'b1: Swap output P/N for Data Lane 1
3		RG_DSI_LNT1_IMINUS	**Decreases bias current for DSI Data Lane 1** 1'b00: Normal 1'b01: -10%
2		RG_DSI_LNT1_IP LUS	**Increases bias current for DSI Data Lane 1** 1'b00: Normal 1'b01: +10%
1		RG_DSI_LNT1_CK	**Selects clock source for DSI Data Lane 1**

Bit(s)	Mnemonic	Name	Description
		LANE_EN	1'b0: In phase clock for data lane 1'b1: Quadrature phase clock for clock lane
0		RG_DSI_LNT1_LDOOUT_EN	**Enables LDO output for DSI Data Lane 1** 1'b0: Disable 1'b1: Enable

1021E010 DSI_DATA_LANE_2 DSI Data Lane 2 Configuration Register 00000800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_DSI_LNT2_RT_CODE						RG_DSI_LNT2_EO_SWAP	RG_DSI_LNT2_PN_SWAP	RG_DSI_LNT2_IMINUS	RG_DSI_LNT2_IPLUS	RG_DSI_LNT2_CKLANE_EN	RG_DSI_LNT2_LDOOUT_EN
Type					RW						RW	RW	RW	RW	RW	RW
Reset					1	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:8		RG_DSI_LNT2_RT_CODE	**DSI Data Lane 2 HS impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
5		RG_DSI_LNT2_EO_SWAP	**Swaps even and odd bits for DSI Data Lane 2** 1'b0: Normal 1'b1: Swap even and odd bits for Data Lane 2
4		RG_DSI_LNT2_PN_SWAP	**Swaps P/N pins for DSI Data Lane 2** 1'b0: Normal 1'b1: Swap output P/N for Data Lane 2
3		RG_DSI_LNT2_IMINUS	**Decreases bias current for DSI Data Lane 2** 1'b00: Normal 1'b01: -10%
2		RG_DSI_LNT2_IPLUS	**Increases bias current for DSI Data Lane 2** 1'b00: Normal 1'b01: +10%
1		RG_DSI_LNT2_CKLANE_EN	**Selects clock source for DSI Data Lane 2** 1'b0: In phase clock for data lane 1'b1: Quadrature phase clock for clock lane
0		RG_DSI_LNT2_LDOOUT_EN	**Enables LDO output for DSI Data Lane 2** 1'b0: Disable 1'b1: Enable

1021E014 DSI_DATA_LANE_3 DSI Data Lane 3 Configuration Register 00000800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name					RG_DSI_LNT3_RT_CODE						RG_DSI_LNT3_EO_SWAP	RG_DSI_LNT3_PN_SWAP	RG_DSI_LNT3_IMINUS	RG_DSI_LNT3_IPLUS	RG_DSI_LNT3_CKLANE_EN	RG_DSI_LNT3_LDOOUT_EN
Type					RW						RW	RW	RW	RW	RW	RW
Reset					1	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:8		RG_DSI_LNT3_RT_CODE	**DSI Data Lane 3 HS impedance control code** 4'b0000: Maximum impedance 4'b1111: Minimum impedance
5		RG_DSI_LNT3_EO_SWAP	**Swaps even and odd bits for DSI Data Lane 3** 1'b0: Normal 1'b1: Swap even and odd bits for Data Lane 3
4		RG_DSI_LNT3_PN_SWAP	**Swaps P/N pins for DSI Data Lane 3** 1'b0: Normal 1'b1: Swap the output P/N for Data Lane 3
3		RG_DSI_LNT3_IMINUS	**Decreases bias current for DSI Data Lane 3** 1'b00: Normal 1'b01: -10%
2		RG_DSI_LNT3_IP LUS	**Increases bias current for DSI Data Lane 3** 1'b00: Normal 1'b01: +10%
1		RG_DSI_LNT3_CKLANE_EN	**Selects clock source for DSI Data Lane 3** 1'b0: In phase clock for data lane 1'b1: Quadrature phase clock for clock lane
0		RG_DSI_LNT3_LDOOUT_EN	**Enables the LDO output for DSI Data Lane 3** 1'b0: Disable 1'b1: Enable

1021E040 DSI_TOP_CON **DSI Top Configuration Register** **0000F800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_DSI_PRESERVE1				RG_DSI_PAD_TIE_LOW_EN	RG_DSI_LNT_AIO_SEL			RG_DSI_PRESERVE0				RG_DSI_LNT_TESTMODE_EN			
Type	RW				RW	RW			RW				RW			
Reset	1	1	1	1	1	0	0	0	0	0	0	0	0			

Bit(s)	Mnemonic	Name	Description
15:12		RG_DSI_PRESERVE1	**DSI preserved registers**
11		RG_DSI_PAD_TIE_LOW_EN	**Enables tie-low resistors for DSI 10 pads** 1'b0: Floating or depends on line driver. 1'b1: Tie to ground with 20k ohm resistors
10:8		RG_DSI_LNT_AIO_SEL	**Selects analog debug output** 3'b000: Output VREF 0.2V 3'b001: Output VREF 0.32V

Bit(s)	Mnemonic	Name	Description
			3'b010: Output VREF 0.4V 3'b011: Output VREF 0.72V 3'b100: Output VREF 0.86V 3'b101: Output VREF 1.2V 3'b110: Output VCCK09 3'b111: Output PLL_TST
7:4		RG_DSI_PRESERV E0	**DSI preserved registers**
3		RG_DSI_LNT_TES TMODE_EN	**Enables analog test mode in DSI** 1'b0: Disable 1'b1: Enable

1021E044 DSI_BG_CON **DSI BG Configuration Register** **01249240**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								RG_DSI_V03_SEL			RG_DSI_V035_SEL			RG_DSI_V07_SEL		
Type								RW			RW			RW		
Reset								1	0	0	1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_DSI_V075_SEL			RG_DSI_V04_SEL			RG_DSI_V10_SEL			RG_DSI_V12_SEL						RG_DSI_BG_CORE_EN
Type	RW			RW			RW			RW						RW
Reset	1	0	0	1	0	0	1	0	0	1	0	0				0

Bit(s)	Mnemonic	Name	Description
24:22		RG_DSI_V03_SEL	**Selects 0.3V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
21:19		RG_DSI_V035_SE L	**Selects 0.35V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
18:16		RG_DSI_V07_SEL	**Selects 0.7V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
15:13		RG_DSI_V075_SE L	**Selects 0.75V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
12:10		RG_DSI_V04_SEL	**Selects 0.4V output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
9:7		RG_DSI_V10_SEL	**Selects AVDD10 output voltage** 3'b000: Minimum voltage 3'b100: Typical voltage 3'b111: Maximum voltage
6:4		RG_DSI_V12_SEL	**Selects 1.2V output voltage** 3'b0000: Minimum voltage

Bit(s)	Mnemonic	Name	Description
			3'b0100: Typical voltage 3'b0111: Maximum voltage
0		RG_DSI_BG_CORE_EN	**Enables R-string for reference voltage** 1'b0: Power off 1'b1: Enable R-string voltages

1021E050 DSI_PLL_CON0 **DSI PLL Configuration 0 Register** **F0002010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_DSI_MPPLL_PRESERV_E1				RG_DSI_MPPLL_PRESERV_E0											
Type	RW				RW											
Reset	1	1	1	1	0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_DSI_MPPLL_PLLOUT_EN	RG_DSI_MPPLL_S2QDIV		RG_DSI_MPPLL_VOD_EN		RG_DSI_MPPLL_MONREF_EN	RG_DSI_MPPLL_MONVC_EN		RG_DSI_MPPLL_POSDIV			RG_DSI_MPPLL_PREDIV			RG_DSI_MPPLL_PLL_EN
Type		RW	RW		RW		RW	RW		RW			RW			RW
Reset		0	1	0	0		0	0		0	0	1	0	0		0

Bit(s)	Mnemonic	Name	Description
31:28		RG_DSI_MPPLL_PRESERVE1	**DSI MPPLL preserved registers**
27:24		RG_DSI_MPPLL_PRESERVE0	**DSI MPPLL preserved registers**
14		RG_DSI_MPPLL_PLLOUT_EN	**Enables PLL output for LVDS** 1'b0: Disable 1'b1: Enable
13:12		RG_DSI_MPPLL_S2QDIV	**Selects divisor for the quadrature phase divider** 2'b00: Gate the output to ground 2'b01: Divided by 2 2'b1x: Divided by 4
11		RG_DSI_MPPLL_VOD_EN	**Overdrive LDO** 1'b0: Disable 1'b1: Enable
9		RG_DSI_MPPLL_MONREF_EN	**Monitor PLL reference clock** 1'b0: Disable 1'b1: Enable
8		RG_DSI_MPPLL_MONVC_EN	**Monitor VCO controlled voltage** 1'b0: Disable 1'b1: Enable
6:4		RG_DSI_MPPLL_POSDIV	**PLL post divide ratio** 3'b000: /1 3'b001: /2 3'b010: /4 3'b011: /8 3'b100: /16 Others: Clock gating
3:2		RG_DSI_MPPLL_PREDIV	**Pre divide ratio** 2'b00: /1 2'b01: /2 2'b1x: /4

Bit(s)	Mnemonic	Name	Description
0		RG_DSI_MPPLL_PLL_EN	**Enables MIPI PLL** 1'b0: Power down 1'b1: Enable

1021E054 DSI_PLL_CON1 **DSI PLL Configuration 1 Register** **00000003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_DSI_MPPLL_SDM_SSC_PRD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_DSI_MPPLL_SDM_SSC_EN	RG_DSI_MPPLL_SDM_SSC_PH_INIT	RG_DSI_MPPLL_SDM_FRA_EN
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Mnemonic	Name	Description
31:16		RG_DSI_MPPLL_SDM_SSC_PRD	**SDM SSC period** 16'd0: Min. 16'd65536: Max.
2		RG_DSI_MPPLL_SDM_SSC_EN	**Enables SDM SSC** 1'b0: Disable 1'b1: Enable
1		RG_DSI_MPPLL_SDM_SSC_PH_INIT	**Initializes SDM SSC phase** 1'b0: Upward 1'b1: Downward
0		RG_DSI_MPPLL_SDM_FRA_EN	**Enables SDM PLL fractional mode** 1'b0: Integer mode 1'b1: Fractional mode

1021E058 DSI_PLL_CON2 **DSI PLL Configuration 2 Register** **50000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_DSI_MPPLL_SDM_PCW														
Type		RW														
Reset		1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_DSI_MPPLL_SDM_PCW															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		RG_DSI_MPPLL_SDM_PCW	**Feedback divide ratio** 8-bit integer + 24-bit fractional

1021E05C DSI_PLL_CON3 **DSI PLL Configuration 3 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_DSI_MPPLL_SDM_SSC_DELTA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_DSI_MPPLL_SDM_SSC_DELTA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		RG_DSI_MPPLL_SDM_SSC_DELTA	**SDM SSC amplitude** 16'd0: Min. 16'd65536: Max.
15:0		RG_DSI_MPPLL_SDM_SSC_DELTA1	**SDM SSC amplitude 1** 16'd0: Min. 16'd65536: Max.

1021E060 DSI_PLL_CHG **DSI PLL Charge Register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_DSI_MPPLL_SDM_PCW_CHG
Type																RW
Reset																1

Bit(s)	Mnemonic	Name	Description
0		RG_DSI_MPPLL_SDM_PCW_CHG	Trigger signal to update divide ratio of feedback divider

1021E064 DSI_PLL_TOP **DSI PLL Top Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_DSI_MPPLL_TSTSEL		RG_DSI_MPPLL_TSTCK_EN	RG_DSI_MPPLL_TST_EN

Type													RW		RW	RW
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:2		RG_DSI_MPPLL_TSTSEL	**Selects MIPI PLL test mode** [0]: Used for RG_DSI_MPPLL_MONCK_EN [1]: Not used
1		RG_DSI_MPPLL_TSTCK_EN	**Enables MIPI PLL test clock** 1'b0: Disable 1'b1: Enable
0		RG_DSI_MPPLL_TST_EN	**Enables MIPI PLL test** 1'b0: Disable 1'b1: Enable

1021E068 DSI_PLL_PWR DSI PLL Power Control Register 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								AD_DSI_MPPLL_SDM_PWR_ACK							DA_DSI_MPPLL_SDM_ISO_EN	DA_DSI_MPPLL_SDM_PWR_ON
Type								RU							RW	RW
Reset								0							1	0

Bit(s)	Mnemonic	Name	Description
8		AD_DSI_MPPLL_SDM_PWR_ACK	**Acknowledges PLL power-on** 1'b0: No effect 1'b1: Power-on ack
1		DA_DSI_MPPLL_SDM_ISO_EN	**Enables PLL isolation** 1'b0: Disable 1'b1: Enable
0		DA_DSI_MPPLL_SDM_PWR_ON	**Controls PLL power-on** 1'b0: Power-off 1'b1: Power-on

1021E070 DSI_GPI_CON DSI GPI Control 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							RG_DSI_GPI9_SMT	RG_DSI_GPI8_SMT	RG_DSI_GPI7_SMT	RG_DSI_GPI6_SMT	RG_DSI_GPI5_SMT	RG_DSI_GPI4_SMT	RG_DSI_GPI3_SMT	RG_DSI_GPI2_SMT	RG_DSI_GPI1_SMT	RG_DSI_GPI0_SMT
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_DSI_G	RG_DSI_G	RG_DSI_G	RG_DSI_G	RG_DSI_G	RG_DSI_G	RG_DSI_G	RG_DSI_G	RG_DSI_G	RG_DSI_G

							PI9_IES	PI8_IES	PI7_IES	PI6_IES	PI5_IES	PI4_IES	PI3_IES	PI2_IES	PI1_IES	PI0_IES
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25		RG_DSI_GPI9_SMT	**DSI GPI9 Schmitt trigger for PAD_TDN3** 1'b0: Disable 1'b1: Enable
24		RG_DSI_GPI8_SMT	**DSI GPI8 Schmitt trigger for PAD_TDP3** 1'b0: Disable 1'b1: Enable
23		RG_DSI_GPI7_SMT	**DSI GPI7 Schmitt trigger for PAD_TDN2** 1'b0: Disable 1'b1: Enable
22		RG_DSI_GPI6_SMT	**DSI GPI6 Schmitt trigger for PAD_TDP2** 1'b0: Disable 1'b1: Enable
21		RG_DSI_GPI5_SMT	**DSI GPI5 Schmitt trigger for PAD_TCN** 1'b0: Disable 1'b1: Enable
20		RG_DSI_GPI4_SMT	**DSI GPI4 Schmitt trigger for PAD_TCP** 1'b0: Disable 1'b1: Enable
19		RG_DSI_GPI3_SMT	**DSI GPI3 Schmitt trigger for PAD_TDN1** 1'b0: Disable 1'b1: Enable
18		RG_DSI_GPI2_SMT	**DSI GPI2 Schmitt trigger for PAD_TDP1** 1'b0: Disable 1'b1: Enable
17		RG_DSI_GPI1_SMT	**DSI GPI1 Schmitt trigger for PAD_TDN0** 1'b0: Disable 1'b1: Enable
16		RG_DSI_GPI0_SMT	**DSI GPI0 Schmitt trigger for PAD_TDP0** 1'b0: Disable 1'b1: Enable
9		RG_DSI_GPI9_IES	**Enables DSI GPI9 input buffer for PAD_TDN3** 1'b0: Disable 1'b1: Enable
8		RG_DSI_GPI8_IES	**Enables DSI GPI8 input buffer for PAD_TDP3** 1'b0: Disable 1'b1: Enable
7		RG_DSI_GPI7_IES	**Enables DSI GPI7 input buffer for PAD_TDN2** 1'b0: Disable 1'b1: Enable
6		RG_DSI_GPI6_IES	**Enables DSI GPI6 input buffer for PAD_TDP2** 1'b0: Disable 1'b1: Enable
5		RG_DSI_GPI5_IES	**Enables DSI GPI5 input buffer for PAD_TCN** 1'b0: Disable 1'b1: Enable
4		RG_DSI_GPI4_IES	**Enables DSI GPI4 input buffer for PAD_TCP** 1'b0: Disable 1'b1: Enable
3		RG_DSI_GPI3_IES	**Enables DSI GPI3 input buffer for PAD_TDN1**

Bit(s)	Mnemonic	Name	Description
			1'b0: Disable 1'b1: Enable
2		RG_DSI_GPI2_IE S	**Enables DSI GPI2 input buffer for PAD_TDP1** 1'b0: Disable 1'b1: Enable
1		RG_DSI_GPI1_IE S	**Enables DSI GPI1 input buffer for PAD_TDN0** 1'b0: Disable 1'b1: Enable
0		RG_DSI_GPI0_IE S	**Enables DSI GPI0 input buffer for PAD_TDP0** 1'b0: Disable 1'b1: Enable

1021E074 DSI_GPI_CON1 **DSI GPI Control 1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							RG_DSI_GPI9_PD	RG_DSI_GPI8_PD	RG_DSI_GPI7_PD	RG_DSI_GPI6_PD	RG_DSI_GPI5_PD	RG_DSI_GPI4_PD	RG_DSI_GPI3_PD	RG_DSI_GPI2_PD	RG_DSI_GPI1_PD	RG_DSI_GPI0_PD
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_DSI_GPI9_PU	RG_DSI_GPI8_PU	RG_DSI_GPI7_PU	RG_DSI_GPI6_PU	RG_DSI_GPI5_PU	RG_DSI_GPI4_PU	RG_DSI_GPI3_PU	RG_DSI_GPI2_PU	RG_DSI_GPI1_PU	RG_DSI_GPI0_PU
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25		RG_DSI_GPI9_PD	**DSI GPI9 pull-down control for PAD_TDN3** 1'b0: Disable 1'b1: Enable
24		RG_DSI_GPI8_PD	**DSI GPI8 pull-down control for PAD_TDP3** 1'b0: Disable 1'b1: Enable
23		RG_DSI_GPI7_PD	**DSI GPI7 pull-down control for PAD_TDN2** 1'b0: Disable 1'b1: Enable
22		RG_DSI_GPI6_PD	**DSI GPI6 pull-down control for PAD_TDP2** 1'b0: Disable 1'b1: Enable
21		RG_DSI_GPI5_PD	**DSI GPI5 pull-down control for PAD_TCN** 1'b0: Disable 1'b1: Enable
20		RG_DSI_GPI4_PD	**DSI GPI4 pull-down control for PAD_TCP** 1'b0: Disable 1'b1: Enable
19		RG_DSI_GPI3_PD	**DSI GPI3 pull-down control for PAD_TDN1** 1'b0: Disable 1'b1: Enable
18		RG_DSI_GPI2_PD	**DSI GPI2 pull-down control for PAD_TDP1** 1'b0: Disable

Bit(s)	Mnemonic	Name	Description
			1'b1: Enable
17		RG_DSI_GPI1_PD	**DSI GPI1 pull-down control for PAD_TDN0** 1'b0: Disable 1'b1: Enable
16		RG_DSI_GPI0_PD	**DSI GPI0 pull-down control for PAD_TDP0** 1'b0: Disable 1'b1: Enable
9		RG_DSI_GPI9_PU	**DSI GPI9 pull-up control for PAD_TDN3** 1'b0: Disable 1'b1: Enable
8		RG_DSI_GPI8_PU	**DSI GPI8 pull-up control for PAD_TDP3** 1'b0: Disable 1'b1: Enable
7		RG_DSI_GPI7_PU	**DSI GPI7 pull-up control for PAD_TDN2** 1'b0: Disable 1'b1: Enable
6		RG_DSI_GPI6_PU	**DSI GPI6 pull-up control for PAD_TDP2** 1'b0: Disable 1'b1: Enable
5		RG_DSI_GPI5_PU	**DSI GPI5 pull-up control for PAD_TCN** 1'b0: Disable 1'b1: Enable
4		RG_DSI_GPI4_PU	**DSI GPI4 pull-up control for PAD_TCP** 1'b0: Disable 1'b1: Enable
3		RG_DSI_GPI3_PU	**DSI GPI3 pull-up control for PAD_TDN1** 1'b0: Disable 1'b1: Enable
2		RG_DSI_GPI2_PU	**DSI GPI2 pull-up control for PAD_TDP1** 1'b0: Disable 1'b1: Enable
1		RG_DSI_GPI1_PU	**DSI GPI1 pull-up control for PAD_TDN0** 1'b0: Disable 1'b1: Enable
0		RG_DSI_GPI0_PU	**DSI GPI0 pull-up control for PAD_TDP0** 1'b0: Disable 1'b1: Enable

1021E078 DSI_GPI_CON2 **DSI GPI Control 1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													RG_DSI_GPI9_RDSEL		RG_DSI_GPI8_RDSEL	
Type													RW		RW	
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_DSI_GPI7_RDSEL		RG_DSI_GPI6_RDSEL		RG_DSI_GPI5_RDSEL		RG_DSI_GPI4_RDSEL		RG_DSI_GPI3_RDSEL		RG_DSI_GPI2_RDSEL		RG_DSI_GPI1_RDSEL		RG_DSI_GPI0_RDSEL	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
19:18		RG_DSI_GPI9_RD SEL	**Selects DSI GPI9 RX duty for PAD_TDN3** 1'b0: Disable 1'b1: Enable
17:16		RG_DSI_GPI8_RD SEL	**Selects DSI GPI8 RX duty for PAD_TDP3** 1'b0: Disable 1'b1: Enable
15:14		RG_DSI_GPI7_RD SEL	**Selects DSI GPI7 RX duty for PAD_TDN2** 1'b0: Disable 1'b1: Enable
13:12		RG_DSI_GPI6_RD SEL	**Selects DSI GPI6 RX duty for PAD_TDP2** 1'b0: Disable 1'b1: Enable
11:10		RG_DSI_GPI5_RD SEL	**Selects DSI GPI5 RX duty for PAD_TCN** 1'b0: Disable 1'b1: Enable
9:8		RG_DSI_GPI4_RD SEL	**Selects DSI GPI4 RX duty for PAD_TCP** 1'b0: Disable 1'b1: Enable
7:6		RG_DSI_GPI3_RD SEL	**Selects DSI GPI3 RX duty for PAD_TDN1** 1'b0: Disable 1'b1: Enable
5:4		RG_DSI_GPI2_RD SEL	**Selects DSI GPI2 RX duty for PAD_TDP1** 1'b0: Disable 1'b1: Enable
3:2		RG_DSI_GPI1_RD SEL	**Selects DSI GPI1 RX duty for PAD_TDN0** 1'b0: Disable 1'b1: Enable
1:0		RG_DSI_GPI0_RD SEL	**Selects DSI GPI0 RX duty for PAD_TDP0** 1'b0: Disable 1'b1: Enable

1021E07C DSI_PHY_SEL **DSI MIPI TX PHY Lane Swap Selection** **00043210**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										MIPI_TX_LPRX_SEL				MIPI_TX_PHYC_SEL		
Type										RW				RW		
Reset										0	0	0		1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		MIPI_TX_PHY3_SEL				MIPI_TX_PHY2_SEL				MIPI_TX_PHY1_SEL				MIPI_TX_PHY0_SEL		
Type		RW				RW				RW				RW		
Reset		0	1	1		0	1	0		0	0	1		0	0	0

Bit(s)	Mnemonic	Name	Description
22:20		MIPI_TX_LPRX_SEL	**Selects MIPI TX PHY Lane RX**
18:16		MIPI_TX_PHYC_SEL	**Selects MIPI TX PHY Lane CK**
14:12		MIPI_TX_PHY3_SEL	**Selects MIPI TX PHY Lane 3**
10:8		MIPI_TX_PHY2_SEL	**Selects MIPI TX PHY Lane 2**
6:4		MIPI_TX_PHY1_SEL	**Selects MIPI TX PHY Lane 1**
2:0		MIPI_TX_PHY0_SEL	**Selects MIPI TX PHY Lane 0** 3'd0: DSI lane 0 3'd1: DSI lane 1 3'd2: DSI lane 2

Bit(s)	Mnemonic	Name	Description
			3'd3: DSI lane 3 3'd4: DSI lane CK

1021E080 DSI_SW_CTRL_EN **DSI Software Control Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**MIPI_TX_SW_CTRL_EN**
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		MIPI_TX_SW_CTRL_EN	**Enables DSI software control** 1'b0: Disable 1'b1: Enable

1021E084 DSI_SW_CTRL_CON0 **DSI Software Control Configuration Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MIPI_TX_SW_LNTC_HSTX_DATA**								**MIPI_TX_SW_LNTC_LPRX_EN**	**MIPI_TX_SW_LNTC_HSTX_RDY**	**MIPI_TX_SW_LNTC_HSTX_OE**	**MIPI_TX_SW_LNTC_HSTX_PRE_OE**	**MIPI_TX_SW_LNTC_LPTX_DN**	**MIPI_TX_SW_LNTC_LPTX_DP**	**MIPI_TX_SW_LNTC_LPTX_OE**	**MIPI_TX_SW_LNTC_LPTX_PRE_OE**
Type	RW								RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8		MIPI_TX_SW_LNTC_HSTX_DATA	DSI CK Lane HSTX data
7		MIPI_TX_SW_LNTC_LPRX_EN	Enables DSI CK Lane LPRX
6		MIPI_TX_SW_LNTC_HSTX_RDY	DSI CK Lane HSTX ready
5		MIPI_TX_SW_LNTC_HSTX_OE	DSI CK Lane HSTX OE
4		MIPI_TX_SW_LNTC_HSTX_PRE_OE	DSI CK Lane HSTX Pre OE
3		MIPI_TX_SW_LNT	DSI CK Lane LPTX DN

Bit(s)	Mnemonic	Name	Description
2		C_LPTX_DN MIPI_TX_SW_LNTC_LPTX_DP	DSI CK Lane LPTX DP
1		MIPI_TX_SW_LNTC_LPTX_OE	DSI CK Lane LPTX OE
0		MIPI_TX_SW_LNTC_LPTX_PRE_OE	DSI CK Lane LPTX Pre OE

1021E088 DSI_SW_CTRL_CON1 **DSI Software Control Configuration Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIPI_TX_SW_LNT3_LPRX_EN	MIPI_TX_SW_LNT3_HSTX_RDY	MIPI_TX_SW_LNT3_HSTX_OE	MIPI_TX_SW_LNT3_HSTX_PRE_OE	MIPI_TX_SW_LNT3_LPTX_DN	MIPI_TX_SW_LNT3_LPTX_DP	MIPI_TX_SW_LNT3_LPTX_OE	MIPI_TX_SW_LNT3_LPTX_PRE_OE	MIPI_TX_SW_LNT2_LPRX_EN	MIPI_TX_SW_LNT2_HSTX_RDY	MIPI_TX_SW_LNT2_HSTX_OE	MIPI_TX_SW_LNT2_HSTX_PRE_OE	MIPI_TX_SW_LNT2_LPTX_DN	MIPI_TX_SW_LNT2_LPTX_DP	MIPI_TX_SW_LNT2_LPTX_OE	MIPI_TX_SW_LNT2_LPTX_PRE_OE
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIPI_TX_SW_LNT1_LPRX_EN	MIPI_TX_SW_LNT1_HSTX_RDY	MIPI_TX_SW_LNT1_HSTX_OE	MIPI_TX_SW_LNT1_HSTX_PRE_OE	MIPI_TX_SW_LNT1_LPTX_DN	MIPI_TX_SW_LNT1_LPTX_DP	MIPI_TX_SW_LNT1_LPTX_OE	MIPI_TX_SW_LNT1_LPTX_PRE_OE	MIPI_TX_SW_LNT0_LPRX_EN	MIPI_TX_SW_LNT0_HSTX_RDY	MIPI_TX_SW_LNT0_HSTX_OE	MIPI_TX_SW_LNT0_HSTX_PRE_OE	MIPI_TX_SW_LNT0_LPTX_DN	MIPI_TX_SW_LNT0_LPTX_DP	MIPI_TX_SW_LNT0_LPTX_OE	MIPI_TX_SW_LNT0_LPTX_PRE_OE
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		MIPI_TX_SW_LNT3_LPRX_EN	Enables DSI Data Lane 3 LPRX
30		MIPI_TX_SW_LNT3_HSTX_RDY	DSI Data Lane 3 HSTX ready
29		MIPI_TX_SW_LNT3_HSTX_OE	DSI Data Lane 3 HSTX OE
28		MIPI_TX_SW_LNT3_HSTX_PRE_OE	DSI Data Lane 3 HSTX Pre OE
27		MIPI_TX_SW_LNT3_LPTX_DN	DSI Data Lane 3 LPTX DN
26		MIPI_TX_SW_LNT3_LPTX_DP	DSI Data Lane 3 LPTX DP
25		MIPI_TX_SW_LNT3_LPTX_OE	DSI Data Lane 3 LPTX OE
24		MIPI_TX_SW_LNT3_LPTX_PRE_OE	DSI Data Lane 3 LPTX Pre OE
23		MIPI_TX_SW_LNT2_LPRX_EN	Enables DSI Data Lane 2 LPRX
22		MIPI_TX_SW_LNT2_HSTX_RDY	DSI Data Lane 2 HSTX ready
21		MIPI_TX_SW_LNT2_HSTX_OE	DSI Data Lane 2 HSTX OE
20		MIPI_TX_SW_LNT2_HSTX_PRE_OE	DSI Data Lane 2 HSTX Pre OE
19		MIPI_TX_SW_LNT2_LPTX_DN	DSI Data Lane 2 LPTX DN
18		MIPI_TX_SW_LNT	DSI Data Lane 2 LPTX DP

Bit(s)	Mnemonic	Name	Description
		2_LPTX_DP	
17		MIPI_TX_SW_LNT 2_LPTX_OE	DSI Data Lane 2 LPTX OE
16		MIPI_TX_SW_LNT 2_LPTX_PRE_OE	DSI Data Lane 2 LPTX Pre OE
15		MIPI_TX_SW_LNT 1_LPRX_EN	Enables DSI Data Lane 1 LPRX
14		MIPI_TX_SW_LNT 1_HSTX_RDY	DSI Data Lane 1 HSTX ready
13		MIPI_TX_SW_LNT 1_HSTX_OE	DSI Data Lane 1 HSTX OE
12		MIPI_TX_SW_LNT 1_HSTX_PRE_OE	DSI Data Lane 1 HSTX Pre OE
11		MIPI_TX_SW_LNT 1_LPTX_DN	DSI Data Lane 1 LPTX DN
10		MIPI_TX_SW_LNT 1_LPTX_DP	DSI Data Lane 1 LPTX DP
9		MIPI_TX_SW_LNT 1_LPTX_OE	DSI Data Lane 1 LPTX OE
8		MIPI_TX_SW_LNT 1_LPTX_PRE_OE	DSI Data Lane 1 LPTX Pre OE
7		MIPI_TX_SW_LNT 0_LPRX_EN	Enables DSI Data Lane 0 LPRX
6		MIPI_TX_SW_LNT 0_HSTX_RDY	DSI Data Lane 0 HSTX ready
5		MIPI_TX_SW_LNT 0_HSTX_OE	DSI Data Lane 0 HSTX OE
4		MIPI_TX_SW_LNT 0_HSTX_PRE_OE	DSI Data Lane 0 HSTX Pre OE
3		MIPI_TX_SW_LNT 0_LPTX_DN	DSI Data Lane 0 LPTX DN
2		MIPI_TX_SW_LNT 0_LPTX_DP	DSI Data Lane 0 LPTX DP
1		MIPI_TX_SW_LNT 0_LPTX_OE	DSI Data Lane 0 LPTX OE
0		MIPI_TX_SW_LNT 0_LPTX_PRE_OE	DSI Data Lane 0 LPTX Pre OE

1021E08C DSI_SW_CTRL_CON2 **DSI Software Control Configuration Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MIPI_TX_SW_LNTD_HSTX_DATA							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		MIPI_TX_SW_LNTD_HSTX_DATA	**DSI Data Lane 0~3 HSTX data**

1021E090 DSI_DBG_CO **DSI Debug Control Register** **00000000**

N

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MIPI_TX_TST_CK_OUT_SEL	MIPI_TX_TST_CK_OUT_EN		MIPI_TX_GPIO_MODE_EN	MIPI_TX_DBG_OUT_EN	MIPI_TX_DBG_SEL			
Type								RW	RW		RW	RW	RW			
Reset								0	0		0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8		MIPI_TX_TST_CK_OUT_SEL	Selects MIPI clocks to frequency meter
7		MIPI_TX_TST_CK_OUT_EN	Enables MIPI clock output to frequency meter
5		MIPI_TX_GPIO_MODE_EN	Enables GPIO of MIPI TX pads
4		MIPI_TX_DBG_OUT_EN	Enables debug output of MIPI probe bus
3:0		MIPI_TX_DBG_SEL	Selects debug mux of MIPI debug bus

1021E094 DSI_DBG_OUT **DSI Debug Out Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIPI_TX_DBG_OUT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIPI_TX_DBG_OUT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		MIPI_TX_DBG_OUT	MIPI debug bus out status

1021E098 DSI_APB_ASYNC_STA **DSI APB Async Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						MIPI_TX_APB_ASYNC_ERR_ADDR										MIPI_TX_APB_ASYNC_ER

																R
Type						RO										RO
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
10:1		MIPI_TX_APB_ASYNC_ERR_ADDR	MIPI APB async error address
0		MIPI_TX_APB_ASYNC_ERR	MIPI APB async error status

1021E200 DSI_HS_BIST_CON CSI HS BIST Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														TX_HS_BIST_RDY_SEL		
Type														RW		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TX_HS_BIST_TM_ZERO								TX_HS_BIST_MODE		TX_HS_BIST_SKEW_MODE	TX_HS_BIST_LANE_NUM			
Type		RW								RW		RW	RW			
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
18:16		TX_HS_BIST_RDY_SEL	
14:8		TX_HS_BIST_TM_ZERO	
6:5		TX_HS_BIST_MODE	Selects BIST mode
4		TX_HS_BIST_SKEW_MODE	Selects skew mode
3:0		TX_HS_BIST_LANE_NUM	CSI BIST lane number

1021E204 DSI_HS_BIST_PAT CSI HS BIST Pattern 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_HS_BIST_PAT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_HS_BIST_PAT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		TX_HS_BIST_PAT	CSI BIST pattern

Module name: mipi_tx_cphy Base address: (+10218000h)

Address	Name	Width	Register Function
10218000	MIPI_TX0_CPHY0_00	32	MIPI_CPHY TRIO0
10218004	MIPI_TX0_CPHY0_04	32	MIPI_CPHY CKG
10218008	MIPI_TX0_CPHY0_08	32	MIPI_CPHY TOP
1021800C	MIPI_TX0_CPHY0_0C	32	MIPI_CPHY TOP 2
10218010	MIPI_TX0_CPHY0_10	32	MIPI_CPHY DSIPLL
10218014	MIPI_TX0_CPHY0_14	32	MIPI_CPHY DSIPLL 2
10218018	MIPI_TX0_CPHY0_18	32	MIPI_CPHY FORCEMODE
1021801C	MIPI_TX0_CPHY0_1C	32	MIPI_CPHY debug
10218040	MIPI_TX0_CPHY0_40	32	CPHY_TX_PRBS_CON
10218044	MIPI_TX0_CPHY0_44	32	CPHY_TX_PRBS_DEBUG
10218048	MIPI_TX0_CPHY0_48	32	CPHY_TX_PREAMBLE
1021804C	MIPI_TX0_CPHY0_4C	32	CPHY_TX_DRIVER_X_CON
10218050	MIPI_TX0_CPHY0_50	32	CPHY_TX_DRIVER_Y_CON
10218054	MIPI_TX0_CPHY0_54	32	CPHY_TX_DRIVER_Z_CON
10218058	MIPI_TX0_CPHY0_58	32	CPHY_TX_PROGSEQ_1
1021805C	MIPI_TX0_CPHY0_5C	32	CPHY_TX_PROGSEQ_2
10218060	MIPI_TX0_CPHY0_60	32	CPHY_TX_SYNC_CODE
10218064	MIPI_TX0_CPHY0_64	32	CPHY_TX_ESCAPE_CODE
10218068	MIPI_TX0_CPHY0_68	32	CPHY_TX_CON
1021806C	MIPI_TX0_CPHY0_6C	32	CPHY_TX_CNT0
10218070	MIPI_TX0_CPHY0_70	32	CPHY_TX_CNT1
10218074	MIPI_TX0_CPHY0_74	32	CPHY_TX_CNT2
10218078	MIPI_TX0_CPHY0_78	32	CPHY_TX_CNT3
1021807C	MIPI_TX0_CPHY0_7C	32	CPHY_TX_CNT4
10218080	MIPI_TX0_CPHY0_80	32	CPHY_TX_FSM
10218084	MIPI_TX0_CPHY0_84	32	CPHY_TX_WIRE_FORCE_EN

Address	Name	Width	Register Function
10218088	MIPI_TX0_CPHY0_88	32	CPHY_TX_WIRE_FORCE_LSB
1021808C	MIPI_TX0_CPHY0_8C	32	CPHY_TX_WIRE_FORCE_MSB
10218090	MIPI_TX0_CPHY0_90	32	CPHY_TX_DA_FORCE_EN
10218094	MIPI_TX0_CPHY0_94	32	CPHY_TX_DA_FORCE_CTL
10218098	MIPI_TX0_CPHY0_98	32	CPHY_TX_SPARE
10218200	MIPI_TX1_CPHY0_00	32	MIPI_CPHY TRIO0
10218204	MIPI_TX1_CPHY0_04	32	MIPI_CPHY CKG
10218208	MIPI_TX1_CPHY0_08	32	MIPI_CPHY TOP
1021820C	MIPI_TX1_CPHY0_0C	32	MIPI_CPHY TOP 2
10218210	MIPI_TX1_CPHY0_10	32	MIPI_CPHY DSIPLL
10218214	MIPI_TX1_CPHY0_14	32	MIPI_CPHY DSIPLL 2
10218218	MIPI_TX1_CPHY0_18	32	MIPI_CPHY FORCEMODE
1021821C	MIPI_TX1_CPHY0_1C	32	MIPI_CPHY debug
10218240	MIPI_TX1_CPHY0_40	32	CPHY_TX_PRBS_CON
10218244	MIPI_TX1_CPHY0_44	32	CPHY_TX_PRBS_DEBUG
10218248	MIPI_TX1_CPHY0_48	32	CPHY_TX_PREAMBLE
1021824C	MIPI_TX1_CPHY0_4C	32	CPHY_TX_DRIVER_X_CON
10218250	MIPI_TX1_CPHY0_50	32	CPHY_TX_DRIVER_Y_CON
10218254	MIPI_TX1_CPHY0_54	32	CPHY_TX_DRIVER_Z_CON
10218258	MIPI_TX1_CPHY0_58	32	CPHY_TX_PROGSEQ_1
1021825C	MIPI_TX1_CPHY0_5C	32	CPHY_TX_PROGSEQ_2
10218260	MIPI_TX1_CPHY0_60	32	CPHY_TX_SYNC_CODE
10218264	MIPI_TX1_CPHY0_64	32	CPHY_TX_ESCAPE_CODE
10218268	MIPI_TX1_CPHY0_68	32	CPHY_TX_CON
1021826C	MIPI_TX1_CPHY0_6C	32	CPHY_TX_CNT0
10218270	MIPI_TX1_CPHY0_70	32	CPHY_TX_CNT1
10218274	MIPI_TX1_CPHY0_74	32	CPHY_TX_CNT2

Address	Name	Width	Register Function
10218278	MIPI_TX1_CPHY0_78	32	CPHY_TX_CNT3
1021827C	MIPI_TX1_CPHY0_7C	32	CPHY_TX_CNT4
10218280	MIPI_TX1_CPHY0_80	32	CPHY_TX_FSM
10218284	MIPI_TX1_CPHY0_84	32	CPHY_TX_WIRE_FORCE_EN
10218288	MIPI_TX1_CPHY0_88	32	CPHY_TX_WIRE_FORCE_LSB
1021828C	MIPI_TX1_CPHY0_8C	32	CPHY_TX_WIRE_FORCE_MSB
10218290	MIPI_TX1_CPHY0_90	32	CPHY_TX_DA_FORCE_EN
10218294	MIPI_TX1_CPHY0_94	32	CPHY_TX_DA_FORCE_CTL
10218298	MIPI_TX1_CPHY0_98	32	CPHY_TX_SPARE

10218000 MIPI_TX0_CPHY0_00 MIPI_CPHY TRIO0 00000880

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSIo_CPHYTX_IMINUS	RG_CSIo_CPHYTX_IPLUS			RG_CSIo_CPHYTX_ERT_CODE				RG_CSIo_CPHYTX_IRT_CODE						RG_CSIo_CPHYTX_CKLANE_EN	RG_CSIo_CPHYTX_LDOOUT_EN
Type	RW	RW			RW				RW						RW	RW
Reset	0	0			1	0	0	0	1	0	0	0			0	0

Bit(s)	Name	Description
15	RG_CSIo_CPHYTX_IMINUS	**Decreases the bias current for TRIO o** 1'b00: normal 1'b01: -10%
14	RG_CSIo_CPHYTX_IPLUS	**Increases the bias current for TRIO o** 1'b00: normal 1'b01: +10%
11:8	RG_CSIo_CPHYTX_ERT_CODE	**TRIO o HS impedance control code** 4'b0000: maximum impedance 4'b1111: minimum impedance
7:4	RG_CSIo_CPHYTX_IRT_CODE	**TRIO o HS impedance control code** 4'b0000: maximum impedance 4'b1111: minimum impedance
1	RG_CSIo_CPHYTX_CKLANE_EN	**Select the clock source** 1'b0: In phase clock for data lane 1'b1: quadrature phase clock for clock lane
0	RG_CSIo_CPHYTX_LDOOUT_EN	**Enables the LDO output for TRIO o** 1'b0: disable 1'b1: enable

Bit(s)	Name	Description

10218004 MIPI_TX0_CPHY0_04 MIPI_CPHY CKG 00000800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSIo_CPHYTX_D14DIV_EN				RG_CSIo_CPHYTX_PAD_TIE_LOW_EN	RG_CSIo_CPHYTX_CKG_IMINUS	RG_CSIo_CPHYTX_CKG_IPLUS		RG_CSIo_CPHYTX_PHYCLK_SEL		RG_CSIo_CPHYTX_LD_IDX_SEL		RG_CSIo_CPHYTX_BCLK_SEL		RG_CSIo_CPHYTX_CPHY0CLK_FREQ_SEL	RG_CSIo_CPHYTX_CKG_LDOOUT_EN
Type	RW				RW	RW	RW		RW		RW		RW		RW	RW
Reset	0				1	0	0		0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RG_CSIo_CPHYTX_D14DIV_EN	**Enables the /14 post divider** 1'b0: gated 1'b1: divided-by-14
11	RG_CSIo_CPHYTX_PAD_TIE_LOW_EN	**Enables the tie-low resistors for 3 pads** 1'b0: floating or depends on line driver. 1'b1: tie to ground with 20k ohm resistors
10	RG_CSIo_CPHYTX_CKG_IMINUS	**Decreases the bias current for clock generator** 1'b00: normal 1'b01: -10%
9	RG_CSIo_CPHYTX_CKG_IPLUS	**Increases the bias current for clock generator** 1'b00: normal 1'b01: +10%
7:6	RG_CSIo_CPHYTX_PHYCLK_SEL	**Selects the phase of CPHY PHYCLK** 2'b00: align with BCLK 2'b01: align with BCLKQ 2'b10: align with BCLKB 2'b11: align with BCLKQB
5:4	RG_CSIo_CPHYTX_LD_IDX_SEL	**Selects the phase of LD_IDX** 2'b00: align with CKQ 2'b01: align with CKB 2'b10: align with CKQB 2'b11: align with CK
3:2	RG_CSIo_CPHYTX_BCLK_SEL	**Selects the phase of PHYCLK** 2'b00: align with CK 2'b01: align with CKQ 2'b10: align with CKB 2'b11: align with CKQB
1	RG_CSIo_CPHYTX_CPHY0CLK_FREQ_SEL	**Selects the frequency of DSICLK** 1'b0: 2X of PHYCLK 1'b1: 1X of PHYCLK
0	RG_CSIo_CPHYTX_CKG_LDOOUT_EN	**Enables the LDO output for clock generator** 1'b0: disable 1'b1: enable

10218008 MIPI_TX0_CPHY0_08 **MIPI_CPHY TOP** **88888880**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI0_CPHYTX_V03_SEL				RG_CSI0_CPHYTX_V035_SEL				RG_CSI0_CPHYTX_V07_SEL				RG_CSI0_CPHYTX_V075_SEL			
Type	RW				RW				RW				RW			
Reset	1	0	0		1	0	0		1	0	0		1	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI0_CPHYTX_V04_SEL				RG_CSI0_CPHYTX_V10_SEL				RG_CSI0_CPHYTX_V12_SEL					RG_CSI0_CPHYTX_LDO_LPF_EN	RG_CSI0_CPHYTX_LDOCORE_EN	RG_CSI0_CPHYTX_BG_CORE_EN
Type	RW				RW				RW					RW	RW	RW
Reset	1	0	0		1	0	0		1	0	0			0	0	0

Bit(s)	Name	Description
31:29	RG_CSI0_CPHYTX_V03_SEL	**Selects 0.3V output voltage** 3'b000: minimum voltage 3'b100: typical voltage 3'b111: maximum voltage
27:25	RG_CSI0_CPHYTX_V035_SEL	**Selects 0.35V output voltage** 3'b000: minimum voltage 3'b100: typical voltage 3'b111: maximum voltage
23:21	RG_CSI0_CPHYTX_V07_SEL	**Selects 0.7V output voltage** 3'b000: minimum voltage 3'b100: typical voltage 3'b111: maximum voltage
19:17	RG_CSI0_CPHYTX_V075_SEL	**Selects 0.75V output voltage** 3'b000: minimum voltage 3'b100: typical voltage 3'b111: maximum voltage
15:13	RG_CSI0_CPHYTX_V04_SEL	**Selects 0.4V output voltage** 3'b000: minimum voltage 3'b100: typical voltage 3'b111: maximum voltage
11:9	RG_CSI0_CPHYTX_V10_SEL	**Selects AVDD10 output voltage** 3'b000: minimum voltage 3'b100: typical voltage 3'b111: maximum voltage
7:5	RG_CSI0_CPHYTX_V12_SEL	**Selects 1.2V output voltage** 3'b0000: minimum voltage 3'b0100: typical voltage 3'b0111: maximum voltage
2	RG_CSI0_CPHYTX_LDO_LPF_EN	**Enables the low-pass filter for TX LDOs** 1'b0: Disable low-pass filter 1'b1: Enable low-pass filter
1	RG_CSI0_CPHYTX_LDOCORE_EN	**Enables the bias current for TX LDOs** 1'b0: disable 1'b1: enable
0	RG_CSI0_CPHYTX_BG_CORE_EN	**Enables the R-string for reference voltage** 1'b0: Power off 1'b1: Enables R-string voltages

1021800C MIPI_TX0_C **MIPI_CPHY TOP 2** **00000F00**

PHY0_0C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_CSI0_CPHYTX_PRESERVE1				RG_CSI0_CPHYTX_PRESERVE0				RG_CSI0_CPHYTX_LNT_AIO_SEL			RG_CSI0_CPHYTX_LNT_TESTMODE_EN
Type					RW				RW				RW			RW
Reset					1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:8	RG_CSI0_CPHYTX_PRESERVE1	**CPHYTX Preserved registers**
7:4	RG_CSI0_CPHYTX_PRESERVE0	**CPHYTX Preserved registers**
3:1	RG_CSI0_CPHYTX_LNT_AIO_SEL	**Selects the analog debug output**
0	RG_CSI0_CPHYTX_LNT_TESTMODE_EN	**Enables analog test mode in CPHYTX** 1'b0: disable 1'b1: enable

10218010 MIPI_TX0_CPHY0_10 MIPI_CPHY DSIPLL C04EC4ED

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI0_CPHYTX_CSIPLL_SDM_PCW															
Type	RW															
Reset	1	1	0	0	0	0	0	0	0	1	0	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI0_CPHYTX_CSIPLL_SDM_PCW															RG_CSI0_CPHYTX_CSIPLL_SDM_PCW_CHG
Type	RW															RW
Reset	1	1	0	0	0	1	0	0	1	1	1	0	1	1	0	1

Bit(s)	Name	Description
31:1	RG_CSI0_CPHYTX_CSIPLL_SDM_PCW	**Feedback divide ratio** 7bit integer + 24bit fractional
0	RG_CSI0_CPHYTX_CSIPLL_SDM_PCW_CHG	**The trigger signal to update the divide ratio of feedback divider**

10218014 MIPI_TX0_CPHY0_14 MIPI_CPHY DSIPLL 2 000EC000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RG_CSIo_CPHYTX_CSIPLL_EN	RG_CSIo_CPHYTX_CSIPLL_MONREF_EN	RG_CSIo_CPHYTX_CSIPLL_MONVC_EN	RG_CSIo_CPHYTX_CSIPLL_MONCK_EN							RG_CSIo_CPHYTX_CSIPLL_RST_DLY		RG_CSIo_CPHYTX_CSIPLL_BLP	RG_CSIo_CPHYTX_CSIPLL_BR	RG_CSIo_CPHYTX_CSIPLL_BP	RG_CSIo_CPHYTX_CSIPLL_VOD_EN
Type	RW	RW	RW	RW							RW		RW	RW	RW	RW
Reset	0	0	0	0							0	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSIo_CPHYTX_CSIPLL_SDM_HREN	RG_CSIo_CPHYTX_CSIPLL_SDM_FRA_EN	RG_CSIo_CPHYTX_CSIPLL_PREDIV		RG_CSIo_CPHYTX_CSIPLL_POSDIV											
Type	RW	RW	RW		RW											
Reset	1	1	0	0	0	0	0									

Bit(s)	Name	Description
31	RG_CSIo_CPHYTX_CSIPLL_EN	**Enables the PLL CPHYTX** 1'b0: Power Down 1'b1: Enable
30	RG_CSIo_CPHYTX_CSIPLL_MONREF_EN	**Monitor PLL reference clock** 1'b0: disable 1'b1: enable
29	RG_CSIo_CPHYTX_CSIPLL_MONVC_EN	**Monitor VCO controlled voltage** 1'b0: disable 1'b1: enable
28	RG_CSIo_CPHYTX_CSIPLL_MONCK_EN	**Monitor PLL output clock** 1'b0: disable 1'b1: enable
21:20	RG_CSIo_CPHYTX_CSIPLL_RST_DLY	**PLL pwr on rst delay adjustment**
19	RG_CSIo_CPHYTX_CSIPLL_BLP	**PLL LPF enable**
18	RG_CSIo_CPHYTX_CSIPLL_BR	**PLL bandwidth tracking adjustment**
17	RG_CSIo_CPHYTX_CSIPLL_BP	**PLL pole adjustment**
16	RG_CSIo_CPHYTX_CSIPLL_VOD_EN	**Overdrive LDO**
15	RG_CSIo_CPHYTX_CSIPLL_SDM_HREN	**SDM High Resolution Enable** 1'b0: Disable 1'b1: Enable
14	RG_CSIo_CPHYTX_CSIPLL_SDM_FRA_EN	**SDMPLL Fractional Mode En** 1'b0: Integer Mode 1'b1: Fractional Mode
13:12	RG_CSIo_CPHYTX_CSIPLL_PREDIV	**Pre divide ratio** 2'b00: /1 2'b01: /2 2'b1x: /4
11:9	RG_CSIo_CPHYTX_CSIPLL_POSDIV	**Post divide ratio** 3'b000: /1 3'b001: /2 3'b010: /4 3'b011: /8 3'b100: /16 Others: Clock Gating

10218018 MIPI_TX0_CPHY0_18 MIPI_CPHY FORCEMODE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSIo_CPHYTX_FORCEMODE_EN	RG_CSIo_CPHYTX_HSTX_DRDY	RG_CSIo_CPHYTX_HSTX_OE	RG_CSIo_CPHYTX_HSTX_PRE_OE	RG_CSIo_CPHYTX_LPTX_OE	RG_CSIo_CPHYTX_LPTX_PRE_OE										
Type	RW	RW	RW	RW	RW	RW										
Reset	0	0	0	0	0	0										

Bit(s)	Name	Description
15	RG_CSIo_CPHYTX_FORCEMODE_EN	
14	RG_CSIo_CPHYTX_HSTX_DRDY	
13	RG_CSIo_CPHYTX_HSTX_OE	
12	RG_CSIo_CPHYTX_HSTX_PRE_OE	
11	RG_CSIo_CPHYTX_LPTX_OE	
10	RG_CSIo_CPHYTX_LPTX_PRE_OE	

1021801C MIPI_TX0_CPHY0_1C MIPI_CPHY debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							DA_CSIo_CPHYTX_HSTX_DRDY	DA_CSIo_CPHYTX_HSTX_OE			DA_CSIo_CPHYTX_HSTX_PRE_OE	DA_CSIo_CPHYTX_LPTX_C	DA_CSIo_CPHYTX_LPTX_B	DA_CSIo_CPHYTX_LPTX_A	DA_CSIo_CPHYTX_LPTX_OE	DA_CSIo_CPHYTX_LPTX_PRE_OE
Type							RU	RU			RU	RU	RU	RU	RU	RU
Reset							0	0			0	0	0	0	0	0

Bit(s)	Name	Description
9	DA_CSIo_CPHYTX_HSTX_DRDY	
8	DA_CSIo_CPHYTX_HSTX_OE	
5	DA_CSIo_CPHYTX_HSTX_PRE_OE	
4	DA_CSIo_CPHYTX_LPTX_C	
3	DA_CSIo_CPHYTX_LPTX_B	
2	DA_CSIo_CPHYTX_LPTX_A	
1	DA_CSIo_CPHYTX_LPTX_OE	
0	DA_CSIo_CPHYTX_LPTX_PRE_O	

Bit(s)	Name	Description
	E	

10218040 MIPI_TX0_CPHY0_40 CPHY_TX_PRBS_CON 00FFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PRBS_DELAY_EN	TX_PRBS_PATTERN_SEL							TX_PRBS_SEED_2							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PRBS_SEED_1								TX_PRBS_SEED_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	TX_PRBS_DELAY_EN	
30:24	TX_PRBS_PATTERN_SEL	
23:16	TX_PRBS_SEED_2	
15:8	TX_PRBS_SEED_1	
7:0	TX_PRBS_SEED_0	

10218044 MIPI_TX0_CPHY0_44 CPHY_TX_PRBS_DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PRBS_DATA_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PRBS_DATA_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PRBS_DATA_OUT	

10218048 MIPI_TX0_CPHY0_48 CPHY_TX_PREAMBLE 00000433

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						TX_POST_SYMBOL				TX_PREEND_SYMBOL				TX_PREBEGIN_SYMBOL		
Type						RW				RW				RW		
Reset						1	0	0		0	1	1		0	1	1

Bit(s)	Name	Description
10:8	TX_POST_SYMBOL	
6:4	TX_PREEND_SYMBOL	
2:0	TX_PREBEGIN_SYMBOL	

1021804C MIPI_TX0_CPHY0_4C CPHY_TX_DRIVER_X_CON 05A30A53

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					TX_DRIVER_X_N											
Type					RW											
Reset					0	1	0	1	1	0	1	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_DRIVER_X_P											
Type					RW											
Reset					1	0	1	0	0	1	0	1	0	0	1	1

Bit(s)	Name	Description
27:16	TX_DRIVER_X_N	
11:0	TX_DRIVER_X_P	

10218050 MIPI_TX0_CPHY0_50 CPHY_TX_DRIVER_Y_CON 035A03A5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					TX_DRIVER_Y_N											
Type					RW											
Reset					0	0	1	1	0	1	0	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_DRIVER_Y_P											
Type					RW											
Reset					0	0	1	1	1	0	1	0	0	1	0	1

Bit(s)	Name	Description
27:16	TX_DRIVER_Y_N	
11:0	TX_DRIVER_Y_P	

10218054 MIPI_TX0_CPHY0_54 CPHY_TX_DRIVER_Z_CON 0A35053A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					TX_DRIVER_Z_N											
Type					RW											
Reset					1	0	1	0	0	0	1	1	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_DRIVER_Z_P											
Type					RW											
Reset					0	1	0	1	0	0	1	1	1	0	1	0

Bit(s)	Name	Description
27:16	TX_DRIVER_Z_N	
11:0	TX_DRIVER_Z_P	

10218058 MIPI_TX0_CPHY0_58 CPHY_TX_PROGSEQ_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			TX_PROGSEQ_S9			TX_PROGSEQ_S8			TX_PROGSEQ_S7			TX_PROGSEQ_S6			TX_PROGSEQ_S5	
Type			RW			RW			RW			RW			RW	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PROGSEQ_S5	TX_PROGSEQ_S4			TX_PROGSEQ_S3			TX_PROGSEQ_S2			TX_PROGSEQ_S1			TX_PROGSEQ_S0		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:27	TX_PROGSEQ_S9	
26:24	TX_PROGSEQ_S8	
23:21	TX_PROGSEQ_S7	
20:18	TX_PROGSEQ_S6	
17:15	TX_PROGSEQ_S5	
14:12	TX_PROGSEQ_S4	
11:9	TX_PROGSEQ_S3	
8:6	TX_PROGSEQ_S2	
5:3	TX_PROGSEQ_S1	
2:0	TX_PROGSEQ_S0	

1021805C MIPI_TX0_CPHY0_5C CPHY_TX_PROGSEQ_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_PROGSEQ_S13			TX_PROGSEQ_S12			TX_PROGSEQ_S11			TX_PROGSEQ_S10		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:9	TX_PROGSEQ_S13	
8:6	TX_PROGSEQ_S12	
5:3	TX_PROGSEQ_S11	
2:0	TX_PROGSEQ_S10	

10218060 MIPI_TX0_C CPHY_TX_SYNC_CODE 40E49233

PHY0_60

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		TX_INITIAL_WIRE_STATE						TX_SYNC_SYMBOL								
Type		RW						RW								
Reset		1	0	0				0	1	1	1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_SYNC_SYMBOL													TX_PRESYNC_SYMBOL		
Type	RW													RW		
Reset	1	0	0	1	0	0	1	0	0	0	1	1		0	1	1

Bit(s)	Name	Description
30:28	TX_INITIAL_WIRE_STATE	
24:4	TX_SYNC_SYMBOL	
2:0	TX_PRESYNC_SYMBOL	

10218064 MIPI_TX0_C PHY0_64 CPHY_TX_ESCAPE_CODE 000E4923

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												TX_ESCAPE_SYMBOL				
Type												RW				
Reset												0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_ESCAPE_SYMBOL															
Type	RW															
Reset	0	1	0	0	1	0	0	1	0	0	1	0	0	0	1	1

Bit(s)	Name	Description
20:0	TX_ESCAPE_SYMBOL	

10218068 MIPI_TX0_C PHY0_68 CPHY_TX_CON 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SW_RST															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										TX_PACKET_FIX	TX_PACKET_TEST_MODE_OUT_EN	TX_PACKET_TEST_MODE	TX_START_EN	TX_ESCAPE_EN	TX_PROGSEQ_EN	TX_EN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
31	TX_SW_RST	
6	TX_PACKET_FIX	
5	TX_PACKET_TEST_MODE_OUT_EN	
4	TX_PACKET_TEST_MODE	
3	TX_START_EN	
2	TX_ESCAPE_EN	
1	TX_PROGSEQ_EN	
0	TX_EN	

1021806C MIPI_TX0_CPHY0_6C CPHY_TX_CNT0 00150A15

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PREBEGIN_CNT								TX_SETTLE_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PREP_CNT								TX_LP001_CNT							
Type	RW								RW							
Reset	0	0	0	0	1	0	1	0	0	0	0	1	0	1	0	1

Bit(s)	Name	Description
31:24	TX_PREBEGIN_CNT	
23:16	TX_SETTLE_CNT	
15:8	TX_PREP_CNT	
7:0	TX_LP001_CNT	

10218070 MIPI_TX0_CPHY0_70 CPHY_TX_CNT1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PREEND_CNT								TX_PROGSEQ_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	TX_PREEND_CNT	
7:0	TX_PROGSEQ_CNT	

10218074 MIPI_TX0_CPHY0_74 CPHY_TX_CNT2 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_ESCAPE_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PACKET_CNT															
Type	RW															
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_ESCAPE_CNT	
15:0	TX_PACKET_CNT	

10218078 MIPI_TX0_CPHY0_78 CPHY_TX_CNT3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TX_POST_CNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	TX_POST_CNT	

1021807C MIPI_TX0_CPHY0_7C CPHY_TX_CNT4 00000064

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TX_LPTX_OE_CNT							
Type									RW							
Reset									0	1	1	0	0	1	0	0

Bit(s)	Name	Description
7:0	TX_LPTX_OE_CNT	

10218080 MIPI_TX0_CPHY0_80 CPHY_TX_FSM 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TX_FSM												
Type				RU												

Reset				0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
12:0	TX_FSM	

10218084 MIPI_TX0_CPHY0_84 CPHY_TX_WIRE_FORCE_EN 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																csr_tx_force_wire_en
Type																RW
Reset																0

Bit(s)	Name	Description
0	csr_tx_force_wire_en	

10218088 MIPI_TX0_CPHY0_88 CPHY_TX_WIRE_FORCE_LSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			csr_tx_force_wire_data_lsb													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	csr_tx_force_wire_data_lsb															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:0	csr_tx_force_wire_data_lsb	

1021808C MIPI_TX0_CPHY0_8C CPHY_TX_WIRE_FORCE_MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					csr_tx_force_wire_data_msb											
Type					RW											

Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	csr_tx_force_wire_data_msb	

10218090 MIPI_TX0_CPHY0_90 CPHY_TX_DA_FORCE_EN 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																csr_tx_force_da_en
Type																RW
Reset																0

Bit(s)	Name	Description
0	csr_tx_force_da_en	

10218094 MIPI_TX0_CPHY0_94 CPHY_TX_DA_FORCE_CTL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												csr_tx_force_hstx_drdy	csr_tx_force_hstx_oe	csr_tx_force_lptx_oe	csr_tx_force_hstx_pre_oe	csr_tx_force_lptx_pre_oe
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	csr_tx_force_hstx_drdy	
3	csr_tx_force_hstx_oe	
2	csr_tx_force_lptx_oe	
1	csr_tx_force_hstx_pre_oe	
0	csr_tx_force_lptx_pre_oe	

10218098 MIPI_TX0_CPHY0_98 CPHY_TX_SPARE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	csr_tx_spare0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	csr_tx_spare0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	csr_tx_spare0	

10218200 MIPI_TX1_CPHY0_00 MIPI_CPHY TRIO0 00000880

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSIo_CPHYTX_IMINUS	RG_CSIo_CPHYTX_IPLUS			RG_CSIo_CPHYTX_ERT_CODE				RG_CSIo_CPHYTX_IRT_CODE						RG_CSIo_CPHYTX_CKLANE_EN	RG_CSIo_CPHYTX_LDOOUT_EN
Type	RW	RW			RW				RW						RW	RW
Reset	0	0			1	0	0	0	1	0	0	0			0	0

Bit(s)	Name	Description
15	RG_CSIo_CPHYTX_IMINUS	**Decreases the bias current for TRIO 0** 1'b00: normal 1'b01: -10%
14	RG_CSIo_CPHYTX_IPLUS	**Increases the bias current for TRIO 0** 1'b00: normal 1'b01: +10%
11:8	RG_CSIo_CPHYTX_ERT_CODE	**TRIO 0 HS impedance control code** 4'b0000: maximum impedance 4'b1111: minimum impedance
7:4	RG_CSIo_CPHYTX_IRT_CODE	**TRIO 0 HS impedance control code** 4'b0000: maximum impedance 4'b1111: minimum impedance
1	RG_CSIo_CPHYTX_CKLANE_EN	**Select the clock source** 1'b0: In phase clock for data lane 1'b1: quadrature phase clock for clock lane
0	RG_CSIo_CPHYTX_LDOOUT_EN	**Enables the LDO output for TRIO 0** 1'b0: disable 1'b1: enable

10218204 MIPI_TX1_CPHY0_04 MIPI_CPHY CKG 00000800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSIo_CPHYTX_D14DIV_EN				RG_CSIo_CPHYTX_PAD_TIE_LOW_EN	RG_CSIo_CPHYTX_CKG_IMINUS	RG_CSIo_CPHYTX_CKG_IPLUS		RG_CSIo_CPHYTX_PHYCLK_SEL		RG_CSIo_CPHYTX_LD_IDX_SEL		RG_CSIo_CPHYTX_BCLK_SEL		RG_CSIo_CPHYTX_CPHYoCLK_FREQ_SEL	RG_CSIo_CPHYTX_CKG_LDOOUT_EN
Type	RW				RW	RW	RW		RW		RW		RW		RW	RW
Reset	0				1	0	0		0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RG_CSIo_CPHYTX_D14DIV_EN	**Enables the /14 post divider** 1'b0: gated 1'b1: divided-by-14
11	RG_CSIo_CPHYTX_PAD_TIE_LOW_EN	**Enables the tie-low resistors for 3 pads** 1'b0: floating or depends on line driver. 1'b1: tie to ground with 20k ohm resistors
10	RG_CSIo_CPHYTX_CKG_IMINUS	**Decreases the bias current for clock generator** 1'b00: normal 1'b01: -10%
9	RG_CSIo_CPHYTX_CKG_IPLUS	**Increases the bias current for clock generator** 1'b00: normal 1'b01: +10%
7:6	RG_CSIo_CPHYTX_PHYCLK_SEL	**Selects the phase of CPHY PHYCLK** 2'b00: align with BCLK 2'b01: align with BCLKQ 2'b10: align with BCLKB 2'b11: align with BCLKQB
5:4	RG_CSIo_CPHYTX_LD_IDX_SEL	**Selects the phase of LD_IDX** 2'b00: align with CKQ 2'b01: align with CKB 2'b10: align with CKQB 2'b11: align with CK
3:2	RG_CSIo_CPHYTX_BCLK_SEL	**Selects the phase of PHYCLK** 2'b00: align with CK 2'b01: align with CKQ 2'b10: align with CKB 2'b11: align with CKQB
1	RG_CSIo_CPHYTX_CPHYoCLK_FREQ_SEL	**Selects the frequency of DSICLK** 1'b0: 2X of PHYCLK 1'b1: 1X of PHYCLK
0	RG_CSIo_CPHYTX_CKG_LDOOUT_EN	**Enables the LDO output for clock generator** 1'b0: disable 1'b1: enable

10218208 MIPI_TX1_CPHY0_08 **MIPI_CPHY TOP** **88888880**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSIo_CPHYTX_V03_SEL				RG_CSIo_CPHYTX_V035_SEL				RG_CSIo_CPHYTX_V07_SEL				RG_CSIo_CPHYTX_V075_SEL			
Type	RW				RW				RW				RW			
Reset	1	0	0		1	0	0		1	0	0		1	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RG_CSI0_CPHYTX_V04_SEL				RG_CSI0_CPHYTX_V10_SEL				RG_CSI0_CPHYTX_V12_SEL					RG_CSI0_CPHYTX_LDO_LPF_EN	RG_CSI0_CPHYTX_LDOCORE_EN	RG_CSI0_CPHYTX_BG_CORE_EN
Type	RW				RW				RW					RW	RW	RW
Reset	1	0	0		1	0	0		1	0	0			0	0	0

Bit(s)	Name	Description
31:29	RG_CSI0_CPHYTX_V03_SEL	**Selects 0.3V output voltage** 3'b000: minimum voltage 3'b100: typical voltage 3'b111: maximum voltage
27:25	RG_CSI0_CPHYTX_V035_SEL	**Selects 0.35V output voltage** 3'b000: minimum voltage 3'b100: typical voltage 3'b111: maximum voltage
23:21	RG_CSI0_CPHYTX_V07_SEL	**Selects 0.7V output voltage** 3'b000: minimum voltage 3'b100: typical voltage 3'b111: maximum voltage
19:17	RG_CSI0_CPHYTX_V075_SEL	**Selects 0.75V output voltage** 3'b000: minimum voltage 3'b100: typical voltage 3'b111: maximum voltage
15:13	RG_CSI0_CPHYTX_V04_SEL	**Selects 0.4V output voltage** 3'b000: minimum voltage 3'b100: typical voltage 3'b111: maximum voltage
11:9	RG_CSI0_CPHYTX_V10_SEL	**Selects AVDD10 output voltage** 3'b000: minimum voltage 3'b100: typical voltage 3'b111: maximum voltage
7:5	RG_CSI0_CPHYTX_V12_SEL	**Selects 1.2V output voltage** 3'b0000: minimum voltage 3'b0100: typical voltage 3'b0111: maximum voltage
2	RG_CSI0_CPHYTX_LDO_LPF_EN	**Enables the low-pass filter for TX LDOs** 1'b0: Disable low-pass filter 1'b1: Enable low-pass filter
1	RG_CSI0_CPHYTX_LDOCORE_EN	**Enables the bias current for TX LDOs** 1'b0: disable 1'b1: enable
0	RG_CSI0_CPHYTX_BG_CORE_EN	**Enables the R-string for reference voltage** 1'b0: Power off 1'b1: Enables R-string voltages

1021820C MIPI_TX1_CPHY0_0C **MIPI_CPHY TOP 2** **00000F00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_CSI0_CPHYTX_PRESERVE1				RG_CSI0_CPHYTX_PRESERVE0				RG_CSI0_CPHYTX_LNT_AIO_SEL			RG_CSI0_

																CPHYTX_LNT_TESTMODE_EN
Type					RW				RW				RW			RW
Reset					1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:8	RG_CSI0_CPHYTX_PRESERVE1	**CPHYTX Preserved registers**
7:4	RG_CSI0_CPHYTX_PRESERVE0	**CPHYTX Preserved registers**
3:1	RG_CSI0_CPHYTX_LNT_AIO_SEL	**Selects the analog debug output**
0	RG_CSI0_CPHYTX_LNT_TESTMODE_EN	**Enables analog test mode in CPHYTX** 1'b0: disable 1'b1: enable

10218210 MIPI_TX1_CPHY0_10 MIPI_CPHY DSIPLL C04EC4ED

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI0_CPHYTX_CSIPLL_SDM_PCW															
Type	RW															
Reset	1	1	0	0	0	0	0	0	0	1	0	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSI0_CPHYTX_CSIPLL_SDM_PCW															RG_CSI0_CPHYTX_CSIPLL_SDM_PCW_CHG
Type	RW															RW
Reset	1	1	0	0	0	1	0	0	1	1	1	0	1	1	0	1

Bit(s)	Name	Description
31:1	RG_CSI0_CPHYTX_CSIPLL_SDM_PCW	**Feedback divide ratio** 7bit integer + 24bit fractional
0	RG_CSI0_CPHYTX_CSIPLL_SDM_PCW_CHG	**The trigger signal to update the divide ratio of feedback divider**

10218214 MIPI_TX1_CPHY0_14 MIPI_CPHY DSIPLL 2 000EC000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CSI0_CPHYTX_CSIPLL_EN	RG_CSI0_CPHYTX_CSIPLL_MONREF_EN	RG_CSI0_CPHYTX_CSIPLL_MONVC_EN	RG_CSI0_CPHYTX_CSIPLL_MONCK_EN							RG_CSI0_CPHYTX_CSIPLL_RST_DLY		RG_CSI0_CPHYTX_CSIPLL_BLP	RG_CSI0_CPHYTX_CSIPLL_BR	RG_CSI0_CPHYTX_CSIPLL_BP	RG_CSI0_CPHYTX_CSIPLL_VOD_EN
Type	RW	RW	RW	RW							RW		RW	RW	RW	RW

Reset	0	0	0	0							0	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSIo_CPHYTX_CSIPLL_SDM_HREN	RG_CSIo_CPHYTX_CSIPLL_SDM_FRA_EN	RG_CSIo_CPHYTX_CSIPLL_PREDIV		RG_CSIo_CPHYTX_CSIPLL_POSDIV											
Type	RW	RW	RW		RW											
Reset	1	1	0	0	0	0	0									

Bit(s)	Name	Description
31	RG_CSIo_CPHYTX_CSIPLL_EN	**Enables the PLL CPHYTX** 1'b0: Power Down 1'b1: Enable
30	RG_CSIo_CPHYTX_CSIPLL_MONREF_EN	**Monitor PLL reference clock** 1'b0: disable 1'b1: enable
29	RG_CSIo_CPHYTX_CSIPLL_MONVC_EN	**Monitor VCO controlled voltage** 1'b0: disable 1'b1: enable
28	RG_CSIo_CPHYTX_CSIPLL_MONCK_EN	**Monitor PLL output clock** 1'b0: disable 1'b1: enable
21:20	RG_CSIo_CPHYTX_CSIPLL_RST_DLY	**PLL pwr on rst delay adjustment**
19	RG_CSIo_CPHYTX_CSIPLL_BLP	**PLL LPF enable**
18	RG_CSIo_CPHYTX_CSIPLL_BR	**PLL bandwidth tracking adjustment**
17	RG_CSIo_CPHYTX_CSIPLL_BP	**PLL pole adjustment**
16	RG_CSIo_CPHYTX_CSIPLL_VOD_EN	**Overdrive LDO**
15	RG_CSIo_CPHYTX_CSIPLL_SDM_HREN	**SDM High Resolution Enable** 1'b0: Disable 1'b1: Enable
14	RG_CSIo_CPHYTX_CSIPLL_SDM_FRA_EN	**SDMPLL Fractional Mode En** 1'b0: Integer Mode 1'b1: Fractional Mode
13:12	RG_CSIo_CPHYTX_CSIPLL_PREDIV	**Pre divide ratio** 2'b00: /1 2'b01: /2 2'b1x: /4
11:9	RG_CSIo_CPHYTX_CSIPLL_POSDIV	**Post divide ratio** 3'b000: /1 3'b001: /2 3'b010: /4 3'b011: /8 3'b100: /16 Others: Clock Gating

10218218 MIPI_TX1_CPHY0_18 MIPI_CPHY FORCEMODE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CSIo_CPHYTX_FORCEMODE_EN	RG_CSIo_CPHYTX_HSTX_DRDY	RG_CSIo_CPHYTX_HSTX_OE	RG_CSIo_CPHYTX_HSTX_PRE_OE	RG_CSIo_CPHYTX_LPTX_OE	RG_CSIo_CPHYTX_LPTX_PRE_OE										
Type	RW	RW	RW	RW	RW	RW										
Reset	0	0	0	0	0	0										

Bit(s)	Name	Description
15	RG_CSIo_CPHYTX_FORCEMODE_EN	
14	RG_CSIo_CPHYTX_HSTX_DRDY	
13	RG_CSIo_CPHYTX_HSTX_OE	
12	RG_CSIo_CPHYTX_HSTX_PRE_OE	
11	RG_CSIo_CPHYTX_LPTX_OE	
10	RG_CSIo_CPHYTX_LPTX_PRE_OE	

1021821C MIPI_TX1_CPHY0_1C MIPI_CPHY debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							DA_CSIo_CPHYTX_HSTX_DRDY	DA_CSIo_CPHYTX_HSTX_OE			DA_CSIo_CPHYTX_HSTX_PRE_OE	DA_CSIo_CPHYTX_LPTX_C	DA_CSIo_CPHYTX_LPTX_B	DA_CSIo_CPHYTX_LPTX_A	DA_CSIo_CPHYTX_LPTX_OE	DA_CSIo_CPHYTX_LPTX_PRE_OE
Type							RO	RO			RO	RO	RO	RO	RO	RO
Reset							0	0			0	0	0	0	0	0

Bit(s)	Name	Description
9	DA_CSIo_CPHYTX_HSTX_DRDY	
8	DA_CSIo_CPHYTX_HSTX_OE	
5	DA_CSIo_CPHYTX_HSTX_PRE_OE	
4	DA_CSIo_CPHYTX_LPTX_C	
3	DA_CSIo_CPHYTX_LPTX_B	
2	DA_CSIo_CPHYTX_LPTX_A	
1	DA_CSIo_CPHYTX_LPTX_OE	
0	DA_CSIo_CPHYTX_LPTX_PRE_OE	

10218240 MIPI_TX1_CPHY0_40 CPHY_TX_PRBS_CON 00FFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	TX_PRBS_DELAY_EN	TX_PRBS_PATTERN_SEL							TX_PRBS_SEED_2							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PRBS_SEED_1								TX_PRBS_SEED_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	TX_PRBS_DELAY_EN	
30:24	TX_PRBS_PATTERN_SEL	
23:16	TX_PRBS_SEED_2	
15:8	TX_PRBS_SEED_1	
7:0	TX_PRBS_SEED_0	

10218244 MIPI_TX1_CPHY0_44 CPHY_TX_PRBS_DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PRBS_DATA_OUT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PRBS_DATA_OUT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PRBS_DATA_OUT	

10218248 MIPI_TX1_CPHY0_48 CPHY_TX_PREAMBLE 00000433

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						TX_POST_SYMBOL				TX_PREEND_SYMBOL				TX_PREBEGIN_SYMBOL		
Type						RW				RW				RW		
Reset						1	0	0		0	1	1		0	1	1

Bit(s)	Name	Description
10:8	TX_POST_SYMBOL	
6:4	TX_PREEND_SYMBOL	
2:0	TX_PREBEGIN_SYMBOL	

10218240C MIPI_TX1_CPHY0_4C CPHY_TX_DRIVER_X_CON 05A30A53

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					TX_DRIVER_X_N											
Type					RW											
Reset					0	1	0	1	1	0	1	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_DRIVER_X_P											
Type					RW											
Reset					1	0	1	0	0	1	0	1	0	0	1	1

Bit(s)	Name	Description
27:16	TX_DRIVER_X_N	
11:0	TX_DRIVER_X_P	

10218250 MIPI_TX1_CPHY0_50 CPHY_TX_DRIVER_Y_CON 035A03A5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					TX_DRIVER_Y_N											
Type					RW											
Reset					0	0	1	1	0	1	0	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_DRIVER_Y_P											
Type					RW											
Reset					0	0	1	1	1	0	1	0	0	1	0	1

Bit(s)	Name	Description
27:16	TX_DRIVER_Y_N	
11:0	TX_DRIVER_Y_P	

10218254 MIPI_TX1_CPHY0_54 CPHY_TX_DRIVER_Z_CON 0A35053A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					TX_DRIVER_Z_N											
Type					RW											
Reset					1	0	1	0	0	0	1	1	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_DRIVER_Z_P											
Type					RW											
Reset					0	1	0	1	0	0	1	1	1	0	1	0

Bit(s)	Name	Description
27:16	TX_DRIVER_Z_N	
11:0	TX_DRIVER_Z_P	

10218258 MIPI_TX1_C CPHY_TX_PROGSEQ_1 00000000

PHY0_58

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			TX_PROGSEQ_S9			TX_PROGSEQ_S8			TX_PROGSEQ_S7			TX_PROGSEQ_S6			TX_PROGSEQ_S5	
Type			RW			RW			RW			RW			RW	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PROGSEQ_S5	TX_PROGSEQ_S4			TX_PROGSEQ_S3			TX_PROGSEQ_S2			TX_PROGSEQ_S1			TX_PROGSEQ_S0		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:27	TX_PROGSEQ_S9	
26:24	TX_PROGSEQ_S8	
23:21	TX_PROGSEQ_S7	
20:18	TX_PROGSEQ_S6	
17:15	TX_PROGSEQ_S5	
14:12	TX_PROGSEQ_S4	
11:9	TX_PROGSEQ_S3	
8:6	TX_PROGSEQ_S2	
5:3	TX_PROGSEQ_S1	
2:0	TX_PROGSEQ_S0	

1021825C MIPI_TX1_C PHY0_5C CPHY_TX_PROGSEQ_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_PROGSEQ_S13			TX_PROGSEQ_S12			TX_PROGSEQ_S11			TX_PROGSEQ_S10		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:9	TX_PROGSEQ_S13	
8:6	TX_PROGSEQ_S12	
5:3	TX_PROGSEQ_S11	
2:0	TX_PROGSEQ_S10	

10218260 MIPI_TX1_C PHY0_60 CPHY_TX_SYNC_CODE 40E49233

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		TX_INITIAL_WIRE_STATE						TX_SYNC_SYMBOL								
Type		RW						RW								
Reset		1	0	0				0	1	1	1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_SYNC_SYMBOL													TX_PRESYNC_SY		

														MBOL		
Type	RW													RW		
Reset	1	0	0	1	0	0	1	0	0	0	1	1		0	1	1

Bit(s)	Name	Description
30:28	TX_INITIAL_WIRE_STATE	
24:4	TX_SYNC_SYMBOL	
2:0	TX_PRESYNC_SYMBOL	

10218264 MIPI_TX1_CPHY0_64 CPHY_TX_ESCAPE_CODE 000E4923

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												TX_ESCAPE_SYMBOL				
Type												RW				
Reset												0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_ESCAPE_SYMBOL															
Type	RW															
Reset	0	1	0	0	1	0	0	1	0	0	1	0	0	0	1	1

Bit(s)	Name	Description
20:0	TX_ESCAPE_SYMBOL	

10218268 MIPI_TX1_CPHY0_68 CPHY_TX_CON 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SW_RST															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										TX_PACKET_FIX	TX_PACKET_TEST_MODE_OUT_EN	TX_PACKET_TEST_MODE	TX_START_EN	TX_ESCAPE_EN	TX_PROGSEQ_EN	TX_EN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TX_SW_RST	
6	TX_PACKET_FIX	
5	TX_PACKET_TEST_MODE_OUT_EN	
4	TX_PACKET_TEST_MODE	
3	TX_START_EN	
2	TX_ESCAPE_EN	
1	TX_PROGSEQ_EN	
0	TX_EN	

Bit(s)	Name	Description

1021826C MIPI_TX1_CPHY0_6C **CPHY_TX_CNT0** **00150A15**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PREBEGIN_CNT								TX_SETTLE_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PREP_CNT								TX_LP001_CNT							
Type	RW								RW							
Reset	0	0	0	0	1	0	1	0	0	0	0	1	0	1	0	1

Bit(s)	Name	Description
31:24	TX_PREBEGIN_CNT	
23:16	TX_SETTLE_CNT	
15:8	TX_PREP_CNT	
7:0	TX_LP001_CNT	

10218270 MIPI_TX1_CPHY0_70 **CPHY_TX_CNT1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PREEND_CNT								TX_PROGSEQ_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	TX_PREEND_CNT	
7:0	TX_PROGSEQ_CNT	

10218274 MIPI_TX1_CPHY0_74 **CPHY_TX_CNT2** **00000400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_ESCAPE_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PACKET_CNT															
Type	RW															
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_ESCAPE_CNT	
15:0	TX_PACKET_CNT	

Bit(s)	Name	Description

10218278 MIPI_TX1_CPHY0_78 CPHY_TX_CNT3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TX_POST_CNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	TX_POST_CNT	

1021827C MIPI_TX1_CPHY0_7C CPHY_TX_CNT4 00000064

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TX_LPTX_OE_CNT							
Type									RW							
Reset									0	1	1	0	0	1	0	0

Bit(s)	Name	Description
7:0	TX_LPTX_OE_CNT	

10218280 MIPI_TX1_CPHY0_80 CPHY_TX_FSM 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TX_FSM												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
12:0	TX_FSM	

10218284 MIPI_TX1_CPHY0_84 CPHY_TX_WIRE_FORCE_EN 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																csr_tx_force_wire_en
Type																RW
Reset																0

Bit(s)	Name	Description
0	csr_tx_force_wire_en	

10218288 MIPI_TX1_CPHY0_88 CPHY_TX_WIRE_FORCE_LSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			csr_tx_force_wire_data_lsb													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	csr_tx_force_wire_data_lsb															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:0	csr_tx_force_wire_data_lsb	

1021828C MIPI_TX1_CPHY0_8C CPHY_TX_WIRE_FORCE_MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					csr_tx_force_wire_data_msb											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	csr_tx_force_wire_data_msb	

10218290 MIPI_TX1_CPHY0_90 CPHY_TX_DA_FORCE_EN 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																csr_tx_force_da_en
Type																RW
Reset																0

Bit(s)	Name	Description
0	csr_tx_force_da_en	

10218294 MIPI_TX1_CPHY0_94 CPHY_TX_DA_FORCE_CTL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												csr_tx_force_hstx_drdy	csr_tx_force_hstx_oe	csr_tx_force_lptx_oe	csr_tx_force_hstx_pre_oe	csr_tx_force_lptx_pre_oe
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	csr_tx_force_hstx_drdy	
3	csr_tx_force_hstx_oe	
2	csr_tx_force_lptx_oe	
1	csr_tx_force_hstx_pre_oe	
0	csr_tx_force_lptx_pre_oe	

10218298 MIPI_TX1_CPHY0_98 CPHY_TX_SPARE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	csr_tx_spareo															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	csr_tx_spareo															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	csr_tx_spare0	

Module name: seninf1 Base address: (+1a040200h)

Address	Name	Width	Register Function
1A040200	SENINF1_CTRL	32	SENINF 1 Control Register
1A040204	SENINF1_CTRL_EXT	32	SENINF 1 Control Register Extend
1A040208	SENINF1_ASYNC_CTRL	32	SENINF 1 Async Control Register

1A040200 SENINF1_CTRL SENINF 1 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PAD2CAM_DATA_SEL							SENINF_DEBUG_SEL							
Type		RW							RW							
Reset		0	0	0					0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_SRC_SEL							CSI3_SW_RST	CSI2_SW_RST	SCAM_SW_RST	TEST_MODEL_SW_RST	CKGEN_SW_RST	CCIR_SW_RST	OCSI2_SW_RST	NCSI2_SW_RST	SENINF_EN
Type	RW							RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:28	PAD2CAM_DATA_SEL	0: PAD2CAM_DATA[9:0] 3: {PAD2CAM_DATA[7:0],2'b00} 4: {PAD2CAM_DATA[9:2]2'b00} 0: PAD2CAM_DATA[9:0] 3: {PAD2CAM_DATA[7:0],2'b00} 4: {PAD2CAM_DATA[9:2]2'b00}
23:20	SENINF_DEBUG_SEL	**Selects SENINF1 debug**
15:12	SENINF_SRC_SEL	**Selects SENINF input source** 0: CSI2 1: Test Model 2: CCIR656 3: Parallel Sensor 4: Serial Sensor 8: NCSI2
8	CSI3_SW_RST	**CSI3 software reset, active high** 0: De-assert reset 1: Assert reset
7	CSI2_SW_RST	**CSI2 software reset, active high** 0: De-assert reset 1: Assert reset
6	SCAM_SW_RST	**SCAM software reset, active high** 0: De-assert reset

Bit(s)	Name	Description
		1: Assert reset
5	TEST_MODEL_SW_RST	**Test model software reset, active high** 0: De-assert reset 1: Assert reset
4	CKGEN_SW_RST	**CKGEN software reset, active high** 0: De-assert reset 1: Assert reset
3	CCIR_SW_RST	**CCIR software reset, active high** 0: De-assert reset 1: Assert reset
2	OCSI2_SW_RST	**OCSI2 software reset, active high** 0: De-assert reset 1: Assert reset
1	NCSI2_SW_RST	**NCSI2 software reset, active high** 0: De-assert reset 1: Assert reset
0	SENINF_EN	

1A040204 SENINF1_CTRL_EXT — **SENINF 1 Control Register Extend** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															SENINF_SRC_SEL_EXT	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SENINF_CSI3_IP_EN	SENINF_CSI2_IP_EN	SENINF_NCSI2_IP_EN	SENINF_SCAM_IP_EN			SENINF_TESTMDL_IP_EN	SENINF_OCSI2_IP_EN
Type									RW	RW	RW	RW			RW	RW
Reset									0	0	0	0			0	0

Bit(s)	Name	Description
17:16	SENINF_SRC_SEL_EXT	[0] Set 1'b1 for CSI2 [1] Set 1'b1 for CSI3 For constraints only.
7	SENINF_CSI3_IP_EN	Enables CSI3 IP
6	SENINF_CSI2_IP_EN	Enables CSI2 IP
5	SENINF_NCSI2_IP_EN	Enables NCSI2 IP
4	SENINF_SCAM_IP_EN	Enables SCAM IP
1	SENINF_TESTMDL_IP_EN	Enables TESTMDL IP
0	SENINF_OCSI2_IP_EN	Enables OCSI2 IP

1A040208 SENINF1_ASYNC_CTRL — **SENINF 1 Async Control Register** — **1B1F0002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			FIFO_FLUSH_EN								FIFO_PUSH_EN					
Type			RW								RW					
Reset			0	1	1	0	1	1			0	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SENINF_HSYNC_POL	SENINF_VSYNC_POL	SENINF_HSYNC_MASK	SENINF_ASYNC_FIFO_RST
Type													RW	RW	RW	RW
Reset													0	0	1	0

Bit(s)	Name	Description
29:24	FIFO_FLUSH_EN	**Normal mode: 6'b011011** JPEG two pixel mode: 6'b011000
21:16	FIFO_PUSH_EN	**Normal mode: 6'b011111** JPEG two pixel mode: 6'b011110
3	SENINF_HSYNC_POL	**SENINF HSYNC polarity**
2	SENINF_VSYNC_POL	**SENINF VSYNC polarity**
1	SENINF_HSYNC_MASK	**Masks hsync** 0: Send hsync when vsync = 1 1: Does not send hsync when vsync = 1
0	SENINF_ASYNC_FIFO_RST	**Async FIFO software reset**

Module name: seninf1_csi2 Base address: (+1a040a00h)

Address	Name	Width	Register Function
1A040A00	SENINF1_CSI2_CTL	32	CSI2 Function Enable
1A040A04	SENINF1_CSI2_LNRC_TIMING	32	CSI2 Clock Lane Timing Parameters
1A040A08	SENINF1_CSI2_LNRD_TIMING	32	CSI2 Data Lane Timing Parameters
1A040A0C	SENINF1_CSI2_DPCM	32	CSI2 DPCM Parameters
1A040A10	SENINF1_CSI2_INT_EN	32	CSI2 Interrupt Enable
1A040A14	SENINF1_CSI2_INT_STATUS	32	CSI2 Interrupt Status
1A040A18	SENINF1_CSI2_DGB_SEL	32	CSI2 Debug Selection
1A040A1C	SENINF1_CSI2_DBG_PORT	32	CSI2 Debug Port
1A040A20	SENINF1_CSI2_SPARE0	32	SPARE0
1A040A24	SENINF1_CSI2_SPARE1	32	SPARE1
1A040A28	SENINF1_CSI2_LNRC_FSM	32	CSI2 Clock Lane RX FSM
1A040A2C	SENINF1_CSI2_LNRD_FSM	32	CSI2 Data Lane RX FSM
1A040A30	SENINF1_CSI2_FRAME_LINE_NUM	32	CSI2 Frame/Line Number
1A040A34	SENINF1_CSI2_GENERIC_SHORT	32	CSI2 Generic Short Packet
1A040A38	SENINF1_CSI2_HSRX_DBG	32	CSI2 HSRX Enable
1A040A3C	SENINF1_CSI2_DI	32	CSI2 Data Interleaving Parameters

Address	Name	Width	Register Function
1A040A40	SENINF1_CSI2_HS_TRAIL	32	CSI2 HS Trail Timing Parameters
1A040A44	SENINF1_CSI2_DI_CTRL	32	CSI2 Data Interleaving Control
1A040A48	SENINF1_CSI2_LNRD_FSM_X	32	CSI2 Data Lane RX FSM Other
1A040A4C	SENINF1_CSI2_DETECT_CON1	32	CSI2 CPHY Detect Control Sync
1A040A50	SENINF1_CSI2_DETECT_CON2	32	CSI2 CPHY Detect Control Escape
1A040A54	SENINF1_CSI2_DETECT_CON3	32	CSI2 CPHY Detect Control Post
1A040A58	SENINF1_CSI2_RLR0_CON0	32	CSI2 CPHY RLR0 CON0
1A040A5C	SENINF1_CSI2_RLR1_CON0	32	CSI2 CPHY RLR1 CON0
1A040A60	SENINF1_CSI2_RLR2_CON0	32	CSI2 CPHY RLR2 CON0
1A040A64	SENINF1_CSI2_RLR_CON0	32	CSI2 CPHY RLR CON0
1A040A68	SENINF1_CSI2_MUX_CON	32	CSI2 Pin Pux Sel
1A040A6C	SENINF1_CSI2_DETECT_DBG0	32	CSI2 Detection Debug 0
1A040A70	SENINF1_CSI2_DETECT_DBG1	32	CSI2 Detection Debug 1
1A040A74	SENINF1_CSI2_RESYNC_MERGE_CTL	32	CSI2 Lane Resync Merge Control
1A040A78	SENINF1_CSI2_CTRL_TRIO_MUX	32	CSI2 Control Trio Mux
1A040A7C	SENINF1_CSI2_CTRL_TRIO_CON	32	CSI2 Control Trio Config
1A040A80	SENINF1_FIX_ADDR_CPHY0_DBG	32	cphy_fix_point_addr_cphy0_debug
1A040A84	SENINF1_FIX_ADDR_CPHY1_DBG	32	cphy_fix_point_addr_cphy1_debug
1A040A88	SENINF1_FIX_ADDR_CPHY2_DBG	32	cphy_fix_point_addr_cphy2_debug
1A040A8C	SENINF1_FIX_ADDR_DBG	32	cphy_fix_point_addr_debug
1A040A90	SENINF1_WIRE_STATE_DECODE_CPHY0_DBG0	32	cphy_wire_state_decode_cphy0_debug0
1A040A94	SENINF1_WIRE_STATE_DECODE_CPHY0_DBG1	32	cphy_wire_state_decode_cphy0_debug1
1A040A98	SENINF1_WIRE_STATE_DECODE_CPHY1_DBG0	32	cphy_wire_state_decode_cphy1_debug0
1A040A9C	SENINF1_WIRE_STATE_DECODE_CPHY1_DBG1	32	cphy_wire_state_decode_cphy1_debug1
1A040AA0	SENINF1_WIRE_STATE_DECODE_CP	32	cphy_wire_state_decode_cphy2_debug0

Address	Name	Width	Register Function
	HY2_DBG0		
1A040AA4	SENINF1_WIRE_STATE_DECODE_CPHY2_DBG1	32	cphy_wire_state_decode_cphy2_debug1
1A040AA8	SENINF1_SYNC_RESYNC_CTL	32	CSI2 Sync Resync Control
1A040AAC	SENINF1_POST_DETECT_CTL	32	CSI2 Post Detect Control
1A040AB0	SENINF1_WIRE_STATE_DECODE_CONFIG	32	CSI2 Wire State Decode Config
1A040AB4	SENINF1_CSI2_CPHY_LNRD_FSM	32	CPHY Data Lane RX FSM
1A040AB8	SENINF1_FIX_ADDR_CPHY0_DBG0	32	cphy_fix_point_addr_cphy0_debug0
1A040ABC	SENINF1_FIX_ADDR_CPHY0_DBG1	32	cphy_fix_point_addr_cphy0_debug1
1A040AC0	SENINF1_FIX_ADDR_CPHY0_DBG2	32	cphy_fix_point_addr_cphy0_debug2
1A040AC4	SENINF1_FIX_ADDR_CPHY1_DBG0	32	cphy_fix_point_addr_cphy1_debug0
1A040AC8	SENINF1_FIX_ADDR_CPHY1_DBG1	32	cphy_fix_point_addr_cphy1_debug1
1A040ACC	SENINF1_FIX_ADDR_CPHY1_DBG2	32	cphy_fix_point_addr_cphy1_debug2
1A040AD0	SENINF1_FIX_ADDR_CPHY2_DBG0	32	cphy_fix_point_addr_cphy2_debug0
1A040AD4	SENINF1_FIX_ADDR_CPHY2_DBG1	32	cphy_fix_point_addr_cphy2_debug1
1A040AD8	SENINF1_FIX_ADDR_CPHY2_DBG2	32	cphy_fix_point_addr_cphy2_debug2
1A040ADC	SENINF1_FIX_ADDR_DBG0	32	cphy_fix_point_addr_debug0
1A040AE0	SENINF1_FIX_ADDR_DBG1	32	cphy_fix_point_addr_debug1
1A040AE4	SENINF1_FIX_ADDR_DBG2	32	cphy_fix_point_addr_debug2
1A040AE8	SENINF1_CSI2_MODE	32	CSI2 Packet Structure
1A040AF0	SENINF1_CSI2_DI_EXT	32	CSI2 Data Interleaving Parameters Extend
1A040AF4	SENINF1_CSI2_DI_CTRL_EXT	32	CSI2 Data Interleaving Control Extend
1A040AF8	SENINF1_CSI2_CPHY_LOOPBACK	32	CSI2 SW Trigger sync_init and hs_en
1A040B00	SENINF1_CSI2_PROGSEQ_0	32	CSI2 CPHY program sequence_0
1A040B04	SENINF1_CSI2_PROGSEQ_1	32	CSI2 CPHY program sequence_1
1A040B10	SENINF1_CSI2_INT_EN_EXT	32	CSI2 Interrupt Enable Extend
1A040B14	SENINF1_CSI2_INT_STATUS_EXT	32	CSI2 Interrupt Status Extend
1A040B18	SENINF1_CSI2_CPHY_FIX_POINT_	32	CSI2 CPHY Fix Point Reset Mode

Address	Name	Width	Register Function
	RST		
1A040B20	SENINF1_CSI2_DPHY_RESYNC_CTL	32	CSI2 DPHY Lane Resync Control

1A040A00 SENINF1_CSI2_CTL **CSI2 Function Enable** **01886160**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA_LANE7_EN	DATA_LANE6_EN	VS_OUT_CYCLE_NUMBER		CLOCK_HS_OPTION	REF_SYNC_DET_EN	HS_TRAIL_EN	ASYNC_FIFO_RST_SCH		SYNC_DET_BITSWAP_EN	SYNC_DET_EN	SYNC_DET_SCHEME	FLUSH_MODE			ED_SEL
Type	RW	RW	RW		RW	RW	RW	RW		RW	RW	RW	RW			RW
Reset	0	0	0	0	0	0	0	1	1	0	0	0	1	0		0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VS_TYPE	BYTE2PIXEL_EN	IMAGE_PACKET_EN	GENERIC_LONG_PACKET_EN	DATA_LANE5_EN	DATA_LANE4_EN	HS_END_EN	HS_PRPR_EN	HSRX_DET_EN	CRC_EN	ECC_EN	CLOCK_LANE_EN	DATA_LANE3_EN	DATA_LANE2_EN	DATA_LANE1_EN	DATA_LANE0_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	1	1	0	0	0	0	1	0	1	1	0	0	0	0	0

Bit(s)	Name	Description
31	DATA_LANE7_EN	**Enables data lane 7**
30	DATA_LANE6_EN	**Enables data lane 6**
29:28	VS_OUT_CYCLE_NUMBER	0: 4T 1: 8T
27	CLOCK_HS_OPTION	0: Enable clock lane HS based on LP11, LP01, LP00 1: Enable clock lane HS based on LP00
26	REF_SYNC_DET_EN	**Reference sync detect signal to do analog sync**
25	HS_TRAIL_EN	**Extends HS trail**
24:23	ASYNC_FIFO_RST_SCH	
22	SYNC_DET_BITSWAP_EN	
21	SYNC_DET_EN	**Enables sync sequence detection**
20	SYNC_DET_SCHEME	0: B8 1: 101110
19:18	FLUSH_MODE	0: Disable 1: Flush at first cycle of LP11 2: Flush at LP11 3: Reserved
16	ED_SEL	0: {WCH,WCL,DI} 1: {DI,WCL,WCH}
15	VS_TYPE	**VS type** 0: 4T 1: Frame start to frame end
14	BYTE2PIXEL_EN	**Byte 2 pixel conversion**
13	IMAGE_PACKET_EN	**Image data types**
12	GENERIC_LONG_PACKET_EN	**Generic long packet data types**
11	DATA_LANE5_EN	**Enables data lane 6**
10	DATA_LANE4_EN	**Enables data lane 5**
9	HS_END_EN	**Enables HS_EX reset at packet end**
8	HS_PRPR_EN	**Enables RX_HS_PRPR state**
7	HSRX_DET_EN	**Enables HSRX termination auto-detection flow**

Bit(s)	Name	Description
6	CRC_EN	**Enables checksum**
5	ECC_EN	**Enables packet header ECC**
4	CLOCK_LANE_EN	**Enables clock lane**
3	DATA_LANE3_EN	**Enables data lane 3**
2	DATA_LANE2_EN	**Enables data lane 2**
1	DATA_LANE1_EN	**Enables data lane 1**
0	DATA_LANE0_EN	**Enables data lane 0**

1A040A04 SENINF1_CSI2_LNRC_TIMING **CSI2 Clock Lane Timing Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLOCK_SETTLE_PARAMETER								CLOCK_TERM_PARAMETER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	CLOCK_SETTLE_PARAMETER	TD_SETTLE parameter
7:0	CLOCK_TERM_PARAMETER	TD_TERM_EN parameter

1A040A08 SENINF1_CSI2_LNRD_TIMING **CSI2 Data Lane Timing Parameters** **00002000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_SETTLE_PARAMETER								DATA_TERM_PARAMETER							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	DATA_SETTLE_PARAMETER	TD_SETTLE parameter
7:0	DATA_TERM_PARAMETER	TD_TERM_EN parameter

1A040A0C SENINF1_CSI2_DPCM **CSI2 DPCM Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	DI_2A_DPCM_EN	DI_37_DPCM_EN	DI_36_DPCM_EN	DI_35_DPCM_EN	DI_34_DPCM_EN	DI_33_DPCM_EN	DI_32_DPCM_EN	DI_31_DPCM_EN	DI_30_DPCM_EN				DPCM_MODE			
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW				RW			
Reset	0	0	0	0	0	0	0	0	0				0	0	0	0

Bit(s)	Name	Description
15	DI_2A_DPCM_EN	**Enables DPCM**
14	DI_37_DPCM_EN	**Enables DPCM**
13	DI_36_DPCM_EN	**Enables DPCM**
12	DI_35_DPCM_EN	**Enables DPCM**
11	DI_34_DPCM_EN	**Enables DPCM**
10	DI_33_DPCM_EN	**Enables DPCM**
9	DI_32_DPCM_EN	**Enables DPCM**
8	DI_31_DPCM_EN	**Enables DPCM**
7	DI_30_DPCM_EN	**Enables DPCM**
3:0	DPCM_MODE	0: 10-8-10

1A040A10 SENINF1_CSI2_INT_EN **CSI2 Interrupt Enable** **1FFFBFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_WCLR_EN			TRIO2_ESCAPE_CODE_DETECT	TRIO1_ESCAPE_CODE_DETECT	TRIO0_ESCAPE_CODE_DETECT	TRIO2_RESYNC_FIFO_OVERFLOW	TRIO1_RESYNC_FIFO_OVERFLOW	TRIO0_RESYNC_FIFO_OVERFLOW	ERR_LANE_RESYNC	ERR_FRAME_SYNC_S5	ERR_FRAME_SYNC_S4	ERR_FRAME_SYNC_S3	ERR_FRAME_SYNC_S2	ERR_FRAME_SYNC_S1	ERR_FRAME_SYNC_S0
Type	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0			1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FE	GS	LS	FS	ERR_SOT_SYNC_HS_LNRD3	ERR_SOT_SYNC_HS_LNRD2	ERR_SOT_SYNC_HS_LNRD1	ERR_SOT_SYNC_HS_LNRD0	ERR_MULTI_LANE_SYNC	ERR_AFIFO	ERR_CRC	ERR_ECC_DOUBLE	ERR_ECC_CORRECTED	ERR_ECC_NO_ERROR	ERR_ID	ERR_FRAME_SYNC
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	INT_WCLR_EN	**Enables interrupt write clear**
28	TRIO2_ESCAPE_CODE_DETECT	**Enables TRIO2_ESCAPE_CODE_DETECT interrupt**
27	TRIO1_ESCAPE_CODE_DETECT	**Enables TRIO1_ESCAPE_CODE_DETECT interrupt**
26	TRIO0_ESCAPE_CODE_DETECT	**Enables TRIO0_ESCAPE_CODE_DETECT interrupt**
25	TRIO2_RESYNC_FIFO_OVERFLOW	**Enables TRIO2_RESYNC_FIFO_OVERFLOW interrupt**
24	TRIO1_RESYNC_FIFO_OVERFLOW	**Enables TRIO1_RESYNC_FIFO_OVERFLOW interrupt**
23	TRIO0_RESYNC_FIFO_OVERFLOW	**Enables TRIO0_RESYNC_FIFO_OVERFLOW interrupt**
22	ERR_LANE_RESYNC	**Enables ERR_LANE_RESYNC interrupt**
21	ERR_FRAME_SYNC_S5	**Enables ERR_FRAME_SYNC interrupt**
20	ERR_FRAME_SYNC_S4	**Enables ERR_FRAME_SYNC interrupt**
19	ERR_FRAME_SYNC_S3	**Enables ERR_FRAME_SYNC interrupt**
18	ERR_FRAME_SYNC_S2	**Enables ERR_FRAME_SYNC interrupt**
17	ERR_FRAME_SYNC_S1	**Enables ERR_FRAME_SYNC interrupt**

Bit(s)	Name	Description
16	ERR_FRAME_SYNC_S0	Enables ERR_FRAME_SYNC interrupt
15	FE	Enables frame end interrupt
14	GS	Enables generic short packet interrupt
13	LS	Enables line start interrupt
12	FS	Enables frame start interrupt
11	ERR_SOT_SYNC_HS_LNRD3	Enables ERR_SOT_SYNC_HS interrupt
10	ERR_SOT_SYNC_HS_LNRD2	Enables ERR_SOT_SYNC_HS interrupt
9	ERR_SOT_SYNC_HS_LNRD1	Enables ERR_SOT_SYNC_HS interrupt
8	ERR_SOT_SYNC_HS_LNRD0	Enables ERR_SOT_SYNC_HS interrupt
7	ERR_MULTI_LANE_SYNC	Enables ERR_MULTI_LANE_SYNC interrupt
6	ERR_AFIFO	Enables ERR_AFIFO interrupt
5	ERR_CRC	Enables ERR_CRC interrupt
4	ERR_ECC_DOUBLE	Enables ERR_ECC_DOUBLE interrupt
3	ERR_ECC_CORRECTED	Enables ERR_ECC_CORRECTED interrupt
2	ERR_ECC_NO_ERROR	ERR_ECC_NO_ERROR interrupt
1	ERR_ID	Enables ERR_ID interrupt
0	ERR_FRAME_SYNC	Enables ERR_FRAME_SYNC interrupt

1A040A14 SENINF1_CSI2_INT_STATUS **CSI2 Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				TRIO2_ESCAPE_CODE_DETECT_STA	TRIO1_ESCAPE_CODE_DETECT_STA	TRIO0_ESCAPE_CODE_DETECT_STA	TRIO2_RESYNC_FIFO_OVERFLOW_STA	TRIO1_RESYNC_FIFO_OVERFLOW_STA	TRIO0_RESYNC_FIFO_OVERFLOW_STA	ERR_LANE_RESYNC_STA	ERR_FRAME_SYNC_S5_STA	ERR_FRAME_SYNC_S4_STA	ERR_FRAME_SYNC_S3_STA	ERR_FRAME_SYNC_S2_STA	ERR_FRAME_SYNC_S1_STA	ERR_FRAME_SYNC_S0_STA
Type				RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FE_STA	GS_STA	LS_STA	FS_STA	ERR_SOT_SYNC_HS_LNRD3_STA	ERR_SOT_SYNC_HS_LNRD2_STA	ERR_SOT_SYNC_HS_LNRD1_STA	ERR_SOT_SYNC_HS_LNRD0_STA	ERR_MULTI_LANE_SYNC_STA	ERR_AFIFO_STA	ERR_CRC_STA	ERR_ECC_DOUBLE_STA	ERR_ECC_CORRECTED_STA	ERR_ECC_NO_ERROR_STA	ERR_ID_STA	ERR_FRAME_SYNC_STA
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	TRIO2_ESCAPE_CODE_DETECT_STA	Asserted when the escape code of trio2 is detected
27	TRIO1_ESCAPE_CODE_DETECT_STA	Asserted when the escape code of trio1 is detected
26	TRIO0_ESCAPE_CODE_DETECT_STA	Asserted when the escape code of trio0 is detected
25	TRIO2_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of CPHY trio2 is overflowed
24	TRIO1_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of CPHY trio1 is overflowed
23	TRIO0_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of CPHY trio0 is overflowed
22	ERR_LANE_RESYNC_STA	Asserted when CPHY lane sync detect time is longer than setting resync cycles

Bit(s)	Name	Description
21	ERR_FRAME_SYNC_S5_STA	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
20	ERR_FRAME_SYNC_S4_STA	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
19	ERR_FRAME_SYNC_S3_STA	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
18	ERR_FRAME_SYNC_S2_STA	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
17	ERR_FRAME_SYNC_S1_STA	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
16	ERR_FRAME_SYNC_S0_STA	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
15	FE_STA	**Frame end interrupt**
14	GS_STA	**Enables generic short packet interrupt**
13	LS_STA	**Line start interrupt**
12	FS_STA	**Frame start interrupt**
11	ERR_SOT_SYNC_HS_LNRD3_STA	**Asserted when proper synchronization cannot be expected**
10	ERR_SOT_SYNC_HS_LNRD2_STA	**Asserted when proper synchronization cannot be expected**
9	ERR_SOT_SYNC_HS_LNRD1_STA	**Asserted when proper synchronization cannot be expected**
8	ERR_SOT_SYNC_HS_LNRD0_STA	**Asserted when proper synchronization cannot be expected**
7	ERR_MULTI_LANE_SYNC_STA	**Asserted when multiple lane synchronization fails**
6	ERR_AFIFO_STA	**Asserted when error occurs in asynchronous FIFO**
5	ERR_CRC_STA	**Asserted when computed CRC code is differen from received CRC code**
4	ERR_ECC_DOUBLE_STA	**Asserted when an ECC syndrome is computed and two bit-errors are detected in the received packet header**
3	ERR_ECC_CORRECTED_STA	**Asserted when an ECC syndrome is computed and a single bit-error in the packet header is detected and corrected**
2	ERR_ECC_NO_ERROR_STA	**Asserted when an ECC syndrome is computed and the result is zero indicating a packet header that is considered to be without errors or has more than two bit errors** CSI-2's ECC mechanism cannot detect this type of error.
1	ERR_ID_STA	**Asserted whean a packet header is decoded with an unrecognized or unimplemented data ID**
0	ERR_FRAME_SYNC_STA	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**

1A040A18 SENINF1_CSI2_DGB_SEL CSI2 Debug Selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_EN															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DEBUG_SEL							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	DEBUG_EN	Enables debug
7:0	DEBUG_SEL	Selects debug

1A040A1C SENINF1_CSI2_DBG_PORT CSI2 Debug Port 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CTL_DBG_PORT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	CTL_DBG_PORT	Febug port

1A040A20 SENINF1_CSI2_SPARE0 SPARE0 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	SPARE0	Spare register

1A040A24 SENINF1_CSI2_SPARE1 SPARE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE1	Spare register

1A040A28 SENINF1_CSI2_LNRC_FSM — CSI2 Clock Lane RX FSM — 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											LNRC_RX_FSM					
Type											RO					
Reset											0	0	0	0	0	1

Bit(s)	Name	Description
5:0	LNRC_RX_FSM	RX FSM of clock lane

1A040A2C SENINF1_CSI2_LNRD_FSM — CSI2 Data Lane RX FSM — 01010101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LNRD3_RX_FSM								LNRD2_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		LNRD1_RX_FSM								LNRD0_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1

Bit(s)	Name	Description
30:24	LNRD3_RX_FSM	RX FSM of data lane 3
22:16	LNRD2_RX_FSM	RX FSM of data lane 2
14:8	LNRD1_RX_FSM	RX FSM of data lane 1
6:0	LNRD0_RX_FSM	RX FSM of data lane 0

1A040A30 SENINF1_CSI2_FRAME_LINE_NUM — CSI2 Frame/Line Number — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LINE_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FRAME_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	LINE_NUM	Line number

Bit(s)	Name	Description
15:0	FRAME_NUM	Frame number

1A040A34 SENINF1_CSI2_GENERIC_SHORT — CSI2 Generic Short Packet — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GENERIC_SHORT_PACKET_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											GENERIC_SHORT_PACKET_DT						
Type											RO					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
31:16	GENERIC_SHORT_PACKET_DATA	Generic short packet data
5:0	GENERIC_SHORT_PACKET_DT	Generic short packet data

1A040A38 SENINF1_CSI2_HSRX_DBG — CSI2 HSRX Enable — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DATA_LANE7_HSRX_EN	DATA_LANE6_HSRX_EN	DATA_LANE5_HSRX_EN	DATA_LANE4_HSRX_EN	CLOCK_LANE_HSRX_EN	DATA_LANE3_HSRX_EN	DATA_LANE2_HSRX_EN	DATA_LANE1_HSRX_EN	DATA_LANE0_HSRX_EN
Type								RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	DATA_LANE7_HSRX_EN	Enables data lane 3 HSRX circuit
7	DATA_LANE6_HSRX_EN	Enables data lane 2 HSRX circuit
6	DATA_LANE5_HSRX_EN	Enables data lane 1 HSRX circuit
5	DATA_LANE4_HSRX_EN	Enables data lane 0 HSRX circuit
4	CLOCK_LANE_HSRX_EN	Enables clock lane HSRX circut
3	DATA_LANE3_HSRX_EN	Enables data lane 3 HSRX circuit
2	DATA_LANE2_HSRX_EN	Enables data lane 2 HSRX circuit
1	DATA_LANE1_HSRX_EN	Enables data lane 1 HSRX circuit
0	DATA_LANE0_HSRX_EN	Enables data lane 0 HSRX circuit

1A040A3C SENINF1_CSI2_DI — CSI2 Data Interleaving Parameters — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	DT3						VC3		DT2						VC2	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DT1						VC1		DT0						VC0	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:26	DT3	Data type identifier
25:24	VC3	Virtual channel identifier
23:18	DT2	Data type identifier
17:16	VC2	Virtual channel identifier
15:10	DT1	Data type identifier
9:8	VC1	Virtual channel identifier
7:2	DT0	Data type identifier
1:0	VC0	Virtual channel identifier

1A040A40 SENINF1_CSI2_HS_TRAIL **CSI2 HS Trail Timing Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									HS_TRAIL_PARAMETER							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	HS_TRAIL_PARAMETER	HS TRAIL parameter

1A040A44 SENINF1_CSI2_DI_CTRL **CSI2 Data Interleaving Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						DT3_INTERLEAVING		VC3_INTERLEAVING						DT2_INTERLEAVING		VC2_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DT1_INTERLEAVING		VC1_INTERLEAVING						DT0_INTERLEAVING		VC0_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
26:25	DT3_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
24	VC3_INTERLEAVING	**Virtual channel identifier interleaving**
18:17	DT2_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
16	VC2_INTERLEAVING	**Virtual channel identifier interleaving**
10:9	DT1_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
8	VC1_INTERLEAVING	**Virtual channel identifier interleaving**
2:1	DT0_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
0	VC0_INTERLEAVING	**Virtual channel identifier interleaving**

1A040A48 SENINF1_CSI2_LNRD_FSM_X **CSI2 Data Lane RX FSM Other** **01010101**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LNRD7_RX_FSM								LNRD6_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		LNRD5_RX_FSM								LNRD4_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1

Bit(s)	Name	Description
30:24	LNRD7_RX_FSM	RX FSM of data lane 3
22:16	LNRD6_RX_FSM	RX FSM of data lane 2
14:8	LNRD5_RX_FSM	RX FSM of data lane 1
6:0	LNRD4_RX_FSM	RX FSM of data lane 0

1A040A4C SENINF1_CSI2_DETECT_CON1 **CSI2 CPHY Detect Control Sync** **0E492300**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				SYNC_WORD												
Type				RW												
Reset				0	1	1	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYNC_WORD								DETECT_SYNC_MASK							DETECT_SYNC_

																DISABLE
Type	RW								RW							RW
Reset	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:8	SYNC_WORD	
7:1	DETECT_SYNC_MASK	
0	DETECT_SYNC_DISABLE	

1A040A50 SENINF1_CSI2_DETECT_CON2 — CSI2 CPHY Detect Control Escape — 0E492300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				ESCAPE_WORD												
Type				RW												
Reset				0	1	1	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ESCAPE_WORD								DETECT_ESCAPE_MASK							DETECT_ESCAPE_DISABLE
Type	RW								RW							RW
Reset	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:8	ESCAPE_WORD	
7:1	DETECT_ESCAPE_MASK	
0	DETECT_ESCAPE_DISABLE	

1A040A54 SENINF1_CSI2_DETECT_CON3 — CSI2 CPHY Detect Control Post — 12492400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				POST_WORD												
Type				RW												
Reset				1	0	0	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	POST_WORD								DETECT_POST_MASK							DETECT_POST_DISABLE
Type	RW								RW							RW
Reset	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:8	POST_WORD	
7:1	DETECT_POST_MASK	
0	DETECT_POST_DISABLE	

Bit(s)	Name	Description

1A040A58 SENINF1_CSI2_RLR0_CON0 CSI2 CPHY RLR0 CON0 FFFFFF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLR0_PRBS_SEED_2								RLR0_PRBS_SEED_1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLR0_PRBS_SEED_0								RLR0_PRBS_PATTERN_SEL							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RLR0_PRBS_SEED_2	
23:16	RLR0_PRBS_SEED_1	
15:8	RLR0_PRBS_SEED_0	
7:0	RLR0_PRBS_PATTERN_SEL	

1A040A5C SENINF1_CSI2_RLR1_CON0 CSI2 CPHY RLR1 CON0 FFFFFF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLR1_PRBS_SEED_2								RLR1_PRBS_SEED_1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLR1_PRBS_SEED_0								RLR1_PRBS_PATTERN_SEL							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RLR1_PRBS_SEED_2	
23:16	RLR1_PRBS_SEED_1	
15:8	RLR1_PRBS_SEED_0	
7:0	RLR1_PRBS_PATTERN_SEL	

1A040A60 SENINF1_CSI2_RLR2_CON0 CSI2 CPHY RLR2 CON0 FFFFFF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLR2_PRBS_SEED_2								RLR2_PRBS_SEED_1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLR2_PRBS_SEED_0								RLR2_PRBS_PATTERN_SEL							
Type	RW								RW							

Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RLR2_PRBS_SEED_2	
23:16	RLR2_PRBS_SEED_1	
15:8	RLR2_PRBS_SEED_0	
7:0	RLR2_PRBS_PATTERN_SEL	

1A040A64 SENINF1_CSI2_RLR_CON CSI2 CPHY RLR CON0 FFFFFF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLRN_PRBS_SEED_2								RLRN_PRBS_SEED_1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLRN_PRBS_SEED_0								RLRN_PRBS_PATTERN_SEL							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RLRN_PRBS_SEED_2	
23:16	RLRN_PRBS_SEED_1	
15:8	RLRN_PRBS_SEED_0	
7:0	RLRN_PRBS_PATTERN_SEL	

1A040A68 SENINF1_CSI2_MUX_CON CSI2 Pin Pux Sel 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												POST_PACKET_IGNORE_EN	RLR_PATTERN_DELAY_EN	CPHY_RX_EXTERNAL_EN	CPHY_TX_EXTERNAL_EN	DPHY_RX_EXTERNAL_EN
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	POST_PACKET_IGNORE_EN	
3	RLR_PATTERN_DELAY_EN	
2	CPHY_RX_EXTERNAL_EN	
1	CPHY_TX_EXTERNAL_EN	
0	DPHY_RX_EXTERNAL_EN	

1A040A6C SENINF1_CSI2 Detection Debug 0 00000000

I2_DETECT_DBG0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		POSITION_SYNC_LANE2_ST				DETECT_POST_LANE2_ST	DETECT_ESCAPE_LANE2_ST	DETECT_SYNC_LANE2_ST		POSITION_ESCAPE_LANE1_ST				POSITION_SYNC_LANE1_ST		
Type		RO				RO	RO	RO		RO				RO		
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	POSITION_SYNC_LANE1_ST	DETECT_POST_LANE1_ST	DETECT_ESCAPE_LANE1_ST	DETECT_SYNC_LANE1_ST		POSITION_ESCAPE_LANE0_ST				POSITION_SYNC_LANE0_ST				DETECT_POST_LANE0_ST	DETECT_ESCAPE_LANE0_ST	DETECT_SYNC_LANE0_ST
Type	RO	RO	RO	RO		RO				RO				RO	RO	RO
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:27	POSITION_SYNC_LANE2_ST	
26	DETECT_POST_LANE2_ST	
25	DETECT_ESCAPE_LANE2_ST	
24	DETECT_SYNC_LANE2_ST	
22:19	POSITION_ESCAPE_LANE1_ST	
18:15	POSITION_SYNC_LANE1_ST	
14	DETECT_POST_LANE1_ST	
13	DETECT_ESCAPE_LANE1_ST	
12	DETECT_SYNC_LANE1_ST	
10:7	POSITION_ESCAPE_LANE0_ST	
6:3	POSITION_SYNC_LANE0_ST	
2	DETECT_POST_LANE0_ST	
1	DETECT_ESCAPE_LANE0_ST	
0	DETECT_SYNC_LANE0_ST	

1A040A70 SENINF1_CSI2_DETECT_DBG1 **CSI2 Detection Debug 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													POSITION_ESCAPE_LANE2_ST			
Type													RO			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	POSITION_ESCAPE_LANE2_ST	

1A040A74 SENINF1_CSI2_RESYNC_MERGE_CTL **CSI2 Lane Resync Merge Control** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								LANE_RESYNC_FLUSH_EN				LANE_MERGE_INPUT_SEL		CPHY_LANE_RESYNC_CNT		
Type								RW				RW		RW		
Reset								0				0		0	0	1

Bit(s)	Name	Description
8	LANE_RESYNC_FLUSH_EN	
4	LANE_MERGE_INPUT_SEL	
2:0	CPHY_LANE_RESYNC_CNT	

1A040A78 SENINF1_CSI2_CTRL_TRIO_MUX **CSI2 Control Trio Mux** **00000088**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TRIO2_MUX			TRIO1_MUX			TRIO0_MUX		
Type								RW			RW			RW		
Reset								0	1	0	0	0	1	0	0	0

Bit(s)	Name	Description
8:6	TRIO2_MUX	
5:3	TRIO1_MUX	
2:0	TRIO0_MUX	

1A040A7C SENINF1_CSI2_CTRL_TRIO_CON **CSI2 Control Trio Config** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											TRIO2_HSRX_EN	TRIO2_LPRX_EN	TRIO1_HSRX_EN	TRIO1_LPRX_EN	TRIO0_HSRX_EN	TRIO0_LPRX_EN

Type											RW	RW	RW	RW	RW	RW
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5	TRIO2_HSRX_EN	
4	TRIO2_LPRX_EN	
3	TRIO1_HSRX_EN	
2	TRIO1_LPRX_EN	
1	TRIO0_HSRX_EN	
0	TRIO0_LPRX_EN	

1A040A80 SENINF1_FIX_ADDR_CPHY0_DBG cphy_fix_point_addr_cphy0_debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								WORD_COUNT_OVER_FLOAT_CPHY0	ERROR_COUNT_CPHY0							
Type								RO	RO							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
24	WORD_COUNT_OVER_FLOAT_CPHY0	
23:16	ERROR_COUNT_CPHY0	

1A040A84 SENINF1_FIX_ADDR_CPHY1_DBG cphy_fix_point_addr_cphy1_debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								WORD_COUNT_OVER_FLOAT_CPHY1	ERROR_COUNT_CPHY1							
Type								RO	RO							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
24	WORD_COUNT_OVER_FLOAT_CPHY1	
23:16	ERROR_COUNT_CPHY1	

1A040A88 SENINF1_FIX_ADDR_CPHY2_DBG cphy_fix_point_addr_cphy2_debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								WORD_COUNT_OVER_FLOAT_CPHY2	ERROR_COUNT_CPHY2							
Type								RO	RO							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
24	WORD_COUNT_OVER_FLOAT_CPHY2	
23:16	ERROR_COUNT_CPHY2	

1A040A8C SENINF1_FIX_ADDR_DBG cphy_fix_point_addr_debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								WORD_COUNT_OVER_FLOAT	ERROR_COUNT							
Type								RO	RO							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
24	WORD_COUNT_OVER_FLOAT	
23:16	ERROR_COUNT	

1A040A90 SENINF1_WIRE_STATE_D cphy_wire_state_decode_cphy0_debug0 00000000

ECODE_CPHY0_DBG0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYMBOL_STREAM0_CPHY0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYMBOL_STREAM0_CPHY0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SYMBOL_STREAM0_CPHY0	

1A040A94 SENINF1_WIRE_STATE_DECODE_CPHY0_DBG1 cphy_wire_state_decode_cphy0_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SYMBOL_STREAM_VALID_CPHY0	SYMBOL_STREAM1_CPHY0									
Type						RO	RO									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	SYMBOL_STREAM_VALID_CPHY0	
9:0	SYMBOL_STREAM1_CPHY0	

1A040A98 SENINF1_WIRE_STATE_DECODE_CPHY1_DBG0 cphy_wire_state_decode_cphy1_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYMBOL_STREAM0_CPHY1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYMBOL_STREAM0_CPHY1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SYMBOL_STREAM0_CPHY1	

1A040A9C SENINF1_WIRE_STATE_DECODE_CPHY1_DBG1 cphy_wire_state_decode_cphy1_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SYMBOL_STREAM_VALID_CPHY1	SYMBOL_STREAM1_CPHY1									
Type						RO	RO									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	SYMBOL_STREAM_VALID_CPHY1	
9:0	SYMBOL_STREAM1_CPHY1	

1A040AA0 SENINF1_WIRE_STATE_DECODE_CPHY2_DBG0 cphy_wire_state_decode_cphy2_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYMBOL_STREAM0_CPHY2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYMBOL_STREAM0_CPHY2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SYMBOL_STREAM0_CPHY2	

1A040AA4 SENINF1_WIRE_STATE_DECODE_CPHY2_DBG1 cphy_wire_state_decode_cphy2_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SYMBOL_STREAM_VALID_CPHY2	SYMBOL_STREAM1_CPHY2									
Type						RO	RO									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	SYMBOL_STREAM_VALID_CPHY2	
9:0	SYMBOL_STREAM1_CPHY2	

1A040AA8 SENINF1_SYNC_RESYNC_CTL **CSI2 Sync Resync Control** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													FLUSH_VALID	SYNC_DETECTION_SEL		
Type													RW	RW		
Reset													0	0	0	1

Bit(s)	Name	Description
3	FLUSH_VALID	
2:0	SYNC_DETECTION_SEL	

1A040AAC SENINF1_POST_DETECT_CTL **CSI2 Post Detect Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															POST_EN	POST_DETECT_DISABLE
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
1	POST_EN	
0	POST_DETECT_DISABLE	

1A040AB0 SENINF1_WIRE_STATE_DECODE_CONFIG — CSI2 Wire State Decode Config — 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INIT_STATE_DECODE		
Type														RW		
Reset														1	0	0

Bit(s)	Name	Description
2:0	INIT_STATE_DECODE	

1A040AB4 SENINF1_CSI2_CPHY_LNRD_FSM — CPHY Data Lane RX FSM — 01010100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		TRIO2_RX_FSM								TRIO1_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TRIO0_RX_FSM														
Type		RO														
Reset		0	0	0	0	0	0	1								

Bit(s)	Name	Description
30:24	TRIO2_RX_FSM	RX FSM of data trio 2
22:16	TRIO1_RX_FSM	RX FSM of data trio 1
14:8	TRIO0_RX_FSM	RX FSM of data trio 0

1A040AB8 SENINF1_FIX_ADDR_CPHY0_DBG0 — cphy_fix_point_addr_cphy0_debug0 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD_COUNT_CPHY0_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY0_DBG0															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD_COUNT_CPHY0_DBG0	

1A040ABC SENINF1_FIX_ADDR_CPHY0_DBG1 cphy_fix_point_addr_cphy0_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY0_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY0_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERROR_RECORD_CPHY0_DBG0	
15:0	WORD_COUNT_CPHY0_DBG1	

1A040AC0 SENINF1_FIX_ADDR_CPHY0_DBG2 cphy_fix_point_addr_cphy0_debug2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY0_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERROR_RECORD_CPHY0_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ERROR_RECORD_CPHY0_DBG1	

1A040AC4 SENINF1_FIX_ADDR_CPHY1_DBG0 cphy_fix_point_addr_cphy1_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD_COUNT_CPHY1_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY1_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD_COUNT_CPHY1_DBG0	

1A040AC8 SENINF1_FIX_ADDR_CPHY1_DBG1 cphy_fix_point_addr_cphy1_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY1_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY1_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERROR_RECORD_CPHY1_DBG0	
15:0	WORD_COUNT_CPHY1_DBG1	

1A040ACC SENINF1_FIX_ADDR_CPHY1_DBG2 cphy_fix_point_addr_cphy1_debug2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY1_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERROR_RECORD_CPHY1_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ERROR_RECORD_CPHY1_DBG1	

1A040AD0 SENINF1_FIX_ADDR_CPHY2_DBG0 cphy_fix_point_addr_cphy2_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD_COUNT_CPHY2_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY2_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD_COUNT_CPHY2_DBG0	

1A040AD4 SENINF1_FIX_ADDR_CPHY2_DBG1 cphy_fix_point_addr_cphy2_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY2_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY2_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERROR_RECORD_CPHY2_DBG0	
15:0	WORD_COUNT_CPHY2_DBG1	

1A040AD8 SENINF1_FIX_ADDR_CPHY2_DBG2 cphy_fix_point_addr_cphy2_debug2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY2_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERROR_RECORD_CPHY2_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ERROR_RECORD_CPHY2_DBG1	

1A040ADC SENINF1_FIX_ADDR_DBG cphy_fix_point_addr_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD_COUNT_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD_COUNT_DBG0	

Bit(s)	Name	Description

1A040AE0 SENINF1_FIX_ADDR_DBG1 cphy_fix_point_addr_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERROR_RECORD_DBG0	
15:0	WORD_COUNT_DBG1	

1A040AE4 SENINF1_FIX_ADDR_DBG2 cphy_fix_point_addr_debug2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERROR_RECORD_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ERROR_RECORD_DBG1	

1A040AE8 SENINF1_CSI2_MODE CSI2 Packet Structure 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	csr_cphy_wc_pos								csr_cphy_di_pos							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						csr_csi2_header_len			csr_csi2_mode							
Type						RW			RW							
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	csr_cphy_wc_pos	
23:16	csr_cphy_di_pos	

Bit(s)	Name	Description
10:8	csr_csi2_header_len	0: 4 bytes 1: 12 bytes 2: 24 bytes 4: 36 bytes
7:0	csr_csi2_mode	

1A040AF0 SENINF1_CSI2_DI_EXT **CSI2 Data Interleaving Parameters Extend** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DT5						VC5		DT4						VC4	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:10	DT5	Data type identifier
9:8	VC5	Virtual channel identifier
7:2	DT4	Data type identifier
1:0	VC4	Virtual channel identifier

1A040AF4 SENINF1_CSI2_DI_CTRL_EXT **CSI2 Data Interleaving Control Extend** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DT5_INTERLEAVING		VC5_INTERLEAVING						DT4_INTERLEAVING		VC4_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0

Bit(s)	Name	Description
10:9	DT5_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
8	VC5_INTERLEAVING	**Virtual channel identifier interleaving**
2:1	DT4_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
0	VC4_INTERLEAVING	**Virtual channel identifier interleaving**

1A040AF8 SENINF1_CSI2_CPHY_LOOPBACK **CSI2 SW Trigger sync_init and hs_en** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RELEASE_SYNC_INIT	TRIGGER_SYNC_INIT
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RELEASE_SYNC_INIT	Releases sync_init in CPHY TX loopback test mode
0	TRIGGER_SYNC_INIT	Triggers sync_init and hs_en in CPHY TX loopback test mode

1A040B00 SENINF1_CSI2_PROGSEQ_0 **CSI2 CPHY program sequence_0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PROG SEQ_ S7				PROG SEQ_ S6				PROGSEQ_S5				PROGSEQ_S4		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PROGSEQ_S3				PROGSEQ_S2				PROGSEQ_S1				PROGSEQ_S0		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	PROGSEQ_S7	Fix symbol for prbs generator
26:24	PROGSEQ_S6	Fix symbol for prbs generator
22:20	PROGSEQ_S5	Fix symbol for prbs generator
18:16	PROGSEQ_S4	Fix symbol for prbs generator
14:12	PROGSEQ_S3	Fix symbol for prbs generator
10:8	PROGSEQ_S2	Fix symbol for prbs generator
6:4	PROGSEQ_S1	Fix symbol for prbs generator
2:0	PROGSEQ_S0	Fix symbol for prbs generator

1A040B04 SENINF1_CSI2_PROGSEQ_1 **CSI2 CPHY program sequence_1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										PROG SEQ_ S13				PROGSEQ_S 12		
Type										RW				RW		
Reset										0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PROGSEQ_S11				PROGSEQ_S10				PROGSEQ_S9				PROGSEQ_S8		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
22:20	PROGSEQ_S13	Fix symbol for prbs generator
18:16	PROGSEQ_S12	Fix symbol for prbs generator
14:12	PROGSEQ_S11	Fix symbol for prbs generator
10:8	PROGSEQ_S10	Fix symbol for prbs generator
6:4	PROGSEQ_S9	Fix symbol for prbs generator
2:0	PROGSEQ_S8	Fix symbol for prbs generator

1A040B10 SENINF1_CSI2_INT_EN_EXT **CSI2 Interrupt Enable Extend** **0000071F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_WCLR_EN															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						ERR_SOT_SYNC_HS_TRIO2	ERR_SOT_SYNC_HS_TRIO1	ERR_SOT_SYNC_HS_TRIO0				DPHY3_RESYNC_FIFO_OVERFLOW	DPHY2_RESYNC_FIFO_OVERFLOW	DPHY1_RESYNC_FIFO_OVERFLOW	DPHY0_RESYNC_FIFO_OVERFLOW	ERR_LANE_RESYNC
Type						RW	RW	RW				RW	RW	RW	RW	RW
Reset						1	1	1				1	1	1	1	1

Bit(s)	Name	Description
31	INT_WCLR_EN	Enables Interrupt write clear
10	ERR_SOT_SYNC_HS_TRIO2	Enables TRIO2 ERR_SOT_SYNC_HS interrupt
9	ERR_SOT_SYNC_HS_TRIO1	Enables TRIO1 ERR_SOT_SYNC_HS interrupt
8	ERR_SOT_SYNC_HS_TRIO0	Enables TRIO0 ERR_SOT_SYNC_HS interrupt
4	DPHY3_RESYNC_FIFO_OVERFLOW	Enables LANE3_RESYNC_FIFO_OVERFLOW interrupt
3	DPHY2_RESYNC_FIFO_OVERFLOW	Enables LANE2_RESYNC_FIFO_OVERFLOW interrupt
2	DPHY1_RESYNC_FIFO_OVERFLOW	Enables LANE1_RESYNC_FIFO_OVERFLOW interrupt
1	DPHY0_RESYNC_FIFO_OVERFLOW	Enables LANE0_RESYNC_FIFO_OVERFLOW interrupt
0	ERR_LANE_RESYNC	Enables ERR_LANE_RESYNC interrupt

1A040B14 SENINF1_CSI2_INT_STATUS_EXT **CSI2 Interrupt Status Extend** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						ERR_SOT_SYNC_HS_TRIO2_STA	ERR_SOT_SYNC_HS_TRIO1_STA	ERR_SOT_SYNC_HS_TRIO0_STA				DPHY3_RESYNC_FIFO_OVERFLOW_STA	DPHY2_RESYNC_FIFO_OVERFLOW_STA	DPHY1_RESYNC_FIFO_OVERFLOW_STA	DPHY0_RESYNC_FIFO_OVERFLOW_STA	ERR_LANE_RESYNC_STA
Type						RO	RO	RO				RO	RO	RO	RO	RO
Reset						0	0	0				0	0	0	0	0

Bit(s)	Name	Description
10	ERR_SOT_SYNC_HS_TRIO2_STA	Asserted when proper synchronization cannot be expected
9	ERR_SOT_SYNC_HS_TRIO1_STA	Asserted when proper synchronization cannot be expected
8	ERR_SOT_SYNC_HS_TRIO0_STA	Asserted when proper synchronization cannot be expected
4	DPHY3_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of dphy lane3 is overflowed
3	DPHY2_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of dphy lane2 is overflowed
2	DPHY1_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of dphy lane1 is overflowed
1	DPHY0_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of dphy lane0 is overflowed
0	ERR_LANE_RESYNC_STA	Asserted when dphy lane sync detect time is larger than setting resync cycles

1A040B18 SENINF1_CSI2_CPHY_FIX_POINT_RST — **CSI2 CPHY Fix Point Reset Mode** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CPHY_FIX_POINT_RST_MODE	CPHY_FIX_POINT_SW_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	CPHY_FIX_POINT_RST_MODE	Fix point rest mode
0	CPHY_FIX_POINT_SW_RST	Fix point software reset

1A040B20 SENINF1_CSI2_DPHY_RESYNC_CTL — **CSI2 DPHY Lane Resync Control** — **00000100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DPHY_RESYNC_CNT								DPHY_RESYNC_FLUSH_EN	DPHY_RESYNC_DATAOUT_OPTION	DPHY_BYPASS_LANE_RESYNC
Type						RW								RW	RW	RW
Reset						0	0	1						0	0	0

Bit(s)	Name	Description
10:8	DPHY_RESYNC_CNT	Detect lane skew cycle count
2	DPHY_RESYNC_FLUSH_EN	Enables lane resync flush
1	DPHY_RESYNC_DATAOUT_OPTION	Data output option
0	DPHY_BYPASS_LANE_RESYNC	Bypass lane resync function

Module name: mipi_rx_config_csi0 Base address: (+1a040800h)

Address	Name	Width	Register Function
1A040800	MIPI_RX_CON00_CSI0	32	MIPI RX Config Register
1A040804	MIPI_RX_CON04_CSI0	32	MIPI RX Config Register
1A040808	MIPI_RX_CON08_CSI0	32	MIPI RX Config Register
1A040824	MIPI_RX_CON24_CSI0	32	MIPI RX Config Register
1A040828	MIPI_RX_CON28_CSI0	32	MIPI RX Config Register
1A040834	MIPI_RX_CON34_CSI0	32	MIPI RX Config Register
1A040838	MIPI_RX_CON38_CSI0	32	MIPI RX Config Register
1A04083C	MIPI_RX_CON3C_CSI0	32	MIPI RX Config Register
1A040840	MIPI_RX_CON40_CSI0	32	MIPI RX Config Register
1A040844	MIPI_RX_CON44_CSI0	32	MIPI RX Config Register
1A040848	MIPI_RX_CON48_CSI0	32	MIPI RX Config Register
1A04084C	MIPI_RX_CON4C_CSI0	32	MIPI RX Config Register
1A040850	MIPI_RX_CON50_CSI0	32	MIPI RX Config Register
1A04087C	MIPI_RX_CON7C_CSI0	32	MIPI RX Config Register
1A040880	MIPI_RX_CON80_CSI0	32	MIPI RX Config Register

Address	Name	Width	Register Function
1A040884	MIPI_RX_CON84_CSIo	32	MIPI RX Config Register
1A040888	MIPI_RX_CON88_CSIo	32	MIPI RX Config Register
1A04088C	MIPI_RX_CON8C_CSIo	32	MIPI RX Config Register
1A040890	MIPI_RX_CON90_CSIo	32	MIPI RX Config Register
1A040894	MIPI_RX_CON94_CSIo	32	MIPI RX Config Register
1A040898	MIPI_RX_CON98_CSIo	32	MIPI RX Config Register
1A0408A0	MIPI_RX_CONA0_CSIo	32	MIPI RX Config Register
1A0408B0	MIPI_RX_CONB0_CSIo	32	Deskew control register
1A0408B4	MIPI_RX_CONB4_CSIo	32	Deskew sync detection sequence
1A0408B8	MIPI_RX_CONB8_CSIo	32	Deskew timing control
1A0408BC	MIPI_RX_CONBC_CSIo	32	Deskew mode
1A0408C0	MIPI_RX_CONC0_CSIo	32	Interrupt enable
1A0408C4	MIPI_RX_CONC4_CSIo	32	Interrupt status
1A0408C8	MIPI_RX_CONC8_CSIo	32	Debug mux select
1A0408CC	MIPI_RX_CONCC_CSIo	32	Debug outputs
1A0408D0	MIPI_RX_COND0_CSIo	32	Deskew delay length

1A040800 MIPI_RX_CON00_CSIo **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_CSIo_LNR3_HSRX_OFFSET_CODE					RG_CSIo_LNR3_HSRX_CAL_EN	RG_CSIo_LNR3_HSRX_CAL_APPLY		RG_CSIo_LNR2_HSRX_OFFSET_CODE					RG_CSIo_LNR2_HSRX_CAL_EN	RG_CSIo_LNR2_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSIo_LNR1_HSRX_OFFSET_CODE					RG_CSIo_LNR1_HSRX_CAL_EN	RG_CSIo_LNR1_HSRX_CAL_APPLY		RG_CSIo_LNR0_HSRX_OFFSET_CODE					RG_CSIo_LNR0_HSRX_CAL_EN	RG_CSIo_LNR0_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW

Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	RG_CSI0_LNR3_HSRX_OFFSET_CODE	**Lane3 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
25	RG_CSI0_LNR3_HSRX_CAL_EN	**Lane3 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
24	RG_CSI0_LNR3_HSRX_CAL_APPLY	**Lane3 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
22:18	RG_CSI0_LNR2_HSRX_OFFSET_CODE	**Lane2 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
17	RG_CSI0_LNR2_HSRX_CAL_EN	**Lane2 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
16	RG_CSI0_LNR2_HSRX_CAL_APPLY	**Lane2 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
14:10	RG_CSI0_LNR1_HSRX_OFFSET_CODE	**Lane1 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
9	RG_CSI0_LNR1_HSRX_CAL_EN	**Lane1 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
8	RG_CSI0_LNR1_HSRX_CAL_APPLY	**Lane1 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
6:2	RG_CSI0_LNR0_HSRX_OFFSET_CODE	**Lane0 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
1	RG_CSI0_LNR0_HSRX_CAL_EN	**Lane0 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
0	RG_CSI0_LNR0_HSRX_CAL_APPLY	**Lane0 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result

1A040804 MIPI_RX_CON04_CSI0 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_CSI0_LNR7_HSRX_OFFSET_CODE					RG_CSI0_LNR7_HSRX_CAL_EN	RG_CSI0_LNR7_HSRX_CAL_APPLY		RG_CSI0_LNR6_HSRX_OFFSET_CODE					RG_CSI0_LNR6_HSRX_CAL_EN	RG_CSI0_LNR6_HSRX_CAL_APPLY

Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI0_LNR5_HSRX_OFFSET_CODE					RG_CSI0_LNR5_HSRX_CAL_EN	RG_CSI0_LNR5_HSRX_CAL_APPLY		RG_CSI0_LNR4_HSRX_OFFSET_CODE					RG_CSI0_LNR4_HSRX_CAL_EN	RG_CSI0_LNR4_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	RG_CSI0_LNR7_HSRX_OFFSET_CODE	**Lane7 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
25	RG_CSI0_LNR7_HSRX_CAL_EN	**Lane7 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
24	RG_CSI0_LNR7_HSRX_CAL_APPLY	**Lane7 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
22:18	RG_CSI0_LNR6_HSRX_OFFSET_CODE	**Lane6 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
17	RG_CSI0_LNR6_HSRX_CAL_EN	**Lane6 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
16	RG_CSI0_LNR6_HSRX_CAL_APPLY	**Lane6 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
14:10	RG_CSI0_LNR5_HSRX_OFFSET_CODE	**Lane5 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
9	RG_CSI0_LNR5_HSRX_CAL_EN	**Lane5 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
8	RG_CSI0_LNR5_HSRX_CAL_APPLY	**Lane5 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
6:2	RG_CSI0_LNR4_HSRX_OFFSET_CODE	**Lane4 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
1	RG_CSI0_LNR4_HSRX_CAL_EN	**Lane4 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
0	RG_CSI0_LNR4_HSRX_CAL_APPLY	**Lane4 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result

1A040808 MIPI_RX_CON08_CSI0 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_CSI0_LNR11_HSRX_OFFSET_CODE					RG_CSI0_LNR11_HSRX_CAL_EN	RG_CSI0_LNR11_HSRX_CAL_APPLY		RG_CSI0_LNR10_HSRX_OFFSET_CODE					RG_CSI0_LNR10_HSRX_CAL_EN	RG_CSI0_LNR10_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI0_LNR9_HSRX_OFFSET_CODE					RG_CSI0_LNR9_HSRX_CAL_EN	RG_CSI0_LNR9_HSRX_CAL_APPLY		RG_CSI0_LNR8_HSRX_OFFSET_CODE					RG_CSI0_LNR8_HSRX_CAL_EN	RG_CSI0_LNR8_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	RG_CSI0_LNR11_HSRX_OFFSET_CODE	**Lane11 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
25	RG_CSI0_LNR11_HSRX_CAL_EN	**Lane11 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
24	RG_CSI0_LNR11_HSRX_CAL_APPLY	**Lane11 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
22:18	RG_CSI0_LNR10_HSRX_OFFSET_CODE	**Lane10 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
17	RG_CSI0_LNR10_HSRX_CAL_EN	**Lane10 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
16	RG_CSI0_LNR10_HSRX_CAL_APPLY	**Lane10 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
14:10	RG_CSI0_LNR9_HSRX_OFFSET_CODE	**Lane9 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
9	RG_CSI0_LNR9_HSRX_CAL_EN	**Lane9 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
8	RG_CSI0_LNR9_HSRX_CAL_APPLY	**Lane9 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
6:2	RG_CSI0_LNR8_HSRX_OFFSET_CODE	**Lane8 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage

Bit(s)	Name	Description
		5'bx1111: maximum output voltage
1	RG_CSIo_LNR8_HSRX_CAL_EN	**Lane8 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
0	RG_CSIo_LNR8_HSRX_CAL_APPLY	**Lane8 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result

1A040824 MIPI_RX_CON24_CSIo **MIPI RX Config Register** **E4000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSIo_BIST_LN3_MUX		CSIo_BIST_LN2_MUX		CSIo_BIST_LN1_MUX		CSIo_BIST_LN0_MUX		CSIo_BIST_SETTLE_DELAY							
Type	RW		RW		RW		RW		RW							
Reset	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSIo_BIST_TERM_DELAY								CSIo_BIST_CLK4X_SEL	CSIo_BIST_CLK_SEL	CSIo_BIST_FIX_PAT			CSIo_BIST_EN	CSIo_BIST_NUM	
Type	RW								RW	RW	RW			RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0			0	0	0

Bit(s)	Name	Description
31:30	CSIo_BIST_LN3_MUX	**CSIo Lane mux**
29:28	CSIo_BIST_LN2_MUX	**CSIo Lane mux**
27:26	CSIo_BIST_LN1_MUX	**CSIo Lane mux**
25:24	CSIo_BIST_LN0_MUX	**CSIo Lane mux**
23:16	CSIo_BIST_SETTLE_DELAY	**CSIo Settle Delay Setting**
15:8	CSIo_BIST_TERM_DELAY	**CSIo Term Delay Setting**
7	CSIo_BIST_CLK4X_SEL	**CSIo CLK4X Sel** 0: inverse 1: not inverse
6	CSIo_BIST_CLK_SEL	**CSIo CLK Sel** 0: inverse 1: not inverse
5	CSIo_BIST_FIX_PAT	**CSIo Bist Patern** 0: Random 1: Fix
2	CSIo_BIST_EN	**CSIo Bist Enalbe**
1:0	CSIo_BIST_NUM	**CSIo Bist num** 0: 1 lane 1: 2 lane 2: 3 lane 3: 4 lane

1A040828 MIPI_RX_CON28_CSIo **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CSIo_BIST_CSI2_DATA_OK	CSIo_BIST_LANE_FSM_OK	CSIo_BIST_HS_FSM_OK	CSIo_BIST_DATA_OK	CSIo_BIST_START
Type												RO	RO	RO	RO	RO
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	CSIo_BIST_CSI2_DATA_OK	CSIo BIST CSI2 Data ok
3	CSIo_BIST_LANE_FSM_OK	CSIo BIST High Speed FSM ok
2	CSIo_BIST_HS_FSM_OK	CSIo BIST Data Lane FSM ok
1	CSIo_BIST_DATA_OK	CSIo BIST DPHY Data ok
0	CSIo_BIST_START	CSIo BIST start status

1A040834 MIPI_RX_CON34_CSIo — MIPI RX Config Register — E4000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSIo_BIST_LN7_MUX		CSIo_BIST_LN6_MUX		CSIo_BIST_LN5_MUX		CSIo_BIST_LN4_MUX		CSIo_BIST_HSDET_MUX							
Type	RW		RW		RW		RW		RW							
Reset	1	1	1	0	0	1	0	0	0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BIST_MODE
Type																RW
Reset																0

Bit(s)	Name	Description
31:30	CSIo_BIST_LN7_MUX	CSIo Lane mux
29:28	CSIo_BIST_LN6_MUX	CSIo Lane mux
27:26	CSIo_BIST_LN5_MUX	CSIo Lane mux
25:24	CSIo_BIST_LN4_MUX	CSIo Lane mux
23:22	CSIo_BIST_HSDET_MUX	CSIo HSDET mux
0	BIST_MODE	BIST mode enable

1A040838 MIPI_RX_CON38_CSIo — MIPI RX Config Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ckphase_trio2					rg_ckphase_trio1						rg_ckphase_trio0				
Type	RW					RW						RW				
Reset	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						MIPI_RX_SW_CPHY_RX_M	MIPI_RX_SW_CPHY_TX_M	MIPI_RX_SW_RST					MIPI_RX_HW_CAL_OPTIO	MIPI_RX_HW_CAL_START	MIPI_RX_SW_CAL_MODE	MIPI_RX_SW_CTRL_MODE

						ODE	ODE						N			
Type						RW	RW	RW					RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:27	rg_ckphase_trio2	
26:22	rg_ckphase_trio1	
20:16	rg_ckphase_trio0	
10	MIPI_RX_SW_CPHY_RX_MODE	**CPHY RX SW Control mode**
9	MIPI_RX_SW_CPHY_TX_MODE	**CPHY TX SW Control mode**
8:4	MIPI_RX_SW_RST	**SW reset**
3	MIPI_RX_HW_CAL_OPTION	**HW Calibration Option 0: 8cycle 1 :16cycle**
2	MIPI_RX_HW_CAL_START	**HW Calibration trigger**
1	MIPI_RX_SW_CAL_MODE	**SW Calibration mode**
0	MIPI_RX_SW_CTRL_MODE	**SW Control mode**

1A04083C MIPI_RX_CON3C_CSI0 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIPI_RX_SW_CTRL_															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIPI_RX_SW_CTRL_															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MIPI_RX_SW_CTRL_	**SW Control**

1A040840 MIPI_RX_CON40_CSI0 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_CSI0_LNRD3_HSRX_INVERT	RG_CSI0_LNRD3_LPRX_SWAP	RG_CSI0_LNRD2_HSRX_INVERT	RG_CSI0_LNRD2_LPRX_SWAP	RG_CSI0_LNRD1_HSRX_INVERT	RG_CSI0_LNRD1_LPRX_SWAP	RG_CSI0_LNRD0_HSRX_INVERT	RG_CSI0_LNRD0_LPRX_SWAP			RG_CSI0_LNRC_HSRX_INVERT	RG_CSI0_LNRC_LPRX_SWAP
Type					RW	RW	RW	RW	RW	RW	RW	RW			RW	RW
Reset					0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
11	RG_CSI0_LNRD3_HSRX_INVERT	
10	RG_CSI0_LNRD3_LPRX_SWAP	
9	RG_CSI0_LNRD2_HSRX_INVERT	
8	RG_CSI0_LNRD2_LPRX_SWAP	

Bit(s)	Name	Description
7	RG_CSI0_LNRD1_HSRX_INVERT	
6	RG_CSI0_LNRD1_LPRX_SWAP	
5	RG_CSI0_LNRD0_HSRX_INVERT	
4	RG_CSI0_LNRD0_LPRX_SWAP	
1	RG_CSI0_LNRC_HSRX_INVERT	
0	RG_CSI0_LNRC_LPRX_SWAP	

1A040844 MIPI_RX_CON44_CSI0 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSI0_LNR3_HSRX_OFFSET_CODE					DA_CSI0_LNR3_HSRX_CAL_EN	DA_CSI0_LNR3_HSRX_CAL_APPLY		DA_CSI0_LNR2_HSRX_OFFSET_CODE					DA_CSI0_LNR2_HSRX_CAL_EN	DA_CSI0_LNR2_HSRX_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DA_CSI0_LNR1_HSRX_OFFSET_CODE					DA_CSI0_LNR1_HSRX_CAL_EN	DA_CSI0_LNR1_HSRX_CAL_APPLY		DA_CSI0_LNR0_HSRX_OFFSET_CODE					DA_CSI0_LNR0_HSRX_CAL_EN	DA_CSI0_LNR0_HSRX_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	DA_CSI0_LNR3_HSRX_OFFSET_CODE	
25	DA_CSI0_LNR3_HSRX_CAL_EN	
24	DA_CSI0_LNR3_HSRX_CAL_APPLY	
22:18	DA_CSI0_LNR2_HSRX_OFFSET_CODE	
17	DA_CSI0_LNR2_HSRX_CAL_EN	
16	DA_CSI0_LNR2_HSRX_CAL_APPLY	
14:10	DA_CSI0_LNR1_HSRX_OFFSET_CODE	
9	DA_CSI0_LNR1_HSRX_CAL_EN	
8	DA_CSI0_LNR1_HSRX_CAL_APPLY	
6:2	DA_CSI0_LNR0_HSRX_OFFSET_CODE	
1	DA_CSI0_LNR0_HSRX_CAL_EN	
0	DA_CSI0_LNR0_HSRX_CAL_APPLY	

1A040848 MIPI_RX_CON48_CSI0 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name		DA_CSI0_L NR7_HSRX_ OFFSET_CO DE					DA_C SI0_ LNR7 _HSR X_CA L_EN	DA_C SI0_ LNR7 _HSR X_CA L_AP PLY		DA_CSI0_LNR6_HSRX_OFF SET_CODE					DA_C SI0_ LNR6 _HSR X_CA L_EN	DA_C SI0_ LNR6 _HSR X_CA L_AP PLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DA_CSI0_LNR5_HSRX_OFF SET_CODE					DA_C SI0_ LNR5 _HSR X_CA L_EN	DA_C SI0_ LNR5 _HSR X_CA L_AP PLY		DA_CSI0_LNR4_HSRX_OFF SET_CODE					DA_C SI0_ LNR4 _HSR X_CA L_EN	DA_C SI0_ LNR4 _HSR X_CA L_AP PLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	DA_CSI0_LNR7_HSRX_OFFSET_ CODE	
25	DA_CSI0_LNR7_HSRX_CAL_EN	
24	DA_CSI0_LNR7_HSRX_CAL_APP LY	
22:18	DA_CSI0_LNR6_HSRX_OFFSET_ CODE	
17	DA_CSI0_LNR6_HSRX_CAL_EN	
16	DA_CSI0_LNR6_HSRX_CAL_APP LY	
14:10	DA_CSI0_LNR5_HSRX_OFFSET_ CODE	
9	DA_CSI0_LNR5_HSRX_CAL_EN	
8	DA_CSI0_LNR5_HSRX_CAL_APP LY	
6:2	DA_CSI0_LNR4_HSRX_OFFSET_ CODE	
1	DA_CSI0_LNR4_HSRX_CAL_EN	
0	DA_CSI0_LNR4_HSRX_CAL_APP LY	

1A04084C MIPI_RX_CO N4C_CSI0 — MIPI RX Config Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSI0_L NR11_HSRX _OFFSET_C ODE					DA_C SI0_ LNR1 1_HS RX_C AL_E N	DA_C SI0_ LNR1 1_HS RX_C AL_A PPLY		DA_CSI0_LNR10_HSRX_OF FSET_CODE					DA_C SI0_ LNR1 0_HS RX_C AL_E N	DA_C SI0_ LNR1 0_HS RX_C AL_A PPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DA_CSI0_LNR9_HSRX_OFF SET_CODE					DA_C SI0_ LNR9 _HSR	DA_C SI0_ LNR9 _HSR		DA_CSI0_LNR8_HSRX_OFF SET_CODE					DA_C SI0_ LNR8 _HSR	DA_C SI0_ LNR8 _HSR

							X_CAL_EN	X_CAL_APPLY							X_CAL_EN	X_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	DA_CSI0_LNR11_HSRX_OFFSET_CODE	
25	DA_CSI0_LNR11_HSRX_CAL_EN	
24	DA_CSI0_LNR11_HSRX_CAL_APPLY	
22:18	DA_CSI0_LNR10_HSRX_OFFSET_CODE	
17	DA_CSI0_LNR10_HSRX_CAL_EN	
16	DA_CSI0_LNR10_HSRX_CAL_APPLY	
14:10	DA_CSI0_LNR9_HSRX_OFFSET_CODE	
9	DA_CSI0_LNR9_HSRX_CAL_EN	
8	DA_CSI0_LNR9_HSRX_CAL_APPLY	
6:2	DA_CSI0_LNR8_HSRX_OFFSET_CODE	
1	DA_CSI0_LNR8_HSRX_CAL_EN	
0	DA_CSI0_LNR8_HSRX_CAL_APPLY	

1A040850 MIPI_RX_CON50_CSI0 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_CSI0_BCLK_INV
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_CSI0_BCLK_INV	**CSI0 Byte Clock** 0: not inverse 1: inverse

1A04087C MIPI_RX_CON7C_CSI0 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DA_CSIo_LNRDo_HSRX_DELAY_CODE				DA_CSIo_LNRDo_HSRX_DELAY_APPLY	DA_CSIo_LNRDo_HSRX_DELAY_EN
Type											RO				RO	RO
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:2	DA_CSIo_LNRDo_HSRX_DELAY_CODE	
1	DA_CSIo_LNRDo_HSRX_DELAY_APPLY	
0	DA_CSIo_LNRDo_HSRX_DELAY_EN	

1A040880 MIPI_RX_CON80_CSIo **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DA_CSIo_LNRD1_HSRX_DELAY_CODE				DA_CSIo_LNRD1_HSRX_DELAY_APPLY	DA_CSIo_LNRD1_HSRX_DELAY_EN
Type											RO				RO	RO
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:2	DA_CSIo_LNRD1_HSRX_DELAY_CODE	
1	DA_CSIo_LNRD1_HSRX_DELAY_APPLY	
0	DA_CSIo_LNRD1_HSRX_DELAY_EN	

1A040884 MIPI_RX_CON84_CSIo **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name											DA_CSIo_LNRD2_HSRX_DELAY_CODE				DA_CSIo_LNRD2_HSRX_DELAY_APPLY	DA_CSIo_LNRD2_HSRX_DELAY_EN
Type											RO				RO	RO
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:2	DA_CSIo_LNRD2_HSRX_DELAY_CODE	
1	DA_CSIo_LNRD2_HSRX_DELAY_APPLY	
0	DA_CSIo_LNRD2_HSRX_DELAY_EN	

1A040888 MIPI_RX_CON88_CSIo **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DA_CSIo_LNRD3_HSRX_DELAY_CODE				DA_CSIo_LNRD3_HSRX_DELAY_APPLY	DA_CSIo_LNRD3_HSRX_DELAY_EN
Type											RO				RO	RO
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:2	DA_CSIo_LNRD3_HSRX_DELAY_CODE	
1	DA_CSIo_LNRD3_HSRX_DELAY_APPLY	
0	DA_CSIo_LNRD3_HSRX_DELAY_EN	

1A04088C MIPI_RX_CON8C_CSIo **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSIo_LNRDo_HSRX_DELAY_CODE						RG_CSIo_	RG_CSIo_

															LNRD0_HSRX_DELAY_APPLY	LNRD0_HSRX_DELAY_EN
Type									RW						RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSI0_LNRD0_HSRX_DELAY_CODE	
1	RG_CSI0_LNRD0_HSRX_DELAY_APPLY	
0	RG_CSI0_LNRD0_HSRX_DELAY_EN	

1A040890 MIPI_RX_CON90_CSI0 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSI0_LNRD1_HSRX_DELAY_CODE						RG_CSI0_LNRD1_HSRX_DELAY_APPLY	RG_CSI0_LNRD1_HSRX_DELAY_EN
Type									RW						RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSI0_LNRD1_HSRX_DELAY_CODE	
1	RG_CSI0_LNRD1_HSRX_DELAY_APPLY	
0	RG_CSI0_LNRD1_HSRX_DELAY_EN	

1A040894 MIPI_RX_CON94_CSI0 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSI0_LNRD2_HSRX_DELAY_CODE						RG_CSI0_LNRD2_HS	RG_CSI0_LNRD2_HS

															RX_DELAY_APPLY	RX_DELAY_EN
Type									RW						RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSIo_LNRD2_HSRX_DELAY_CODE	
1	RG_CSIo_LNRD2_HSRX_DELAY_APPLY	
0	RG_CSIo_LNRD2_HSRX_DELAY_EN	

1A040898 MIPI_RX_CON98_CSIo **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSIo_LNRD3_HSRX_DELAY_CODE						RG_CSIo_LNRD3_HSRX_DELAY_APPLY	RG_CSIo_LNRD3_HSRX_DELAY_EN
Type									RW						RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSIo_LNRD3_HSRX_DELAY_CODE	
1	RG_CSIo_LNRD3_HSRX_DELAY_APPLY	
0	RG_CSIo_LNRD3_HSRX_DELAY_EN	

1A0408A0 MIPI_RX_CONA0_CSIo **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSIo_LNRC_HSRX_DELAY_CODE						RG_CSIo_LNRC_HSRX_DELAY_	RG_CSIo_LNRC_HSRX_DELAY_

															APPLY	EN
Type									RW						RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSI0_LNRC_HSRX_DELAY_CODE	
1	RG_CSI0_LNRC_HSRX_DELAY_APPLY	
0	RG_CSI0_LNRC_HSRX_DELAY_EN	

1A0408B0 MIPI_RX_CONB0_CSI0 **Deskew control register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DESKEW_ENABLE	DESKEW_IP_SEL														DESKEW_CSI2_RST_ENABLE
Type	RW	RW														RW
Reset	0	0														0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DESKEW_ACC_MODE					DESKEW_TRIGGER_MODE			DESKEW_SW_RST				Delay_APPLY_MODE			
Type	RW					RW			RW				RW			
Reset	0	0	0	0		0	0	0	0				0	0	0	0

Bit(s)	Name	Description
31	DESKEW_ENABLE	**Deskew enable**
30	DESKEW_IP_SEL	0: New IP 1: Old IP
16	DESKEW_CSI2_RST_ENABLE	**Reset CSI2 IP when in DESKEW mode**
15:12	DESKEW_ACC_MODE	**Deskew edge mode**
10:8	DESKEW_TRIGGER_MODE	**Conditions for trigger DESKEW function**
7	DESKEW_SW_RST	**Deskew SW reset**
3:0	Delay_APPLY_MODE	**Delay apply mode:** 00/01: HW mode 10: RG mode 11: SW mode

1A0408B4 MIPI_RX_CONB4_CSI0 **Deskew sync detection sequence** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EXPECTED_SYNC_CODE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYNC_CODE_MASK															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	EXPECTED_SYNC_CODE	Programmable sync code. In normal case, it should be 16'hFFFF.
15:0	SYNC_CODE_MASK	When the bit is set to 1'b1, HW will compare its value with received sync code. Otherewise, no compare.

1A0408B8 MIPI_RX_CONB8_CSIo — Deskew timing control — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								DESKEW_TIME_OUT_EN	DESKEW_TIME_OUT							
Type								RW	RW							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DESKEW_HOLD_TIME								DESKEW_SETUP_TIME			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
24	DESKEW_TIME_OUT_EN	**Deskew time out enable.**
23:16	DESKEW_TIME_OUT	**Deskew time out period.** If no deskew sync code is detected, FSM will be reset after this period.
11:8	DESKEW_HOLD_TIME	**Delay code apply hold time**
3:0	DESKEW_SETUP_TIME	**Delay code apply setup time**

1A0408BC MIPI_RX_CONBC_CSIo — Deskew mode — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							DESKEW_LANE_NUMBER						DESKEW_DELAY_APPLY_MODE			
Type							RW						RW			
Reset							0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DESKEW_DETECTION_CNT											DESKEW_DETECTION_MODE			
Type		RW											RW			
Reset		0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
25:24	DESKEW_LANE_NUMBER	Deskew lane number
19:16	DESKEW_DELAY_APPLY_MODE	Deskew delay apply mode
14:8	DESKEW_DETECTION_CNT	Deskew detection count
3:0	DESKEW_DETECTION_MODE	Deskew detection mode

Bit(s)	Name	Description

1A0408C0 MIPI_RX_CONC0_CSI0 Interrupt enable 80000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DESKEW_INTERRUPT_W1C_EN															
Type	RW															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DESKEW_INTERRUPT_ENABLE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	DESKEW_INTERRUPT_W1C_EN	Interrupt W1C enable
7:0	DESKEW_INTERRUPT_ENABLE	Interrupt enable

1A0408C4 MIPI_RX_CONC4_CSI0 Interrupt status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DESKEW_INTERRUPT_STATUS							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DESKEW_INTERRUPT_STATUS	Interrupt status

1A0408C8 MIPI_RX_CONC8_CSI0 Debug mux select 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DESKEW_DEBUG_MUX_SELECT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DESKEW_DEBUG_MUX_SELECT	Debug signal select

1A0408CC MIPI_RX_CONCC_CSI0 **Debug outputs** **00100100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DESKEW_DEBUG_OUTPUTS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DESKEW_DEBUG_OUTPUTS															
Type	RO															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DESKEW_DEBUG_OUTPUTS	Debug signal outputs

1A0408D0 MIPI_RX_COND0_CSI0 **Deskew delay length** **0000000F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DESKEW_DELAY_LENGTH						
Type											RW					
Reset											0	0	1	1	1	1

Bit(s)	Name	Description
5:0	DESKEW_DELAY_LENGTH	Deskew delay length

Module name: seninf1_mux Base address: (+1a040d00h)

Address	Name	Width	Register Function
1A040D00	SENINF1_MUX_CTRL	32	SENINF 1 Control Register
1A040D04	SENINF1_MUX_INTEN	32	SENINF 1 Interrupt Enable Register
1A040D08	SENINF1_MUX_INTSTA	32	SENINF 1 Interrupt Status Register
1A040D0C	SENINF1_MUX_SIZE	32	SENINF 1 Image Size Register
1A040D10	SENINF1_MUX_DEBUG_1	32	SENINF 1 Debug Register 1
1A040D14	SENINF1_MUX_DEBUG_2	32	SENINF 1 Debug Register 2
1A040D18	SENINF1_MUX_DEBUG_3	32	SENINF 1 Debug Register 3

Address	Name	Width	Register Function
1A040D1C	SENINF1_MUX_DEBUG_4	32	SENINF 1 Debug Register 4
1A040D20	SENINF1_MUX_DEBUG_5	32	SENINF 1 Debug Register 5
1A040D24	SENINF1_MUX_DEBUG_6	32	SENINF 1 Debug Register 6
1A040D28	SENINF1_MUX_DEBUG_7	32	SENINF 1 Debug Register 7
1A040D2C	SENINF1_MUX_SPARE	32	SENINF 1 Spare Register
1A040D30	SENINF1_MUX_DATA	32	SENINF 1 Data Register
1A040D34	SENINF1_MUX_DATA_CNT	32	SENINF 1 Data Count Register
1A040D38	SENINF1_MUX_CROP	32	SENINF 1 Crop Size Register
1A040D3C	SENINF1_MUX_CTRL_EXT	32	SENINF 1 Control Register Extend

1A040D00 SENINF1_MUX_CTRL **SENINF 1 Control Register** **06DF0080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_MUX_EN	CROP_EN	FIFO_FULL_WR_EN		FIFO_FLUSH_EN						FIFO_PUSH_EN					
Type	RW	RW	RW		RW						RW					
Reset	0	0	0	0	0	1	1	0	1	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_SRC_SEL				OVERRUN_RST_EN	SENINF_HSYNC_POL	SENINF_VSYNC_POL	SENINF_PIX_SEL	SENINF_HSYNC_MASK		SENINF_MUX_RDY_VALUE	SENINF_MUX_RDY_MODE			SENINF_IRQ_SW_RST	SENINF_MUX_SW_RST
Type	RW				RW	RW	RW	RW	RW		RW	RW			RW	RW
Reset	0	0	0	0	0	0	0	0	1		0	0			0	0

Bit(s)	Name	Description
31	SENINF_MUX_EN	**Enables seninf_mux** 0: Disable 1: Enable
30	CROP_EN	**Sensor crop function**
29:28	FIFO_FULL_WR_EN	0: FIFO write operation is prohibited when FIFO is full. 1: FIFO write operation is prohibited after FIFO full occurs. 2: FIFO write operation is allowed when FIFO is full.
27:22	FIFO_FLUSH_EN	**Normal mode: 6'b011011** JPEG two pixel mode: 6'b011000
21:16	FIFO_PUSH_EN	**Normal mode: 6'b011111** JPEG two pixel mode : 6'b011110
15:12	SENINF_SRC_SEL	**Selects SENINF input source:** {seninf_mux_sel_ext, seninf_mux_sel} 00: OCSI2 VC0 01: Test model 02: CCIR656

Bit(s)	Name	Description
		03: Parallel sensor 04: Serial sensor 06: OCSI2 VC1 08: NCSI2 VC0 09: NCSI2 VC1 0A: NCSI2 VC2 0B: NCSI2 VC3 0C: NCSI2 VC4 0D: NCSI2 VC5
11	OVERRUN_RST_EN	**Enables SENINF mux software reset for overrun** 0: No action 1: Auto self-reset for overrun situation
10	SENINF_HSYNC_POL	**SENINF HSYNC polarity**
9	SENINF_VSYNC_POL	**SENINF VSYNC polarity**
8	SENINF_PIX_SEL	**SENINF output bus width:** {seninf_pixel_sel_ext, seninf_pixel_sel} 00: 1 pixel/cycle 01: 2 pixels/cycle 10: 4 pixels/cycle
7	SENINF_HSYNC_MASK	**Masks hsync** 0: Send hsync when vsync = 1 1: Does not send hsync when vsync = 1
5	SENINF_MUX_RDY_VALUE	**seninf_rdy value in force mode**
4	SENINF_MUX_RDY_MODE	0: seninf_rdy normal mode 1: seninf_rdy force mode
1	SENINF_IRQ_SW_RST	**SENINF IRQ software reset, active high** 0: De-assert reset 1: Assert reset
0	SENINF_MUX_SW_RST	**SENINF mux software reset, active high** 0: De-assert reset 1: Assert reset

1A040D04 SENINF1_MUX_INTEN **SENINF 1 Interrupt Enable Register** **8000007F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_IRQ_CLR_SEL															
Type	RW															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SENINF_SENSOR_HSIZEERR_IRQ_EN	SENINF_SENSOR_VSIZEERR_IRQ_EN	SENINF_HSIZEERR_IRQ_EN	SENINF_VSIZEERR_IRQ_EN	SENINF_FSMERR_IRQ_EN	SENINF_CRCERR_IRQ_EN	SENINF_OVERRUN_IRQ_EN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										1	1	1	1	1	1	1

Bit(s)	Name	Description

Bit(s)	Name	Description
31	SENINF_IRQ_CLR_SEL	0: Read clear 1: Write clear
6	SENINF_SENSOR_HSIZEERR_IRQ_EN	Enables sensor HSIZE ERROR IRQ
5	SENINF_SENSOR_VSIZEERR_IRQ_EN	Enables sensor VSIZE ERROR IRQ
4	SENINF_HSIZEERR_IRQ_EN	Enables async FIFO HSIZE ERROR IRQ
3	SENINF_VSIZEERR_IRQ_EN	Enables async FIFO VSIZE ERROR IRQ
2	SENINF_FSMERR_IRQ_EN	Enables FSM ERROR IRQ
1	SENINF_CRCERR_IRQ_EN	Enables CRR ERROR IRQ
0	SENINF_OVERRUN_IRQ_EN	Enables FIFO OVERRUN IRQ

1A040D08 SENINF1_MUX_INTSTA SENINF 1 Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SENINF_SENSOR_HSIZEERR_IRQ_STA	SENINF_SENSOR_VSIZEERR_IRQ_STA	SENINF_HSIZEERR_IRQ_STA	SENINF_VSIZEERR_IRQ_STA	SENINF_FSMERR_IRQ_STA	SENINF_CRCERR_IRQ_STA	SENINF_OVERRUN_IRQ_STA
Type										RO	RO	RO	RO	RO	RO	RO
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	SENINF_SENSOR_HSIZEERR_IRQ_STA	Sensor HSIZE ERROR IRQ status
5	SENINF_SENSOR_VSIZEERR_IRQ_STA	Sensor VSIZE ERROR IRQ status
4	SENINF_HSIZEERR_IRQ_STA	Async FIFO HSIZE ERROR IRQ status
3	SENINF_VSIZEERR_IRQ_STA	Async FIFO VSIZE ERROR IRQ status
2	SENINF_FSMERR_IRQ_STA	FSM ERROR IRQ status
1	SENINF_CRCERR_IRQ_STA	CRR ERROR IRQ status
0	SENINF_OVERRUN_IRQ_STA	FIFO OVERRUN IRQ status

1A040D0C SENINF1_MUX_SIZE SENINF 1 Image Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_HSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_VSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_HSIZE	Senor image horizontal size
15:0	SENINF_VSIZE	Senor image vertical size

1A040D10 SENINF1_MUX_DEBUG_1 **SENINF 1 Debug Register 1** **0000C303**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	1	1	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A040D14 SENINF1_MUX_DEBUG_2 **SENINF 1 Debug Register 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A040D18 SENINF1_MUX_DEBUG_3 **SENINF 1 Debug Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A040D1C SENINF1_MUX_DEBUG_4 SENINF 1 Debug Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A040D20 SENINF1_MUX_DEBUG_5 SENINF 1 Debug Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A040D24 SENINF1_MUX_DEBUG_6 SENINF 1 Debug Register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A040D28 SENINF1_MUX_DEBUG_7 SENINF 1 Debug Register 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A040D2C SENINF1_MUX_SPARE SENINF 1 Spare Register 000E2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SENI NF_S PARE			
Type													RW			
Reset													1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENI NF_S PARE		SENI NF_F IFO_ FULL _SEL	SENI NF_V CNT_ SEL		SENINF_CR C_SEL										
Type	RW		RW	RW		RW										
Reset	0	0	1	0	0	0	0									

Bit(s)	Name	Description
19:14	SENINF_SPARE	**Spare register**
13	SENINF_FIFO_FULL_SEL	0: Does not send FIFO full to cam 1: Send FIFO full to cam
12:11	SENINF_VCNT_SEL	0: Vsync rising 1: Vsync rising d1 2: Vsync rising d2 3: Vsync rising d3
10:9	SENINF_CRC_SEL	0: Vsync rising 1: Vsync rising d1 2: Vsync rising d2 3: Vsync rising d3

1A040D30 SENINF1_MUX_DATA SENINF 1 Data Register 40000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA1															
Type	RO															
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_DATA1	

Bit(s)	Name	Description
15:0	SENINF_DATA0	

1A040D34 SENINF1_MUX_DATA_CNT — SENINF 1 Data Count Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENINF_DATA_CNT	

1A040D38 SENINF1_MUX_CROP — SENINF 1 Crop Size Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_CROP_X2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_CROP_X1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_CROP_X2	
15:0	SENINF_CROP_X1	

1A040D3C SENINF1_MUX_CTRL_EXT — SENINF 1 Control Register Extend — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												SENINF_PIX_SEL_EXT			SENINF_SRC_SEL_EXT	
Type												RW			RW	
Reset												0			0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
4	SENINF_PIX_SEL_EXT	**SENINF output bus width:** {seninf_pixel_sel_ext, seninf_pixel_sel} 00: 1 pixel/cycle 01: 2 pixels/cycle 10: 4 pixels/cycle
1:0	SENINF_SRC_SEL_EXT	**Selects SENINF input source:** {seninf_src_sel_ext, seninf_src_sel} 18: CSI2 VC0 19: CSI2 VC1 1A: CSI2 VC2 1B: CSI2 VC3 1C: CSI2 VC4 28: CSI3 VC0 29: CSI3 VC1 2A: CSI3 VC2 2B: CSI3 VC3 2C: CSI3 VC4

Module name: SENINF1_NCSI2 Base address: (+1a040700h)

Address	Name	Width	Register Function
1A040700	SENINF1_NCSI2_CTL	32	CSI2 Function Enable
1A040704	SENINF1_NCSI2_LNRC_TIMING	32	CSI2 Clock Lane Timing Parameters
1A040708	SENINF1_NCSI2_LNRD_TIMING	32	CSI2 Data Lane Timing Parameters
1A04070C	SENINF1_NCSI2_DPCM	32	CSI2 DPCM Parameters
1A040710	SENINF1_NCSI2_INT_EN	32	CSI2 Interrupt Enable
1A040714	SENINF1_NCSI2_INT_STATUS	32	CSI2 Interrupt Status
1A040718	SENINF1_NCSI2_DGB_SEL	32	CSI2 Debug Selection
1A04071C	SENINF1_NCSI2_DBG_PORT	32	CSI2 Debug Port
1A040720	SENINF1_NCSI2_SPARE0	32	SPARE0
1A040724	SENINF1_NCSI2_SPARE1	32	SPARE1
1A040728	SENINF1_NCSI2_LNRC_FSM	32	CSI2 Clock Lane RX FSM
1A04072C	SENINF1_NCSI2_LNRD_FSM	32	CSI2 Data Lane RX FSM
1A040730	SENINF1_NCSI2_FRAME_LINE_NUM	32	CSI2 Frame/Line Number
1A040734	SENINF1_NCSI2_GENERIC_SHORT	32	CSI2 Generic Short Packet
1A040738	SENINF1_NCSI2_HSRX_DBG	32	CSI2 HSRX Enable
1A04073C	SENINF1_NCSI2_DI	32	CSI2 Data Interleaving Parameters
1A040740	SENINF1_NCSI2_	32	CSI2 HS Trail Timing Parameters

Address	Name	Width	Register Function
	HS_TRAIL		
1A040744	SENINF1_NCSI2_DI_CTRL	32	CSI2 Data Interleaving Control
1A040748	SENINF1_NCSI2_DI_1	32	CSI2 Data Interleaving Parameters
1A04074C	SENINF1_NCSI2_DI_CTRL_1	32	CSI2 Data Interleaving Control
1A040750	SENINF1_NCSI2_DPHY_RESYNC_CTL	32	CSI2 DPHY Lane resync Control

1A040700 SENINF1_NCSI2_CTL **CSI2 Function Enable** **018861E0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			VS_OUT_CYCLE_NUMBER		CLOCK_HS_OPTION	REF_SYNC_DET_EN	HS_TRAIL_EN	ASYNC_FIFO_RST_SCH		SYNC_DET_BITSWAP_EN	SYNC_DET_EN	SYNC_DET_SCHEME	FLUSH_MODE			ED_SEL
Type			RW		RW	RW	RW	RW		RW	RW	RW	RW			RW
Reset			0	0	0	0	0	1	1	0	0	0	1	0		0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VS_TYPE	BYTE2PIXEL_EN	IMAGE_PACKET_EN	GENERIC_LONG_PACKET_EN			HS_END_EN	HS_PRPR_EN	HSRX_DET_EN	CRC_EN	ECC_EN	CLOCK_LANE_EN	DATA_LANE3_EN	DATA_LANE2_EN	DATA_LANE1_EN	DATA_LANE0_EN
Type	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	1	1	0			0	1	1	1	1	0	0	0	0	0

Bit(s)	Name	Description
29:28	VS_OUT_CYCLE_NUMBER	0: 4T 1: 8T
27	CLOCK_HS_OPTION	0: Enable clock lane HS based on LP11, LP01, LP00 1: Enable clock lane HS based on LP00
26	REF_SYNC_DET_EN	**Reference sync detect signal to do analog sync**
25	HS_TRAIL_EN	**Extends HS trail**
24:23	ASYNC_FIFO_RST_SCH	
22	SYNC_DET_BITSWAP_EN	
21	SYNC_DET_EN	**Enables sync sequence detection**
20	SYNC_DET_SCHEME	0: B8 1: 101110
19:18	FLUSH_MODE	0: Disable 1: Flush at first cycle of LP11 2: Flush at LP11 3: Reserved
16	ED_SEL	0: {WCH,WCL,DI} 1: {DI,WCL,WCH}
15	VS_TYPE	**VS type** 0: 4T 1: Frame start to frame end
14	BYTE2PIXEL_EN	**Byte 2 pixel conversion**
13	IMAGE_PACKET_EN	**Image data types**
12	GENERIC_LONG_PACKET_EN	**Generic long packet Data types**

Bit(s)	Name	Description
9	HS_END_EN	**Enables HS_EX reset at packet end**
8	HS_PRPR_EN	**Enables RX_HS_PRPR state**
7	HSRX_DET_EN	**Enables HSRX termination auto-detection flow**
6	CRC_EN	**Enables checksum**
5	ECC_EN	**Enables packet header ECC**
4	CLOCK_LANE_EN	**Enables clock lane**
3	DATA_LANE3_EN	**Enables data lane 3**
2	DATA_LANE2_EN	**Enables data lane 2**
1	DATA_LANE1_EN	**Enables data lane 1**
0	DATA_LANE0_EN	**Enables data lane 0**

1A040704 SENINF1_NCSI2_LNRC_TIMING **CSI2 Clock Lane Timing Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SETTLE_PARAMETER								TERM_PARAMETER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	SETTLE_PARAMETER	TD_SETTLE parameter
7:0	TERM_PARAMETER	TD_TERM_EN parameter

1A040708 SENINF1_NCSI2_LNRD_TIMING **CSI2 Data Lane Timing Parameters** **00002000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SETTLE_PARAMETER								TERM_PARAMETER							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	SETTLE_PARAMETER	TD_SETTLE parameter
7:0	TERM_PARAMETER	TD_TERM_EN parameter

1A04070C SENINF1_NCSI2_DPCM **CSI2 DPCM Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DI_2A_DPCM_EN	DI_37_DPCM_EN	DI_36_DPCM_EN	DI_35_DPCM_EN	DI_34_DPCM_EN	DI_33_DPCM_EN	DI_32_DPCM_EN	DI_31_DPCM_EN	DI_30_DPCM_EN				DPCM_MODE			
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW				RW			
Reset	0	0	0	0	0	0	0	0	0				0	0	0	0

Bit(s)	Name	Description
15	DI_2A_DPCM_EN	**Enables DPCM**
14	DI_37_DPCM_EN	**Enables DPCM**
13	DI_36_DPCM_EN	**Enables DPCM**
12	DI_35_DPCM_EN	**Enables DPCM**
11	DI_34_DPCM_EN	**Enables DPCM**
10	DI_33_DPCM_EN	**Enables DPCM**
9	DI_32_DPCM_EN	**Enables DPCM**
8	DI_31_DPCM_EN	**Enables DPCM**
7	DI_30_DPCM_EN	**Enables DPCM**
3:0	DPCM_MODE	0: 10-8-10

1A040710 SENINF1_NCSI2_INT_EN **CSI2 Interrupt Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_WCLR_EN					DPHY3_RESYNC_FIFO_OVERFLOW	DPHY2_RESYNC_FIFO_OVERFLOW	DPHY1_RESYNC_FIFO_OVERFLOW	DPHY0_RESYNC_FIFO_OVERFLOW	ERR_LANE_RESYNC	ERR_FRAME_SYNC_S5	ERR_FRAME_SYNC_S4	ERR_FRAME_SYNC_S3	ERR_FRAME_SYNC_S2	ERR_FRAME_SYNC_S1	ERR_FRAME_SYNC_S0
Type	RW					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0					0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GS	LS	FS	ERR_SOT_SYNC_HS_LNRD3	ERR_SOT_SYNC_HS_LNRD2	ERR_SOT_SYNC_HS_LNRD1	ERR_SOT_SYNC_HS_LNRD0	ERR_MULTI_LANE_SYNC	ERR_AFIFO	ERR_CRC	ERR_ECC_DOUBLE	ERR_ECC_CORRECTED	ERR_ECC_NO_ERROR	ERR_ID	ERR_FRAME_SYNC
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	INT_WCLR_EN	Enables Interrupt write clear
26	DPHY3_RESYNC_FIFO_OVERFLOW	Enables LANE3_RESYNC_FIFO_OVERFLOW interrupt
25	DPHY2_RESYNC_FIFO_OVERFLOW	Enables LANE2_RESYNC_FIFO_OVERFLOW interrupt
24	DPHY1_RESYNC_FIFO_OVERFLOW	Enables LANE1_RESYNC_FIFO_OVERFLOW interrupt
23	DPHY0_RESYNC_FIFO_OVERFLOW	Enables LANE0_RESYNC_FIFO_OVERFLOW interrupt
22	ERR_LANE_RESYNC	Enables ERR_LANE_RESYNC interrupt
21	ERR_FRAME_SYNC_S5	Enables ERR_FRAME_SYNC interrupt
20	ERR_FRAME_SYNC_S4	Enables ERR_FRAME_SYNC interrupt
19	ERR_FRAME_SYNC_S3	Enables ERR_FRAME_SYNC interrupt

Bit(s)	Name	Description
18	ERR_FRAME_SYNC_S2	Enables ERR_FRAME_SYNC interrupt
17	ERR_FRAME_SYNC_S1	Enables ERR_FRAME_SYNC interrupt
16	ERR_FRAME_SYNC_S0	Enables ERR_FRAME_SYNC interrupt t
14	GS	Enables generic short packet interrupt
13	LS	Enables line start interrupt
12	FS	Enables frame start interrupt
11	ERR_SOT_SYNC_HS_LNRD3	Enables ERR_SOT_SYNC_HS interrupt
10	ERR_SOT_SYNC_HS_LNRD2	Enables ERR_SOT_SYNC_HS interrupt
9	ERR_SOT_SYNC_HS_LNRD1	Enables ERR_SOT_SYNC_HS interrupt
8	ERR_SOT_SYNC_HS_LNRD0	Enables ERR_SOT_SYNC_HS interrupt
7	ERR_MULTI_LANE_SYNC	Enables ERR_MULTI_LANE_SYNC interrupt
6	ERR_AFIFO	Enables ERR_AFIFO interrupt
5	ERR_CRC	Enables ERR_CRC interrupt
4	ERR_ECC_DOUBLE	Enables ERR_ECC_DOUBLE interrupt
3	ERR_ECC_CORRECTED	Enables ERR_ECC_CORRECTED interrupt
2	ERR_ECC_NO_ERROR	ERR_ECC_NO_ERROR interrupt
1	ERR_ID	Enables ERR_ID interrupt
0	ERR_FRAME_SYNC	Enables ERR_FRAME_SYNC interrupt

1A040714 SENINF1_NCSI2_INT_STATUS CSI2 Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						DPHY3_RESYNC_FIFO_OVERFLOW_STA	DPHY2_RESYNC_FIFO_OVERFLOW_STA	DPHY1_RESYNC_FIFO_OVERFLOW_STA	DPHY0_RESYNC_FIFO_OVERFLOW_STA	ERR_LANE_RESYNC_STA	ERR_FRAME_SYNC_S5	ERR_FRAME_SYNC_S4	ERR_FRAME_SYNC_S3	ERR_FRAME_SYNC_S2	ERR_FRAME_SYNC_S1	ERR_FRAME_SYNC_S0
Type						RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GS	LS	FS	ERR_SOT_SYNC_HS_LNRD3	ERR_SOT_SYNC_HS_LNRD2	ERR_SOT_SYNC_HS_LNRD1	ERR_SOT_SYNC_HS_LNRD0	ERR_MULTI_LANE_SYNC	ERR_AFIFO	ERR_CRC	ERR_ECC_DOUBLE	ERR_ECC_CORRECTED	ERR_ECC_NO_ERROR	ERR_ID	ERR_FRAME_SYNC
Type		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26	DPHY3_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of DPHY lane 3 is overflowed**
25	DPHY2_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of DPHY lane 2 is overflowed**
24	DPHY1_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of DPHY lane 1 is overflowed**
23	DPHY0_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of DPHY lane 0 is overflowed**
22	ERR_LANE_RESYNC_STA	**Asserted when DPHY lane sync detect time is longer than set resync cycles**
21	ERR_FRAME_SYNC_S5	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
20	ERR_FRAME_SYNC_S4	**Asserted when a Frame End is not paired with a**

Bit(s)	Name	Description
		Frame Start on the same virtual channel
19	ERR_FRAME_SYNC_S3	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
18	ERR_FRAME_SYNC_S2	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
17	ERR_FRAME_SYNC_S1	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
16	ERR_FRAME_SYNC_S0	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
14	GS	**Enables generic short packet interrupt**
13	LS	**Line start interrupt**
12	FS	**Frame start interrupt**
11	ERR_SOT_SYNC_HS_LNRD3	**Asserted when proper synchronization cannot be expected**
10	ERR_SOT_SYNC_HS_LNRD2	**Asserted when proper synchronization cannot be expected**
9	ERR_SOT_SYNC_HS_LNRD1	**Asserted when proper synchronization cannot be expected**
8	ERR_SOT_SYNC_HS_LNRD0	**Asserted when proper synchronization cannot be expected**
7	ERR_MULTI_LANE_SYNC	**Asserted when multiple lane synchronization fails**
6	ERR_AFIFO	**Asserted when error occurs in asynchronous FIFO**
5	ERR_CRC	**Asserted when computed CRC code is different from received CRC code**
4	ERR_ECC_DOUBLE	**Asserted when an ECC syndrome is computed and two bit-errors are detected in the received packet header**
3	ERR_ECC_CORRECTED	**Asserted when an ECC syndrome is computed and a single bit-error in the packet header was detected and corrected**
2	ERR_ECC_NO_ERROR	**Asserted when an ECC syndrome is computed and the result is zero indicating a packet header that is considered to be without errors or has more than two bit errors** SI-2's ECC mechanism cannot detect this type of error.
1	ERR_ID	**Asserted whean a packet header is decoded with an unrecognized or unimplemented data ID**
0	ERR_FRAME_SYNC	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**

1A040718 SENINF1_NCSI2_DGB_SEL **CSI2 Debug Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DEBUG_SEL							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DEBUG_SEL	Selects debug

1A04071C SENINF1_NCSI2_DBG_PORT CSI2 Debug Port 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CTL_DBG_PORT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	CTL_DBG_PORT	Debug port

1A040720 SENINF1_NCSI2_SPARE0 SPARE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE0	Spare register

1A040724 SENINF1_NCSI2_SPARE1 SPARE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE1	Spare register

1A040728 SENINF1_NCSI2_LNRC_FSM CSI2 Clock Lane RX FSM 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											LNRC_RX_FSM					
Type											RO					
Reset											0	0	0	0	0	1

Bit(s)	Name	Description
5:0	LNRC_RX_FSM	RX FSM of clock lane

1A04072C SENINF1_NCSI2_LNRD_FSM CSI2 Data Lane RX FSM 01010101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LNRD3_RX_FSM								LNRD2_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		LNRD1_RX_FSM								LNRD0_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1

Bit(s)	Name	Description
30:24	LNRD3_RX_FSM	RX FSM of data lane 3
22:16	LNRD2_RX_FSM	RX FSM of data lane 2
14:8	LNRD1_RX_FSM	RX FSM of data lane 1
6:0	LNRD0_RX_FSM	RX FSM of data lane 0

1A040730 SENINF1_NCSI2_FRAME_LINE_NUM CSI2 Frame/Line Number 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LINE_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FRAME_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	LINE_NUM	Line number
15:0	FRAME_NUM	Frame number

1A040734 SENINF1_NC CSI2 Generic Short Packet 00000000

SI2_GENERIC_SHORT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GENERIC_SHORT_PACKET_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											GENERIC_SHORT_PACKET_DT						
Type											RO					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
31:16	GENERIC_SHORT_PACKET_DATA	Generic short packet data
5:0	GENERIC_SHORT_PACKET_DT	Generic short packet data

1A040738 SENINF1_NCSI2_HSRX_DBG **CSI2 HSRX Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLOCK_LANE_HSRX_EN	DATA_LANE3_HSRX_EN	DATA_LANE2_HSRX_EN	DATA_LANE1_HSRX_EN	DATA_LANE0_HSRX_EN
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	CLOCK_LANE_HSRX_EN	Enables clock lane HSRX circut
3	DATA_LANE3_HSRX_EN	Enables data lane 3 HSRX circuit
2	DATA_LANE2_HSRX_EN	Enables data lane 2 HSRX circuit
1	DATA_LANE1_HSRX_EN	Enables data lane 1 HSRX circuit
0	DATA_LANE0_HSRX_EN	Enables data lane 0 HSRX circuit

1A04073C SENINF1_NCSI2_DI **CSI2 Data Interleaving Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DT3						VC3		DT2						VC2	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DT1						VC1		DT0						VC0	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
31:26	DT3	Data type indentifier
25:24	VC3	Virtual channel indentifier
23:18	DT2	Data type indentifier
17:16	VC2	Virtual channel indentifier
15:10	DT1	Data type indentifier
9:8	VC1	Virtual channel indentifier
7:2	DT0	Data type indentifier
1:0	VC0	Virtual channel indentifier

1A040740 SENINF1_NCSI2_HS_TRAIL **CSI2 HS Trail Timing Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									HS_TRAIL_PARAMETER							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	HS_TRAIL_PARAMETER	HS trail parameter

1A040744 SENINF1_NCSI2_DI_CTRL **CSI2 Data Interleaving Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						DT3_INTERLEAVING		VC3_INTERLEAVING						DT2_INTERLEAVING		VC2_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DT1_INTERLEAVING		VC1_INTERLEAVING						DT0_INTERLEAVING		VC0_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0

Bit(s)	Name	Description
26:25	DT3_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
24	VC3_INTERLEAVING	**Virtual channel identifier interleaving**
18:17	DT2_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include

Bit(s)	Name	Description
		2: Exclude
16	VC2_INTERLEAVING	**Virtual channel identifier interleaving**
10:9	DT1_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
8	VC1_INTERLEAVING	**Virtual channel identifier interleaving**
2:1	DT0_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
0	VC0_INTERLEAVING	**Virtual channel identifier interleaving**

1A040748 SENINF1_NCSI2_DI_1 **CSI2 Data Interleaving Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DT5						VC5		DT4						VC4	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:10	DT5	Data type indentifier
9:8	VC5	Virtual channel indentifier
7:2	DT4	Data type indentifier
1:0	VC4	Virtual channel indentifier

1A04074C SENINF1_NCSI2_DI_CTRL_1 **CSI2 Data Interleaving Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DT5_INTERLEAVING		VC5_INTERLEAVING						DT4_INTERLEAVING		VC4_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0

Bit(s)	Name	Description
10:9	DT5_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude

Bit(s)	Name	Description
8	VC5_INTERLEAVING	**Virtual channel identifier interleaving**
2:1	DT4_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
0	VC4_INTERLEAVING	**Virtual channel identifier interleaving**

1A040750 SENINF1_NCSI2_DPHY_RESYNC_CTL CSI2 DPHY Lane resync Control 00000101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DPHY_RESYNC_CNT								DPHY_RESYNC_FLUSH_EN	DPHY_RESYNC_DATAOUT_OPTION	DPHY_BYPASS_LANE_RESYNC
Type						RW								RW	RW	RW
Reset						0	0	1						0	0	1

Bit(s)	Name	Description
10:8	DPHY_RESYNC_CNT	Detects lane skew cycle count
2	DPHY_RESYNC_FLUSH_EN	Enables lane resync flush
1	DPHY_RESYNC_DATAOUT_OPTION	Data output option
0	DPHY_BYPASS_LANE_RESYNC	Bypass lane resync function

Module name: seninf1_ocsi2 Base address: (+1a040300h)

Address	Name	Width	Register Function
1A040360	SENINF1_OCSI2_CTRL	32	CSI2 Control Register
1A040364	SENINF1_OCSI2_DELAY	32	CSI2 Delay Control Register
1A040368	SENINF1_OCSI2_INTEN	32	CSI2 Interrupt Enable Register
1A04036C	SENINF1_OCSI2_INTSTA	32	CSI2 Interrupt Status Register
1A040370	SENINF1_OCSI2_ECCDBG	32	CSI2 ECC Debug Register
1A040374	SENINF1_OCSI2_CRCDBG	32	CSI2 CRC Debug Register
1A040378	SENINF1_OCSI2_DBG	32	CSI2 Debug Register
1A04037C	SENINF1_OCSI2_VER	32	CSI2 Version Code Register
1A040380	SENINF1_OCSI2_	32	CSI2 Short Packet Information Register

Address	Name	Width	Register Function
	SHORT_INFO		
1A040384	SENINF1_OCSI2_LNFSM	32	CSI2 Lane FSM Register
1A040388	SENINF1_OCSI2_LNMUX	32	CSI2 Lane Mux Register
1A04038C	SENINF1_OCSI2_HSYNC_CNT	32	CSI2 Hsync Counter Register
1A040390	SENINF1_OCSI2_CAL	32	CSI2 Calibration Register
1A040394	SENINF1_OCSI2_DS	32	CSI2 Downsample Register
1A040398	SENINF1_OCSI2_VS	32	CSI2 Vsync Register
1A04039C	SENINF1_OCSI2_BIST	32	CSI2 BIST Register

1A040360 SENINF1_OCSI2_CTRL CSI2 Control Register 00002D80

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_BIST_CSI2_DATA_OK	CSI2_LANE_FSM_OK	CSI2_HS_FSM_OK	CSI2_BIST_DATA_OK	CSI2_BIST_START	CSI2_BIST_ERROR_COUNT								CSI2_DATA_FLOW		CSI2_ASYNC_OPTION
Type	RO	RO	RO	RO	RO	RO								RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_SYNC_CLR_EXTEND	CSI2_HSRXEN_PFOOT_CLR	CSI2_VSYNC_TYPE	CSI2_SW_RST	CSI2_SCLK4X_SEL	CSI2_SCLK_SEL	CSI2_ESC_EN	CSI2_SYNC_RST_EN	CSI2_LP11_RST_EN	CSI2_CLK_MISS_EN	CSI2_ED_SEL	CSI2_ECC_EN	DLANE3_EN	DLANE2_EN	DLANE1_EN	CSI2_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	1	0	1	1	0	1	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	CSI2_BIST_CSI2_DATA_OK	**CSI2 BIST CSI2 data ok**
30	CSI2_LANE_FSM_OK	**CSI2 BIST data lane FSM ok**
29	CSI2_HS_FSM_OK	**CSI2 BIST high speed FSM ok**
28	CSI2_BIST_DATA_OK	**CSI2 BIST DPHY data ok**
27	CSI2_BIST_START	**CSI2 BIST start status**
26:19	CSI2_BIST_ERROR_COUNT	**CSI2 bist test error count**
18:17	CSI2_DATA_FLOW	**CSI2 data flow** 0: Data packet 1: Generic long packet 2: All data packet
16	CSI2_ASYNC_OPTION	
15	CSI2_SYNC_CLR_EXTEND	
14	CSI2_HSRXEN_PFOOT_CLR	
13	CSI2_VSYNC_TYPE	**VSYNC type to CAM module** 0: High from short packet "frame start" to short packet "frame end" 1: 4T pulse after short packet "frame start"

Bit(s)	Name	Description
12	CSI2_SW_RST	**CSI2 software reset, active high** 0: De-assert reset 1: Assert reset
11	CSI2_SCLK4X_SEL	**Selects CSI2 4x sample clock** 0: Invert 1: Does not invert csi2_clk from D-PHY
10	CSI2_SCLK_SEL	**Selects CSI2 sample clock** 0: Invert 1: Does not invert csi2_clk from D-PHY
9	CSI2_ESC_EN	**Enables CSI2 escape mode**
8	CSI2_SYNC_RST_EN	**When this bit is set high, data high speed FSM will enter state "SYNC" whenever sync code is seen.** Used in case packet ends unexpectedly.
7	CSI2_LP11_RST_EN	**When this bit is set high, data/clk lane FSM will enter state "STOP" whenever LP-11 is seen.** Used in case low power and high speed state transition is unexpected.
6	CSI2_CLK_MISS_EN	**Enables high speed mode clock miss monitoring**
5	CSI2_ED_SEL	**Selects CSI2 header format**
4	CSI2_ECC_EN	**Enables CSI2 ECC**
3	DLANE3_EN	**Enables CSI2 3 data lane**
2	DLANE2_EN	**Enables CSI2 2 data lane**
1	DLANE1_EN	**Enables CSI2 1 data lane**
0	CSI2_EN	**Enable sCSI2 0 data lane**

1A040364 SENINF1_CSI2_DELAY **CSI2 Delay Control Register** **000A0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LP2HS_DATA_TERM_DELAY								LP2HS_DATA_SETTLE_DELAY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LP2HS_CLK_TERM_DELAY							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	LP2HS_DATA_TERM_DELAY	CSI2 data lane low power to high speed termination enable delay count.
23:16	LP2HS_DATA_SETTLE_DELAY	CSI2 data lane low power to high speed sync code search delay.
7:0	LP2HS_CLK_TERM_DELAY	CSI2 CLK lane low power to high speed termination enable delay count

1A040368 SENINF1_CSI2_INTEN **CSI2 Interrupt Enable Register** **00000007**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VCHANNEL_ID		CSI2_DATA_TYPE						CSI2_WC_NUMBER							
Type	RO		RO						RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	CSI2_WC_NUMBER												CSI2SYNC_NONSYNC_IRQ_EN	ECC_CORRECT_IRQ_EN	ECC_ERR_IRQ_EN	CRC_ERR_IRQ_EN
Type	RO												RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0					0	1	1	1

Bit(s)	Name	Description
31:30	VCHANNEL_ID	CSI2 virtual channel identifier corrected by error correction if ECC is on
29:24	CSI2_DATA_TYPE	CSI2 long packet data type corrected by error correction if ECC is on
23:8	CSI2_WC_NUMBER	CSI2 long packet data size corrected by error correction if ECC is on
3	CSI2SYNC_NONSYNC_IRQ_EN	CSI2SYNC_NONSYNC_IRQ
2	ECC_CORRECT_IRQ_EN	Enables ECC correction interrupt
1	ECC_ERR_IRQ_EN	Enables ECC error interrupt
0	CRC_ERR_IRQ_EN	Enables CRC error interrupt

1A04036C SENINF1_OCSI2_INTSTA CSI2 Interrupt Status Register 00000070

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CSI2OUT_VSYNC	CSI2OUT_HSYNC				
Type											RO	RO				
Reset											0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CSI2_SPARE			CSI2_IRQ_CLR_SEL	CSI2SYNC_NONSYNC_IRQ	ECC_CORRECT_IRQ	ECC_ERR_IRQ	CRC_ERR_IRQ
Type									RW			RW	RO	RO	RO	RO
Reset									0	1	1	1	0	0	0	0

Bit(s)	Name	Description
21	CSI2OUT_VSYNC	**CSI2 vsync output to cam** Read only.
20	CSI2OUT_HSYNC	**CSI2 hsync output to cam** Read only.
7:5	CSI2_SPARE	**Spare register**
4	CSI2_IRQ_CLR_SEL	0: Read clear 1: Write clear
3	CSI2SYNC_NONSYNC_IRQ	**IRQ status bit to indicate that sync between different lanes is not sampled at the same time** Write clear.
2	ECC_CORRECT_IRQ	**ECC correction interrupt status**
1	ECC_ERR_IRQ	**ECC error interrupt status**
0	CRC_ERR_IRQ	**CRC error interrupt status**

1A040370 SENINF1_OC CSI2 ECC Debug Register 00000000

SI2_ECCDBG

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_ECCDB_BSEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_ECCDB_BSEL															CSI2_ECCDB_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CSI2_ECCDB_BSEL	**Selects CSI2 packet header error generation bit** To generate packet header error, set one of the 24 bits to 1. Because there is only one bit error that can be corrected, only one bit of the 24 bits can be 1.
0	CSI2_ECCDB_EN	**Enables CSI2 packet header error generation**

1A040374 SENINF1_OCSI2_CRCDBG CSI2 CRC Debug Register 0000000E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_CRCDB_BSEL								CSI2_CRCDB_WSEL							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_CRCDB_WSEL								CSI2_SPARE							CSI2_CRCDB_EN
Type	RW								RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Bit(s)	Name	Description
31:24	CSI2_CRCDB_BSEL	**Selects CSI2 data error generation bit** Set to 1 to generate selected word bit error. Note: Only word number selected by csi2_crcdb_wsel will be put error on it.
23:8	CSI2_CRCDB_WSEL	**Selects CSI2 data error generation data word**
7:1	CSI2_SPARE	**Spare register**
0	CSI2_CRCDB_EN	**Enables CSI2 data error generation**

1A040378 SENINF1_OCSI2_DBG CSI2 Debug Register 00040820

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LN3_HSRXDB_EN	LN2_HSRXDB_EN	LN1_HSRXDB_EN	LN0_HSRXDB_EN	LNC_HSRXDB_EN	LN3_LPRXDB_EN	LN2_LPRXDB_EN	LN1_LPRXDB_EN	LN0_LPRXDB_EN	LNC_LPRXDB_EN		VCHANNEL_ID_EN	VCHANNEL1_ID		VCHANNEL0_ID	
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0		0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	CSI2_CLK_LANE_CS					CSI2_DATA_HS_CS						CSI2_DBG_SRC_SEL				CSI2_DEBUG_ON
Type	RO					RO						RW				RW
Reset	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31	LN3_HSRXDB_EN	**Enables data lane 1 termination directly** For test only.
30	LN2_HSRXDB_EN	**Enables data lane 0 termination directly** For test only.
29	LN1_HSRXDB_EN	**Enables data lane 1 termination directly** For test only.
28	LN0_HSRXDB_EN	**Enables data lane 0 termination directly** For test only.
27	LNC_HSRXDB_EN	**Enables clock lane termination directly** For test only.
26	LN3_LPRXDB_EN	**Enables data lane 3 low power mode directly** For test only.
25	LN2_LPRXDB_EN	**Enables data lane 2 low power mode directly** For test only.
24	LN1_LPRXDB_EN	**Enables data lane 1 low power mode directly** For test only.
23	LN0_LPRXDB_EN	**Enables data lane 0 low power mode directly** For test only.
22	LNC_LPRXDB_EN	**Enables clock lane low power mode directly** For test only.
20	VCHANNEL_ID_EN	**Enables virtual channel**
19:18	VCHANNEL1_ID	**Virtual channel 1 ID**
17:16	VCHANNEL0_ID	**Virtual channel 0 ID**
15:11	CSI2_CLK_LANE_CS	**Clock lane FSM current state** 1: IDLE 2: STOP 4: HS_REQ 8: HS_PREP 16: HS_RX
10:5	CSI2_DATA_HS_CS	**Data high speed state** 1: IDLE 2: SYNC 4: PHEAD 8: PECC 16: PDATA 32: PFOOT
4:1	CSI2_DBG_SRC_SEL	**Selects CSI2 debug port source**
0	CSI2_DEBUG_ON	**Enables CSI2 debug** When CSI2 debug is enabled, CSI2 output raw data will include header to cam. *Note: To output CSI2 debug data,* *1. Set cam to JPEG interface mode ((CAM + 0024)[14], JPGINF_EN:1).* *2. Set up Vsync polarity ((CAM + 0010)[7], VSPOL:1).* *3. Set up output type raw data output ((CAM + 0024)[21:20] OUTPATH_TYPE:0).* *4. Set up raw data type to 8-bit mode ((CAM + 0024)[24] OUTPATH_TYPE:0).* *5. Enable ISP data output to memory ((CAM + 0024)[16],OUT_PATH_EN:1).*

1A04037C SENINF1_OCSI2_VER CSI2 Version Code Register 20110815

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	YEAR															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MONTH								DATE							
Type	RO								RO							
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	1

Bit(s)	Name	Description
31:16	YEAR	Year code
15:8	MONTH	Month code
7:0	DATE	Date code

1A040380 SENINF1_OCSI2_SHORT_INFO CSI2 Short Packet Information Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_FRAME_NO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_LINE_NO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	CSI2_FRAME_NO	Frame number information in short packet data type
15:0	CSI2_LINE_NO	Line number information in short packet data type

1A040384 SENINF1_OCSI2_LNFSM CSI2 Lane FSM Register 01010101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CSI2_DATA_LN3_CS								CSI2_DATA_LN2_CS						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CSI2_DATA_LN1_CS								CSI2_DATA_LN0_CS						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1

Bit(s)	Name	Description
30:24	CSI2_DATA_LN3_CS	**Data lane 3 FSM current state**
22:16	CSI2_DATA_LN2_CS	**Data lane 2 FSM current state**
14:8	CSI2_DATA_LN1_CS	**Data lane 1 FSM current state**
6:0	CSI2_DATA_LN0_CS	**Data lane 0 FSM current state**

Bit(s)	Name	Description
		1: IDLE 2: STOP 4: HS_REQ 8: HS_PREP 16: HS_TERM 32: HS_RX 64: HS_ESC

1A040388 SENINF1_OCSI2_LNMUX CSI2 Lane Mux Register 000000E4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CSI2_DATA_LN3_MUX		CSI2_DATA_LN2_MUX		CSI2_DATA_LN1_MUX		CSI2_DATA_LN0_MUX	
Type									RW		RW		RW		RW	
Reset									1	1	1	0	0	1	0	0

Bit(s)	Name	Description
7:6	CSI2_DATA_LN3_MUX	**CSI2 data lane mux** 0: LANE 0 1: LANE 1 2: LANE 2 3: LANE 3
5:4	CSI2_DATA_LN2_MUX	**CSI2 data lane mux** 0: LANE 0 1: LANE 1 2: LANE 2 3: LANE 3
3:2	CSI2_DATA_LN1_MUX	**CSI2 data lane mux** 0: LANE 0 1: LANE 1 2: LANE 2 3: LANE 3
1:0	CSI2_DATA_LN0_MUX	**CSI2 data lane mux** 0: LANE 0 1: LANE 1 2: LANE 2 3: LANE 3

1A04038C SENINF1_OCSI2_HSYNC_CNT CSI2 Hsync Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CSI2_HSYNC_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	CSI2_HSYNC_CNT	CSI2 hsync counter

1A040390 SENINF1_OCSI2_CAL CSI2 Calibration Register 01010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2 _CAL _CNT _2								CSI2_CAL_CNT_1							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										CSI2_CAL_STAT E						CSI2 _CAL _EN
Type										RO						RW
Reset										0	0	0				0

Bit(s)	Name	Description
31:24	CSI2_CAL_CNT_2	**CSI2 calibration counter 2 (term enable to sync)** Settle delay <= CSI2 Calibration Counter 2 - Term Delay - 3 byte clk - 3 bclk - 1 bclk
23:16	CSI2_CAL_CNT_1	**CSI2 calibration counter 1 (term enable to HS00)** Term delay <= CSI2 Calibration Counter 1 - 2 byte clk - 3 bclk
6:4	CSI2_CAL_STATE	**CSI2 calibration current state**
0	CSI2_CAL_EN	**Enables CSI2 calibration**

1A040394 SENINF1_OCSI2_DS CSI2 Downsample Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CSI2_DS_C TRL		CSI2 _DS_ EN
Type														RW		RW
Reset														0	0	0

Bit(s)	Name	Description
2:1	CSI2_DS_CTRL	**Controls CSI2 downsample factor** 0: 1 1: 1/2 2: 1/4 3: 1/8
0	CSI2_DS_EN	**Enables CSI2 downsample**

Bit(s)	Name	Description

1A040398 SENINF1_OCSI2_VS CSI2 Vsync Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CSI2_VS_CTRL	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	CSI2_VS_CTRL	**Extends CSI2 vsync period** 0: 4T 1: 8T 2: 12T 3: 16T

1A04039C SENINF1_OCSI2_BIST CSI2 BIST Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CSI2_BIST_LNR3_DATA_OK	CSI2_BIST_LNR2_DATA_OK	CSI2_BIST_LNR1_DATA_OK	CSI2_BIST_LNR0_DATA_OK
Type													RO	RO	RO	RO
Reset													0	0	0	0

Bit(s)	Name	Description
3	CSI2_BIST_LNR3_DATA_OK	CSI2 BIST Lane 3 DPHY data ok
2	CSI2_BIST_LNR2_DATA_OK	CSI2 BIST Lane 2 DPHY data ok
1	CSI2_BIST_LNR1_DATA_OK	CSI2 BIST Lane 1 DPHY data ok
0	CSI2_BIST_LNR0_DATA_OK	CSI2 BIST Lane 0 DPHY data ok

Module name: SENINF1_TG Base address: (+1a040600h)

Address	Name	Width	Register Function
1A040600	SENINF_TG1_PH_CNT	32	TG Phase Counter
1A040604	SENINF_TG1_SEN_CK	32	TG Sensor Clock Divider

Address	Name	Width	Register Function
1A040608	SENINF_TG1_TM_CTL	32	TM Control
1A04060C	SENINF_TG1_TM_SIZE	32	TM Size
1A040610	SENINF_TG1_TM_CLK	32	TM Clock
1A040614	SENINF_TG1_TM_STP	32	TG1_TM_STP

1A040600 SENINF_TG1_PH_CNT **TG Phase Counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PCEN		ADCLK_EN	CLKPOL												
Type	RW		RW	RW												
Reset	0		0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CAM_PCLK_INV	PAD_PCLK_INV	EXT_PWRDN	EXT_RST		CLKFL_POL	TGCLK_SEL	
Type									RW	RW	RW	RW		RW	RW	
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
31	PCEN	**TG phase counter enable control**
29	ADCLK_EN	**Enables sensor master clock (mclk) output to sensor**
28	CLKPOL	**Controls sensor master clock polarity**
7	CAM_PCLK_INV	**Inverts pixel clock in CAM**
6	PAD_PCLK_INV	**Inverts pixel clock in PAD side**
5	EXT_PWRDN	**Powers down sensor**
4	EXT_RST	**Resets sensor**
2	CLKFL_POL	**Sensor clock falling edge polarity**
1:0	TGCLK_SEL	**Selects sensor master clock** 0: isp_clk 1: cam_pll 2: 3rd clock source

1A040604 SENINF_TG1_SEN_CK **TG Sensor Clock Divider** **00010001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CLKCNT					
Type											RW					
Reset											0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			CLKRS								CLKFL					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	1

Bit(s)	Name	Description

Bit(s)	Name	Description
21:16	CLKCNT	**Controls sensor master clock frequency divider** Sensor master clock = ISP_clock/(CLKCNT+1); CLKCNT >=1
13:8	CLKRS	**Controls sensor master clock rising edge**
5:0	CLKFL	**Controls sensor master clock falling edge**

1A040608 SENINF_TG1_TM_CTL **TM Control** **00300004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									TM_DUMMYPXL							
Type									RW							
Reset									0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TM_VSYNC								TM_PAT					TM_FMT	TM_RST	TM_EN
Type	RW								RW					RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0		1	0	0

Bit(s)	Name	Description
23:16	TM_DUMMYPXL	**Test model horizontal dummy pixel**
15:8	TM_VSYNC	**VSYNC high duration in line unit (TM_DUMMYPXL + PIXEL)**
7:4	TM_PAT	**Test model decision** 0: White 1: Yellow 2: Cyan 3: Green 4: Magenta 5: Red 6: Blue 7: Black 8: Horizontal gray level (Unit 1) 9: Horizontal gray level (Unit 4) 10: Horizontal gray level (take 1024 pixel as one period) (only bayer) 11: Vertical gray level (Unit 1) 12: Static horizontal color bar 13: Static vertical color bar (only bayer) 14: R,G,B,W flashes every two frames (only bayer) 15: Dynamic horizontal colorbar (only bayer)
2	TM_FMT	**Test model format** 0: Bayer 1: YUV
1	TM_RST	**Resets test model** 1'b0: Does not reset test model 1'b1: Reset test model
0	TM_EN	**Enables test model** 0: Disable 1: Enable

1A04060C SENINF_TG1_TM_SIZE **TM Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			TM_LINE													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TM_PXL												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	TM_LINE	Test model line number
12:0	TM_PXL	Test model pixel number (HSYNC high duration in pixel unit)

1A040610 SENINF_TG1_TM_CLK TM Clock 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		TM_CLRBAR_IDX					TM_CLRBAR_OFT									
Type		RW					RW									
Reset		0	0	0			0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TM_CLK_CNT			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
30:28	TM_CLRBAR_IDX	**Test model colorbar index offset** 0: White 1: Yellow 2: Cyan 3: Green 4: Magenta 5: Red 6: Blue 7: Black
25:16	TM_CLRBAR_OFT	**Test model colorbar offset** This value should be smaller than (TM_PXL>>3).
3:0	TM_CLK_CNT	**Test model clock divided count**

1A040614 SENINF_TG1_TM_STP TG1_TM_STP 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TG1_TM_STP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TG1_TM_STP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TG1_TM_STP	Time stamp divider

Module name: seninf2 Base address: (+1a041200h)

Address	Name	Width	Register Function
1A041200	**SENINF2_CTRL**	32	SENINF 2 Control Register
1A041204	**SENINF2_CTRL_EXT**	32	SENINF 2 Control Register Extend
1A041208	**SENINF2_ASYNC_CTRL**	32	SENINF 2 Async Control Register

1A041200 SENINF2_CTRL SENINF 2 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PAD2CAM_DATA_SEL							SENINF_DEBUG_SEL							
Type		RW							RW							
Reset		0	0	0					0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_SRC_SEL							CSI3_SW_RST	CSI2_SW_RST	SCAM_SW_RST	TEST_MODEL_SW_RST	CKGEN_SW_RST	CCIR_SW_RST	OCSI2_SW_RST	NCSI2_SW_RST	SENINF_EN
Type	RW							RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:28	PAD2CAM_DATA_SEL	0: PAD2CAM_DATA[9:0] 3: {PAD2CAM_DATA[7:0],2'b00} 4: {PAD2CAM_DATA[9:2]2'b00}
23:20	SENINF_DEBUG_SEL	**Selects SENINF1 debug**
15:12	SENINF_SRC_SEL	**Selects SENINF input source** 0: CSI2 1: Test model 2: CCIR656 3: Parallel sensor 4: Serial sensor 8: NCSI2
8	CSI3_SW_RST	**CSI3 software reset, active high** 0: De-assert reset 1: Assert reset
7	CSI2_SW_RST	**CSI2 software reset, active high** 0: De-assert reset 1: Assert reset
6	SCAM_SW_RST	**SCAM software reset, active high** 0: De-assert reset 1: Assert reset
5	TEST_MODEL_SW_RST	**Test model software reset, active high** 0: De-assert reset 1: Assert reset
4	CKGEN_SW_RST	**CKGEN software reset, active high**

Bit(s)	Name	Description
		0: De-assert reset 1: Assert reset
3	CCIR_SW_RST	**CCIR software reset, active high** 0: De-assert reset 1: Assert reset
2	OCSI2_SW_RST	**OCSI2 software reset, active high** 0: De-assert reset 1: Assert reset
1	NCSI2_SW_RST	**NCSI2 software reset, active high** 0: De-assert reset 1: Assert reset
0	SENINF_EN	

1A041204 SENINF2_CTRL_EXT — **SENINF 2 Control Register Extend** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															SENINF_SRC_SEL_EXT	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SENINF_CSI3_IP_EN	SENINF_CSI2_IP_EN	SENINF_NCSI2_IP_EN	SENINF_SCAM_IP_EN			SENINF_TESTMDL_IP_EN	SENINF_OCSI2_IP_EN
Type									RW	RW	RW	RW			RW	RW
Reset									0	0	0	0			0	0

Bit(s)	Name	Description
17:16	SENINF_SRC_SEL_EXT	[0] Set 1'b1 for CSI2 [1] Set 1'b1 for CSI3 For constraints only.
7	SENINF_CSI3_IP_EN	Enables CSI3 IP
6	SENINF_CSI2_IP_EN	Enables CSI2 IP
5	SENINF_NCSI2_IP_EN	Enables NCSI2 IP
4	SENINF_SCAM_IP_EN	Enables SCAM IP
1	SENINF_TESTMDL_IP_EN	Enables TESTMDL IP
0	SENINF_OCSI2_IP_EN	Enables OCSI2 IP

1A041208 SENINF2_ASYNC_CTRL — **SENINF 2 Async Control Register** — **1B1F0002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			FIFO_FLUSH_EN								FIFO_PUSH_EN					
Type			RW								RW					
Reset			0	1	1	0	1	1			0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SENINF_HSYNC_POL	SENINF_VSYNC_POL	SENINF_HSYNC_MASK	SENINF_ASYNC_FIFO_RS

																T
Type													RW	RW	RW	RW
Reset													0	0	1	0

Bit(s)	Name	Description
29:24	FIFO_FLUSH_EN	**Normal mode: 6'b011011** JPEG two pixel mode: 6'b011000
21:16	FIFO_PUSH_EN	**Normal mode: 6'b011111** JPEG two pixel mode: 6'b011110
3	SENINF_HSYNC_POL	**SENINF HSYNC polarity**
2	SENINF_VSYNC_POL	**SENINF VSYNC polarity**
1	SENINF_HSYNC_MASK	**Masks hsync** 0: Send hsync when vsync = 1 1: Does not send hsync when vsync = 1
0	SENINF_ASYNC_FIFO_RST	**Async FIFO software reset**

Module name: seninf2_csi2 Base address: (+1a041a00h)

Address	Name	Width	Register Function
1A041A00	SENINF2_CSI2_CTL	32	CSI2 Function Enable
1A041A04	SENINF2_CSI2_LNRC_TIMING	32	CSI2 Clock Lane Timing Parameters
1A041A08	SENINF2_CSI2_LNRD_TIMING	32	CSI2 Data Lane Timing Parameters
1A041A0C	SENINF2_CSI2_DPCM	32	CSI2 DPCM Parameters
1A041A10	SENINF2_CSI2_INT_EN	32	CSI2 Interrupt Enable
1A041A14	SENINF2_CSI2_INT_STATUS	32	CSI2 Interrupt Status
1A041A18	SENINF2_CSI2_DGB_SEL	32	CSI2 Debug Selection
1A041A1C	SENINF2_CSI2_DBG_PORT	32	CSI2 Debug Port
1A041A20	SENINF2_CSI2_SPARE0	32	SPARE0
1A041A24	SENINF2_CSI2_SPARE1	32	SPARE1
1A041A28	SENINF2_CSI2_LNRC_FSM	32	CSI2 Clock Lane RX FSM
1A041A2C	SENINF2_CSI2_LNRD_FSM	32	CSI2 Data Lane RX FSM
1A041A30	SENINF2_CSI2_FRAME_LINE_NUM	32	CSI2 Frame/Line Number
1A041A34	SENINF2_CSI2_GENERIC_SHORT	32	CSI2 Generic Short Packet
1A041A38	SENINF2_CSI2_HSRX_DBG	32	CSI2 HSRX Enable
1A041A3C	SENINF2_CSI2_DI	32	CSI2 Data Interleaving Parameters
1A041A40	SENINF2_CSI2_HS_TRAIL	32	CSI2 HS Trail Timing Parameters
1A041A44	SENINF2_CSI2_DI_CTRL	32	CSI2 Data Interleaving Control
1A041A48	SENINF2_CSI2_L	32	CSI2 Data Lane RX FSM Other

Address	Name	Width	Register Function
	NRD_FSM_X		
1A041A4C	SENINF2_CSI2_DETECT_CON1	32	CSI2 CPHY Detect Control sync
1A041A50	SENINF2_CSI2_DETECT_CON2	32	CSI2 CPHY Detect Control Escape
1A041A54	SENINF2_CSI2_DETECT_CON3	32	CSI2 CPHY Detect Control Post
1A041A58	SENINF2_CSI2_RLR0_CON0	32	CSI2 CPHY RLR0 CON0
1A041A5C	SENINF2_CSI2_RLR1_CON0	32	CSI2 CPHY RLR1 CON0
1A041A60	SENINF2_CSI2_RLR2_CON0	32	CSI2 CPHY RLR2 CON0
1A041A64	SENINF2_CSI2_RLR_CON0	32	CSI2 CPHY RLR CON0
1A041A68	SENINF2_CSI2_MUX_CON	32	CSI2 Pin Pux Sel
1A041A6C	SENINF2_CSI2_DETECT_DBG0	32	CSI2 Detection Debug 0
1A041A70	SENINF2_CSI2_DETECT_DBG1	32	CSI2 Detection Debug 1
1A041A74	SENINF2_CSI2_RESYNC_MERGE_CTL	32	CSI2 Lane Resync Merge Control
1A041A78	SENINF2_CSI2_CTRL_TRIO_MUX	32	CSI2 Control Trio Mux
1A041A7C	SENINF2_CSI2_CTRL_TRIO_CON	32	CSI2 Control Trio Config
1A041A80	SENINF2_FIX_ADDR_CPHY0_DBG	32	cphy_fix_point_addr_cphy0_debug
1A041A84	SENINF2_FIX_ADDR_CPHY1_DBG	32	cphy_fix_point_addr_cphy1_debug
1A041A88	SENINF2_FIX_ADDR_CPHY2_DBG	32	cphy_fix_point_addr_cphy2_debug
1A041A8C	SENINF2_FIX_ADDR_DBG	32	cphy_fix_point_addr_debug
1A041A90	SENINF2_WIRE_STATE_DECODE_CPHY0_DBG0	32	cphy_wire_state_decode_cphy0_debug0
1A041A94	SENINF2_WIRE_STATE_DECODE_CPHY0_DBG1	32	cphy_wire_state_decode_cphy0_debug1
1A041A98	SENINF2_WIRE_STATE_DECODE_CPHY1_DBG0	32	cphy_wire_state_decode_cphy1_debug0
1A041A9C	SENINF2_WIRE_STATE_DECODE_CPHY1_DBG1	32	cphy_wire_state_decode_cphy1_debug1
1A041AA0	SENINF2_WIRE_STATE_DECODE_CPHY2_DBG0	32	cphy_wire_state_decode_cphy2_debug0
1A041AA4	SENINF2_WIRE_STATE_DECODE_CPHY2_DBG1	32	cphy_wire_state_decode_cphy2_debug1
1A041AA8	SENINF2_SYNC_R	32	CSI2 Sync Resync Control

Address	Name	Width	Register Function
	ESYNC_CTL		
1A041AAC	SENINF2_POST_DETECT_CTL	32	CSI2 Post Detect Control
1A041AB0	SENINF2_WIRE_STATE_DECODE_CONFIG	32	CSI2 Wire State Decode Config
1A041AB4	SENINF2_CSI2_CPHY_LNRD_FSM	32	CPHY Data Lane RX FSM
1A041AB8	SENINF2_FIX_ADDR_CPHY0_DBG0	32	cphy_fix_point_addr_cphy0_debug0
1A041ABC	SENINF2_FIX_ADDR_CPHY0_DBG1	32	cphy_fix_point_addr_cphy0_debug1
1A041AC0	SENINF2_FIX_ADDR_CPHY0_DBG2	32	cphy_fix_point_addr_cphy0_debug2
1A041AC4	SENINF2_FIX_ADDR_CPHY1_DBG0	32	cphy_fix_point_addr_cphy1_debug0
1A041AC8	SENINF2_FIX_ADDR_CPHY1_DBG1	32	cphy_fix_point_addr_cphy1_debug1
1A041ACC	SENINF2_FIX_ADDR_CPHY1_DBG2	32	cphy_fix_point_addr_cphy1_debug2
1A041AD0	SENINF2_FIX_ADDR_CPHY2_DBG0	32	cphy_fix_point_addr_cphy2_debug0
1A041AD4	SENINF2_FIX_ADDR_CPHY2_DBG1	32	cphy_fix_point_addr_cphy2_debug1
1A041AD8	SENINF2_FIX_ADDR_CPHY2_DBG2	32	cphy_fix_point_addr_cphy2_debug2
1A041ADC	SENINF2_FIX_ADDR_DBG0	32	cphy_fix_point_addr_debug0
1A041AE0	SENINF2_FIX_ADDR_DBG1	32	cphy_fix_point_addr_debug1
1A041AE4	SENINF2_FIX_ADDR_DBG2	32	cphy_fix_point_addr_debug2
1A041AE8	SENINF2_CSI2_MODE	32	CSI2 Packet Structure
1A041AF0	SENINF2_CSI2_DI_EXT	32	CSI2 Data Interleaving Parameters Extend
1A041AF4	SENINF2_CSI2_DI_CTRL_EXT	32	CSI2 Data Interleaving Control Extend
1A041AF8	SENINF2_CSI2_CPHY_LOOPBACK	32	CSI2 SW Trigger sync_init and hs_en
1A041B00	SENINF2_CSI2_PROGSEQ_0	32	CSI2 CPHY Program sequence_0
1A041B04	SENINF2_CSI2_PROGSEQ_1	32	CSI2 CPHY Program sequence_1
1A041B10	SENINF2_CSI2_INT_EN_EXT	32	CSI2 Interrupt Enable Extend
1A041B14	SENINF2_CSI2_INT_STATUS_EXT	32	CSI2 Interrupt Status Extend
1A041B18	SENINF2_CSI2_CPHY_FIX_POINT_RST	32	CSI2 CPHY fix point reset mode
1A041B20	SENINF2_CSI2_DPHY_RESYNC_CTL	32	CSI2 DPHY Lane Resync Control

1A041A00 SENINF2_CSI2_CTL **CSI2 Function Enable** **01886160**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA_LANE7_EN	DATA_LANE6_EN	VS_OUT_CYCLE_NUMBER		CLOCK_HS_OPTION	REF_SYNC_DET_EN	HS_TRAIL_EN	ASYNC_FIFO_RST_SCH		SYNC_DET_BITSWAP_EN	SYNC_DET_EN	SYNC_DET_SCHEME	FLUSH_MODE			ED_SEL
Type	RW	RW	RW		RW	RW	RW	RW		RW	RW	RW	RW			RW
Reset	0	0	0	0	0	0	0	1	1	0	0	0	1	0		0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VS_TYPE	BYTE2PIXEL_EN	IMAGE_PACKET_EN	GENERIC_LONG_PACKET_EN	DATA_LANE5_EN	DATA_LANE4_EN	HS_END_EN	HS_PRPR_EN	HSRX_DET_EN	CRC_EN	ECC_EN	CLOCK_LANE_EN	DATA_LANE3_EN	DATA_LANE2_EN	DATA_LANE1_EN	DATA_LANE0_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	1	1	0	0	0	0	1	0	1	1	0	0	0	0	0

Bit(s)	Name	Description
31	DATA_LANE7_EN	**Enables data lane 7**
30	DATA_LANE6_EN	**Enables data lane 6**
29:28	VS_OUT_CYCLE_NUMBER	0: 4T 1: 8T
27	CLOCK_HS_OPTION	0: Enable clock lane HS based on LP11, LP01, LP00 1: Enable clock lane HS based on LP00
26	REF_SYNC_DET_EN	**Reference sync detect signal to do analog sync**
25	HS_TRAIL_EN	**Extends HS trail**
24:23	ASYNC_FIFO_RST_SCH	
22	SYNC_DET_BITSWAP_EN	
21	SYNC_DET_EN	**Enables sync sequence detection**
20	SYNC_DET_SCHEME	0: B8 1: 101110
19:18	FLUSH_MODE	0: Disable 1: Flush at first cycle of LP11 2: Flush at LP11 3: Reserved
16	ED_SEL	0: {WCH,WCL,DI} 1: {DI,WCL,WCH}
15	VS_TYPE	**VS type** 0: 4T 1: Frame start to frame end
14	BYTE2PIXEL_EN	**Byte 2 pixel conversion**
13	IMAGE_PACKET_EN	**Image data types**
12	GENERIC_LONG_PACKET_EN	**Generic long packet data types**
11	DATA_LANE5_EN	**Enables data lane 6**
10	DATA_LANE4_EN	**Enables data lane 5**
9	HS_END_EN	**Enables HS_EX reset at packet end**
8	HS_PRPR_EN	**Enables RX_HS_PRPR state**
7	HSRX_DET_EN	**Enables HSRX termination auto-detection flow**
6	CRC_EN	**Enables checksum**
5	ECC_EN	**Enables packet header ECC**
4	CLOCK_LANE_EN	**Enables clock lane**
3	DATA_LANE3_EN	**Enables data lane 3**
2	DATA_LANE2_EN	**Enables data lane 2**
1	DATA_LANE1_EN	**Enables data lane 1**
0	DATA_LANE0_EN	**Enables data lane 0**

Bit(s)	Name	Description

1A041A04 SENINF2_CSI2_LNRC_TIMING **CSI2 Clock Lane Timing Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLOCK_SETTLE_PARAMETER								CLOCK_TERM_PARAMETER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	CLOCK_SETTLE_PARAMETER	TD_SETTLE parameter
7:0	CLOCK_TERM_PARAMETER	TD_TERM_EN parameter

1A041A08 SENINF2_CSI2_LNRD_TIMING **CSI2 Data Lane Timing Parameters** **00002000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_SETTLE_PARAMETER								DATA_TERM_PARAMETER							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	DATA_SETTLE_PARAMETER	TD_SETTLE parameter
7:0	DATA_TERM_PARAMETER	TD_TERM_EN parameter

1A041A0C SENINF2_CSI2_DPCM **CSI2 DPCM Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DI_2A_DPCM_EN	DI_37_DPCM_EN	DI_36_DPCM_EN	DI_35_DPCM_EN	DI_34_DPCM_EN	DI_33_DPCM_EN	DI_32_DPCM_EN	DI_31_DPCM_EN	DI_30_DPCM_EN				DPCM_MODE			
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW				RW			
Reset	0	0	0	0	0	0	0	0	0				0	0	0	0

Bit(s)	Name	Description
15	DI_2A_DPCM_EN	**Enables DPCM**
14	DI_37_DPCM_EN	**Enables DPCM**
13	DI_36_DPCM_EN	**Enables DPCM**
12	DI_35_DPCM_EN	**Enables DPCM**
11	DI_34_DPCM_EN	**Enables DPCM**
10	DI_33_DPCM_EN	**Enables DPCM**
9	DI_32_DPCM_EN	**Enables DPCM**
8	DI_31_DPCM_EN	**Enables DPCM**
7	DI_30_DPCM_EN	**Enables DPCM**
3:0	DPCM_MODE	0: 10-8-10

1A041A10 SENINF2_CSI2_INT_EN **CSI2 Interrupt Enable** **1FFFBFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_WCLR_EN			TRIO2_ESCAPE_CODE_DETECT	TRIO1_ESCAPE_CODE_DETECT	TRIO0_ESCAPE_CODE_DETECT	TRIO2_RESYNC_FIFO_OVERFLOW	TRIO1_RESYNC_FIFO_OVERFLOW	TRIO0_RESYNC_FIFO_OVERFLOW	ERR_LANE_RESYNC	ERR_FRAME_SYNC_S5	ERR_FRAME_SYNC_S4	ERR_FRAME_SYNC_S3	ERR_FRAME_SYNC_S2	ERR_FRAME_SYNC_S1	ERR_FRAME_SYNC_S0
Type	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0			1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FE	GS	LS	FS	ERR_SOT_SYNC_HS_LNRD3	ERR_SOT_SYNC_HS_LNRD2	ERR_SOT_SYNC_HS_LNRD1	ERR_SOT_SYNC_HS_LNRD0	ERR_MULTI_LANE_SYNC	ERR_AFIFO	ERR_CRC	ERR_ECC_DOUBLE	ERR_ECC_CORRECTED	ERR_ECC_NO_ERROR	ERR_ID	ERR_FRAME_SYNC
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	INT_WCLR_EN	Enables interrupt write clear
28	TRIO2_ESCAPE_CODE_DETECT	Enables TRIO2_ESCAPE_CODE_DETECT interrupt
27	TRIO1_ESCAPE_CODE_DETECT	Enables TRIO1_ESCAPE_CODE_DETECT interrupt
26	TRIO0_ESCAPE_CODE_DETECT	Enables TRIO0_ESCAPE_CODE_DETECT interrupt
25	TRIO2_RESYNC_FIFO_OVERFLOW	Enables TRIO2_RESYNC_FIFO_OVERFLOW interrupt
24	TRIO1_RESYNC_FIFO_OVERFLOW	Enables TRIO1_RESYNC_FIFO_OVERFLOW interrupt
23	TRIO0_RESYNC_FIFO_OVERFLOW	Enables TRIO0_RESYNC_FIFO_OVERFLOW interrupt
22	ERR_LANE_RESYNC	Enables ERR_LANE_RESYNC interrupt
21	ERR_FRAME_SYNC_S5	Enables ERR_FRAME_SYNC interrupt
20	ERR_FRAME_SYNC_S4	Enables ERR_FRAME_SYNC interrupt
19	ERR_FRAME_SYNC_S3	Enables ERR_FRAME_SYNC interrupt
18	ERR_FRAME_SYNC_S2	Enables ERR_FRAME_SYNC interrupt
17	ERR_FRAME_SYNC_S1	Enables ERR_FRAME_SYNC interrupt
16	ERR_FRAME_SYNC_S0	Enables ERR_FRAME_SYNC interrupt
15	FE	Enables frame end interrupt
14	GS	Enables generic short packet interrupt
13	LS	Enables line start interrupt
12	FS	Enables frame start interrupt
11	ERR_SOT_SYNC_HS_LNRD3	Enables ERR_SOT_SYNC_HS interrupt
10	ERR_SOT_SYNC_HS_LNRD2	Enables ERR_SOT_SYNC_HS interrupt

Bit(s)	Name	Description
9	ERR_SOT_SYNC_HS_LNRD1	Enables ERR_SOT_SYNC_HS interrupt
8	ERR_SOT_SYNC_HS_LNRD0	Enables ERR_SOT_SYNC_HS interrupt
7	ERR_MULTI_LANE_SYNC	Enables ERR_MULTI_LANE_SYNC interrupt
6	ERR_AFIFO	Enables ERR_AFIFO interrupt
5	ERR_CRC	Enables ERR_CRC interrupt
4	ERR_ECC_DOUBLE	Enables ERR_ECC_DOUBLE interrupt
3	ERR_ECC_CORRECTED	Enables ERR_ECC_CORRECTED interrupt
2	ERR_ECC_NO_ERROR	ERR_ECC_NO_ERROR interrupt
1	ERR_ID	Enables ERR_ID interrupt
0	ERR_FRAME_SYNC	Enables ERR_FRAME_SYNC interrupt

1A041A14 SENINF2_CSI2_INT_STATUS **CSI2 Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				TRIO2_ESCAPE_CODE_DETECT_STA	TRIO1_ESCAPE_CODE_DETECT_STA	TRIO0_ESCAPE_CODE_DETECT_STA	TRIO2_RESYNC_FIFO_OVERFLOW_STA	TRIO1_RESYNC_FIFO_OVERFLOW_STA	TRIO0_RESYNC_FIFO_OVERFLOW_STA	ERR_LANE_RESYNC_STA	ERR_FRAME_SYNC_S5_STA	ERR_FRAME_SYNC_S4_STA	ERR_FRAME_SYNC_S3_STA	ERR_FRAME_SYNC_S2_STA	ERR_FRAME_SYNC_S1_STA	ERR_FRAME_SYNC_S0_STA
Type				RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FE_STA	GS_STA	LS_STA	FS_STA	ERR_SOT_SYNC_HS_LNRD3_STA	ERR_SOT_SYNC_HS_LNRD2_STA	ERR_SOT_SYNC_HS_LNRD1_STA	ERR_SOT_SYNC_HS_LNRD0_STA	ERR_MULTI_LANE_SYNC_STA	ERR_AFIFO_STA	ERR_CRC_STA	ERR_ECC_DOUBLE_STA	ERR_ECC_CORRECTED_STA	ERR_ECC_NO_ERROR_STA	ERR_ID_STA	ERR_FRAME_SYNC_STA
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	TRIO2_ESCAPE_CODE_DETECT_STA	**Asserted when the escape code of trio2 is detected**
27	TRIO1_ESCAPE_CODE_DETECT_STA	**Asserted when the escape code of trio1 is detected**
26	TRIO0_ESCAPE_CODE_DETECT_STA	**Asserted when the escape code of trio0 is detected**
25	TRIO2_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of CPHY trio2 is overflowed**
24	TRIO1_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of CPHY trio1 is overflowed**
23	TRIO0_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of CPHY trio0 is overflowed**
22	ERR_LANE_RESYNC_STA	**Asserted when CPHY lane sync detect time is longer than setting resync cycles**
21	ERR_FRAME_SYNC_S5_STA	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
20	ERR_FRAME_SYNC_S4_STA	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
19	ERR_FRAME_SYNC_S3_STA	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
18	ERR_FRAME_SYNC_S2_STA	**Asserted when a Frame End is not paired with a**

Bit(s)	Name	Description
		Frame Start on the same virtual channel
17	ERR_FRAME_SYNC_S1_STA	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
16	ERR_FRAME_SYNC_S0_STA	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
15	FE_STA	**Frame end interrupt**
14	GS_STA	**Enables generic short packet interrupt**
13	LS_STA	**Line start interrupt**
12	FS_STA	**Frame start interrupt**
11	ERR_SOT_SYNC_HS_LNRD3_STA	**Asserted when proper synchronization cannot be expected**
10	ERR_SOT_SYNC_HS_LNRD2_STA	**Asserted when proper synchronization cannot be expected**
9	ERR_SOT_SYNC_HS_LNRD1_STA	**Asserted when proper synchronization cannot be expected**
8	ERR_SOT_SYNC_HS_LNRD0_STA	**Asserted when proper synchronization cannot be expected**
7	ERR_MULTI_LANE_SYNC_STA	**Asserted when multiple lane synchronization fails**
6	ERR_AFIFO_STA	**Asserted when error occurs in asynchronous FIFO**
5	ERR_CRC_STA	**Asserted when computed CRC code is different from received CRC code**
4	ERR_ECC_DOUBLE_STA	**Asserted when an ECC syndrome is computed and two bit errors are detected in the received packet header**
3	ERR_ECC_CORRECTED_STA	**Asserted when an ECC syndrome is computed and a single bit error in the packet header is detected and corrected**
2	ERR_ECC_NO_ERROR_STA	**Asserted when an ECC syndrome is computed and the result is zero indicating a packet header that is considered to be without errors or has more than two bit errors** CSI-2's ECC mechanism cannot detect this type of error.
1	ERR_ID_STA	**Asserted whean a packet header is decoded with an unrecognized or unimplemented data ID**
0	ERR_FRAME_SYNC_STA	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**

1A041A18 SENINF2_CSI2_DGB_SEL CSI2 Debug Selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_EN															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DEBUG_SEL							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	DEBUG_EN	Enables debug
7:0	DEBUG_SEL	Selects debug

1A041A1C SENINF2_CSI2 CSI2 Debug Port 00000001

I2_DBG_PORT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CTL_DBG_PORT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	CTL_DBG_PORT	Debug port

1A041A20 SENINF2_CSI2_SPARE0 SPARE0 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	SPARE0	Spare register

1A041A24 SENINF2_CSI2_SPARE1 SPARE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE1	Spare register

1A041A28 SENINF2_CSI2_LNRC_FSM CSI2 Clock Lane RX FSM 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											LNRC_RX_FSM					
Type											RO					
Reset											0	0	0	0	0	1

Bit(s)	Name	Description
5:0	LNRC_RX_FSM	RX FSM of clock lane

1A041A2C SENINF2_CSI2_LNRD_FSM — CSI2 Data Lane RX FSM — 01010101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LNRD3_RX_FSM								LNRD2_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		LNRD1_RX_FSM								LNRD0_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1

Bit(s)	Name	Description
30:24	LNRD3_RX_FSM	RX FSM of data lane 3
22:16	LNRD2_RX_FSM	RX FSM of data lane 2
14:8	LNRD1_RX_FSM	RX FSM of data lane 1
6:0	LNRD0_RX_FSM	RX FSM of data lane 0

1A041A30 SENINF2_CSI2_FRAME_LINE_NUM — CSI2 Frame/Line Number — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LINE_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FRAME_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	LINE_NUM	Line number
15:0	FRAME_NUM	Frame number

1A041A34 SENINF2_CSI2_GENERIC_SHORT — CSI2 Generic Short Packet — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GENERIC_SHORT_PACKET_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											GENERIC_SHORT_PACKET_DT						
Type											RO					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
31:16	GENERIC_SHORT_PACKET_DATA	Generic short packet data
5:0	GENERIC_SHORT_PACKET_DT	Generic short packet data

1A041A38 SENINF2_CSI2_HSRX_DBG CSI2 HSRX Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DATA_LANE7_HSRX_EN	DATA_LANE6_HSRX_EN	DATA_LANE5_HSRX_EN	DATA_LANE4_HSRX_EN	CLOCK_LANE_HSRX_EN	DATA_LANE3_HSRX_EN	DATA_LANE2_HSRX_EN	DATA_LANE1_HSRX_EN	DATA_LANE0_HSRX_EN
Type								RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	DATA_LANE7_HSRX_EN	Enables data lane 3 HSRX circuit
7	DATA_LANE6_HSRX_EN	Enables data lane 2 HSRX circuit
6	DATA_LANE5_HSRX_EN	Enables data lane 1 HSRX circuit
5	DATA_LANE4_HSRX_EN	Enables data lane 0 HSRX circuit
4	CLOCK_LANE_HSRX_EN	Enables clock lane HSRX circut
3	DATA_LANE3_HSRX_EN	Enables data lane 3 HSRX circuit
2	DATA_LANE2_HSRX_EN	Enables data lane 2 HSRX circuit
1	DATA_LANE1_HSRX_EN	Enables data lane 1 HSRX circuit
0	DATA_LANE0_HSRX_EN	Enables data lane 0 HSRX circuit

1A041A3C SENINF2_CSI2_DI CSI2 Data Interleaving Parameters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DT3						VC3		DT2						VC2	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DT1						VC1		DT0						VC0	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:26	DT3	Data type identifier
25:24	VC3	Virtual channel identifier
23:18	DT2	Data type identifier
17:16	VC2	Virtual channel identifier
15:10	DT1	Data type identifier
9:8	VC1	Virtual channel identifier
7:2	DT0	Data type identifier
1:0	VC0	Virtual channel identifier

1A041A40 SENINF2_CSI2_HS_TRAIL **CSI2 HS Trail Timing Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									HS_TRAIL_PARAMETER							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	HS_TRAIL_PARAMETER	HS TRAIL parameter

1A041A44 SENINF2_CSI2_DI_CTRL **CSI2 Data Interleaving Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						DT3_INTERLEAVING		VC3_INTERLEAVING						DT2_INTERLEAVING		VC2_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DT1_INTERLEAVING		VC1_INTERLEAVING						DT0_INTERLEAVING		VC0_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0

Bit(s)	Name	Description
26:25	DT3_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
24	VC3_INTERLEAVING	**Virtual channel identifier interleaving**
18:17	DT2_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude

Bit(s)	Name	Description
16	VC2_INTERLEAVING	**Virtual channel identifier interleaving**
10:9	DT1_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
8	VC1_INTERLEAVING	**Virtual channel identifier interleaving**
2:1	DT0_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
0	VC0_INTERLEAVING	**Virtual channel identifier interleaving**

1A041A48 SENINF2_CSI2_LNRD_FSM_X CSI2 Data Lane RX FSM Other 01010101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LNRD7_RX_FSM								LNRD6_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		LNRD5_RX_FSM								LNRD4_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1

Bit(s)	Name	Description
30:24	LNRD7_RX_FSM	RX FSM of data lane 3
22:16	LNRD6_RX_FSM	RX FSM of data lane 2
14:8	LNRD5_RX_FSM	RX FSM of data lane 1
6:0	LNRD4_RX_FSM	RX FSM of data lane 0

1A041A4C SENINF2_CSI2_DETECT_CON1 CSI2 CPHY Detect Control sync 0E492300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				SYNC_WORD												
Type				RW												
Reset				0	1	1	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYNC_WORD								DETECT_SYNC_MASK							DETECT_SYNC_DISABLE
Type	RW								RW							RW
Reset	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:8	SYNC_WORD	
7:1	DETECT_SYNC_MASK	
0	DETECT_SYNC_DISABLE	

Bit(s)	Name	Description

1A041A50 SENINF2_CSI2_DETECT_CON2 **CSI2 CPHY Detect Control Escape** **0E492300**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				ESCAPE_WORD												
Type				RW												
Reset				0	1	1	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ESCAPE_WORD								DETECT_ESCAPE_MASK							DETECT_ESCAPE_DISABLE
Type	RW								RW							RW
Reset	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:8	ESCAPE_WORD	
7:1	DETECT_ESCAPE_MASK	
0	DETECT_ESCAPE_DISABLE	

1A041A54 SENINF2_CSI2_DETECT_CON3 **CSI2 CPHY Detect Control Post** **12492400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				POST_WORD												
Type				RW												
Reset				1	0	0	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	POST_WORD								DETECT_POST_MASK							DETECT_POST_DISABLE
Type	RW								RW							RW
Reset	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:8	POST_WORD	
7:1	DETECT_POST_MASK	
0	DETECT_POST_DISABLE	

1A041A58 SENINF2_CSI2_RLR0_CON0 **CSI2 CPHY RLR0 CON0** **FFFFFF00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLR0_PRBS_SEED_2								RLR0_PRBS_SEED_1							

Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLR0_PRBS_SEED_0								RLR0_PRBS_PATTERN_SEL							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RLR0_PRBS_SEED_2	
23:16	RLR0_PRBS_SEED_1	
15:8	RLR0_PRBS_SEED_0	
7:0	RLR0_PRBS_PATTERN_SEL	

1A041A5C SENINF2_CSI2_RLR1_CON0 CSI2 CPHY RLR1 CON0 FFFFFF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLR1_PRBS_SEED_2								RLR1_PRBS_SEED_1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLR1_PRBS_SEED_0								RLR1_PRBS_PATTERN_SEL							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RLR1_PRBS_SEED_2	
23:16	RLR1_PRBS_SEED_1	
15:8	RLR1_PRBS_SEED_0	
7:0	RLR1_PRBS_PATTERN_SEL	

1A041A60 SENINF2_CSI2_RLR2_CON0 CSI2 CPHY RLR2 CON0 FFFFFF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLR2_PRBS_SEED_2								RLR2_PRBS_SEED_1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLR2_PRBS_SEED_0								RLR2_PRBS_PATTERN_SEL							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RLR2_PRBS_SEED_2	
23:16	RLR2_PRBS_SEED_1	
15:8	RLR2_PRBS_SEED_0	
7:0	RLR2_PRBS_PATTERN_SEL	

1A041A64 SENINF2_CSI2_RLR_CON0 CSI2 CPHY RLR CON0 FFFFFF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLRN_PRBS_SEED_2								RLRN_PRBS_SEED_1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLRN_PRBS_SEED_0								RLRN_PRBS_PATTERN_SEL							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RLRN_PRBS_SEED_2	
23:16	RLRN_PRBS_SEED_1	
15:8	RLRN_PRBS_SEED_0	
7:0	RLRN_PRBS_PATTERN_SEL	

1A041A68 SENINF2_CSI2_MUX_CON CSI2 Pin Pux Sel 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												POST_PACKET_IGNORE_EN	RLR_PATTERN_DELAY_EN	CPHY_RX_EXTERNAL_EN	CPHY_TX_EXTERNAL_EN	DPHY_RX_EXTERNAL_EN
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	POST_PACKET_IGNORE_EN	
3	RLR_PATTERN_DELAY_EN	
2	CPHY_RX_EXTERNAL_EN	
1	CPHY_TX_EXTERNAL_EN	
0	DPHY_RX_EXTERNAL_EN	

1A041A6C SENINF2_CSI2_DETECT_DBG0 CSI2 Detection Debug 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		POSITION_SYNC_LANE2_ST				DETECT_POST_LANE2_ST	DETECT_ESCAPE_LANE2_ST	DETECT_SYNC_LANE2_ST		POSITION_ESCAPE_LANE1_ST				POSITION_SYNC_LANE1_ST		
Type		RO				RO	RO	RO		RO				RO		
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	POSITION_SYNC_LANE1_ST	DETECT_POST_LANE1_ST	DETECT_ESCAPE_LANE1_ST	DETECT_SYNC_LANE1_ST		POSITION_ESCAPE_LANE0_ST				POSITION_SYNC_LANE0_ST				DETECT_POST_LANE0_ST	DETECT_ESCAPE_LANE0_ST	DETECT_SYNC_LANE0_ST
Type	RO	RO	RO	RO		RO				RO				RO	RO	RO
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:27	POSITION_SYNC_LANE2_ST	
26	DETECT_POST_LANE2_ST	
25	DETECT_ESCAPE_LANE2_ST	
24	DETECT_SYNC_LANE2_ST	
22:19	POSITION_ESCAPE_LANE1_ST	
18:15	POSITION_SYNC_LANE1_ST	
14	DETECT_POST_LANE1_ST	
13	DETECT_ESCAPE_LANE1_ST	
12	DETECT_SYNC_LANE1_ST	
10:7	POSITION_ESCAPE_LANE0_ST	
6:3	POSITION_SYNC_LANE0_ST	
2	DETECT_POST_LANE0_ST	
1	DETECT_ESCAPE_LANE0_ST	
0	DETECT_SYNC_LANE0_ST	

1A041A70 SENINF2_CSI2_DETECT_DBG1 — CSI2 Detection Debug 1 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													POSITION_ESCAPE_LANE2_ST			
Type													RO			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	POSITION_ESCAPE_LANE2_ST	

1A041A74 SENINF2_CSI2_RESYNC_MERGE_CTL — CSI2 Lane Resync Merge Control — 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								LANE_RES				LANE_MER		CPHY_LANE_RESYNC_CNT		

								YNC_FLUSH_EN				GE_INPUT_SEL				
Type								RW				RW		RW		
Reset								0				0		0	0	1

Bit(s)	Name	Description
8	LANE_RESYNC_FLUSH_EN	
4	LANE_MERGE_INPUT_SEL	
2:0	CPHY_LANE_RESYNC_CNT	

1A041A78 SENINF2_CSI2_CTRL_TRIO_MUX — CSI2 Control Trio Mux — 00000088

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TRIO2_MUX			TRIO1_MUX			TRIO0_MUX		
Type								RW			RW			RW		
Reset								0	1	0	0	0	1	0	0	0

Bit(s)	Name	Description
8:6	TRIO2_MUX	
5:3	TRIO1_MUX	
2:0	TRIO0_MUX	

1A041A7C SENINF2_CSI2_CTRL_TRIO_CON — CSI2 Control Trio Config — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											TRIO2_HSRX_EN	TRIO2_LPRX_EN	TRIO1_HSRX_EN	TRIO1_LPRX_EN	TRIO0_HSRX_EN	TRIO0_LPRX_EN
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5	TRIO2_HSRX_EN	
4	TRIO2_LPRX_EN	
3	TRIO1_HSRX_EN	
2	TRIO1_LPRX_EN	
1	TRIO0_HSRX_EN	
0	TRIO0_LPRX_EN	

Bit(s)	Name	Description

1A041A80 SENINF2_FIX_ADDR_CPHY0_DBG cphy_fix_point_addr_cphy0_debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								WORD_COUNT_OVER_FLOAT_CPHY0	ERROR_COUNT_CPHY0							
Type								RO	RO							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
24	WORD_COUNT_OVER_FLOAT_CPHY0	
23:16	ERROR_COUNT_CPHY0	

1A041A84 SENINF2_FIX_ADDR_CPHY1_DBG cphy_fix_point_addr_cphy1_debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								WORD_COUNT_OVER_FLOAT_CPHY1	ERROR_COUNT_CPHY1							
Type								RO	RO							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
24	WORD_COUNT_OVER_FLOAT_CPHY1	
23:16	ERROR_COUNT_CPHY1	

1A041A88 SENINF2_FIX_ADDR_CPH cphy_fix_point_addr_cphy2_debug 00000000

Y2_DBG

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								WORD_COUNT_OVER_FLOAT_CPHY2	ERRO R_CO UNT_ CPHY 2							
Type								RO	RO							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
24	WORD_COUNT_OVER_FLOAT_CPHY2	
23:16	ERROR_COUNT_CPHY2	

1A041A8C SENINF2_FIX_ADDR_DBG cphy_fix_point_addr_debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								WORD_COUNT_OVER_FLOAT	ERRO R_CO UNT							
Type								RO	RO							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
24	WORD_COUNT_OVER_FLOAT	
23:16	ERROR_COUNT	

1A041A90 SENINF2_WIRE_STATE_DECODE_CPHY0_DBG0 cphy_wire_state_decode_cphy0_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYMBOL_STREAM0_CPHY0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYMBOL_STREAM0_CPHY0															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SYMBOL_STREAM0_CPHY0	

1A041A94 SENINF2_WIRE_STATE_DECODE_CPHY0_DBG1 cphy_wire_state_decode_cphy0_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SYMBOL_STREAM_VALID_CPHY0	SYMBOL_STREAM1_CPHY0									
Type						RO	RO									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	SYMBOL_STREAM_VALID_CPHY0	
9:0	SYMBOL_STREAM1_CPHY0	

1A041A98 SENINF2_WIRE_STATE_DECODE_CPHY1_DBG0 cphy_wire_state_decode_cphy1_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYMBOL_STREAM0_CPHY1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYMBOL_STREAM0_CPHY1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SYMBOL_STREAM0_CPHY1	

1A041A9C SENINF2_WIRE_STATE_DECODE_CPHY1_DBG1 cphy_wire_state_decode_cphy1_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SYMBOL_STREAM_VALID_CPHY1	SYMBOL_STREAM1_CPHY1									
Type						RO	RO									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	SYMBOL_STREAM_VALID_CPHY1	
9:0	SYMBOL_STREAM1_CPHY1	

1A041AA0 SENINF2_WIRE_STATE_DECODE_CPHY2_DBG0 cphy_wire_state_decode_cphy2_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYMBOL_STREAM0_CPHY2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYMBOL_STREAM0_CPHY2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SYMBOL_STREAM0_CPHY2	

1A041AA4 SENINF2_WIRE_STATE_DECODE_CPHY2_DBG1 cphy_wire_state_decode_cphy2_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SYMBOL_STREAM_VALID_CPHY2	SYMBOL_STREAM1_CPHY2									
Type						RO	RO									

Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	SYMBOL_STREAM_VALID_CPHY2	
9:0	SYMBOL_STREAM1_CPHY2	

1A041AA8 SENINF2_SYNC_RESYNC_CTL **CSI2 Sync Resync Control** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													FLUSH_VALID	SYNC_DETECTION_SEL		
Type													RW	RW		
Reset													0	0	0	1

Bit(s)	Name	Description
3	FLUSH_VALID	
2:0	SYNC_DETECTION_SEL	

1A041AAC SENINF2_POST_DETECT_CTL **CSI2 Post Detect Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															POST_EN	POST_DETECT_DISABLE
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	POST_EN	
0	POST_DETECT_DISABLE	

1A041AB0 SENINF2_WIRE_STATE_DECODE_CONFIG **CSI2 Wire State Decode Config** **00000004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INIT_STATE_DECODE		
Type														RW		
Reset														1	0	0

Bit(s)	Name	Description
2:0	INIT_STATE_DECODE	

1A041AB4 SENINF2_CSI2_CPHY_LNRD_FSM CPHY Data Lane RX FSM 01010100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		TRIO 2_RX _FSM								TRIO1_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TRIO0_RX_FSM														
Type		RO														
Reset		0	0	0	0	0	0	1								

Bit(s)	Name	Description
30:24	TRIO2_RX_FSM	RX FSM of data trio 2
22:16	TRIO1_RX_FSM	RX FSM of data trio 1
14:8	TRIO0_RX_FSM	RX FSM of data trio 0

1A041AB8 SENINF2_FIX_ADDR_CPHY0_DBG0 cphy_fix_point_addr_cphy0_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD_COUNT_CPHY0_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY0_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD_COUNT_CPHY0_DBG0	

1A041ABC SENINF2_FIX_ADDR_CPH cphy_fix_point_addr_cphy0_debug1 00000000

Y0_DBG1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY0_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY0_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERROR_RECORD_CPHY0_DBG0	
15:0	WORD_COUNT_CPHY0_DBG1	

1A041AC0 SENINF2_FIX_ADDR_CPHY0_DBG2 cphy_fix_point_addr_cphy0_debug2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY0_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERROR_RECORD_CPHY0_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ERROR_RECORD_CPHY0_DBG1	

1A041AC4 SENINF2_FIX_ADDR_CPHY1_DBG0 cphy_fix_point_addr_cphy1_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD_COUNT_CPHY1_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY1_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD_COUNT_CPHY1_DBG0	

1A041AC8 SENINF2_FIX_ADDR_CPHY1_DBG1 cphy_fix_point_addr_cphy1_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY1_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY1_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERROR_RECORD_CPHY1_DBG0	
15:0	WORD_COUNT_CPHY1_DBG1	

1A041ACC SENINF2_FIX_ADDR_CPHY1_DBG2 cphy_fix_point_addr_cphy1_debug2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY1_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERROR_RECORD_CPHY1_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ERROR_RECORD_CPHY1_DBG1	

1A041AD0 SENINF2_FIX_ADDR_CPHY2_DBG0 cphy_fix_point_addr_cphy2_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD_COUNT_CPHY2_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY2_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD_COUNT_CPHY2_DBG0	

1A041AD4 SENINF2_FIX_ADDR_CPHY2_DBG1 cphy_fix_point_addr_cphy2_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY2_DBG0															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY2_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERROR_RECORD_CPHY2_DBG0	
15:0	WORD_COUNT_CPHY2_DBG1	

1A041AD8 SENINF2_FIX_ADDR_CPHY2_DBG2 cphy_fix_point_addr_cphy2_debug2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY2_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERROR_RECORD_CPHY2_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ERROR_RECORD_CPHY2_DBG1	

1A041ADC SENINF2_FIX_ADDR_DBG cphy_fix_point_addr_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD_COUNT_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD_COUNT_DBG0	

1A041AE0 SENINF2_FIX_ADDR_DBG1 cphy_fix_point_addr_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	WORD_COUNT_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERROR_RECORD_DBG0	
15:0	WORD_COUNT_DBG1	

1A041AE4 SENINF2_FIX_ADDR_DBG2 cphy_fix_point_addr_debug2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERROR_RECORD_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ERROR_RECORD_DBG1	

1A041AE8 SENINF2_CSI2_MODE CSI2 Packet Structure 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	csr_cphy_wc_pos								csr_cphy_di_pos							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						csr_csi2_header_len			csr_csi2_mode							
Type						RW			RW							
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	csr_cphy_wc_pos	
23:16	csr_cphy_di_pos	
10:8	csr_csi2_header_len	0: 4 bytes 1: 12 bytes 2: 24 bytes 4: 36 bytes
7:0	csr_csi2_mode	

1A041AF0 SENINF2_CSI2_DI_EXT CSI2 Data Interleaving Parameters Extend 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DT5						VC5		DT4						VC4	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:10	DT5	Data type identifier
9:8	VC5	Virtual channel identifier
7:2	DT4	Data type identifier
1:0	VC4	Virtual channel identifier

1A041AF4 SENINF2_CSI2_DI_CTRL_EXT CSI2 Data Interleaving Control Extend 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DT5_INTERLEAVING		VC5_INTERLEAVING						DT4_INTERLEAVING		VC4_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0

Bit(s)	Name	Description
10:9	DT5_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
8	VC5_INTERLEAVING	**Virtual channel identifier interleaving**
2:1	DT4_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
0	VC4_INTERLEAVING	**Virtual channel identifier interleaving**

1A041AF8 SENINF2_CSI2_CPHY_LOOPBACK CSI2 SW Trigger sync_init and hs_en 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RELEASE_SYNC	TRIGGER_SYNC

															_INIT	_INIT
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RELEASE_SYNC_INIT	Releases sync_init in CPHY TX loopback test mode
0	TRIGGER_SYNC_INIT	Triggers sync_init and hs_en in CPHY TX loopback test mode

1A041B00 SENINF2_CSI2_PROGSEQ_0 **CSI2 CPHY Program sequence_0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PROG SEQ_ S7				PROG SEQ_ S6				PROGSEQ_S5				PROGSEQ_S4		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PROGSEQ_S3				PROGSEQ_S2				PROGSEQ_S1				PROGSEQ_S0		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	PROGSEQ_S7	Fix symbol for prbs generator
26:24	PROGSEQ_S6	Fix symbol for prbs generator
22:20	PROGSEQ_S5	Fix symbol for prbs generator
18:16	PROGSEQ_S4	Fix symbol for prbs generator
14:12	PROGSEQ_S3	Fix symbol for prbs generator
10:8	PROGSEQ_S2	Fix symbol for prbs generator
6:4	PROGSEQ_S1	Fix symbol for prbs generator
2:0	PROGSEQ_S0	Fix symbol for prbs generator

1A041B04 SENINF2_CSI2_PROGSEQ_1 **CSI2 CPHY Program sequence_1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										PROG SEQ_ S13				PROGSEQ_S 12		
Type										RW				RW		
Reset										0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PROGSEQ_S11				PROGSEQ_S10				PROGSEQ_S9				PROGSEQ_S8		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
22:20	PROGSEQ_S13	Fix symbol for prbs generator
18:16	PROGSEQ_S12	Fix symbol for prbs generator
14:12	PROGSEQ_S11	Fix symbol for prbs generator
10:8	PROGSEQ_S10	Fix symbol for prbs generator
6:4	PROGSEQ_S9	Fix symbol for prbs generator
2:0	PROGSEQ_S8	Fix symbol for prbs generator

Bit(s)	Name	Description

1A041B10 SENINF2_CSI2_INT_EN_EXT **CSI2 Interrupt Enable Extend** **0000071F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_WCLR_EN															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						ERR_SOT_SYNC_HS_TRIO2	ERR_SOT_SYNC_HS_TRIO1	ERR_SOT_SYNC_HS_TRIO0				DPHY3_RESYNC_FIFO_OVERFLOW	DPHY2_RESYNC_FIFO_OVERFLOW	DPHY1_RESYNC_FIFO_OVERFLOW	DPHY0_RESYNC_FIFO_OVERFLOW	ERR_LANE_RESYNC
Type						RW	RW	RW				RW	RW	RW	RW	RW
Reset						1	1	1				1	1	1	1	1

Bit(s)	Name	Description
31	INT_WCLR_EN	Enables interrupt write clear
10	ERR_SOT_SYNC_HS_TRIO2	Enables TRIO2 ERR_SOT_SYNC_HS interrupt
9	ERR_SOT_SYNC_HS_TRIO1	Enables TRIO1 ERR_SOT_SYNC_HS interrupt
8	ERR_SOT_SYNC_HS_TRIO0	Enables TRIO0 ERR_SOT_SYNC_HS interrupt
4	DPHY3_RESYNC_FIFO_OVERFLOW	Enables LANE3_RESYNC_FIFO_OVERFLOW interrupt
3	DPHY2_RESYNC_FIFO_OVERFLOW	Enables LANE2_RESYNC_FIFO_OVERFLOW interrupt
2	DPHY1_RESYNC_FIFO_OVERFLOW	Enables LANE1_RESYNC_FIFO_OVERFLOW interrupt
1	DPHY0_RESYNC_FIFO_OVERFLOW	Enables LANE0_RESYNC_FIFO_OVERFLOW interrupt
0	ERR_LANE_RESYNC	Enables ERR_LANE_RESYNC interrupt

1A041B14 SENINF2_CSI2_INT_STATUS_EXT **CSI2 Interrupt Status Extend** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						ERR_SOT_SYNC_HS_TRIO2_STA	ERR_SOT_SYNC_HS_TRIO1_STA	ERR_SOT_SYNC_HS_TRIO0_STA				DPHY3_RESYNC_FIFO_OVERFLOW_STA	DPHY2_RESYNC_FIFO_OVERFLOW_STA	DPHY1_RESYNC_FIFO_OVERFLOW_STA	DPHY0_RESYNC_FIFO_OVERFLOW_STA	ERR_LANE_RESYNC_STA
Type						RO	RO	RO				RO	RO	RO	RO	RO
Reset						0	0	0				0	0	0	0	0

Bit(s)	Name	Description
10	ERR_SOT_SYNC_HS_TRIO2_STA	Asserted when proper synchronization cannot be expected
9	ERR_SOT_SYNC_HS_TRIO1_STA	Asserted when proper synchronization cannot be expected
8	ERR_SOT_SYNC_HS_TRIO0_STA	Asserted when proper synchronization cannot be expected
4	DPHY3_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of DPHY lane 3 is overflowed
3	DPHY2_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of DPHY lane 2 is overflowed
2	DPHY1_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of DPHY lane 1 is overflowed
1	DPHY0_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of DPHY lane 0 is overflowed
0	ERR_LANE_RESYNC_STA	Asserted when DPHY lane sync detect time is longer than setting resync cycles

1A041B18 SENINF2_CSI2_CPHY_FIX_POINT_RST **CSI2 CPHY fix point reset mode** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CPHY_FIX_POINT_RST_MODE	CPHY_FIX_POINT_SW_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	CPHY_FIX_POINT_RST_MODE	Fix point rest mode
0	CPHY_FIX_POINT_SW_RST	Fix point software reset

1A041B20 SENINF2_CSI2_DPHY_RESYNC_CTL **CSI2 DPHY Lane Resync Control** **00000100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DPHY_RESYNC_CNT								DPHY_RESYNC_FLUSH_EN	DPHY_RESYNC_DATAOUT_OPTION	DPHY_BYPASS_LANE_RESYNC
Type						RW								RW	RW	RW

Reset						0	0	1						0	0	0

Bit(s)	Name	Description
10:8	DPHY_RESYNC_CNT	Detect lane skew cycle count
2	DPHY_RESYNC_FLUSH_EN	Enables lane resync flush
1	DPHY_RESYNC_DATAOUT_OPTION	Data output option
0	DPHY_BYPASS_LANE_RESYNC	Bypass lane resync function

Module name: mipi_rx_config_csi1 Base address: (+1a041800h)

Address	Name	Width	Register Function
1A041800	MIPI_RX_CON00_CSI1	32	MIPI RX Config Register
1A041804	MIPI_RX_CON04_CSI1	32	MIPI RX Config Register
1A041808	MIPI_RX_CON08_CSI1	32	MIPI RX Config Register
1A041824	MIPI_RX_CON24_CSI1	32	MIPI RX Config Register
1A041828	MIPI_RX_CON28_CSI1	32	MIPI RX Config Register
1A041834	MIPI_RX_CON34_CSI1	32	MIPI RX Config Register
1A041838	MIPI_RX_CON38_CSI1	32	MIPI RX Config Register
1A04183C	MIPI_RX_CON3C_CSI1	32	MIPI RX Config Register
1A041840	MIPI_RX_CON40_CSI1	32	MIPI RX Config Register
1A041844	MIPI_RX_CON44_CSI1	32	MIPI RX Config Register
1A041848	MIPI_RX_CON48_CSI1	32	MIPI RX Config Register
1A04184C	MIPI_RX_CON4C_CSI1	32	MIPI RX Config Register
1A041850	MIPI_RX_CON50_CSI1	32	MIPI RX Config Register
1A04187C	MIPI_RX_CON7C_CSI1	32	MIPI RX Config Register
1A041880	MIPI_RX_CON80_CSI1	32	MIPI RX Config Register
1A041884	MIPI_RX_CON84_CSI1	32	MIPI RX Config Register
1A041888	MIPI_RX_CON88_CSI1	32	MIPI RX Config Register
1A04188C	MIPI_RX_CON8C_CSI1	32	MIPI RX Config Register
1A041890	MIPI_RX_CON90_CSI1	32	MIPI RX Config Register
1A041894	MIPI_RX_CON94_CSI1	32	MIPI RX Config Register
1A041898	MIPI_RX_CON98_CSI1	32	MIPI RX Config Register

Address	Name	Width	Register Function
1A0418A0	MIPI_RX_CONA0_CSI1	32	MIPI RX Config Register
1A0418B0	MIPI_RX_CONB0_CSI1	32	Deskew control register
1A0418B4	MIPI_RX_CONB4_CSI1	32	Deskew sync detection sequence
1A0418B8	MIPI_RX_CONB8_CSI1	32	Deskew timing control
1A0418BC	MIPI_RX_CONBC_CSI1	32	Deskew mode
1A0418C0	MIPI_RX_CONC0_CSI1	32	Interrupt enable
1A0418C4	MIPI_RX_CONC4_CSI1	32	Interrupt status
1A0418C8	MIPI_RX_CONC8_CSI1	32	Debug mux select
1A0418CC	MIPI_RX_CONCC_CSI1	32	Debug outputs
1A0418D0	MIPI_RX_COND0_CSI1	32	Deskew delay length

1A041800 MIPI_RX_CON00_CSI1 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_CSI0_LNR3_HSRX_OFFSET_CODE					RG_CSI0_LNR3_HSRX_CAL_EN	RG_CSI0_LNR3_HSRX_CAL_APPLY		RG_CSI0_LNR2_HSRX_OFFSET_CODE					RG_CSI0_LNR2_HSRX_CAL_EN	RG_CSI0_LNR2_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI0_LNR1_HSRX_OFFSET_CODE					RG_CSI0_LNR1_HSRX_CAL_EN	RG_CSI0_LNR1_HSRX_CAL_APPLY		RG_CSI0_LNR0_HSRX_OFFSET_CODE					RG_CSI0_LNR0_HSRX_CAL_EN	RG_CSI0_LNR0_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	RG_CSI0_LNR3_HSRX_OFFSET_CODE	**Lane3 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
25	RG_CSI0_LNR3_HSRX_CAL_EN	**Lane3 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
24	RG_CSI0_LNR3_HSRX_CAL_APPLY	**Lane3 HSRX offset calibration apply:** 1'b0: don't use calibration result

Bit(s)	Name	Description
		1'b1: use calibration result
22:18	RG_CSI0_LNR2_HSRX_OFFSET_CODE	**Lane2 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
17	RG_CSI0_LNR2_HSRX_CAL_EN	**Lane2 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
16	RG_CSI0_LNR2_HSRX_CAL_APPLY	**Lane2 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
14:10	RG_CSI0_LNR1_HSRX_OFFSET_CODE	**Lane1 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
9	RG_CSI0_LNR1_HSRX_CAL_EN	**Lane1 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
8	RG_CSI0_LNR1_HSRX_CAL_APPLY	**Lane1 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
6:2	RG_CSI0_LNR0_HSRX_OFFSET_CODE	**Lane0 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
1	RG_CSI0_LNR0_HSRX_CAL_EN	**Lane0 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
0	RG_CSI0_LNR0_HSRX_CAL_APPLY	**Lane0 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result

1A041804 MIPI_RX_CON04_CSI1 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_CSI0_LNR7_HSRX_OFFSET_CODE					RG_CSI0_LNR7_HSRX_CAL_EN	RG_CSI0_LNR7_HSRX_CAL_APPLY		RG_CSI0_LNR6_HSRX_OFFSET_CODE					RG_CSI0_LNR6_HSRX_CAL_EN	RG_CSI0_LNR6_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI0_LNR5_HSRX_OFFSET_CODE					RG_CSI0_LNR5_HSRX_CAL_EN	RG_CSI0_LNR5_HSRX_CAL_APPLY		RG_CSI0_LNR4_HSRX_OFFSET_CODE					RG_CSI0_LNR4_HSRX_CAL_EN	RG_CSI0_LNR4_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	RG_CSI0_LNR7_HSRX_OFFSET_CODE	**Lane7 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
25	RG_CSI0_LNR7_HSRX_CAL_EN	**Lane7 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
24	RG_CSI0_LNR7_HSRX_CAL_APPLY	**Lane7 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
22:18	RG_CSI0_LNR6_HSRX_OFFSET_CODE	**Lane6 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
17	RG_CSI0_LNR6_HSRX_CAL_EN	**Lane6 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
16	RG_CSI0_LNR6_HSRX_CAL_APPLY	**Lane6 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
14:10	RG_CSI0_LNR5_HSRX_OFFSET_CODE	**Lane5 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
9	RG_CSI0_LNR5_HSRX_CAL_EN	**Lane5 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
8	RG_CSI0_LNR5_HSRX_CAL_APPLY	**Lane5 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
6:2	RG_CSI0_LNR4_HSRX_OFFSET_CODE	**Lane4 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
1	RG_CSI0_LNR4_HSRX_CAL_EN	**Lane4 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
0	RG_CSI0_LNR4_HSRX_CAL_APPLY	**Lane4 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result

1A041808 MIPI_RX_CON08_CSI1 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_CSI0_LNR11_HSRX_OFFSET_CODE					RG_CSI0_LNR11_HSRX_CAL_EN	RG_CSI0_LNR11_HSRX_CAL_APPLY		RG_CSI0_LNR10_HSRX_OFFSET_CODE					RG_CSI0_LNR10_HSRX_CAL_EN	RG_CSI0_LNR10_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name		RG_CSI0_LNR9_HSRX_OFFSET_CODE					RG_CSI0_LNR9_HSRX_CAL_EN	RG_CSI0_LNR9_HSRX_CAL_APPLY		RG_CSI0_LNR8_HSRX_OFFSET_CODE					RG_CSI0_LNR8_HSRX_CAL_EN	RG_CSI0_LNR8_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	RG_CSI0_LNR11_HSRX_OFFSET_CODE	**Lane11 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
25	RG_CSI0_LNR11_HSRX_CAL_EN	**Lane11 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
24	RG_CSI0_LNR11_HSRX_CAL_APPLY	**Lane11 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
22:18	RG_CSI0_LNR10_HSRX_OFFSET_CODE	**Lane10 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
17	RG_CSI0_LNR10_HSRX_CAL_EN	**Lane10 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
16	RG_CSI0_LNR10_HSRX_CAL_APPLY	**Lane10 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
14:10	RG_CSI0_LNR9_HSRX_OFFSET_CODE	**Lane9 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
9	RG_CSI0_LNR9_HSRX_CAL_EN	**Lane9 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
8	RG_CSI0_LNR9_HSRX_CAL_APPLY	**Lane9 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
6:2	RG_CSI0_LNR8_HSRX_OFFSET_CODE	**Lane8 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
1	RG_CSI0_LNR8_HSRX_CAL_EN	**Lane8 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
0	RG_CSI0_LNR8_HSRX_CAL_APPLY	**Lane8 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result

1A041824 MIPI_RX_CON24_CSI1 **MIPI RX Config Register** **E4000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSIo _BIST_LN3_MUX		CSIo_BIST_LN2_MUX		CSIo_BIST_LN1_MUX		CSIo_BIST_LNo_MUX		CSIo_BIST_SETTLE_DELAY							
Type	RW		RW		RW		RW		RW							
Reset	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSIo_BIST_TERM_DELAY								CSIo_BIST_CLK4X_SEL	CSIo_BIST_CLK_SEL	CSIo_BIST_FIX_PAT			CSIo_BIST_EN	CSIo_BIST_NUM	
Type	RW								RW	RW	RW			RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0			0	0	0

Bit(s)	Name	Description
31:30	CSIo_BIST_LN3_MUX	**CSIo Lane mux**
29:28	CSIo_BIST_LN2_MUX	**CSIo Lane mux**
27:26	CSIo_BIST_LN1_MUX	**CSIo Lane mux**
25:24	CSIo_BIST_LNo_MUX	**CSIo Lane mux**
23:16	CSIo_BIST_SETTLE_DELAY	**CSIo Settle Delay Setting**
15:8	CSIo_BIST_TERM_DELAY	**CSIo Term Delay Setting**
7	CSIo_BIST_CLK4X_SEL	**CSIo CLK4X Sel** 0: inverse 1: not inverse
6	CSIo_BIST_CLK_SEL	**CSIo CLK Sel** 0: inverse 1: not inverse
5	CSIo_BIST_FIX_PAT	**CSIo Bist Patern** 0: Random 1: Fix
2	CSIo_BIST_EN	**CSIo Bist Enalbe**
1:0	CSIo_BIST_NUM	**CSIo Bist num** 0: 1 lane 1: 2 lane 2: 3 lane 3: 4 lane

1A041828 MIPI_RX_CON28_CSI1 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CSIo_BIST_CSI2_DATA_OK	CSIo_BIST_LANE_FSM_OK	CSIo_BIST_HS_FSM_OK	CSIo_BIST_DATA_OK	CSIo_BIST_START
Type												RO	RO	RO	RO	RO
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	CSIo_BIST_CSI2_DATA_OK	CSIo BIST CSI2 Data ok

Bit(s)	Name	Description
3	CSIo_BIST_LANE_FSM_OK	CSIo BIST High Speed FSM ok
2	CSIo_BIST_HS_FSM_OK	CSIo BIST Data Lane FSM ok
1	CSIo_BIST_DATA_OK	CSIo BIST DPHY Data ok
0	CSIo_BIST_START	CSIo BIST start status

1A041834 MIPI_RX_CON34_CSI1 MIPI RX Config Register E4000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSIo_BIST_LN7_MUX		CSIo_BIST_LN6_MUX		CSIo_BIST_LN5_MUX		CSIo_BIST_LN4_MUX		CSIo_BIST_HSDET_MUX							
Type	RW		RW		RW		RW		RW							
Reset	1	1	1	0	0	1	0	0	0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BIST_MODE
Type																RW
Reset																0

Bit(s)	Name	Description
31:30	CSIo_BIST_LN7_MUX	CSIo Lane mux
29:28	CSIo_BIST_LN6_MUX	CSIo Lane mux
27:26	CSIo_BIST_LN5_MUX	CSIo Lane mux
25:24	CSIo_BIST_LN4_MUX	CSIo Lane mux
23:22	CSIo_BIST_HSDET_MUX	CSIo HSDET mux
0	BIST_MODE	BIST mode enable

1A041838 MIPI_RX_CON38_CSI1 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_ckphase_trio2					rg_ckphase_trio1						rg_ckphase_trio0				
Type	RW					RW						RW				
Reset	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						MIPI_RX_SW_CPHY_RX_MODE	MIPI_RX_SW_CPHY_TX_MODE	MIPI_RX_SW_RST					MIPI_RX_HW_CAL_OPTION	MIPI_RX_HW_CAL_START	MIPI_RX_SW_CAL_MODE	MIPI_RX_SW_CTRL_MODE
Type						RW	RW	RW					RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:27	rg_ckphase_trio2	
26:22	rg_ckphase_trio1	
20:16	rg_ckphase_trio0	
10	MIPI_RX_SW_CPHY_RX_MODE	**CPHY RX SW control mode**
9	MIPI_RX_SW_CPHY_TX_MODE	**CPHY TX SW control mode**
8:4	MIPI_RX_SW_RST	**SW reset**
3	MIPI_RX_HW_CAL_OPTION	**HW calibration option**

Bit(s)	Name	Description
		0: 8cycles 1 :16 cycles
2	MIPI_RX_HW_CAL_START	**HW calibration trigger**
1	MIPI_RX_SW_CAL_MODE	**SW calibration mode**
0	MIPI_RX_SW_CTRL_MODE	**SW control mode**

1A04183C MIPI_RX_CON3C_CSI1 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIPI_RX_SW_CTRL_															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIPI_RX_SW_CTRL_															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MIPI_RX_SW_CTRL_	SW control

1A041840 MIPI_RX_CON40_CSI1 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_CSIo_LNRD3_HSRX_INVERT	RG_CSIo_LNRD3_LPRX_SWAP	RG_CSIo_LNRD2_HSRX_INVERT	RG_CSIo_LNRD2_LPRX_SWAP	RG_CSIo_LNRD1_HSRX_INVERT	RG_CSIo_LNRD1_LPRX_SWAP	RG_CSIo_LNRDo_HSRX_INVERT	RG_CSIo_LNRDo_LPRX_SWAP			RG_CSIo_LNRC_HSRX_INVERT	RG_CSIo_LNRC_LPRX_SWAP
Type					RW	RW	RW	RW	RW	RW	RW	RW			RW	RW
Reset					0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
11	RG_CSIo_LNRD3_HSRX_INVERT	
10	RG_CSIo_LNRD3_LPRX_SWAP	
9	RG_CSIo_LNRD2_HSRX_INVERT	
8	RG_CSIo_LNRD2_LPRX_SWAP	
7	RG_CSIo_LNRD1_HSRX_INVERT	
6	RG_CSIo_LNRD1_LPRX_SWAP	
5	RG_CSIo_LNRDo_HSRX_INVERT	
4	RG_CSIo_LNRDo_LPRX_SWAP	
1	RG_CSIo_LNRC_HSRX_INVERT	
0	RG_CSIo_LNRC_LPRX_SWAP	

1A041844 MIPI_RX_CON MIPI RX Config Register 00000000

N44_CSI1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSIo_L NR3_HSRX_ OFFSET_CO DE					DA_CSIo_ LNR3_HSR X_CAL_EN	DA_CSIo_ LNR3_HSR X_CAL_AP PLY		DA_CSIo_LNR2_HSRX_OFF SET_CODE					DA_CSIo_ LNR2_HSR X_CAL_EN	DA_CSIo_ LNR2_HSR X_CAL_AP PLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DA_CSIo_LNR1_HSRX_OFF SET_CODE					DA_CSIo_ LNR1_HSR X_CAL_EN	DA_CSIo_ LNR1_HSR X_CAL_AP PLY		DA_CSIo_LNR0_HSRX_OFF SET_CODE					DA_CSIo_ LNR0_HSR X_CAL_EN	DA_CSIo_ LNR0_HSR X_CAL_AP PLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	DA_CSI0_LNR3_HSRX_OFFSET_CODE	
25	DA_CSI0_LNR3_HSRX_CAL_EN	
24	DA_CSI0_LNR3_HSRX_CAL_APPLY	
22:18	DA_CSI0_LNR2_HSRX_OFFSET_CODE	
17	DA_CSI0_LNR2_HSRX_CAL_EN	
16	DA_CSI0_LNR2_HSRX_CAL_APPLY	
14:10	DA_CSI0_LNR1_HSRX_OFFSET_CODE	
9	DA_CSI0_LNR1_HSRX_CAL_EN	
8	DA_CSI0_LNR1_HSRX_CAL_APPLY	
6:2	DA_CSI0_LNR0_HSRX_OFFSET_CODE	
1	DA_CSI0_LNR0_HSRX_CAL_EN	
0	DA_CSI0_LNR0_HSRX_CAL_APPLY	

1A041848 MIPI_RX_CO N48_CSI1 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSIo_L NR7_HSRX_ OFFSET_CO DE					DA_CSIo_ LNR7_HSR X_CAL_EN	DA_CSIo_ LNR7_HSR X_CAL_AP PLY		DA_CSIo_LNR6_HSRX_OFF SET_CODE					DA_CSIo_ LNR6_HSR X_CAL_EN	DA_CSIo_ LNR6_HSR X_CAL_AP PLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DA_CSIo_LNR5_HSRX_OFF SET_CODE					DA_CSIo_	DA_CSIo_		DA_CSIo_LNR4_HSRX_OFF SET_CODE					DA_CSIo_	DA_CSIo_

							LNR5_HSRX_CAL_EN	LNR5_HSRX_CAL_APPLY							LNR4_HSRX_CAL_EN	LNR4_HSRX_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	DA_CSI0_LNR7_HSRX_OFFSET_CODE	
25	DA_CSI0_LNR7_HSRX_CAL_EN	
24	DA_CSI0_LNR7_HSRX_CAL_APPLY	
22:18	DA_CSI0_LNR6_HSRX_OFFSET_CODE	
17	DA_CSI0_LNR6_HSRX_CAL_EN	
16	DA_CSI0_LNR6_HSRX_CAL_APPLY	
14:10	DA_CSI0_LNR5_HSRX_OFFSET_CODE	
9	DA_CSI0_LNR5_HSRX_CAL_EN	
8	DA_CSI0_LNR5_HSRX_CAL_APPLY	
6:2	DA_CSI0_LNR4_HSRX_OFFSET_CODE	
1	DA_CSI0_LNR4_HSRX_CAL_EN	
0	DA_CSI0_LNR4_HSRX_CAL_APPLY	

1A04184C MIPI_RX_CON4C_CSI1 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSI0_LNR11_HSRX_OFFSET_CODE					DA_CSI0_LNR11_HSRX_CAL_EN	DA_CSI0_LNR11_HSRX_CAL_APPLY		DA_CSI0_LNR10_HSRX_OFFSET_CODE					DA_CSI0_LNR10_HSRX_CAL_EN	DA_CSI0_LNR10_HSRX_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DA_CSI0_LNR9_HSRX_OFFSET_CODE					DA_CSI0_LNR9_HSRX_CAL_EN	DA_CSI0_LNR9_HSRX_CAL_APPLY		DA_CSI0_LNR8_HSRX_OFFSET_CODE					DA_CSI0_LNR8_HSRX_CAL_EN	DA_CSI0_LNR8_HSRX_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	DA_CSI0_LNR11_HSRX_OFFSET_CODE	
25	DA_CSI0_LNR11_HSRX_CAL_EN	
24	DA_CSI0_LNR11_HSRX_CAL_AP	

Bit(s)	Name	Description
	PLY	
22:18	DA_CSI0_LNR10_HSRX_OFFSET_CODE	
17	DA_CSI0_LNR10_HSRX_CAL_EN	
16	DA_CSI0_LNR10_HSRX_CAL_APPLY	
14:10	DA_CSI0_LNR9_HSRX_OFFSET_CODE	
9	DA_CSI0_LNR9_HSRX_CAL_EN	
8	DA_CSI0_LNR9_HSRX_CAL_APPLY	
6:2	DA_CSI0_LNR8_HSRX_OFFSET_CODE	
1	DA_CSI0_LNR8_HSRX_CAL_EN	
0	DA_CSI0_LNR8_HSRX_CAL_APPLY	

1A041850 MIPI_RX_CON50_CSI1 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_CSI0_BCLK_INV
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_CSI0_BCLK_INV	**CSI0 byte clock** 0: Not inverse 1: inverse

1A04187C MIPI_RX_CON7C_CSI1 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DA_CSI0_LNRD0_HSRX_DELAY_CODE					DA_CSI0_LNRD0_HSRX_DELAY_APPLY	DA_CSI0_LNRD0_HSRX_DELAY_EN
Type											RO				RO	RO
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:2	DA_CSI0_LNRD0_HSRX_DELAY_CODE	
1	DA_CSI0_LNRD0_HSRX_DELAY_APPLY	
0	DA_CSI0_LNRD0_HSRX_DELAY_EN	

1A041880 MIPI_RX_CON80_CSI1 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DA_CSI0_LNRD1_HSRX_DELAY_CODE					DA_CSI0_LNRD1_HSRX_DELAY_APPLY	DA_CSI0_LNRD1_HSRX_DELAY_EN
Type											RO				RO	RO
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:2	DA_CSI0_LNRD1_HSRX_DELAY_CODE	
1	DA_CSI0_LNRD1_HSRX_DELAY_APPLY	
0	DA_CSI0_LNRD1_HSRX_DELAY_EN	

1A041884 MIPI_RX_CON84_CSI1 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DA_CSI0_LNRD2_HSRX_DELAY_CODE					DA_CSI0_LNRD2_HSRX_DELAY_APPLY	DA_CSI0_LNRD2_HSRX_DELAY_EN
Type											RO				RO	RO
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:2	DA_CSI0_LNRD2_HSRX_DELAY_CODE	
1	DA_CSI0_LNRD2_HSRX_DELAY_APPLY	
0	DA_CSI0_LNRD2_HSRX_DELAY_EN	

1A041888 MIPI_RX_CON88_CSI1 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DA_CSI0_LNRD3_HSRX_DELAY_CODE					DA_CSI0_LNRD3_HSRX_DELAY_APPLY	DA_CSI0_LNRD3_HSRX_DELAY_EN
Type											RO				RO	RO
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:2	DA_CSI0_LNRD3_HSRX_DELAY_CODE	
1	DA_CSI0_LNRD3_HSRX_DELAY_APPLY	
0	DA_CSI0_LNRD3_HSRX_DELAY_EN	

1A04188C MIPI_RX_CON8C_CSI1 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSI0_LNRD0_HSRX_DELAY_CODE						RG_CSI0_LNRD0_HSRX_DELAY_APPLY	RG_CSI0_LNRD0_HSRX_DELAY_EN
Type									RW						RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
7:2	RG_CSI0_LNRD0_HSRX_DELAY_CODE	
1	RG_CSI0_LNRD0_HSRX_DELAY_APPLY	
0	RG_CSI0_LNRD0_HSRX_DELAY_EN	

1A041890 MIPI_RX_CON90_CSI1 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSI0_LNRD1_HSRX_DELAY_CODE						RG_CSI0_LNRD1_HSRX_DELAY_APPLY	RG_CSI0_LNRD1_HSRX_DELAY_EN
Type									RW						RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSI0_LNRD1_HSRX_DELAY_CODE	
1	RG_CSI0_LNRD1_HSRX_DELAY_APPLY	
0	RG_CSI0_LNRD1_HSRX_DELAY_EN	

1A041894 MIPI_RX_CON94_CSI1 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSI0_LNRD2_HSRX_DELAY_CODE						RG_CSI0_LNRD2_HSRX_DELAY_APPLY	RG_CSI0_LNRD2_HSRX_DELAY_EN
Type									RW						RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
7:2	RG_CSI0_LNRD2_HSRX_DELAY_CODE	
1	RG_CSI0_LNRD2_HSRX_DELAY_APPLY	
0	RG_CSI0_LNRD2_HSRX_DELAY_EN	

1A041898 MIPI_RX_CON98_CSI1 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSI0_LNRD3_HSRX_DELAY_CODE						RG_CSI0_LNRD3_HSRX_DELAY_APPLY	RG_CSI0_LNRD3_HSRX_DELAY_EN
Type									RW						RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSI0_LNRD3_HSRX_DELAY_CODE	
1	RG_CSI0_LNRD3_HSRX_DELAY_APPLY	
0	RG_CSI0_LNRD3_HSRX_DELAY_EN	

1A0418A0 MIPI_RX_CONA0_CSI1 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSI0_LNRC_HSRX_DELAY_CODE						RG_CSI0_LNRC_HSRX_DELAY_APPLY	RG_CSI0_LNRC_HSRX_DELAY_EN
Type									RW						RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
7:2	RG_CSI0_LNRC_HSRX_DELAY_CODE	
1	RG_CSI0_LNRC_HSRX_DELAY_APPLY	
0	RG_CSI0_LNRC_HSRX_DELAY_EN	

1A0418B0 MIPI_RX_CONB0_CSI1 Deskew control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DESKEW_ENABLE	DESKEW_IP_SEL														DESKEW_CSI2_RST_ENABLE
Type	RW	RW														RW
Reset	0	0														0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DESKEW_ACC_MODE					DESKEW_TRIGGER_MODE			DESKEW_SW_RST				Delay_APPLY_MODE			
Type	RW					RW			RW				RW			
Reset	0	0	0	0		0	0	0	0				0	0	0	0

Bit(s)	Name	Description
31	DESKEW_ENABLE	**Deskew enable**
30	DESKEW_IP_SEL	0: New IP 1: Old IP
16	DESKEW_CSI2_RST_ENABLE	**Reset CSI2 IP when in DESKEW mode**
15:12	DESKEW_ACC_MODE	**Deskew edge mode**
10:8	DESKEW_TRIGGER_MODE	**Conditions for trigger DESKEW function**
7	DESKEW_SW_RST	**Deskew SW reset**
3:0	Delay_APPLY_MODE	**Delay apply mode:** 00/01: HW mode 10: RG mode 11: SW mode

1A0418B4 MIPI_RX_CONB4_CSI1 Deskew sync detection sequence 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EXPECTED_SYNC_CODE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYNC_CODE_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	EXPECTED_SYNC_CODE	**Programmable sync code**

Bit(s)	Name	Description
15:0	SYNC_CODE_MASK	In normal case, it should be 16'hFFFF. **When the bit is set to 1'b1, HW will compare its value with received sync code.** Otherwise, no compare.

1A0418B8 MIPI_RX_CONB8_CSI1 Deskew timing control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								DESKEW_TIME_OUT_EN	DESKEW_TIME_OUT							
Type								RW	RW							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DESKEW_HOLD_TIME								DESKEW_SETUP_TIME			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
24	DESKEW_TIME_OUT_EN	**Deskew time out enable**
23:16	DESKEW_TIME_OUT	**Deskew time out period** If no deskew sync code is detected, FSM will be reset after this period.
11:8	DESKEW_HOLD_TIME	**Delay code apply hold time**
3:0	DESKEW_SETUP_TIME	**Delay code apply setup time**

1A0418BC MIPI_RX_CONBC_CSI1 Deskew mode 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							DESKEW_LANE_NUMBER						DESKEW_DELAY_APPLY_MODE			
Type							RW						RW			
Reset							0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DESKEW_DETECTION_CNT											DESKEW_DETECTION_MODE			
Type		RW											RW			
Reset		0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
25:24	DESKEW_LANE_NUMBER	Deskew lane number
19:16	DESKEW_DELAY_APPLY_MODE	Deskew delay apply mode
14:8	DESKEW_DETECTION_CNT	Deskew detection count
3:0	DESKEW_DETECTION_MODE	Deskew detection mode

1A0418C0 MIPI_RX_CO Interrupt enable 80000000

NC0_CSI1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DESKEW_INTERRUPT_W1C_EN															
Type	RW															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DESKEW_INTERRUPT_ENABLE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	DESKEW_INTERRUPT_W1C_EN	Interrupt W1C enable
7:0	DESKEW_INTERRUPT_ENABLE	Interrupt enable

1A0418C4 MIPI_RX_CO NC4_CSI1 **Interrupt status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DESKEW_INTERRUPT_STATUS							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DESKEW_INTERRUPT_STATUS	Interrupt status

1A0418C8 MIPI_RX_CO NC8_CSI1 **Debug mux select** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DESKEW_DEBUG_MUX_SELECT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DESKEW_DEBUG_MUX_SELECT	Debug signal select

1A0418CC MIPI_RX_CONCC_CSI1 **Debug outputs** **00100100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DESKEW_DEBUG_OUTPUTS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DESKEW_DEBUG_OUTPUTS															
Type	RO															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DESKEW_DEBUG_OUTPUTS	Debug signal outputs

1A0418D0 MIPI_RX_COND0_CSI1 **Deskew delay length** **0000000F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DESKEW_DELAY_LENGTH						
Type											RW					
Reset											0	0	1	1	1	1

Bit(s)	Name	Description
5:0	DESKEW_DELAY_LENGTH	Deskew delay length

Module name: seninf2_mux Base address: (+1a041d00h)

Address	Name	Width	Register Function
1A041D00	SENINF2_MUX_CTRL	32	SENINF 2 Control Register
1A041D04	SENINF2_MUX_INTEN	32	SENINF 2 Interrupt Enable Register
1A041D08	SENINF2_MUX_INTSTA	32	SENINF 2 Interrupt Status Register
1A041D0C	SENINF2_MUX_SIZE	32	SENINF 2 Image Size Register
1A041D10	SENINF2_MUX_DEBUG_1	32	SENINF 2 Debug Register 1
1A041D14	SENINF2_MUX_DEBUG_2	32	SENINF 2 Debug Register 2
1A041D18	SENINF2_MUX_DEBUG_3	32	SENINF 2 Debug Register 3
1A041D1C	SENINF2_MUX_DEBUG_4	32	SENINF 2 Debug Register 4
1A041D20	SENINF2_MUX_DEBUG_5	32	SENINF 2 Debug Register 5
1A041D24	SENINF2_MUX_DE	32	SENINF 2 Debug Register 6

Address	Name	Width	Register Function
	BUG_6		
1A041D28	SENINF2_MUX_DEBUG_7	32	SENINF 2 Debug Register 7
1A041D2C	SENINF2_MUX_SPARE	32	SENINF 2 spare Register
1A041D30	SENINF2_MUX_DATA	32	SENINF 2 Data Register
1A041D34	SENINF2_MUX_DATA_CNT	32	SENINF 2 Data Count Register
1A041D38	SENINF2_MUX_CROP	32	SENINF 2 Crop Size Register
1A041D3C	SENINF2_MUX_CTRL_EXT	32	SENINF 2 Control Register Extend

1A041D00 SENINF2_MUX_CTRL **SENINF 2 Control Register** **06DF0080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_MUX_EN	CROP_EN	FIFO_FULL_WR_EN		FIFO_FLUSH_EN						FIFO_PUSH_EN					
Type	RW	RW	RW		RW						RW					
Reset	0	0	0	0	0	1	1	0	1	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_SRC_SEL				OVERRUN_RST_EN	SENINF_HSYNC_POL	SENINF_VSYNC_POL	SENINF_PIX_SEL	SENINF_HSYNC_MASK		SENINF_MUX_RDY_VALUE	SENINF_MUX_RDY_MODE			SENINF_IRQ_SW_RST	SENINF_MUX_SW_RST
Type	RW				RW	RW	RW	RW	RW		RW	RW			RW	RW
Reset	0	0	0	0	0	0	0	0	1		0	0			0	0

Bit(s)	Name	Description
31	SENINF_MUX_EN	**Enables seninf_mux** 0: Disable 1: Enable
30	CROP_EN	**Sensor crop function**
29:28	FIFO_FULL_WR_EN	0: FIFO write operation is prohibited when FIFO is full. 1: FIFO write operation is prohibited after FIFO full occurs. 2: FIFO write operation is allowed when FIFO is full.
27:22	FIFO_FLUSH_EN	**Normal mode: 6'b011011** JPEG two pixel mode: 6'b011000
21:16	FIFO_PUSH_EN	**Normal mode: 6'b011111** JPEG two pixel mode : 6'b011110
15:12	SENINF_SRC_SEL	**Selects SENINF input source:** {seninf_mux_sel_ext, seninf_mux_sel} 00: OCSI2 VC0 01: Test model 02: CCIR656 03: Parallel sensor 04: Serial sensor 06: OCSI2 VC1 08: NCSI2 VC0 09: NCSI2 VC1

Bit(s)	Name	Description
		0A: NCSI2 VC2 0B: NCSI2 VC3 0C: NCSI2 VC4 0D: NCSI2 VC5
11	OVERRUN_RST_EN	**Enables SENINF mux software reset for overrun** 0: No action 1: Auto self-reset for overrun situation
10	SENINF_HSYNC_POL	**SENINF HSYNC polarity**
9	SENINF_VSYNC_POL	**SENING VSYNC polarity**
8	SENINF_PIX_SEL	**SENINF output bus width:** {seninf_pixel_sel_ext, seninf_pixel_sel} 00: 1 pixel/cycle 01: 2 pixels/cycle 10: 4 pixels/cycle
7	SENINF_HSYNC_MASK	**Masks hsync** 0: Send hsync when vsync = 1 1: Does not send hsync when vsync = 1
5	SENINF_MUX_RDY_VALUE	**seninf_rdy value in force mode**
4	SENINF_MUX_RDY_MODE	0: seninf_rdy normal mode 1: seninf_rdy force mode
1	SENINF_IRQ_SW_RST	**SENINF IRQ software reset, active high** 0: De-assert reset 1: Assert reset
0	SENINF_MUX_SW_RST	**SENINF mux software reset, active high** 0: De-assert reset 1: Assert reset

1A041D04 SENINF2_MUX_INTEN — **SENINF 2 Interrupt Enable Register** — **8000007F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_IRQ_CLR_SEL															
Type	RW															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SENINF_SENSOR_HSIZEERR_IRQ_EN	SENINF_SENSOR_VSIZEERR_IRQ_EN	SENINF_HSIZEERR_IRQ_EN	SENINF_VSIZEERR_IRQ_EN	SENINF_FSMERR_IRQ_EN	SENINF_CRCERR_IRQ_EN	SENINF_OVERRUN_IRQ_EN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										1	1	1	1	1	1	1

Bit(s)	Name	Description
31	SENINF_IRQ_CLR_SEL	0: Read clear 1: Write clear
6	SENINF_SENSOR_HSIZEERR_IRQ_EN	**Enables sensor HSIZE ERROR IRQ**
5	SENINF_SENSOR_VSIZEERR_IR	**Enables sensor VSIZE ERROR IRQ**

Bit(s)	Name	Description
	Q_EN	
4	SENINF_HSIZEERR_IRQ_EN	**Enables async FIFO HSIZE ERROR IRQ**
3	SENINF_VSIZEERR_IRQ_EN	**Enables async FIFO VSIZE ERROR IRQ**
2	SENINF_FSMERR_IRQ_EN	**Enables FSM ERROR IRQ**
1	SENINF_CRCERR_IRQ_EN	**Enables CRR ERROR IRQ**
0	SENINF_OVERRUN_IRQ_EN	**Enables FIFO OVERRUN IRQ**

1A041D08 SENINF2_MUX_INTSTA **SENINF 2 Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SENINF_SENSOR_HSIZEERR_IRQ_STA	SENINF_SENSOR_VSIZEERR_IRQ_STA	SENINF_HSIZEERR_IRQ_STA	SENINF_VSIZEERR_IRQ_STA	SENINF_FSMERR_IRQ_STA	SENINF_CRCERR_IRQ_STA	SENINF_OVERRUN_IRQ_STA
Type										RO	RO	RO	RO	RO	RO	RO
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	SENINF_SENSOR_HSIZEERR_IRQ_STA	Sensor HSIZE ERROR IRQ status
5	SENINF_SENSOR_VSIZEERR_IRQ_STA	Sensor VSIZE ERROR IRQ status
4	SENINF_HSIZEERR_IRQ_STA	Async FIFO HSIZE ERROR IRQ status
3	SENINF_VSIZEERR_IRQ_STA	Async FIFO VSIZE ERROR IRQ status
2	SENINF_FSMERR_IRQ_STA	FSM ERROR IRQ status
1	SENINF_CRCERR_IRQ_STA	CRR ERROR IRQ status
0	SENINF_OVERRUN_IRQ_STA	FIFO OVERRUN IRQ status

1A041D0C SENINF2_MUX_SIZE **SENINF 2 Image Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_HSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_VSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_HSIZE	Senor image horizontal size
15:0	SENINF_VSIZE	Senor image vertical size

1A041D10 SENINF2_MUX_DEBUG_1 SENINF 2 Debug Register 1 0000C303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	1	1	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A041D14 SENINF2_MUX_DEBUG_2 SENINF 2 Debug Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A041D18 SENINF2_MUX_DEBUG_3 SENINF 2 Debug Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A041D1C SENINF2_MUX_DEBUG_4 SENINF 2 Debug Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A041D20 SENINF2_MUX_DEBUG_5 SENINF 2 Debug Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A041D24 SENINF2_MUX_DEBUG_6 SENINF 2 Debug Register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A041D28 SENINF2_MUX_DEBUG_7 SENINF 2 Debug Register 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A041D2C SENINF2_MUX_SPARE SENINF 2 spare Register 000E2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SENI NF_S PARE			
Type													RW			
Reset													1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENI NF_S PARE		SENI NF_F IFO_ FULL _SEL	SENI NF_V CNT_ SEL		SENINF_CR C_SEL										
Type	RW		RW	RW		RW										
Reset	0	0	1	0	0	0	0									

Bit(s)	Name	Description
19:14	SENINF_SPARE	**Spare register**
13	SENINF_FIFO_FULL_SEL	0: Does not send FIFO full to cam 1: Send FIFO full to cam
12:11	SENINF_VCNT_SEL	0: Vsync rising 1: Vsync rising d1 2: Vsync rising d2 3: Vsync rising d3
10:9	SENINF_CRC_SEL	0: Vsync rising 1: Vsync rising d1 2: Vsync rising d2 3: Vsync rising d3

1A041D30 SENINF2_MUX_DATA SENINF 2 Data Register 40000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA1															
Type	RO															
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_DATA1	
15:0	SENINF_DATA0	

1A041D34 SENINF2_MUX_DATA_CNT SENINF 2 Data Count Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENINF_DATA_CNT	

1A041D38 SENINF2_MUX_CROP — SENINF 2 Crop Size Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_CROP_X2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_CROP_X1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_CROP_X2	
15:0	SENINF_CROP_X1	

1A041D3C SENINF2_MUX_CTRL_EXT — SENINF 2 Control Register extend — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												SENINF_PIX_SEL_EXT			SENINF_SRC_SEL_EXT	
Type												RW			RW	
Reset												0			0	0

Bit(s)	Name	Description
4	SENINF_PIX_SEL_EXT	**SENINF output bus width:** {seninf_pixel_sel_ext, seninf_pixel_sel} 00: One pixel/cycle 01: Two pixels/cycle 10: four pixels/cycle
1:0	SENINF_SRC_SEL_EXT	**Selects SENINF input source:** {seninf_src_sel_ext, seninf_src_sel} 18: CSI2 VC0

Bit(s)	Name	Description
		19: CSI2 VC1 1A: CSI2 VC2 1B: CSI2 VC3 1C: CSI2 VC4 28: CSI3 VC0 29: CSI3 VC1 2A: CSI3 VC2 2B: CSI3 VC3 2C: CSI3 VC4

Module name: SENINF2_NCSI2 Base address: (+1a041700h)

Address	Name	Width	Register Function
1A041700	SENINF2_NCSI2_CTL	32	CSI2 Function Enable
1A041704	SENINF2_NCSI2_LNRC_TIMING	32	CSI2 Clock Lane Timing Parameters
1A041708	SENINF2_NCSI2_LNRD_TIMING	32	CSI2 data Lane Timing Parameters
1A04170C	SENINF2_NCSI2_DPCM	32	CSI2 DPCM Parameters
1A041710	SENINF2_NCSI2_INT_EN	32	CSI2 Interrupt Enable
1A041714	SENINF2_NCSI2_INT_STATUS	32	CSI2 Interrupt Status
1A041718	SENINF2_NCSI2_DGB_SEL	32	CSI2 Debug Selection
1A04171C	SENINF2_NCSI2_DBG_PORT	32	CSI2 Debug Port
1A041720	SENINF2_NCSI2_SPARE0	32	SPARE0
1A041724	SENINF2_NCSI2_SPARE1	32	SPARE1
1A041728	SENINF2_NCSI2_LNRC_FSM	32	CSI2 Clock Lane RX FSM
1A04172C	SENINF2_NCSI2_LNRD_FSM	32	CSI2 Data Lane RX FSM
1A041730	SENINF2_NCSI2_FRAME_LINE_NUM	32	CSI2 Frame/Line Number
1A041734	SENINF2_NCSI2_GENERIC_SHORT	32	CSI2 Generic Short Packet
1A041738	SENINF2_NCSI2_HSRX_DBG	32	CSI2 HSRX Enable
1A04173C	SENINF2_NCSI2_DI	32	CSI2 Data Interleaving Parameters
1A041740	SENINF2_NCSI2_HS_TRAIL	32	CSI2 HS Trail Timing Parameters
1A041744	SENINF2_NCSI2_DI_CTRL	32	CSI2 Data Interleaving Control
1A041748	SENINF2_NCSI2_DI_1	32	CSI2 Data Interleaving Parameters
1A04174C	SENINF2_NCSI2_DI_CTRL_1	32	CSI2 Data Interleaving Control
1A041750	SENINF2_NCSI2_DPHY_RESYNC_CT	32	CSI2 DPHY Lane Resync Control

Address	Name	Width	Register Function
	L		

1A041700 SENINF2_NCSI2_CTL **CSI2 Function Enable** **018861E0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			VS_OUT_CYCLE_NUMBER		CLOCK_HS_OPTION	REF_SYNC_DET_EN	HS_TRAIL_EN	ASYNC_FIFO_RST_SCH		SYNC_DET_BITSWAP_EN	SYNC_DET_EN	SYNC_DET_SCHEME	FLUSH_MODE			ED_SEL
Type			RW		RW	RW	RW	RW		RW	RW	RW	RW			RW
Reset			0	0	0	0	0	1	1	0	0	0	1	0		0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VS_TYPE	BYTE2PIXEL_EN	IMAGE_PACKET_EN	GENERIC_LONG_PACKET_EN			HS_END_EN	HS_PRPR_EN	HSRX_DET_EN	CRC_EN	ECC_EN	CLOCK_LANE_EN	DATA_LANE3_EN	DATA_LANE2_EN	DATA_LANE1_EN	DATA_LANE0_EN
Type	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	1	1	0			0	1	1	1	1	0	0	0	0	0

Bit(s)	Name	Description
29:28	VS_OUT_CYCLE_NUMBER	0: 4T 1: 8T
27	CLOCK_HS_OPTION	0: Enable clock lane HS based on LP11, LP01, LP00 1: Enable clock lane HS based on LP00
26	REF_SYNC_DET_EN	**Reference sync detect signal to do analog sync**
25	HS_TRAIL_EN	**Extends HS trail**
24:23	ASYNC_FIFO_RST_SCH	
22	SYNC_DET_BITSWAP_EN	
21	SYNC_DET_EN	**Enables sync sequence detection**
20	SYNC_DET_SCHEME	0: B8 1: 101110
19:18	FLUSH_MODE	0: Disable 1: Flush at first cycle of LP11 2: Flush at LP11 3: Reserved
16	ED_SEL	0: {WCH,WCL,DI} 1: {DI,WCL,WCH}
15	VS_TYPE	**VS type** 0: 4T 1: Frame start to frame end
14	BYTE2PIXEL_EN	**Byte 2 pixel conversion**
13	IMAGE_PACKET_EN	**Image data types**
12	GENERIC_LONG_PACKET_EN	**Generic long packet data types**
9	HS_END_EN	**Enables HS_EX reset at packet end**
8	HS_PRPR_EN	**Enables RX_HS_PRPR state**
7	HSRX_DET_EN	**Enables HSRX termination auto-detection flow**
6	CRC_EN	**Enables checksum**
5	ECC_EN	**Enables packet header ECC**
4	CLOCK_LANE_EN	**Enables clock lane**
3	DATA_LANE3_EN	**Enables data lane 3**
2	DATA_LANE2_EN	**Enables data lane 2**
1	DATA_LANE1_EN	**Enables data lane 1**
0	DATA_LANE0_EN	**Enables data lane 0**

Bit(s)	Name	Description

1A041704 SENINF2_NCSI2_LNRC_TIMING CSI2 Clock Lane Timing Parameters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SETTLE_PARAMETER								TERM_PARAMETER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	SETTLE_PARAMETER	TD_SETTLE parameter
7:0	TERM_PARAMETER	TD_TERM_EN parameter

1A041708 SENINF2_NCSI2_LNRD_TIMING CSI2 data Lane Timing Parameters 00002000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SETTLE_PARAMETER								TERM_PARAMETER							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	SETTLE_PARAMETER	TD_SETTLE parameter
7:0	TERM_PARAMETER	TD_TERM_EN parameter

1A04170C SENINF2_NCSI2_DPCM CSI2 DPCM Parameters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DI_2A_DPCM_EN	DI_37_DPCM_EN	DI_36_DPCM_EN	DI_35_DPCM_EN	DI_34_DPCM_EN	DI_33_DPCM_EN	DI_32_DPCM_EN	DI_31_DPCM_EN	DI_30_DPCM_EN				DPCM_MODE			
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW				RW			
Reset	0	0	0	0	0	0	0	0	0				0	0	0	0

Bit(s)	Name	Description
15	DI_2A_DPCM_EN	**Enables DPCM**
14	DI_37_DPCM_EN	**Enables DPCM**
13	DI_36_DPCM_EN	**Enables DPCM**
12	DI_35_DPCM_EN	**Enables DPCM**
11	DI_34_DPCM_EN	**Enables DPCM**
10	DI_33_DPCM_EN	**Enables DPCM**
9	DI_32_DPCM_EN	**Enables DPCM**
8	DI_31_DPCM_EN	**Enables DPCM**
7	DI_30_DPCM_EN	**Enables DPCM**
3:0	DPCM_MODE	0: 10-8-10

1A041710 SENINF2_NCSI2_INT_EN CSI2 Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_WCLR_EN					DPHY3_RESYNC_FIFO_OVERFLOW	DPHY2_RESYNC_FIFO_OVERFLOW	DPHY1_RESYNC_FIFO_OVERFLOW	DPHY0_RESYNC_FIFO_OVERFLOW	ERR_LANE_RESYNC	ERR_FRAME_SYNC_S5	ERR_FRAME_SYNC_S4	ERR_FRAME_SYNC_S3	ERR_FRAME_SYNC_S2	ERR_FRAME_SYNC_S1	ERR_FRAME_SYNC_S0
Type	RW					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0					0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GS	LS	FS	ERR_SOT_SYNC_HS_LNRD3	ERR_SOT_SYNC_HS_LNRD2	ERR_SOT_SYNC_HS_LNRD1	ERR_SOT_SYNC_HS_LNRD0	ERR_MULTI_LANE_SYNC	ERR_AFIFO	ERR_CRC	ERR_ECC_DOUBLE	ERR_ECC_CORRECTED	ERR_ECC_NO_ERROR	ERR_ID	ERR_FRAME_SYNC
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	INT_WCLR_EN	Enables interrupt write clear
26	DPHY3_RESYNC_FIFO_OVERFLOW	Enables LANE3_RESYNC_FIFO_OVERFLOW interrupt
25	DPHY2_RESYNC_FIFO_OVERFLOW	Enables LANE2_RESYNC_FIFO_OVERFLOW interrupt
24	DPHY1_RESYNC_FIFO_OVERFLOW	Enables LANE1_RESYNC_FIFO_OVERFLOW interrupt
23	DPHY0_RESYNC_FIFO_OVERFLOW	Enables LANE0_RESYNC_FIFO_OVERFLOW interrupt
22	ERR_LANE_RESYNC	Enables ERR_LANE_RESYNC interrupt
21	ERR_FRAME_SYNC_S5	Enables ERR_FRAME_SYNC interrupt
20	ERR_FRAME_SYNC_S4	Enables ERR_FRAME_SYNC interrupt
19	ERR_FRAME_SYNC_S3	Enables ERR_FRAME_SYNC interrupt
18	ERR_FRAME_SYNC_S2	Enables ERR_FRAME_SYNC interrupt
17	ERR_FRAME_SYNC_S1	Enables ERR_FRAME_SYNC interrupt
16	ERR_FRAME_SYNC_S0	Enables ERR_FRAME_SYNC interrupt
14	GS	Enables generic short packet interrupt
13	LS	Enables line start interrupt
12	FS	Enables frame start interrupt
11	ERR_SOT_SYNC_HS_LNRD3	Enables ERR_SOT_SYNC_HS interrupt
10	ERR_SOT_SYNC_HS_LNRD2	Enables ERR_SOT_SYNC_HS interrupt
9	ERR_SOT_SYNC_HS_LNRD1	Enables ERR_SOT_SYNC_HS interrupt
8	ERR_SOT_SYNC_HS_LNRD0	Enables ERR_SOT_SYNC_HS interrupt

Bit(s)	Name	Description
7	ERR_MULTI_LANE_SYNC	Enables ERR_MULTI_LANE_SYNC interrupt
6	ERR_AFIFO	Enables ERR_AFIFO interrupt
5	ERR_CRC	Enables ERR_CRC interrupt
4	ERR_ECC_DOUBLE	Enables ERR_ECC_DOUBLE interrupt
3	ERR_ECC_CORRECTED	Enables ERR_ECC_CORRECTED interrupt
2	ERR_ECC_NO_ERROR	ERR_ECC_NO_ERROR interrupt
1	ERR_ID	Enables ERR_ID interrupt
0	ERR_FRAME_SYNC	Enables ERR_FRAME_SYNC interrupt

1A041714 SENINF2_NCSI2_INT_STATUS CSI2 Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						DPHY3_RESYNC_FIFO_OVERFLOW_STA	DPHY2_RESYNC_FIFO_OVERFLOW_STA	DPHY1_RESYNC_FIFO_OVERFLOW_STA	DPHY0_RESYNC_FIFO_OVERFLOW_STA	ERR_LANE_RESYNC_STA	ERR_FRAME_SYNC_S5	ERR_FRAME_SYNC_S4	ERR_FRAME_SYNC_S3	ERR_FRAME_SYNC_S2	ERR_FRAME_SYNC_S1	ERR_FRAME_SYNC_S0
Type						RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GS	LS	FS	ERR_SOT_SYNC_HS_LNRD3	ERR_SOT_SYNC_HS_LNRD2	ERR_SOT_SYNC_HS_LNRD1	ERR_SOT_SYNC_HS_LNRD0	ERR_MULTI_LANE_SYNC	ERR_AFIFO	ERR_CRC	ERR_ECC_DOUBLE	ERR_ECC_CORRECTED	ERR_ECC_NO_ERROR	ERR_ID	ERR_FRAME_SYNC
Type		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26	DPHY3_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of DPHY lane3 is overflowed**
25	DPHY2_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of DPHY lane2 is overflowed**
24	DPHY1_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of DPHY lane1 is overflowed**
23	DPHY0_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of DPHY lane0 is overflowed**
22	ERR_LANE_RESYNC_STA	**Asserted when DPHY lane sync detect time is longer than set resync cycles**
21	ERR_FRAME_SYNC_S5	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
20	ERR_FRAME_SYNC_S4	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
19	ERR_FRAME_SYNC_S3	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
18	ERR_FRAME_SYNC_S2	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
17	ERR_FRAME_SYNC_S1	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
16	ERR_FRAME_SYNC_S0	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
14	GS	**Enables generic short packet interrupt**

Bit(s)	Name	Description
13	LS	**Line start interrupt**
12	FS	**Frame start interrupt**
11	ERR_SOT_SYNC_HS_LNRD3	**Asserted when proper synchronization cannot be expected**
10	ERR_SOT_SYNC_HS_LNRD2	**Asserted when proper synchronization cannot be expected**
9	ERR_SOT_SYNC_HS_LNRD1	**Asserted when proper synchronization cannot be expected**
8	ERR_SOT_SYNC_HS_LNRD0	**Asserted when proper synchronization cannot be expected**
7	ERR_MULTI_LANE_SYNC	**Asserted when multiple lane synchronization fails**
6	ERR_AFIFO	**Asserted when error occurs in asynchronous FIFO**
5	ERR_CRC	**Asserted when computed CRC code is different from received CRC code**
4	ERR_ECC_DOUBLE	**Asserted when an ECC syndrome is computed and two bit errors are detected in the received packet header**
3	ERR_ECC_CORRECTED	**Asserted when an ECC syndrome is computed and a single bit error in the packet header was detected and corrected**
2	ERR_ECC_NO_ERROR	**Asserted when an ECC syndrome is computed and the result is zero indicating a packet header that is considered to be without errors or has more than two bit errors** CSI-2's ECC mechanism cannot detect this type of error.
1	ERR_ID	**Asserted whean a packet header is decoded with an unrecognized or unimplemented data ID**
0	ERR_FRAME_SYNC	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**

1A041718 SENINF2_NCSI2_DGB_SEL CSI2 Debug Selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DEBUG_SEL							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DEBUG_SEL	Selects debug

1A04171C SENINF2_NCSI2_DBG_PORT CSI2 Debug Port 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CTL_DBG_PORT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	CTL_DBG_PORT	Debug port

1A041720 SENINF2_NCSI2_SPARE0 SPARE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE0	Spare register

1A041724 SENINF2_NCSI2_SPARE1 SPARE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE1	Spare register

1A041728 SENINF2_NCSI2_LNRC_FSM CSI2 Clock Lane RX FSM 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											LNRC_RX_FSM					
Type											RO					
Reset											0	0	0	0	0	1

Bit(s)	Name	Description
5:0	LNRC_RX_FSM	RX FSM of clock lane

1A04172C SENINF2_NCSI2_LNRD_FSM — CSI2 Data Lane RX FSM — 01010101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LNRD3_RX_FSM								LNRD2_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		LNRD1_RX_FSM								LNRD0_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1

Bit(s)	Name	Description
30:24	LNRD3_RX_FSM	RX FSM of data lane 3
22:16	LNRD2_RX_FSM	RX FSM of data lane 2
14:8	LNRD1_RX_FSM	RX FSM of data lane 1
6:0	LNRD0_RX_FSM	RX FSM of data lane 0

1A041730 SENINF2_NCSI2_FRAME_LINE_NUM — CSI2 Frame/Line Number — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LINE_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FRAME_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	LINE_NUM	Line number
15:0	FRAME_NUM	Frame number

1A041734 SENINF2_NCSI2_GENERIC_SHORT — CSI2 Generic Short Packet — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GENERIC_SHORT_PACKET_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											GENERIC_SHORT_PACKET_DT						

Type											RO					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
31:16	GENERIC_SHORT_PACKET_DATA	Generic short packet data
5:0	GENERIC_SHORT_PACKET_DT	Generic short packet data

1A041738 SENINF2_NCSI2_HSRX_DBG CSI2 HSRX Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLOCK_LANE_HSRX_EN	DATA_LANE3_HSRX_EN	DATA_LANE2_HSRX_EN	DATA_LANE1_HSRX_EN	DATA_LANE0_HSRX_EN
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	CLOCK_LANE_HSRX_EN	Enables clock lane HSRX circut
3	DATA_LANE3_HSRX_EN	Enables data lane 3 HSRX circuit
2	DATA_LANE2_HSRX_EN	Enables data lane 2 HSRX circuit
1	DATA_LANE1_HSRX_EN	Enables data lane 1 HSRX circuit
0	DATA_LANE0_HSRX_EN	Enables data lane 0 HSRX circuit

1A04173C SENINF2_NCSI2_DI CSI2 Data Interleaving Parameters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DT3						VC3		DT2						VC2	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DT1						VC1		DT0						VC0	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:26	DT3	Data type identifier
25:24	VC3	Virtual channel identifier
23:18	DT2	Data type identifier
17:16	VC2	Virtual channel identifier
15:10	DT1	Data type identifier
9:8	VC1	Virtual channel identifier
7:2	DT0	Data type identifier
1:0	VC0	Virtual channel identifier

1A041740 SENINF2_NCSI2_HS_TRAIL **CSI2 HS Trail Timing Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**HS_TRAIL_PARAMETER**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	HS_TRAIL_PARAMETER	HS trail parameter

1A041744 SENINF2_NCSI2_DI_CTRL **CSI2 Data Interleaving Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						**DT3_INTERLEAVING**		**VC3_INTERLEAVING**						**DT2_INTERLEAVING**		**VC2_INTERLEAVING**
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**DT1_INTERLEAVING**		**VC1_INTERLEAVING**						**DT0_INTERLEAVING**		**VC0_INTERLEAVING**
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0

Bit(s)	Name	Description
26:25	DT3_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
24	VC3_INTERLEAVING	**Virtual channel identifier interleaving**
18:17	DT2_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
16	VC2_INTERLEAVING	**Virtual channel identifier interleaving**
10:9	DT1_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
8	VC1_INTERLEAVING	**Virtual channel identifier interleaving**
2:1	DT0_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include

Bit(s)	Name	Description
		2: Exclude
0	VC0_INTERLEAVING	**Virtual channel identifier interleaving**

1A041748 SENINF2_NCSI2_DI_1 CSI2 Data Interleaving Parameters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DT5						VC5		DT4						VC4	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:10	DT5	Data type identifier
9:8	VC5	Virtual channel identifier
7:2	DT4	Data type identifier
1:0	VC4	Virtual channel identifier

1A04174C SENINF2_NCSI2_DI_CTRL_1 CSI2 Data Interleaving Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DT5_INTERLEAVING		VC5_INTERLEAVING						DT4_INTERLEAVING		VC4_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0

Bit(s)	Name	Description
10:9	DT5_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
8	VC5_INTERLEAVING	**Virtual channel identifier interleaving**
2:1	DT4_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
0	VC4_INTERLEAVING	**Virtual channel identifier interleaving**

1A041750 SENINF2_NC CSI2 DPHY Lane Resync 00000101

SI2_DPHY_RESYNC_CTL **Control**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DPHY_RESYNC_CNT								DPHY_RESYNC_FLUSH_EN	DPHY_RESYNC_DATAOUT_OPTION	DPHY_BYPASS_LANE_RESYNC
Type						RW								RW	RW	RW
Reset						0	0	1						0	0	1

Bit(s)	Name	Description
10:8	DPHY_RESYNC_CNT	Detect lane skew cycle count
2	DPHY_RESYNC_FLUSH_EN	Enables lane resync flush
1	DPHY_RESYNC_DATAOUT_OPTION	Data output option
0	DPHY_BYPASS_LANE_RESYNC	Bypass lane resync function

Module name: seninf2_ocsi2 Base address: (+1a041300h)

Address	Name	Width	Register Function
1A041360	SENINF2_OCSI2_CTRL	32	CSI2 Control Register
1A041364	SENINF2_OCSI2_DELAY	32	CSI2 Delay Control Register
1A041368	SENINF2_OCSI2_INTEN	32	CSI2 Interrupt Enable Register
1A04136C	SENINF2_OCSI2_INTSTA	32	CSI2 Interrupt Status Register
1A041370	SENINF2_OCSI2_ECCDBG	32	CSI2 ECC Debug Register
1A041374	SENINF2_OCSI2_CRCDBG	32	CSI2 CRC Debug Register
1A041378	SENINF2_OCSI2_DBG	32	CSI2 Debug Register
1A04137C	SENINF2_OCSI2_VER	32	CSI2 Version Code Register
1A041380	SENINF2_OCSI2_SHORT_INFO	32	CSI2 Short Packet Information Register
1A041384	SENINF2_OCSI2_LNFSM	32	CSI2 Lane FSM Register
1A041388	SENINF2_OCSI2_LNMUX	32	CSI2 Lane Mux Register
1A04138C	SENINF2_OCSI2_HSYNC_CNT	32	CSI2 Hsync Counter Register
1A041390	SENINF2_OCSI2_CAL	32	CSI2 Calibration Register
1A041394	SENINF2_OCSI2_DS	32	CSI2 Downsample Register

Address	Name	Width	Register Function
1A041398	SENINF2_OCSI2_VS	32	CSI2 Vsync Register
1A04139C	SENINF2_OCSI2_BIST	32	CSI2 BIST Register

1A041360 SENINF2_OCSI2_CTRL CSI2 Control Register 00002D80

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_BIST_CSI2_DATA_OK	CSI2_LANE_FSM_OK	CSI2_HS_FSM_OK	CSI2_BIST_DATA_OK	CSI2_BIST_START	CSI2_BIST_ERROR_COUNT								CSI2_DATA_FLOW		CSI2_ASYNC_OPTION
Type	RO	RO	RO	RO	RO	RO								RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_SYNC_CLR_EXTEND	CSI2_HSRXEN_PFOOT_CLR	CSI2_VSYNC_TYPE	CSI2_SW_RST	CSI2_SCLK4X_SEL	CSI2_SCLK_SEL	CSI2_ESC_EN	CSI2_SYNC_RST_EN	CSI2_LP11_RST_EN	CSI2_CLK_MISS_EN	CSI2_ED_SEL	CSI2_ECC_EN	DLANE3_EN	DLANE2_EN	DLANE1_EN	CSI2_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	1	0	1	1	0	1	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	CSI2_BIST_CSI2_DATA_OK	**CSI2 BIST CSI2 data ok**
30	CSI2_LANE_FSM_OK	**CSI2 BIST data lane FSM ok**
29	CSI2_HS_FSM_OK	**CSI2 BIST high speed FSM ok**
28	CSI2_BIST_DATA_OK	**CSI2 BIST DPHY data ok**
27	CSI2_BIST_START	**CSI2 BIST start status**
26:19	CSI2_BIST_ERROR_COUNT	**CSI2 bist test error count**
18:17	CSI2_DATA_FLOW	**CSI2 data flow** 0: Data packet 1: Generic long packet 2: All data packet
16	CSI2_ASYNC_OPTION	
15	CSI2_SYNC_CLR_EXTEND	
14	CSI2_HSRXEN_PFOOT_CLR	
13	CSI2_VSYNC_TYPE	**VSYNC type to CAM module** 0: High from short packet "frame start" to short packet "frame end" 1: 4T pulse after short packet "frame start"
12	CSI2_SW_RST	**CSI2 software reset, active high** 0: De-assert reset 1: Assert reset
11	CSI2_SCLK4X_SEL	**Selects CSI2 4x sample clock** 0: Invert 1: Does not invert csi2_clk from D-PHY
10	CSI2_SCLK_SEL	**Selects CSI2 sample clock** 0: Invert 1: Does not invert csi2_clk from D-PHY
9	CSI2_ESC_EN	**Enables CSI2 Escape mode**
8	CSI2_SYNC_RST_EN	**When this bit is set high, data high speed FSM will enter state "SYNC" whenever sync code is seen.**

Bit(s)	Name	Description
7	CSI2_LP11_RST_EN	Used in case packet ends unexpectedly. **When this bit is set high, data/clk lane FSM will enter state "STOP" whenever LP-11 is seen.** Used in case low power and high speed state transition is unexpected.
6	CSI2_CLK_MISS_EN	**Enables high speed mode clock miss monitoring**
5	CSI2_ED_SEL	**Selects CSI2 header format**
4	CSI2_ECC_EN	**Enables CSI2 ECC**
3	DLANE3_EN	**Enables CSI2 3 data lane**
2	DLANE2_EN	**Enables CSI2 2 data lane**
1	DLANE1_EN	**Enables CSI2 1 data lane**
0	CSI2_EN	**Enables CSI2 0 data lane**

1A041364 SENINF2_CSI2_DELAY **CSI2 Delay Control Register** **000A0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LP2HS_DATA_TERM_DELAY								LP2HS_DATA_SETTLE_DELAY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LP2HS_CLK_TERM_DELAY							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	LP2HS_DATA_TERM_DELAY	CSI2 data lane low power to high speed termination enable delay count
23:16	LP2HS_DATA_SETTLE_DELAY	CSI2 data lane low power to high speed sync code search delay
7:0	LP2HS_CLK_TERM_DELAY	CSI2 CLK lane low power to high speed termination enable delay count

1A041368 SENINF2_CSI2_INTEN **CSI2 Interrupt Enable Register** **00000007**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VCHANNEL_ID		CSI2_DATA_TYPE						CSI2_WC_NUMBER							
Type	RO		RO						RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_WC_NUMBER												CSI2_SYNC_NONSYNC_IRQ_EN	ECC_CORRECT_IRQ_EN	ECC_ERR_IRQ_EN	CRC_ERR_IRQ_EN
Type	RO												RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0					0	1	1	1

Bit(s)	Name	Description
31:30	VCHANNEL_ID	CSI2 virtual channel identifier corrected by error correction if ECC is on

Bit(s)	Name	Description
29:24	CSI2_DATA_TYPE	CSI2 long packet data type corrected by error correction if ECC is on
23:8	CSI2_WC_NUMBER	CSI2 long packet data size corrected by error correction if ECC is on
3	CSI2SYNC_NONSYNC_IRQ_EN	CSI2SYNC_NONSYNC_IRQ
2	ECC_CORRECT_IRQ_EN	Enables ECC correction interrupt
1	ECC_ERR_IRQ_EN	Enables ECC error interrupt
0	CRC_ERR_IRQ_EN	Enables CRC error interrupt

1A04136C SENINF2_OCSI2_INTSTA CSI2 Interrupt Status Register 00000070

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CSI2OUT_VSYNC	CSI2OUT_HSYNC				
Type											RO	RO				
Reset											0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CSI2_SPARE			CSI2_IRQ_CLR_SEL	CSI2SYNC_NONSYNC_IRQ	ECC_CORRECT_IRQ	ECC_ERR_IRQ	CRC_ERR_IRQ
Type									RW			RW	RO	RO	RO	RO
Reset									0	1	1	1	0	0	0	0

Bit(s)	Name	Description
21	CSI2OUT_VSYNC	**CSI2 vsync output to cam** Read only.
20	CSI2OUT_HSYNC	**CSI2 hsync output to cam** Read only.
7:5	CSI2_SPARE	**Spare register**
4	CSI2_IRQ_CLR_SEL	0: Read clear 1: Write clear
3	CSI2SYNC_NONSYNC_IRQ	**IRQ status bit to indicate that sync between different lanes is not sampled at the same time** Write clear.
2	ECC_CORRECT_IRQ	**ECC correction interrupt status**
1	ECC_ERR_IRQ	**ECC error interrupt status**
0	CRC_ERR_IRQ	**CRC error interrupt status**

1A041370 SENINF2_OCSI2_ECCDBG CSI2 ECC Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_ECCDB_BSEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_ECCDB_BSEL															CSI2_ECCDB_EN
Type	RW															RW

Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CSI2_ECCDB_BSEL	**Selects CSI2 packet header error generation bit** To generate packet header error, set one of the 24 bits to 1. Because there is only one bit error can be corrected, only one bit of the 24 bits can be 1.
0	CSI2_ECCDB_EN	**Enables CSI2 packet header error generation**

1A041374 SENINF2_OCSI2_CRCDBG CSI2 CRC Debug Register 0000000E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_CRCDB_BSEL								CSI2_CRCDB_WSEL							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_CRCDB_WSEL								CSI2_SPARE							CSI2_CRCDB_EN
Type	RW								RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Bit(s)	Name	Description
31:24	CSI2_CRCDB_BSEL	**Selects CSI2 data error generation bit** Set to 1 to generate selected word bit error. Note: Only word number selected by csi2_crcdb_wsel will be put error on it.
23:8	CSI2_CRCDB_WSEL	**Selects CSI2 data error generation data word**
7:1	CSI2_SPARE	**Spare register**
0	CSI2_CRCDB_EN	**Enables CSI2 data error generation**

1A041378 SENINF2_OCSI2_DBG CSI2 Debug Register 00040820

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LN3_HSRXDB_EN	LN2_HSRXDB_EN	LN1_HSRXDB_EN	LN0_HSRXDB_EN	LNC_HSRXDB_EN	LN3_LPRXDB_EN	LN2_LPRXDB_EN	LN1_LPRXDB_EN	LN0_LPRXDB_EN	LNC_LPRXDB_EN		VCHANNEL_ID_EN	VCHANNEL1_ID		VCHANNEL0_ID	
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0		0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_CLK_LANE_CS					CSI2_DATA_HS_CS						CSI2_DBG_SRC_SEL				CSI2_DEBUG_ON
Type	RO					RO						RW				RW
Reset	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31	LN3_HSRXDB_EN	**Enables data lane 1 termination directly** For test only.
30	LN2_HSRXDB_EN	**Enables data lane 0 termination directly**

Bit(s)	Name	Description
		For test only.
29	LN1_HSRXDB_EN	**Enables data lane 1 termination directly** For test only.
28	LN0_HSRXDB_EN	**Enables data lane 0 termination directly** For test only.
27	LNC_HSRXDB_EN	**Enables clock lane termination directly** For test only.
26	LN3_LPRXDB_EN	**Enables data lane 3 low power mode directly** For test only.
25	LN2_LPRXDB_EN	**Enables data lane 2 low power mode directly** For test only.
24	LN1_LPRXDB_EN	**Enables data lane 1 low power mode directly** For test only.
23	LN0_LPRXDB_EN	**Enables data lane 0 low power mode directly** For test only.
22	LNC_LPRXDB_EN	**Enables clock lane low power mode directly** For test only.
20	VCHANNEL_ID_EN	**Enables virtual channel**
19:18	VCHANNEL1_ID	**Virtual channel 1 ID**
17:16	VCHANNEL0_ID	**Virtual channel 0 ID**
15:11	CSI2_CLK_LANE_CS	**Clock lane FSM current state** 1: IDLE 2: STOP 4: HS_REQ 8: HS_PREP 16: HS_RX
10:5	CSI2_DATA_HS_CS	**Data high speed state** 1: IDLE 2: SYNC 4: PHEAD 8: PECC 16: PDATA 32: PFOOT
4:1	CSI2_DBG_SRC_SEL	**Selects CSI2 Debug port source**
0	CSI2_DEBUG_ON	**Enables CSI2 debug** When CSI2 debug is enabled, CSI2 output raw data will include header to cam. *Note: To output CSI2 debug data,* *1. Set cam to JPEG interface mode ((CAM + 0024)[14], JPGINF_EN:1).* *2. Set up Vsync polarity ((CAM + 0010)[7], VSPOL:1).* *3. Set up output type raw data output ((CAM + 0024)[21:20] OUTPATH_TYPE:0).* *4. Set up raw data type to 8-bit mode ((CAM + 0024)[24] OUTPATH_TYPE:0).* *5. Enable ISP data output to memory ((CAM + 0024)[16],OUT_PATH_EN:1).*

1A04137C SENINF2_OCSI2_VER CSI2 Version Code Register 20110815

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	YEAR															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MONTH								DATE							

Type	RO								RO							
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	1

Bit(s)	Name	Description
31:16	YEAR	Year code
15:8	MONTH	Month code
7:0	DATE	Date code

1A041380 SENINF2_OCSI2_SHORT_INFO CSI2 Short Packet Information Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_FRAME_NO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_LINE_NO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	CSI2_FRAME_NO	Frame number information in short packet data type
15:0	CSI2_LINE_NO	Line number information in short packet data type

1A041384 SENINF2_OCSI2_LNFSM CSI2 Lane FSM Register 01010101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CSI2_DATA_LN3_CS								CSI2_DATA_LN2_CS						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CSI2_DATA_LN1_CS								CSI2_DATA_LN0_CS						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1

Bit(s)	Name	Description
30:24	CSI2_DATA_LN3_CS	**Data lane 3 FSM current state**
22:16	CSI2_DATA_LN2_CS	**Data lane 2 FSM current state**
14:8	CSI2_DATA_LN1_CS	**Data lane 1 FSM current state**
6:0	CSI2_DATA_LN0_CS	**Data lane 0 FSM current state** 1: IDLE 2: STOP 4: HS_REQ 8: HS_PREP 16: HS_TERM 32: HS_RX 64: HS_ESC

1A041388 SENINF2_OCSI2_LNMUX CSI2 Lane Mux Register 000000E4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CSI2_DATA_LN3_MUX		CSI2_DATA_LN2_MUX		CSI2_DATA_LN1_MUX		CSI2_DATA_LN0_MUX	
Type									RW		RW		RW		RW	
Reset									1	1	1	0	0	1	0	0

Bit(s)	Name	Description
7:6	CSI2_DATA_LN3_MUX	**CSI2 data lane mux** 0: LANE 0 1: LANE 1 2: LANE 2 3: LANE 3
5:4	CSI2_DATA_LN2_MUX	**CSI2 data lane mux** 0: LANE 0 1: LANE 1 2: LANE 2 3: LANE 3
3:2	CSI2_DATA_LN1_MUX	**CSI2 data lane mux** 0: LANE 0 1: LANE 1 2: LANE 2 3: LANE 3
1:0	CSI2_DATA_LN0_MUX	**CSI2 data lane mux** 0: LANE 0 1: LANE 1 2: LANE 2 3: LANE 3

1A04138C SENINF2_OCSI2_HSYNC_CNT CSI2 Hsync Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CSI2_HSYNC_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	CSI2_HSYNC_CNT	CSI2 hsync counter

1A041390 SENINF2_OC CSI2 Calibration Register 01010000

SI2_CAL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2 _CAL _CNT _2								CSI2_CAL_CNT_1							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										CSI2_CAL_STAT E						CSI2 _CAL _EN
Type										RO						RW
Reset										0	0	0				0

Bit(s)	Name	Description
31:24	CSI2_CAL_CNT_2	**CSI2 calibration counter 2 (term enable to sync)** Settle delay <= CSI2 Calibration Counter 2 - Term Delay - 3 byte clk - 3 bclk - 1 bclk
23:16	CSI2_CAL_CNT_1	**CSI2 calibration counter 1 (term enable to HS00)** Term delay <= CSI2 Calibration Counter 1 - 2 byte clk - 3 bclk
6:4	CSI2_CAL_STATE	**CSI2 calibration current state**
0	CSI2_CAL_EN	**Enables CSI2 calibration**

1A041394 SENINF2_OC SI2_DS CSI2 Downsample Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CSI2_DS_C TRL		CSI2 _DS_ EN
Type														RW		RW
Reset														0	0	0

Bit(s)	Name	Description
2:1	CSI2_DS_CTRL	**Controls CSI2 downsample factor** 0: 1 1: 1/2 2: 1/4 3: 1/8
0	CSI2_DS_EN	**Enables CSI2 downsample**

1A041398 SENINF2_OC SI2_VS CSI2 Vsync Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CSI2_VS_C TRL	

Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	CSI2_VS_CTRL	**Extends CSI2 vsync period** 0: 4T 1: 8T 2: 12T 3: 16T

1A04139C SENINF2_OCSI2_BIST **CSI2 BIST Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CSI2_BIST_LNR3_DATA_OK	CSI2_BIST_LNR2_DATA_OK	CSI2_BIST_LNR1_DATA_OK	CSI2_BIST_LNR0_DATA_OK
Type													RO	RO	RO	RO
Reset													0	0	0	0

Bit(s)	Name	Description
3	CSI2_BIST_LNR3_DATA_OK	CSI2 BIST Lane 3 DPHY data ok
2	CSI2_BIST_LNR2_DATA_OK	CSI2 BIST Lane 2 DPHY data ok
1	CSI2_BIST_LNR1_DATA_OK	CSI2 BIST Lane 1 DPHY data ok
0	CSI2_BIST_LNR0_DATA_OK	CSI2 BIST Lane 0 DPHY data ok

Module name: SENINF2_TG Base address: (+1a041600h)

Address	Name	Width	Register Function
1A041600	SENINF_TG2_PH_CNT	32	TG Phase Counter
1A041604	SENINF_TG2_SEN_CK	32	TG Sensor Clock Divider
1A041608	SENINF_TG2_TM_CTL	32	TM Control
1A04160C	SENINF_TG2_TM_SIZE	32	TM Size
1A041610	SENINF_TG2_TM_CLK	32	TM Clock
1A041614	SENINF_TG2_TM_STP	32	TG1_TM_STP

1A041600 SENINF_TG2_PH_CNT **TG Phase Counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PCEN		ADCLK_EN	CLKPOL												
Type	RW		RW	RW												
Reset	0		0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CAM_PCLK_INV	PAD_PCLK_INV	EXT_PWRDN	EXT_RST		CLKFL_POL	TGCLK_SEL	
Type									RW	RW	RW	RW		RW	RW	
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
31	PCEN	**TG phase counter enable control**
29	ADCLK_EN	**Enables sensor master clock (mclk) output to sensor**
28	CLKPOL	**Controls sensor master clock polarity**
7	CAM_PCLK_INV	**Inverts pixel clock in CAM**
6	PAD_PCLK_INV	**Inverts pixel clock in PAD side**
5	EXT_PWRDN	**Powers down sensor**
4	EXT_RST	**Resets sensor**
2	CLKFL_POL	**Sensor clock falling edge polarity**
1:0	TGCLK_SEL	**Selects sensor master clock** 0: isp_clk 1: cam_pll 2: 3rd clock source

1A041604 SENINF_TG2_SEN_CK TG Sensor Clock Divider 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CLKCNT					
Type											RW					
Reset											0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			CLKRS								CLKFL					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	1

Bit(s)	Name	Description
21:16	CLKCNT	**Controls sensor master clock frequency divider** Sensor master clock = ISP_clock/(CLKCNT+1); CLKCNT >=1
13:8	CLKRS	**Controls sensor master clock rising edge**
5:0	CLKFL	**Controls sensor master clock falling edge**

1A041608 SENINF_TG2_TM_CTL TM Control 00300004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									TM_DUMMYPXL							
Type									RW							
Reset									0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TM_VSYNC								TM_PAT					TM_F	TM_R	TM_E

														MT	ST	N
Type	RW								RW					RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0		1	0	0

Bit(s)	Name	Description
23:16	TM_DUMMYPXL	**Test model horizontal dummy pixel**
15:8	TM_VSYNC	**VSYNC high duration in line unit (TM_DUMMYPXL + PIXEL)**
7:4	TM_PAT	**Test model decision** 0: White 1: Yellow 2: Cyan 3: Green 4: Magenta 5: Red 6: Blue 7: Black 8: Horizontal gray level (Unit 1) 9: Horizontal gray level (Unit 4) 10: Horizontal gray level (take 1024 pixel as one period) (only bayer) 11: Vertical gray level (Unit 1) 12: Static horizontal color bar 13: Static vertical color bar (only bayer) 14: R,G,B,W flashes every two frames (only bayer) 15: Dynamic horizontal colorbar (only bayer)
2	TM_FMT	**Test model format** 0: Bayer 1: YUV
1	TM_RST	**Test model reset** 1'b0: Does not reset test model 1'b1: Reset test model
0	TM_EN	**Enables test model** 0: Disable 1: Enable

1A04160C SENINF_TG2_TM_SIZE **TM Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			TM_LINE													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TM_PXL												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	TM_LINE	Test model line number
12:0	TM_PXL	Test model pixel number (HSYNC high duration in pixel unit)

1A041610 SENINF_TG2_TM_CLK TM Clock 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		TM_CLRBAR_IDX					TM_CLRBAR_OFT									
Type		RW					RW									
Reset		0	0	0			0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TM_CLK_CNT			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
30:28	TM_CLRBAR_IDX	**Test model colorbar index offset** 0: White 1: Yellow 2: Cyan 3: Green 4: Magenta 5: Rred 6: Blue 7: Black
25:16	TM_CLRBAR_OFT	**Test model colorbar offset** This value should be smaller than (TM_PXL>>3).
3:0	TM_CLK_CNT	**Test model clock divided count**

1A041614 SENINF_TG2_TM_STP TG1_TM_STP 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TG1_TM_STP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TG1_TM_STP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TG1_TM_STP	Time stamp divider

Module name: seninf3 Base address: (+1a042200h)

Address	Name	Width	Register Function
1A042200	SENINF3_CTRL	32	SENINF 3 Control Register
1A042204	SENINF3_CTRL_EXT	32	SENINF 3 Control Register Extend
1A042208	SENINF3_ASYNC_CTRL	32	SENINF 3 Async Control Register

1A042200 SENINF3_CTRL **SENINF 3 Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PAD2CAM_DATA_SEL							SENINF_DEBUG_SEL							
Type		RW							RW							
Reset		0	0	0					0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_SRC_SEL							CSI3_SW_RST	CSI2_SW_RST	SCAM_SW_RST	TEST_MODEL_SW_RST	CKGEN_SW_RST	CCIR_SW_RST	OCSI2_SW_RST	NCSI2_SW_RST	SENINF_EN
Type	RW							RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:28	PAD2CAM_DATA_SEL	0: PAD2CAM_DATA[9:0] 3: {PAD2CAM_DATA[7:0],2'b00} 4: {PAD2CAM_DATA[9:2]2'b00}
23:20	SENINF_DEBUG_SEL	**Selects SENINF1 debug**
15:12	SENINF_SRC_SEL	**Selects SENINF input source** 0: CSI2 1: Test model 2: CCIR656 3: Parallel sensor 4: Serial sensor 8: NCSI2
8	CSI3_SW_RST	**CSI3 software reset, active high** 0: De-assert reset 1: Assert reset
7	CSI2_SW_RST	**CSI2 software reset, active high** 0: De-assert reset 1: Assert reset
6	SCAM_SW_RST	**SCAM software reset, active high** 0: De-assert reset 1: Assert reset
5	TEST_MODEL_SW_RST	**Test model software reset, active high** 0: De-assert reset 1: Assert reset
4	CKGEN_SW_RST	**CKGEN software reset, active high** 0: De-assert reset 1: Assert reset
3	CCIR_SW_RST	**CCIR software reset, active high** 0: De-assert reset 1: Assert reset
2	OCSI2_SW_RST	**OCSI2 software reset, active high** 0: De-assert reset 1: Assert reset
1	NCSI2_SW_RST	**NCSI2 software reset, active high** 0: De-assert reset 1: Assert reset
0	SENINF_EN	

1A042204 SENINF3_CT **SENINF 3 Control Register** **00000000**

RL_EXT **Extend**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															SENINF_SRC_SEL_EXT	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SENINF_CSI3_IP_EN	SENINF_CSI2_IP_EN	SENINF_NCSI2_IP_EN	SENINF_SCAM_IP_EN			SENINF_TESTMDL_IP_EN	SENINF_OCSI2_IP_EN
Type									RW	RW	RW	RW			RW	RW
Reset									0	0	0	0			0	0

Bit(s)	Name	Description
17:16	SENINF_SRC_SEL_EXT	[0] Set 1'b1 for CSI2 [1] Set 1'b1 for CSI3 For constraints only.
7	SENINF_CSI3_IP_EN	Enables CSI3 IP
6	SENINF_CSI2_IP_EN	Enables CSI2 IP
5	SENINF_NCSI2_IP_EN	Enables NCSI2 IP
4	SENINF_SCAM_IP_EN	Enables SCAM IP
1	SENINF_TESTMDL_IP_EN	Enables TESTMDL IP
0	SENINF_OCSI2_IP_EN	Enables OCSI2 IP

1A042208 SENINF3_ASYNC_CTRL **SENINF 3 Async Control Register** **1B1F0002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			FIFO_FLUSH_EN								FIFO_PUSH_EN					
Type			RW								RW					
Reset			0	1	1	0	1	1			0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SENINF_HSYNC_POL	SENINF_VSYNC_POL	SENINF_HSYNC_MASK	SENINF_ASYNC_FIFO_RST
Type													RW	RW	RW	RW
Reset													0	0	1	0

Bit(s)	Name	Description
29:24	FIFO_FLUSH_EN	**Normal mode: 6'b011011** JPEG two pixel mode: 6'b011000
21:16	FIFO_PUSH_EN	**Normal mode: 6'b011111** JPEG two pixel mode: 6'b011110
3	SENINF_HSYNC_POL	**SENINF HSYNC polarity**
2	SENINF_VSYNC_POL	**SENINF VSYNC polarity**
1	SENINF_HSYNC_MASK	**Masks hsync** 0: Send hsync when vsync = 1 1: Does not send hsync when vsync = 1
0	SENINF_ASYNC_FIFO_RST	**Async FIFO software reset**

Module name: seninf3_csi2 Base address: (+1a042a00h)

Address	Name	Width	Register Function
1A042A00	SENINF3_CSI2_CTL	32	CSI2 Function Enable
1A042A04	SENINF3_CSI2_LNRC_TIMING	32	CSI2 Clock Lane Timing Parameters
1A042A08	SENINF3_CSI2_LNRD_TIMING	32	CSI2 Data Lane Timing Parameters
1A042A0C	SENINF3_CSI2_DPCM	32	CSI2 DPCM Parameters
1A042A10	SENINF3_CSI2_INT_EN	32	CSI2 Interrupt Enable
1A042A14	SENINF3_CSI2_INT_STATUS	32	CSI2 Interrupt Status
1A042A18	SENINF3_CSI2_DGB_SEL	32	CSI2 Debug Selection
1A042A1C	SENINF3_CSI2_DBG_PORT	32	CSI2 Debug Port
1A042A20	SENINF3_CSI2_SPARE0	32	SPARE0
1A042A24	SENINF3_CSI2_SPARE1	32	SPARE1
1A042A28	SENINF3_CSI2_LNRC_FSM	32	CSI2 Clock Lane RX FSM
1A042A2C	SENINF3_CSI2_LNRD_FSM	32	CSI2 Data Lane RX FSM
1A042A30	SENINF3_CSI2_FRAME_LINE_NUM	32	CSI2 Frame/Line Number
1A042A34	SENINF3_CSI2_GENERIC_SHORT	32	CSI2 Generic Short Packet
1A042A38	SENINF3_CSI2_HSRX_DBG	32	CSI2 HSRX Enable
1A042A3C	SENINF3_CSI2_DI	32	CSI2 Data Interleaving Parameters
1A042A40	SENINF3_CSI2_HS_TRAIL	32	CSI2 HS Trail Timing Parameters
1A042A44	SENINF3_CSI2_DI_CTRL	32	CSI2 Data Interleaving Control
1A042A48	SENINF3_CSI2_LNRD_FSM_X	32	CSI2 Data Lane RX FSM Other
1A042A4C	SENINF3_CSI2_DETECT_CON1	32	CSI2 CPHY Detect Control sync
1A042A50	SENINF3_CSI2_DETECT_CON2	32	CSI2 CPHY Detect Control Escape
1A042A54	SENINF3_CSI2_DETECT_CON3	32	CSI2 CPHY Detect Control Post
1A042A58	SENINF3_CSI2_RLR0_CON0	32	CSI2 CPHY RLR0 CON0
1A042A5C	SENINF3_CSI2_RLR1_CON0	32	CSI2 CPHY RLR1 CON0
1A042A60	SENINF3_CSI2_RLR2_CON0	32	CSI2 CPHY RLR2 CON0
1A042A64	SENINF3_CSI2_RLR_CON0	32	CSI2 CPHY RLR CON0
1A042A68	SENINF3_CSI2_MUX_CON	32	CSI2 Pin Pux Sel

Address	Name	Width	Register Function
1A042A6C	SENINF3_CSI2_DETECT_DBG0	32	CSI2 Detection Debug 0
1A042A70	SENINF3_CSI2_DETECT_DBG1	32	CSI2 Detection Debug 1
1A042A74	SENINF3_CSI2_RESYNC_MERGE_CTL	32	CSI2 Lane Resync Merge Control
1A042A78	SENINF3_CSI2_CTRL_TRIO_MUX	32	CSI2 Control Trio Mux
1A042A7C	SENINF3_CSI2_CTRL_TRIO_CON	32	CSI2 Control Trio Config
1A042A80	SENINF3_FIX_ADDR_CPHY0_DBG	32	cphy_fix_point_addr_cphy0_debug
1A042A84	SENINF3_FIX_ADDR_CPHY1_DBG	32	cphy_fix_point_addr_cphy1_debug
1A042A88	SENINF3_FIX_ADDR_CPHY2_DBG	32	cphy_fix_point_addr_cphy2_debug
1A042A8C	SENINF3_FIX_ADDR_DBG	32	cphy_fix_point_addr_debug
1A042A90	SENINF3_WIRE_STATE_DECODE_CPHY0_DBG0	32	cphy_wire_state_decode_cphy0_debug0
1A042A94	SENINF3_WIRE_STATE_DECODE_CPHY0_DBG1	32	cphy_wire_state_decode_cphy0_debug1
1A042A98	SENINF3_WIRE_STATE_DECODE_CPHY1_DBG0	32	cphy_wire_state_decode_cphy1_debug0
1A042A9C	SENINF3_WIRE_STATE_DECODE_CPHY1_DBG1	32	cphy_wire_state_decode_cphy1_debug1
1A042AA0	SENINF3_WIRE_STATE_DECODE_CPHY2_DBG0	32	cphy_wire_state_decode_cphy2_debug0
1A042AA4	SENINF3_WIRE_STATE_DECODE_CPHY2_DBG1	32	cphy_wire_state_decode_cphy2_debug1
1A042AA8	SENINF3_SYNC_RESYNC_CTL	32	CSI2 Sync Resync Control
1A042AAC	SENINF3_POST_DETECT_CTL	32	CSI2 Post Detect Control
1A042AB0	SENINF3_WIRE_STATE_DECODE_CONFIG	32	CSI2 Wire State Decode Config
1A042AB4	SENINF3_CSI2_CPHY_LNRD_FSM	32	CPHY Data Lane RX FSM
1A042AB8	SENINF3_FIX_ADDR_CPHY0_DBG0	32	cphy_fix_point_addr_cphy0_debug0
1A042ABC	SENINF3_FIX_ADDR_CPHY0_DBG1	32	cphy_fix_point_addr_cphy0_debug1
1A042AC0	SENINF3_FIX_ADDR_CPHY0_DBG2	32	cphy_fix_point_addr_cphy0_debug2
1A042AC4	SENINF3_FIX_ADDR_CPHY1_DBG0	32	cphy_fix_point_addr_cphy1_debug0
1A042AC8	SENINF3_FIX_AD	32	cphy_fix_point_addr_cphy1_debug1

Address	Name	Width	Register Function
	DR_CPHY1_DBG1		
1A042ACC	SENINF3_FIX_ADDR_CPHY1_DBG2	32	cphy_fix_point_addr_cphy1_debug2
1A042AD0	SENINF3_FIX_ADDR_CPHY2_DBG0	32	cphy_fix_point_addr_cphy2_debug0
1A042AD4	SENINF3_FIX_ADDR_CPHY2_DBG1	32	cphy_fix_point_addr_cphy2_debug1
1A042AD8	SENINF3_FIX_ADDR_CPHY2_DBG2	32	cphy_fix_point_addr_cphy2_debug2
1A042ADC	SENINF3_FIX_ADDR_DBG0	32	cphy_fix_point_addr_debug0
1A042AE0	SENINF3_FIX_ADDR_DBG1	32	cphy_fix_point_addr_debug1
1A042AE4	SENINF3_FIX_ADDR_DBG2	32	cphy_fix_point_addr_debug2
1A042AE8	SENINF3_CSI2_MODE	32	CSI2 Packet Structure
1A042AF0	SENINF3_CSI2_DI_EXT	32	CSI2 Data Interleaving Parameters Extend
1A042AF4	SENINF3_CSI2_DI_CTRL_EXT	32	CSI2 Data Interleaving Control Extend
1A042AF8	SENINF3_CSI2_CPHY_LOOPBACK	32	CSI2 SW Trigger sync_init and hs_en
1A042B00	SENINF3_CSI2_PROGSEQ_0	32	CSI2 CPHY Program sequence_0
1A042B04	SENINF3_CSI2_PROGSEQ_1	32	CSI2 CPHY Program sequence_1
1A042B10	SENINF3_CSI2_INT_EN_EXT	32	CSI2 Interrupt Enable Extend
1A042B14	SENINF3_CSI2_INT_STATUS_EXT	32	CSI2 Interrupt Status Extend
1A042B18	SENINF3_CSI2_CPHY_FIX_POINT_RST	32	CSI2 CPHY Fix Point Reset Mode
1A042B20	SENINF3_CSI2_DPHY_RESYNC_CTL	32	CSI2 DPHY Lane Resync Control

1A042A00 SENINF3_CSI2_CTL **CSI2 Function Enable** **01886160**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA_LANE7_EN	DATA_LANE6_EN	VS_OUT_CYCLE_NUMBER		CLOCK_HS_OPTION	REF_SYNC_DET_EN	HS_TRAIL_EN	ASYNC_FIFO_RST_SCH		SYNC_DET_BIT_SWAP_EN	SYNC_DET_EN	SYNC_DET_SCHEME	FLUSH_MODE			ED_SEL
Type	RW	RW	RW		RW	RW	RW	RW		RW	RW	RW	RW			RW
Reset	0	0	0	0	0	0	0	1	1	0	0	0	1	0		0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VS_TYPE	BYTE2PIXEL_EN	IMAGE_PACKET_EN	GENERIC_LONG_PACKET_	DATA_LANE5_EN	DATA_LANE4_EN	HS_END_EN	HS_PRPR_EN	HSRX_DET_EN	CRC_EN	ECC_EN	CLOCK_LANE_EN	DATA_LANE3_EN	DATA_LANE2_EN	DATA_LANE1_EN	DATA_LANE0_EN

				EN												
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	1	1	0	0	0	0	1	0	1	1	0	0	0	0	0

Bit(s)	Name	Description
31	DATA_LANE7_EN	**Enables data lane 7**
30	DATA_LANE6_EN	**Enables data lane 6**
29:28	VS_OUT_CYCLE_NUMBER	0: 4T 1: 8T
27	CLOCK_HS_OPTION	0: Enable clock lane HS based on LP11, LP01, LP00 1: Enable clock lane HS based on LP00
26	REF_SYNC_DET_EN	**Reference sync detect signal to do analog sync**
25	HS_TRAIL_EN	**Extends HS trail**
24:23	ASYNC_FIFO_RST_SCH	
22	SYNC_DET_BITSWAP_EN	
21	SYNC_DET_EN	**Enables sync sequence detection**
20	SYNC_DET_SCHEME	0: B8 1: 101110
19:18	FLUSH_MODE	0: Disable 1: Flush at first cycle of LP11 2: Flush at LP11 3: Reserved
16	ED_SEL	0: {WCH,WCL,DI} 1: {DI,WCL,WCH}
15	VS_TYPE	**VS type** 0: 4T 1: Frame start to frame end
14	BYTE2PIXEL_EN	**Byte 2 pixel conversion**
13	IMAGE_PACKET_EN	**Image data types**
12	GENERIC_LONG_PACKET_EN	**Generic long packet data types**
11	DATA_LANE5_EN	**Enables data lane 6**
10	DATA_LANE4_EN	**Enables data lane 5**
9	HS_END_EN	**Enables HS_EX reset at packet end**
8	HS_PRPR_EN	**Enables RX_HS_PRPR state**
7	HSRX_DET_EN	**Enables HSRX termination auto-detection flow**
6	CRC_EN	**Enables checksum**
5	ECC_EN	**Enables packet header ECC**
4	CLOCK_LANE_EN	**Enables clock lane**
3	DATA_LANE3_EN	**Enables data lane 3**
2	DATA_LANE2_EN	**Enables data lane 2**
1	DATA_LANE1_EN	**Enables data lane 1**
0	DATA_LANE0_EN	**Enables data lane 0**

1A042A04 SENINF3_CSI2_LNRC_TIMING **CSI2 Clock Lane Timing Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLOCK_SETTLE_PARAMETER								CLOCK_TERM_PARAMETER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	CLOCK_SETTLE_PARAMETER	TD_SETTLE parameter
7:0	CLOCK_TERM_PARAMETER	TD_TERM_EN parameter

1A042A08 SENINF3_CSI2_LNRD_TIMING **CSI2 Data Lane Timing Parameters** **00002000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_SETTLE_PARAMETER								DATA_TERM_PARAMETER							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	DATA_SETTLE_PARAMETER	TD_SETTLE parameter
7:0	DATA_TERM_PARAMETER	TD_TERM_EN parameter

1A042A0C SENINF3_CSI2_DPCM **CSI2 DPCM Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DI_2A_DPCM_EN	DI_37_DPCM_EN	DI_36_DPCM_EN	DI_35_DPCM_EN	DI_34_DPCM_EN	DI_33_DPCM_EN	DI_32_DPCM_EN	DI_31_DPCM_EN	DI_30_DPCM_EN				DPCM_MODE			
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW				RW			
Reset	0	0	0	0	0	0	0	0	0				0	0	0	0

Bit(s)	Name	Description
15	DI_2A_DPCM_EN	**Enables DPCM**
14	DI_37_DPCM_EN	**Enables DPCM**
13	DI_36_DPCM_EN	**Enables DPCM**
12	DI_35_DPCM_EN	**Enables DPCM**
11	DI_34_DPCM_EN	**Enables DPCM**
10	DI_33_DPCM_EN	**Enables DPCM**
9	DI_32_DPCM_EN	**Enables DPCM**
8	DI_31_DPCM_EN	**Enables DPCM**
7	DI_30_DPCM_EN	**Enables DPCM**
3:0	DPCM_MODE	0: 10-8-10

1A042A10 SENINF3_CSI2_INT_EN **CSI2 Interrupt Enable** **1FFFBFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	INT_WCLR_EN			TRIO2_ESCAPE_CODE_DETECT	TRIO1_ESCAPE_CODE_DETECT	TRIO0_ESCAPE_CODE_DETECT	TRIO2_RESYNC_FIFO_OVERFLOW	TRIO1_RESYNC_FIFO_OVERFLOW	TRIO0_RESYNC_FIFO_OVERFLOW	ERR_LANE_RESYNC	ERR_FRAME_SYNC_S5	ERR_FRAME_SYNC_S4	ERR_FRAME_SYNC_S3	ERR_FRAME_SYNC_S2	ERR_FRAME_SYNC_S1	ERR_FRAME_SYNC_S0
Type	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0			1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FE	GS	LS	FS	ERR_SOT_SYNC_HS_LNRD3	ERR_SOT_SYNC_HS_LNRD2	ERR_SOT_SYNC_HS_LNRD1	ERR_SOT_SYNC_HS_LNRD0	ERR_MULTI_LANE_SYNC	ERR_AFIFO	ERR_CRC	ERR_ECC_DOUBLE	ERR_ECC_CORRECTED	ERR_ECC_NO_ERROR	ERR_ID	ERR_FRAME_SYNC
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	INT_WCLR_EN	Enables interrupt write clear
28	TRIO2_ESCAPE_CODE_DETECT	Enables TRIO2_ESCAPE_CODE_DETECT interrupt
27	TRIO1_ESCAPE_CODE_DETECT	Enables TRIO1_ESCAPE_CODE_DETECT interrupt
26	TRIO0_ESCAPE_CODE_DETECT	Enables TRIO0_ESCAPE_CODE_DETECT interrupt
25	TRIO2_RESYNC_FIFO_OVERFLOW	Enables TRIO2_RESYNC_FIFO_OVERFLOW interrupt
24	TRIO1_RESYNC_FIFO_OVERFLOW	Enables TRIO1_RESYNC_FIFO_OVERFLOW interrupt
23	TRIO0_RESYNC_FIFO_OVERFLOW	Enables TRIO0_RESYNC_FIFO_OVERFLOW interrupt
22	ERR_LANE_RESYNC	Enables ERR_LANE_RESYNC interrupt
21	ERR_FRAME_SYNC_S5	Enables ERR_FRAME_SYNC interrupt
20	ERR_FRAME_SYNC_S4	Enables ERR_FRAME_SYNC interrupt
19	ERR_FRAME_SYNC_S3	Enables ERR_FRAME_SYNC interrupt
18	ERR_FRAME_SYNC_S2	Enables ERR_FRAME_SYNC interrupt
17	ERR_FRAME_SYNC_S1	Enables ERR_FRAME_SYNC interrupt
16	ERR_FRAME_SYNC_S0	Enables ERR_FRAME_SYNC interrupt
15	FE	Enables frame end interrupt
14	GS	Enables generic short packet interrupt
13	LS	Enables line start interrupt
12	FS	Enables frame start interrupt
11	ERR_SOT_SYNC_HS_LNRD3	Enables ERR_SOT_SYNC_HS interrupt
10	ERR_SOT_SYNC_HS_LNRD2	Enables ERR_SOT_SYNC_HS interrupt
9	ERR_SOT_SYNC_HS_LNRD1	Enables ERR_SOT_SYNC_HS interrupt
8	ERR_SOT_SYNC_HS_LNRD0	Enables ERR_SOT_SYNC_HS interrupt
7	ERR_MULTI_LANE_SYNC	Enables ERR_MULTI_LANE_SYNC interrupt
6	ERR_AFIFO	Enables ERR_AFIFO interrupt
5	ERR_CRC	Enables ERR_CRC interrupt
4	ERR_ECC_DOUBLE	Enables ERR_ECC_DOUBLE interrupt
3	ERR_ECC_CORRECTED	Enables ERR_ECC_CORRECTED interrupt
2	ERR_ECC_NO_ERROR	ERR_ECC_NO_ERROR interrupt
1	ERR_ID	Enables ERR_ID interrupt
0	ERR_FRAME_SYNC	Enables ERR_FRAME_SYNC interrupt

1A042A14 SENINF3_CSI2_INT_STATUS **CSI2 Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name				TRIO2_ESCAPE_CODE_DETECT_STA	TRIO1_ESCAPE_CODE_DETECT_STA	TRIO0_ESCAPE_CODE_DETECT_STA	TRIO2_RESYNC_FIFO_OVERFLOW_STA	TRIO1_RESYNC_FIFO_OVERFLOW_STA	TRIO0_RESYNC_FIFO_OVERFLOW_STA	ERR_LANE_RESYNC_STA	ERR_FRAME_SYNC_S5_STA	ERR_FRAME_SYNC_S4_STA	ERR_FRAME_SYNC_S3_STA	ERR_FRAME_SYNC_S2_STA	ERR_FRAME_SYNC_S1_STA	ERR_FRAME_SYNC_S0_STA
Type				RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FE_STA	GS_STA	LS_STA	FS_STA	ERR_SOT_SYNC_HS_LNRD3_STA	ERR_SOT_SYNC_HS_LNRD2_STA	ERR_SOT_SYNC_HS_LNRD1_STA	ERR_SOT_SYNC_HS_LNRD0_STA	ERR_MULTI_LANE_SYNC_STA	ERR_AFIFO_STA	ERR_CRC_STA	ERR_ECC_DOUBLE_STA	ERR_ECC_CORRECTED_STA	ERR_ECC_NO_ERROR_STA	ERR_ID_STA	ERR_FRAME_SYNC_STA
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	TRIO2_ESCAPE_CODE_DETECT_STA	Asserted when the escape code of trio2 is detected
27	TRIO1_ESCAPE_CODE_DETECT_STA	Asserted when the escape code of trio1 is detected
26	TRIO0_ESCAPE_CODE_DETECT_STA	Asserted when the escape code of trio0 is detected
25	TRIO2_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of CPHY trio2 is overflowed
24	TRIO1_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of CPHY trio1 is overflowed
23	TRIO0_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of CPHY trio0 is overflowed
22	ERR_LANE_RESYNC_STA	Asserted when CPHY lane sync detect time is longer than set resync cycles
21	ERR_FRAME_SYNC_S5_STA	Asserted when a Frame End is not paired with a Frame Start on the same virtual channel
20	ERR_FRAME_SYNC_S4_STA	Asserted when a Frame End is not paired with a Frame Start on the same virtual channel
19	ERR_FRAME_SYNC_S3_STA	Asserted when a Frame End is not paired with a Frame Start on the same virtual channel
18	ERR_FRAME_SYNC_S2_STA	Asserted when a Frame End is not paired with a Frame Start on the same virtual channel
17	ERR_FRAME_SYNC_S1_STA	Asserted when a Frame End is not paired with a Frame Start on the same virtual channel
16	ERR_FRAME_SYNC_S0_STA	Asserted when a Frame End is not paired with a Frame Start on the same virtual channel
15	FE_STA	Frame end interrupt
14	GS_STA	Enables generic short packet interrupt
13	LS_STA	Line start interrupt
12	FS_STA	Frame start interrupt
11	ERR_SOT_SYNC_HS_LNRD3_STA	Asserted when proper synchronization cannot be expected
10	ERR_SOT_SYNC_HS_LNRD2_STA	Asserted when proper synchronization cannot be expected
9	ERR_SOT_SYNC_HS_LNRD1_STA	Asserted when proper synchronization cannot be expected
8	ERR_SOT_SYNC_HS_LNRD0_STA	Asserted when proper synchronization cannot be expected
7	ERR_MULTI_LANE_SYNC_STA	Asserted when multiple lane synchronization fails
6	ERR_AFIFO_STA	Asserted when error occurs in asynchronous FIFO

Bit(s)	Name	Description
5	ERR_CRC_STA	**Asserted when computed CRC code is different from received CRC code**
4	ERR_ECC_DOUBLE_STA	**Asserted when an ECC syndrome is computed and two bit errors are detected in the received packet header**
3	ERR_ECC_CORRECTED_STA	**Asserted when an ECC syndrome is computed and a single bit-error in the packet header was detected and corrected**
2	ERR_ECC_NO_ERROR_STA	**Asserted when an ECC syndrome is computed and the result is zero indicating a packet header that is considered to be without errors or has more than two bit-errors** CSI-2's ECC mechanism cannot detect this type of error.
1	ERR_ID_STA	**Asserted whean a packet header is decoded with an unrecognized or unimplemented data ID**
0	ERR_FRAME_SYNC_STA	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**

1A042A18 SENINF3_CSI2_DGB_SEL CSI2 Debug Selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_EN															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DEBUG_SEL							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	DEBUG_EN	Enables debug
7:0	DEBUG_SEL	Selects debug

1A042A1C SENINF3_CSI2_DBG_PORT CSI2 Debug Port 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CTL_DBG_PORT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	CTL_DBG_PORT	Debug port

1A042A20 SENINF3_CSI2_SPARE0 SPARE0 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	SPARE0	Spare register

1A042A24 SENINF3_CSI2_SPARE1 SPARE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE1	Spare register

1A042A28 SENINF3_CSI2_LNRC_FSM CSI2 Clock Lane RX FSM 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											LNRC_RX_FSM					
Type											RO					
Reset											0	0	0	0	0	1

Bit(s)	Name	Description
5:0	LNRC_RX_FSM	RX FSM of clock lane

1A042A2C SENINF3_CSI2_LNRD_FSM CSI2 Data Lane RX FSM 01010101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LNRD3_RX_FSM								LNRD2_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		LNRD1_RX_FSM								LNRD0_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1

Bit(s)	Name	Description
30:24	LNRD3_RX_FSM	RX FSM of data lane 3
22:16	LNRD2_RX_FSM	RX FSM of data lane 2
14:8	LNRD1_RX_FSM	RX FSM of data lane 1
6:0	LNRD0_RX_FSM	RX FSM of data lane 0

1A042A30 SENINF3_CSI2_FRAME_LINE_NUM — CSI2 Frame/Line Number — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LINE_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FRAME_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	LINE_NUM	Line number
15:0	FRAME_NUM	Frame number

1A042A34 SENINF3_CSI2_GENERIC_SHORT — CSI2 Generic Short Packet — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GENERIC_SHORT_PACKET_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											GENERIC_SHORT_PACKET_DT						
Type											RO					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
31:16	GENERIC_SHORT_PACKET_DATA	Generic short packet data
5:0	GENERIC_SHORT_PACKET_DT	Generic short packet data

1A042A38 SENINF3_CSI2_HSRX_DBG — CSI2 HSRX Enable — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DATA_LANE7_HSRX_EN	DATA_LANE6_HSRX_EN	DATA_LANE5_HSRX_EN	DATA_LANE4_HSRX_EN	CLOCK_LANE_HSRX_EN	DATA_LANE3_HSRX_EN	DATA_LANE2_HSRX_EN	DATA_LANE1_HSRX_EN	DATA_LANE0_HSRX_EN
Type								RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	DATA_LANE7_HSRX_EN	Enables data lane 3 HSRX circuit
7	DATA_LANE6_HSRX_EN	Enables data lane 2 HSRX circuit
6	DATA_LANE5_HSRX_EN	Enables data lane 1 HSRX circuit
5	DATA_LANE4_HSRX_EN	Enables data lane 0 HSRX circuit
4	CLOCK_LANE_HSRX_EN	Enables clock lane HSRX circut
3	DATA_LANE3_HSRX_EN	Enables data lane 3 HSRX circuit
2	DATA_LANE2_HSRX_EN	Enables data lane 2 HSRX circuit
1	DATA_LANE1_HSRX_EN	Enables data lane 1 HSRX circuit
0	DATA_LANE0_HSRX_EN	Enables data lane 0 HSRX circuit

1A042A3C SENINF3_CSI2_DI — CSI2 Data Interleaving Parameters — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DT3						VC3		DT2						VC2	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DT1						VC1		DT0						VC0	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:26	DT3	Data type identifier
25:24	VC3	Virtual channel identifier
23:18	DT2	Data type identifier
17:16	VC2	Virtual channel identifier
15:10	DT1	Data type identifier
9:8	VC1	Virtual channel identifier
7:2	DT0	Data type identifier
1:0	VC0	Virtual channel identifier

1A042A40 SENINF3_CSI2_HS_TRAIL — CSI2 HS Trail Timing Parameters — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									HS_TRAIL_PARAMETER							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	HS_TRAIL_PARAMETER	HS TRAIL parameter

1A042A44 SENINF3_CSI2_DI_CTRL **CSI2 Data Interleaving Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						DT3_INTERLEAVING		VC3_INTERLEAVING						DT2_INTERLEAVING		VC2_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DT1_INTERLEAVING		VC1_INTERLEAVING						DT0_INTERLEAVING		VC0_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0

Bit(s)	Name	Description
26:25	DT3_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
24	VC3_INTERLEAVING	**Virtual channel identifier interleaving**
18:17	DT2_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
16	VC2_INTERLEAVING	**Virtual channel identifier interleaving**
10:9	DT1_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
8	VC1_INTERLEAVING	**Virtual channel identifier interleaving**
2:1	DT0_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
0	VC0_INTERLEAVING	**Virtual channel identifier interleaving**

1A042A48 SENINF3_CSI2_LNRD_FS **CSI2 Data Lane RX FSM Other** **01010101**

M_X

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LNRD7_RX_FSM								LNRD6_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		LNRD5_RX_FSM								LNRD4_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1

Bit(s)	Name	Description
30:24	LNRD7_RX_FSM	RX FSM of data lane 3
22:16	LNRD6_RX_FSM	RX FSM of data lane 2
14:8	LNRD5_RX_FSM	RX FSM of data lane 1
6:0	LNRD4_RX_FSM	RX FSM of data lane 0

1A042A4C SENINF3_CSI2_DETECT_CON1 **CSI2 CPHY Detect Control sync** **0E492300**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				SYNC_WORD												
Type				RW												
Reset				0	1	1	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYNC_WORD								DETECT_SYNC_MASK							DETECT_SYNC_DISABLE
Type	RW								RW							RW
Reset	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:8	SYNC_WORD	
7:1	DETECT_SYNC_MASK	
0	DETECT_SYNC_DISABLE	

1A042A50 SENINF3_CSI2_DETECT_CON2 **CSI2 CPHY Detect Control Escape** **0E492300**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				ESCAPE_WORD												
Type				RW												
Reset				0	1	1	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ESCAPE_WORD								DETECT_ESCAPE_MASK							DETECT_ESCAPE_DISABLE

Type	RW								RW							RW
Reset	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:8	ESCAPE_WORD	
7:1	DETECT_ESCAPE_MASK	
0	DETECT_ESCAPE_DISABLE	

1A042A54 SENINF3_CSI2_DETECT_CON3 CSI2 CPHY Detect Control Post 12492400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				POST_WORD												
Type				RW												
Reset				1	0	0	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	POST_WORD								DETECT_POST_MASK							DETECT_POST_DISABLE
Type	RW								RW							RW
Reset	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:8	POST_WORD	
7:1	DETECT_POST_MASK	
0	DETECT_POST_DISABLE	

1A042A58 SENINF3_CSI2_RLR0_CON0 CSI2 CPHY RLR0 CON0 FFFFFF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLR0_PRBS_SEED_2								RLR0_PRBS_SEED_1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLR0_PRBS_SEED_0								RLR0_PRBS_PATTERN_SEL							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RLR0_PRBS_SEED_2	
23:16	RLR0_PRBS_SEED_1	
15:8	RLR0_PRBS_SEED_0	
7:0	RLR0_PRBS_PATTERN_SEL	

1A042A5C SENINF3_CSI2_RLR1_CO CSI2 CPHY RLR1 CON0 FFFFFF00

No

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLR1_PRBS_SEED_2								RLR1_PRBS_SEED_1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLR1_PRBS_SEED_0								RLR1_PRBS_PATTERN_SEL							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RLR1_PRBS_SEED_2	
23:16	RLR1_PRBS_SEED_1	
15:8	RLR1_PRBS_SEED_0	
7:0	RLR1_PRBS_PATTERN_SEL	

1A042A60 SENINF3_CSI2_RLR2_CON0 CSI2 CPHY RLR2 CON0 FFFFFF00

No

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLR2_PRBS_SEED_2								RLR2_PRBS_SEED_1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLR2_PRBS_SEED_0								RLR2_PRBS_PATTERN_SEL							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RLR2_PRBS_SEED_2	
23:16	RLR2_PRBS_SEED_1	
15:8	RLR2_PRBS_SEED_0	
7:0	RLR2_PRBS_PATTERN_SEL	

1A042A64 SENINF3_CSI2_RLR_CON CSI2 CPHY RLR CON0 FFFFFF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLRN_PRBS_SEED_2								RLRN_PRBS_SEED_1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLRN_PRBS_SEED_0								RLRN_PRBS_PATTERN_SEL							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RLRN_PRBS_SEED_2	
23:16	RLRN_PRBS_SEED_1	
15:8	RLRN_PRBS_SEED_0	
7:0	RLRN_PRBS_PATTERN_SEL	

Bit(s)	Name	Description

1A042A68 SENINF3_CSI2_MUX_CON **CSI2 Pin Pux Sel** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												POST_PACKET_IGNORE_EN	RLR_PATTERN_DELAY_EN	CPHY_RX_EXTERNAL_EN	CPHY_TX_EXTERNAL_EN	DPHY_RX_EXTERNAL_EN
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	POST_PACKET_IGNORE_EN	
3	RLR_PATTERN_DELAY_EN	
2	CPHY_RX_EXTERNAL_EN	
1	CPHY_TX_EXTERNAL_EN	
0	DPHY_RX_EXTERNAL_EN	

1A042A6C SENINF3_CSI2_DETECT_DBG0 **CSI2 Detection Debug 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		POSITION_SYNC_LANE2_ST				DETECT_POST_LANE2_ST	DETECT_ESCAPE_LANE2_ST	DETECT_SYNC_LANE2_ST		POSITION_ESCAPE_LANE1_ST				POSITION_SYNC_LANE1_ST		
Type		RO				RO	RO	RO		RO				RO		
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	POSITION_SYNC_LANE1_ST	DETECT_POST_LANE1_ST	DETECT_ESCAPE_LANE1_ST	DETECT_SYNC_LANE1_ST		POSITION_ESCAPE_LANE0_ST				POSITION_SYNC_LANE0_ST				DETECT_POST_LANE0_ST	DETECT_ESCAPE_LANE0_ST	DETECT_SYNC_LANE0_ST
Type	RO	RO	RO	RO		RO				RO				RO	RO	RO
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:27	POSITION_SYNC_LANE2_ST	
26	DETECT_POST_LANE2_ST	
25	DETECT_ESCAPE_LANE2_ST	
24	DETECT_SYNC_LANE2_ST	
22:19	POSITION_ESCAPE_LANE1_ST	
18:15	POSITION_SYNC_LANE1_ST	

Bit(s)	Name	Description
14	DETECT_POST_LANE1_ST	
13	DETECT_ESCAPE_LANE1_ST	
12	DETECT_SYNC_LANE1_ST	
10:7	POSITION_ESCAPE_LANE0_ST	
6:3	POSITION_SYNC_LANE0_ST	
2	DETECT_POST_LANE0_ST	
1	DETECT_ESCAPE_LANE0_ST	
0	DETECT_SYNC_LANE0_ST	

1A042A70 SENINF3_CSI2_DETECT_DBG1 CSI2 Detection Debug 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													POSITION_ESCAPE_LANE2_ST			
Type													RO			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	POSITION_ESCAPE_LANE2_ST	

1A042A74 SENINF3_CSI2_RESYNC_MERGE_CTL CSI2 Lane Resync Merge Control 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								LANE_RESYNC_FLUSH_EN				LANE_MERGE_INPUT_SEL		CPHY_LANE_RESYNC_CNT		
Type								RW				RW		RW		
Reset								0				0		0	0	1

Bit(s)	Name	Description
8	LANE_RESYNC_FLUSH_EN	
4	LANE_MERGE_INPUT_SEL	
2:0	CPHY_LANE_RESYNC_CNT	

1A042A78 SENINF3_CSI2_CTRL_TR CSI2 Control Trio Mux 00000088

IO_MUX

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TRIO2_MUX			TRIO1_MUX			TRIO0_MUX		
Type								RW			RW			RW		
Reset								0	1	0	0	0	1	0	0	0

Bit(s)	Name	Description
8:6	TRIO2_MUX	
5:3	TRIO1_MUX	
2:0	TRIO0_MUX	

1A042A7C SENINF3_CSI2_CTRL_TRIO_CON **CSI2 Control Trio Config** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											TRIO2_HSRX_EN	TRIO2_LPRX_EN	TRIO1_HSRX_EN	TRIO1_LPRX_EN	TRIO0_HSRX_EN	TRIO0_LPRX_EN
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5	TRIO2_HSRX_EN	
4	TRIO2_LPRX_EN	
3	TRIO1_HSRX_EN	
2	TRIO1_LPRX_EN	
1	TRIO0_HSRX_EN	
0	TRIO0_LPRX_EN	

1A042A80 SENINF3_FIX_ADDR_CPHY0_DBG **cphy_fix_point_addr_cphy0_debug** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								WORD_COUNT_OVER_FLOAT_CPHY0	ERROR_COUNT_CPHY0							
Type								RO	RO							
Reset								0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
24	WORD_COUNT_OVER_FLOAT_CPHY0	
23:16	ERROR_COUNT_CPHY0	

1A042A84 SENINF3_FIX_ADDR_CPHY1_DBG cphy_fix_point_addr_cphy1_debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								WORD_COUNT_OVER_FLOAT_CPHY1	ERROR_COUNT_CPHY1							
Type								RO	RO							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
24	WORD_COUNT_OVER_FLOAT_CPHY1	
23:16	ERROR_COUNT_CPHY1	

1A042A88 SENINF3_FIX_ADDR_CPHY2_DBG cphy_fix_point_addr_cphy2_debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								WORD_COUNT_OVER_FLOAT_CPHY2	ERROR_COUNT_CPHY2							
Type								RO	RO							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
24	WORD_COUNT_OVER_FLOAT_CPHY2	
23:16	ERROR_COUNT_CPHY2	

1A042A8C SENINF3_FIX_ADDR_DBG cphy_fix_point_addr_debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								WORD_COUNT_OVER_FLOAT	ERROR_COUNT							
Type								RO	RO							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
24	WORD_COUNT_OVER_FLOAT	
23:16	ERROR_COUNT	

1A042A90 SENINF3_WIRE_STATE_DECODE_CPHY0_DBG0 cphy_wire_state_decode_cphy0_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYMBOL_STREAM0_CPHY0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYMBOL_STREAM0_CPHY0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SYMBOL_STREAM0_CPHY0	

1A042A94 SENINF3_WIRE_STATE_DECODE_CPHY0_DBG1 cphy_wire_state_decode_cphy0_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SYMBOL_STREAM_VALID_CPHY0	SYMBOL_STREAM1_CPHY0									
Type						RO	RO									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	SYMBOL_STREAM_VALID_CPHY0	
9:0	SYMBOL_STREAM1_CPHY0	

1A042A98 SENINF3_WIRE_STATE_DECODE_CPHY1_DBG0 cphy_wire_state_decode_cphy1_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYMBOL_STREAM0_CPHY1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYMBOL_STREAM0_CPHY1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SYMBOL_STREAM0_CPHY1	

1A042A9C SENINF3_WIRE_STATE_DECODE_CPHY1_DBG1 cphy_wire_state_decode_cphy1_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SYMBOL_STREAM_VALID_CPHY1	SYMBOL_STREAM1_CPHY1									
Type						RO	RO									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	SYMBOL_STREAM_VALID_CPHY1	

Bit(s)	Name	Description
9:0	SYMBOL_STREAM1_CPHY1	

1A042AA0 SENINF3_WIRE_STATE_DECODE_CPHY2_DBG0 cphy_wire_state_decode_cphy2_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYMBOL_STREAM0_CPHY2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYMBOL_STREAM0_CPHY2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SYMBOL_STREAM0_CPHY2	

1A042AA4 SENINF3_WIRE_STATE_DECODE_CPHY2_DBG1 cphy_wire_state_decode_cphy2_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SYMBOL_STREAM_VALID_CPHY2	SYMBOL_STREAM1_CPHY2									
Type						RO	RO									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	SYMBOL_STREAM_VALID_CPHY2	
9:0	SYMBOL_STREAM1_CPHY2	

1A042AA8 SENINF3_SYNC_RESYNC_CTL CSI2 Sync Resync Control 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													FLUSH_VALID	SYNC_DETECTION_SEL		
Type													RW	RW		
Reset													0	0	0	1

Bit(s)	Name	Description
3	FLUSH_VALID	
2:0	SYNC_DETECTION_SEL	

1A042AAC SENINF3_POST_DETECT_CTL — CSI2 Post Detect Control — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															POST_EN	POST_DETECT_DISABLE
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	POST_EN	
0	POST_DETECT_DISABLE	

1A042AB0 SENINF3_WIRE_STATE_DECODE_CONFIG — CSI2 Wire State Decode Config — 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INIT_STATE_DECODE		
Type														RW		
Reset														1	0	0

Bit(s)	Name	Description
2:0	INIT_STATE_DECODE	

1A042AB4 SENINF3_CSI2_CPHY_LNRD_FSM **CPHY Data Lane RX FSM** **01010100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		TRIO 2_RX _FSM								TRIO1_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TRIO0_RX_FSM														
Type		RO														
Reset		0	0	0	0	0	0	1								

Bit(s)	Name	Description
30:24	TRIO2_RX_FSM	RX FSM of data trio 2
22:16	TRIO1_RX_FSM	RX FSM of data trio 1
14:8	TRIO0_RX_FSM	RX FSM of data trio 0

1A042AB8 SENINF3_FIX_ADDR_CPHY0_DBG0 **cphy_fix_point_addr_cphy0_debug0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD_COUNT_CPHY0_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY0_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD_COUNT_CPHY0_DBG0	

1A042ABC SENINF3_FIX_ADDR_CPHY0_DBG1 **cphy_fix_point_addr_cphy0_debug1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY0_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY0_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERROR_RECORD_CPHY0_DBG0	
15:0	WORD_COUNT_CPHY0_DBG1	

1A042AC0 SENINF3_FIX_ADDR_CPHY0_DBG2 cphy_fix_point_addr_cphy0_debug2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY0_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERROR_RECORD_CPHY0_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ERROR_RECORD_CPHY0_DBG1	

1A042AC4 SENINF3_FIX_ADDR_CPHY1_DBG0 cphy_fix_point_addr_cphy1_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD_COUNT_CPHY1_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY1_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD_COUNT_CPHY1_DBG0	

1A042AC8 SENINF3_FIX_ADDR_CPHY1_DBG1 cphy_fix_point_addr_cphy1_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY1_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY1_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERROR_RECORD_CPHY1_DBG0	
15:0	WORD_COUNT_CPHY1_DBG1	

1A042ACC SENINF3_FI cphy_fix_point_addr_cphy1_debug2 00000000

X_ADDR_CPH Y1_DBG2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY1_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERROR_RECORD_CPHY1_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ERROR_RECORD_CPHY1_DBG1	

1A042AD0 SENINF3_FIX_ADDR_CPHY2_DBG0 cphy_fix_point_addr_cphy2_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD_COUNT_CPHY2_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY2_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD_COUNT_CPHY2_DBG0	

1A042AD4 SENINF3_FIX_ADDR_CPHY2_DBG1 cphy_fix_point_addr_cphy2_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY2_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY2_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERROR_RECORD_CPHY2_DBG0	
15:0	WORD_COUNT_CPHY2_DBG1	

1A042AD8 SENINF3_FIX_ADDR_CPH cphy_fix_point_addr_cphy2_debug2 00000000

Y2_DBG2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY2_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERROR_RECORD_CPHY2_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ERROR_RECORD_CPHY2_DBG1	

1A042ADC SENINF3_FIX_ADDR_DBG cphy_fix_point_addr_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD_COUNT_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD_COUNT_DBG0	

1A042AE0 SENINF3_FIX_ADDR_DBG1 cphy_fix_point_addr_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERROR_RECORD_DBG0	
15:0	WORD_COUNT_DBG1	

1A042AE4 SENINF3_FIX_ADDR_DBG2 cphy_fix_point_addr_debug2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	ERROR_RECORD_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERROR_RECORD_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ERROR_RECORD_DBG1	

1A042AE8 SENINF3_CSI2_MODE — CSI2 Packet Structure — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	csr_cphy_wc_pos								csr_cphy_di_pos							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						csr_csi2_header_len			csr_csi2_mode							
Type						RW			RW							
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	csr_cphy_wc_pos	
23:16	csr_cphy_di_pos	
10:8	csr_csi2_header_len	0: 4 bytes 1: 12 bytes 2: 24 bytes 4: 36 bytes
7:0	csr_csi2_mode	

1A042AF0 SENINF3_CSI2_DI_EXT — CSI2 Data Interleaving Parameters Extend — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DT5						VC5		DT4						VC4	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:10	DT5	Data type identifier
9:8	VC5	Virtual channel identifier
7:2	DT4	Data type identifier
1:0	VC4	Virtual channel identifier

1A042AF4 SENINF3_CSI2_DI_CTRL_EXT **CSI2 Data Interleaving Control Extend** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DT5_INTERLEAVING		VC5_INTERLEAVING						DT4_INTERLEAVING		VC4_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0

Bit(s)	Name	Description
10:9	DT5_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
8	VC5_INTERLEAVING	**Virtual channel identifier interleaving**
2:1	DT4_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
0	VC4_INTERLEAVING	**Virtual channel identifier interleaving**

1A042AF8 SENINF3_CSI2_CPHY_LOOPBACK **CSI2 SW Trigger sync_init and hs_en** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RELEASE_SYNC_INIT	TRIGGER_SYNC_INIT
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RELEASE_SYNC_INIT	Releases sync_init in cphy tx loopback test mode
0	TRIGGER_SYNC_INIT	Triggers sync_init and hs_en in cphy tx loopback test mode

1A042B00 SENINF3_CSI2_PROGSEQ_0 **CSI2 CPHY Program sequence_0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name		PROG SEQ_ S7				PROG SEQ_ S6				PROGSEQ_S5				PROGSEQ_S4		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PROGSEQ_S3				PROGSEQ_S2				PROGSEQ_S1				PROGSEQ_S0		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	PROGSEQ_S7	Fix symbol for prbs generator
26:24	PROGSEQ_S6	Fix symbol for prbs generator
22:20	PROGSEQ_S5	Fix symbol for prbs generator
18:16	PROGSEQ_S4	Fix symbol for prbs generator
14:12	PROGSEQ_S3	Fix symbol for prbs generator
10:8	PROGSEQ_S2	Fix symbol for prbs generator
6:4	PROGSEQ_S1	Fix symbol for prbs generator
2:0	PROGSEQ_S0	Fix symbol for prbs generator

1A042B04 SENINF3_CSI2_PROGSEQ_1 — **CSI2 CPHY Program sequence_1** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										PROG SEQ_ S13				PROGSEQ_S 12		
Type										RW				RW		
Reset										0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PROGSEQ_S11				PROGSEQ_S10				PROGSEQ_S9				PROGSEQ_S8		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
22:20	PROGSEQ_S13	Fix symbol for prbs generator
18:16	PROGSEQ_S12	Fix symbol for prbs generator
14:12	PROGSEQ_S11	Fix symbol for prbs generator
10:8	PROGSEQ_S10	Fix symbol for prbs generator
6:4	PROGSEQ_S9	Fix symbol for prbs generator
2:0	PROGSEQ_S8	Fix symbol for prbs generator

1A042B10 SENINF3_CSI2_INT_EN_EXT — **CSI2 Interrupt Enable Extend** — **0000071F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_WCLR_EN															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						ERR_SOT_SYNC	ERR_SOT_SYNC	ERR_SOT_SYNC				DPHY3_RESYNC	DPHY2_RESYNC	DPHY1_RESYNC	DPHY0_RESYNC	ERR_LANE_RES

						_HS_TRIO2	_HS_TRIO1	_HS_TRIO0				_FIFO_OVERFLOW	_FIFO_OVERFLOW	_FIFO_OVERFLOW	_FIFO_OVERFLOW	YNC
Type						RW	RW	RW				RW	RW	RW	RW	RW
Reset						1	1	1				1	1	1	1	1

Bit(s)	Name	Description
31	INT_WCLR_EN	Enables Interrupt write clear
10	ERR_SOT_SYNC_HS_TRIO2	Enables TRIO2 ERR_SOT_SYNC_HS interrupt
9	ERR_SOT_SYNC_HS_TRIO1	Enables TRIO1 ERR_SOT_SYNC_HS interrupt
8	ERR_SOT_SYNC_HS_TRIO0	Enables TRIO0 ERR_SOT_SYNC_HS interrupt
4	DPHY3_RESYNC_FIFO_OVERFLOW	Enables LANE3_RESYNC_FIFO_OVERFLOW interrupt
3	DPHY2_RESYNC_FIFO_OVERFLOW	Enables LANE2_RESYNC_FIFO_OVERFLOW interrupt
2	DPHY1_RESYNC_FIFO_OVERFLOW	Enables LANE1_RESYNC_FIFO_OVERFLOW interrupt
1	DPHY0_RESYNC_FIFO_OVERFLOW	Enables LANE0_RESYNC_FIFO_OVERFLOW interrupt
0	ERR_LANE_RESYNC	Enables ERR_LANE_RESYNC interrupt

1A042B14 SENINF3_CSI2_INT_STATUS_EXT CSI2 Interrupt Status Extend 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						ERR_SOT_SYNC_HS_TRIO2_STA	ERR_SOT_SYNC_HS_TRIO1_STA	ERR_SOT_SYNC_HS_TRIO0_STA				DPHY3_RESYNC_FIFO_OVERFLOW_STA	DPHY2_RESYNC_FIFO_OVERFLOW_STA	DPHY1_RESYNC_FIFO_OVERFLOW_STA	DPHY0_RESYNC_FIFO_OVERFLOW_STA	ERR_LANE_RESYNC_STA
Type						RO	RO	RO				RO	RO	RO	RO	RO
Reset						0	0	0				0	0	0	0	0

Bit(s)	Name	Description
10	ERR_SOT_SYNC_HS_TRIO2_STA	Asserted when proper synchronization cannot be expected
9	ERR_SOT_SYNC_HS_TRIO1_STA	Asserted when proper synchronization cannot be expected
8	ERR_SOT_SYNC_HS_TRIO0_STA	Asserted when proper synchronization cannot be expected
4	DPHY3_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of dphy lane3 is overflowed
3	DPHY2_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of dphy lane2 is overflowed
2	DPHY1_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of dphy lane1 is overflowed
1	DPHY0_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of dphy lane0 is overflowed
0	ERR_LANE_RESYNC_STA	Asserted when dphy lane sync detect time is larger than setting resync cycles

1A042B18 SENINF3_CSI2_CPHY_FIX_POINT_RST **CSI2 CPHY Fix Point Reset Mode** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CPHY_FIX_POINT_RST_MODE	CPHY_FIX_POINT_SW_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	CPHY_FIX_POINT_RST_MODE	Fix point rest mode
0	CPHY_FIX_POINT_SW_RST	Fix point software reset

1A042B20 SENINF3_CSI2_DPHY_RESYNC_CTL **CSI2 DPHY Lane Resync Control** **00000100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DPHY_RESYNC_CNT								DPHY_RESYNC_FLUSH_EN	DPHY_RESYNC_DATAOUT_OPTION	DPHY_BYPASS_LANE_RESYNC
Type						RW								RW	RW	RW
Reset						0	0	1						0	0	0

Bit(s)	Name	Description
10:8	DPHY_RESYNC_CNT	Detect lane skew cycle count
2	DPHY_RESYNC_FLUSH_EN	Enables lane resync flush
1	DPHY_RESYNC_DATAOUT_OPTION	Data output option
0	DPHY_BYPASS_LANE_RESYNC	Bypass lane resync function

Module name: mipi_rx_config_csi2 Base address: (+1a042800h)

Address	Name	Width	Register Function
1A042800	MIPI_RX_CON00_CSI2	32	MIPI RX Config Register

Address	Name	Width	Register Function
1A042804	MIPI_RX_CON04_CSI2	32	MIPI RX Config Register
1A042808	MIPI_RX_CON08_CSI2	32	MIPI RX Config Register
1A042824	MIPI_RX_CON24_CSI2	32	MIPI RX Config Register
1A042828	MIPI_RX_CON28_CSI2	32	MIPI RX Config Register
1A042834	MIPI_RX_CON34_CSI2	32	MIPI RX Config Register
1A042838	MIPI_RX_CON38_CSI2	32	MIPI RX Config Register
1A04283C	MIPI_RX_CON3C_CSI2	32	MIPI RX Config Register
1A042840	MIPI_RX_CON40_CSI2	32	MIPI RX Config Register
1A042844	MIPI_RX_CON44_CSI2	32	MIPI RX Config Register
1A042848	MIPI_RX_CON48_CSI2	32	MIPI RX Config Register
1A04284C	MIPI_RX_CON4C_CSI2	32	MIPI RX Config Register
1A042850	MIPI_RX_CON50_CSI2	32	MIPI RX Config Register
1A04287C	MIPI_RX_CON7C_CSI2	32	MIPI RX Config Register
1A042880	MIPI_RX_CON80_CSI2	32	MIPI RX Config Register
1A042884	MIPI_RX_CON84_CSI2	32	MIPI RX Config Register
1A042888	MIPI_RX_CON88_CSI2	32	MIPI RX Config Register
1A04288C	MIPI_RX_CON8C_CSI2	32	MIPI RX Config Register
1A042890	MIPI_RX_CON90_CSI2	32	MIPI RX Config Register
1A042894	MIPI_RX_CON94_CSI2	32	MIPI RX Config Register
1A042898	MIPI_RX_CON98_CSI2	32	MIPI RX Config Register
1A0428A0	MIPI_RX_CONA0_CSI2	32	MIPI RX Config Register
1A0428B0	MIPI_RX_CONB0_CSI2	32	Deskew control register
1A0428B4	MIPI_RX_CONB4_CSI2	32	Deskew sync detection sequence
1A0428B8	MIPI_RX_CONB8_CSI2	32	Deskew timing control
1A0428BC	MIPI_RX_CONBC_CSI2	32	Deskew mode
1A0428C0	MIPI_RX_CONC0_CSI2	32	Interrupt enable
1A0428C4	MIPI_RX_CONC4_CSI2	32	Interrupt status

Address	Name	Width	Register Function
1A0428C8	MIPI_RX_CONC8_CSI2	32	Debug mux select
1A0428CC	MIPI_RX_CONCC_CSI2	32	Debug outputs
1A0428D0	MIPI_RX_COND0_CSI2	32	Deskew delay length

1A042800 MIPI_RX_CON00_CSI2 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_CSI0_LNR3_HSRX_OFFSET_CODE					RG_CSI0_LNR3_HSRX_CAL_EN	RG_CSI0_LNR3_HSRX_CAL_APPLY		RG_CSI0_LNR2_HSRX_OFFSET_CODE					RG_CSI0_LNR2_HSRX_CAL_EN	RG_CSI0_LNR2_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI0_LNR1_HSRX_OFFSET_CODE					RG_CSI0_LNR1_HSRX_CAL_EN	RG_CSI0_LNR1_HSRX_CAL_APPLY		RG_CSI0_LNR0_HSRX_OFFSET_CODE					RG_CSI0_LNR0_HSRX_CAL_EN	RG_CSI0_LNR0_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	RG_CSI0_LNR3_HSRX_OFFSET_CODE	**Lane3 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
25	RG_CSI0_LNR3_HSRX_CAL_EN	**Lane3 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
24	RG_CSI0_LNR3_HSRX_CAL_APPLY	**Lane3 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
22:18	RG_CSI0_LNR2_HSRX_OFFSET_CODE	**Lane2 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
17	RG_CSI0_LNR2_HSRX_CAL_EN	**Lane2 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
16	RG_CSI0_LNR2_HSRX_CAL_APPLY	**Lane2 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
14:10	RG_CSI0_LNR1_HSRX_OFFSET_CODE	**Lane1 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage

Bit(s)	Name	Description
		5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
9	RG_CSI0_LNR1_HSRX_CAL_EN	**Lane1 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
8	RG_CSI0_LNR1_HSRX_CAL_APPLY	**Lane1 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
6:2	RG_CSI0_LNR0_HSRX_OFFSET_CODE	**Lane0 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
1	RG_CSI0_LNR0_HSRX_CAL_EN	**Lane0 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
0	RG_CSI0_LNR0_HSRX_CAL_APPLY	**Lane0 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result

1A042804 MIPI_RX_CON04_CSI2 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_CSI0_LNR7_HSRX_OFFSET_CODE					RG_CSI0_LNR7_HSRX_CAL_EN	RG_CSI0_LNR7_HSRX_CAL_APPLY		RG_CSI0_LNR6_HSRX_OFFSET_CODE					RG_CSI0_LNR6_HSRX_CAL_EN	RG_CSI0_LNR6_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI0_LNR5_HSRX_OFFSET_CODE					RG_CSI0_LNR5_HSRX_CAL_EN	RG_CSI0_LNR5_HSRX_CAL_APPLY		RG_CSI0_LNR4_HSRX_OFFSET_CODE					RG_CSI0_LNR4_HSRX_CAL_EN	RG_CSI0_LNR4_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	RG_CSI0_LNR7_HSRX_OFFSET_CODE	**Lane7 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
25	RG_CSI0_LNR7_HSRX_CAL_EN	**Lane7 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
24	RG_CSI0_LNR7_HSRX_CAL_APPLY	**Lane7 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
22:18	RG_CSI0_LNR6_HSRX_OFFSET_CODE	**Lane6 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage

Bit(s)	Name	Description
		5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
17	RG_CSI0_LNR6_HSRX_CAL_EN	**Lane6 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
16	RG_CSI0_LNR6_HSRX_CAL_APPLY	**Lane6 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
14:10	RG_CSI0_LNR5_HSRX_OFFSET_CODE	**Lane5 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
9	RG_CSI0_LNR5_HSRX_CAL_EN	**Lane5 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
8	RG_CSI0_LNR5_HSRX_CAL_APPLY	**Lane5 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
6:2	RG_CSI0_LNR4_HSRX_OFFSET_CODE	**Lane4 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
1	RG_CSI0_LNR4_HSRX_CAL_EN	**Lane4 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
0	RG_CSI0_LNR4_HSRX_CAL_APPLY	**Lane4 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result

1A042808 MIPI_RX_CON08_CSI2 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_CSI0_LNR11_HSRX_OFFSET_CODE					RG_CSI0_LNR11_HSRX_CAL_EN	RG_CSI0_LNR11_HSRX_CAL_APPLY		RG_CSI0_LNR10_HSRX_OFFSET_CODE					RG_CSI0_LNR10_HSRX_CAL_EN	RG_CSI0_LNR10_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI0_LNR9_HSRX_OFFSET_CODE					RG_CSI0_LNR9_HSRX_CAL_EN	RG_CSI0_LNR9_HSRX_CAL_APPLY		RG_CSI0_LNR8_HSRX_OFFSET_CODE					RG_CSI0_LNR8_HSRX_CAL_EN	RG_CSI0_LNR8_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	RG_CSI0_LNR11_HSRX_OFFSET	**Lane11 HSRX offset calibration code:**

Bit(s)	Name	Description
	_CODE	5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
25	RG_CSI0_LNR11_HSRX_CAL_EN	**Lane11 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
24	RG_CSI0_LNR11_HSRX_CAL_APPLY	**Lane11 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
22:18	RG_CSI0_LNR10_HSRX_OFFSET_CODE	**Lane10 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
17	RG_CSI0_LNR10_HSRX_CAL_EN	**Lane10 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
16	RG_CSI0_LNR10_HSRX_CAL_APPLY	**Lane10 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
14:10	RG_CSI0_LNR9_HSRX_OFFSET_CODE	**Lane9 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
9	RG_CSI0_LNR9_HSRX_CAL_EN	**Lane9 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
8	RG_CSI0_LNR9_HSRX_CAL_APPLY	**Lane9 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
6:2	RG_CSI0_LNR8_HSRX_OFFSET_CODE	**Lane8 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
1	RG_CSI0_LNR8_HSRX_CAL_EN	**Lane8 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
0	RG_CSI0_LNR8_HSRX_CAL_APPLY	**Lane8 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result

1A042824 MIPI_RX_CON24_CSI2 **MIPI RX Config Register** **E4000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI0_BIST_LN3_MUX		CSI0_BIST_LN2_MUX		CSI0_BIST_LN1_MUX		CSI0_BIST_LN0_MUX		CSI0_BIST_SETTLE_DELAY							
Type	RW		RW		RW		RW		RW							
Reset	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI0_BIST_TERM_DELAY								CSI0_BIST_CLK4X_SEL	CSI0_BIST_CLK_SEL	CSI0_BIST_FIX_PAT			CSI0_BIST_EN	CSI0_BIST_NUM	

Type	RW								RW	RW	RW			RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0			0	0	0

Bit(s)	Name	Description
31:30	CSI0_BIST_LN3_MUX	**CSI0 Lane mux**
29:28	CSI0_BIST_LN2_MUX	**CSI0 Lane mux**
27:26	CSI0_BIST_LN1_MUX	**CSI0 Lane mux**
25:24	CSI0_BIST_LN0_MUX	**CSI0 Lane mux**
23:16	CSI0_BIST_SETTLE_DELAY	**CSI0 Settle Delay Setting**
15:8	CSI0_BIST_TERM_DELAY	**CSI0 Term Delay Setting**
7	CSI0_BIST_CLK4X_SEL	**CSI0 CLK4X Sel** 0: inverse 1: not inverse
6	CSI0_BIST_CLK_SEL	**CSI0 CLK Sel** 0: inverse 1: not inverse
5	CSI0_BIST_FIX_PAT	**CSI0 Bist Patern** 0: Random 1: Fix
2	CSI0_BIST_EN	**CSI0 Bist Enalbe**
1:0	CSI0_BIST_NUM	**CSI0 Bist num** 0: 1 lane 1: 2 lane 2: 3 lane 3: 4 lane

1A042828 MIPI_RX_CON28_CSI2 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CSI0_BIST_CSI2_DATA_OK	CSI0_BIST_LANE_FSM_OK	CSI0_BIST_HS_FSM_OK	CSI0_BIST_DATA_OK	CSI0_BIST_START
Type												RO	RO	RO	RO	RO
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	CSI0_BIST_CSI2_DATA_OK	CSI0 BIST CSI2 Data ok
3	CSI0_BIST_LANE_FSM_OK	CSI0 BIST High Speed FSM ok
2	CSI0_BIST_HS_FSM_OK	CSI0 BIST Data Lane FSM ok
1	CSI0_BIST_DATA_OK	CSI0 BIST DPHY Data ok
0	CSI0_BIST_START	CSI0 BIST start status

1A042834 MIPI_RX_CON34_CSI2 MIPI RX Config Register E4000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI0 _BIS		CSI0 _BIS		CSI0 _BIS		CSI0 _BIS		CSI0 _BIS							

	T_LN 7_MUX		T_LN 6_MUX		T_LN 5_MUX		T_LN 4_MUX		T_HS DET_MUX							
Type	RW		RW		RW		RW		RW							
Reset	1	1	1	0	0	1	0	0	0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BIST_MODE
Type																RW
Reset																0

Bit(s)	Name	Description
31:30	CSI0_BIST_LN7_MUX	CSI0 Lane mux
29:28	CSI0_BIST_LN6_MUX	CSI0 Lane mux
27:26	CSI0_BIST_LN5_MUX	CSI0 Lane mux
25:24	CSI0_BIST_LN4_MUX	CSI0 Lane mux
23:22	CSI0_BIST_HSDET_MUX	CSI0 HSDET mux
0	BIST_MODE	BIST mode enable

1A042838 MIPI_RX_CON38_CSI2 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_c kpha se_t rio2					rg_ckphase_trio1						rg_ckphase_trio0				
Type	RW					RW						RW				
Reset	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						MIPI_RX_SW_CPHY_RX_MODE	MIPI_RX_SW_CPHY_TX_MODE	MIPI_RX_SW_RST					MIPI_RX_HW_CAL_OPTION	MIPI_RX_HW_CAL_START	MIPI_RX_SW_CAL_MODE	MIPI_RX_SW_CTRL_MODE
Type						RW	RW	RW					RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:27	rg_ckphase_trio2	
26:22	rg_ckphase_trio1	
20:16	rg_ckphase_trio0	
10	MIPI_RX_SW_CPHY_RX_MODE	**CPHY RX SW control mode**
9	MIPI_RX_SW_CPHY_TX_MODE	**CPHY TX SW control mode**
8:4	MIPI_RX_SW_RST	**SW reset**
3	MIPI_RX_HW_CAL_OPTION	**HW calibration option** 0: 8 cycles 1 : 16cycles
2	MIPI_RX_HW_CAL_START	**HW calibration trigger**
1	MIPI_RX_SW_CAL_MODE	**SW calibration mode**
0	MIPI_RX_SW_CTRL_MODE	**SW control mode**

1A04283C MIPI_RX_CON3C_CSI2 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIPI_RX_SW_CTRL_															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIPI_RX_SW_CTRL_															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MIPI_RX_SW_CTRL_	SW control

1A042840 MIPI_RX_CON40_CSI2 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_CSIo_LNRD3_HSRX_INVERT	RG_CSIo_LNRD3_LPRX_SWAP	RG_CSIo_LNRD2_HSRX_INVERT	RG_CSIo_LNRD2_LPRX_SWAP	RG_CSIo_LNRD1_HSRX_INVERT	RG_CSIo_LNRD1_LPRX_SWAP	RG_CSIo_LNRDo_HSRX_INVERT	RG_CSIo_LNRDo_LPRX_SWAP			RG_CSIo_LNRC_HSRX_INVERT	RG_CSIo_LNRC_LPRX_SWAP
Type					RW	RW	RW	RW	RW	RW	RW	RW			RW	RW
Reset					0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
11	RG_CSIo_LNRD3_HSRX_INVERT	
10	RG_CSIo_LNRD3_LPRX_SWAP	
9	RG_CSIo_LNRD2_HSRX_INVERT	
8	RG_CSIo_LNRD2_LPRX_SWAP	
7	RG_CSIo_LNRD1_HSRX_INVERT	
6	RG_CSIo_LNRD1_LPRX_SWAP	
5	RG_CSIo_LNRDo_HSRX_INVERT	
4	RG_CSIo_LNRDo_LPRX_SWAP	
1	RG_CSIo_LNRC_HSRX_INVERT	
o	RG_CSIo_LNRC_LPRX_SWAP	

1A042844 MIPI_RX_CON44_CSI2 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSIo_LNR3_HSRX_OFFSET_CODE					DA_CSIo_LNR3_HSRX_CAL_EN	DA_CSIo_LNR3_HSRX_CAL_APPLY		DA_CSIo_LNR2_HSRX_OFFSET_CODE					DA_CSIo_LNR2_HSRX_CAL_EN	DA_CSIo_LNR2_HSRX_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DA_CSIo_LNR1_HSRX_OFF					DA_C	DA_C		DA_CSIo_LNRo_HSRX_OFF					DA_C	DA_C

		SET_CODE					SIo_LNR1_HSRX_CAL_EN	SIo_LNR1_HSRX_CAL_APPLY		SET_CODE					SIo_LNRo_HSRX_CAL_EN	SIo_LNRo_HSRX_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	DA_CSI0_LNR3_HSRX_OFFSET_CODE	
25	DA_CSI0_LNR3_HSRX_CAL_EN	
24	DA_CSI0_LNR3_HSRX_CAL_APPLY	
22:18	DA_CSI0_LNR2_HSRX_OFFSET_CODE	
17	DA_CSI0_LNR2_HSRX_CAL_EN	
16	DA_CSI0_LNR2_HSRX_CAL_APPLY	
14:10	DA_CSI0_LNR1_HSRX_OFFSET_CODE	
9	DA_CSI0_LNR1_HSRX_CAL_EN	
8	DA_CSI0_LNR1_HSRX_CAL_APPLY	
6:2	DA_CSI0_LNR0_HSRX_OFFSET_CODE	
1	DA_CSI0_LNR0_HSRX_CAL_EN	
0	DA_CSI0_LNR0_HSRX_CAL_APPLY	

1A042848 MIPI_RX_CON48_CSI2 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSI0_LNR7_HSRX_OFFSET_CODE					DA_CSI0_LNR7_HSRX_CAL_EN	DA_CSI0_LNR7_HSRX_CAL_APPLY		DA_CSI0_LNR6_HSRX_OFFSET_CODE					DA_CSI0_LNR6_HSRX_CAL_EN	DA_CSI0_LNR6_HSRX_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DA_CSI0_LNR5_HSRX_OFFSET_CODE					DA_CSI0_LNR5_HSRX_CAL_EN	DA_CSI0_LNR5_HSRX_CAL_APPLY		DA_CSI0_LNR4_HSRX_OFFSET_CODE					DA_CSI0_LNR4_HSRX_CAL_EN	DA_CSI0_LNR4_HSRX_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	DA_CSI0_LNR7_HSRX_OFFSET_CODE	
25	DA_CSI0_LNR7_HSRX_CAL_EN	

Bit(s)	Name	Description
24	DA_CSI0_LNR7_HSRX_CAL_APPLY	
22:18	DA_CSI0_LNR6_HSRX_OFFSET_CODE	
17	DA_CSI0_LNR6_HSRX_CAL_EN	
16	DA_CSI0_LNR6_HSRX_CAL_APPLY	
14:10	DA_CSI0_LNR5_HSRX_OFFSET_CODE	
9	DA_CSI0_LNR5_HSRX_CAL_EN	
8	DA_CSI0_LNR5_HSRX_CAL_APPLY	
6:2	DA_CSI0_LNR4_HSRX_OFFSET_CODE	
1	DA_CSI0_LNR4_HSRX_CAL_EN	
0	DA_CSI0_LNR4_HSRX_CAL_APPLY	

1A04284C MIPI_RX_CON4C_CSI2 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSI0_LNR11_HSRX_OFFSET_CODE					DA_CSI0_LNR11_HSRX_CAL_EN	DA_CSI0_LNR11_HSRX_CAL_APPLY		DA_CSI0_LNR10_HSRX_OFFSET_CODE					DA_CSI0_LNR10_HSRX_CAL_EN	DA_CSI0_LNR10_HSRX_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DA_CSI0_LNR9_HSRX_OFFSET_CODE					DA_CSI0_LNR9_HSRX_CAL_EN	DA_CSI0_LNR9_HSRX_CAL_APPLY		DA_CSI0_LNR8_HSRX_OFFSET_CODE					DA_CSI0_LNR8_HSRX_CAL_EN	DA_CSI0_LNR8_HSRX_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	DA_CSI0_LNR11_HSRX_OFFSET_CODE	
25	DA_CSI0_LNR11_HSRX_CAL_EN	
24	DA_CSI0_LNR11_HSRX_CAL_APPLY	
22:18	DA_CSI0_LNR10_HSRX_OFFSET_CODE	
17	DA_CSI0_LNR10_HSRX_CAL_EN	
16	DA_CSI0_LNR10_HSRX_CAL_APPLY	
14:10	DA_CSI0_LNR9_HSRX_OFFSET_CODE	
9	DA_CSI0_LNR9_HSRX_CAL_EN	
8	DA_CSI0_LNR9_HSRX_CAL_APPLY	

Bit(s)	Name	Description
6:2	DA_CSIo_LNR8_HSRX_OFFSET_CODE	
1	DA_CSIo_LNR8_HSRX_CAL_EN	
0	DA_CSIo_LNR8_HSRX_CAL_APPLY	

1A042850 MIPI_RX_CON50_CSI2 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_CSIo_BCLK_INV
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_CSIo_BCLK_INV	**CSIo byte clock** 0: Not inverse 1: Inverse

1A04287C MIPI_RX_CON7C_CSI2 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DA_CSIo_LNRDo_HSRX_DELAY_CODE					DA_CSIo_LNRDo_HSRX_DELAY_APPLY	DA_CSIo_LNRDo_HSRX_DELAY_EN
Type											RO				RO	RO
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:2	DA_CSIo_LNRDo_HSRX_DELAY_CODE	
1	DA_CSIo_LNRDo_HSRX_DELAY_APPLY	
0	DA_CSIo_LNRDo_HSRX_DELAY_EN	

1A042880 MIPI_RX_CON80_CSI2 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DA_CSI0_LNRD1_HSRX_DELAY_CODE					DA_CSI0_LNRD1_HSRX_DELAY_APPLY	DA_CSI0_LNRD1_HSRX_DELAY_EN
Type											RO				RO	RO
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:2	DA_CSI0_LNRD1_HSRX_DELAY_CODE	
1	DA_CSI0_LNRD1_HSRX_DELAY_APPLY	
0	DA_CSI0_LNRD1_HSRX_DELAY_EN	

1A042884 MIPI_RX_CON84_CSI2 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DA_CSI0_LNRD2_HSRX_DELAY_CODE					DA_CSI0_LNRD2_HSRX_DELAY_APPLY	DA_CSI0_LNRD2_HSRX_DELAY_EN
Type											RO				RO	RO
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:2	DA_CSI0_LNRD2_HSRX_DELAY_CODE	
1	DA_CSI0_LNRD2_HSRX_DELAY_APPLY	
0	DA_CSI0_LNRD2_HSRX_DELAY_EN	

1A042888 MIPI_RX_CON88_CSI2 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DA_CSIo_LNRD3_HSRX_DELAY_CODE					DA_CSIo_LNRD3_HSRX_DELAY_APPLY	DA_CSIo_LNRD3_HSRX_DELAY_EN
Type											RO				RO	RO
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:2	DA_CSIo_LNRD3_HSRX_DELAY_CODE	
1	DA_CSIo_LNRD3_HSRX_DELAY_APPLY	
0	DA_CSIo_LNRD3_HSRX_DELAY_EN	

1A04288C MIPI_RX_CON8C_CSI2 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSIo_LNRDo_HSRX_DELAY_CODE						RG_CSIo_LNRDo_HSRX_DELAY_APPLY	RG_CSIo_LNRDo_HSRX_DELAY_EN
Type									RW						RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSIo_LNRDo_HSRX_DELAY_CODE	
1	RG_CSIo_LNRDo_HSRX_DELAY_APPLY	
0	RG_CSIo_LNRDo_HSRX_DELAY_EN	

1A042890 MIPI_RX_CO **MIPI RX Config Register** **00000000**

N90_CSI2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSIo_LNRD1_HSRX_DELAY_CODE						RG_CSIo_LNRD1_HSRX_DELAY_APPLY	RG_CSIo_LNRD1_HSRX_DELAY_EN
Type									RW						RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSIo_LNRD1_HSRX_DELAY_CODE	
1	RG_CSIo_LNRD1_HSRX_DELAY_APPLY	
0	RG_CSIo_LNRD1_HSRX_DELAY_EN	

1A042894 MIPI_RX_CON94_CSI2 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSIo_LNRD2_HSRX_DELAY_CODE						RG_CSIo_LNRD2_HSRX_DELAY_APPLY	RG_CSIo_LNRD2_HSRX_DELAY_EN
Type									RW						RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSIo_LNRD2_HSRX_DELAY_CODE	
1	RG_CSIo_LNRD2_HSRX_DELAY_APPLY	
0	RG_CSIo_LNRD2_HSRX_DELAY_EN	

1A042898 MIPI_RX_CON98_CSI2 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSIo_LNRD3_HSRX_DELAY_CODE						RG_CSIo_LNRD3_HSRX_DELAY_APPLY	RG_CSIo_LNRD3_HSRX_DELAY_EN
Type									RW						RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSIo_LNRD3_HSRX_DELAY_CODE	
1	RG_CSIo_LNRD3_HSRX_DELAY_APPLY	
0	RG_CSIo_LNRD3_HSRX_DELAY_EN	

1A0428A0 MIPI_RX_CONA0_CSI2 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSIo_LNRC_HSRX_DELAY_CODE						RG_CSIo_LNRC_HSRX_DELAY_APPLY	RG_CSIo_LNRC_HSRX_DELAY_EN
Type									RW						RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSIo_LNRC_HSRX_DELAY_CODE	
1	RG_CSIo_LNRC_HSRX_DELAY_APPLY	
0	RG_CSIo_LNRC_HSRX_DELAY_EN	

1A0428B0 MIPI_RX_CONB0_CSI2 **Deskew control register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	DESKEW_ENABLE	DESKEW_IP_SEL														DESKEW_CSI2_RST_ENABLE
Type	RW	RW														RW
Reset	0	0														0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DESKEW_ACC_MODE					DESKEW_TRIGGER_MODE			DESKEW_SW_RST				Delay_APPLY_MODE			
Type	RW					RW			RW				RW			
Reset	0	0	0	0		0	0	0	0				0	0	0	0

Bit(s)	Name	Description
31	DESKEW_ENABLE	**Deskew enable**
30	DESKEW_IP_SEL	0: New IP 1: Old IP
16	DESKEW_CSI2_RST_ENABLE	**Reset CSI2 IP when in DESKEW mode**
15:12	DESKEW_ACC_MODE	**Deskew edge mode**
10:8	DESKEW_TRIGGER_MODE	**Conditions for trigger DESKEW function**
7	DESKEW_SW_RST	**Deskew SW reset**
3:0	Delay_APPLY_MODE	**Delay apply mode:** 00/01: HW mode 10: RG mode 11: SW mode

1A0428B4 MIPI_RX_CONB4_CSI2 Deskew sync detection sequence 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EXPECTED_SYNC_CODE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYNC_CODE_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	EXPECTED_SYNC_CODE	**Programmable sync code** In normal case, it should be 16'hFFFF.
15:0	SYNC_CODE_MASK	**When the bit is set to 1'b1, HW will compare its value with received sync code.** Otherwise, no compare.

1A0428B8 MIPI_RX_CONB8_CSI2 Deskew timing control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								DESKEW_TIME_OUT_	DESKEW_TIME_OUT							

								EN								
Type								RW	RW							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DESKEW_HOLD_TIME								DESKEW_SETUP_TIME			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
24	DESKEW_TIME_OUT_EN	**Deskew time out enable**
23:16	DESKEW_TIME_OUT	**Deskew time out period** If no deskew sync code is detected, FSM will be reset after this period.
11:8	DESKEW_HOLD_TIME	**Delay code apply hold time**
3:0	DESKEW_SETUP_TIME	**Delay code apply setup time**

1A0428BC MIPI_RX_CONBC_CSI2 **Deskew mode** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							DESKEW_LANE_NUMBER						DESKEW_DELAY_APPLY_MODE			
Type							RW						RW			
Reset							0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DESKEW_DETECTION_CNT											DESKEW_DETECTION_MODE			
Type		RW											RW			
Reset		0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
25:24	DESKEW_LANE_NUMBER	Deskew lane number
19:16	DESKEW_DELAY_APPLY_MODE	Deskew delay apply mode
14:8	DESKEW_DETECTION_CNT	Deskew detection count
3:0	DESKEW_DETECTION_MODE	Deskew detection mode

1A0428C0 MIPI_RX_CONC0_CSI2 **Interrupt enable** **80000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DESKEW_INTERRUPT_W1C_EN															
Type	RW															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DESKEW_INTERRUPT_ENABLE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	DESKEW_INTERRUPT_W1C_EN	Interrupt W1C enable
7:0	DESKEW_INTERRUPT_ENABLE	Interrupt enable

1A0428C4 MIPI_RX_CONC4_CSI2 Interrupt status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DESKEW_INTERRUPT_STATUS							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DESKEW_INTERRUPT_STATUS	Interrupt status

1A0428C8 MIPI_RX_CONC8_CSI2 Debug mux select 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DESKEW_DEBUG_MUX_SELECT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DESKEW_DEBUG_MUX_SELECT	Debug signal select

1A0428CC MIPI_RX_CONCC_CSI2 Debug outputs 00100100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DESKEW_DEBUG_OUTPUTS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DESKEW_DEBUG_OUTPUTS															
Type	RO															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DESKEW_DEBUG_OUTPUTS	Debug signal outputs

Bit(s)	Name	Description

1A0428D0 MIPI_RX_CON D0_CSI2 **Deskew delay length** **0000000F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DESKEW_DELAY_LENGTH					
Type											RW					
Reset											0	0	1	1	1	1

Bit(s)	Name	Description
5:0	DESKEW_DELAY_LENGTH	Deskew delay length

Module name: seninf3_mux Base address: (+1a042d00h)

Address	Name	Width	Register Function
1A042D00	SENINF3_MUX_CTRL	32	SENINF 3 Control Register
1A042D04	SENINF3_MUX_INTEN	32	SENINF 3 Interrupt Enable Register
1A042D08	SENINF3_MUX_INTSTA	32	SENINF 3 Interrupt Status Register
1A042D0C	SENINF3_MUX_SIZE	32	SENINF 3 Image Size Register
1A042D10	SENINF3_MUX_DEBUG_1	32	SENINF 3 Debug Register 1
1A042D14	SENINF3_MUX_DEBUG_2	32	SENINF 3 Debug Register 2
1A042D18	SENINF3_MUX_DEBUG_3	32	SENINF 3 Debug Register 3
1A042D1C	SENINF3_MUX_DEBUG_4	32	SENINF 3 Debug Register 4
1A042D20	SENINF3_MUX_DEBUG_5	32	SENINF 3 Debug Register 5
1A042D24	SENINF3_MUX_DEBUG_6	32	SENINF 3 Debug Register 6
1A042D28	SENINF3_MUX_DEBUG_7	32	SENINF 3 Debug Register 7
1A042D2C	SENINF3_MUX_SPARE	32	SENINF 3 Spare Register
1A042D30	SENINF3_MUX_DATA	32	SENINF 3 Data Register
1A042D34	SENINF3_MUX_DATA_CNT	32	SENINF 3 Data Count Register
1A042D38	SENINF3_MUX_CROP	32	SENINF 3 Crop Size Register
1A042D3C	SENINF3_MUX_CTRL_EXT	32	SENINF 3 Control Register Extend

1A042D00 SENINF3_MUX_CTRL **SENINF 3 Control Register** **06DF0080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_MUX_EN	CROP_EN	FIFO_FULL_WR_EN		FIFO_FLUSH_EN						FIFO_PUSH_EN					
Type	RW	RW	RW		RW						RW					
Reset	0	0	0	0	0	1	1	0	1	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_SRC_SEL				OVERRUN_RST_EN	SENINF_HSYNC_POL	SENINF_VSYNC_POL	SENINF_PIX_SEL	SENINF_HSYNC_MASK		SENINF_MUX_RDY_VALUE	SENINF_MUX_RDY_MODE			SENINF_IRQ_SW_RST	SENINF_MUX_SW_RST
Type	RW				RW	RW	RW	RW	RW		RW	RW			RW	RW
Reset	0	0	0	0	0	0	0	0	1		0	0			0	0

Bit(s)	Name	Description
31	SENINF_MUX_EN	**Enables seninf_mux** 0: Disable 1: Enable
30	CROP_EN	**Sensor crop function**
29:28	FIFO_FULL_WR_EN	0: FIFO write operation is prohibited when FIFO is full. 1: FIFO write operation is prohibited after FIFO full occurs. 2: FIFO write operation is allowed when FIFO is full.
27:22	FIFO_FLUSH_EN	**Normal mode: 6'b011011** JPEG two pixel mode: 6'b011000
21:16	FIFO_PUSH_EN	**Normal mode: 6'b011111** JPEG two pixel mode : 6'b011110
15:12	SENINF_SRC_SEL	**Selects SENINF input source:** {seninf_mux_sel_ext, seninf_mux_sel} 00: OCSI2 VC0 01: Test model 02: CCIR656 03: Parallel sensor 04: Serial sensor 06: OCSI2 VC1 08: NCSI2 VC0 09: NCSI2 VC1 0A: NCSI2 VC2 0B: NCSI2 VC3 0C: NCSI2 VC4 0D: NCSI2 VC5
11	OVERRUN_RST_EN	**Enables SENINF mux software reset for overrun** 0: No action 1: Auto self-reset for overrun situation
10	SENINF_HSYNC_POL	**SENINF HSYNC polarity**
9	SENINF_VSYNC_POL	**SENINF VSYNC polarity**
8	SENINF_PIX_SEL	**SENINF output bus width:** {seninf_pixel_sel_ext, seninf_pixel_sel} 00: 1 pixel/cycle 01: 2 pixels/cycle 10: 4 pixels/cycle
7	SENINF_HSYNC_MASK	**Masks hsync**

Bit(s)	Name	Description
		0: Send hsync when vsync = 1 1: Does not send hsync when vsync = 1
5	SENINF_MUX_RDY_VALUE	**seninf_rdy value in force mode**
4	SENINF_MUX_RDY_MODE	0: seninf_rdy normal mode 1: seninf_rdy force mode
1	SENINF_IRQ_SW_RST	**SENINF IRQ software reset, active high** 0: De-assert reset 1: Assert reset
0	SENINF_MUX_SW_RST	**SENINF mux software reset, active high** 0: De-assert reset 1: Assert reset

1A042D04 SENINF3_MUX_INTEN **SENINF 3 Interrupt Enable Register** **8000007F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_IRQ_CLR_SEL															
Type	RW															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SENINF_SENSOR_HSIZEERR_IRQ_EN	SENINF_SENSOR_VSIZEERR_IRQ_EN	SENINF_HSIZEERR_IRQ_EN	SENINF_VSIZEERR_IRQ_EN	SENINF_FSMERR_IRQ_EN	SENINF_CRCERR_IRQ_EN	SENINF_OVERRUN_IRQ_EN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										1	1	1	1	1	1	1

Bit(s)	Name	Description
31	SENINF_IRQ_CLR_SEL	0: Read clear 1: Write clear
6	SENINF_SENSOR_HSIZEERR_IRQ_EN	Enables sensor HSIZE ERROR IRQ
5	SENINF_SENSOR_VSIZEERR_IRQ_EN	Enables sensor VSIZE ERROR IRQ
4	SENINF_HSIZEERR_IRQ_EN	Enables async FIFO HSIZE ERROR IRQ
3	SENINF_VSIZEERR_IRQ_EN	Enables async FIFO VSIZE ERROR IRQ
2	SENINF_FSMERR_IRQ_EN	Enables FSM ERROR IRQ
1	SENINF_CRCERR_IRQ_EN	Enables CRR ERROR IRQ
0	SENINF_OVERRUN_IRQ_EN	Enables FIFO OVERRUN IRQ

1A042D08 SENINF3_MUX_INTSTA **SENINF 3 Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SENINF_SENSOR_HSIZEERR_IRQ_STA	SENINF_SENSOR_VSIZEERR_IRQ_STA	SENINF_HSIZEERR_IRQ_STA	SENINF_VSIZEERR_IRQ_STA	SENINF_FSMERR_IRQ_STA	SENINF_CRCERR_IRQ_STA	SENINF_OVERRUN_IRQ_STA
Type										RO	RO	RO	RO	RO	RO	RO
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	SENINF_SENSOR_HSIZEERR_IRQ_STA	Sensor HSIZE ERROR IRQ status
5	SENINF_SENSOR_VSIZEERR_IRQ_STA	Sensor VSIZE ERROR IRQ status
4	SENINF_HSIZEERR_IRQ_STA	Async FIFO HSIZE ERROR IRQ status
3	SENINF_VSIZEERR_IRQ_STA	Async FIFO VSIZE ERROR IRQ status
2	SENINF_FSMERR_IRQ_STA	FSM ERROR IRQ status
1	SENINF_CRCERR_IRQ_STA	CRR ERROR IRQ status
0	SENINF_OVERRUN_IRQ_STA	FIFO OVERRUN IRQ status

1A042D0C SENINF3_MUX_SIZE — SENINF 3 Image Size Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_HSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_VSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_HSIZE	Senor image horizontal size
15:0	SENINF_VSIZE	Senor image vertical size

1A042D10 SENINF3_MUX_DEBUG_1 — SENINF 3 Debug Register 1 — 0000C303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	1	1	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A042D14 SENINF3_MUX_DEBUG_2 — SENINF 3 Debug Register 2 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A042D18 SENINF3_MUX_DEBUG_3 — SENINF 3 Debug Register 3 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A042D1C SENINF3_MUX_DEBUG_4 — SENINF 3 Debug Register 4 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A042D20 SENINF3_MUX_DEBUG_5 — SENINF 3 Debug Register 5 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A042D24 SENINF3_MUX_DEBUG_6 SENINF 3 Debug Register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A042D28 SENINF3_MUX_DEBUG_7 SENINF 3 Debug Register 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A042D2C SENINF3_MUX_SPARE SENINF 3 Spare Register 000E2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SENI NF_S PARE			
Type													RW			
Reset													1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENI NF_S PARE		SENI NF_F IFO_	SENI NF_V CNT_ SEL		SENINF_CR C_SEL										

			FULL_SEL													
Type	RW		RW	RW		RW										
Reset	0	0	1	0	0	0	0									

Bit(s)	Name	Description
19:14	SENINF_SPARE	**Spare register**
13	SENINF_FIFO_FULL_SEL	0: Does not send FIFO full to cam 1: Send FIFO full to cam
12:11	SENINF_VCNT_SEL	0: Vsync rising 1: Vsync rising d1 2: Vsync rising d2 3: Vsync rising d3
10:9	SENINF_CRC_SEL	0: Vsync rising 1: Vsync rising d1 2: Vsync rising d2 3: Vsync rising d3

1A042D30 SENINF3_MUX_DATA SENINF 3 Data Register 40000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA1															
Type	RO															
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_DATA1	
15:0	SENINF_DATA0	

1A042D34 SENINF3_MUX_DATA_CNT SENINF 3 Data Count Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENINF_DATA_CNT	

1A042D38 SENINF3_MUX_CROP SENINF 3 Crop Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_CROP_X2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_CROP_X1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_CROP_X2	
15:0	SENINF_CROP_X1	

1A042D3C SENINF3_MUX_CTRL_EXT **SENINF 3 Control Register Extend** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												SENINF_PIX_SEL_EXT			SENINF_SRC_SEL_EXT	
Type												RW			RW	
Reset												0			0	0

Bit(s)	Name	Description
4	SENINF_PIX_SEL_EXT	**SENINF output bus width:** {seninf_pixel_sel_ext, seninf_pixel_sel} 00: 1 pixel/cycle 01: 2 pixels/cycle 10: 4 pixels/cycle
1:0	SENINF_SRC_SEL_EXT	**Selects SENINF input source:** {seninf_src_sel_ext, seninf_src_sel} 18: CSI2 VC0 19: CSI2 VC1 1A: CSI2 VC2 1B: CSI2 VC3 1C: CSI2 VC4 28: CSI3 VC0 29: CSI3 VC1 2A: CSI3 VC2 2B: CSI3 VC3 2C: CSI3 VC4

Module name: SENINF3_NCSI2 Base address: (+1a042700h)

Address	Name	Width	Register Function
1A042700	SENINF3_NCSI2_CTL	32	CSI2 Function Enable

Address	Name	Width	Register Function
1A042704	SENINF3_NCSI2_LNRC_TIMING	32	CSI2 Clock Lane Timing Parameters
1A042708	SENINF3_NCSI2_LNRD_TIMING	32	CSI2 Data Lane Timing Parameters
1A04270C	SENINF3_NCSI2_DPCM	32	CSI2 DPCM Parameters
1A042710	SENINF3_NCSI2_INT_EN	32	CSI2 Interrupt Enable
1A042714	SENINF3_NCSI2_INT_STATUS	32	CSI2 Interrupt Status
1A042718	SENINF3_NCSI2_DGB_SEL	32	CSI2 Debug Selection
1A04271C	SENINF3_NCSI2_DBG_PORT	32	CSI2 Debug Port
1A042720	SENINF3_NCSI2_SPARE0	32	SPARE0
1A042724	SENINF3_NCSI2_SPARE1	32	SPARE1
1A042728	SENINF3_NCSI2_LNRC_FSM	32	CSI2 Clock Lane RX FSM
1A04272C	SENINF3_NCSI2_LNRD_FSM	32	CSI2 Data Lane RX FSM
1A042730	SENINF3_NCSI2_FRAME_LINE_NUM	32	CSI2 Frame/Lline Number
1A042734	SENINF3_NCSI2_GENERIC_SHORT	32	CSI2 Generic Short Packet
1A042738	SENINF3_NCSI2_HSRX_DBG	32	CSI2 HSRX Enable
1A04273C	SENINF3_NCSI2_DI	32	CSI2 Data Interleaving Parameters
1A042740	SENINF3_NCSI2_HS_TRAIL	32	CSI2 HS Trail Timing Parameters
1A042744	SENINF3_NCSI2_DI_CTRL	32	CSI2 Data Interleaving Control
1A042748	SENINF3_NCSI2_DI_1	32	CSI2 Data Interleaving Parameters
1A04274C	SENINF3_NCSI2_DI_CTRL_1	32	CSI2 Data Interleaving Control
1A042750	SENINF3_NCSI2_DPHY_RESYNC_CTL	32	CSI2 DPHY Lane Resync Control

1A042700 SENINF3_NCSI2_CTL **CSI2 Function Enable** **018861E0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			VS_OUT_CYCLE_NUM	BER	CLOCK_HS_OPTION	REF_SYNC_DET_EN	HS_TRAIL_EN	ASYNC_FIFO_RST_SCH		SYNC_DET_BIT_SWAP_EN	SYNC_DET_EN	SYNC_DET_SCHEME	FLUSH_MODE			ED_SEL
Type			RW		RW	RW	RW	RW		RW	RW	RW	RW			RW
Reset			0	0	0	0	0	1	1	0	0	0	1	0		0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VS_T	BYTE	IMAG	GENE			HS_E	HS_P	HSRX	CRC_	ECC_	CLOC	DATA	DATA	DATA	DATA

	YPE	2PIX EL_E N	E_PA CKET _EN	RIC_ LONG _PAC KET_ EN			ND_E N	RPR_ EN	_DET _EN	EN	EN	K_LA NE_E N	_LAN E3_E N	_LAN E2_E N	_LAN E1_E N	_LAN E0_E N
Type	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	1	1	0			0	1	1	1	1	0	0	0	0	0

Bit(s)	Name	Description
29:28	VS_OUT_CYCLE_NUMBER	0: 4T 1: 8T
27	CLOCK_HS_OPTION	0: Enable clock lane HS based on LP11, LP01, LP00 1: Enable clock lane HS based on LP00
26	REF_SYNC_DET_EN	**Reference sync detect signal to do analog sync**
25	HS_TRAIL_EN	**Extends HS trail**
24:23	ASYNC_FIFO_RST_SCH	
22	SYNC_DET_BITSWAP_EN	
21	SYNC_DET_EN	**Enables sync sequence detection**
20	SYNC_DET_SCHEME	0: B8 1: 101110
19:18	FLUSH_MODE	0: Disable 1: Flush at first cycle of LP11 2: Flush at LP11 3: Reserved
16	ED_SEL	0: {WCH,WCL,DI} 1: {DI,WCL,WCH}
15	VS_TYPE	**VS type** 0: 4T 1: Frame start to frame end
14	BYTE2PIXEL_EN	**Byte 2 pixel conversion**
13	IMAGE_PACKET_EN	**Image data types**
12	GENERIC_LONG_PACKET_EN	**Generic long packet data types**
9	HS_END_EN	**Enables HS_EX reset at packet end**
8	HS_PRPR_EN	**Enables RX_HS_PRPR state**
7	HSRX_DET_EN	**Enables HSRX termination auto-detection flow**
6	CRC_EN	**Enables checksum**
5	ECC_EN	**Enables packet header ECC**
4	CLOCK_LANE_EN	**Enables clock lane**
3	DATA_LANE3_EN	**Enables data lane 3**
2	DATA_LANE2_EN	**Enables data lane 2**
1	DATA_LANE1_EN	**Enables data lane 1**
0	DATA_LANE0_EN	**Enables data lane 0**

1A042704 SENINF3_NCSI2_LNRC_TIMING **CSI2 Clock Lane Timing Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SETTLE_PARAMETER								TERM_PARAMETER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	SETTLE_PARAMETER	TD_SETTLE parameter
7:0	TERM_PARAMETER	TD_TERM_EN parameter

1A042708 SENINF3_NCSI2_LNRD_TIMING **CSI2 Data Lane Timing Parameters** **00002000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SETTLE_PARAMETER								TERM_PARAMETER							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	SETTLE_PARAMETER	TD_SETTLE parameter
7:0	TERM_PARAMETER	TD_TERM_EN parameter

1A04270C SENINF3_NCSI2_DPCM **CSI2 DPCM Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DI_2A_DPCM_EN	DI_37_DPCM_EN	DI_36_DPCM_EN	DI_35_DPCM_EN	DI_34_DPCM_EN	DI_33_DPCM_EN	DI_32_DPCM_EN	DI_31_DPCM_EN	DI_30_DPCM_EN				DPCM_MODE			
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW				RW			
Reset	0	0	0	0	0	0	0	0	0				0	0	0	0

Bit(s)	Name	Description
15	DI_2A_DPCM_EN	**Enables DPCM**
14	DI_37_DPCM_EN	**Enables DPCM**
13	DI_36_DPCM_EN	**Enables DPCM**
12	DI_35_DPCM_EN	**Enables DPCM**
11	DI_34_DPCM_EN	**Enables DPCM**
10	DI_33_DPCM_EN	**Enables DPCM**
9	DI_32_DPCM_EN	**Enables DPCM**
8	DI_31_DPCM_EN	**Enables DPCM**
7	DI_30_DPCM_EN	**Enables DPCM**
3:0	DPCM_MODE	0: 10-8-10

1A042710 SENINF3_NCSI2_INT_EN **CSI2 Interrupt Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	INT_WCLR_EN					DPHY3_RESYNC_FIFO_OVERFLOW	DPHY2_RESYNC_FIFO_OVERFLOW	DPHY1_RESYNC_FIFO_OVERFLOW	DPHY0_RESYNC_FIFO_OVERFLOW	ERR_LANE_RESYNC	ERR_FRAME_SYNC_S5	ERR_FRAME_SYNC_S4	ERR_FRAME_SYNC_S3	ERR_FRAME_SYNC_S2	ERR_FRAME_SYNC_S1	ERR_FRAME_SYNC_S0
Type	RW					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0					0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GS	LS	FS	ERR_SOT_SYNC_HS_LNRD3	ERR_SOT_SYNC_HS_LNRD2	ERR_SOT_SYNC_HS_LNRD1	ERR_SOT_SYNC_HS_LNRD0	ERR_MULTI_LANE_SYNC	ERR_AFIFO	ERR_CRC	ERR_ECC_DOUBLE	ERR_ECC_CORRECTED	ERR_ECC_NO_ERROR	ERR_ID	ERR_FRAME_SYNC
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	INT_WCLR_EN	Enables Interrupt write clear
26	DPHY3_RESYNC_FIFO_OVERFLOW	Enables LANE3_RESYNC_FIFO_OVERFLOW interrupt
25	DPHY2_RESYNC_FIFO_OVERFLOW	Enables LANE2_RESYNC_FIFO_OVERFLOW interrupt
24	DPHY1_RESYNC_FIFO_OVERFLOW	Enables LANE1_RESYNC_FIFO_OVERFLOW interrupt
23	DPHY0_RESYNC_FIFO_OVERFLOW	Enables LANE0_RESYNC_FIFO_OVERFLOW interrupt
22	ERR_LANE_RESYNC	Enables ERR_LANE_RESYNC interrupt
21	ERR_FRAME_SYNC_S5	Enables ERR_FRAME_SYNC interrupt
20	ERR_FRAME_SYNC_S4	Enables ERR_FRAME_SYNC interrupt
19	ERR_FRAME_SYNC_S3	Enables ERR_FRAME_SYNC interrupt
18	ERR_FRAME_SYNC_S2	Enables ERR_FRAME_SYNC interrupt
17	ERR_FRAME_SYNC_S1	Enables ERR_FRAME_SYNC interrupt
16	ERR_FRAME_SYNC_S0	Enables ERR_FRAME_SYNC interrupt t
14	GS	Enables generic short packet interrupt
13	LS	Enables line start interrupt
12	FS	Enables frame start interrupt
11	ERR_SOT_SYNC_HS_LNRD3	Enables ERR_SOT_SYNC_HS interrupt
10	ERR_SOT_SYNC_HS_LNRD2	Enables ERR_SOT_SYNC_HS interrupt
9	ERR_SOT_SYNC_HS_LNRD1	Enables ERR_SOT_SYNC_HS interrupt
8	ERR_SOT_SYNC_HS_LNRD0	Enables ERR_SOT_SYNC_HS interrupt
7	ERR_MULTI_LANE_SYNC	Enables ERR_MULTI_LANE_SYNC interrupt
6	ERR_AFIFO	Enables ERR_AFIFO interrupt
5	ERR_CRC	Enables ERR_CRC interrupt
4	ERR_ECC_DOUBLE	Enables ERR_ECC_DOUBLE interrupt
3	ERR_ECC_CORRECTED	Enables ERR_ECC_CORRECTED interrupt
2	ERR_ECC_NO_ERROR	ERR_ECC_NO_ERROR interrupt
1	ERR_ID	Enables ERR_ID interrupt
0	ERR_FRAME_SYNC	Enables ERR_FRAME_SYNC interrupt

1A042714 SENINF3_NCSI2_INT_STATUS **CSI2 Interrupt Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						DPHY3_RESYNC	DPHY2_RESYNC	DPHY1_RESYNC	DPHY0_RESYNC	ERR_LANE_RES	ERR_FRAME_SY	ERR_FRAME_SY	ERR_FRAME_SY	ERR_FRAME_SY	ERR_FRAME_SY	ERR_FRAME_SY

						_FIFO_OVERFLOW_STA	_FIFO_OVERFLOW_STA	_FIFO_OVERFLOW_STA	_FIFO_OVERFLOW_STA	YNC_STA	NC_S5	NC_S4	NC_S3	NC_S2	NC_S1	NC_S0
Type						RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GS	LS	FS	ERR_SOT_SYNC_HS_LNRD3	ERR_SOT_SYNC_HS_LNRD2	ERR_SOT_SYNC_HS_LNRD1	ERR_SOT_SYNC_HS_LNRD0	ERR_MULTI_LANE_SYNC	ERR_AFIFO	ERR_CRC	ERR_ECC_DOUBLE	ERR_ECC_CORRECTED	ERR_ECC_NO_ERROR	ERR_ID	ERR_FRAME_SYNC
Type		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26	DPHY3_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of DPHY lane3 is overflowed**
25	DPHY2_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of DPHY lane2 is overflowed**
24	DPHY1_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of DPHY lane1 is overflowed**
23	DPHY0_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of DPHY lane0 is overflowed**
22	ERR_LANE_RESYNC_STA	**Asserted when DPHY lane sync detect time is longer than setting resync cycles**
21	ERR_FRAME_SYNC_S5	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
20	ERR_FRAME_SYNC_S4	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
19	ERR_FRAME_SYNC_S3	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
18	ERR_FRAME_SYNC_S2	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
17	ERR_FRAME_SYNC_S1	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
16	ERR_FRAME_SYNC_S0	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
14	GS	**Enables generic short packet interrupt**
13	LS	**Line start interrupt**
12	FS	**Frame start interrupt**
11	ERR_SOT_SYNC_HS_LNRD3	**Asserted when proper synchronization cannot be expected**
10	ERR_SOT_SYNC_HS_LNRD2	**Asserted when proper synchronization cannot be expected**
9	ERR_SOT_SYNC_HS_LNRD1	**Asserted when proper synchronization cannot be expected**
8	ERR_SOT_SYNC_HS_LNRD0	**Asserted when proper synchronization cannot be expected**
7	ERR_MULTI_LANE_SYNC	**Asserted when multiple lane synchronization fails**
6	ERR_AFIFO	**Asserted when error occurs in asynchronous FIFO**
5	ERR_CRC	**Asserted when computed CRC code is different from received CRC code**
4	ERR_ECC_DOUBLE	**Asserted when an ECC syndrome is computed and two bit-errors are detected in the received packet header**
3	ERR_ECC_CORRECTED	**Asserted when an ECC syndrome is computed and a single bit-error in the packet header was detected and corrected**
2	ERR_ECC_NO_ERROR	**Asserted when an ECC syndrome is computed and**

Bit(s)	Name	Description
		the result is zero indicating a packet header that is considered to be without errors or has more than two bit errors CSI-2's ECC mechanism cannot detect this type of error.
1	ERR_ID	**Asserted whean a packet header is decoded with an unrecognized or unimplemented data ID**
0	ERR_FRAME_SYNC	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**

1A042718 SENINF3_NCSI2_DGB_SEL CSI2 Debug Selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DEBUG_SEL							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DEBUG_SEL	Selects debug

1A04271C SENINF3_NCSI2_DBG_PORT CSI2 Debug Port 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CTL_DBG_PORT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	CTL_DBG_PORT	Debug port

1A042720 SENINF3_NCSI2_SPARE0 SPARE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE0															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE0	Spare register

1A042724 SENINF3_NCSI2_SPARE1 SPARE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE1	Spare register

1A042728 SENINF3_NCSI2_LNRC_FSM CSI2 Clock Lane RX FSM 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											LNRC_RX_FSM					
Type											RO					
Reset											0	0	0	0	0	1

Bit(s)	Name	Description
5:0	LNRC_RX_FSM	RX FSM of clock lane

1A04272C SENINF3_NCSI2_LNRD_FSM CSI2 Data Lane RX FSM 01010101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LNRD3_RX_FSM								LNRD2_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		LNRD1_RX_FSM								LNRD0_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1

Bit(s)	Name	Description
30:24	LNRD3_RX_FSM	RX FSM of data lane 3
22:16	LNRD2_RX_FSM	RX FSM of data lane 2
14:8	LNRD1_RX_FSM	RX FSM of data lane 1
6:0	LNRD0_RX_FSM	RX FSM of data lane 0

1A042730 SENINF3_NCSI2_FRAME_LINE_NUM CSI2 Frame/Lline Number 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LINE_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FRAME_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	LINE_NUM	Line number
15:0	FRAME_NUM	Frame number

1A042734 SENINF3_NCSI2_GENERIC_SHORT CSI2 Generic Short Packet 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GENERIC_SHORT_PACKET_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											GENERIC_SHORT_PACKET_DT						
Type											RO					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
31:16	GENERIC_SHORT_PACKET_DATA	Generic short packet data
5:0	GENERIC_SHORT_PACKET_DT	Generic short packet data

1A042738 SENINF3_NCSI2_HSRX_DBG CSI2 HSRX Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name												CLOCK_LANE_HSRX_EN	DATA_LANE3_HSRX_EN	DATA_LANE2_HSRX_EN	DATA_LANE1_HSRX_EN	DATA_LANE0_HSRX_EN
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	CLOCK_LANE_HSRX_EN	Enables clock lane HSRX circut
3	DATA_LANE3_HSRX_EN	Enables data lane 3 HSRX circuit
2	DATA_LANE2_HSRX_EN	Enables data lane 2 HSRX circuit
1	DATA_LANE1_HSRX_EN	Enables data lane 1 HSRX circuit
0	DATA_LANE0_HSRX_EN	Enables data lane 0 HSRX circuit

1A04273C SENINF3_NCSI2_DI — **CSI2 Data Interleaving Parameters** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DT3						VC3		DT2						VC2	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DT1						VC1		DT0						VC0	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:26	DT3	Data type indentifier
25:24	VC3	Virtual channel indentifier
23:18	DT2	Data type indentifier
17:16	VC2	Virtual channel indentifier
15:10	DT1	Data type indentifier
9:8	VC1	Virtual channel indentifier
7:2	DT0	Data type indentifier
1:0	VC0	Virtual channel indentifier

1A042740 SENINF3_NCSI2_HS_TRAIL — **CSI2 HS Trail Timing Parameters** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									HS_TRAIL_PARAMETER							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	HS_TRAIL_PARAMETER	**HS trail parameter**

1A042744 SENINF3_NCSI2_DI_CTRL **CSI2 Data Interleaving Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						DT3_INTERLEAVING		VC3_INTERLEAVING						DT2_INTERLEAVING		VC2_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DT1_INTERLEAVING		VC1_INTERLEAVING						DT0_INTERLEAVING		VC0_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0

Bit(s)	Name	Description
26:25	DT3_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
24	VC3_INTERLEAVING	**Virtual channel identifier interleaving**
18:17	DT2_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
16	VC2_INTERLEAVING	**Virtual channel identifier interleaving**
10:9	DT1_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
8	VC1_INTERLEAVING	**Virtual channel identifier interleaving**
2:1	DT0_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
0	VC0_INTERLEAVING	**Virtual channel identifier interleaving**

1A042748 SENINF3_NCSI2_DI_1 **CSI2 Data Interleaving Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DT5						VC5		DT4						VC4	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
15:10	DT5	Data type indentifier
9:8	VC5	Virtual channel indentifier
7:2	DT4	Data type indentifier
1:0	VC4	Virtual channel indentifier

1A04274C SENINF3_NCSI2_DI_CTRL_1 CSI2 Data Interleaving Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DT5_INTERLEAVING		VC5_INTERLEAVING						DT4_INTERLEAVING		VC4_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0

Bit(s)	Name	Description
10:9	DT5_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
8	VC5_INTERLEAVING	**Virtual channel identifier interleaving**
2:1	DT4_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
0	VC4_INTERLEAVING	**Virtual channel identifier interleaving**

1A042750 SENINF3_NCSI2_DPHY_RESYNC_CTL CSI2 DPHY Lane Resync Control 00000101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DPHY_RESYNC_CNT								DPHY_RESYNC_FLUSH_EN	DPHY_RESYNC_DATAOUT_OPTION	DPHY_BYPASS_LANE_RESYNC
Type						RW								RW	RW	RW
Reset						0	0	1						0	0	1

Bit(s)	Name	Description

Bit(s)	Name	Description
10:8	DPHY_RESYNC_CNT	Detect lane skew cycle count
2	DPHY_RESYNC_FLUSH_EN	Enables lane resync flush
1	DPHY_RESYNC_DATAOUT_OPTION	Data output option
0	DPHY_BYPASS_LANE_RESYNC	Bypass lane resync function

Module name: seninf3_ocsi2 Base address: (+1a042300h)

Address	Name	Width	Register Function
1A042360	SENINF3_OCSI2_CTRL	32	CSI2 Control Register
1A042364	SENINF3_OCSI2_DELAY	32	CSI2 Delay Control Register
1A042368	SENINF3_OCSI2_INTEN	32	CSI2 Interrupt Enable Register
1A04236C	SENINF3_OCSI2_INTSTA	32	CSI2 Interrupt Status Register
1A042370	SENINF3_OCSI2_ECCDBG	32	CSI2 ECC Debug Register
1A042374	SENINF3_OCSI2_CRCDBG	32	CSI2 CRC Debug Register
1A042378	SENINF3_OCSI2_DBG	32	CSI2 Debug Register
1A04237C	SENINF3_OCSI2_VER	32	CSI2 Version Code Register
1A042380	SENINF3_OCSI2_SHORT_INFO	32	CSI2 Short packet information Register
1A042384	SENINF3_OCSI2_LNFSM	32	CSI2 Lane FSM Register
1A042388	SENINF3_OCSI2_LNMUX	32	CSI2 Lane Mux Register
1A04238C	SENINF3_OCSI2_HSYNC_CNT	32	CSI2 Hsync Counter Register
1A042390	SENINF3_OCSI2_CAL	32	CSI2 Calibration Register
1A042394	SENINF3_OCSI2_DS	32	CSI2 Downsample Register
1A042398	SENINF3_OCSI2_VS	32	CSI2 Vsync Register
1A04239C	SENINF3_OCSI2_BIST	32	CSI2 BIST Register

1A042360 SENINF3_OCSI2_CTRL CSI2 Control Register 00002D80

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_BIST_CSI2_DATA_OK	CSI2_LANE_FSM_OK	CSI2_HS_FSM_OK	CSI2_BIST_DATA_OK	CSI2_BIST_START	CSI2_BIST_ERROR_COUNT								CSI2_DATA_FLOW		CSI2_ASYNC_OPTION
Type	RO	RO	RO	RO	RO	RO								RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_SYNC_CLR_EXTEND	CSI2_HSRXEN_PFOOT_CLR	CSI2_VSYNC_TYPE	CSI2_SW_RST	CSI2_SCLK4X_SEL	CSI2_SCLK_SEL	CSI2_ESC_EN	CSI2_SYNC_RST_EN	CSI2_LP11_RST_EN	CSI2_CLK_MISS_EN	CSI2_ED_SEL	CSI2_ECC_EN	DLANE3_EN	DLANE2_EN	DLANE1_EN	CSI2_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	1	0	1	1	0	1	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	CSI2_BIST_CSI2_DATA_OK	**CSI2 BIST CSI2 data ok**
30	CSI2_LANE_FSM_OK	**CSI2 BIST data lane FSM ok**
29	CSI2_HS_FSM_OK	**CSI2 BIST high speed FSM ok**
28	CSI2_BIST_DATA_OK	**CSI2 BIST DPHY data ok**
27	CSI2_BIST_START	**CSI2 BIST start status**
26:19	CSI2_BIST_ERROR_COUNT	**CSI2 bist test error count**
18:17	CSI2_DATA_FLOW	**CSI2 data flow** 0: Data packet 1: Generic long packet 2: All data packet
16	CSI2_ASYNC_OPTION	
15	CSI2_SYNC_CLR_EXTEND	
14	CSI2_HSRXEN_PFOOT_CLR	
13	CSI2_VSYNC_TYPE	**VSYNC type to CAM module** 0: High from short packet "frame start" to short packet "frame end" 1: 4T pulse after short packet "frame start"
12	CSI2_SW_RST	**CSI2 software reset, active high** 0: De-assert reset 1: Assert reset
11	CSI2_SCLK4X_SEL	**Selects CSI2 4x sample clock** 0: Invert 1: Does not invert csi2_clk from D-PHY
10	CSI2_SCLK_SEL	**Selects CSI2 sample clock** 0: Invert 1: Does not invert csi2_clk from D-PHY
9	CSI2_ESC_EN	**Enables CSI2 Escape mode**
8	CSI2_SYNC_RST_EN	**When this bit is set high, data high speed FSM will enter state "SYNC" whenever sync code is seen.** Used in case packet ends unexpectedly.
7	CSI2_LP11_RST_EN	**When this bit is set high, data/clk lane FSM will enter state "STOP" whenever LP-11 is seen.** Used in case low power and high speed state transition is unexpected.
6	CSI2_CLK_MISS_EN	**Enables high speed mode clock miss monitoring**
5	CSI2_ED_SEL	**Selects CSI2 header format**
4	CSI2_ECC_EN	**Enables CSI2 ECC**
3	DLANE3_EN	**Enables CSI2 3 data lane**
2	DLANE2_EN	**Enables CSI2 2 data lane**
1	DLANE1_EN	**Enables CSI2 1 data lane**
0	CSI2_EN	**Enables CSI2 0 data lane**

1A042364 SENINF3_CSI2_DELAY **CSI2 Delay Control Register** **000A0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LP2HS_DATA_TERM_DELAY								LP2HS_DATA_SETTLE_DELAY							
Type	RW								RW							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LP2HS_CLK_TERM_DELAY							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	LP2HS_DATA_TERM_DELAY	CSI2 data lane low power to high speed termination enable delay count
23:16	LP2HS_DATA_SETTLE_DELAY	CSI2 data lane low power to high speed sync code search delay
7:0	LP2HS_CLK_TERM_DELAY	CSI2 CLK lane low power to high speed termination enable delay count

1A042368 SENINF3_OCSI2_INTEN CSI2 Interrupt Enable Register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VCHANNEL_ID		CSI2_DATA_TYPE						CSI2_WC_NUMBER							
Type	RO		RO						RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_WC_NUMBER												CSI2SYNC_NONSYNC_IRQ_EN	ECC_CORRECT_IRQ_EN	ECC_ERR_IRQ_EN	CRC_ERR_IRQ_EN
Type	RO												RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0					0	1	1	1

Bit(s)	Name	Description
31:30	VCHANNEL_ID	CSI2 virtual channel identifier corrected by error correction if ECC is on
29:24	CSI2_DATA_TYPE	CSI2 long packet data type corrected by error correction if ECC is on
23:8	CSI2_WC_NUMBER	CSI2 long packet data size corrected by error correction if ECC is on
3	CSI2SYNC_NONSYNC_IRQ_EN	CSI2SYNC_NONSYNC_IRQ
2	ECC_CORRECT_IRQ_EN	Enables ECC correction interrupt
1	ECC_ERR_IRQ_EN	Enables ECC error interrupt
0	CRC_ERR_IRQ_EN	Enables CRC error interrupt

1A04236C SENINF3_OCSI2_INTSTA CSI2 Interrupt Status Register 00000070

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CSI2OUT_VSYNC	CSI2OUT_HSYNC				
Type											RO	RO				
Reset											0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CSI2_SPARE			CSI2	CSI2	ECC_	ECC_	CRC_

												_IRQ _CLR _SEL	SYNC _NON SYNC _IRQ	CORR ECT_ IRQ	ERR_ IRQ	ERR_ IRQ
Type									RW			RW	RO	RO	RO	RO
Reset									0	1	1	1	0	0	0	0

Bit(s)	Name	Description
21	CSI2OUT_VSYNC	**CSI2 vsync output to cam** Read only.
20	CSI2OUT_HSYNC	**CSI2 hsync output to cam** Read only.
7:5	CSI2_SPARE	**Spare register**
4	CSI2_IRQ_CLR_SEL	0: Read clear 1: Write clear
3	CSI2SYNC_NONSYNC_IRQ	**IRQ status bit to indicate that sync between different lanes is not sampled at the same time** Write clear.
2	ECC_CORRECT_IRQ	**ECC correction interrupt status**
1	ECC_ERR_IRQ	**ECC error interrupt status**
0	CRC_ERR_IRQ	**CRC error interrupt status**

1A042370 SENINF3_OCSI2_ECCDBG CSI2 ECC Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_ECCDB_BSEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_ECCDB_BSEL															CSI2_ECCDB_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CSI2_ECCDB_BSEL	**Selects CSI2 packet header error generation bit** To generate packet header error, set one of the 24 bits to 1. Because there is only one bit error can be corrected, only one bit of the 24 bits can be 1.
0	CSI2_ECCDB_EN	**Enables CSI2 packet header error generation**

1A042374 SENINF3_OCSI2_CRCDBG CSI2 CRC Debug Register 0000000E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_CRCDB_BSEL								CSI2_CRCDB_WSEL							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_CRCDB_WSEL								CSI2_SPARE							CSI2_CRCDB_EN

Type	RW								RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Bit(s)	Name	Description
31:24	CSI2_CRCDB_BSEL	**Selects CSI2 data error generation** Set to 1 to generate selected word bit error. *Note: Only word number selected by csi2_crcdb_wsel will be put error on it.*
23:8	CSI2_CRCDB_WSEL	**Selects CSI2 data error generation data word**
7:1	CSI2_SPARE	**Spare register**
0	CSI2_CRCDB_EN	**Enables CSI2 data error generation**

1A042378 SENINF3_OCSI2_DBG CSI2 Debug Register 00040820

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LN3_HSRXDB_EN	LN2_HSRXDB_EN	LN1_HSRXDB_EN	LN0_HSRXDB_EN	LNC_HSRXDB_EN	LN3_LPRXDB_EN	LN2_LPRXDB_EN	LN1_LPRXDB_EN	LN0_LPRXDB_EN	LNC_LPRXDB_EN		VCHANNEL_ID_EN	VCHANNEL1_ID		VCHANNEL0_ID	
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0		0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_CLK_LANE_CS					CSI2_DATA_HS_CS						CSI2_DBG_SRC_SEL				CSI2_DEBUG_ON
Type	RO					RO						RW				RW
Reset	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31	LN3_HSRXDB_EN	**Enables data lane 1 termination directly** For test only.
30	LN2_HSRXDB_EN	**Enables data lane 0 termination directly** For test only.
29	LN1_HSRXDB_EN	**Enables data lane 1 termination directly** For test only.
28	LN0_HSRXDB_EN	**Enables data lane 0 termination directly** For test only.
27	LNC_HSRXDB_EN	**Enables clock lane termination directly** For test only.
26	LN3_LPRXDB_EN	**Enables data lane 3 low power mode directly** For test only.
25	LN2_LPRXDB_EN	**Enables data lane 2 low power mode directly** For test only.
24	LN1_LPRXDB_EN	**Enables data lane 1 low power mode directly** For test only.
23	LN0_LPRXDB_EN	**Enables data lane 0 low power mode directly** For test only.
22	LNC_LPRXDB_EN	**Enables clock lane low power mode directly** For test only.
20	VCHANNEL_ID_EN	**Enables virtual channel**
19:18	VCHANNEL1_ID	**Virtual channel 1 ID**
17:16	VCHANNEL0_ID	**Virtual channel 0 ID**
15:11	CSI2_CLK_LANE_CS	**Clock lane FSM current state** 1: IDLE 2: STOP 4: HS_REQ

Bit(s)	Name	Description
		8: HS_PREP 16: HS_RX
10:5	CSI2_DATA_HS_CS	**Data high speed state** 1: IDLE 2: SYNC 4: PHEAD 8: PECC 16: PDATA 32: PFOOT
4:1	CSI2_DBG_SRC_SEL	**Selects CSI2 debug port source**
0	CSI2_DEBUG_ON	**Enables CSI2 debug** When CSI2 debug is enabled, CSI2 output raw data will include header to cam. *Note: To output CSI2 debug data,* *1. Set cam to JPEG interface mode ((CAM + 0024)[14], JPGINF_EN: 1).* *2. Set up Vsync polarity ((CAM + 0010)[7], VSPOL:1).* *3. Set up output type raw data output ((CAM + 0024)[21:20] OUTPATH_TYPE:0).* *4. Set up raw data type to 8-bit mode ((CAM + 0024)[24] OUTPATH_TYPE:0).* *5. Enable ISP data output to memory ((CAM + 0024)[16],OUT_PATH_EN:1).*

1A04237C SENINF3_OCSI2_VER **CSI2 Version Code Register** **20110815**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	YEAR															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MONTH								DATE							
Type	RO								RO							
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	1

Bit(s)	Name	Description
31:16	YEAR	Year code
15:8	MONTH	Month code
7:0	DATE	Date code

1A042380 SENINF3_OCSI2_SHORT_INFO **CSI2 Short packet information Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_FRAME_NO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_LINE_NO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	CSI2_FRAME_NO	Frame number information in short packet data type
15:0	CSI2_LINE_NO	Line number information in short packet data type

1A042384 SENINF3_OCSI2_LNFSM CSI2 Lane FSM Register 01010101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CSI2_DATA_LN3_CS								CSI2_DATA_LN2_CS						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CSI2_DATA_LN1_CS								CSI2_DATA_LN0_CS						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1

Bit(s)	Name	Description
30:24	CSI2_DATA_LN3_CS	**Data lane 3 FSM current state**
22:16	CSI2_DATA_LN2_CS	**Data lane 2 FSM current state**
14:8	CSI2_DATA_LN1_CS	**Data lane 1 FSM current state**
6:0	CSI2_DATA_LN0_CS	**Data lane 0 FSM current state** 1: IDLE 2: STOP 4: HS_REQ 8: HS_PREP 16: HS_TERM 32: HS_RX 64: HS_ESC

1A042388 SENINF3_OCSI2_LNMUX CSI2 Lane Mux Register 000000E4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CSI2_DATA_LN3_MUX		CSI2_DATA_LN2_MUX		CSI2_DATA_LN1_MUX		CSI2_DATA_LN0_MUX	
Type									RW		RW		RW		RW	
Reset									1	1	1	0	0	1	0	0

Bit(s)	Name	Description
7:6	CSI2_DATA_LN3_MUX	**CSI2 data lane mux** 0: LANE 0 1: LANE 1 2: LANE 2 3: LANE 3
5:4	CSI2_DATA_LN2_MUX	**CSI2 data lane mux** 0: LANE 0 1: LANE 1 2: LANE 2

Bit(s)	Name	Description
		3: LANE 3
3:2	CSI2_DATA_LN1_MUX	**CSI2 data lane mux** 0: LANE 0 1: LANE 1 2: LANE 2 3: LANE 3
1:0	CSI2_DATA_LN0_MUX	**CSI2 data lane mux** 0: LANE 0 1: LANE 1 2: LANE 2 3: LANE 3

1A04238C SENINF3_OCSI2_HSYNC_CNT CSI2 Hsync Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CSI2_HSYNC_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	CSI2_HSYNC_CNT	CSI2 hsync counter

1A042390 SENINF3_OCSI2_CAL CSI2 Calibration Register 01010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2 _CAL _CNT _2								CSI2_CAL_CNT_1							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										CSI2_CAL_STAT E						CSI2 _CAL _EN
Type										RO						RW
Reset										0	0	0				0

Bit(s)	Name	Description
31:24	CSI2_CAL_CNT_2	**CSI2 calibration counter 2 (term enable to Sync)** Settle delay <= CSI2 Calibration Counter 2 - Term Delay - 3 byte clk - 3 bclk - 1 bclk
23:16	CSI2_CAL_CNT_1	**CSI2 calibration counter 1 (term enable to HS00)** Term delay <= CSI2 Calibration Counter 1 - 2 byte clk - 3 bclk
6:4	CSI2_CAL_STATE	**CSI2 calibration current state**
0	CSI2_CAL_EN	**Enables CSI2 calibration**

1A042394 SENINF3_OCSI2_DS CSI2 Downsample Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CSI2_DS_CTRL		CSI2_DS_EN
Type														RW		RW
Reset														0	0	0

Bit(s)	Name	Description
2:1	CSI2_DS_CTRL	**Controls CSI2 downsample factor** 0: 1 1: 1/2 2: 1/4 3: 1/8
0	CSI2_DS_EN	**Enables CSI2 downsample**

1A042398 SENINF3_OCSI2_VS CSI2 Vsync Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CSI2_VS_CTRL	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	CSI2_VS_CTRL	**Extends CSI2 vsync period** 0: 4T 1: 8T 2: 12T 3: 16T

1A04239C SENINF3_OCSI2_BIST CSI2 BIST Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CSI2_BIST_LNR3_D	CSI2_BIST_LNR2_D	CSI2_BIST_LNR1_D	CSI2_BIST_LNR0_D

													ATA_OK	ATA_OK	ATA_OK	ATA_OK
Type													RO	RO	RO	RO
Reset													0	0	0	0

Bit(s)	Name	Description
3	CSI2_BIST_LNR3_DATA_OK	CSI2 BIST Lane 3 DPHY data ok
2	CSI2_BIST_LNR2_DATA_OK	CSI2 BIST Lane 2 DPHY data ok
1	CSI2_BIST_LNR1_DATA_OK	CSI2 BIST Lane 1 DPHY data ok
0	CSI2_BIST_LNR0_DATA_OK	CSI2 BIST Lane 0 DPHY data ok

Module name: SENINF3_TG Base address: (+1a042600h)

Address	Name	Width	Register Function
1A042600	SENINF_TG3_PH_CNT	32	TG Phase Counter
1A042604	SENINF_TG3_SEN_CK	32	TG Sensor Clock Divider
1A042608	SENINF_TG3_TM_CTL	32	TM Contorl
1A04260C	SENINF_TG3_TM_SIZE	32	TM Size
1A042610	SENINF_TG3_TM_CLK	32	TM Clock
1A042614	SENINF_TG3_TM_STP	32	TG1_TM_STP

1A042600 SENINF_TG3_PH_CNT TG Phase Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PCEN		ADCLK_EN	CLKPOL												
Type	RW		RW	RW												
Reset	0		0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CAM_PCLK_INV	PAD_PCLK_INV	EXT_PWRDN	EXT_RST		CLKFL_POL	TGCLK_SEL	
Type									RW	RW	RW	RW		RW	RW	
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
31	PCEN	**TG phase counter enable control**
29	ADCLK_EN	**Enables sensor master clock (mclk) output to sensor**
28	CLKPOL	**Controls sensor master clock polarity**
7	CAM_PCLK_INV	**Inverts pixel clock in CAM**
6	PAD_PCLK_INV	**Inverts pixel clock in PAD side**
5	EXT_PWRDN	**Powers down sensor**
4	EXT_RST	**Resets sensor**
2	CLKFL_POL	**Sensor clock falling edge polarity**
1:0	TGCLK_SEL	**Selects sensor master clock** 0: isp_clk 1: cam_pll

Bit(s)	Name	Description
		2: 3rd clock source

1A042604 SENINF_TG3_SEN_CK **TG Sensor Clock Divider** **00010001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CLKCNT					
Type											RW					
Reset											0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			CLKRS								CLKFL					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	1

Bit(s)	Name	Description
21:16	CLKCNT	**Controls sensor master clock frequency divider** Sensor master clock = ISP_clock/(CLKCNT+1); CLKCNT >=1
13:8	CLKRS	**Controls sensor master clock rising edge**
5:0	CLKFL	**Controls sensor master clock falling edge**

1A042608 SENINF_TG3_TM_CTL **TM Contorl** **00300004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									TM_DUMMYPXL							
Type									RW							
Reset									0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TM_VSYNC								TM_PAT					TM_FMT	TM_RST	TM_EN
Type	RW								RW					RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0		1	0	0

Bit(s)	Name	Description
23:16	TM_DUMMYPXL	**Test model horizontal dummy pixel**
15:8	TM_VSYNC	**VSYNC high duration in line unit (TM_DUMMYPXL + PIXEL)**
7:4	TM_PAT	**Test model decision** 0: White 1: Yellow 2: Cyan 3: Green 4: Magenta 5: Red 6: Blue 7: Black 8: Horizontal gray level (Unit 1) 9: Horizontal gray level (Unit 4) 10: Horizontal gray level (take 1024 pixel as one period) (only bayer) 11: Vertical gray level (Unit 1)

Bit(s)	Name	Description
		12: Static horizontal color bar 13: Static vertical color bar (only bayer) 14: R,G,B,W flashes every two frames (only bayer) 15: Dynamic horizontal colorbar (only bayer)
2	TM_FMT	**Test model format** 0: Bayer 1: YUV
1	TM_RST	**Resets test model** 1'b0: Does not reset test model 1'b1: Reset test model
0	TM_EN	**Enables test model** 0: Disable 1: Enable

1A04260C SENINF_TG3_TM_SIZE **TM Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			TM_LINE													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TM_PXL												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	TM_LINE	Test model line number
12:0	TM_PXL	Test model pixel number (HSYNC high duration in pixel unit)

1A042610 SENINF_TG3_TM_CLK **TM Clock** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		TM_CLRBAR_IDX					TM_CLRBAR_OFT									
Type		RW					RW									
Reset		0	0	0			0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TM_CLK_CNT			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
30:28	TM_CLRBAR_IDX	**Test model colorbar index offset** 0: White 1: Yellow 2: Cyan 3: Green 4: Magenta 5: Red

Bit(s)	Name	Description
		6: Blue 7: Black
25:16	TM_CLRBAR_OFT	**Test model colorbar offset** This value should be smaller than (TM_PXL>>3).
3:0	TM_CLK_CNT	**Test model clock divided count**

1A042614 SENINF_TG3_TM_STP TG1_TM_STP 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TG1_TM_STP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TG1_TM_STP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TG1_TM_STP	Time stamp divider

Module name: seninf4 Base address: (+1a043200h)

Address	Name	Width	Register Function
1A043200	SENINF4_CTRL	32	SENINF 4 Control Register
1A043204	SENINF4_CTRL_EXT	32	SENINF 4 Control Register Extend
1A043208	SENINF4_ASYNC_CTRL	32	SENINF 4 Async Control Register

1A043200 SENINF4_CTRL SENINF 4 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PAD2CAM_DATA_SEL							SENINF_DEBUG_SEL							
Type		RW							RW							
Reset		0	0	0					0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_SRC_SEL							CSI3_SW_RST	CSI2_SW_RST	SCAM_SW_RST	TEST_MODEL_SW_RST	CKGEN_SW_RST	CCIR_SW_RST	OCSI2_SW_RST	NCSI2_SW_RST	SENINF_EN
Type	RW							RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:28	PAD2CAM_DATA_SEL	0: PAD2CAM_DATA[9:0] 3: {PAD2CAM_DATA[7:0],2'b00} 4: {PAD2CAM_DATA[9:2]2'b00}

Bit(s)	Name	Description
23:20	SENINF_DEBUG_SEL	**Selects SENINF1 debug**
15:12	SENINF_SRC_SEL	**Selects SENINF input source** 0: CSI2 1: Test model 2: CCIR656 3: Parallel sensor 4: Serial sensor 8: NCSI2
8	CSI3_SW_RST	**CSI3 software reset, active high** 0: De-assert reset 1: Assert reset
7	CSI2_SW_RST	**CSI2 software reset, active high** 0: De-assert reset 1: Assert reset
6	SCAM_SW_RST	**SCAM software reset, active high** 0: De-assert reset 1: Assert reset
5	TEST_MODEL_SW_RST	**Test model software reset, active high** 0: De-assert reset 1: Assert reset
4	CKGEN_SW_RST	**CKGEN software reset, active high** 0: De-assert reset 1: Assert reset
3	CCIR_SW_RST	**CCIR software reset, active high** 0: De-assert reset 1: Assert reset
2	OCSI2_SW_RST	**OCSI2 software reset, active high** 0: De-assert reset 1: Assert reset
1	NCSI2_SW_RST	**NCSI2 software reset, active high** 0: De-assert reset 1: Assert reset
0	SENINF_EN	

1A043204 SENINF4_CTRL_EXT **SENINF 4 Control Register Extend** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															SENINF_SRC_SEL_EXT	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SENINF_CSI3_IP_EN	SENINF_CSI2_IP_EN	SENINF_NCSI2_IP_EN	SENINF_SCAM_IP_EN			SENINF_TESTMDL_IP_EN	SENINF_OCSI2_IP_EN
Type									RW	RW	RW	RW			RW	RW
Reset									0	0	0	0			0	0

Bit(s)	Name	Description
17:16	SENINF_SRC_SEL_EXT	[0] Set 1'b1 for CSI2 [1] Set 1'b1 for CSI3 For constraints only.

Bit(s)	Name	Description
7	SENINF_CSI3_IP_EN	**Enables CSI3 IP**
6	SENINF_CSI2_IP_EN	**Enables CSI2 IP**
5	SENINF_NCSI2_IP_EN	**Enables NCSI2 IP**
4	SENINF_SCAM_IP_EN	**Enables SCAM IP**
1	SENINF_TESTMDL_IP_EN	**Enables TESTMDL IP**
0	SENINF_OCSI2_IP_EN	**Enables OCSI2 IP**

1A043208 SENINF4_ASYNC_CTRL **SENINF 4 Async Control Register** **1B1F0002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			FIFO_FLUSH_EN								FIFO_PUSH_EN					
Type			RW								RW					
Reset			0	1	1	0	1	1			0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SENINF_HSYNC_POL	SENINF_VSYNC_POL	SENINF_HSYNC_MASK	SENINF_ASYNC_FIFO_RST
Type													RW	RW	RW	RW
Reset													0	0	1	0

Bit(s)	Name	Description
29:24	FIFO_FLUSH_EN	**Normal mode: 6'b011011** JPEG two pixel mode: 6'b011000
21:16	FIFO_PUSH_EN	**Normal mode: 6'b011111** JPEG two pixel mode : 6'b011110
3	SENINF_HSYNC_POL	**SENINF HSYNC polarity**
2	SENINF_VSYNC_POL	**SENINF VSYNC polarity**
1	SENINF_HSYNC_MASK	**Masks hsync** 0: Send hsync when vsync = 1 1: Does not send hsync when vsync = 1
0	SENINF_ASYNC_FIFO_RST	**Async FIFO software reset**

Module name: seninf4_csi2 Base address: (+1a043a00h)

Address	Name	Width	Register Function
1A043A00	**SENINF4_CSI2_CTL**	32	CSI2 Function Enable
1A043A04	**SENINF4_CSI2_LNRC_TIMING**	32	CSI2 Clock Lane Timing Parameters
1A043A08	**SENINF4_CSI2_LNRD_TIMING**	32	CSI2 Data Lane Timing Parameters
1A043A0C	**SENINF4_CSI2_DPCM**	32	CSI2 DPCM Parameters
1A043A10	**SENINF4_CSI2_INT_EN**	32	CSI2 Interrupt Enable
1A043A14	**SENINF4_CSI2_INT_STATUS**	32	CSI2 Interrupt status
1A043A18	**SENINF4_CSI2_DGB_SEL**	32	CSI2 Debug Selection
1A043A1C	**SENINF4_CSI2_D**	32	CSI2 Debug Port

Address	Name	Width	Register Function
	BG_PORT		
1A043A20	SENINF4_CSI2_SPARE0	32	SPARE0
1A043A24	SENINF4_CSI2_SPARE1	32	SPARE1
1A043A28	SENINF4_CSI2_LNRC_FSM	32	CSI2 Clock Lane RX FSM
1A043A2C	SENINF4_CSI2_LNRD_FSM	32	CSI2 Data Lane RX FSM
1A043A30	SENINF4_CSI2_FRAME_LINE_NUM	32	CSI2 Frame/Line Number
1A043A34	SENINF4_CSI2_GENERIC_SHORT	32	CSI2 Generic Short Packet
1A043A38	SENINF4_CSI2_HSRX_DBG	32	CSI2 HSRX Enable
1A043A3C	SENINF4_CSI2_DI	32	CSI2 Data Interleaving Parameters
1A043A40	SENINF4_CSI2_HS_TRAIL	32	CSI2 HS Trail Timing Parameters
1A043A44	SENINF4_CSI2_DI_CTRL	32	CSI2 Data Interleaving Control
1A043A48	SENINF4_CSI2_LNRD_FSM_X	32	CSI2 Data Lane RX FSM Other
1A043A4C	SENINF4_CSI2_DETECT_CON1	32	CSI2 CPHY Detect Control Sync
1A043A50	SENINF4_CSI2_DETECT_CON2	32	CSI2 CPHY Detect Control Escape
1A043A54	SENINF4_CSI2_DETECT_CON3	32	CSI2 CPHY Detect Control Post
1A043A58	SENINF4_CSI2_RLR0_CON0	32	CSI2 CPHY RLR0 CON0
1A043A5C	SENINF4_CSI2_RLR1_CON0	32	CSI2 CPHY RLR1 CON0
1A043A60	SENINF4_CSI2_RLR2_CON0	32	CSI2 CPHY RLR2 CON0
1A043A64	SENINF4_CSI2_RLR_CON0	32	CSI2 CPHY RLR CON0
1A043A68	SENINF4_CSI2_MUX_CON	32	CSI2 Pin Pux Sel
1A043A6C	SENINF4_CSI2_DETECT_DBG0	32	CSI2 Detection Debug 0
1A043A70	SENINF4_CSI2_DETECT_DBG1	32	CSI2 Detection Debug 1
1A043A74	SENINF4_CSI2_RESYNC_MERGE_CTL	32	CSI2 Lane Resync Merge Control
1A043A78	SENINF4_CSI2_CTRL_TRIO_MUX	32	CSI2 Control Trio Mux
1A043A7C	SENINF4_CSI2_CTRL_TRIO_CON	32	CSI2 Control Trio Config
1A043A80	SENINF4_FIX_ADDR_CPHY0_DBG	32	cphy_fix_point_addr_cphy0_debug
1A043A84	SENINF4_FIX_ADDR_CPHY1_DBG	32	cphy_fix_point_addr_cphy1_debug
1A043A88	SENINF4_FIX_AD	32	cphy_fix_point_addr_cphy2_debug

Address	Name	Width	Register Function
	DR_CPHY2_DBG		
1A043A8C	SENINF4_FIX_ADDR_DBG	32	cphy_fix_point_addr_debug
1A043A90	SENINF4_WIRE_STATE_DECODE_CPHY0_DBG0	32	cphy_wire_state_decode_cphy0_debug0
1A043A94	SENINF4_WIRE_STATE_DECODE_CPHY0_DBG1	32	cphy_wire_state_decode_cphy0_debug1
1A043A98	SENINF4_WIRE_STATE_DECODE_CPHY1_DBG0	32	cphy_wire_state_decode_cphy1_debug0
1A043A9C	SENINF4_WIRE_STATE_DECODE_CPHY1_DBG1	32	cphy_wire_state_decode_cphy1_debug1
1A043AA0	SENINF4_WIRE_STATE_DECODE_CPHY2_DBG0	32	cphy_wire_state_decode_cphy2_debug0
1A043AA4	SENINF4_WIRE_STATE_DECODE_CPHY2_DBG1	32	cphy_wire_state_decode_cphy2_debug1
1A043AA8	SENINF4_SYNC_RESYNC_CTL	32	CSI2 Sync Resync Control
1A043AAC	SENINF4_POST_DETECT_CTL	32	CSI2 Post Detect Control
1A043AB0	SENINF4_WIRE_STATE_DECODE_CONFIG	32	CSI2 Wire State Decode Config
1A043AB4	SENINF4_CSI2_CPHY_LNRD_FSM	32	CPHY Data Lane RX FSM
1A043AB8	SENINF4_FIX_ADDR_CPHY0_DBG0	32	cphy_fix_point_addr_cphy0_debug0
1A043ABC	SENINF4_FIX_ADDR_CPHY0_DBG1	32	cphy_fix_point_addr_cphy0_debug1
1A043AC0	SENINF4_FIX_ADDR_CPHY0_DBG2	32	cphy_fix_point_addr_cphy0_debug2
1A043AC4	SENINF4_FIX_ADDR_CPHY1_DBG0	32	cphy_fix_point_addr_cphy1_debug0
1A043AC8	SENINF4_FIX_ADDR_CPHY1_DBG1	32	cphy_fix_point_addr_cphy1_debug1
1A043ACC	SENINF4_FIX_ADDR_CPHY1_DBG2	32	cphy_fix_point_addr_cphy1_debug2
1A043AD0	SENINF4_FIX_ADDR_CPHY2_DBG0	32	cphy_fix_point_addr_cphy2_debug0
1A043AD4	SENINF4_FIX_ADDR_CPHY2_DBG1	32	cphy_fix_point_addr_cphy2_debug1
1A043AD8	SENINF4_FIX_ADDR_CPHY2_DBG2	32	cphy_fix_point_addr_cphy2_debug2
1A043ADC	SENINF4_FIX_ADDR_DBG0	32	cphy_fix_point_addr_debug0
1A043AE0	SENINF4_FIX_ADDR_DBG1	32	cphy_fix_point_addr_debug1
1A043AE4	SENINF4_FIX_ADDR_DBG2	32	cphy_fix_point_addr_debug2
1A043AE8	SENINF4_CSI2_M	32	CSI2 Packet Structure

Address	Name	Width	Register Function
	ODE		
1A043AF0	SENINF4_CSI2_DI_EXT	32	CSI2 Data Interleaving Parameters Extend
1A043AF4	SENINF4_CSI2_DI_CTRL_EXT	32	CSI2 Data Interleaving Control Extend
1A043AF8	SENINF4_CSI2_CPHY_LOOPBACK	32	CSI2 SW Trigger sync_init and hs_en
1A043B00	SENINF4_CSI2_PROGSEQ_0	32	CSI2 CPHY Program sequence_0
1A043B04	SENINF4_CSI2_PROGSEQ_1	32	CSI2 CPHY Program sequence_1
1A043B10	SENINF4_CSI2_INT_EN_EXT	32	CSI2 Interrupt Enable Extend
1A043B14	SENINF4_CSI2_INT_STATUS_EXT	32	CSI2 Interrupt Status Extend
1A043B18	SENINF4_CSI2_CPHY_FIX_POINT_RST	32	CSI2 CPHY Fix Point Reset Mode
1A043B20	SENINF4_CSI2_DPHY_RESYNC_CTL	32	CSI2 DPHY Lane Resync Control

1A043A00 SENINF4_CSI2_CTL **CSI2 Function Enable** **01886160**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA_LANE7_EN	DATA_LANE6_EN	VS_OUT_CYCLE_NUMBER		CLOCK_HS_OPTION	REF_SYNC_DET_EN	HS_TRAIL_EN	ASYNC_FIFO_RST_SCH		SYNC_DET_BITSWAP_EN	SYNC_DET_EN	SYNC_DET_SCHEME	FLUSH_MODE			ED_SEL
Type	RW	RW	RW		RW	RW	RW	RW		RW	RW	RW	RW			RW
Reset	0	0	0	0	0	0	0	1	1	0	0	0	1	0		0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VS_TYPE	BYTE2PIXEL_EN	IMAGE_PACKET_EN	GENERIC_LONG_PACKET_EN	DATA_LANE5_EN	DATA_LANE4_EN	HS_END_EN	HS_PRPR_EN	HSRX_DET_EN	CRC_EN	ECC_EN	CLOCK_LANE_EN	DATA_LANE3_EN	DATA_LANE2_EN	DATA_LANE1_EN	DATA_LANE0_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	1	1	0	0	0	0	1	0	1	1	0	0	0	0	0

Bit(s)	Name	Description
31	DATA_LANE7_EN	**Enables data lane 7**
30	DATA_LANE6_EN	**Enables data lane 6**
29:28	VS_OUT_CYCLE_NUMBER	0: 4T 1: 8T
27	CLOCK_HS_OPTION	0: Enable clock lane HS based on LP11, LP01, LP00 1: Enable clock lane HS based on LP00
26	REF_SYNC_DET_EN	**Reference sync detect signal to do analog sync**
25	HS_TRAIL_EN	**Extends HS trail**
24:23	ASYNC_FIFO_RST_SCH	
22	SYNC_DET_BITSWAP_EN	
21	SYNC_DET_EN	**Enables sync sequence detection**
20	SYNC_DET_SCHEME	0: B8

Bit(s)	Name	Description
		1: 101110
19:18	FLUSH_MODE	0: Disable 1: Flush at first cycle of LP11 2: Flush at LP11 3: Reserved
16	ED_SEL	0: {WCH,WCL,DI} 1: {DI,WCL,WCH}
15	VS_TYPE	**VS type** 0: 4T 1: Frame start to frame end
14	BYTE2PIXEL_EN	**Byte 2 pixel conversion**
13	IMAGE_PACKET_EN	**Image data types**
12	GENERIC_LONG_PACKET_EN	**Generic long packet data types**
11	DATA_LANE5_EN	**Enables data lane 6**
10	DATA_LANE4_EN	**Enables data lane 5**
9	HS_END_EN	**Enable HS_EX reset at packet end**
8	HS_PRPR_EN	**Enables RX_HS_PRPR state**
7	HSRX_DET_EN	**Enables HSRX termination auto-detection flow**
6	CRC_EN	**Enables checksum**
5	ECC_EN	**Enables packet header ECC**
4	CLOCK_LANE_EN	**Enables clock lane**
3	DATA_LANE3_EN	**Enables data lane 3**
2	DATA_LANE2_EN	**Enables data lane 2**
1	DATA_LANE1_EN	**Enables data lane 1**
0	DATA_LANE0_EN	**Enables data lane 0**

1A043A04 SENINF4_CSI2_LNRC_TIMING — CSI2 Clock Lane Timing Parameters — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLOCK_SETTLE_PARAMETER								CLOCK_TERM_PARAMETER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	CLOCK_SETTLE_PARAMETER	TD_SETTLE parameter
7:0	CLOCK_TERM_PARAMETER	TD_TERM_EN parameter

1A043A08 SENINF4_CSI2_LNRD_TIMING — CSI2 Data Lane Timing Parameters — 00002000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_SETTLE_PARAMETER								DATA_TERM_PARAMETER							

Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	DATA_SETTLE_PARAMETER	TD_SETTLE parameter
7:0	DATA_TERM_PARAMETER	TD_TERM_EN parameter

1A043A0C SENINF4_CSI2_DPCM **CSI2 DPCM Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DI_2A_DPCM_EN	DI_37_DPCM_EN	DI_36_DPCM_EN	DI_35_DPCM_EN	DI_34_DPCM_EN	DI_33_DPCM_EN	DI_32_DPCM_EN	DI_31_DPCM_EN	DI_30_DPCM_EN				DPCM_MODE			
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW				RW			
Reset	0	0	0	0	0	0	0	0	0				0	0	0	0

Bit(s)	Name	Description
15	DI_2A_DPCM_EN	**Enables DPCM**
14	DI_37_DPCM_EN	**Enables DPCM**
13	DI_36_DPCM_EN	**Enables DPCM**
12	DI_35_DPCM_EN	**Enables DPCM**
11	DI_34_DPCM_EN	**Enables DPCM**
10	DI_33_DPCM_EN	**Enables DPCM**
9	DI_32_DPCM_EN	**Enables DPCM**
8	DI_31_DPCM_EN	**Enables DPCM**
7	DI_30_DPCM_EN	**Enables DPCM**
3:0	DPCM_MODE	0: 10-8-10

1A043A10 SENINF4_CSI2_INT_EN **CSI2 Interrupt Enable** **1FFFBFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_WCLR_EN			TRIO2_ESCAPE_CODE_DETECT	TRIO1_ESCAPE_CODE_DETECT	TRIO0_ESCAPE_CODE_DETECT	TRIO2_RESYNC_FIFO_OVERFLOW	TRIO1_RESYNC_FIFO_OVERFLOW	TRIO0_RESYNC_FIFO_OVERFLOW	ERR_LANE_RESYNC	ERR_FRAME_SYNC_S5	ERR_FRAME_SYNC_S4	ERR_FRAME_SYNC_S3	ERR_FRAME_SYNC_S2	ERR_FRAME_SYNC_S1	ERR_FRAME_SYNC_S0
Type	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0			1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FE	GS	LS	FS	ERR_SOT_SYNC_HS_LNRD3	ERR_SOT_SYNC_HS_LNRD2	ERR_SOT_SYNC_HS_LNRD1	ERR_SOT_SYNC_HS_LNRD0	ERR_MULTI_LANE_SYNC	ERR_AFIFO	ERR_CRC	ERR_ECC_DOUBLE	ERR_ECC_CORRECTED	ERR_ECC_NO_ERROR	ERR_ID	ERR_FRAME_SYNC
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	INT_WCLR_EN	Enables interrupt write clear
28	TRIO2_ESCAPE_CODE_DETECT	Enables TRIO2_ESCAPE_CODE_DETECT interrupt
27	TRIO1_ESCAPE_CODE_DETECT	Enables TRIO1_ESCAPE_CODE_DETECT interrupt
26	TRIO0_ESCAPE_CODE_DETECT	Enables TRIO0_ESCAPE_CODE_DETECT interrupt
25	TRIO2_RESYNC_FIFO_OVERFLOW	Enables TRIO2_RESYNC_FIFO_OVERFLOW interrupt
24	TRIO1_RESYNC_FIFO_OVERFLOW	Enables TRIO1_RESYNC_FIFO_OVERFLOW interrupt
23	TRIO0_RESYNC_FIFO_OVERFLOW	Enables TRIO0_RESYNC_FIFO_OVERFLOW interrupt
22	ERR_LANE_RESYNC	Enables ERR_LANE_RESYNC interrupt
21	ERR_FRAME_SYNC_S5	Enables ERR_FRAME_SYNC interrupt
20	ERR_FRAME_SYNC_S4	Enables ERR_FRAME_SYNC interrupt
19	ERR_FRAME_SYNC_S3	Enables ERR_FRAME_SYNC interrupt
18	ERR_FRAME_SYNC_S2	Enables ERR_FRAME_SYNC interrupt
17	ERR_FRAME_SYNC_S1	Enables ERR_FRAME_SYNC interrupt
16	ERR_FRAME_SYNC_S0	Enables ERR_FRAME_SYNC interrupt
15	FE	Enables frame end interrupt
14	GS	Enables generic short packet interrupt
13	LS	Enables line start interrupt
12	FS	Enables frame start interrupt
11	ERR_SOT_SYNC_HS_LNRD3	Enables ERR_SOT_SYNC_HS interrupt
10	ERR_SOT_SYNC_HS_LNRD2	Enables ERR_SOT_SYNC_HS interrupt
9	ERR_SOT_SYNC_HS_LNRD1	Enables ERR_SOT_SYNC_HS interrupt
8	ERR_SOT_SYNC_HS_LNRD0	Enables ERR_SOT_SYNC_HS interrupt
7	ERR_MULTI_LANE_SYNC	Enables ERR_MULTI_LANE_SYNC interrupt
6	ERR_AFIFO	Enables ERR_AFIFO interrupt
5	ERR_CRC	Enables ERR_CRC interrupt
4	ERR_ECC_DOUBLE	Enables ERR_ECC_DOUBLE interrupt
3	ERR_ECC_CORRECTED	Enables ERR_ECC_CORRECTED interrupt
2	ERR_ECC_NO_ERROR	ERR_ECC_NO_ERROR interrupt
1	ERR_ID	Enables ERR_ID interrupt
0	ERR_FRAME_SYNC	Enables ERR_FRAME_SYNC interrupt

1A043A14 SENINF4_CSI2_INT_STATUS **CSI2 Interrupt status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				TRIO2_ESCAPE_CODE_DETECT_STA	TRIO1_ESCAPE_CODE_DETECT_STA	TRIO0_ESCAPE_CODE_DETECT_STA	TRIO2_RESYNC_FIFO_OVERFLOW_STA	TRIO1_RESYNC_FIFO_OVERFLOW_STA	TRIO0_RESYNC_FIFO_OVERFLOW_STA	ERR_LANE_RESYNC_STA	ERR_FRAME_SYNC_S5_STA	ERR_FRAME_SYNC_S4_STA	ERR_FRAME_SYNC_S3_STA	ERR_FRAME_SYNC_S2_STA	ERR_FRAME_SYNC_S1_STA	ERR_FRAME_SYNC_S0_STA
Type				RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FE_STA	GS_STA	LS_STA	FS_STA	ERR_SOT_SYNC_HS_LNRD3_STA	ERR_SOT_SYNC_HS_LNRD2_STA	ERR_SOT_SYNC_HS_LNRD1_STA	ERR_SOT_SYNC_HS_LNRD0_STA	ERR_MULTI_LANE_SYNC_STA	ERR_AFIFO_STA	ERR_CRC_STA	ERR_ECC_DOUBLE_STA	ERR_ECC_CORRECTED_STA	ERR_ECC_NO_ERROR_STA	ERR_ID_STA	ERR_FRAME_SYNC_STA
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	TRIO2_ESCAPE_CODE_DETECT_STA	**Asserted when the escape code of trio2 is detected**
27	TRIO1_ESCAPE_CODE_DETECT_STA	**Asserted when the escape code of trio1 is detected**
26	TRIO0_ESCAPE_CODE_DETECT_STA	**Asserted when the escape code of trio0 is detected**
25	TRIO2_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of CPHY trio2 is overflowed**
24	TRIO1_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of CPHY trio1 is overflowed**
23	TRIO0_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of CPHY trio0 is overflowed**
22	ERR_LANE_RESYNC_STA	**Asserted when CPHY lane sync detect time is longer than set resync cycles**
21	ERR_FRAME_SYNC_S5_STA	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
20	ERR_FRAME_SYNC_S4_STA	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
19	ERR_FRAME_SYNC_S3_STA	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
18	ERR_FRAME_SYNC_S2_STA	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
17	ERR_FRAME_SYNC_S1_STA	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
16	ERR_FRAME_SYNC_S0_STA	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
15	FE_STA	**Frame end interrupt**
14	GS_STA	**Generic Short Packet interrupt enable**
13	LS_STA	**Line start interrupt**
12	FS_STA	**Frame start interrupt**
11	ERR_SOT_SYNC_HS_LNRD3_STA	**Asserted when proper synchronization cannot be expected**
10	ERR_SOT_SYNC_HS_LNRD2_STA	**Asserted when proper synchronization cannot be expected**
9	ERR_SOT_SYNC_HS_LNRD1_STA	**Asserted when proper synchronization cannot be expected**
8	ERR_SOT_SYNC_HS_LNRD0_STA	**Asserted when proper synchronization cannot be expected**
7	ERR_MULTI_LANE_SYNC_STA	**Asserted when multiple lane synchronization fails**
6	ERR_AFIFO_STA	**Asserted when error occurs in asynchronous FIFO**
5	ERR_CRC_STA	**Asserted when computed CRC code is different from received CRC code**
4	ERR_ECC_DOUBLE_STA	**Asserted when an ECC syndrome is computed and two bit errors are detected in the received packet header**
3	ERR_ECC_CORRECTED_STA	**Asserted when an ECC syndrome is computed and a single bit error in the packet header is detected and corrected**
2	ERR_ECC_NO_ERROR_STA	**Asserted when an ECC syndrome is computed and the result is zero indicating a packet header that is considered to be without errors or has more than two bit errors** CSI-2's ECC mechanism cannot detect this type of error.
1	ERR_ID_STA	**Asserted whean a packet header is decoded with an unrecognized or unimplemented data ID**
0	ERR_FRAME_SYNC_STA	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**

1A043A18 SENINF4_CSI2_DGB_SEL CSI2 Debug Selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_EN															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DEBUG_SEL							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	DEBUG_EN	Enables debug
7:0	DEBUG_SEL	Selects debug

1A043A1C SENINF4_CSI2_DBG_PORT CSI2 Debug Port 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CTL_DBG_PORT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	CTL_DBG_PORT	Debug port

1A043A20 SENINF4_CSI2_SPARE0 SPARE0 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	SPARE0	Spare register

1A043A24 SENINF4_CS SPARE1 00000000

I2_SPARE1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE1	Spare register

1A043A28 SENINF4_CSI2_LNRC_FSM CSI2 Clock Lane RX FSM 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											LNRC_RX_FSM					
Type											RO					
Reset											0	0	0	0	0	1

Bit(s)	Name	Description
5:0	LNRC_RX_FSM	RX FSM of clock lane

1A043A2C SENINF4_CSI2_LNRD_FSM CSI2 Data Lane RX FSM 01010101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LNRD3_RX_FSM								LNRD2_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		LNRD1_RX_FSM								LNRD0_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1

Bit(s)	Name	Description
30:24	LNRD3_RX_FSM	RX FSM of data lane 3
22:16	LNRD2_RX_FSM	RX FSM of data lane 2
14:8	LNRD1_RX_FSM	RX FSM of data lane 1
6:0	LNRD0_RX_FSM	RX FSM of data lane 0

1A043A30 SENINF4_CSI2_FRAME_LINE_NUM — CSI2 Frame/Line Number — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LINE_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FRAME_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	LINE_NUM	Line number
15:0	FRAME_NUM	Frame number

1A043A34 SENINF4_CSI2_GENERIC_SHORT — CSI2 Generic Short Packet — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GENERIC_SHORT_PACKET_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											GENERIC_SHORT_PACKET_DT						
Type											RO					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
31:16	GENERIC_SHORT_PACKET_DATA	Generic short packet data
5:0	GENERIC_SHORT_PACKET_DT	Generic short packet data

1A043A38 SENINF4_CSI2_HSRX_DBG — CSI2 HSRX Enable — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DATA_LANE7_HSRX_EN	DATA_LANE6_HSRX_EN	DATA_LANE5_HSRX_EN	DATA_LANE4_HSRX_EN	CLOCK_LANE_HSRX_EN	DATA_LANE3_HSRX_EN	DATA_LANE2_HSRX_EN	DATA_LANE1_HSRX_EN	DATA_LANE0_HSRX_EN
Type								RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
8	DATA_LANE7_HSRX_EN	Enables data lane 3 HSRX circuit
7	DATA_LANE6_HSRX_EN	Enables data lane 2 HSRX circuit
6	DATA_LANE5_HSRX_EN	Enables data lane 1 HSRX circuit
5	DATA_LANE4_HSRX_EN	Enables data lane 0 HSRX circuit
4	CLOCK_LANE_HSRX_EN	Enables clock lane HSRX circut
3	DATA_LANE3_HSRX_EN	Enables data lane 3 HSRX circuit
2	DATA_LANE2_HSRX_EN	Enables data lane 2 HSRX circuit
1	DATA_LANE1_HSRX_EN	Enables data lane 1 HSRX circuit
0	DATA_LANE0_HSRX_EN	Enables data lane 0 HSRX circuit

1A043A3C SENINF4_CSI2_DI **CSI2 Data Interleaving Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DT3						VC3		DT2						VC2	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DT1						VC1		DT0						VC0	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:26	DT3	Data type identifier
25:24	VC3	Virtual channel identifier
23:18	DT2	Data type identifier
17:16	VC2	Virtual channel identifier
15:10	DT1	Data type identifier
9:8	VC1	Virtual channel identifier
7:2	DT0	Data type identifier
1:0	VC0	Virtual channel identifier

1A043A40 SENINF4_CSI2_HS_TRAIL **CSI2 HS Trail Timing Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									HS_TRAIL_PARAMETER							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	HS_TRAIL_PARAMETER	HS TRAIL parameter

1A043A44 SENINF4_CSI2_DI_CTRL **CSI2 Data Interleaving Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						DT3_INTERLEAVING		VC3_INTERLEAVING						DT2_INTERLEAVING		VC2_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DT1_INTERLEAVING		VC1_INTERLEAVING						DT0_INTERLEAVING		VC0_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0

Bit(s)	Name	Description
26:25	DT3_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
24	VC3_INTERLEAVING	**Virtual channel identifier interleaving**
18:17	DT2_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
16	VC2_INTERLEAVING	**Virtual channel identifier interleaving**
10:9	DT1_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
8	VC1_INTERLEAVING	**Virtual channel identifier interleaving**
2:1	DT0_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
0	VC0_INTERLEAVING	**Virtual channel identifier interleaving**

1A043A48 SENINF4_CSI2_LNRD_FSM_X **CSI2 Data Lane RX FSM Other** **01010101**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LNRD7_RX_FSM								LNRD6_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		LNRD5_RX_FSM								LNRD4_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1

Bit(s)	Name	Description
30:24	LNRD7_RX_FSM	RX FSM of data lane 3
22:16	LNRD6_RX_FSM	RX FSM of data lane 2
14:8	LNRD5_RX_FSM	RX FSM of data lane 1
6:0	LNRD4_RX_FSM	RX FSM of data lane 0

Bit(s)	Name	Description

1A043A4C SENINF4_CSI2_DETECT_CON1 **CSI2 CPHY Detect Control Sync** **0E492300**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				SYNC_WORD												
Type				RW												
Reset				0	1	1	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYNC_WORD								DETECT_SYNC_MASK							DETECT_SYNC_DISABLE
Type	RW								RW							RW
Reset	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:8	SYNC_WORD	
7:1	DETECT_SYNC_MASK	
0	DETECT_SYNC_DISABLE	

1A043A50 SENINF4_CSI2_DETECT_CON2 **CSI2 CPHY Detect Control Escape** **0E492300**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				ESCAPE_WORD												
Type				RW												
Reset				0	1	1	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ESCAPE_WORD								DETECT_ESCAPE_MASK							DETECT_ESCAPE_DISABLE
Type	RW								RW							RW
Reset	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:8	ESCAPE_WORD	
7:1	DETECT_ESCAPE_MASK	
0	DETECT_ESCAPE_DISABLE	

1A043A54 SENINF4_CSI2_DETECT_CON3 **CSI2 CPHY Detect Control Post** **12492400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				POST_WORD												

Type				RW												
Reset				1	0	0	1	0	0	1	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	POST_WORD								DETECT_POST_MASK							DETECT_POST_DISABLE
Type	RW								RW							RW
Reset	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:8	POST_WORD	
7:1	DETECT_POST_MASK	
0	DETECT_POST_DISABLE	

1A043A58 SENINF4_CSI2_RLR0_CON0 CSI2 CPHY RLR0 CON0 FFFFFF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLR0_PRBS_SEED_2								RLR0_PRBS_SEED_1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLR0_PRBS_SEED_0								RLR0_PRBS_PATTERN_SEL							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RLR0_PRBS_SEED_2	
23:16	RLR0_PRBS_SEED_1	
15:8	RLR0_PRBS_SEED_0	
7:0	RLR0_PRBS_PATTERN_SEL	

1A043A5C SENINF4_CSI2_RLR1_CON0 CSI2 CPHY RLR1 CON0 FFFFFF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLR1_PRBS_SEED_2								RLR1_PRBS_SEED_1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLR1_PRBS_SEED_0								RLR1_PRBS_PATTERN_SEL							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RLR1_PRBS_SEED_2	
23:16	RLR1_PRBS_SEED_1	
15:8	RLR1_PRBS_SEED_0	
7:0	RLR1_PRBS_PATTERN_SEL	

Bit(s)	Name	Description

1A043A60 **SENINF4_CSI2_RLR2_CON0** **CSI2 CPHY RLR2 CON0** **FFFFFF00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLR2_PRBS_SEED_2								RLR2_PRBS_SEED_1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLR2_PRBS_SEED_0								RLR2_PRBS_PATTERN_SEL							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RLR2_PRBS_SEED_2	
23:16	RLR2_PRBS_SEED_1	
15:8	RLR2_PRBS_SEED_0	
7:0	RLR2_PRBS_PATTERN_SEL	

1A043A64 **SENINF4_CSI2_RLR_CON** **CSI2 CPHY RLR CON0** **FFFFFF00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLRN_PRBS_SEED_2								RLRN_PRBS_SEED_1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLRN_PRBS_SEED_0								RLRN_PRBS_PATTERN_SEL							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	RLRN_PRBS_SEED_2	
23:16	RLRN_PRBS_SEED_1	
15:8	RLRN_PRBS_SEED_0	
7:0	RLRN_PRBS_PATTERN_SEL	

1A043A68 **SENINF4_CSI2_MUX_CON** **CSI2 Pin Pux Sel** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												POST_PACKET_IGNORE_E	RLR_PATTERN_DELAY_EN	CPHY_RX_EXTERNAL_EN	CPHY_TX_EXTERNAL_EN	DPHY_RX_EXTERNAL_EN

												N				
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	POST_PACKET_IGNORE_EN	
3	RLR_PATTERN_DELAY_EN	
2	CPHY_RX_EXTERNAL_EN	
1	CPHY_TX_EXTERNAL_EN	
0	DPHY_RX_EXTERNAL_EN	

1A043A6C SENINF4_CSI2_DETECT_DBG0 CSI2 Detection Debug 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		POSITION_SYNC_LANE2_ST				DETECT_POST_LANE2_ST	DETECT_ESCAPE_LANE2_ST	DETECT_SYNC_LANE2_ST		POSITION_ESCAPE_LANE1_ST				POSITION_SYNC_LANE1_ST		
Type		RO				RO	RO	RO		RO				RO		
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	POSITION_SYNC_LANE1_ST	DETECT_POST_LANE1_ST	DETECT_ESCAPE_LANE1_ST	DETECT_SYNC_LANE1_ST		POSITION_ESCAPE_LANE0_ST				POSITION_SYNC_LANE0_ST				DETECT_POST_LANE0_ST	DETECT_ESCAPE_LANE0_ST	DETECT_SYNC_LANE0_ST
Type	RO	RO	RO	RO		RO				RO				RO	RO	RO
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:27	POSITION_SYNC_LANE2_ST	
26	DETECT_POST_LANE2_ST	
25	DETECT_ESCAPE_LANE2_ST	
24	DETECT_SYNC_LANE2_ST	
22:19	POSITION_ESCAPE_LANE1_ST	
18:15	POSITION_SYNC_LANE1_ST	
14	DETECT_POST_LANE1_ST	
13	DETECT_ESCAPE_LANE1_ST	
12	DETECT_SYNC_LANE1_ST	
10:7	POSITION_ESCAPE_LANE0_ST	
6:3	POSITION_SYNC_LANE0_ST	
2	DETECT_POST_LANE0_ST	
1	DETECT_ESCAPE_LANE0_ST	
0	DETECT_SYNC_LANE0_ST	

1A043A70 SENINF4_CSI2_DETECT_DBG1 CSI2 Detection Debug 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													POSITION_ESCAPE_LANE2_ST			
Type													RO			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	POSITION_ESCAPE_LANE2_ST	

1A043A74 SENINF4_CSI2_RESYNC_MERGE_CTL **CSI2 Lane Resync Merge Control** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								LANE_RESYNC_FLUSH_EN				LANE_MERGE_INPUT_SEL		CPHY_LANE_RESYNC_CNT		
Type								RW				RW		RW		
Reset								0				0		0	0	1

Bit(s)	Name	Description
8	LANE_RESYNC_FLUSH_EN	
4	LANE_MERGE_INPUT_SEL	
2:0	CPHY_LANE_RESYNC_CNT	

1A043A78 SENINF4_CSI2_CTRL_TRIO_MUX **CSI2 Control Trio Mux** **00000088**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TRIO2_MUX			TRIO1_MUX			TRIO0_MUX		
Type								RW			RW			RW		
Reset								0	1	0	0	0	1	0	0	0

Bit(s)	Name	Description
8:6	TRIO2_MUX	
5:3	TRIO1_MUX	
2:0	TRIO0_MUX	

1A043A7C SENINF4_CSI2_CTRL_TRIO_CON **CSI2 Control Trio Config** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											TRIO2_HSRX_EN	TRIO2_LPRX_EN	TRIO1_HSRX_EN	TRIO1_LPRX_EN	TRIO0_HSRX_EN	TRIO0_LPRX_EN
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5	TRIO2_HSRX_EN	
4	TRIO2_LPRX_EN	
3	TRIO1_HSRX_EN	
2	TRIO1_LPRX_EN	
1	TRIO0_HSRX_EN	
0	TRIO0_LPRX_EN	

1A043A80 SENINF4_FIX_ADDR_CPHY0_DBG **cphy_fix_point_addr_cphy0_debug** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								WORD_COUNT_OVER_FLOAT_CPHY0	ERROR_COUNT_CPHY0							
Type								RO	RO							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
24	WORD_COUNT_OVER_FLOAT_CPHY0	
23:16	ERROR_COUNT_CPHY0	

1A043A84 SENINF4_FIX_ADDR_CPHY1_DBG **cphy_fix_point_addr_cphy1_debug** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name								WORD_COUNT_OVER_FLOAT_CPHY1	ERRO R_CO UNT_ CPHY 1							
Type								RO	RO							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
24	WORD_COUNT_OVER_FLOAT_CPHY1	
23:16	ERROR_COUNT_CPHY1	

1A043A88 SENINF4_FIX_ADDR_CPHY2_DBG cphy_fix_point_addr_cphy2_debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								WORD_COUNT_OVER_FLOAT_CPHY2	ERRO R_CO UNT_ CPHY 2							
Type								RO	RO							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
24	WORD_COUNT_OVER_FLOAT_CPHY2	
23:16	ERROR_COUNT_CPHY2	

1A043A8C SENINF4_FIX_ADDR_DBG cphy_fix_point_addr_debug 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								WORD_COUNT_OVER_FLOAT	ERRO R_CO UNT							
Type								RO	RO							
Reset								0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
24	WORD_COUNT_OVER_FLOAT	
23:16	ERROR_COUNT	

1A043A90 SENINF4_WIRE_STATE_DECODE_CPHY0_DBG0 cphy_wire_state_decode_cphy0_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYMBOL_STREAM0_CPHY0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYMBOL_STREAM0_CPHY0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SYMBOL_STREAM0_CPHY0	

1A043A94 SENINF4_WIRE_STATE_DECODE_CPHY0_DBG1 cphy_wire_state_decode_cphy0_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SYMBOL_STREAM_VALID_CPHY0	SYMBOL_STREAM1_CPHY0									
Type						RO	RO									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	SYMBOL_STREAM_VALID_CPHY0	
9:0	SYMBOL_STREAM1_CPHY0	

1A043A98 SENINF4_WIRE_STATE_DECODE_CPHY1_DBG0 cphy_wire_state_decode_cphy1_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYMBOL_STREAM0_CPHY1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYMBOL_STREAM0_CPHY1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SYMBOL_STREAM0_CPHY1	

1A043A9C SENINF4_WIRE_STATE_DECODE_CPHY1_DBG1 cphy_wire_state_decode_cphy1_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SYMBOL_STREAM_VALID_CPHY1	SYMBOL_STREAM1_CPHY1									
Type						RO	RO									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	SYMBOL_STREAM_VALID_CPHY1	
9:0	SYMBOL_STREAM1_CPHY1	

1A043AA0 SENINF4_WIRE_STATE_DECODE_CPHY2_DBG0 cphy_wire_state_decode_cphy2_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYMBOL_STREAM0_CPHY2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYMBOL_STREAM0_CPHY2															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SYMBOL_STREAM0_CPHY2	

1A043AA4 SENINF4_WIRE_STATE_DECODE_CPHY2_DBG1 cphy_wire_state_decode_cphy2_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SYMBOL_STREAM_VALID_CPHY2	SYMBOL_STREAM1_CPHY2									
Type						RO	RO									
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	SYMBOL_STREAM_VALID_CPHY2	
9:0	SYMBOL_STREAM1_CPHY2	

1A043AA8 SENINF4_SYNC_RESYNC_CTL CSI2 Sync Resync Control 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													FLUSH_VALID	SYNC_DETECTION_SEL		
Type													RW	RW		
Reset													0	0	0	1

Bit(s)	Name	Description
3	FLUSH_VALID	
2:0	SYNC_DETECTION_SEL	

1A043AAC SENINF4_POST_DETECT_CTL CSI2 Post Detect Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															POST_EN	POST_DETECT_DISABLE
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	POST_EN	
0	POST_DETECT_DISABLE	

1A043AB0 SENINF4_WIRE_STATE_DECODE_CONFIG — CSI2 Wire State Decode Config — 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INIT_STATE_DECODE		
Type														RW		
Reset														1	0	0

Bit(s)	Name	Description
2:0	INIT_STATE_DECODE	

1A043AB4 SENINF4_CSI2_CPHY_LNRD_FSM — CPHY Data Lane RX FSM — 01010100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		TRIO2_RX_FSM								TRIO1_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TRIO0_RX_FSM														
Type		RO														
Reset		0	0	0	0	0	0	1								

Bit(s)	Name	Description
30:24	TRIO2_RX_FSM	RX FSM of data trio 2
22:16	TRIO1_RX_FSM	RX FSM of data trio 1

Bit(s)	Name	Description
14:8	TRIO0_RX_FSM	RX FSM of data trio 0

1A043AB8 SENINF4_FIX_ADDR_CPHY0_DBG0 cphy_fix_point_addr_cphy0_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD_COUNT_CPHY0_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY0_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD_COUNT_CPHY0_DBG0	

1A043ABC SENINF4_FIX_ADDR_CPHY0_DBG1 cphy_fix_point_addr_cphy0_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY0_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY0_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERROR_RECORD_CPHY0_DBG0	
15:0	WORD_COUNT_CPHY0_DBG1	

1A043AC0 SENINF4_FIX_ADDR_CPHY0_DBG2 cphy_fix_point_addr_cphy0_debug2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY0_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERROR_RECORD_CPHY0_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ERROR_RECORD_CPHY0_DBG1	

Bit(s)	Name	Description

1A043AC4 SENINF4_FIX_ADDR_CPHY1_DBG0 cphy_fix_point_addr_cphy1_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD_COUNT_CPHY1_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY1_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD_COUNT_CPHY1_DBG0	

1A043AC8 SENINF4_FIX_ADDR_CPHY1_DBG1 cphy_fix_point_addr_cphy1_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY1_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY1_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERROR_RECORD_CPHY1_DBG0	
15:0	WORD_COUNT_CPHY1_DBG1	

1A043ACC SENINF4_FIX_ADDR_CPHY1_DBG2 cphy_fix_point_addr_cphy1_debug2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY1_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERROR_RECORD_CPHY1_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ERROR_RECORD_CPHY1_DBG1	

Bit(s)	Name	Description

1A043AD0 SENINF4_FIX_ADDR_CPHY2_DBG0 cphy_fix_point_addr_cphy2_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD_COUNT_CPHY2_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY2_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD_COUNT_CPHY2_DBG0	

1A043AD4 SENINF4_FIX_ADDR_CPHY2_DBG1 cphy_fix_point_addr_cphy2_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY2_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_CPHY2_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERROR_RECORD_CPHY2_DBG0	
15:0	WORD_COUNT_CPHY2_DBG1	

1A043AD8 SENINF4_FIX_ADDR_CPHY2_DBG2 cphy_fix_point_addr_cphy2_debug2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_CPHY2_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERROR_RECORD_CPHY2_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ERROR_RECORD_CPHY2_DBG1	

Bit(s)	Name	Description

1A043ADC SENINF4_FIX_ADDR_DBG cphy_fix_point_addr_debug0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WORD_COUNT_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WORD_COUNT_DBG0	

1A043AE0 SENINF4_FIX_ADDR_DBG1 cphy_fix_point_addr_debug1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_DBG0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WORD_COUNT_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ERROR_RECORD_DBG0	
15:0	WORD_COUNT_DBG1	

1A043AE4 SENINF4_FIX_ADDR_DBG2 cphy_fix_point_addr_debug2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERROR_RECORD_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERROR_RECORD_DBG1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ERROR_RECORD_DBG1	

1A043AE8 SENINF4_CSI2_MODE — CSI2 Packet Structure — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	csr_cphy_wc_pos								csr_cphy_di_pos							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						csr_csi2_header_len			csr_csi2_mode							
Type						RW			RW							
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	csr_cphy_wc_pos	
23:16	csr_cphy_di_pos	
10:8	csr_csi2_header_len	0: 4 bytes 1: 12 bytes 2: 24 bytes 4: 36 bytes
7:0	csr_csi2_mode	

1A043AF0 SENINF4_CSI2_DI_EXT — CSI2 Data Interleaving Parameters Extend — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DT5						VC5		DT4						VC4	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:10	DT5	Data type identifier
9:8	VC5	Virtual channel identifier
7:2	DT4	Data type identifier
1:0	VC4	Virtual channel identifier

1A043AF4 SENINF4_CSI2_DI_CTRL_EXT — CSI2 Data Interleaving Control Extend — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DT5_INTERLEAVING		VC5_INTERLEA						DT4_INTERLEAVING		VC4_INTERLEA

								VING								VING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0

Bit(s)	Name	Description
10:9	DT5_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
8	VC5_INTERLEAVING	**Virtual channel identifier interleaving**
2:1	DT4_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
0	VC4_INTERLEAVING	**Virtual channel identifier interleaving**

1A043AF8 SENINF4_CSI2_CPHY_LOOPBACK **CSI2 SW Trigger sync_init and hs_en** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RELEASE_SYNC_INIT	TRIGGER_SYNC_INIT
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RELEASE_SYNC_INIT	Releases sync_init in CPHY TX loopback test mode
0	TRIGGER_SYNC_INIT	Triggers sync_init and hs_en in CPHY TX loopback test mode

1A043B00 SENINF4_CSI2_PROGSEQ_0 **CSI2 CPHY Program sequence_0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PROG SEQ_ S7				PROG SEQ_ S6				PROGSEQ_S5				PROGSEQ_S4		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PROGSEQ_S3				PROGSEQ_S2				PROGSEQ_S1				PROGSEQ_S0		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	PROGSEQ_S7	Fix symbol for prbs generator

Bit(s)	Name	Description
26:24	PROGSEQ_S6	Fix symbol for prbs generator
22:20	PROGSEQ_S5	Fix symbol for prbs generator
18:16	PROGSEQ_S4	Fix symbol for prbs generator
14:12	PROGSEQ_S3	Fix symbol for prbs generator
10:8	PROGSEQ_S2	Fix symbol for prbs generator
6:4	PROGSEQ_S1	Fix symbol for prbs generator
2:0	PROGSEQ_S0	Fix symbol for prbs generator

1A043B04 SENINF4_CSI2_PROGSEQ_1 — **CSI2 CPHY Program sequence_1** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										PROG SEQ_ S13				PROGSEQ_S 12		
Type										RW				RW		
Reset										0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PROGSEQ_S11				PROGSEQ_S10				PROGSEQ_S9				PROGSEQ_S8		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
22:20	PROGSEQ_S13	Fix symbol for prbs generator
18:16	PROGSEQ_S12	Fix symbol for prbs generator
14:12	PROGSEQ_S11	Fix symbol for prbs generator
10:8	PROGSEQ_S10	Fix symbol for prbs generator
6:4	PROGSEQ_S9	Fix symbol for prbs generator
2:0	PROGSEQ_S8	Fix symbol for prbs generator

1A043B10 SENINF4_CSI2_INT_EN_EXT — **CSI2 Interrupt Enable Extend** — **0000071F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_WCLR_EN															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						ERR_SOT_SYNC_HS_TRIO2	ERR_SOT_SYNC_HS_TRIO1	ERR_SOT_SYNC_HS_TRIO0				DPHY3_RESYNC_FIFO_OVERFLOW	DPHY2_RESYNC_FIFO_OVERFLOW	DPHY1_RESYNC_FIFO_OVERFLOW	DPHY0_RESYNC_FIFO_OVERFLOW	ERR_LANE_RESYNC
Type						RW	RW	RW				RW	RW	RW	RW	RW
Reset						1	1	1				1	1	1	1	1

Bit(s)	Name	Description
31	INT_WCLR_EN	Enables Interrupt write clear
10	ERR_SOT_SYNC_HS_TRIO2	Enables TRIO2 ERR_SOT_SYNC_HS interrupt

Bit(s)	Name	Description
9	ERR_SOT_SYNC_HS_TRIO1	Enables TRIO1 ERR_SOT_SYNC_HS interrupt
8	ERR_SOT_SYNC_HS_TRIO0	Enables TRIO0 ERR_SOT_SYNC_HS interrupt
4	DPHY3_RESYNC_FIFO_OVERFLOW	Enables LANE3_RESYNC_FIFO_OVERFLOW interrupt
3	DPHY2_RESYNC_FIFO_OVERFLOW	Enables LANE2_RESYNC_FIFO_OVERFLOW interrupt
2	DPHY1_RESYNC_FIFO_OVERFLOW	Enables LANE1_RESYNC_FIFO_OVERFLOW interrupt
1	DPHY0_RESYNC_FIFO_OVERFLOW	Enables LANE0_RESYNC_FIFO_OVERFLOW interrupt
0	ERR_LANE_RESYNC	Enables ERR_LANE_RESYNC interrupt

1A043B14 SENINF4_CSI2_INT_STATUS_EXT CSI2 Interrupt Status Extend 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						ERR_SOT_SYNC_HS_TRIO2_STA	ERR_SOT_SYNC_HS_TRIO1_STA	ERR_SOT_SYNC_HS_TRIO0_STA				DPHY3_RESYNC_FIFO_OVERFLOW_STA	DPHY2_RESYNC_FIFO_OVERFLOW_STA	DPHY1_RESYNC_FIFO_OVERFLOW_STA	DPHY0_RESYNC_FIFO_OVERFLOW_STA	ERR_LANE_RESYNC_STA
Type						RO	RO	RO				RO	RO	RO	RO	RO
Reset						0	0	0				0	0	0	0	0

Bit(s)	Name	Description
10	ERR_SOT_SYNC_HS_TRIO2_STA	Asserted when proper synchronization cannot be expected
9	ERR_SOT_SYNC_HS_TRIO1_STA	Asserted when proper synchronization cannot be expected
8	ERR_SOT_SYNC_HS_TRIO0_STA	Asserted when proper synchronization cannot be expected
4	DPHY3_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of dphy lane3 is overflowed
3	DPHY2_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of dphy lane2 is overflowed
2	DPHY1_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of dphy lane1 is overflowed
1	DPHY0_RESYNC_FIFO_OVERFLOW_STA	Asserted when the resync FIFO of dphy lane0 is overflowed
0	ERR_LANE_RESYNC_STA	Asserted when DPHY lane sync detect time is longer than set resync cycles

1A043B18 SENINF4_CSI2_CPHY_FIX_POINT_RST CSI2 CPHY Fix Point Reset Mode 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CPHY_FIX_POINT_RST_MODE	CPHY_FIX_POINT_SW_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	CPHY_FIX_POINT_RST_MODE	Fix point rest mode
0	CPHY_FIX_POINT_SW_RST	Fix point software reset

1A043B20 SENINF4_CSI2_DPHY_RESYNC_CTL CSI2 DPHY Lane Resync Control 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DPHY_RESYNC_CNT								DPHY_RESYNC_FLUSH_EN	DPHY_RESYNC_DATAOUT_OPTION	DPHY_BYPASS_LANE_RESYNC
Type						RW								RW	RW	RW
Reset						0	0	1						0	0	0

Bit(s)	Name	Description
10:8	DPHY_RESYNC_CNT	Detect lane skew cycle count
2	DPHY_RESYNC_FLUSH_EN	Enables lane resync flush
1	DPHY_RESYNC_DATAOUT_OPTION	Data output option
0	DPHY_BYPASS_LANE_RESYNC	Bypass lane resync function

Module name: mipi_rx_config_csi3 Base address: (+1a043800h)

Address	Name	Width	Register Function
1A043800	MIPI_RX_CON00_CSI3	32	MIPI RX Config Register
1A043804	MIPI_RX_CON04_CSI3	32	MIPI RX Config Register
1A043808	MIPI_RX_CON08_CSI3	32	MIPI RX Config Register
1A043824	MIPI_RX_CON24_CSI3	32	MIPI RX Config Register
1A043828	MIPI_RX_CON28_CSI3	32	MIPI RX Config Register

Address	Name	Width	Register Function
1A043834	MIPI_RX_CON34_CSI3	32	MIPI RX Config Register
1A043838	MIPI_RX_CON38_CSI3	32	MIPI RX Config Register
1A04383C	MIPI_RX_CON3C_CSI3	32	MIPI RX Config Register
1A043840	MIPI_RX_CON40_CSI3	32	MIPI RX Config Register
1A043844	MIPI_RX_CON44_CSI3	32	MIPI RX Config Register
1A043848	MIPI_RX_CON48_CSI3	32	MIPI RX Config Register
1A04384C	MIPI_RX_CON4C_CSI3	32	MIPI RX Config Register
1A043850	MIPI_RX_CON50_CSI3	32	MIPI RX Config Register
1A04387C	MIPI_RX_CON7C_CSI3	32	MIPI RX Config Register
1A043880	MIPI_RX_CON80_CSI3	32	MIPI RX Config Register
1A043884	MIPI_RX_CON84_CSI3	32	MIPI RX Config Register
1A043888	MIPI_RX_CON88_CSI3	32	MIPI RX Config Register
1A04388C	MIPI_RX_CON8C_CSI3	32	MIPI RX Config Register
1A043890	MIPI_RX_CON90_CSI3	32	MIPI RX Config Register
1A043894	MIPI_RX_CON94_CSI3	32	MIPI RX Config Register
1A043898	MIPI_RX_CON98_CSI3	32	MIPI RX Config Register
1A0438A0	MIPI_RX_CONA0_CSI3	32	MIPI RX Config Register
1A0438B0	MIPI_RX_CONB0_CSI3	32	Deskew control register
1A0438B4	MIPI_RX_CONB4_CSI3	32	Deskew sync detection sequence
1A0438B8	MIPI_RX_CONB8_CSI3	32	Deskew timing control
1A0438BC	MIPI_RX_CONBC_CSI3	32	Deskew mode
1A0438C0	MIPI_RX_CONC0_CSI3	32	Interrupt enable
1A0438C4	MIPI_RX_CONC4_CSI3	32	Interrupt status
1A0438C8	MIPI_RX_CONC8_CSI3	32	Debug mux select
1A0438CC	MIPI_RX_CONCC_CSI3	32	Debug outputs
1A0438D0	MIPI_RX_COND0_CSI3	32	Deskew delay length

1A043800 MIPI_RX_CON00_CSI3 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_CSI0_LNR3_HSRX_OFFSET_CODE					RG_CSI0_LNR3_HSRX_CAL_EN	RG_CSI0_LNR3_HSRX_CAL_APPLY		RG_CSI0_LNR2_HSRX_OFFSET_CODE					RG_CSI0_LNR2_HSRX_CAL_EN	RG_CSI0_LNR2_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI0_LNR1_HSRX_OFFSET_CODE					RG_CSI0_LNR1_HSRX_CAL_EN	RG_CSI0_LNR1_HSRX_CAL_APPLY		RG_CSI0_LNR0_HSRX_OFFSET_CODE					RG_CSI0_LNR0_HSRX_CAL_EN	RG_CSI0_LNR0_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	RG_CSI0_LNR3_HSRX_OFFSET_CODE	**Lane3 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
25	RG_CSI0_LNR3_HSRX_CAL_EN	**Lane3 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
24	RG_CSI0_LNR3_HSRX_CAL_APPLY	**Lane3 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
22:18	RG_CSI0_LNR2_HSRX_OFFSET_CODE	**Lane2 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
17	RG_CSI0_LNR2_HSRX_CAL_EN	**Lane2 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
16	RG_CSI0_LNR2_HSRX_CAL_APPLY	**Lane2 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
14:10	RG_CSI0_LNR1_HSRX_OFFSET_CODE	**Lane1 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
9	RG_CSI0_LNR1_HSRX_CAL_EN	**Lane1 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
8	RG_CSI0_LNR1_HSRX_CAL_APPLY	**Lane1 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
6:2	RG_CSI0_LNR0_HSRX_OFFSET_CODE	**Lane0 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage

Bit(s)	Name	Description
		5'bx1111: maximum output voltage
1	RG_CSI0_LNR0_HSRX_CAL_EN	**Lane0 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
0	RG_CSI0_LNR0_HSRX_CAL_APPLY	**Lane0 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result

1A043804 MIPI_RX_CON04_CSI3 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_CSI0_LNR7_HSRX_OFFSET_CODE					RG_CSI0_LNR7_HSRX_CAL_EN	RG_CSI0_LNR7_HSRX_CAL_APPLY		RG_CSI0_LNR6_HSRX_OFFSET_CODE					RG_CSI0_LNR6_HSRX_CAL_EN	RG_CSI0_LNR6_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI0_LNR5_HSRX_OFFSET_CODE					RG_CSI0_LNR5_HSRX_CAL_EN	RG_CSI0_LNR5_HSRX_CAL_APPLY		RG_CSI0_LNR4_HSRX_OFFSET_CODE					RG_CSI0_LNR4_HSRX_CAL_EN	RG_CSI0_LNR4_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	RG_CSI0_LNR7_HSRX_OFFSET_CODE	**Lane7 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
25	RG_CSI0_LNR7_HSRX_CAL_EN	**Lane7 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
24	RG_CSI0_LNR7_HSRX_CAL_APPLY	**Lane7 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
22:18	RG_CSI0_LNR6_HSRX_OFFSET_CODE	**Lane6 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
17	RG_CSI0_LNR6_HSRX_CAL_EN	**Lane6 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
16	RG_CSI0_LNR6_HSRX_CAL_APPLY	**Lane6 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
14:10	RG_CSI0_LNR5_HSRX_OFFSET_CODE	**Lane5 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage

Bit(s)	Name	Description
		5'bx1111: maximum output voltage
9	RG_CSI0_LNR5_HSRX_CAL_EN	**Lane5 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
8	RG_CSI0_LNR5_HSRX_CAL_APPLY	**Lane5 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
6:2	RG_CSI0_LNR4_HSRX_OFFSET_CODE	**Lane4 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
1	RG_CSI0_LNR4_HSRX_CAL_EN	**Lane4 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
0	RG_CSI0_LNR4_HSRX_CAL_APPLY	**Lane4 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result

1A043808 MIPI_RX_CON08_CSI3 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RG_CSI0_LNR11_HSRX_OFFSET_CODE					RG_CSI0_LNR11_HSRX_CAL_EN	RG_CSI0_LNR11_HSRX_CAL_APPLY		RG_CSI0_LNR10_HSRX_OFFSET_CODE					RG_CSI0_LNR10_HSRX_CAL_EN	RG_CSI0_LNR10_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_CSI0_LNR9_HSRX_OFFSET_CODE					RG_CSI0_LNR9_HSRX_CAL_EN	RG_CSI0_LNR9_HSRX_CAL_APPLY		RG_CSI0_LNR8_HSRX_OFFSET_CODE					RG_CSI0_LNR8_HSRX_CAL_EN	RG_CSI0_LNR8_HSRX_CAL_APPLY
Type		RW					RW	RW		RW					RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	RG_CSI0_LNR11_HSRX_OFFSET_CODE	**Lane11 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
25	RG_CSI0_LNR11_HSRX_CAL_EN	**Lane11 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
24	RG_CSI0_LNR11_HSRX_CAL_APPLY	**Lane11 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
22:18	RG_CSI0_LNR10_HSRX_OFFSET_CODE	**Lane10 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage

Bit(s)	Name	Description
		5'bx1111: maximum output voltage
17	RG_CSI0_LNR10_HSRX_CAL_EN	**Lane10 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
16	RG_CSI0_LNR10_HSRX_CAL_APPLY	**Lane10 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
14:10	RG_CSI0_LNR9_HSRX_OFFSET_CODE	**Lane9 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
9	RG_CSI0_LNR9_HSRX_CAL_EN	**Lane9 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
8	RG_CSI0_LNR9_HSRX_CAL_APPLY	**Lane9 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result
6:2	RG_CSI0_LNR8_HSRX_OFFSET_CODE	**Lane8 HSRX offset calibration code:** 5'b0xxxx: increase positive output voltage 5'b1xxxx: increase negative output voltage 5'bx0000: minimum output voltage 5'bx1111: maximum output voltage
1	RG_CSI0_LNR8_HSRX_CAL_EN	**Lane8 HSRX offset calibration enable:** 1'b0: disable 1'b1: enable
0	RG_CSI0_LNR8_HSRX_CAL_APPLY	**Lane8 HSRX offset calibration apply:** 1'b0: don't use calibration result 1'b1: use calibration result

1A043824 MIPI_RX_CON24_CSI3 **MIPI RX Config Register** **E4000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI0_BIST_LN3_MUX		CSI0_BIST_LN2_MUX		CSI0_BIST_LN1_MUX		CSI0_BIST_LN0_MUX		CSI0_BIST_SETTLE_DELAY							
Type	RW		RW		RW		RW		RW							
Reset	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI0_BIST_TERM_DELAY								CSI0_BIST_CLK4X_SEL	CSI0_BIST_CLK_SEL	CSI0_BIST_FIX_PAT			CSI0_BIST_EN	CSI0_BIST_NUM	
Type	RW								RW	RW	RW			RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0			0	0	0

Bit(s)	Name	Description
31:30	CSI0_BIST_LN3_MUX	**CSI0 Lane mux**
29:28	CSI0_BIST_LN2_MUX	**CSI0 Lane mux**
27:26	CSI0_BIST_LN1_MUX	**CSI0 Lane mux**
25:24	CSI0_BIST_LN0_MUX	**CSI0 Lane mux**
23:16	CSI0_BIST_SETTLE_DELAY	**CSI0 Settle Delay Setting**
15:8	CSI0_BIST_TERM_DELAY	**CSI0 Term Delay Setting**
7	CSI0_BIST_CLK4X_SEL	**CSI0 CLK4X Sel** 0: inverse 1: not inverse
6	CSI0_BIST_CLK_SEL	**CSI0 CLK Sel**

Bit(s)	Name	Description
		0: inverse 1: not inverse
5	CSI0_BIST_FIX_PAT	**CSI0 Bist Patern** 0: Random 1: Fix
2	CSI0_BIST_EN	**CSI0 Bist Enalbe**
1:0	CSI0_BIST_NUM	**CSI0 Bist num** 0: 1 lane 1: 2 lane 2: 3 lane 3: 4 lane

1A043828 MIPI_RX_CON28_CSI3 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CSI0_BIST_CSI2_DATA_OK	CSI0_BIST_LANE_FSM_OK	CSI0_BIST_HS_FSM_OK	CSI0_BIST_DATA_OK	CSI0_BIST_START
Type												RO	RO	RO	RO	RO
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	CSI0_BIST_CSI2_DATA_OK	CSI0 BIST CSI2 Data ok
3	CSI0_BIST_LANE_FSM_OK	CSI0 BIST High Speed FSM ok
2	CSI0_BIST_HS_FSM_OK	CSI0 BIST Data Lane FSM ok
1	CSI0_BIST_DATA_OK	CSI0 BIST DPHY Data ok
0	CSI0_BIST_START	CSI0 BIST start status

1A043834 MIPI_RX_CON34_CSI3 MIPI RX Config Register E4000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI0_BIST_LN7_MUX		CSI0_BIST_LN6_MUX		CSI0_BIST_LN5_MUX		CSI0_BIST_LN4_MUX		CSI0_BIST_HS DET_MUX							
Type	RW		RW		RW		RW		RW							
Reset	1	1	1	0	0	1	0	0	0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BIST_MODE
Type																RW
Reset																0

Bit(s)	Name	Description
31:30	CSI0_BIST_LN7_MUX	**CSI0 Lane mux**
29:28	CSI0_BIST_LN6_MUX	**CSI0 Lane mux**

Bit(s)	Name	Description
27:26	CSI0_BIST_LN5_MUX	CSI0 Lane mux
25:24	CSI0_BIST_LN4_MUX	CSI0 Lane mux
23:22	CSI0_BIST_HSDET_MUX	CSI0 HSDET mux
0	BIST_MODE	BIST mode enable

1A043838 MIPI_RX_CON38_CSI3 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_c kpha se_t rio2					rg_ckphase_trio1						rg_ckphase_trio0				
Type	RW					RW						RW				
Reset	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						MIPI_RX_SW_CPHY_RX_MODE	MIPI_RX_SW_CPHY_TX_MODE	MIPI_RX_SW_RST					MIPI_RX_HW_CAL_OPTION	MIPI_RX_HW_CAL_START	MIPI_RX_SW_CAL_MODE	MIPI_RX_SW_CTRL_MODE
Type						RW	RW	RW					RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:27	rg_ckphase_trio2	
26:22	rg_ckphase_trio1	
20:16	rg_ckphase_trio0	
10	MIPI_RX_SW_CPHY_RX_MODE	**CPHY RX SW control mode**
9	MIPI_RX_SW_CPHY_TX_MODE	**CPHY TX SW control mode**
8:4	MIPI_RX_SW_RST	**SW reset**
3	MIPI_RX_HW_CAL_OPTION	**HW calibration option** 0: 8 cycles 1 : 16cycles
2	MIPI_RX_HW_CAL_START	**HW calibration trigger**
1	MIPI_RX_SW_CAL_MODE	**SW calibration mode**
0	MIPI_RX_SW_CTRL_MODE	**SW control mode**

1A04383C MIPI_RX_CON3C_CSI3 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIPI_RX_SW_CTRL_															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIPI_RX_SW_CTRL_															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MIPI_RX_SW_CTRL_	SW control

1A043840 MIPI_RX_CON MIPI RX Config Register 00000000

N40_CSI3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_CSIo_LNRD3_HSRX_INVERT	RG_CSIo_LNRD3_LPRX_SWAP	RG_CSIo_LNRD2_HSRX_INVERT	RG_CSIo_LNRD2_LPRX_SWAP	RG_CSIo_LNRD1_HSRX_INVERT	RG_CSIo_LNRD1_LPRX_SWAP	RG_CSIo_LNRD0_HSRX_INVERT	RG_CSIo_LNRD0_LPRX_SWAP			RG_CSIo_LNRC_HSRX_INVERT	RG_CSIo_LNRC_LPRX_SWAP
Type					RW	RW	RW	RW	RW	RW	RW	RW			RW	RW
Reset					0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
11	RG_CSIo_LNRD3_HSRX_INVERT	
10	RG_CSIo_LNRD3_LPRX_SWAP	
9	RG_CSIo_LNRD2_HSRX_INVERT	
8	RG_CSIo_LNRD2_LPRX_SWAP	
7	RG_CSIo_LNRD1_HSRX_INVERT	
6	RG_CSIo_LNRD1_LPRX_SWAP	
5	RG_CSIo_LNRD0_HSRX_INVERT	
4	RG_CSIo_LNRD0_LPRX_SWAP	
1	RG_CSIo_LNRC_HSRX_INVERT	
0	RG_CSIo_LNRC_LPRX_SWAP	

1A043844 MIPI_RX_CO N44_CSI3 — MIPI RX Config Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSIo_L NR3_HSRX_OFFSET_CO DE					DA_CSIo_LNR3_HSRX_CAL_EN	DA_CSIo_LNR3_HSRX_CAL_APPLY		DA_CSIo_LNR2_HSRX_OFFSET_CODE					DA_CSIo_LNR2_HSRX_CAL_EN	DA_CSIo_LNR2_HSRX_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DA_CSIo_LNR1_HSRX_OFFSET_CODE					DA_CSIo_LNR1_HSRX_CAL_EN	DA_CSIo_LNR1_HSRX_CAL_APPLY		DA_CSIo_LNRo_HSRX_OFFSET_CODE					DA_CSIo_LNRo_HSRX_CAL_EN	DA_CSIo_LNRo_HSRX_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	DA_CSIo_LNR3_HSRX_OFFSET_CODE	
25	DA_CSIo_LNR3_HSRX_CAL_EN	
24	DA_CSIo_LNR3_HSRX_CAL_APPLY	

Bit(s)	Name	Description
22:18	DA_CSI0_LNR2_HSRX_OFFSET_CODE	
17	DA_CSI0_LNR2_HSRX_CAL_EN	
16	DA_CSI0_LNR2_HSRX_CAL_APPLY	
14:10	DA_CSI0_LNR1_HSRX_OFFSET_CODE	
9	DA_CSI0_LNR1_HSRX_CAL_EN	
8	DA_CSI0_LNR1_HSRX_CAL_APPLY	
6:2	DA_CSI0_LNR0_HSRX_OFFSET_CODE	
1	DA_CSI0_LNR0_HSRX_CAL_EN	
0	DA_CSI0_LNR0_HSRX_CAL_APPLY	

1A043848 MIPI_RX_CON48_CSI3 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSI0_LNR7_HSRX_OFFSET_CODE					DA_CSI0_LNR7_HSRX_CAL_EN	DA_CSI0_LNR7_HSRX_CAL_APPLY		DA_CSI0_LNR6_HSRX_OFFSET_CODE					DA_CSI0_LNR6_HSRX_CAL_EN	DA_CSI0_LNR6_HSRX_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DA_CSI0_LNR5_HSRX_OFFSET_CODE					DA_CSI0_LNR5_HSRX_CAL_EN	DA_CSI0_LNR5_HSRX_CAL_APPLY		DA_CSI0_LNR4_HSRX_OFFSET_CODE					DA_CSI0_LNR4_HSRX_CAL_EN	DA_CSI0_LNR4_HSRX_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	DA_CSI0_LNR7_HSRX_OFFSET_CODE	
25	DA_CSI0_LNR7_HSRX_CAL_EN	
24	DA_CSI0_LNR7_HSRX_CAL_APPLY	
22:18	DA_CSI0_LNR6_HSRX_OFFSET_CODE	
17	DA_CSI0_LNR6_HSRX_CAL_EN	
16	DA_CSI0_LNR6_HSRX_CAL_APPLY	
14:10	DA_CSI0_LNR5_HSRX_OFFSET_CODE	
9	DA_CSI0_LNR5_HSRX_CAL_EN	
8	DA_CSI0_LNR5_HSRX_CAL_APPLY	
6:2	DA_CSI0_LNR4_HSRX_OFFSET_CODE	

Bit(s)	Name	Description
1	DA_CSI0_LNR4_HSRX_CAL_EN	
0	DA_CSI0_LNR4_HSRX_CAL_APPLY	

1A04384C MIPI_RX_CON4C_CSI3 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DA_CSI0_LNR11_HSRX_OFFSET_CODE					DA_CSI0_LNR11_HSRX_CAL_EN	DA_CSI0_LNR11_HSRX_CAL_APPLY		DA_CSI0_LNR10_HSRX_OFFSET_CODE					DA_CSI0_LNR10_HSRX_CAL_EN	DA_CSI0_LNR10_HSRX_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DA_CSI0_LNR9_HSRX_OFFSET_CODE					DA_CSI0_LNR9_HSRX_CAL_EN	DA_CSI0_LNR9_HSRX_CAL_APPLY		DA_CSI0_LNR8_HSRX_OFFSET_CODE					DA_CSI0_LNR8_HSRX_CAL_EN	DA_CSI0_LNR8_HSRX_CAL_APPLY
Type		RO					RO	RO		RO					RO	RO
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	DA_CSI0_LNR11_HSRX_OFFSET_CODE	
25	DA_CSI0_LNR11_HSRX_CAL_EN	
24	DA_CSI0_LNR11_HSRX_CAL_APPLY	
22:18	DA_CSI0_LNR10_HSRX_OFFSET_CODE	
17	DA_CSI0_LNR10_HSRX_CAL_EN	
16	DA_CSI0_LNR10_HSRX_CAL_APPLY	
14:10	DA_CSI0_LNR9_HSRX_OFFSET_CODE	
9	DA_CSI0_LNR9_HSRX_CAL_EN	
8	DA_CSI0_LNR9_HSRX_CAL_APPLY	
6:2	DA_CSI0_LNR8_HSRX_OFFSET_CODE	
1	DA_CSI0_LNR8_HSRX_CAL_EN	
0	DA_CSI0_LNR8_HSRX_CAL_APPLY	

1A043850 MIPI_RX_CON50_CSI3 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_CSIo_BCLK_INV
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_CSIo_BCLK_INV	**CSIo byte clock** 0: Not inverse 1: Inverse

1A04387C MIPI_RX_CON7C_CSI3 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DA_CSIo_LNRD0_HSRX_DELAY_CODE					DA_CSIo_LNRD0_HSRX_DELAY_APPLY	DA_CSIo_LNRD0_HSRX_DELAY_EN
Type											RO				RO	RO
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:2	DA_CSIo_LNRD0_HSRX_DELAY_CODE	
1	DA_CSIo_LNRD0_HSRX_DELAY_APPLY	
0	DA_CSIo_LNRD0_HSRX_DELAY_EN	

1A043880 MIPI_RX_CON80_CSI3 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DA_CSIo_LNRD1_HSRX_DELAY_CODE					DA_CSIo_LNRD1_HSRX_DELAY_APP	DA_CSIo_LNRD1_HSRX_DELAY_EN

															LY	
Type											RO				RO	RO
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:2	DA_CSIo_LNRD1_HSRX_DELAY_CODE	
1	DA_CSIo_LNRD1_HSRX_DELAY_APPLY	
0	DA_CSIo_LNRD1_HSRX_DELAY_EN	

1A043884 MIPI_RX_CON84_CSI3 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DA_CSIo_LNRD2_HSRX_DELAY_CODE					DA_CSIo_LNRD2_HSRX_DELAY_APPLY	DA_CSIo_LNRD2_HSRX_DELAY_EN
Type											RO				RO	RO
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:2	DA_CSIo_LNRD2_HSRX_DELAY_CODE	
1	DA_CSIo_LNRD2_HSRX_DELAY_APPLY	
0	DA_CSIo_LNRD2_HSRX_DELAY_EN	

1A043888 MIPI_RX_CON88_CSI3 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DA_CSIo_LNRD3_HSRX_DELAY_CODE					DA_CSIo_LNRD3_HSRX_DELAY_APPLY	DA_CSIo_LNRD3_HSRX_DELAY_EN

Type											RO				RO	RO
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:2	DA_CSIo_LNRD3_HSRX_DELAY_CODE	
1	DA_CSIo_LNRD3_HSRX_DELAY_APPLY	
0	DA_CSIo_LNRD3_HSRX_DELAY_EN	

1A04388C MIPI_RX_CON8C_CSI3 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSIo_LNRDo_HSRX_DELAY_CODE						RG_CSIo_LNRDo_HSRX_DELAY_APPLY	RG_CSIo_LNRDo_HSRX_DELAY_EN
Type									RW						RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSIo_LNRDo_HSRX_DELAY_CODE	
1	RG_CSIo_LNRDo_HSRX_DELAY_APPLY	
0	RG_CSIo_LNRDo_HSRX_DELAY_EN	

1A043890 MIPI_RX_CON90_CSI3 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSIo_LNRD1_HSRX_DELAY_CODE						RG_CSIo_LNRD1_HSRX_DELAY_APPLY	RG_CSIo_LNRD1_HSRX_DELAY_EN
Type									RW						RW	RW

Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSI0_LNRD1_HSRX_DELAY_CODE	
1	RG_CSI0_LNRD1_HSRX_DELAY_APPLY	
0	RG_CSI0_LNRD1_HSRX_DELAY_EN	

1A043894 MIPI_RX_CON94_CSI3 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSI0_LNRD2_HSRX_DELAY_CODE						RG_CSI0_LNRD2_HSRX_DELAY_APPLY	RG_CSI0_LNRD2_HSRX_DELAY_EN
Type									RW						RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSI0_LNRD2_HSRX_DELAY_CODE	
1	RG_CSI0_LNRD2_HSRX_DELAY_APPLY	
0	RG_CSI0_LNRD2_HSRX_DELAY_EN	

1A043898 MIPI_RX_CON98_CSI3 MIPI RX Config Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSI0_LNRD3_HSRX_DELAY_CODE						RG_CSI0_LNRD3_HSRX_DELAY_APPLY	RG_CSI0_LNRD3_HSRX_DELAY_EN
Type									RW						RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSI0_LNRD3_HSRX_DELAY_CODE	
1	RG_CSI0_LNRD3_HSRX_DELAY_APPLY	
0	RG_CSI0_LNRD3_HSRX_DELAY_EN	

1A0438A0 MIPI_RX_CONA0_CSI3 **MIPI RX Config Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CSI0_LNRC_HSRX_DELAY_CODE						RG_CSI0_LNRC_HSRX_DELAY_APPLY	RG_CSI0_LNRC_HSRX_DELAY_EN
Type									RW						RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:2	RG_CSI0_LNRC_HSRX_DELAY_CODE	
1	RG_CSI0_LNRC_HSRX_DELAY_APPLY	
0	RG_CSI0_LNRC_HSRX_DELAY_EN	

1A0438B0 MIPI_RX_CONB0_CSI3 **Deskew control register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DESKEW_ENABLE	DESKEW_IP_SEL														DESKEW_CSI2_RST_ENABLE
Type	RW	RW														RW
Reset	0	0														0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DESKEW_ACC_MODE					DESKEW_TRIGGER_MODE			DESKEW_SW_RST				Delay_APPLY_MODE			
Type	RW					RW			RW				RW			
Reset	0	0	0	0		0	0	0	0				0	0	0	0

Bit(s)	Name	Description
31	DESKEW_ENABLE	**Deskew enable**
30	DESKEW_IP_SEL	0: New IP 1: Old IP
16	DESKEW_CSI2_RST_ENABLE	**Reset CSI2 IP when in DESKEW mode**
15:12	DESKEW_ACC_MODE	**Deskew edge mode**
10:8	DESKEW_TRIGGER_MODE	**Conditions for trigger DESKEW function**
7	DESKEW_SW_RST	**Deskew SW reset**
3:0	Delay_APPLY_MODE	**Delay apply mode:** 00/01: HW mode 10: RG mode 11: SW mode

1A0438B4 MIPI_RX_CO NB4_CSI3 Deskew sync detection sequence 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EXPECTED_SYNC_CODE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYNC_CODE_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	EXPECTED_SYNC_CODE	**Programmable sync code** In normal case, it should be 16'hFFFF.
15:0	SYNC_CODE_MASK	**When the bit is set to 1'b1, HW will compare its value with received sync code. Otherewise, no compare.**

1A0438B8 MIPI_RX_CO NB8_CSI3 Deskew timing control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								DESKEW_TIME_OUT_EN	DESKEW_TIME_OUT							
Type								RW	RW							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DESKEW_HOLD_TIME								DESKEW_SETUP_TIME			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
24	DESKEW_TIME_OUT_EN	**Deskew time out enable**
23:16	DESKEW_TIME_OUT	**Deskew time out period** If no deskew sync code is detected, FSM will be reset after this period.
11:8	DESKEW_HOLD_TIME	**Delay code apply hold time**
3:0	DESKEW_SETUP_TIME	**Delay code apply setup time**

Bit(s)	Name	Description

1A0438BC MIPI_RX_CONBC_CSI3 **Deskew mode** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							DESKEW_LANE_NUMBER						DESKEW_DELAY_APPLY_MODE			
Type							RW						RW			
Reset							0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DESKEW_DETECTION_CNT											DESKEW_DETECTION_MODE			
Type		RW											RW			
Reset		0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
25:24	DESKEW_LANE_NUMBER	Deskew lane number
19:16	DESKEW_DELAY_APPLY_MODE	Deskew delay apply mode
14:8	DESKEW_DETECTION_CNT	Deskew detection count
3:0	DESKEW_DETECTION_MODE	Deskew detection mode

1A0438C0 MIPI_RX_CONC0_CSI3 **Interrupt enable** **80000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DESKEW_INTERRUPT_W1C_EN															
Type	RW															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DESKEW_INTERRUPT_ENABLE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	DESKEW_INTERRUPT_W1C_EN	Interrupt W1C enable
7:0	DESKEW_INTERRUPT_ENABLE	Interrupt enable

1A0438C4 MIPI_RX_CONC4_CSI3 **Interrupt status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DESKEW_INTERRUPT_STATUS							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DESKEW_INTERRUPT_STATUS	Interrupt status

1A0438C8 MIPI_RX_CONC8_CSI3 Debug mux select 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DESKEW_DEBUG_MUX_SELECT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DESKEW_DEBUG_MUX_SELECT	Debug signal select

1A0438CC MIPI_RX_CONCC_CSI3 Debug outputs 00100100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DESKEW_DEBUG_OUTPUTS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DESKEW_DEBUG_OUTPUTS															
Type	RO															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DESKEW_DEBUG_OUTPUTS	Debug signal outputs

1A0438D0 MIPI_RX_COND0_CSI3 Deskew delay length 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DESKEW_DELAY_LENGTH						
Type											RW					
Reset											0	0	1	1	1	1

Bit(s)	Name	Description
5:0	DESKEW_DELAY_LENGTH	**Deskew delay length**

Module name: seninf4_mux Base address: (+1a043d00h)

Address	Name	Width	Register Function
1A043D00	SENINF4_MUX_CTRL	32	SENINF 4 Control Register
1A043D04	SENINF4_MUX_INTEN	32	SENINF 4 Interrupt Enable Register
1A043D08	SENINF4_MUX_INTSTA	32	SENINF 4 Interrupt Status Register
1A043D0C	SENINF4_MUX_SIZE	32	SENINF 4 Image Size Register
1A043D10	SENINF4_MUX_DEBUG_1	32	SENINF 4 Debug Register 1
1A043D14	SENINF4_MUX_DEBUG_2	32	SENINF 4 Debug Register 2
1A043D18	SENINF4_MUX_DEBUG_3	32	SENINF 4 Debug Register 3
1A043D1C	SENINF4_MUX_DEBUG_4	32	SENINF 4 Debug Register 4
1A043D20	SENINF4_MUX_DEBUG_5	32	SENINF 4 Debug Register 5
1A043D24	SENINF4_MUX_DEBUG_6	32	SENINF 4 Debug Register 6
1A043D28	SENINF4_MUX_DEBUG_7	32	SENINF 4 Debug Register 7
1A043D2C	SENINF4_MUX_SPARE	32	SENINF 4 Spare Register
1A043D30	SENINF4_MUX_DATA	32	SENINF 4 Data Register
1A043D34	SENINF4_MUX_DATA_CNT	32	SENINF 4 Data Count Register
1A043D38	SENINF4_MUX_CROP	32	SENINF 4 Crop Size Register
1A043D3C	SENINF4_MUX_CTRL_EXT	32	SENINF 4 Control Register Extend

1A043D00 SENINF4_MUX_CTRL **SENINF 4 Control Register** **06DF0080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_MUX_EN	CROP_EN	FIFO_FULL_WR_EN		FIFO_FLUSH_EN						FIFO_PUSH_EN					
Type	RW	RW	RW		RW						RW					
Reset	0	0	0	0	0	1	1	0	1	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_SRC_SEL				OVERRUN_RST	SENINF_HSYNC	SENINF_VSYNC	SENINF_PIX_S	SENINF_HSYNC		SENINF_MUX_R	SENINF_MUX_R			SENINF_IRQ_S	SENINF_MUX_S

					EN	_POL	_POL	EL	_MASK		DY_VALUE	DY_MODE			W_RST	W_RST
Type	RW				RW	RW	RW	RW	RW		RW	RW			RW	RW
Reset	0	0	0	0	0	0	0	0	1		0	0			0	0

Bit(s)	Name	Description
31	SENINF_MUX_EN	**Enables seninf_mux** 0: Disable 1: Enable
30	CROP_EN	**Sensor crop function**
29:28	FIFO_FULL_WR_EN	0: FIFO write operation is prohibited when FIFO is full. 1: FIFO write operation is prohibited after FIFO full occurs. 2: FIFO write operation is allowed when FIFO is full.
27:22	FIFO_FLUSH_EN	**Normal mode: 6'b011011** JPEG two pixel mode: 6'b011000
21:16	FIFO_PUSH_EN	**Normal mode: 6'b011111** JPEG two pixel mode : 6'b011110
15:12	SENINF_SRC_SEL	**Selects SENINF input source:** {seninf_mux_sel_ext, seninf_mux_sel} 00: OCSI2 VC0 01: Test model 02: CCIR656 03: Parallel sensor 04: Serial sensor 06: OCSI2 VC1 08: NCSI2 VC0 09: NCSI2 VC1 0A: NCSI2 VC2 0B: NCSI2 VC3 0C: NCSI2 VC4 0D: NCSI2 VC5
11	OVERRUN_RST_EN	**Enables SENINF mux software reset for overrun** 0: No action 1: Auto self-reset for overrun situation
10	SENINF_HSYNC_POL	**SENINF HSYNC polarity**
9	SENINF_VSYNC_POL	**SENINF VSYNC polarity**
8	SENINF_PIX_SEL	**SENINF output bus width:** {seninf_pixel_sel_ext, seninf_pixel_sel} 00: 1 pixel/cycle 01: 2 pixels/cycle 10: 4 pixels/cycle
7	SENINF_HSYNC_MASK	**Masks hsync** 0: Send hsync when vsync = 1 1: Does not send hsync when vsync = 1
5	SENINF_MUX_RDY_VALUE	**seninf_rdy value in force mode**
4	SENINF_MUX_RDY_MODE	0: seninf_rdy normal mode 1: seninf_rdy force mode
1	SENINF_IRQ_SW_RST	**SENINF IRQ software reset, active high** 0: De-assert reset 1: Assert reset
0	SENINF_MUX_SW_RST	**SENINF mux software reset, active high** 0: De-assert reset 1: Assert reset

1A043D04 SENINF4_MU **SENINF 4 Interrupt Enable** **8000007F**

X_INTEN Register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_IRQ_CLR_SEL															
Type	RW															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SENINF_SENSOR_HSIZEERR_IRQ_EN	SENINF_SENSOR_VSIZEERR_IRQ_EN	SENINF_HSIZEERR_IRQ_EN	SENINF_VSIZEERR_IRQ_EN	SENINF_FSMERR_IRQ_EN	SENINF_CRCERR_IRQ_EN	SENINF_OVERRUN_IRQ_EN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										1	1	1	1	1	1	1

Bit(s)	Name	Description
31	SENINF_IRQ_CLR_SEL	0: Read clear 1: Write clear
6	SENINF_SENSOR_HSIZEERR_IRQ_EN	Enables sensor HSIZE ERROR IRQ
5	SENINF_SENSOR_VSIZEERR_IRQ_EN	Enables sensor VSIZE ERROR IRQ
4	SENINF_HSIZEERR_IRQ_EN	Enables async FIFO HSIZE ERROR IRQ
3	SENINF_VSIZEERR_IRQ_EN	Enables async FIFO VSIZE ERROR IRQ
2	SENINF_FSMERR_IRQ_EN	Enables FSM ERROR IRQ
1	SENINF_CRCERR_IRQ_EN	Enables CRR ERROR IRQ
0	SENINF_OVERRUN_IRQ_EN	Enables FIFO OVERRUN IRQ

1A043D08 SENINF4_MUX_INTSTA SENINF 4 Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SENINF_SENSOR_HSIZEERR_IRQ_STA	SENINF_SENSOR_VSIZEERR_IRQ_STA	SENINF_HSIZEERR_IRQ_STA	SENINF_VSIZEERR_IRQ_STA	SENINF_FSMERR_IRQ_STA	SENINF_CRCERR_IRQ_STA	SENINF_OVERRUN_IRQ_STA
Type										RO	RO	RO	RO	RO	RO	RO
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	SENINF_SENSOR_HSIZEERR_IRQ_STA	Sensor HSIZE ERROR IRQ status
5	SENINF_SENSOR_VSIZEERR_IRQ_STA	Sensor VSIZE ERROR IRQ status

Bit(s)	Name	Description
4	SENINF_HSIZEERR_IRQ_STA	Async FIFO HSIZE ERROR IRQ status
3	SENINF_VSIZEERR_IRQ_STA	Async FIFO VSIZE ERROR IRQ status
2	SENINF_FSMERR_IRQ_STA	FSM ERROR IRQ status
1	SENINF_CRCERR_IRQ_STA	CRR ERROR IRQ status
0	SENINF_OVERRUN_IRQ_STA	FIFO OVERRUN IRQ status

1A043D0C SENINF4_MUX_SIZE — SENINF 4 Image Size Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_HSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_VSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_HSIZE	Senor image horizontal size
15:0	SENINF_VSIZE	Senor image vertical size

1A043D10 SENINF4_MUX_DEBUG_1 — SENINF 4 Debug Register 1 — 0000C303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	1	1	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A043D14 SENINF4_MUX_DEBUG_2 — SENINF 4 Debug Register 2 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A043D18 SENINF4_MUX_DEBUG_3 SENINF 4 Debug Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A043D1C SENINF4_MUX_DEBUG_4 SENINF 4 Debug Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A043D20 SENINF4_MUX_DEBUG_5 SENINF 4 Debug Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A043D24 SENINF4_MU SENINF 4 Debug Register 6 00000000

X_DEBUG_6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A043D28 SENINF4_MUX_DEBUG_7 **SENINF 4 Debug Register 7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A043D2C SENINF4_MUX_SPARE **SENINF 4 Spare Register** **000E2000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SENI NF_S PARE			
Type													RW			
Reset													1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENI NF_S PARE		SENI NF_F IFO_ FULL _SEL	SENI NF_V CNT_ SEL		SENINF_CR C_SEL										
Type	RW		RW	RW		RW										
Reset	0	0	1	0	0	0	0									

Bit(s)	Name	Description
19:14	SENINF_SPARE	**Spare register**
13	SENINF_FIFO_FULL_SEL	0: Does not send FIFO full to cam 1: Send FIFO full to cam
12:11	SENINF_VCNT_SEL	0: Vsync rising 1: Vsync rising d1 2: Vsync rising d2 3: Vsync rising d3

Bit(s)	Name	Description
10:9	SENINF_CRC_SEL	0: Vsync rising 1: Vsync rising d1 2: Vsync rising d2 3: Vsync rising d3

1A043D30 SENINF4_MUX_DATA SENINF 4 Data Register 40000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA1															
Type	RO															
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_DATA1	
15:0	SENINF_DATA0	

1A043D34 SENINF4_MUX_DATA_CNT SENINF 4 Data Count Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENINF_DATA_CNT	

1A043D38 SENINF4_MUX_CROP SENINF 4 Crop Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_CROP_X2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_CROP_X1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_CROP_X2	

Bit(s)	Name	Description
15:0	SENINF_CROP_X1	

1A043D3C SENINF4_MUX_CTRL_EXT **SENINF 4 Control Register Extend** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												SENINF_PIX_SEL_EXT			SENINF_SRC_SEL_EXT	
Type												RW			RW	
Reset												0			0	0

Bit(s)	Name	Description
4	SENINF_PIX_SEL_EXT	**SENINF output bus width:** {seninf_pixel_sel_ext, seninf_pixel_sel} 00: One pixel/cycle 01: Two pixels/cycle 10: four pixels/cycle
1:0	SENINF_SRC_SEL_EXT	**Selects SENINF input source:** {seninf_src_sel_ext, seninf_src_sel} 18: CSI2 VC0 19: CSI2 VC1 1A: CSI2 VC2 1B: CSI2 VC3 1C: CSI2 VC4 28: CSI3 VC0 29: CSI3 VC1 2A: CSI3 VC2 2B: CSI3 VC3 2C: CSI3 VC4

Module name: SENINF4_NCSI2 Base address: (+1a043700h)

Address	Name	Width	Register Function
1A043700	SENINF4_NCSI2_CTL	32	CSI2 Function Enable
1A043704	SENINF4_NCSI2_LNRC_TIMING	32	CSI2 Clock Lane Timing Parameters
1A043708	SENINF4_NCSI2_LNRD_TIMING	32	CSI2 Data Lane Timing Parameters
1A04370C	SENINF4_NCSI2_DPCM	32	CSI2 DPCM Parameters
1A043710	SENINF4_NCSI2_INT_EN	32	CSI2 Interrupt Enable
1A043714	SENINF4_NCSI2_INT_STATUS	32	CSI2 Interrupt Status
1A043718	SENINF4_NCSI2_DGB_SEL	32	CSI2 Debug Selection

Address	Name	Width	Register Function
1A04371C	SENINF4_NCSI2_DBG_PORT	32	CSI2 Debug Port
1A043720	SENINF4_NCSI2_SPARE0	32	SPARE0
1A043724	SENINF4_NCSI2_SPARE1	32	SPARE1
1A043728	SENINF4_NCSI2_LNRC_FSM	32	CSI2 Clock Lane RX FSM
1A04372C	SENINF4_NCSI2_LNRD_FSM	32	CSI2 Data Lane RX FSM
1A043730	SENINF4_NCSI2_FRAME_LINE_NUM	32	CSI2 Frame/Line Number
1A043734	SENINF4_NCSI2_GENERIC_SHORT	32	CSI2 Generic Short Packet
1A043738	SENINF4_NCSI2_HSRX_DBG	32	CSI2 HSRX Enable
1A04373C	SENINF4_NCSI2_DI	32	CSI2 Data Interleaving Parameters
1A043740	SENINF4_NCSI2_HS_TRAIL	32	CSI2 HS Trail Timing Parameters
1A043744	SENINF4_NCSI2_DI_CTRL	32	CSI2 Data Interleaving Control
1A043748	SENINF4_NCSI2_DI_1	32	CSI2 Data Interleaving Parameters
1A04374C	SENINF4_NCSI2_DI_CTRL_1	32	CSI2 Data Interleaving Control
1A043750	SENINF4_NCSI2_DPHY_RESYNC_CTL	32	CSI2 DPHY Lane Resync Control

1A043700 SENINF4_NCSI2_CTL **CSI2 Function Enable** **018861E0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			VS_OUT_CYCLE_NUMBER		CLOCK_HS_OPTION	REF_SYNC_DET_EN	HS_TRAIL_EN	ASYNC_FIFO_RST_SCH		SYNC_DET_BIT_SWAP_EN	SYNC_DET_EN	SYNC_DET_SCHEME	FLUSH_MODE			SED_SEL
Type			RW		RW	RW	RW	RW		RW	RW	RW	RW			RW
Reset			0	0	0	0	0	1	1	0	0	0	1	0		0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VS_TYPE	BYTE2PIXEL_EN	IMAGE_PACKET_EN	GENERIC_LONG_PACKET_EN			HS_END_EN	HS_PRPR_EN	HSRX_DET_EN	CRC_EN	ECC_EN	CLOCK_LANE_EN	DATA_LANE3_EN	DATA_LANE2_EN	DATA_LANE1_EN	DATA_LANE0_EN
Type	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	1	1	0			0	1	1	1	1	0	0	0	0	0

Bit(s)	Name	Description
29:28	VS_OUT_CYCLE_NUMBER	0: 4T 1: 8T
27	CLOCK_HS_OPTION	0: Enable clock lane HS based on LP11, LP01, LP00 1: Enable clock lane HS based on LP00

Bit(s)	Name	Description
26	REF_SYNC_DET_EN	**Reference sync detect signal to do analog sync**
25	HS_TRAIL_EN	**Extends HS trail**
24:23	ASYNC_FIFO_RST_SCH	
22	SYNC_DET_BITSWAP_EN	
21	SYNC_DET_EN	**Enables sync sequence detection**
20	SYNC_DET_SCHEME	0: B8 1: 101110
19:18	FLUSH_MODE	0: Disable 1: Flush at first cycle of LP11 2: Flush at LP11 3: Reserved
16	ED_SEL	0: {WCH,WCL,DI} 1: {DI,WCL,WCH}
15	VS_TYPE	**VS type** 0: 4T 1: Frame start to frame end
14	BYTE2PIXEL_EN	**Byte 2 pixel conversion**
13	IMAGE_PACKET_EN	**Image data types**
12	GENERIC_LONG_PACKET_EN	**Generic long packet data types**
9	HS_END_EN	**Enables HS_EX reset at packet end**
8	HS_PRPR_EN	**Enables RX_HS_PRPR state**
7	HSRX_DET_EN	**Enables HSRX termination auto-detection flow**
6	CRC_EN	**Enables checksum**
5	ECC_EN	**Enables packet header ECC**
4	CLOCK_LANE_EN	**Enables clock lane**
3	DATA_LANE3_EN	**Enables data lane 3**
2	DATA_LANE2_EN	**Enables data lane 2**
1	DATA_LANE1_EN	**Enables data lane 1**
0	DATA_LANE0_EN	**Enables data lane 0**

1A043704 SENINF4_NCSI2_LNRC_TIMING **CSI2 Clock Lane Timing Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SETTLE_PARAMETER								TERM_PARAMETER							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	SETTLE_PARAMETER	TD_SETTLE parameter
7:0	TERM_PARAMETER	TD_TERM_EN parameter

1A043708 SENINF4_NCSI2_LNRD_TIMING **CSI2 Data Lane Timing Parameters** **00002000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SETTLE_PARAMETER								TERM_PARAMETER							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	SETTLE_PARAMETER	TD_SETTLE parameter
7:0	TERM_PARAMETER	TD_TERM_EN parameter

1A04370C SENINF4_NCSI2_DPCM — CSI2 DPCM Parameters — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DI_2A_DPCM_EN	DI_37_DPCM_EN	DI_36_DPCM_EN	DI_35_DPCM_EN	DI_34_DPCM_EN	DI_33_DPCM_EN	DI_32_DPCM_EN	DI_31_DPCM_EN	DI_30_DPCM_EN				DPCM_MODE			
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW				RW			
Reset	0	0	0	0	0	0	0	0	0				0	0	0	0

Bit(s)	Name	Description
15	DI_2A_DPCM_EN	**Enables DPCM**
14	DI_37_DPCM_EN	**Enables DPCM**
13	DI_36_DPCM_EN	**Enables DPCM**
12	DI_35_DPCM_EN	**Enables DPCM**
11	DI_34_DPCM_EN	**Enables DPCM**
10	DI_33_DPCM_EN	**Enables DPCM**
9	DI_32_DPCM_EN	**Enables DPCM**
8	DI_31_DPCM_EN	**Enables DPCM**
7	DI_30_DPCM_EN	**Enables DPCM**
3:0	DPCM_MODE	0: 10-8-10

1A043710 SENINF4_NCSI2_INT_EN — CSI2 Interrupt Enable — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_WCLR_EN					DPHY3_RESYNC_FIFO_OVERFLOW	DPHY2_RESYNC_FIFO_OVERFLOW	DPHY1_RESYNC_FIFO_OVERFLOW	DPHY0_RESYNC_FIFO_OVERFLOW	ERR_LANE_RESYNC	ERR_FRAME_SYNC_S5	ERR_FRAME_SYNC_S4	ERR_FRAME_SYNC_S3	ERR_FRAME_SYNC_S2	ERR_FRAME_SYNC_S1	ERR_FRAME_SYNC_S0
Type	RW					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0					0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GS	LS	FS	ERR_SOT_SYNC_HS_	ERR_SOT_SYNC_HS_	ERR_SOT_SYNC_HS_	ERR_SOT_SYNC_HS_	ERR_MULTI_LANE_S	ERR_AFIFO	ERR_CRC	ERR_ECC_DOUBLE	ERR_ECC_CORRECTE	ERR_ECC_NO_ERROR	ERR_ID	ERR_FRAME_SYNC

					LNRD3	LNRD2	LNRD1	LNRD0	YNC				D			
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	INT_WCLR_EN	Enables interrupt write clear
26	DPHY3_RESYNC_FIFO_OVERFLOW	Enables LANE3_RESYNC_FIFO_OVERFLOW interrupt
25	DPHY2_RESYNC_FIFO_OVERFLOW	Enables LANE2_RESYNC_FIFO_OVERFLOW interrupt
24	DPHY1_RESYNC_FIFO_OVERFLOW	Enables LANE1_RESYNC_FIFO_OVERFLOW interrupt
23	DPHY0_RESYNC_FIFO_OVERFLOW	Enables LANE0_RESYNC_FIFO_OVERFLOW interrupt
22	ERR_LANE_RESYNC	Enables ERR_LANE_RESYNC interrupt
21	ERR_FRAME_SYNC_S5	Enables ERR_FRAME_SYNC interrupt
20	ERR_FRAME_SYNC_S4	Enables ERR_FRAME_SYNC interrupt
19	ERR_FRAME_SYNC_S3	Enables ERR_FRAME_SYNC interrupt
18	ERR_FRAME_SYNC_S2	Enables ERR_FRAME_SYNC interrupt
17	ERR_FRAME_SYNC_S1	Enables ERR_FRAME_SYNC interrupt
16	ERR_FRAME_SYNC_S0	Enables ERR_FRAME_SYNC interrupt
14	GS	Enables generic short packet interrupt
13	LS	Enables line start interrupt
12	FS	Enables frame start interrupt
11	ERR_SOT_SYNC_HS_LNRD3	Enables ERR_SOT_SYNC_HS interrupt
10	ERR_SOT_SYNC_HS_LNRD2	Enables ERR_SOT_SYNC_HS interrupt
9	ERR_SOT_SYNC_HS_LNRD1	Enables ERR_SOT_SYNC_HS interrupt
8	ERR_SOT_SYNC_HS_LNRD0	Enables ERR_SOT_SYNC_HS interrupt
7	ERR_MULTI_LANE_SYNC	Enables ERR_MULTI_LANE_SYNC interrupt
6	ERR_AFIFO	Enables ERR_AFIFO interrupt
5	ERR_CRC	Enables ERR_CRC interrupt
4	ERR_ECC_DOUBLE	Enables ERR_ECC_DOUBLE interrupt
3	ERR_ECC_CORRECTED	Enables ERR_ECC_CORRECTED interrupt
2	ERR_ECC_NO_ERROR	ERR_ECC_NO_ERROR interrupt
1	ERR_ID	Enables ERR_ID interrupt
0	ERR_FRAME_SYNC	Enables ERR_FRAME_SYNC interrupt

1A043714 SENINF4_NCSI2_INT_STATUS CSI2 Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						DPHY3_RESYNC_FIFO_OVERFLOW_STA	DPHY2_RESYNC_FIFO_OVERFLOW_STA	DPHY1_RESYNC_FIFO_OVERFLOW_STA	DPHY0_RESYNC_FIFO_OVERFLOW_STA	ERR_LANE_RESYNC_STA	ERR_FRAME_SYNC_S5	ERR_FRAME_SYNC_S4	ERR_FRAME_SYNC_S3	ERR_FRAME_SYNC_S2	ERR_FRAME_SYNC_S1	ERR_FRAME_SYNC_S0
Type						RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GS	LS	FS	ERR_SOT_SYNC_HS_LNRD3	ERR_SOT_SYNC_HS_LNRD2	ERR_SOT_SYNC_HS_LNRD1	ERR_SOT_SYNC_HS_LNRD0	ERR_MULTI_LANE_SYNC	ERR_AFIFO	ERR_CRC	ERR_ECC_DOUBLE	ERR_ECC_CORRECTED	ERR_ECC_NO_ERROR	ERR_ID	ERR_FRAME_SYNC

Type		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26	DPHY3_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of DPHY lane3 is overflowed**
25	DPHY2_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of DPHY lane2 is overflowed**
24	DPHY1_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of DPHY lane1 is overflowed**
23	DPHY0_RESYNC_FIFO_OVERFLOW_STA	**Asserted when the resync FIFO of DPHY lane0 is overflowed**
22	ERR_LANE_RESYNC_STA	**Asserted when DPHY lane sync detect time is longer than set resync cycles**
21	ERR_FRAME_SYNC_S5	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
20	ERR_FRAME_SYNC_S4	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
19	ERR_FRAME_SYNC_S3	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
18	ERR_FRAME_SYNC_S2	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
17	ERR_FRAME_SYNC_S1	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
16	ERR_FRAME_SYNC_S0	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**
14	GS	**Enables generic short packet interrupt**
13	LS	**Line start interrupt**
12	FS	**Frame start interrupt**
11	ERR_SOT_SYNC_HS_LNRD3	**Asserted when proper synchronization cannot be expected**
10	ERR_SOT_SYNC_HS_LNRD2	**Asserted when proper synchronization cannot be expected**
9	ERR_SOT_SYNC_HS_LNRD1	**Asserted when proper synchronization cannot be expected**
8	ERR_SOT_SYNC_HS_LNRD0	**Asserted when proper synchronization cannot be expected**
7	ERR_MULTI_LANE_SYNC	**Asserted when multiple lane synchronization fails**
6	ERR_AFIFO	**Asserted when error occurs in asynchronous FIFO**
5	ERR_CRC	**Asserted when computed CRC code is different from received CRC code**
4	ERR_ECC_DOUBLE	**Asserted when an ECC syndrome is computed and two bit errors are detected in the received packet header**
3	ERR_ECC_CORRECTED	**Asserted when an ECC syndrome is computed and a single bit error in the packet header is detected and corrected**
2	ERR_ECC_NO_ERROR	**Asserted when an ECC syndrome is computed and the result is zero indicating a packet header that is considered to be without errors or has more than two bit errors** CSI-2's ECC mechanism cannot detect this type of error.
1	ERR_ID	**Asserted whean a packet header is decoded with an unrecognized or unimplemented data ID**
0	ERR_FRAME_SYNC	**Asserted when a Frame End is not paired with a Frame Start on the same virtual channel**

1A043718 SENINF4_NC CSI2 Debug Selection 00000000

SI2_DGB_SEL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DEBUG_SEL							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DEBUG_SEL	Selects debug

1A04371C SENINF4_NCSI2_DBG_PORT CSI2 Debug Port 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CTL_DBG_PORT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	CTL_DBG_PORT	Debug port

1A043720 SENINF4_NCSI2_SPARE0 SPARE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE0	Spare register

1A043724 SENINF4_NCSI2_SPARE1 SPARE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE1	Spare register

1A043728 SENINF4_NCSI2_LNRC_FSM CSI2 Clock Lane RX FSM 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											LNRC_RX_FSM					
Type											RO					
Reset											0	0	0	0	0	1

Bit(s)	Name	Description
5:0	LNRC_RX_FSM	RX FSM of clock lane

1A04372C SENINF4_NCSI2_LNRD_FSM CSI2 Data Lane RX FSM 01010101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LNRD3_RX_FSM								LNRD2_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		LNRD1_RX_FSM								LNRD0_RX_FSM						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1

Bit(s)	Name	Description
30:24	LNRD3_RX_FSM	RX FSM of data lane 3
22:16	LNRD2_RX_FSM	RX FSM of data lane 2
14:8	LNRD1_RX_FSM	RX FSM of data lane 1
6:0	LNRD0_RX_FSM	RX FSM of data lane 0

1A043730 SENINF4_NCSI2_FRAME_LINE_NUM CSI2 Frame/Line Number 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LINE_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FRAME_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	LINE_NUM	Line number
15:0	FRAME_NUM	Frame number

1A043734 SENINF4_NCSI2_GENERIC_SHORT — CSI2 Generic Short Packet — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GENERIC_SHORT_PACKET_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											GENERIC_SHORT_PACKET_DT						
Type											RO					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
31:16	GENERIC_SHORT_PACKET_DATA	Generic short packet data
5:0	GENERIC_SHORT_PACKET_DT	Generic short packet data

1A043738 SENINF4_NCSI2_HSRX_DBG — CSI2 HSRX Enable — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLOCK_LANE_HSRX_EN	DATA_LANE3_HSRX_EN	DATA_LANE2_HSRX_EN	DATA_LANE1_HSRX_EN	DATA_LANE0_HSRX_EN
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	CLOCK_LANE_HSRX_EN	Enables clock lane HSRX circut
3	DATA_LANE3_HSRX_EN	Enables data lane 3 HSRX circuit
2	DATA_LANE2_HSRX_EN	Enables data lane 2 HSRX circuit
1	DATA_LANE1_HSRX_EN	Enables data lane 1 HSRX circuit

Bit(s)	Name	Description
0	DATA_LANE0_HSRX_EN	Enables data lane 0 HSRX circuit

1A04373C SENINF4_NCSI2_DI — CSI2 Data Interleaving Parameters — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DT3						VC3		DT2						VC2	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DT1						VC1		DT0						VC0	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:26	DT3	Data type identifier
25:24	VC3	Virtual channel identifier
23:18	DT2	Data type identifier
17:16	VC2	Virtual channel identifier
15:10	DT1	Data type identifier
9:8	VC1	Virtual channel identifier
7:2	DT0	Data type identifier
1:0	VC0	Virtual channel identifier

1A043740 SENINF4_NCSI2_HS_TRAIL — CSI2 HS Trail Timing Parameters — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									HS_TRAIL_PARAMETER							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	HS_TRAIL_PARAMETER	HS trail parameter

1A043744 SENINF4_NCSI2_DI_CTRL — CSI2 Data Interleaving Control — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						DT3_INTERLEAVING		VC3_INTERLEAVING						DT2_INTERLEAVING		VC2_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DT1_INTERLEAVING		VC1_INTERLEAVING						DT0_INTERLEAVING		VC0_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0

Bit(s)	Name	Description
26:25	DT3_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
24	VC3_INTERLEAVING	**Virtual channel identifier interleaving**
18:17	DT2_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
16	VC2_INTERLEAVING	**Virtual channel identifier interleaving**
10:9	DT1_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
8	VC1_INTERLEAVING	**Virtual channel identifier interleaving**
2:1	DT0_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
0	VC0_INTERLEAVING	**Virtual channel identifier interleaving**

1A043748 SENINF4_NCSI2_DI_1 **CSI2 Data Interleaving Parameters** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DT5						VC5		DT4						VC4	
Type	RW						RW		RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:10	DT5	Data type identifier
9:8	VC5	Virtual channel identifier
7:2	DT4	Data type identifier
1:0	VC4	Virtual channel identifier

1A04374C SENINF4_NCSI2_DI_CTRL_1 **CSI2 Data Interleaving Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DT5_INTERLEAVING		VC5_INTERLEAVING						DT4_INTERLEAVING		VC4_INTERLEAVING
Type						RW		RW						RW		RW
Reset						0	0	0						0	0	0

Bit(s)	Name	Description
10:9	DT5_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
8	VC5_INTERLEAVING	**Virtual channel identifier interleaving**
2:1	DT4_INTERLEAVING	**Data type interleaving** 0: Disable 1: Include 2: Exclude
0	VC4_INTERLEAVING	**Virtual channel identifier interleaving**

1A043750 SENINF4_NCSI2_DPHY_RESYNC_CTL **CSI2 DPHY Lane Resync Control** **00000101**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DPHY_RESYNC_CNT								DPHY_RESYNC_FLUSH_EN	DPHY_RESYNC_DATAOUT_OPTION	DPHY_BYPASS_LANE_RESYNC
Type						RW								RW	RW	RW
Reset						0	0	1						0	0	1

Bit(s)	Name	Description
10:8	DPHY_RESYNC_CNT	Detect lane skew cycle count
2	DPHY_RESYNC_FLUSH_EN	Enables lane resync flush
1	DPHY_RESYNC_DATAOUT_OPTION	Data output option
0	DPHY_BYPASS_LANE_RESYNC	Bypass lane resync function

Module name: seninf4_ocsi2 Base address: (+1a043300h)

Address	Name	Width	Register Function
1A043360	SENINF4_OCSI2_CTRL	32	CSI2 Control Register
1A043364	SENINF4_OCSI2_	32	CSI2 Delay Control Register

Address	Name	Width	Register Function
	DELAY		
1A043368	SENINF4_OCSI2_INTEN	32	CSI2 Interrupt Enable Register
1A04336C	SENINF4_OCSI2_INTSTA	32	CSI2 Interrupt Status Register
1A043370	SENINF4_OCSI2_ECCDBG	32	CSI2 ECC Debug Register
1A043374	SENINF4_OCSI2_CRCDBG	32	CSI2 CRC Debug Register
1A043378	SENINF4_OCSI2_DBG	32	CSI2 Debug Register
1A04337C	SENINF4_OCSI2_VER	32	CSI2 Version Code Register
1A043380	SENINF4_OCSI2_SHORT_INFO	32	CSI2 Short Packet Information Register
1A043384	SENINF4_OCSI2_LNFSM	32	CSI2 Lane FSM Register
1A043388	SENINF4_OCSI2_LNMUX	32	CSI2 Lane Mux Register
1A04338C	SENINF4_OCSI2_HSYNC_CNT	32	CSI2 Hsync Counter Register
1A043390	SENINF4_OCSI2_CAL	32	CSI2 Calibration Register
1A043394	SENINF4_OCSI2_DS	32	CSI2 Downsample Register
1A043398	SENINF4_OCSI2_VS	32	CSI2 Vsync Register
1A04339C	SENINF4_OCSI2_BIST	32	CSI2 BIST Register

1A043360 SENINF4_OCSI2_CTRL CSI2 Control Register 00002D80

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_BIST_CSI2_DATA_OK	CSI2_LANE_FSM_OK	CSI2_HS_FSM_OK	CSI2_BIST_DATA_OK	CSI2_BIST_START	CSI2_BIST_ERROR_COUNT								CSI2_DATA_FLOW		CSI2_ASYNC_OPTION
Type	RO	RO	RO	RO	RO	RO								RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_SYNC_CLR_EXTEND	CSI2_HSRXEN_PFOOT_CLR	CSI2_VSYNC_TYPE	CSI2_SW_RST	CSI2_SCLK4X_SEL	CSI2_SCLK_SEL	CSI2_ESC_EN	CSI2_SYNC_RST_EN	CSI2_LP11_RST_EN	CSI2_CLK_MISS_EN	CSI2_ED_SEL	CSI2_ECC_EN	DLANE3_EN	DLANE2_EN	DLANE1_EN	CSI2_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	1	0	1	1	0	1	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	CSI2_BIST_CSI2_DATA_OK	**CSI2 BIST CSI2 data ok**
30	CSI2_LANE_FSM_OK	**CSI2 BIST data lane FSM ok**

Bit(s)	Name	Description
29	CSI2_HS_FSM_OK	**CSI2 BIST high speed FSM ok**
28	CSI2_BIST_DATA_OK	**CSI2 BIST DPHY data ok**
27	CSI2_BIST_START	**CSI2 BIST start status**
26:19	CSI2_BIST_ERROR_COUNT	**CSI2 bist test error count**
18:17	CSI2_DATA_FLOW	**CSI2 data flow** 0: Data packet 1: Generic long packet 2: All data packet
16	CSI2_ASYNC_OPTION	
15	CSI2_SYNC_CLR_EXTEND	
14	CSI2_HSRXEN_PFOOT_CLR	
13	CSI2_VSYNC_TYPE	**VSYNC type to CAM module** 0: High from short packet "frame start" to short packet "frame end" 1: 4T pulse after short packet "frame start"
12	CSI2_SW_RST	**CSI2 software reset, active high** 0: De-assert reset 1: Assert reset
11	CSI2_SCLK4X_SEL	**Selects CSI2 4x sample clock** 0: Invert 1: Does not invert csi2_clk from D-PHY
10	CSI2_SCLK_SEL	**Selects CSI2 sample clock** 0: Invert 1: Does not invert csi2_clk from D-PHY
9	CSI2_ESC_EN	**Enables CSI2 Escape mode**
8	CSI2_SYNC_RST_EN	**When this bit is set high, data high speed FSM will enter state "SYNC" whenever sync code is seen.** Used in case packet ends unexpectedly.
7	CSI2_LP11_RST_EN	**When this bit is set high, data/clk lane FSM will enter state "STOP" whenever LP-11 is seen.** Used in case low power and high speed state transition is unexpected.
6	CSI2_CLK_MISS_EN	**Enables high speed mode clock miss monitoring**
5	CSI2_ED_SEL	**Selects CSI2 header format**
4	CSI2_ECC_EN	**Enables CSI2 ECC**
3	DLANE3_EN	**Enables CSI2 3 data lane**
2	DLANE2_EN	**Enables CSI2 2 data lane**
1	DLANE1_EN	**Enables CSI2 1 data lane**
0	CSI2_EN	**Enables CSI2 0 data lane**

1A043364 SENINF4_CSI2_DELAY CSI2 Delay Control Register 000A0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LP2HS_DATA_TERM_DELAY								LP2HS_DATA_SETTLE_DELAY							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LP2HS_CLK_TERM_DELAY							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	LP2HS_DATA_TERM_DELAY	CSI2 data lane low power to high speed termination enable delay count
23:16	LP2HS_DATA_SETTLE_DELAY	CSI2 data lane low power to high speed sync code search delay

Bit(s)	Name	Description
7:0	LP2HS_CLK_TERM_DELAY	CSI2 CLK lane low power to high speed termination enable delay count

1A043368 SENINF4_OCSI2_INTEN CSI2 Interrupt Enable Register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VCHANNEL_ID		CSI2_DATA_TYPE						CSI2_WC_NUMBER							
Type	RO		RO						RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_WC_NUMBER												CSI2SYNC_NONSYNC_IRQ_EN	ECC_CORRECT_IRQ_EN	ECC_ERR_IRQ_EN	CRC_ERR_IRQ_EN
Type	RO												RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0					0	1	1	1

Bit(s)	Name	Description
31:30	VCHANNEL_ID	CSI2 virtual channel identifier corrected by error correction if ECC is on
29:24	CSI2_DATA_TYPE	CSI2 long packet data type corrected by error correction if ECC is on
23:8	CSI2_WC_NUMBER	CSI2 long packet data size corrected by error correction if ECC is on
3	CSI2SYNC_NONSYNC_IRQ_EN	CSI2SYNC_NONSYNC_IRQ
2	ECC_CORRECT_IRQ_EN	Enables ECC correction interrupt
1	ECC_ERR_IRQ_EN	Enables ECC error interrupt
0	CRC_ERR_IRQ_EN	Enables CRC error interrupt

1A04336C SENINF4_OCSI2_INTSTA CSI2 Interrupt Status Register 00000070

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CSI2OUT_VSYNC	CSI2OUT_HSYNC				
Type											RO	RO				
Reset											0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CSI2_SPARE			CSI2_IRQ_CLR_SEL	CSI2SYNC_NONSYNC_IRQ	ECC_CORRECT_IRQ	ECC_ERR_IRQ	CRC_ERR_IRQ
Type									RW			RW	RO	RO	RO	RO
Reset									0	1	1	1	0	0	0	0

Bit(s)	Name	Description
21	CSI2OUT_VSYNC	**CSI2 vsync output to cam** Read only.

Bit(s)	Name	Description
20	CSI2OUT_HSYNC	**CSI2 hsync output to cam** Read only.
7:5	CSI2_SPARE	**Spare register**
4	CSI2_IRQ_CLR_SEL	0: Read clear 1: Write clear
3	CSI2SYNC_NONSYNC_IRQ	**IRQ status bit to indicate that sync between different lanes is not sampled at the same time** Write clear.
2	ECC_CORRECT_IRQ	**ECC correction interrupt status**
1	ECC_ERR_IRQ	**ECC error interrupt status**
0	CRC_ERR_IRQ	**CRC error interrupt status**

1A043370 SENINF4_OCSI2_ECCDBG CSI2 ECC Debug Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_ECCDB_BSEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_ECCDB_BSEL															CSI2_ECCDB_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
31:8	CSI2_ECCDB_BSEL	**Selects CSI2 packet header error generation bit** To generate packet header error, set one of the 24 bits to 1. Because there is only one bit error can be corrected, only one bit of the 24 bits can be 1.
0	CSI2_ECCDB_EN	**Enables CSI2 packet header error generation**

1A043374 SENINF4_OCSI2_CRCDBG CSI2 CRC Debug Register 0000000E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_CRCDB_BSEL								CSI2_CRCDB_WSEL							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_CRCDB_WSEL								CSI2_SPARE							CSI2_CRCDB_EN
Type	RW								RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Bit(s)	Name	Description
31:24	CSI2_CRCDB_BSEL	**Selects CSI2 data error generation bit** Set to 1 to generate selected word bit error. *Note: Only word number selected by csi2_crcdb_wsel will be put error on it.*
23:8	CSI2_CRCDB_WSEL	**Selects CSI2 data error generation data word**

Bit(s)	Name	Description
7:1	CSI2_SPARE	**Spare register**
0	CSI2_CRCDB_EN	**Enables CSI2 data error generation**

1A043378 SENINF4_OC SI2_DBG **CSI2 Debug Register** **00040820**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LN3_HSRXDB_EN	LN2_HSRXDB_EN	LN1_HSRXDB_EN	LN0_HSRXDB_EN	LNC_HSRXDB_EN	LN3_LPRXDB_EN	LN2_LPRXDB_EN	LN1_LPRXDB_EN	LN0_LPRXDB_EN	LNC_LPRXDB_EN		VCHANNEL_ID_EN	VCHANNEL1_ID		VCHANNEL0_ID	
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0		0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_CLK_LANE_CS					CSI2_DATA_HS_CS						CSI2_DBG_SRC_SEL				CSI2_DEBUG_ON
Type	RO					RO						RW				RW
Reset	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31	LN3_HSRXDB_EN	**Enables data lane 1 termination directly** For test only.
30	LN2_HSRXDB_EN	**Enables data lane 0 termination directly** For test only.
29	LN1_HSRXDB_EN	**Enables data lane 1 termination directly** For test only.
28	LN0_HSRXDB_EN	**Enables data lane 0 termination directly** For test only.
27	LNC_HSRXDB_EN	**Enables clock lane termination directly** For test only.
26	LN3_LPRXDB_EN	**Enables data lane 3 low power mode directly** For test only.
25	LN2_LPRXDB_EN	**Enables data lane 2 low power mode directly** For test only.
24	LN1_LPRXDB_EN	**Enables data lane 1 low power mode directly** For test only.
23	LN0_LPRXDB_EN	**Enables data lane 0 low power mode directly** For test only.
22	LNC_LPRXDB_EN	**Enables clock lane low power mode directly** For test only.
20	VCHANNEL_ID_EN	**Enables virtual channel**
19:18	VCHANNEL1_ID	**Virtual channel 1 ID**
17:16	VCHANNEL0_ID	**Virtual channel 0 ID**
15:11	CSI2_CLK_LANE_CS	**Clock lane FSM current state** 1: IDLE 2: STOP 4: HS_REQ 8: HS_PREP 16: HS_RX
10:5	CSI2_DATA_HS_CS	**Data high speed state** 1: IDLE 2: SYNC 4: PHEAD 8: PECC 16: PDATA

Bit(s)	Name	Description
		32: PFOOT
4:1	CSI2_DBG_SRC_SEL	**Selects CSI2 debug port source**
0	CSI2_DEBUG_ON	**Enables CSI2 debug** When CSI2 debug is enabled, CSI2 output raw data will include header to cam. *Note: To output CSI2 debug data,* *1. Set cam to JPEG interface mode ((CAM + 0024)[14], JPGINF_EN:1).* *2. Set up Vsync polarity ((CAM + 0010)[7], VSPOL:1).* *3. Set up output type raw data output ((CAM + 0024)[21:20] OUTPATH_TYPE:0).* *4. Set up raw data type to 8-bit mode ((CAM + 0024)[24] OUTPATH_TYPE:0).* *5. Enable ISP data output to memory ((CAM + 0024)[16],OUT_PATH_EN:1).*

1A04337C SENINF4_OCSI2_VER **CSI2 Version Code Register** **20110815**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	YEAR															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MONTH								DATE							
Type	RO								RO							
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	1

Bit(s)	Name	Description
31:16	YEAR	Year code
15:8	MONTH	Month code
7:0	DATE	Date code

1A043380 SENINF4_OCSI2_SHORT_INFO **CSI2 Short Packet Information Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_FRAME_NO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSI2_LINE_NO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	CSI2_FRAME_NO	Frame number information in short packet data type
15:0	CSI2_LINE_NO	Line number information in short packet data type

1A043384 SENINF4_OC **CSI2 Lane FSM Register** **01010101**

SI2_LNFSM

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CSI2_DATA_LN3_CS								CSI2_DATA_LN2_CS						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CSI2_DATA_LN1_CS								CSI2_DATA_LN0_CS						
Type		RO								RO						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	1

Bit(s)	Name	Description
30:24	CSI2_DATA_LN3_CS	**Data lane 3 FSM current state**
22:16	CSI2_DATA_LN2_CS	**Data lane 2 FSM current state**
14:8	CSI2_DATA_LN1_CS	**Data lane 1 FSM current state**
6:0	CSI2_DATA_LN0_CS	**Data lane 0 FSM current state** 1: IDLE 2: STOP 4: HS_REQ 8: HS_PREP 16: HS_TERM 32: HS_RX 64: HS_ESC

1A043388 SENINF4_OCSI2_LNMUX **CSI2 Lane Mux Register** **000000E4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CSI2_DATA_LN3_MUX		CSI2_DATA_LN2_MUX		CSI2_DATA_LN1_MUX		CSI2_DATA_LN0_MUX	
Type									RW		RW		RW		RW	
Reset									1	1	1	0	0	1	0	0

Bit(s)	Name	Description
7:6	CSI2_DATA_LN3_MUX	**CSI2 data lane mux** 0: LANE 0 1: LANE 1 2: LANE 2 3: LANE 3
5:4	CSI2_DATA_LN2_MUX	**CSI2 data lane mux** 0: LANE 0 1: LANE 1 2: LANE 2 3: LANE 3
3:2	CSI2_DATA_LN1_MUX	**CSI2 data lane mux** 0: LANE 0 1: LANE 1 2: LANE 2 3: LANE 3
1:0	CSI2_DATA_LN0_MUX	**CSI2 data lane mux**

Bit(s)	Name	Description
		0: LANE 0 1: LANE 1 2: LANE 2 3: LANE 3

1A04338C SENINF4_OCSI2_HSYNC_CNT CSI2 Hsync Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CSI2_HSYNC_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	CSI2_HSYNC_CNT	CSI2 hsync counter

1A043390 SENINF4_OCSI2_CAL CSI2 Calibration Register 01010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSI2_CAL_CNT_2								CSI2_CAL_CNT_1							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										CSI2_CAL_STATE						CSI2_CAL_EN
Type										RO						RW
Reset										0	0	0				0

Bit(s)	Name	Description
31:24	CSI2_CAL_CNT_2	**CSI2 calibration counter 2 (term enable to sync)** Settle delay <= CSI2 Calibration Counter 2 - Term Delay - 3 byte clk - 3 bclk - 1 bclk
23:16	CSI2_CAL_CNT_1	**CSI2 calibration counter 1 (term enable to HS00)** Term delay <= CSI2 Calibration Counter 1 - 2 byte clk - 3 bclk
6:4	CSI2_CAL_STATE	**CSI2 calibration current state**
0	CSI2_CAL_EN	**Enables CSI2 calibration**

1A043394 SENINF4_OCSI2_DS CSI2 Downsample Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CSI2_DS_CTRL		CSI2_DS_EN
Type														RW		RW
Reset														0	0	0

Bit(s)	Name	Description
2:1	CSI2_DS_CTRL	**Controls CSI2 downsample factor** 0: 1 1: 1/2 2: 1/4 3: 1/8
0	CSI2_DS_EN	**Enables CSI2 downsample**

1A043398 SENINF4_OCSI2_VS **CSI2 Vsync Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CSI2_VS_CTRL	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	CSI2_VS_CTRL	**Extends CSI2 vsync period** 0: 4T 1: 8T 2: 12T 3: 16T

1A04339C SENINF4_OCSI2_BIST **CSI2 BIST Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CSI2_BIST_LNR3_DATA_OK	CSI2_BIST_LNR2_DATA_OK	CSI2_BIST_LNR1_DATA_OK	CSI2_BIST_LNR0_DATA_OK
Type													RO	RO	RO	RO
Reset													0	0	0	0

Bit(s)	Name	Description
3	CSI2_BIST_LNR3_DATA_OK	CSI2 BIST Lane 3 DPHY data ok
2	CSI2_BIST_LNR2_DATA_OK	CSI2 BIST Lane 2 DPHY data ok
1	CSI2_BIST_LNR1_DATA_OK	CSI2 BIST Lane 1 DPHY data ok
0	CSI2_BIST_LNR0_DATA_OK	CSI2 BIST Lane 0 DPHY data ok

Module name: SENINF4_TG Base address: (+1a043600h)

Address	Name	Width	Register Function
1A043600	SENINF_TG4_PH_CNT	32	TG Phase Counter
1A043604	SENINF_TG4_SEN_CK	32	TG Sensor Clock Divider
1A043608	SENINF_TG4_TM_CTL	32	TM Control
1A04360C	SENINF_TG4_TM_SIZE	32	TM Size
1A043610	SENINF_TG4_TM_CLK	32	TM Clock
1A043614	SENINF_TG4_TM_STP	32	TG1_TM_STP

1A043600 SENINF_TG4_PH_CNT **TG Phase Counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PCEN		ADCLK_EN	CLKPOL												
Type	RW		RW	RW												
Reset	0		0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CAM_PCLK_INV	PAD_PCLK_INV	EXT_PWRDN	EXT_RST		CLKFL_POL	TGCLK_SEL	
Type									RW	RW	RW	RW		RW	RW	
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
31	PCEN	**TG phase counter enable control**
29	ADCLK_EN	**Enables sensor master clock (mclk) output to sensor**
28	CLKPOL	**Controls sensor master clock polarity**
7	CAM_PCLK_INV	**Inverts pixel clock in CAM**
6	PAD_PCLK_INV	**Inverts pixel clock in PAD side**
5	EXT_PWRDN	**Powers down sensor**
4	EXT_RST	**Resets sensor**
2	CLKFL_POL	**Sensor clock falling edge polarity**
1:0	TGCLK_SEL	**Selects sensor master clock** 0: isp_clk 1: cam_pll 2: 3rd clock source

1A043604 SENINF_TG4 **TG Sensor Clock Divider** **00010001**

_SEN_CK

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CLKCNT					
Type											RW					
Reset											0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			CLKRS								CLKFL					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	1

Bit(s)	Name	Description
21:16	CLKCNT	**Controls sensor master clock frequency divider** Sensor master clock = ISP_clock/(CLKCNT+1); CLKCNT >=1
13:8	CLKRS	**Controls sensor master clock rising edge**
5:0	CLKFL	**Controls sensor master clock falling edge**

1A043608 SENINF_TG4_TM_CTL TM Control 00300004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									TM_DUMMYPXL							
Type									RW							
Reset									0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TM_VSYNC								TM_PAT					TM_FMT	TM_RST	TM_EN
Type	RW								RW					RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0		1	0	0

Bit(s)	Name	Description
23:16	TM_DUMMYPXL	**Test model horizontal dummy pixel**
15:8	TM_VSYNC	**VSYNC high duration in line unit (TM_DUMMYPXL + PIXEL)**
7:4	TM_PAT	**Test model decision** 0: White 1: Yellow 2: Cyan 3: Green 4: Magenta 5: Red 6: Blue 7: Black 8: Horizontal gray level (Unit 1) 9: Horizontal gray level (Unit 4) 10: Horizontal gray level (take 1024 pixel as one period) (only bayer) 11: Vertical gray level (Unit 1) 12: Static horizontal color bar 13: Static vertical color bar (only bayer) 14: R,G,B,W flashes every two frames (only bayer) 15: Dynamic horizontal colorbar (only bayer)
2	TM_FMT	**Test model format** 0: Bayer

Bit(s)	Name	Description
		1: YUV
1	TM_RST	**Resets test model** 1'b0: Does not reset test model 1'b1: Reset test model
0	TM_EN	**Enables test model** 0: Disable 1: Enable

1A04360C SENINF_TG4_TM_SIZE **TM Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			TM_LINE													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TM_PXL												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	TM_LINE	Test model line number
12:0	TM_PXL	Test model pixel number (HSYNC high duration in pixel unit)

1A043610 SENINF_TG4_TM_CLK **TM Clock** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		TM_CLRBAR_IDX					TM_CLRBAR_OFT									
Type		RW					RW									
Reset		0	0	0			0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TM_CLK_CNT			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
30:28	TM_CLRBAR_IDX	**Test model colorbar index offset** 0: White 1: Yellow 2: Cyan 3: Green 4: Magenta 5: Red 6: Blue 7: Black
25:16	TM_CLRBAR_OFT	**Test model colorbar offset** This value should be smaller than (TM_PXL>>3).
3:0	TM_CLK_CNT	**Test model clock divided count**

1A043614 SENINF_TG4_TM_STP TG1_TM_STP 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TG1_TM_STP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TG1_TM_STP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TG1_TM_STP	Time stamp divider

Module name: seninf5_ccir656 Base address: (+1a044400h)

Address	Name	Width	Register Function
1A044400	CCIR656_CTL	32	CCIR656_CTL
1A044404	CCIR656_H	32	CCIR656_H
1A044408	CCIR656_PTGEN_H_1	32	CCIR656_PTGEN_H_1
1A04440C	CCIR656_PTGEN_H_2	32	CCIR656_PTGEN_H_2
1A044410	CCIR656_PTGEN_V_1	32	CCIR656_PTGEN_V_1
1A044414	CCIR656_PTGEN_V_2	32	CCIR656_PTGEN_V_2
1A044418	CCIR656_PTGEN_CTL1	32	CCIR656_PTGEN_CTL1
1A04441C	CCIR656_PTGEN_CTL2	32	CCIR656_PTGEN_CTL2
1A044420	CCIR656_PTGEN_CTL3	32	CCIR656_PTGEN_CTL3
1A044424	CCIR656_STATUS	32	CCIR656_STATUS

1A044400 CCIR656_CTL CCIR656_CTL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CCIR656_DBG_SEL						CCIR656_EN	CCIR656_PT_EN	CCIR656_VS_POL	CCIR656_HS_POL	CCIR656_REV_1	CCIR656_REV_0
Type					RW						RW	RW	RW	RW	RW	RW
Reset					0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
11:8	CCIR656_DBG_SEL	**Selects CCIR656 debug port**
5	CCIR656_EN	**Enables CCIR656**
4	CCIR656_PT_EN	**Enables CCIR656 internal pattern gen** 0: Disable 1: Enable
3	CCIR656_VS_POL	**CCIR656 VS output polarity** 0: Active high 1: Active low
2	CCIR656_HS_POL	**CCIR656 HS output polarity** 0: Active high 1: Active low
1	CCIR656_REV_1	**CCIR656_REV_1**
0	CCIR656_REV_0	**CCIR656_REV_0**

1A044404 CCIR656_H CCIR656_H 059A0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CCIR656_HS_END											
Type					RW											
Reset					0	1	0	1	1	0	0	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CCIR656_HS_START											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	1	1

Bit(s)	Name	Description
27:16	CCIR656_HS_END	CCIR656 HS end in 27MHz clock rate
11:0	CCIR656_HS_START	CCIR656 HS start in 27MHz clock rate

1A044408 CCIR656_PTGEN_H_1 CCIR656_PTGEN_H_1 02D0035A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				CCIR656_PT_HACTIVE												
Type				RW												
Reset				0	0	0	1	0	1	1	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CCIR656_PT_HTOTAL												
Type				RW												
Reset				0	0	0	1	1	0	1	0	1	1	0	1	0

Bit(s)	Name	Description
28:16	CCIR656_PT_HACTIVE	CCIR656 pattern gen horizontal active
12:0	CCIR656_PT_HTOTAL	CCIR656 pattern gen horizontal total

1A04440C CCIR656_PTGEN_H_2 CCIR656_PTGEN_H_2 00850085

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				CCIR656_PT_HSTART												

Type				RW												
Reset				0	0	0	0	0	1	0	0	0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CCIR656_PT_HWIDTH												
Type				RW												
Reset				0	0	0	0	0	1	0	0	0	0	1	0	1

Bit(s)	Name	Description
28:16	CCIR656_PT_HSTART	CCIR656 pattern gen horizontal start
12:0	CCIR656_PT_HWIDTH	CCIR656 pattern gen horizontal width

1A044410 CCIR656_PT_GEN_V_1 CCIR656_PTGEN_V_1 00F00106

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CCIR656_PT_VACTIVE											
Type					RW											
Reset					0	0	0	0	1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CCIR656_PT_VTOTAL											
Type					RW											
Reset					0	0	0	1	0	0	0	0	0	1	1	0

Bit(s)	Name	Description
27:16	CCIR656_PT_VACTIVE	CCIR656 pattern gen vertical active
11:0	CCIR656_PT_VTOTAL	CCIR656 pattern gen vertical total

1A044414 CCIR656_PT_GEN_V_2 CCIR656_PTGEN_V_2 00160016

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CCIR656_PT_VSTART											
Type					RW											
Reset					0	0	0	0	0	0	0	1	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CCIR656_PT_VWIDTH											
Type					RW											
Reset					0	0	0	0	0	0	0	1	0	1	1	0

Bit(s)	Name	Description
27:16	CCIR656_PT_VSTART	CCIR656 pattern gen vertical start
11:0	CCIR656_PT_VWIDTH	CCIR656 pattern gen vertical width

1A044418 CCIR656_PT_GEN_CTL1 CCIR656_PTGEN_CTL1 001E0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					CCIR656_PT_COLOR_ BAR_TH											
Type					RW											

Reset					0	0	0	0	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CCIR656_PT_TYPE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	CCIR656_PT_COLOR_BAR_TH	CCIR656 pattern gen color bar threshold
7:0	CCIR656_PT_TYPE	CCIR656 pattern gen type

1A04441C CCIR656_PT GEN_CTL2 CCIR656_PTGEN_CTL2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CCIR656_PT_CR							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CCIR656_PT_CB								CCIR656_PT_Y							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	CCIR656_PT_CR	CCIR656 pattern gen CR value
15:8	CCIR656_PT_CB	CCIR656 pattern gen CB value
7:0	CCIR656_PT_Y	CCIR656 pattern gen Y value

1A044420 CCIR656_PT GEN_CTL3 CCIR656_PTGEN_CTL3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CCIR656_PT_BD_CR							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CCIR656_PT_BD_CB								CCIR656_PT_BD_Y							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	CCIR656_PT_BD_CR	CCIR656 pattern gen boarder CR value
15:8	CCIR656_PT_BD_CB	CCIR656 pattern gen boarder CB value
7:0	CCIR656_PT_BD_Y	CCIR656 pattern gen boarder Y value

1A044424 CCIR656_STATUS CCIR656_STATUS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CCIR656_IN_VS	CCIR656_IN_FIELD
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	CCIR656_IN_VS	CCIR656 input VS value
0	CCIR656_IN_FIELD	CCIR656 input field value

Module name: seninf5 Base address: (+1a044200h)

Address	Name	Width	Register Function
1A044200	SENINF5_CTRL	32	SENINF 5 Control Register
1A044204	SENINF5_CTRL_EXT	32	SENINF 5 Control Register Extend
1A044208	SENINF5_ASYNC_CTRL	32	SENINF 5 Async Control Register

1A044200 SENINF5_CTRL SENINF 5 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PAD2CAM_DATA_SEL							SENINF_DEBUG_SEL							
Type		RW							RW							
Reset		0	0	0					0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_SRC_SEL							CSI3_SW_RST	CSI2_SW_RST	SCAM_SW_RST	TEST_MODEL_SW_RST	CKGEN_SW_RST	CCIR_SW_RST	OCSI2_SW_RST	NCSI2_SW_RST	SENINF_EN
Type	RW							RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:28	PAD2CAM_DATA_SEL	0: PAD2CAM_DATA[9:0] 3: {PAD2CAM_DATA[7:0],2'b00} 4: {PAD2CAM_DATA[9:2]2'b00}
23:20	SENINF_DEBUG_SEL	**Selects SENINF1 debug**
15:12	SENINF_SRC_SEL	**Selects SENINF input source** 0: CSI2 1: Test model 2: CCIR656 3: Parallel sensor 4: Serial sensor 8: NCSI2
8	CSI3_SW_RST	**CSI3 software reset, active high** 0: De-assert reset 1: Assert reset

Bit(s)	Name	Description
7	CSI2_SW_RST	**CSI2 software reset, active high** 0: De-assert reset 1: Assert reset
6	SCAM_SW_RST	**SCAM software reset, active high** 0: De-assert reset 1: Assert reset
5	TEST_MODEL_SW_RST	**Test model software reset, active high** 0: De-assert reset 1: Assert reset
4	CKGEN_SW_RST	**CKGEN software reset, active high** 0: De-assert reset 1: Assert reset
3	CCIR_SW_RST	**CCIR software reset, active high** 0: De-assert reset 1: Assert reset
2	OCSI2_SW_RST	**OCSI2 software reset, active high** 0: De-assert reset 1: Assert reset
1	NCSI2_SW_RST	**NCSI2 software reset, active high** 0: De-assert reset 1: Assert reset
0	SENINF_EN	

1A044204 SENINF5_CTRL_EXT — **SENINF 5 Control Register Extend** — **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															SENINF_SRC_SEL_EXT	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SENINF_CSI3_IP_EN	SENINF_CSI2_IP_EN	SENINF_NCSI2_IP_EN	SENINF_SCAM_IP_EN			SENINF_TESTMDL_IP_EN	SENINF_OCSI2_IP_EN
Type									RW	RW	RW	RW			RW	RW
Reset									0	0	0	0			0	0

Bit(s)	Name	Description
17:16	SENINF_SRC_SEL_EXT	[0] Set 1'b1 for CSI2 [1] Set 1'b1 for CSI3 For constraints only.
7	SENINF_CSI3_IP_EN	Enables CSI3 IP
6	SENINF_CSI2_IP_EN	Enables CSI2 IP
5	SENINF_NCSI2_IP_EN	Enables NCSI2 IP
4	SENINF_SCAM_IP_EN	Enables SCAM IP
1	SENINF_TESTMDL_IP_EN	Enables TESTMDL IP
0	SENINF_OCSI2_IP_EN	Enables OCSI2 IP

1A044208 SENINF5_ASYNC_CTRL — **SENINF 5 Async Control Register** — **1B1F0002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			FIFO _FLU SH_E N								FIFO _PUS H_EN					
Type			RW								RW					
Reset			0	1	1	0	1	1			0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SENI NF_H SYNC _POL	SENI NF_V SYNC _POL	SENI NF_H SYNC _MAS K	SENI NF_A SYNC _FIF O_RS T
Type													RW	RW	RW	RW
Reset													0	0	1	0

Bit(s)	Name	Description
29:24	FIFO_FLUSH_EN	**Normal mode: 6'b011011** JPEG two pixel mode: 6'b011000
21:16	FIFO_PUSH_EN	**Normal mode: 6'b011111** JPEG two pixel mode: 6'b011110
3	SENINF_HSYNC_POL	**SENINF HSYNC polarity**
2	SENINF_VSYNC_POL	**SENINF VSYNC polarity**
1	SENINF_HSYNC_MASK	**Masks hsync** 0: Send hsync when vsync = 1 1: Does not send hsync when vsync = 1
0	SENINF_ASYNC_FIFO_RST	**Async FIFO software reset**

Module name: seninf5_mux Base address: (+1a044d00h)

Address	Name	Width	Register Function
1A044D00	SENINF5_MUX_CTRL	32	SENINF 5 Control Register
1A044D04	SENINF5_MUX_INTEN	32	SENINF 5 Interrupt Enable Register
1A044D08	SENINF5_MUX_INTSTA	32	SENINF 5 Interrupt Status Register
1A044D0C	SENINF5_MUX_SIZE	32	SENINF 5 Image Size Register
1A044D10	SENINF5_MUX_DEBUG_1	32	SENINF 5 Debug Register 1
1A044D14	SENINF5_MUX_DEBUG_2	32	SENINF 5 Debug Register 2
1A044D18	SENINF5_MUX_DEBUG_3	32	SENINF 5 Debug Register 3
1A044D1C	SENINF5_MUX_DEBUG_4	32	SENINF 5 Debug Register 4
1A044D20	SENINF5_MUX_DEBUG_5	32	SENINF 5 Debug Register 5
1A044D24	SENINF5_MUX_DEBUG_6	32	SENINF 5 Debug Register 6
1A044D28	SENINF5_MUX_DEBUG_7	32	SENINF 5 Debug Register 7
1A044D2C	SENINF5_MUX_SPARE	32	SENINF 5 spare Register
1A044D30	SENINF5_MUX_DATA	32	SENINF 5 Data Register

Address	Name	Width	Register Function
1A044D34	SENINF5_MUX_DATA_CNT	32	SENINF 5 Data Count Register
1A044D38	SENINF5_MUX_CROP	32	SENINF 5 Crop Size Register
1A044D3C	SENINF5_MUX_CTRL_EXT	32	SENINF 5 Control Register Extend

1A044D00 SENINF5_MUX_CTRL **SENINF 5 Control Register** **06DF0080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_MUX_EN	CROP_EN	FIFO_FULL_WR_EN		FIFO_FLUSH_EN						FIFO_PUSH_EN					
Type	RW	RW	RW		RW						RW					
Reset	0	0	0	0	0	1	1	0	1	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_SRC_SEL				OVERRUN_RST_EN	SENINF_HSYNC_POL	SENINF_VSYNC_POL	SENINF_PIX_SEL	SENINF_HSYNC_MASK		SENINF_MUX_RDY_VALUE	SENINF_MUX_RDY_MODE			SENINF_IRQ_SW_RST	SENINF_MUX_SW_RST
Type	RW				RW	RW	RW	RW	RW		RW	RW			RW	RW
Reset	0	0	0	0	0	0	0	0	1		0	0			0	0

Bit(s)	Name	Description
31	SENINF_MUX_EN	**Enables seninf_mux** 0: Disable 1: Enable
30	CROP_EN	**Sensor crop function**
29:28	FIFO_FULL_WR_EN	0: FIFO write operation is prohibited when FIFO is full. 1: FIFO write operation is prohibited after FIFO full occurs. 2: FIFO write operation is allowed when FIFO is full.
27:22	FIFO_FLUSH_EN	**Normal mode: 6'b011011** JPEG two pixel mode: 6'b011000
21:16	FIFO_PUSH_EN	**Normal mode: 6'b011111** JPEG two pixel mode: 6'b011110
15:12	SENINF_SRC_SEL	**Selects SENINF input source:** {seninf_mux_sel_ext, seninf_mux_sel} 00: OCSI2 VC0 01: Test model 02: CCIR656 03: Parallel sensor 04: Serial sensor 06: OCSI2 VC1 08: NCSI2 VC0 09: NCSI2 VC1 0A: NCSI2 VC2 0B: NCSI2 VC3 0C: NCSI2 VC4 0D: NCSI2 VC5
11	OVERRUN_RST_EN	**Enables SENINF mux software reset for overrun** 0: No action 1: Auto self-reset for overrun situation

Bit(s)	Name	Description
10	SENINF_HSYNC_POL	**SENINF HSYNC polarity**
9	SENINF_VSYNC_POL	**SENINF VSYNC polarity**
8	SENINF_PIX_SEL	**SENINF output bus width:** {seninf_pixel_sel_ext, seninf_pixel_sel} 00: 1 pixel/cycle 01: 2 pixels/cycle 10: 4 pixels/cycle
7	SENINF_HSYNC_MASK	**Masks hsync** 0: Send hsync when vsync = 1 1: Does not send hsync when vsync = 1
5	SENINF_MUX_RDY_VALUE	**seninf_rdy value in force mode**
4	SENINF_MUX_RDY_MODE	0: seninf_rdy normal mode 1: seninf_rdy force mode
1	SENINF_IRQ_SW_RST	**SENINF IRQ software reset, active high** 0: De-assert reset 1: Assert reset
0	SENINF_MUX_SW_RST	**SENINF mux software reset, active high** 0: De-assert reset 1: Assert reset

1A044D04 SENINF5_MUX_INTEN **SENINF 5 Interrupt Enable Register** **8000007F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_IRQ_CLR_SEL															
Type	RW															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SENINF_SENSOR_HSIZEERR_IRQ_EN	SENINF_SENSOR_VSIZEERR_IRQ_EN	SENINF_HSIZEERR_IRQ_EN	SENINF_VSIZEERR_IRQ_EN	SENINF_FSMERR_IRQ_EN	SENINF_CRCERR_IRQ_EN	SENINF_OVERRUN_IRQ_EN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										1	1	1	1	1	1	1

Bit(s)	Name	Description
31	SENINF_IRQ_CLR_SEL	0: Read clear 1: Write clear
6	SENINF_SENSOR_HSIZEERR_IRQ_EN	Enables sensor HSIZE ERROR IRQ
5	SENINF_SENSOR_VSIZEERR_IRQ_EN	Enables sensor VSIZE ERROR IRQ
4	SENINF_HSIZEERR_IRQ_EN	Enables async FIFO HSIZE ERROR IRQ
3	SENINF_VSIZEERR_IRQ_EN	Enables async FIFO VSIZE ERROR IRQ
2	SENINF_FSMERR_IRQ_EN	Enables FSM ERROR IRQ
1	SENINF_CRCERR_IRQ_EN	Enables CRR ERROR IRQ
0	SENINF_OVERRUN_IRQ_EN	Enables FIFO OVERRUN IRQ

1A044D08 SENINF5_MUX_INTSTA **SENINF 5 Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SENINF_SENSOR_HSIZEERR_IRQ_STA	SENINF_SENSOR_VSIZEERR_IRQ_STA	SENINF_HSIZEERR_IRQ_STA	SENINF_VSIZEERR_IRQ_STA	SENINF_FSMERR_IRQ_STA	SENINF_CRCERR_IRQ_STA	SENINF_OVERRUN_IRQ_STA
Type										RO	RO	RO	RO	RO	RO	RO
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	SENINF_SENSOR_HSIZEERR_IRQ_STA	Sensor HSIZE ERROR IRQ status
5	SENINF_SENSOR_VSIZEERR_IRQ_STA	Sensor VSIZE ERROR IRQ status
4	SENINF_HSIZEERR_IRQ_STA	Async FIFO HSIZE ERROR IRQ status
3	SENINF_VSIZEERR_IRQ_STA	Async FIFO VSIZE ERROR IRQ status
2	SENINF_FSMERR_IRQ_STA	FSM ERROR IRQ status
1	SENINF_CRCERR_IRQ_STA	CRR ERROR IRQ status
0	SENINF_OVERRUN_IRQ_STA	FIFO OVERRUN IRQ status

1A044D0C SENINF5_MUX_SIZE **SENINF 5 Image Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_HSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_VSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_HSIZE	Senor image horizontal size
15:0	SENINF_VSIZE	Senor image vertical size

1A044D10 SENINF5_MUX_DEBUG_1 **SENINF 5 Debug Register 1** **0000C303**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															

Type	RO															
Reset	1	1	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A044D14 SENINF5_MUX_DEBUG_2 SENINF 5 Debug Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A044D18 SENINF5_MUX_DEBUG_3 SENINF 5 Debug Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A044D1C SENINF5_MUX_DEBUG_4 SENINF 5 Debug Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

Bit(s)	Name	Description

1A044D20 SENINF5_MUX_DEBUG_5 SENINF 5 Debug Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A044D24 SENINF5_MUX_DEBUG_6 SENINF 5 Debug Register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A044D28 SENINF5_MUX_DEBUG_7 SENINF 5 Debug Register 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A044D2C SENINF5_MUX_SPARE SENINF 5 spare Register 000E2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SENI NF_S PARE			
Type													RW			
Reset													1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENI NF_S PARE		SENI NF_F IFO_ FULL _SEL	SENI NF_V CNT_ SEL		SENINF_CR C_SEL										
Type	RW		RW	RW		RW										
Reset	0	0	1	0	0	0	0									

Bit(s)	Name	Description
19:14	SENINF_SPARE	**Spare register**
13	SENINF_FIFO_FULL_SEL	0: Does not send FIFO full to cam 1: Send FIFO full to cam
12:11	SENINF_VCNT_SEL	0: Vsync rising 1: Vsync rising d1 2: Vsync rising d2 3: Vsync rising d3
10:9	SENINF_CRC_SEL	0: Vsync rising 1: Vsync rising d1 2: Vsync rising d2 3: Vsync rising d3

1A044D30 SENINF5_MUX_DATA — SENINF 5 Data Register — 40000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA1															
Type	RO															
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_DATA1	
15:0	SENINF_DATA0	

1A044D34 SENINF5_MUX_DATA_CNT — SENINF 5 Data Count Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENINF_DATA_CNT	

1A044D38 SENINF5_MUX_CROP **SENINF 5 Crop Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_CROP_X2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_CROP_X1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_CROP_X2	
15:0	SENINF_CROP_X1	

1A044D3C SENINF5_MUX_CTRL_EXT **SENINF 5 Control Register Extend** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												SENINF_PIX_SEL_EXT			SENINF_SRC_SEL_EXT	
Type												RW			RW	
Reset												0			0	0

Bit(s)	Name	Description
4	SENINF_PIX_SEL_EXT	**SENINF output bus width:** {seninf_pixel_sel_ext, seninf_pixel_sel} 00: One pixel/cycle 01: Two pixels/cycle 10: four pixels/cycle
1:0	SENINF_SRC_SEL_EXT	**Selects SENINF input source:** {seninf_src_sel_ext, seninf_src_sel} 18: CSI2 VC0 19: CSI2 VC1 1A: CSI2 VC2 1B: CSI2 VC3 1C: CSI2 VC4 28: CSI3 VC0 29: CSI3 VC1 2A: CSI3 VC2 2B: CSI3 VC3 2C: CSI3 VC4

Bit(s)	Name	Description

Module name: SENINF5_TG Base address: (+1a044600h)

Address	Name	Width	Register Function
1A044600	SENINF_TG5_PH_CNT	32	TG Phase Counter
1A044604	SENINF_TG5_SEN_CK	32	TG Sensor Clock Divider
1A044608	SENINF_TG5_TM_CTL	32	TM Control
1A04460C	SENINF_TG5_TM_SIZE	32	TM Size
1A044610	SENINF_TG5_TM_CLK	32	TM Clock
1A044614	SENINF_TG5_TM_STP	32	TG1_TM_STP

1A044600 SENINF_TG5_PH_CNT **TG Phase Counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PCEN		ADCLK_EN	CLKPOL												
Type	RW		RW	RW												
Reset	0		0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CAM_PCLK_INV	PAD_PCLK_INV	EXT_PWRDN	EXT_RST		CLKFL_POL	TGCLK_SEL	
Type									RW	RW	RW	RW		RW	RW	
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
31	PCEN	**TG phase counter enable control**
29	ADCLK_EN	**Enables sensor master clock (mclk) output to sensor**
28	CLKPOL	**Controls sensor master clock polarity**
7	CAM_PCLK_INV	**Inverts pixel clock in CAM**
6	PAD_PCLK_INV	**Inverts pixel clock in PAD side**
5	EXT_PWRDN	**Powers down sensor**
4	EXT_RST	**Resets sensor**
2	CLKFL_POL	**Sensor clock falling edge polarity**
1:0	TGCLK_SEL	**Selects sensor master clock** 0: isp_clk 1: cam_pll 2: 3rd clock source

1A044604 SENINF_TG5_SEN_CK **TG Sensor Clock Divider** **00010001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CLKCNT					
Type											RW					

Reset											0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			CLKRS								CLKFL					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	1

Bit(s)	Name	Description
21:16	CLKCNT	**Controls sensor master clock frequency divider** Sensor master clock = ISP_clock/(CLKCNT+1); CLKCNT >=1
13:8	CLKRS	**Controls sensor master clock rising edge**
5:0	CLKFL	**Controls sensor master clock falling edge**

1A044608 SENINF_TG5_TM_CTL TM Control 00300004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									TM_DUMMYPXL							
Type									RW							
Reset									0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TM_VSYNC								TM_PAT					TM_FMT	TM_RST	TM_EN
Type	RW								RW					RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0		1	0	0

Bit(s)	Name	Description
23:16	TM_DUMMYPXL	**Test model horizontal dummy pixel**
15:8	TM_VSYNC	**VSYNC high duration in line unit (TM_DUMMYPXL + PIXEL)**
7:4	TM_PAT	**Test model decision** 0: White 1: Yellow 2: Cyan 3: Green 4: Magenta 5: Red 6: Blue 7: Black 8: Horizontal gray level (Unit 1) 9: Horizontal gray level (Unit 4) 10: Horizontal gray level (take 1024 pixel as one period) (only bayer) 11: Vertical gray level (Unit 1) 12: Static horizontal color bar 13: Static vertical color bar (only bayer) 14: R,G,B,W flashes every two frames (only bayer) 15: Dynamic horizontal colorbar (only bayer)
2	TM_FMT	**Test model format** 0: Bayer 1: YUV
1	TM_RST	**Resets est model** 1'b0: Does not reset test model 1'b1: Reset test model
0	TM_EN	**Enables test model**

Bit(s)	Name	Description
		0: Disable 1: Enable

1A04460C SENINF_TG5_TM_SIZE **TM Size** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			TM_LINE													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TM_PXL												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	TM_LINE	Test model line number
12:0	TM_PXL	Test model pixel number (HSYNC high duration in pixel unit)

1A044610 SENINF_TG5_TM_CLK **TM Clock** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		TM_CLRBAR_IDX					TM_CLRBAR_OFT									
Type		RW					RW									
Reset		0	0	0			0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TM_CLK_CNT			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
30:28	TM_CLRBAR_IDX	**Test model colorbar index offset** 0: White 1: Yellow 2: Cyan 3: Green 4: Magenta 5: Red 6: Blue 7: Black
25:16	TM_CLRBAR_OFT	**Test model colorbar offset** This value should be smaller than (TM_PXL>>3).
3:0	TM_CLK_CNT	**Test model clock divided count**

1A044614 SENINF_TG5_TM_STP **TG1_TM_STP** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	TG1_TM_STP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TG1_TM_STP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TG1_TM_STP	Time stamp divider

Module name: seninf6_mux Base address: (+1a045d00h)

Address	Name	Width	Register Function
1A045D00	SENINF6_MUX_CTRL	32	SENINF 6 Control Register
1A045D04	SENINF6_MUX_INTEN	32	SENINF 6 Interrupt Enable Register
1A045D08	SENINF6_MUX_INTSTA	32	SENINF 6 Interrupt Status Register
1A045D0C	SENINF6_MUX_SIZE	32	SENINF 6 Image Size Register
1A045D10	SENINF6_MUX_DEBUG_1	32	SENINF 6 Debug Register 1
1A045D14	SENINF6_MUX_DEBUG_2	32	SENINF 6 Debug Register 2
1A045D18	SENINF6_MUX_DEBUG_3	32	SENINF 6 Debug Register 3
1A045D1C	SENINF6_MUX_DEBUG_4	32	SENINF 6 Debug Register 4
1A045D20	SENINF6_MUX_DEBUG_5	32	SENINF 6 Debug Register 5
1A045D24	SENINF6_MUX_DEBUG_6	32	SENINF 6 Debug Register 6
1A045D28	SENINF6_MUX_DEBUG_7	32	SENINF 6 Debug Register 7
1A045D2C	SENINF6_MUX_SPARE	32	SENINF 6 Spare Register
1A045D30	SENINF6_MUX_DATA	32	SENINF 6 Data Register
1A045D34	SENINF6_MUX_DATA_CNT	32	SENINF 6 Data Count Register
1A045D38	SENINF6_MUX_CROP	32	SENINF 6 Crop Size Register
1A045D3C	SENINF6_MUX_CTRL_EXT	32	SENINF 6 Control Register Extend

1A045D00 SENINF6_MUX_CTRL SENINF 6 Control Register 06DF0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_M	CROP_EN	FIFO_FULL_WR_EN		FIFO_FLUSH_EN						FIFO_PUSH_EN					

	UX_EN															
Type	RW	RW	RW		RW						RW					
Reset	0	0	0	0	0	1	1	0	1	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_SRC_SEL				OVERRUN_RST_EN	SENINF_HSYNC_POL	SENINF_VSYNC_POL	SENINF_PIX_SEL	SENINF_HSYNC_MASK		SENINF_MUX_RDY_VALUE	SENINF_MUX_RDY_MODE			SENINF_IRQ_SW_RST	SENINF_MUX_SW_RST
Type	RW				RW	RW	RW	RW	RW		RW	RW			RW	RW
Reset	0	0	0	0	0	0	0	0	1		0	0			0	0

Bit(s)	Name	Description
31	SENINF_MUX_EN	**Enables seninf_mux** 0: Disable 1: Enable
30	CROP_EN	**Sensor crop function**
29:28	FIFO_FULL_WR_EN	**0: FIFO write operation is prohibited when FIFO is full.** 1: FIFO write operation is prohibited after FIFO full occurs. 2: FIFO write operation is allowed when FIFO is full.
27:22	FIFO_FLUSH_EN	**Normal mode: 6'b011011** JPEG two pixel mode: 6'b011000
21:16	FIFO_PUSH_EN	**Normal mode: 6'b011111** JPEG two pixel mode : 6'b011110
15:12	SENINF_SRC_SEL	**Selects SENINF input source:** {seninf_mux_sel_ext, seninf_mux_sel} 00: OCSI2 VC0 01: Test model 02: CCIR656 03: Parallel sensor 04: Serial sensor 06: OCSI2 VC1 08: NCSI2 VC0 09: NCSI2 VC1 0A: NCSI2 VC2 0B: NCSI2 VC3 0C: NCSI2 VC4 0D: NCSI2 VC5
11	OVERRUN_RST_EN	**Enables SENINF mux software reset for overrun** 0: No action 1: Auto self-reset for overrun situation
10	SENINF_HSYNC_POL	**SENINF HSYNC polarity**
9	SENINF_VSYNC_POL	**SENINF VSYNC polarity**
8	SENINF_PIX_SEL	**SENINF output bus width:** {seninf_pixel_sel_ext, seninf_pixel_sel} 00: 1 pixel/cycle 01: 2 pixels/cycle 10: 4 pixels/cycle
7	SENINF_HSYNC_MASK	**Masks hsyncg** 0: Send hsync when vsync = 1 1: Does not send hsync when vsync = 1
5	SENINF_MUX_RDY_VALUE	**seninf_rdy value in force mode**
4	SENINF_MUX_RDY_MODE	0: seninf_rdy normal mode 1: seninf_rdy force mode
1	SENINF_IRQ_SW_RST	**SENINF IRQ software reset, active high** 0: De-assert reset

Bit(s)	Name	Description
		1: Assert reset
0	SENINF_MUX_SW_RST	**SENINF mux software reset, active high** 0: De-assert reset 1: Assert reset

1A045D04 SENINF6_MUX_INTEN **SENINF 6 Interrupt Enable Register** **8000007F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_IRQ_CLR_SEL															
Type	RW															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SENINF_SENSOR_HSIZEERR_IRQ_EN	SENINF_SENSOR_VSIZEERR_IRQ_EN	SENINF_HSIZEERR_IRQ_EN	SENINF_VSIZEERR_IRQ_EN	SENINF_FSMERR_IRQ_EN	SENINF_CRCERR_IRQ_EN	SENINF_OVERRUN_IRQ_EN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										1	1	1	1	1	1	1

Bit(s)	Name	Description
31	SENINF_IRQ_CLR_SEL	0: Read clear 1: Write clear
6	SENINF_SENSOR_HSIZEERR_IRQ_EN	Enables sensor HSIZE ERROR IRQ
5	SENINF_SENSOR_VSIZEERR_IRQ_EN	Enables sensor VSIZE ERROR IRQ
4	SENINF_HSIZEERR_IRQ_EN	Enables async FIFO HSIZE ERROR IRQ
3	SENINF_VSIZEERR_IRQ_EN	Enables async FIFO VSIZE ERROR IRQ
2	SENINF_FSMERR_IRQ_EN	Enables FSM ERROR IRQ
1	SENINF_CRCERR_IRQ_EN	Enables CRR ERROR IRQ
0	SENINF_OVERRUN_IRQ_EN	Enables FIFO OVERRUN IRQ

1A045D08 SENINF6_MUX_INTSTA **SENINF 6 Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SENINF_SENSOR_HSIZEERR_IRQ_STA	SENINF_SENSOR_VSIZEERR_IRQ_STA	SENINF_HSIZEERR_IRQ_STA	SENINF_VSIZEERR_IRQ_STA	SENINF_FSMERR_IRQ_STA	SENINF_CRCERR_IRQ_STA	SENINF_OVERRUN_IRQ_STA

Type										RO	RO	RO	RO	RO	RO	RO
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	SENINF_SENSOR_HSIZEERR_IRQ_STA	Sensor HSIZE ERROR IRQ status
5	SENINF_SENSOR_VSIZEERR_IRQ_STA	Sensor VSIZE ERROR IRQ status
4	SENINF_HSIZEERR_IRQ_STA	Async FIFO HSIZE ERROR IRQ status
3	SENINF_VSIZEERR_IRQ_STA	Async FIFO VSIZE ERROR IRQ status
2	SENINF_FSMERR_IRQ_STA	FSM ERROR IRQ status
1	SENINF_CRCERR_IRQ_STA	CRR ERROR IRQ status
0	SENINF_OVERRUN_IRQ_STA	FIFO OVERRUN IRQ status

1A045D0C SENINF6_MUX_SIZE — SENINF 6 Image Size Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_HSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_VSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_HSIZE	Senor image horizontal size
15:0	SENINF_VSIZE	Senor image vertical size

1A045D10 SENINF6_MUX_DEBUG_1 — SENINF 6 Debug Register 1 — 0000C303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	1	1	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A045D14 SENINF6_MUX_DEBUG_2 — SENINF 6 Debug Register 2 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A045D18 SENINF6_MUX_DEBUG_3 SENINF 6 Debug Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A045D1C SENINF6_MUX_DEBUG_4 SENINF 6 Debug Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A045D20 SENINF6_MUX_DEBUG_5 SENINF 6 Debug Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A045D24 SENINF6_MUX_DEBUG_6 SENINF 6 Debug Register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A045D28 SENINF6_MUX_DEBUG_7 SENINF 6 Debug Register 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A045D2C SENINF6_MUX_SPARE SENINF 6 Spare Register 000E2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SENI NF_S PARE			
Type													RW			
Reset													1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENI NF_S PARE		SENI NF_F IFO_ FULL _SEL	SENI NF_V CNT_ SEL		SENINF_CR C_SEL										
Type	RW		RW	RW		RW										
Reset	0	0	1	0	0	0	0									

Bit(s)	Name	Description

Bit(s)	Name	Description
19:14	SENINF_SPARE	**Spare register**
13	SENINF_FIFO_FULL_SEL	0: Does not send FIFO full to cam 1: Send FIFO full to cam
12:11	SENINF_VCNT_SEL	0: Vsync rising 1: Vsync rising d1 2: Vsync rising d2 3: Vsync rising d3
10:9	SENINF_CRC_SEL	0: Vsync rising 1: Vsync rising d1 2: Vsync rising d2 3: Vsync rising d3

1A045D30 SENINF6_MUX_DATA SENINF 6 Data Register 40000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA1															
Type	RO															
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_DATA1	
15:0	SENINF_DATA0	

1A045D34 SENINF6_MUX_DATA_CNT SENINF 6 Data Count Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENINF_DATA_CNT	

1A045D38 SENINF6_MUX_CROP SENINF 6 Crop Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_CROP_X2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	SENINF_CROP_X1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_CROP_X2	
15:0	SENINF_CROP_X1	

1A045D3C SENINF6_MUX_CTRL_EXT SENINF 6 Control Register Extend 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												SENINF_PIX_SEL_EXT			SENINF_SRC_SEL_EXT	
Type												RW			RW	
Reset												0			0	0

Bit(s)	Name	Description
4	SENINF_PIX_SEL_EXT	**SENINF output bus width:** {seninf_pixel_sel_ext, seninf_pixel_sel} 00: 1 pixel/cycle 01: 2 pixels/cycle 10: 4 pixels/cycle
1:0	SENINF_SRC_SEL_EXT	**Selects SENINF input source:** {seninf_src_sel_ext, seninf_src_sel} 18: CSI2 VC0 19: CSI2 VC1 1A: CSI2 VC2 1B: CSI2 VC3 1C: CSI2 VC4 28: CSI3 VC0 29: CSI3 VC1 2A: CSI3 VC2 2B: CSI3 VC3 2C: CSI3 VC4

Module name: seninf7_mux Base address: (+1a046d00h)

Address	Name	Width	Register Function
1A046D00	SENINF7_MUX_CTRL	32	SENINF 7 Control Register
1A046D04	SENINF7_MUX_INTEN	32	SENINF 7 Interrupt Enable Register
1A046D08	SENINF7_MUX_INTSTA	32	SENINF 7 Interrupt Status Register
1A046D0C	SENINF7_MUX_SI	32	SENINF 7 Image Size Register

Address	Name	Width	Register Function
	ZE		
1A046D10	SENINF7_MUX_DEBUG_1	32	SENINF 7 Debug Register 1
1A046D14	SENINF7_MUX_DEBUG_2	32	SENINF 7 Debug Register 2
1A046D18	SENINF7_MUX_DEBUG_3	32	SENINF 7 Debug Register 3
1A046D1C	SENINF7_MUX_DEBUG_4	32	SENINF 7 Debug Register 4
1A046D20	SENINF7_MUX_DEBUG_5	32	SENINF 7 Debug Register 5
1A046D24	SENINF7_MUX_DEBUG_6	32	SENINF 7 Debug Register 6
1A046D28	SENINF7_MUX_DEBUG_7	32	SENINF 7 Debug Register 7
1A046D2C	SENINF7_MUX_SPARE	32	SENINF 7 Spare Register
1A046D30	SENINF7_MUX_DATA	32	SENINF 7 Data Register
1A046D34	SENINF7_MUX_DATA_CNT	32	SENINF 7 Data Count Register
1A046D38	SENINF7_MUX_CROP	32	SENINF 7 Crop Size Register
1A046D3C	SENINF7_MUX_CTRL_EXT	32	SENINF 7 Control Register Extend

1A046D00 SENINF7_MUX_CTRL **SENINF 7 Control Register** **06DF0080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_MUX_EN	CROP_EN	FIFO_FULL_WR_EN		FIFO_FLUSH_EN						FIFO_PUSH_EN					
Type	RW	RW	RW		RW						RW					
Reset	0	0	0	0	0	1	1	0	1	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_SRC_SEL				OVERRUN_RST_EN	SENINF_HSYNC_POL	SENINF_VSYNC_POL	SENINF_PIX_SEL	SENINF_HSYNC_MASK		SENINF_MUX_RDY_VALUE	SENINF_MUX_RDY_MODE			SENINF_IRQ_SW_RST	SENINF_MUX_SW_RST
Type	RW				RW	RW	RW	RW	RW		RW	RW			RW	RW
Reset	0	0	0	0	0	0	0	0	1		0	0			0	0

Bit(s)	Name	Description
31	SENINF_MUX_EN	**Enables seninf_mux** 0: Disable 1: Enable
30	CROP_EN	**Sensor crop function**
29:28	FIFO_FULL_WR_EN	0: FIFO write operation is prohibited when FIFO is full. 1: FIFO write operation is prohibited after FIFO full occurs. 2: FIFO write operation is allowed when FIFO is full.
27:22	FIFO_FLUSH_EN	**Normal mode: 6'b011011** JPEG two pixel mode: 6'b011000

Bit(s)	Name	Description
21:16	FIFO_PUSH_EN	**Normal mode: 6'b011111** JPEG two pixel mode: 6'b011110
15:12	SENINF_SRC_SEL	**Selects SENINF input source:** {seninf_mux_sel_ext, seninf_mux_sel} 00: OCSI2 VC0 01: Test model 02: CCIR656 03: Parallel sensor 04: Serial sensor 06: OCSI2 VC1 08: NCSI2 VC0 09: NCSI2 VC1 0A: NCSI2 VC2 0B: NCSI2 VC3 0C: NCSI2 VC4 0D: NCSI2 VC5
11	OVERRUN_RST_EN	**Enables SENINF mux software reset for overrun** 0: No action 1: Auto self-reset for overrun situation
10	SENINF_HSYNC_POL	**SENINF HSYNC polarity**
9	SENINF_VSYNC_POL	**SENINF VSYNC polarity**
8	SENINF_PIX_SEL	**SENINF output bus width:** {seninf_pixel_sel_ext, seninf_pixel_sel} 00: 1 pixel/cycle 01: 20 pixels/cycle 10: 4 pixels/cycle
7	SENINF_HSYNC_MASK	**Masks hsync** 0: Send hsync when vsync = 1 1: Does not send hsync when vsync = 1
5	SENINF_MUX_RDY_VALUE	**seninf_rdy value in force mode**
4	SENINF_MUX_RDY_MODE	0: seninf_rdy normal mode 1: seninf_rdy force mode
1	SENINF_IRQ_SW_RST	**SENINF IRQ software reset, active high** 0: De-assert reset 1: Assert reset
0	SENINF_MUX_SW_RST	**SENINF mux software reset, active high** 0: De-assert reset 1: Assert reset

1A046D04 SENINF7_MUX_INTEN — **SENINF 7 Interrupt Enable Register** — **8000007F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_IRQ_CLR_SEL															
Type	RW															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SENINF_SENSOR_HSIZEERR_I	SENINF_SENSOR_VSIZEERR_I	SENINF_HSIZEERR_IRQ_EN	SENINF_VSIZEERR_IRQ_EN	SENINF_FSMERR_IRQ_EN	SENINF_CRCERR_IRQ_EN	SENINF_OVERRUN_IRQ_EN

										RQ_EN	RQ_EN					
Type										RW	RW	RW	RW	RW	RW	RW
Reset										1	1	1	1	1	1	1

Bit(s)	Name	Description
31	SENINF_IRQ_CLR_SEL	0: Read clear 1: Write clear
6	SENINF_SENSOR_HSIZEERR_IRQ_EN	Enables sensor HSIZE ERROR IRQ
5	SENINF_SENSOR_VSIZEERR_IRQ_EN	Enables sensor VSIZE ERROR IRQ
4	SENINF_HSIZEERR_IRQ_EN	Enables async FIFO HSIZE ERROR IRQ
3	SENINF_VSIZEERR_IRQ_EN	Enables async FIFO VSIZE ERROR IRQ
2	SENINF_FSMERR_IRQ_EN	Enables FSM ERROR IRQ
1	SENINF_CRCERR_IRQ_EN	Enables CRR ERROR IRQ
0	SENINF_OVERRUN_IRQ_EN	Enables FIFO OVERRUN IRQ

1A046D08 SENINF7_MUX_INTSTA **SENINF 7 Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SENINF_SENSOR_HSIZEERR_IRQ_STA	SENINF_SENSOR_VSIZEERR_IRQ_STA	SENINF_HSIZEERR_IRQ_STA	SENINF_VSIZEERR_IRQ_STA	SENINF_FSMERR_IRQ_STA	SENINF_CRCERR_IRQ_STA	SENINF_OVERRUN_IRQ_STA
Type										RO	RO	RO	RO	RO	RO	RO
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	SENINF_SENSOR_HSIZEERR_IRQ_STA	Sensor HSIZE ERROR IRQ status
5	SENINF_SENSOR_VSIZEERR_IRQ_STA	Sensor VSIZE ERROR IRQ status
4	SENINF_HSIZEERR_IRQ_STA	Async FIFO HSIZE ERROR IRQ status
3	SENINF_VSIZEERR_IRQ_STA	Async FIFO VSIZE ERROR IRQ status
2	SENINF_FSMERR_IRQ_STA	FSM ERROR IRQ status
1	SENINF_CRCERR_IRQ_STA	CRR ERROR IRQ status
0	SENINF_OVERRUN_IRQ_STA	FIFO OVERRUN IRQ status

1A046D0C SENINF7_MUX_SIZE **SENINF 7 Image Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_HSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_VSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_HSIZE	Senor image horizontal size
15:0	SENINF_VSIZE	Senor image vertical size

1A046D10 SENINF7_MUX_DEBUG_1 SENINF 7 Debug Register 1 0000C303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	1	1	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A046D14 SENINF7_MUX_DEBUG_2 SENINF 7 Debug Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A046D18 SENINF7_MUX_DEBUG_3 SENINF 7 Debug Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A046D1C SENINF7_MUX_DEBUG_4 SENINF 7 Debug Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A046D20 SENINF7_MUX_DEBUG_5 SENINF 7 Debug Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A046D24 SENINF7_MUX_DEBUG_6 SENINF 7 Debug Register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A046D28 SENINF7_MU SENINF 7 Debug Register 7 00000000

X_DEBUG_7

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A046D2C SENINF7_MUX_SPARE — SENINF 7 Spare Register — 000E2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SENI NF_S PARE			
Type													RW			
Reset													1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENI NF_S PARE		SENI NF_F IFO_ FULL _SEL	SENI NF_V CNT_ SEL		SENINF_CR C_SEL										
Type	RW		RW	RW		RW										
Reset	0	0	1	0	0	0	0									

Bit(s)	Name	Description
19:14	SENINF_SPARE	**Spare register**
13	SENINF_FIFO_FULL_SEL	0: Does not send FIFO full to cam 1: Send FIFO full to cam
12:11	SENINF_VCNT_SEL	0: Vsync rising 1: Vsync rising d1 2: Vsync rising d2 3: Vsync rising d3
10:9	SENINF_CRC_SEL	0: Vsync rising 1: Vsync rising d1 2: Vsync rising d2 3: Vsync rising d3

1A046D30 SENINF7_MUX_DATA — SENINF 7 Data Register — 40000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA1															
Type	RO															
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_DATA1	
15:0	SENINF_DATA0	

1A046D34 SENINF7_MUX_DATA_CNT — SENINF 7 Data Count Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENINF_DATA_CNT	

1A046D38 SENINF7_MUX_CROP — SENINF 7 Crop Size Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_CROP_X2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_CROP_X1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_CROP_X2	
15:0	SENINF_CROP_X1	

1A046D3C SENINF7_MUX_CTRL_EXT — SENINF 7 Control Register Extend — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												SENINF_PIX_SEL_EXT			SENINF_SRC_SEL_EXT	
Type												RW			RW	
Reset												0			0	0

Bit(s)	Name	Description
4	SENINF_PIX_SEL_EXT	**SENINF output bus width:** {seninf_pixel_sel_ext, seninf_pixel_sel} 00: One pixel/cycle 01: Two pixels/cycle 10: four pixels/cycle
1:0	SENINF_SRC_SEL_EXT	**Selects SENINF input source:** {seninf_src_sel_ext, seninf_src_sel} 18: CSI2 VC0 19: CSI2 VC1 1A: CSI2 VC2 1B: CSI2 VC3 1C: CSI2 VC4 28: CSI3 VC0 29: CSI3 VC1 2A: CSI3 VC2 2B: CSI3 VC3 2C: CSI3 VC4

Module name: seninf8_mux Base address: (+1a047d00h)

Address	Name	Width	Register Function
1A047D00	SENINF8_MUX_CTRL	32	SENINF 8 Control Register
1A047D04	SENINF8_MUX_INTEN	32	SENINF 8 Interrupt Enable Register
1A047D08	SENINF8_MUX_INTSTA	32	SENINF 8 Interrupt Status Register
1A047D0C	SENINF8_MUX_SIZE	32	SENINF 8 Image Size Register
1A047D10	SENINF8_MUX_DEBUG_1	32	SENINF 8 Debug Register 1
1A047D14	SENINF8_MUX_DEBUG_2	32	SENINF 8 Debug Register 2
1A047D18	SENINF8_MUX_DEBUG_3	32	SENINF 8 Debug Register 3
1A047D1C	SENINF8_MUX_DEBUG_4	32	SENINF 8 Debug Register 4
1A047D20	SENINF8_MUX_DEBUG_5	32	SENINF 8 Debug Register 5
1A047D24	SENINF8_MUX_DEBUG_6	32	SENINF 8 Debug Register 6
1A047D28	SENINF8_MUX_DEBUG_7	32	SENINF 8 Debug Register 7
1A047D2C	SENINF8_MUX_SPARE	32	SENINF 8 spare Register
1A047D30	SENINF8_MUX_DATA	32	SENINF 8 Data Register
1A047D34	SENINF8_MUX_DATA_CNT	32	SENINF 8 Data Count Register
1A047D38	SENINF8_MUX_CROP	32	SENINF 8 Crop Size Register
1A047D3C	SENINF8_MUX_CTRL_EXT	32	SENINF 8 Control Register Extend

1A047D00 SENINF8_MUX_CTRL **SENINF 8 Control Register** **06DF0080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_MUX_EN	CROP_EN	FIFO_FULL_WR_EN		FIFO_FLUSH_EN						FIFO_PUSH_EN					
Type	RW	RW	RW		RW						RW					
Reset	0	0	0	0	0	1	1	0	1	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_SRC_SEL				OVERRUN_RST_EN	SENINF_HSYNC_POL	SENINF_VSYNC_POL	SENINF_PIX_SEL	SENINF_HSYNC_MASK		SENINF_MUX_RDY_VALUE	SENINF_MUX_RDY_MODE			SENINF_IRQ_SW_RST	SENINF_MUX_SW_RST
Type	RW				RW	RW	RW	RW	RW		RW	RW			RW	RW
Reset	0	0	0	0	0	0	0	0	1		0	0			0	0

Bit(s)	Name	Description
31	SENINF_MUX_EN	**Enables seninf_mux** 0: Disable 1: Enable
30	CROP_EN	**Sensor crop function**
29:28	FIFO_FULL_WR_EN	**0: FIFO write operation is prohibited when FIFO is full.** 1: FIFO write operation is prohibited after FIFO full occurs. 2: FIFO write operation is allowed when FIFO is full.
27:22	FIFO_FLUSH_EN	**Normal mode: 6'b011011** JPEG two pixel mode: 6'b011000
21:16	FIFO_PUSH_EN	**Normal mode: 6'b011111** JPEG two pixel mode : 6'b011110
15:12	SENINF_SRC_SEL	**Selects SENINF input source:** {seninf_mux_sel_ext, seninf_mux_sel} 00: OCSI2 VC0 01: Test model 02: CCIR656 03: Parallel sensor 04: Serial sensor 06: OCSI2 VC1 08: NCSI2 VC0 09: NCSI2 VC1 0A: NCSI2 VC2 0B: NCSI2 VC3 0C: NCSI2 VC4 0D: NCSI2 VC5
11	OVERRUN_RST_EN	**Enables SENINF mux software reset for overrun** 0: No action 1: Auto self-reset for overrun situation
10	SENINF_HSYNC_POL	**SENINF HSYNC polarity**
9	SENINF_VSYNC_POL	**SENINF VSYNC polarity**
8	SENINF_PIX_SEL	**SENINF output bus width:** {seninf_pixel_sel_ext, seninf_pixel_sel} 00: 1 pixel/cycle 01: 2 pixels/cycle 10: 4 pixels/cycle
7	SENINF_HSYNC_MASK	**Masks hsync** 0: Send hsync when vsync = 1

Bit(s)	Name	Description
		1: Does not send hsync when vsync = 1
5	SENINF_MUX_RDY_VALUE	**seninf_rdy value in force mode**
4	SENINF_MUX_RDY_MODE	0: seninf_rdy normal mode 1: seninf_rdy force mode
1	SENINF_IRQ_SW_RST	**SENINF IRQ software reset, active high** 0: De-assert reset 1: Assert reset
0	SENINF_MUX_SW_RST	**SENINF mux software reset, active high** 0: De-assert reset 1: Assert reset

1A047D04 SENINF8_MUX_INTEN **SENINF 8 Interrupt Enable Register** **8000007F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_IRQ_CLR_SEL															
Type	RW															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SENINF_SENSOR_HSIZEERR_IRQ_EN	SENINF_SENSOR_VSIZEERR_IRQ_EN	SENINF_HSIZEERR_IRQ_EN	SENINF_VSIZEERR_IRQ_EN	SENINF_FSMERR_IRQ_EN	SENINF_CRCERR_IRQ_EN	SENINF_OVERRUN_IRQ_EN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										1	1	1	1	1	1	1

Bit(s)	Name	Description
31	SENINF_IRQ_CLR_SEL	0: Read clear 1: Write clear
6	SENINF_SENSOR_HSIZEERR_IRQ_EN	Enables sensor HSIZE ERROR IRQ
5	SENINF_SENSOR_VSIZEERR_IRQ_EN	Enables sensor VSIZE ERROR IRQ
4	SENINF_HSIZEERR_IRQ_EN	Enables async FIFO HSIZE ERROR IRQ
3	SENINF_VSIZEERR_IRQ_EN	Enables async FIFO VSIZE ERROR IRQ
2	SENINF_FSMERR_IRQ_EN	Enables FSM ERROR IRQ
1	SENINF_CRCERR_IRQ_EN	Enables CRR ERROR IRQ
0	SENINF_OVERRUN_IRQ_EN	Enables FIFO OVERRUN IRQ

1A047D08 SENINF8_MUX_INTSTA **SENINF 8 Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name										SENINF_SENSOR_HSIZEERR_IRQ_STA	SENINF_SENSOR_VSIZEERR_IRQ_STA	SENINF_HSIZEERR_IRQ_STA	SENINF_VSIZEERR_IRQ_STA	SENINF_FSMERR_IRQ_STA	SENINF_CRCERR_IRQ_STA	SENINF_OVERRUN_IRQ_STA
Type										RO	RO	RO	RO	RO	RO	RO
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	SENINF_SENSOR_HSIZEERR_IRQ_STA	Sensor HSIZE ERROR IRQ status
5	SENINF_SENSOR_VSIZEERR_IRQ_STA	Sensor VSIZE ERROR IRQ status
4	SENINF_HSIZEERR_IRQ_STA	Async FIFO HSIZE ERROR IRQ status
3	SENINF_VSIZEERR_IRQ_STA	Async FIFO VSIZE ERROR IRQ status
2	SENINF_FSMERR_IRQ_STA	FSM ERROR IRQ status
1	SENINF_CRCERR_IRQ_STA	CRR ERROR IRQ status
0	SENINF_OVERRUN_IRQ_STA	FIFO OVERRUN IRQ status

1A047D0C SENINF8_MUX_SIZE — SENINF 8 Image Size Register — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_HSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_VSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_HSIZE	Senor image horizontal size
15:0	SENINF_VSIZE	Senor image vertical size

1A047D10 SENINF8_MUX_DEBUG_1 — SENINF 8 Debug Register 1 — 0000C303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	1	1	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A047D14 SENINF8_MUX_DEBUG_2 SENINF 8 Debug Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A047D18 SENINF8_MUX_DEBUG_3 SENINF 8 Debug Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A047D1C SENINF8_MUX_DEBUG_4 SENINF 8 Debug Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A047D20 SENINF8_MUX_DEBUG_5 SENINF 8 Debug Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A047D24 SENINF8_MUX_DEBUG_6 — SENINF 8 Debug Register 6 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A047D28 SENINF8_MUX_DEBUG_7 — SENINF 8 Debug Register 7 — 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_INFO	Debugging information

1A047D2C SENINF8_MUX_SPARE — SENINF 8 spare Register — 000E2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SENI NF_S PARE			
Type													RW			
Reset													1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENI NF_S PARE		SENI NF_F IFO_ FULL	SENI NF_V CNT_ SEL		SENINF_CR C_SEL										

			_SEL													
Type	RW		RW	RW		RW										
Reset	0	0	1	0	0	0	0									

Bit(s)	Name	Description
19:14	SENINF_SPARE	**Spare register**
13	SENINF_FIFO_FULL_SEL	0: Does not send FIFO full to cam 1: Send FIFO full to cam
12:11	SENINF_VCNT_SEL	0: Vsync rising 1: Vsync rising d1 2: Vsync rising d2 3: Vsync rising d3
10:9	SENINF_CRC_SEL	0: Vsync rising 1: Vsync rising d1 2: Vsync rising d2 3: Vsync rising d3

1A047D30 SENINF8_MUX_DATA SENINF 8 Data Register 40000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA1															
Type	RO															
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_DATA1	
15:0	SENINF_DATA0	

1A047D34 SENINF8_MUX_DATA_CNT SENINF 8 Data Count Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_DATA_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_DATA_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENINF_DATA_CNT	

1A047D38 SENINF8_MUX_CROP SENINF 8 Crop Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENINF_CROP_X2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENINF_CROP_X1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SENINF_CROP_X2	
15:0	SENINF_CROP_X1	

1A047D3C SENINF8_MUX_CTRL_EXT **SENINF 8 Control Register Extend** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												SENINF_PIX_SEL_EXT			SENINF_SRC_SEL_EXT	
Type												RW			RW	
Reset												0			0	0

Bit(s)	Name	Description
4	SENINF_PIX_SEL_EXT	**SENINF output bus width:** {seninf_pixel_sel_ext, seninf_pixel_sel} 00: 1 pixel/cycle 01: 2 pixels/cycle 10: 4 pixels/cycle
1:0	SENINF_SRC_SEL_EXT	**Selects SENINF input source:** {seninf_src_sel_ext, seninf_src_sel} 18: CSI2 VC0 19: CSI2 VC1 1A: CSI2 VC2 1B: CSI2 VC3 1C: CSI2 VC4 28: CSI3 VC0 29: CSI3 VC1 2A: CSI3 VC2 2B: CSI3 VC3 2C: CSI3 VC4

Module name: SENINF_N3D_A Base address: (+1a040100h)

Address	Name	Width	Register Function
1A040100	SENINF_N3D_ASENINF_N3D_A_CTL	32	N3D_A_CTL

Address	Name	Width	Register Function
1A040104	SENINF_N3D_ASENINF_N3D_A_POS	32	N3D_A_POS
1A040108	SENINF_N3D_ASENINF_N3D_A_TRIG	32	N3D_A_TRIG
1A04010C	SENINF_N3D_ASENINF_N3D_A_INT	32	N3D_A_INT
1A040110	SENINF_N3D_ASENINF_N3D_A_CNT0	32	N3D_A_CNT0
1A040114	SENINF_N3D_ASENINF_N3D_A_CNT1	32	N3D_A_CNT1
1A040118	SENINF_N3D_ASENINF_N3D_A_DBG	32	N3D_A_DBG
1A04011C	SENINF_N3D_ASENINF_N3D_A_DIFF_THR	32	N3D_A_DIFF_THR
1A040120	SENINF_N3D_ASENINF_N3D_A_DIFF_CNT	32	N3D_A_DIFF_CNT

1A040100 SENINF_N3D_ASENINF_N3D_A_CTL N3D_A_CTL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SEN2_OV_VS_INT_EN	SEN1_OV_VS_INT_EN	SEN2_TIM_EN	SEN1_TIM_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MODE1_DBG	DDBG_SEL			DIFF_EN	W1CLR	N3D_EN	I2C2_INT_EN	I2C1_INT_EN	I2C2_EN	I2C1_EN	MODE	
Type				RW	RW			RW	RW	RW	RW	RW	RW	RW	RW	
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	SEN2_OV_VS_INT_EN	**SEN2_OV_VS_INT_EN**
18	SEN1_OV_VS_INT_EN	**SEN1_OV_VS_INT_EN**
17	SEN2_TIM_EN	**Enables sensor 2 CQ/I2C** This enable is exclusive with i2c2_en.
16	SEN1_TIM_EN	**Enables sensor 1 CQ/I2C** This enable is exclusive with i2c1_en.
12	MODE1_DBG	0: Normal mode 1: DBG mode
11:9	DDBG_SEL	**DBG_SEL** 0: DBG port is cnt2_vs1 1: Internal state machine
8	DIFF_EN	**Enables different count**
7	W1CLR	**Write one clear for int status**
6	N3D_EN	**Enable N3D**
5	I2C2_INT_EN	**I2C2 RDY interrupt**
4	I2C1_INT_EN	**I2C1 RDY interrupt**
3	I2C2_EN	**Enables I2C2**

Bit(s)	Name	Description
2	I2C1_EN	**Enables I2C1**
1:0	MODE	**N3D mode** 0: Immediate trigger 1: Referenece VS1 2: I2C1 before I2C2 3: I2C2 before I2C1

1A040104 SENINF_N3D_ASENINF_N3D_A_POS N3D_A_POS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N3D_POS															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N3D_POS															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	N3D_POS	**In mode 2/3, TG1/TG2 time difference** Unit: bclk. In mode 1, it relates to VS1 position.

1A040108 SENINF_N3D_ASENINF_N3D_A_TRIG N3D_A_TRIG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															I2CB_TRIG	I2CA_TRIG
Type															WO	WO
Reset															0	0

Bit(s)	Name	Description
1	I2CB_TRIG	**Triggers I2CB** Mode 0: I2C2 trigger Mode 1, 2, 3: No use
0	I2CA_TRIG	**Triggers I2CA** Mode 0: I2C1 trigger Mode 1, 2, 3: I2C 1/2 trigger

1A04010C SENINF_N3D_ASENINF_N3D_A_INT N3D_A_INT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											SEN2_OV_VS_INT	SEN1_OV_VS_INT		DIFF_INT	I2C2_INT	I2C1_INT
Type											RO	RO		RO	RO	RO
Reset											0	0		0	0	0

Bit(s)	Name	Description
5	SEN2_OV_VS_INT	SEN2_OV_VS_INT
4	SEN1_OV_VS_INT	SEN1_OV_VS_INT
2	DIFF_INT	DIFF interrupt
1	I2C2_INT	I2C2 ready
0	I2C1_INT	I2C1 ready

1A040110 SENINF_N3D_ASENINF_N3D_A_CNT0 N3D_A_CNT0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N3D_CNT0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N3D_CNT0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	N3D_CNT0	TG1 period cnt

1A040114 SENINF_N3D_ASENINF_N3D_A_CNT1 N3D_A_CNT1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N3D_CNT1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N3D_CNT1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	N3D_CNT1	TG2 period cnt

1A040118 SENINF_N3D_ASENINF_N3D_A_DBG N3D_A_DBG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N3D_DBG															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N3D_DBG															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	N3D_DBG	N3D debug port

1A04011C SENINF_N3D_ASENINF_N3D_A_DIFF_THR N3D_A_DIFF_THR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N3D_DIFF_THR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N3D_DIFF_THR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	N3D_DIFF_THR	If two vsync difference > this threshold, diff_int will be issued",N3D_DIFF_THR

1A040120 SENINF_N3D_ASENINF_N3D_A_DIFF_CNT N3D_A_DIFF_CNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N3D_DIFF_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N3D_DIFF_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	N3D_DIFF_CNT	bit[31]: 1: vs2 after vs1 0: vs1 after vs2 bit[30:0]: Absolute value for diffcnt

Module name: SENINF_N3D_B Base address: (+1a041100h)

Address	Name	Width	Register Function
1A041100	SENINF_N3D_BSENINF_N3D_B_CTL	32	N3D_B_CTL

Address	Name	Width	Register Function
1A041104	SENINF_N3D_BSENINF_N3D_B_POS	32	N3D_B_POS
1A041108	SENINF_N3D_BSENINF_N3D_B_TRIG	32	N3D_B_TRIG
1A04110C	SENINF_N3D_BSENINF_N3D_B_INT	32	N3D_B_INT
1A041110	SENINF_N3D_BSENINF_N3D_B_CNT0	32	N3D_B_CNT0
1A041114	SENINF_N3D_BSENINF_N3D_B_CNT1	32	N3D_B_CNT1
1A041118	SENINF_N3D_BSENINF_N3D_B_DBG	32	N3D_B_DBG
1A04111C	SENINF_N3D_BSENINF_N3D_B_DIFF_THR	32	N3D_B_DIFF_THR
1A041120	SENINF_N3D_BSENINF_N3D_B_DIFF_CNT	32	N3D_B_DIFF_CNT

1A041100 SENINF_N3D_BSENINF_N3D_B_CTL N3D_B_CTL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SEN2_OV_VS_INT_EN	SEN1_OV_VS_INT_EN	SEN2_TIM_EN	SEN1_TIM_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MODE1_DBG	DDBG_SEL			DIFF_EN	W1CLR	N3D_EN	I2C2_INT_EN	I2C1_INT_EN	I2C2_EN	I2C1_EN	MODE	
Type				RW	RW			RW	RW	RW	RW	RW	RW	RW	RW	
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	SEN2_OV_VS_INT_EN	**SEN2_OV_VS_INT_EN**
18	SEN1_OV_VS_INT_EN	**SEN1_OV_VS_INT_EN**
17	SEN2_TIM_EN	**Enables sensor 2 CQ/I2C** This enable is exclusive with i2c2_en.
16	SEN1_TIM_EN	**Enables sensor 1 CQ/I2C** This enable is exclusive with i2c1_en.
12	MODE1_DBG	0: Normal mode 1: DBG mode
11:9	DDBG_SEL	**DBG_SEL** 0: DBG port is cnt2_vs1 1: Internal state machine
8	DIFF_EN	**Enables different count**
7	W1CLR	**Write one clear for int status**
6	N3D_EN	**Enables N3D**
5	I2C2_INT_EN	**I2C2 RDY interrupt**
4	I2C1_INT_EN	**I2C1 RDY interrupt**
3	I2C2_EN	**Enables I2C2**

Bit(s)	Name	Description
2	I2C1_EN	**Enables I2C1**
1:0	MODE	**N3D mode** 0: Immediate trigger 1: Referenece VS1 2: I2C1 before I2C2 3: I2C2 before I2C1

1A041104 SENINF_N3D_BSENINF_N3D_B_POS N3D_B_POS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N3D_POS															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N3D_POS															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	N3D_POS	**In mode 2/3, TG1/TG2 time difference** Unit: bclk. In mode 1, it relates to VS1 position.

1A041108 SENINF_N3D_BSENINF_N3D_B_TRIG N3D_B_TRIG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															I2CB_TRIG	I2CA_TRIG
Type															WO	WO
Reset															0	0

Bit(s)	Name	Description
1	I2CB_TRIG	**Triggers I2CB** Mode 0: I2C2 trigger Mode 1, 2, 3: No use
0	I2CA_TRIG	**Triggers I2CA** Mode 0: I2C1 trigger Mode 1, 2, 3: I2C 1/2 trigger

1A04110C SENINF_N3D_BSENINF_N3D_B_INT N3D_B_INT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											SEN2_OV_VS_INT	SEN1_OV_VS_INT		DIFF_INT	I2C2_INT	I2C1_INT
Type											RO	RO		RO	RO	RO
Reset											0	0		0	0	0

Bit(s)	Name	Description
5	SEN2_OV_VS_INT	SEN2_OV_VS_INT
4	SEN1_OV_VS_INT	SEN1_OV_VS_INT
2	DIFF_INT	DIFF interrupt
1	I2C2_INT	I2C2 ready
0	I2C1_INT	I2C1 ready

1A041110 SENINF_N3D_BSENINF_N3D_B_CNT0 N3D_B_CNT0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N3D_CNT0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N3D_CNT0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	N3D_CNT0	TG1 period cnt

1A041114 SENINF_N3D_BSENINF_N3D_B_CNT1 N3D_B_CNT1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N3D_CNT1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N3D_CNT1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	N3D_CNT1	TG2 period cnt

1A041118 SENINF_N3D_BSENINF_N3D_B_DBG N3D_B_DBG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N3D_DBG															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N3D_DBG															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	N3D_DBG	N3D debug port

1A04111C SENINF_N3D_BSENINF_N3D_B_DIFF_THR N3D_B_DIFF_THR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N3D_DIFF_THR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N3D_DIFF_THR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	N3D_DIFF_THR	If two vsync difference > this threshold, diff_int will be issued",N3D_DIFF_THR

1A041120 SENINF_N3D_BSENINF_N3D_B_DIFF_CNT N3D_B_DIFF_CNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N3D_DIFF_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N3D_DIFF_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	N3D_DIFF_CNT	**bit[31]:** 1: vs2 after vs1 0: vs1 after vs2 bit[30:0]: Absolute value for diffcnt