AES-ULTRA96-G
Avnet Design Services
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02 - Block Diagram
03 - Zynq Bank 0
04 - Zynq Banks 26 - HD
05 - Zynq Banks 65 66 - HP
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17 - Expansion Headers
18 - PS Display Port Connector
19 - PS Display Port IO
20 - PS Micro SD Card
21 - PS WiFi - Bluetooth
22 - PS USB 3_0 ULPI Upstream
23 - PS USB 3_0 ULPI Downstream
24 - PS USB 3_0 Hub
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AES-ULTRA96-G

Revision:1

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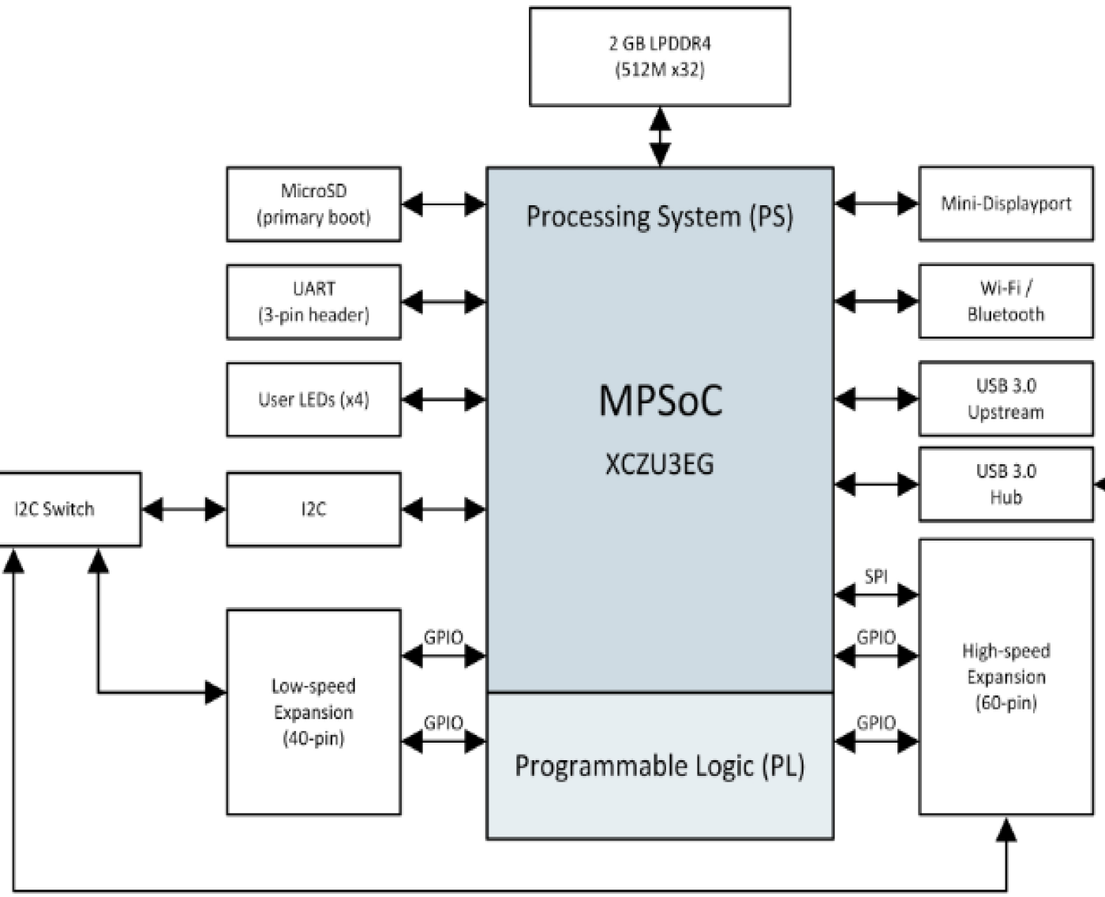
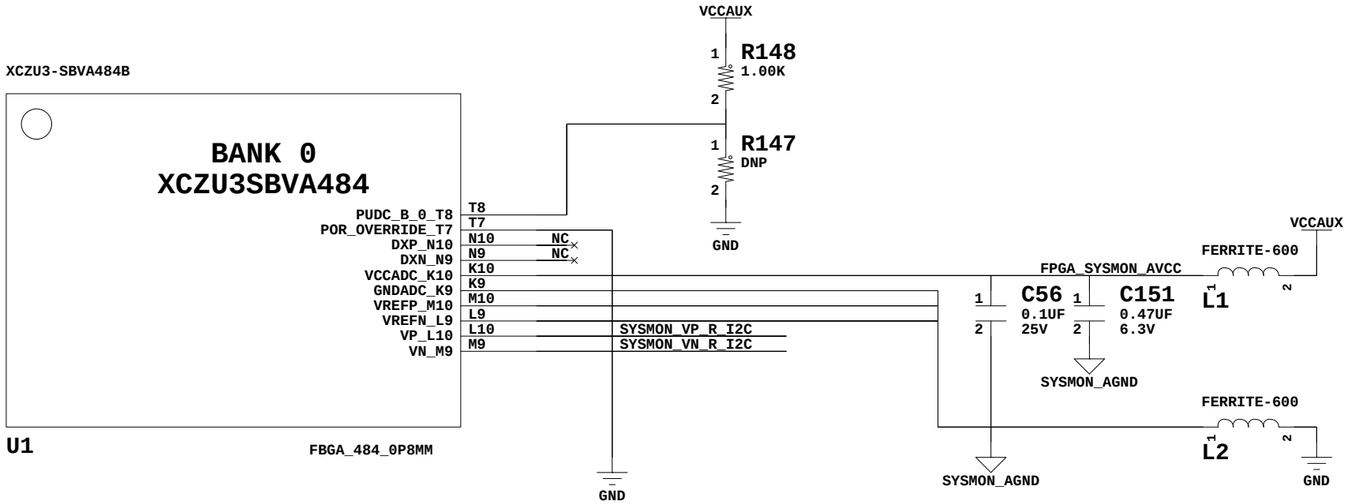
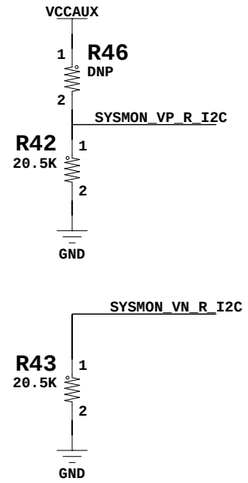
AVNET Avnet Design Services			
Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: Avnet Lead Sheet	Size: B	Sheet: 1 of 27	



AVNET	Avnet Design Services
Project Name: AES-ULTRA96-G	PCB Rev: 1 / BOM: 01 / Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018 / Time: 12:24:07 pm
Sheet Title: **Block Diagram**	Size: B / Sheet: 2 of 27

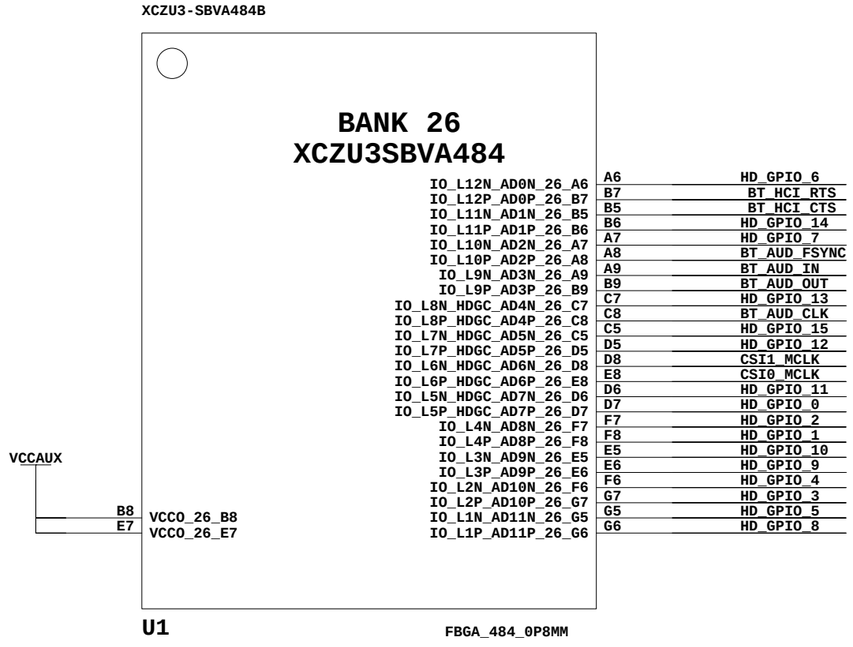




SYSMON I2C Address selection

Zynq Bank 0

AVNET Avnet Design Services			
Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: Zynq Bank 0	Size: B	Sheet: 3 of 27	



Zynq Banks 26 - HD

Avnet Design Services			
Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: Zynq Banks 26 - HD	Size: B	Sheet: 4 of 27	

XCZU3-SBVA484B

BANK 65
XCZU3SBVA484

IO_T3U_N12_65_F4	F4	FAN_PWM
IO_L24N_T3U_N11_PERSTN0_65_C2	C2	HSIC_DATA
IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65_D2	D2	NC
IO_L23N_T3U_N9_65_F2	F2	NC
IO_L23P_T3U_N8_I2C_SCLK_65_F3	F3	NC
IO_L22N_T3U_N7_DBC_AD0N_65_C3	C3	DSI_D3_N
IO_L22P_T3U_N6_DBC_AD0P_65_D3	D3	DSI_D3_P
IO_L21N_T3L_N5_AD8N_65_D1	D1	DSI_D2_N
IO_L21P_T3L_N4_AD8P_65_E1	E1	DSI_D2_P
IO_L20N_T3L_N3_AD1N_65_E3	E3	DSI_D1_N
IO_L20P_T3L_N2_AD1P_65_E4	E4	DSI_D1_P
IO_L19N_T3L_N1_DBC_AD9N_65_F1	F1	DSI_D0_N
IO_L19P_T3L_N0_DBC_AD9P_65_G1	G1	DSI_D0_P
IO_T2U_N12_65_H3	H3	NC
IO_L18N_T2U_N11_AD2N_65_G4	G4	NC
IO_L18P_T2U_N10_AD2P_65_H4	H4	NC
IO_L17N_T2U_N9_AD10N_65_G2	G2	NC
IO_L17P_T2U_N8_AD10P_65_H2	H2	NC
IO_L16N_T2U_N7_QBC_AD3N_65_H5	H5	DSI_CLK_N
IO_L16P_T2U_N6_QBC_AD3P_65_J5	J5	DSI_CLK_P
IO_L15N_T2L_N5_AD11N_65_J1	J1	NC
IO_L15P_T2L_N4_AD11P_65_K1	K1	NC
IO_L14N_T2L_N3_GC_65_K3	K3	NC
IO_L14P_T2L_N2_GC_65_K4	K4	NC
IO_L13N_T2L_N1_GC_QBC_65_J2	J2	NC
IO_L13P_T2L_N0_GC_QBC_65_J3	J3	NC
IO_T1U_N12_65_N3	N3	NC
IO_L12N_T1U_N11_GC_65_L3	L3	NC
IO_L12P_T1U_N10_GC_65_L4	L4	NC
IO_L11N_T1U_N9_GC_65_L1	L1	CSI0_D3_N
IO_L11P_T1U_N8_GC_65_L2	L2	CSI0_D3_P
IO_L10N_T1U_N7_QBC_AD4N_65_M4	M4	CSI0_D2_N
IO_L10P_T1U_N6_QBC_AD4P_65_M5	M5	CSI0_D2_P
IO_L9N_T1L_N5_AD12N_65_M1	M1	CSI0_D1_N
IO_L9P_T1L_N4_AD12P_65_M2	M2	CSI0_D1_P
IO_L8N_T1L_N3_AD5N_65_N4	N4	CSI0_D0_N
IO_L8P_T1L_N2_AD5P_65_N5	N5	CSI0_D0_P
IO_L7N_T1L_N1_QBC_AD13N_65_P1	P1	CSI0_C_N
IO_L7P_T1L_N0_QBC_AD13P_65_N2	N2	CSI0_C_P
IO_T0U_N12_VRP_65_P2	P2	
IO_L6N_T0U_N11_AD6N_65_R5	R5	NC
IO_L6P_T0U_N10_AD6P_65_P5	P5	NC
IO_L5N_T0U_N9_AD14N_65_T1	T1	NC
IO_L5P_T0U_N8_AD14P_65_R1	R1	NC
IO_L4N_T0U_N7_DBC_AD7N_65_T4	T4	NC
IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65_R4	R4	NC
IO_L3N_T0L_N5_AD15N_65_U1	U1	CSI1_D1_N
IO_L3P_T0L_N4_AD15P_65_U2	U2	CSI1_D1_P
IO_L2N_T0L_N3_65_R3	R3	CSI1_D0_N
IO_L2P_T0L_N2_65_P3	P3	CSI1_D0_P
IO_L1N_T0L_N1_DBC_65_T2	T2	CSI1_C_N
IO_L1P_T0L_N0_DBC_65_T3	T3	CSI1_C_P
VREF_65_K5	K5	NC

VCCO_HP

B3	VCCO_65_B3
G3	VCCO_65_G3
K2	VCCO_65_K2
P4	VCCO_65_P4

R145: 240, 1/20W, 1%

GND

U1

FBGA_484_0P8MM

XCZU3-SBVA484B

BANK 66
XCZU3SBVA484

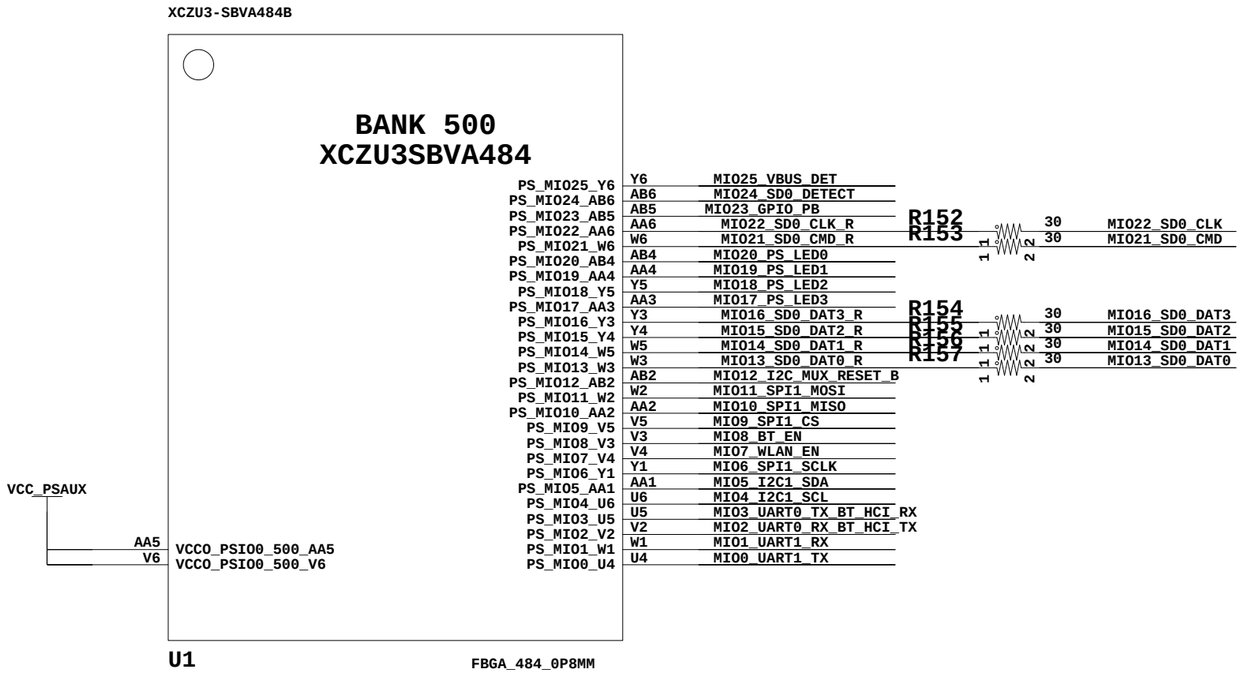
IO_T3U_N12_66_A2	A2	HSIC_STR
IO_L12N_T1U_N11_GC_66_A3	A3	NC
IO_L12P_T1U_N10_GC_66_A4	A4	NC
IO_L11N_T1U_N9_GC_66_B1	B1	NC
IO_L11P_T1U_N8_GC_66_B2	B2	NC
IO_T0U_N12_VRP_66_B4	B4	NC
VREF_66_C4	C4	NC

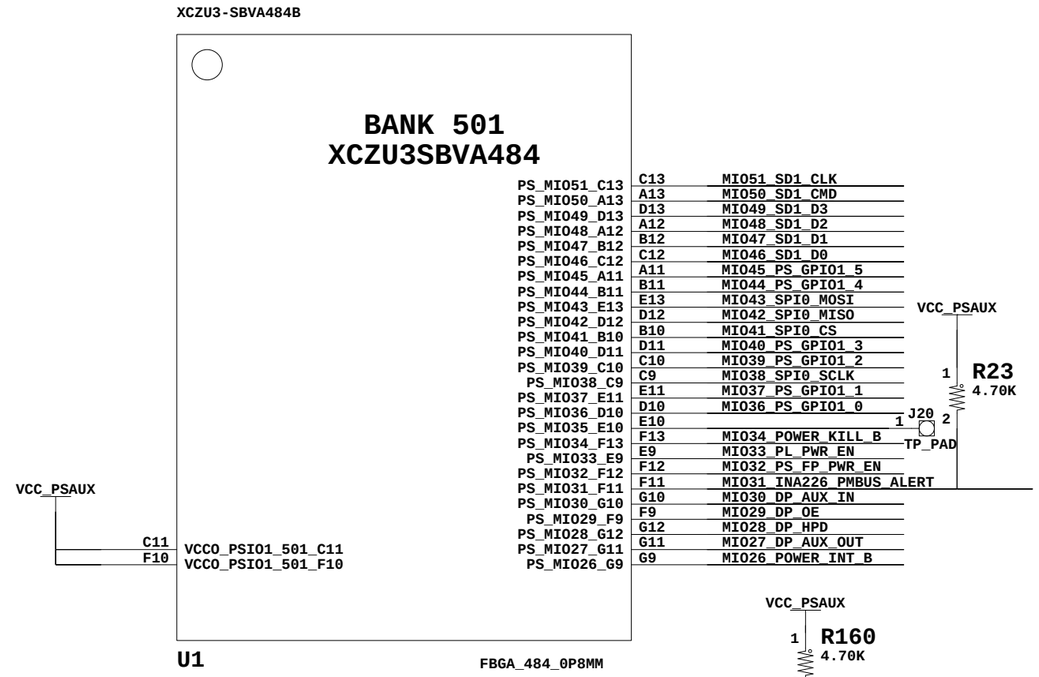
U1

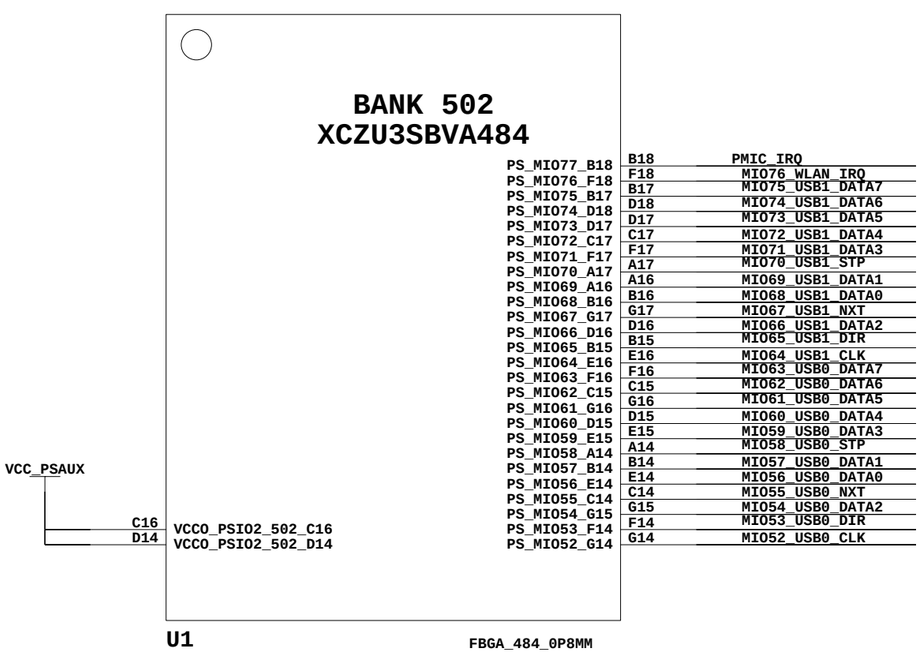
FBGA_484_0P8MM

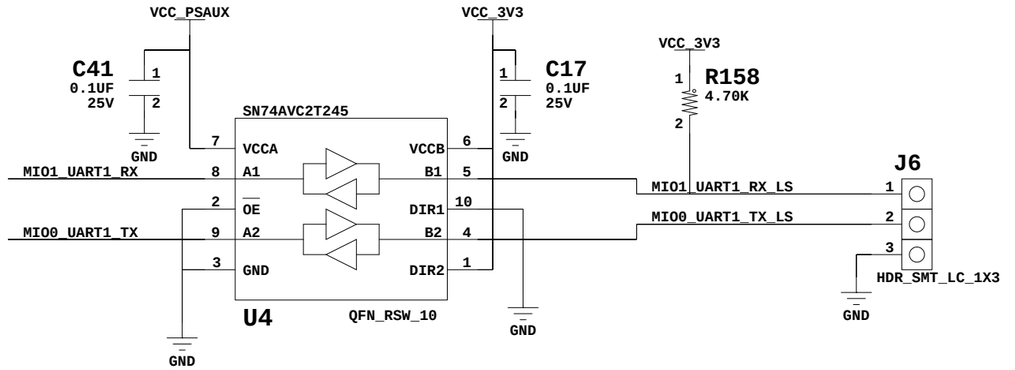
Zynq Banks 65 66 - HP

Avnet Design Services			
Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: Zynq Banks 65 66 - HP	Size: B	Sheet: 5 of 27	



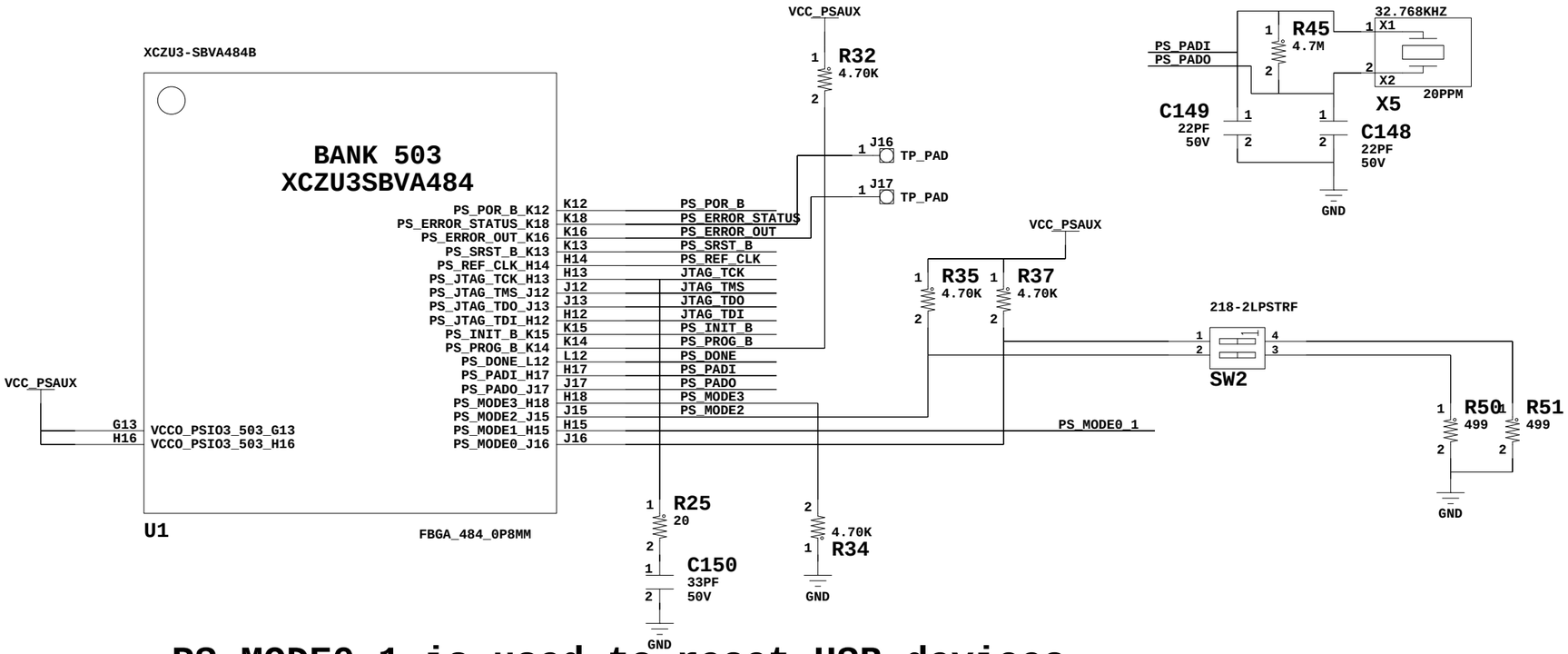




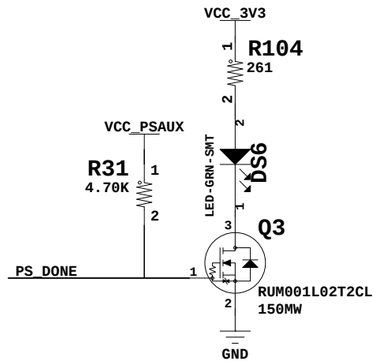


Zynq Banks 500 501 502 - MIO

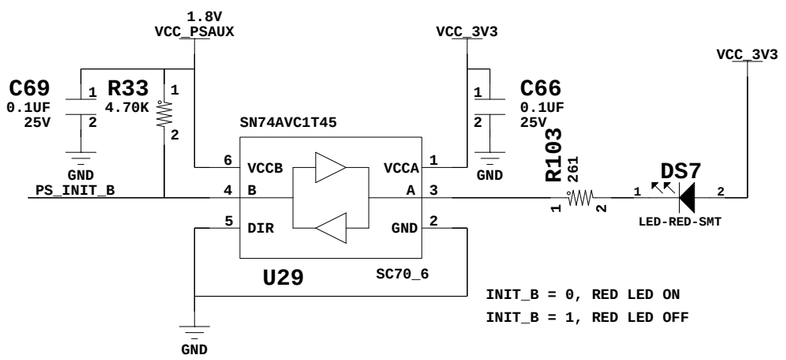
Avnet Design Services			
Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: Zynq Banks 500 501 502 - MIO	Size: B	Sheet: 6 of 27	



PS_MODE0_1 is used to reset USB devices



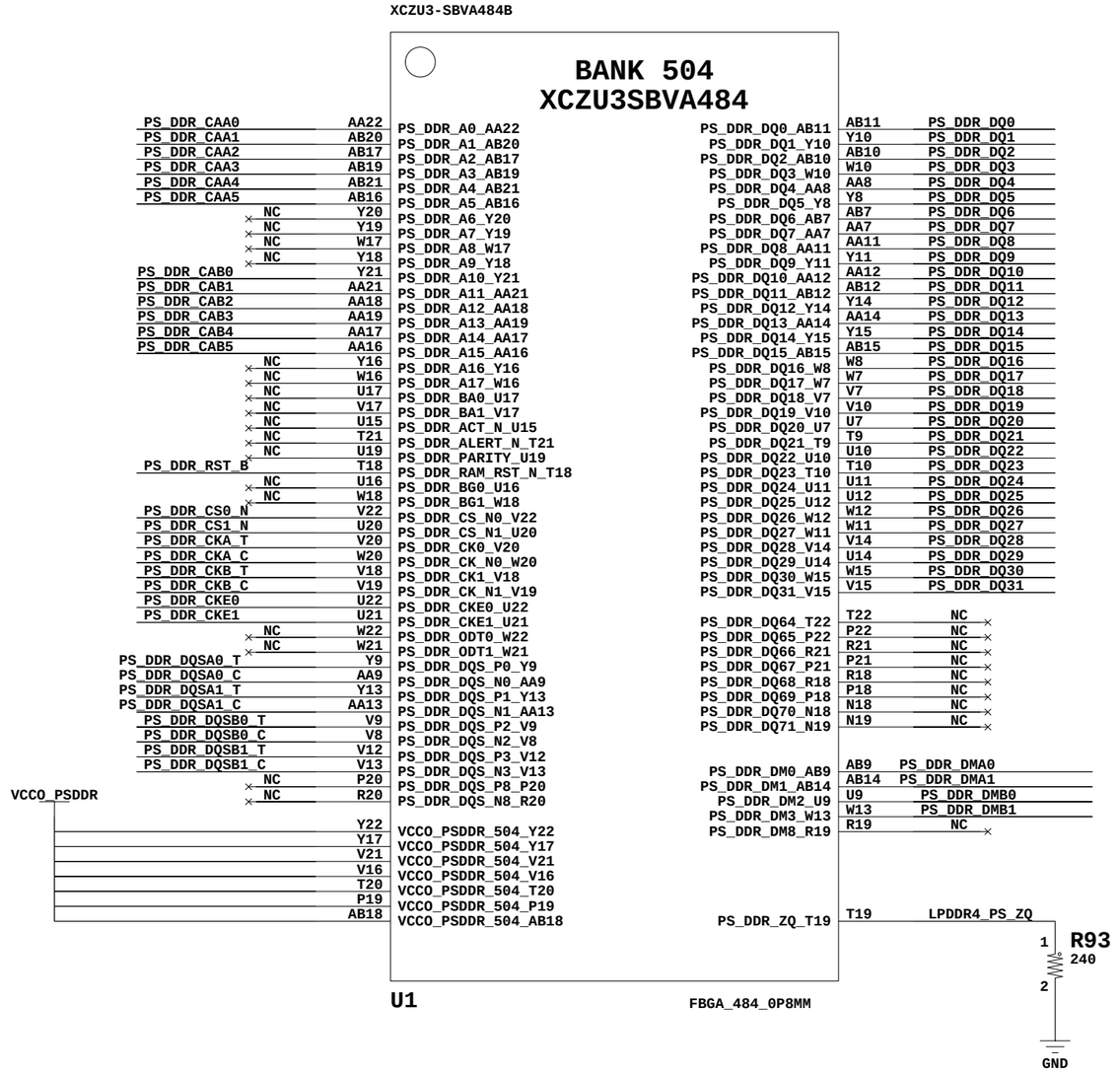
DONE_0 = 0, DONE LED OFF
DONE_0 = 1, DONE LED ON



INIT_B = 0, RED LED ON
INIT_B = 1, RED LED OFF

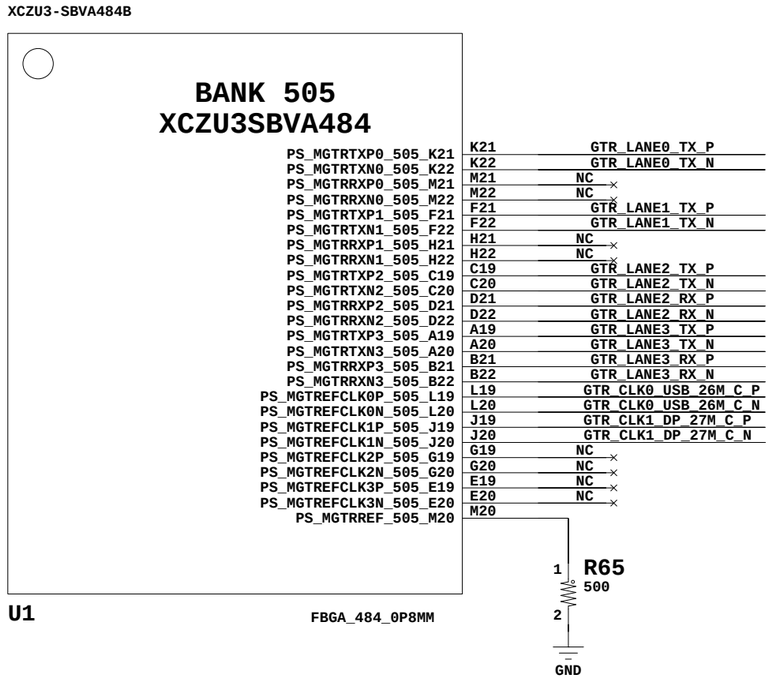
Zynq Banks 503 - Config

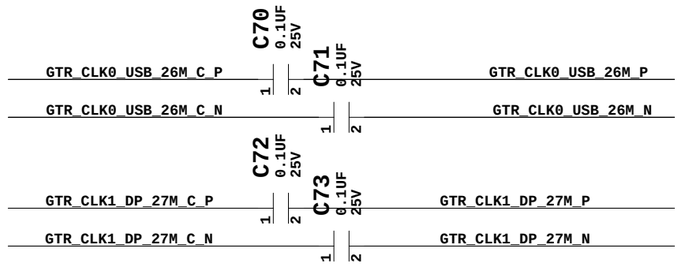
AVNET Avnet Design Services				
Project Name: AES-ULTRA96-G		PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm		
Sheet Title: Zynq Banks 503 - Config	Size: B	Sheet: 7 of 27		



Zynq Bank 504 - Memory

Avnet Design Services			
Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: Zynq Bank 504 - Memory	Size: B	Sheet: 8 of 27	

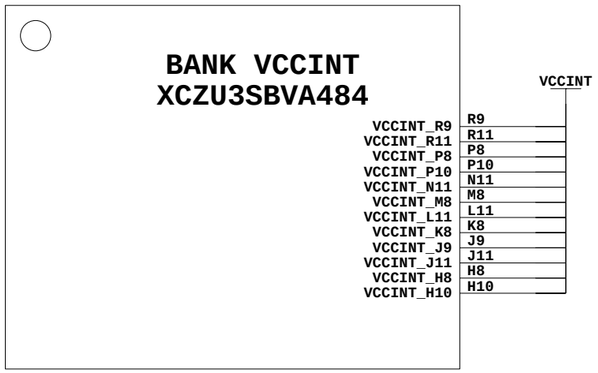




Zynq Banks 505 - GTR

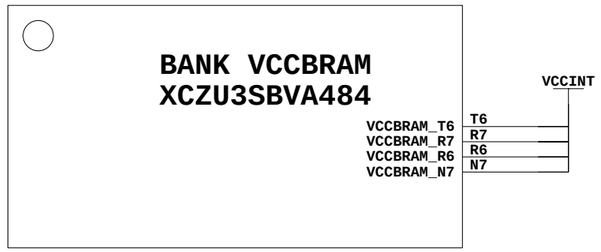
AVNET Avnet Design Services			
Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: Zynq Banks 505 - GTR	Size: B	Sheet: 9 of 27	

XCZU3-SBVA484B



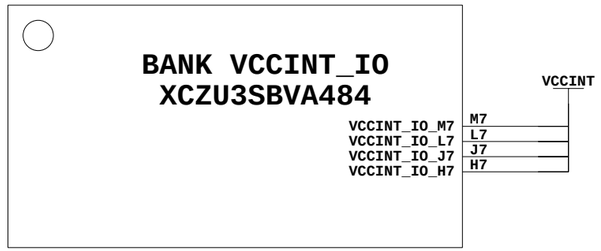
U1 FBGA_484_0P8MM

XCZU3-SBVA484B



U1 FBGA_484_0P8MM

XCZU3-SBVA484B

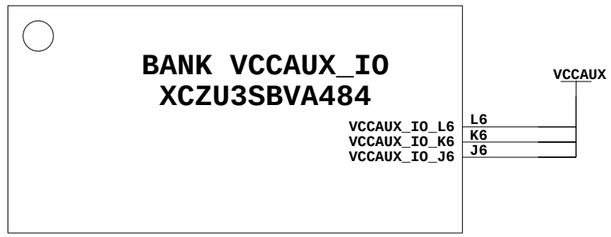


U1 FBGA_484_0P8MM

XCZU3-SBVA484B

U1 FBGA_484_0P8MM

XCZU3-SBVA484B



U1 FBGA_484_0P8MM

Zynq Power 1

AVNET Avnet Design Services				
Project Name: AES-ULTRA96-G		PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm		
Sheet Title: Zynq Power 1		Size: B	Sheet: 10 of 27	

XCZU3-SBVA484B

BANK PS_MGTRAVCC
XCZU3SBVA484

PS_MGTRAVCC_K19 K19
PS_MGTRAVCC_H19 H19
PS_MGTRAVCC_F19 F19

MGTRAVCC

U1

FBGA_484_0P8MM

XCZU3-SBVA484B

BANK PS_MGTRAVTT
XCZU3SBVA484

PS_MGTRAVTT_D19 D19
PS_MGTRAVTT_B19 B19
PS_MGTRAVTT_A21 A21

MGTRAVTT

U1

FBGA_484_0P8MM

XCZU3-SBVA484B

BANK PS_POWER
XCZU3SBVA484

VCC_PSPLL_M12 M12
VCC_PSPLL_L14 L14
VCC_PSPLL_L13 L13
VCC_PSINTLP_R14 R14
VCC_PSINTLP_R13 R13
VCC_PSINTLP_P13 P13
VCC_PSINTLP_P12 P12
VCC_PSINTLP_N13 N13
VCC_PSINTLP_N12 N12
VCC_PSINTFP_DDR_T17 T17
VCC_PSINTFP_DDR_P17 P17
VCC_PSINTFP_DDR_N17 N17
VCC_PSINTFP_T16 T16
VCC_PSINTFP_T14 T14
VCC_PSINTFP_T13 T13
VCC_PSINTFP_T12 T12
VCC_PSINTFP_R16 R16
VCC_PSINTFP_R15 R15
VCC_PSINTFP_N14 N14
VCC_PSDDR_PLL_M15 M15
VCC_PSDDR_PLL_M14 M14
VCC_PSBATT_N15 N15
VCC_PSAUX_M17 M17
VCC_PSAUX_M16 M16
VCC_PSAUX_L17 L17
VCC_PSAUX_L16 L16
VCC_PSADC_P15 P15
GND_PSADC_P16 P16

VCC_PSPLL
VCC_PSINTLP
VCC_PSINTFP
VCC_PSAUX

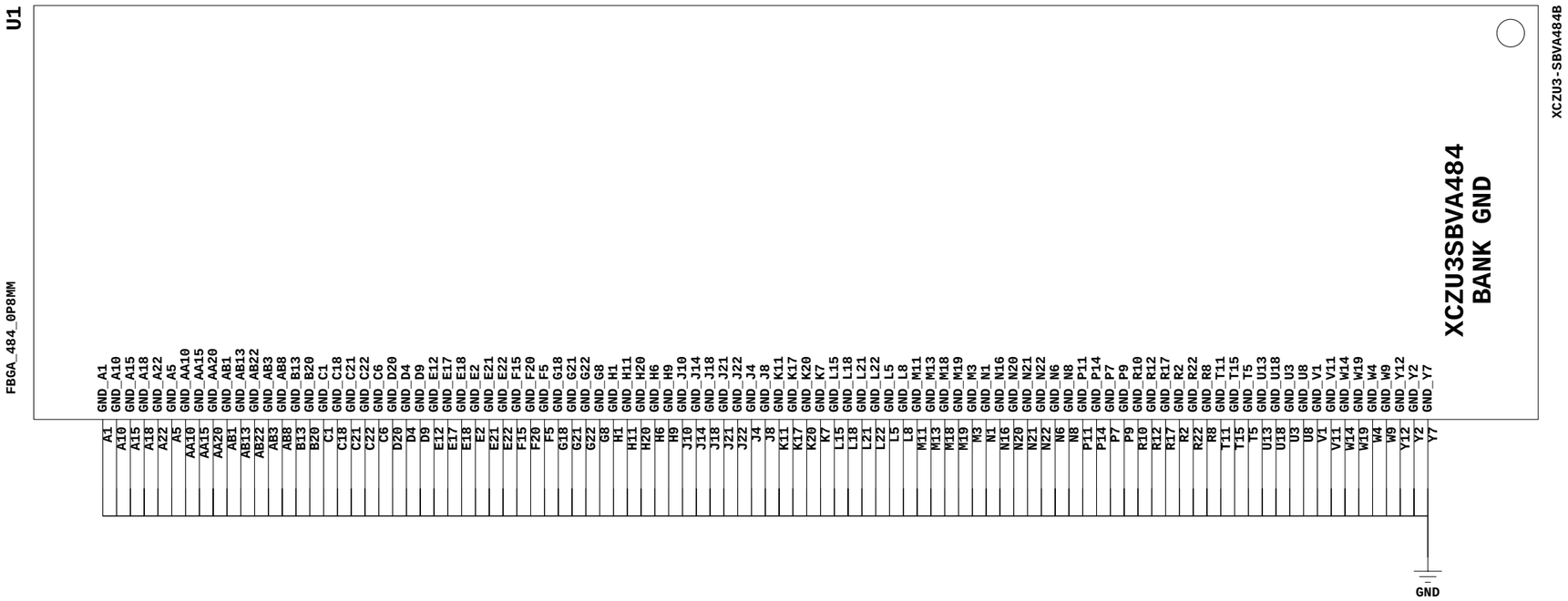
U1

FBGA_484_0P8MM

VCC_PSAUX
FERRITE-600
PS_SYSMON_AVCC
C65 0.1UF 25V
C152 0.47UF 6.3V
L3
PS_SYSMON_AGND
FERRITE-600
L4
GND
PS_SYSMON_AGND

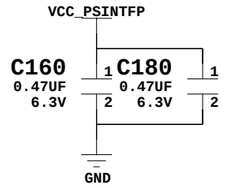
Zynq Power 2

AVNET Avnet Design Services			
Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: Zynq Power 2	Size: B	Sheet: 11 of 27	

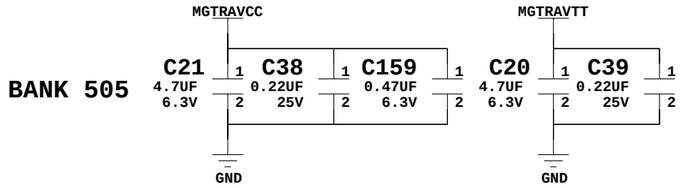


Zynq GND

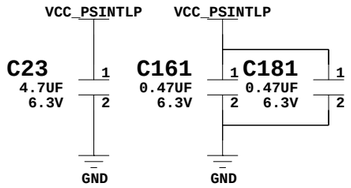
AVNET Avnet Design Services			
Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: Zynq GND	Size: B	Sheet: 12 of 27	



VCCPSINTFP

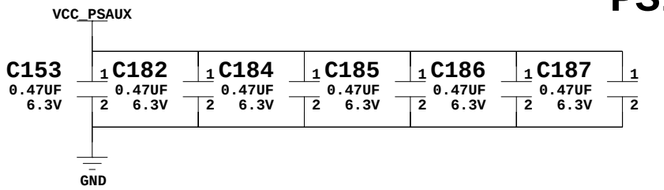


MGTRAVCC/AVTT

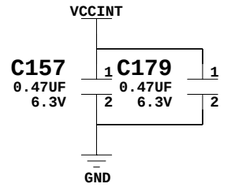


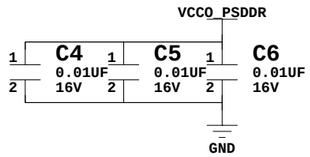
VCCPSINTLP

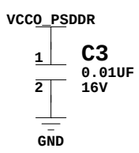
VCCPSAUX/PSADC/PSDDRPLL PSIO1-3



PL VCCINT/VCCBRAM

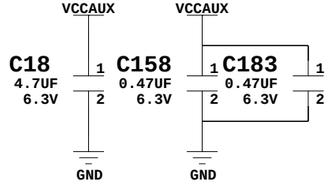






VCCPSDDR

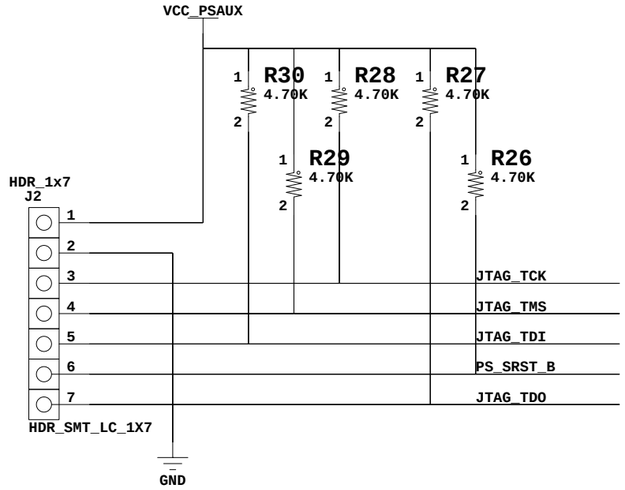
Place this cap directly under U1



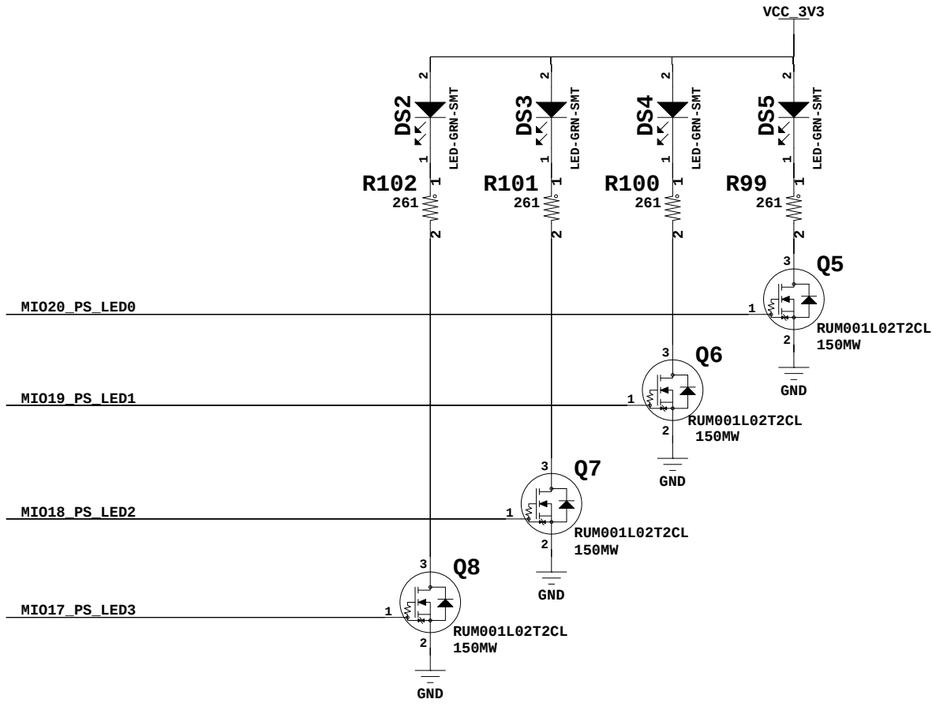
PL VCCAUX / VCCAUX_IO

Zynq Decoupling

AVNET Avnet Design Services			
Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: Zynq Decoupling	Size: B	Sheet: 13 of 27	



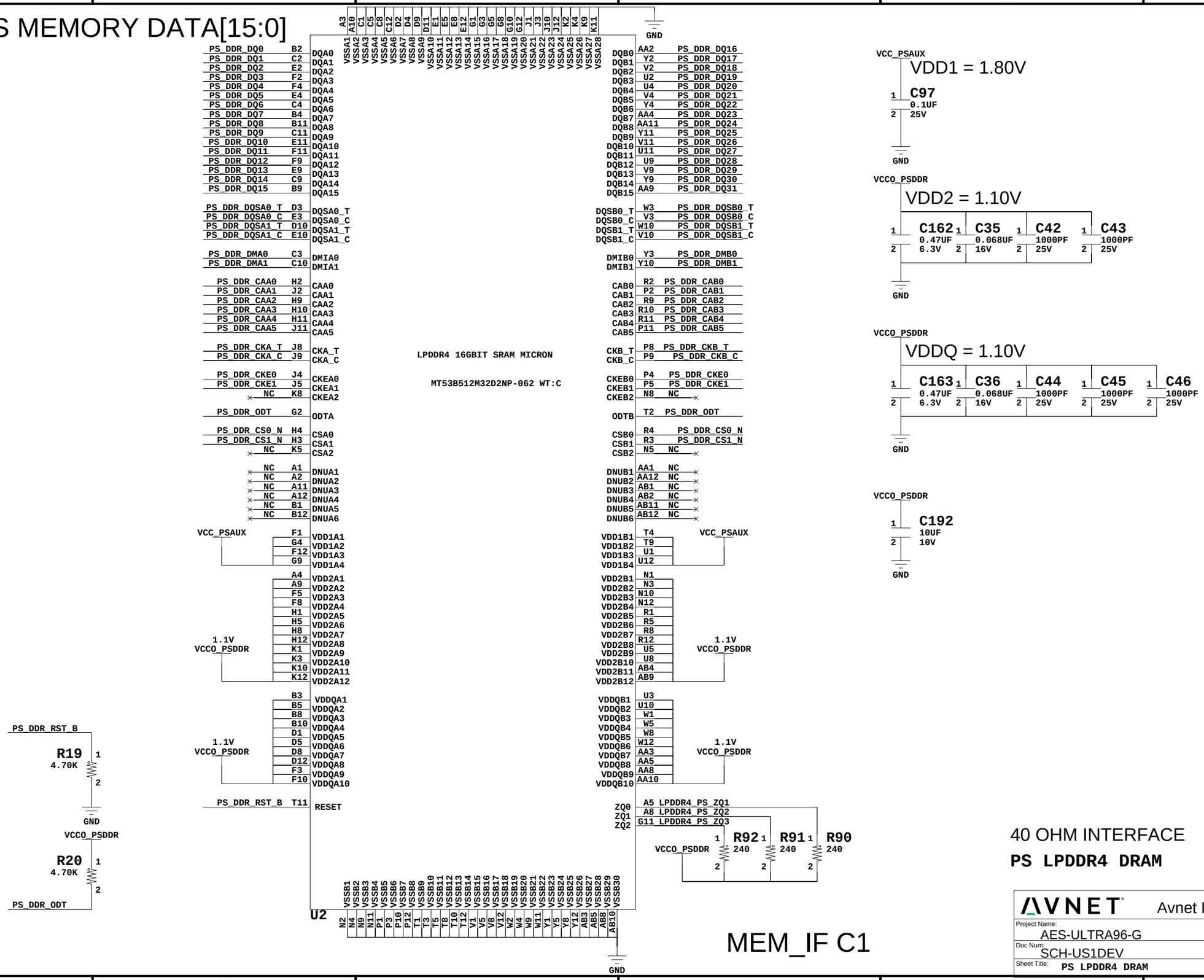
JTAG on Bottomside



JTAG Headers - LEDs

AVNET Avnet Design Services			
Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: JTAG Headers - LEDs	Size: B	Sheet: 14 of 27	

LPDDR4 PS MEMORY DATA[15:0]

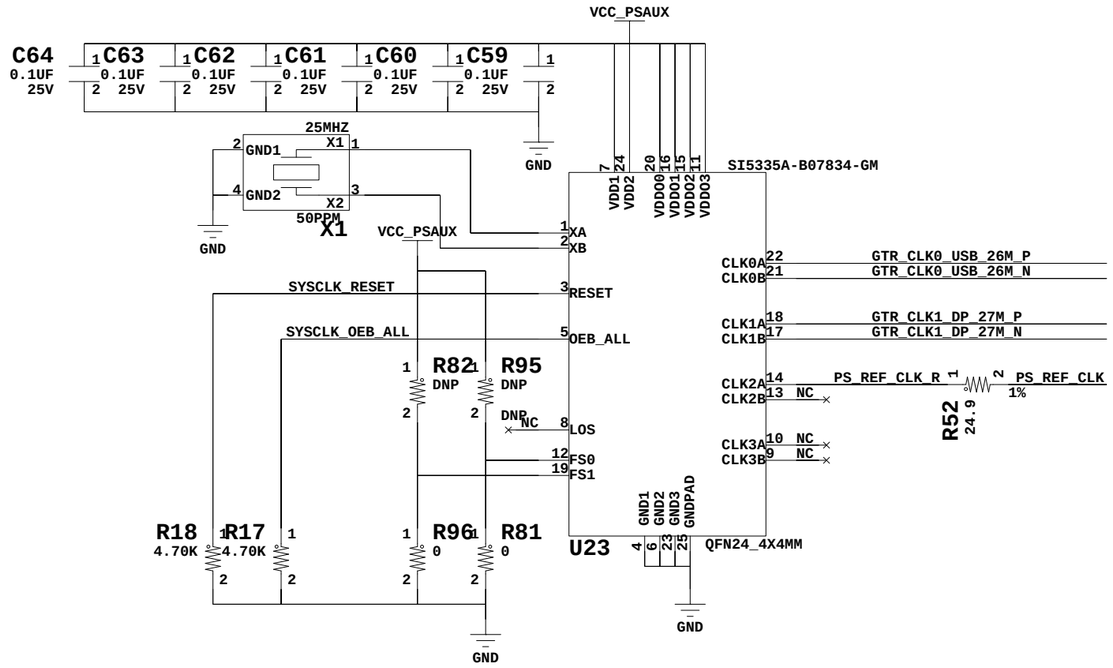


40 OHM INTERFACE

PS LPDDR4 DRAM

MEM_IF C1

AVNET Avnet Design Services			
Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: PS LPDDR4 DRAM	Size: B	Sheet: 15 of 27	



26MHz LVDS

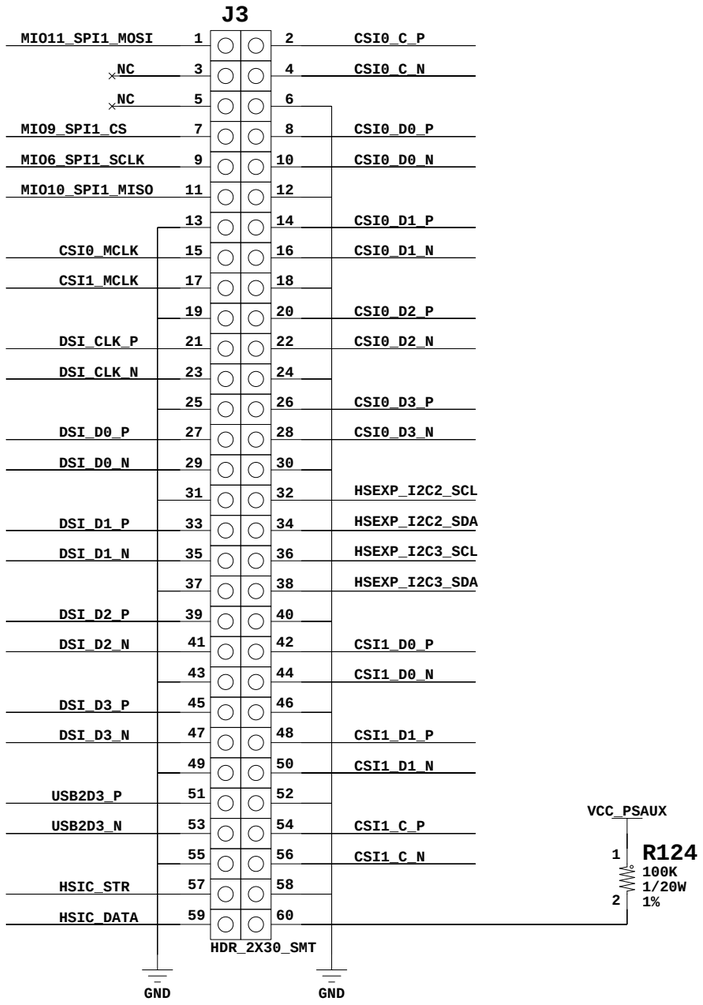
27MHz LVDS

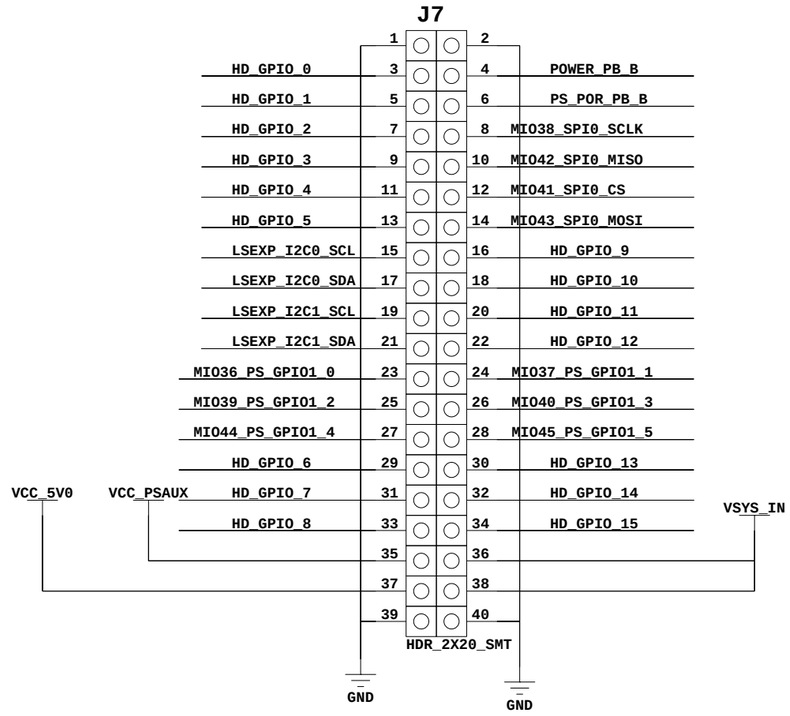
33.33333333MHz LVCMOS (10073)

Fixed Clocks

AVNET Avnet Design Services				
Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00	
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm		
Sheet Title: Fixed Clocks	Size: B	Sheet: 16 of 27		

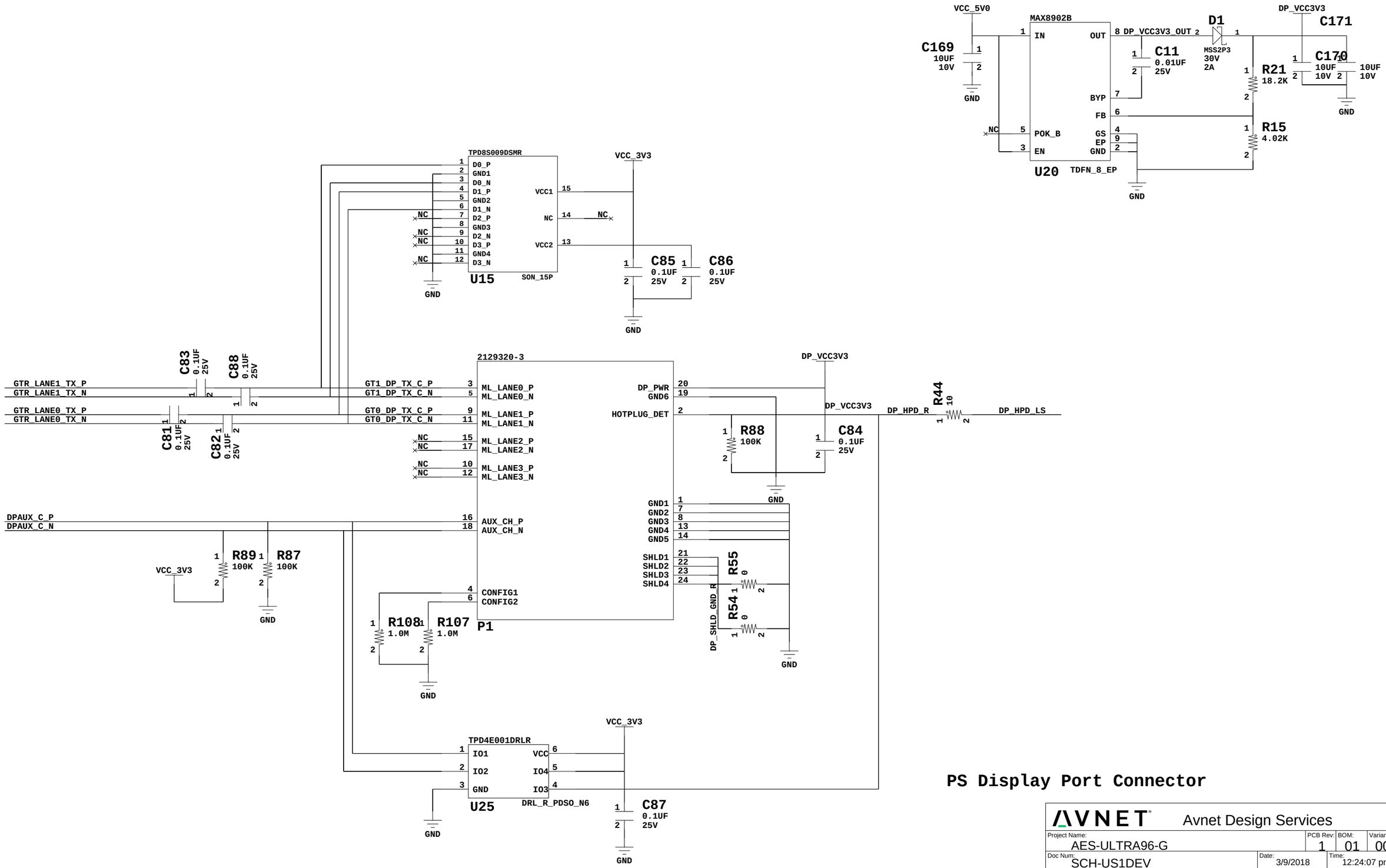
SPI shared with HS header
Different CS signals

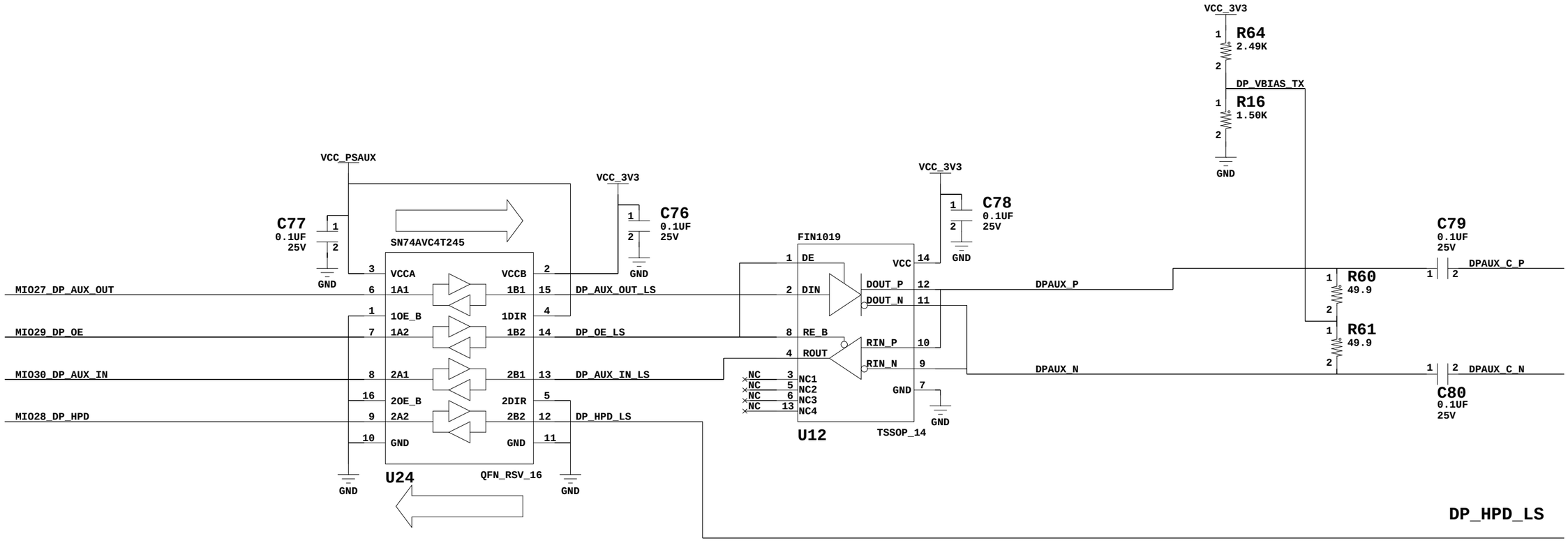




Expansion Headers

AVNET Avnet Design Services			
Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: Expansion Headers	Size: B	Sheet: 17 of 27	

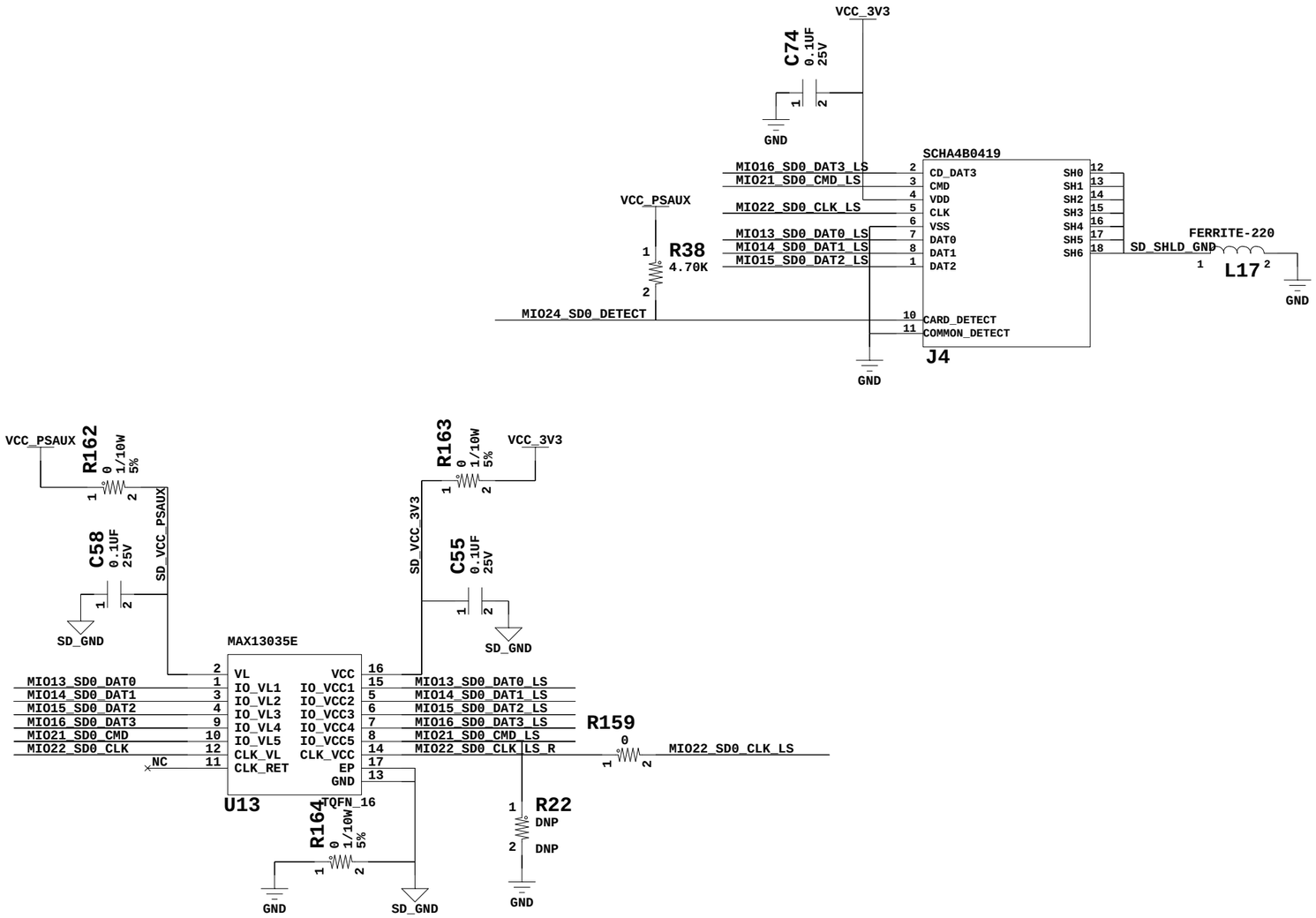

VCC_5V0
C169
10UF
10V
GND
MAX8902B
IN
OUT
BYP
FB
NC
POK_B
EN
GS
EP
GND
U20
TDFN_8_EP
DP_VCC3V3_OUT
D1
MSS2P3
30V
2A
C11
0.01UF
25V
DP_VCC3V3
C171
C170
10UF
10V
R21
18.2K
R15
4.02K
TPD8S009DSMR
D0_P
GND1
D0_N
D1_P
GND2
D1_N
D2_P
GND3
D2_N
D3_P
GND4
D3_N
VCC1
NC
VCC2
U15
SON_15P
VCC_3V3
C85
0.1UF
25V
C86
0.1UF
25V
C83
0.1UF
25V
C88
0.1UF
25V
C81
0.1UF
25V
C82
0.1UF
25V
GTR_LANE1_TX_P
GTR_LANE1_TX_N
GTR_LANE0_TX_P
GTR_LANE0_TX_N
2129320-3
GT1_DP_TX_C_P
GT1_DP_TX_C_N
GT0_DP_TX_C_P
GT0_DP_TX_C_N
ML_LANE0_P
ML_LANE0_N
ML_LANE1_P
ML_LANE1_N
ML_LANE2_P
ML_LANE2_N
ML_LANE3_P
ML_LANE3_N
AUX_CH_P
AUX_CH_N
CONFIG1
CONFIG2
DP_PWR
GND6
HOTPLUG_DET
GND1
GND2
GND3
GND4
GND5
SHLD1
SHLD2
SHLD3
SHLD4
P1
DP_VCC3V3
DP_VCC3V3
DP_HPD_R
DP_HPD_LS
R44
10
R88
100K
C84
0.1UF
25V
DPAUX_C_P
DPAUX_C_N
R89
100K
R87
100K
R108
1.0M
R107
1.0M
R55
0
R54
0
DP_SHLD_GND_R
TPD4E001DRLR
IO1
IO2
GND
VCC
IO4
IO3
U25
DRL_R_PDSO_N6
C87
0.1UF
25V
PS Display Port Connector
AVNET
Avnet Design Services
Project Name:
AES-ULTRA96-G
PCB Rev:
1
BOM:
01
Variant:
00
Doc Num:
SCH-US1DEV
Date:
3/9/2018
Time:
12:24:07 pm
Sheet Title:
PS Display Port Connector
Size:
B
Sheet:
18 of 27



DP_HPD_LS

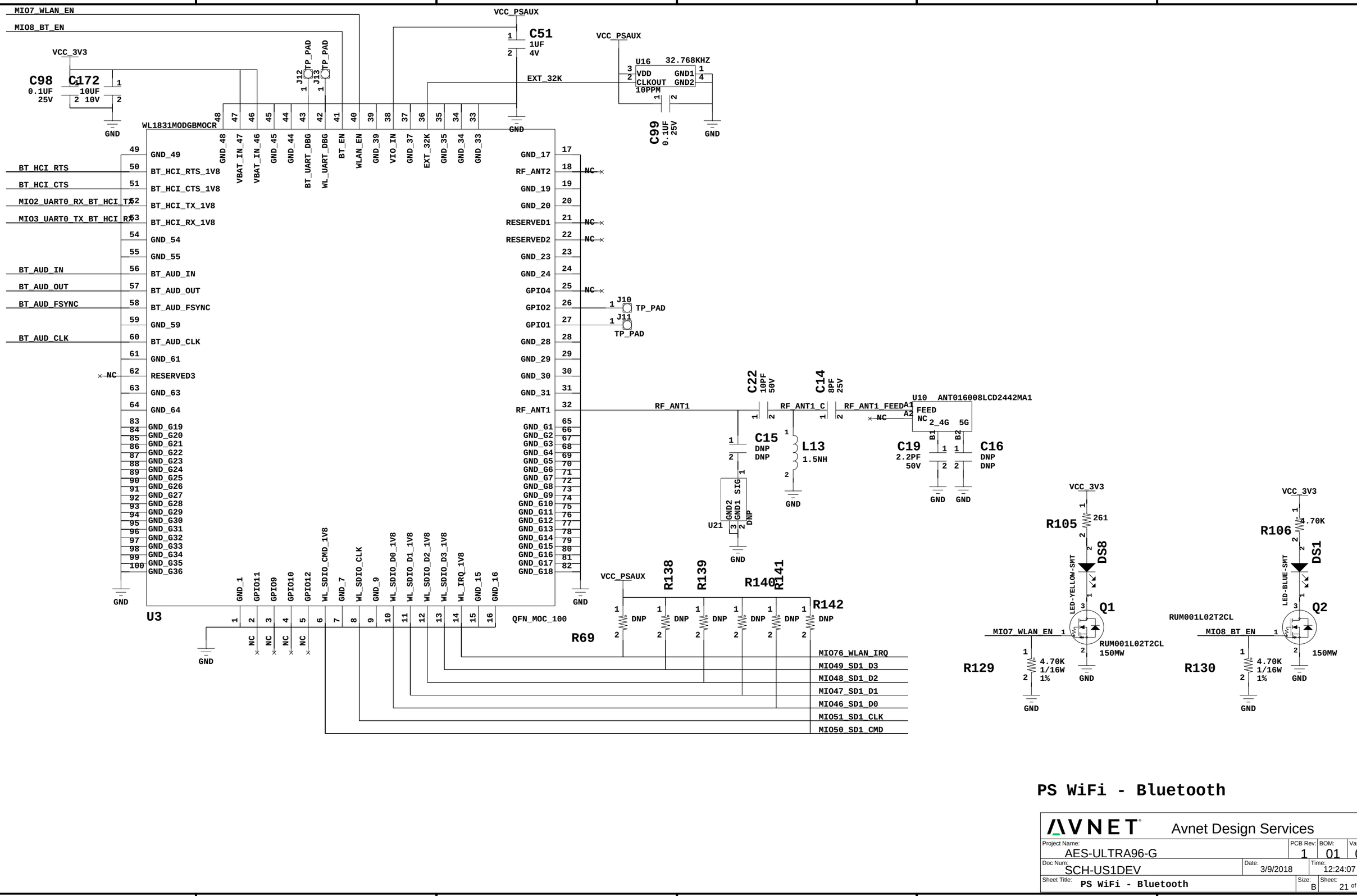
PS Display Port IO

Avnet Design Services			
Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: PS Display Port IO	Size: B	Sheet: 19 of 27	



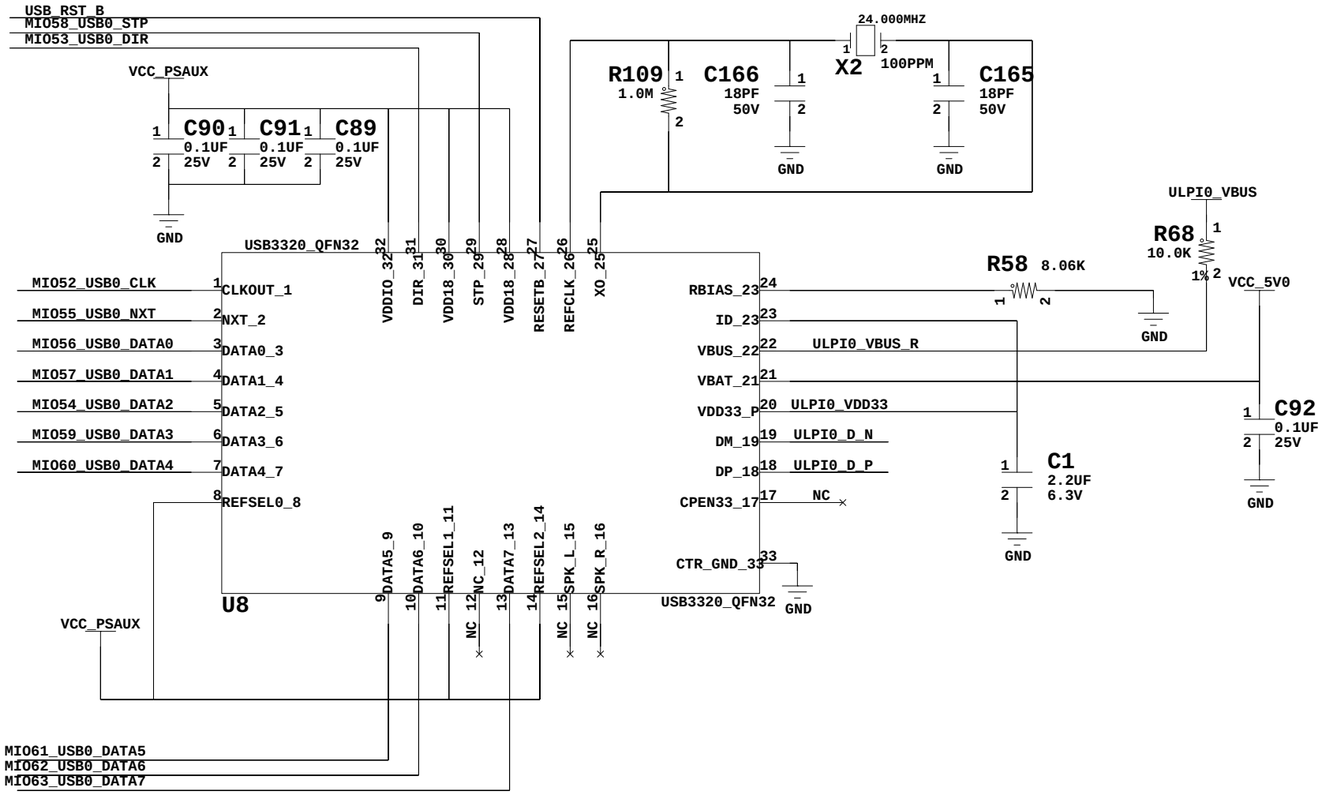
PS Micro SD Card

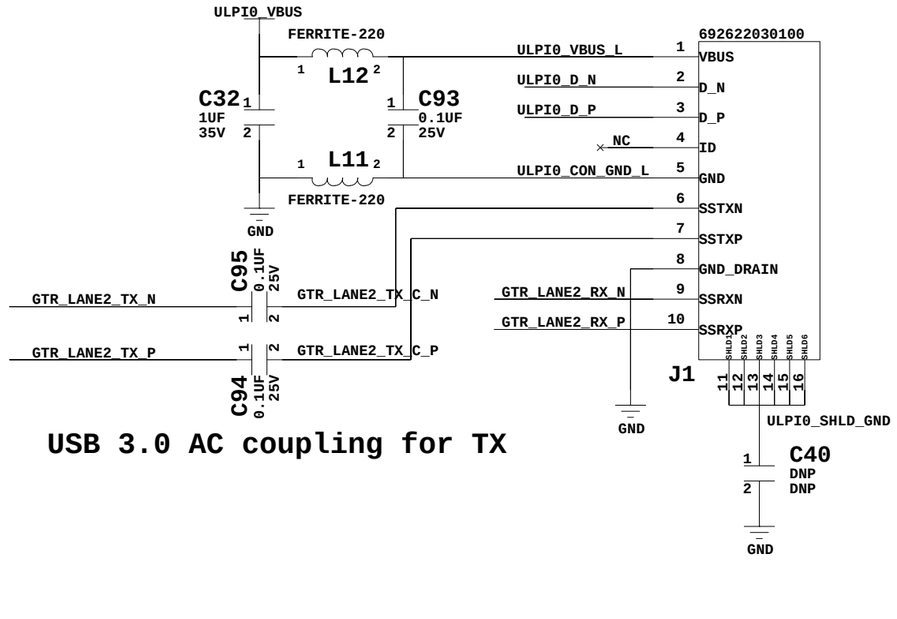
AVNET Avnet Design Services				
Project Name: AES-ULTRA96-G		PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm		
Sheet Title: PS Micro SD Card		Size: B	Sheet: 20 of 27	



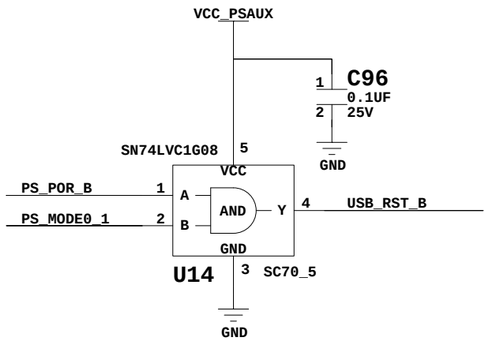
PS WiFi - Bluetooth

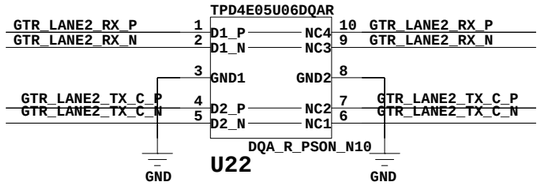
Avnet Design Services			
Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: PS WiFi - Bluetooth	Size: B	Sheet: 21 of 27	





USB 3.0 AC coupling for TX





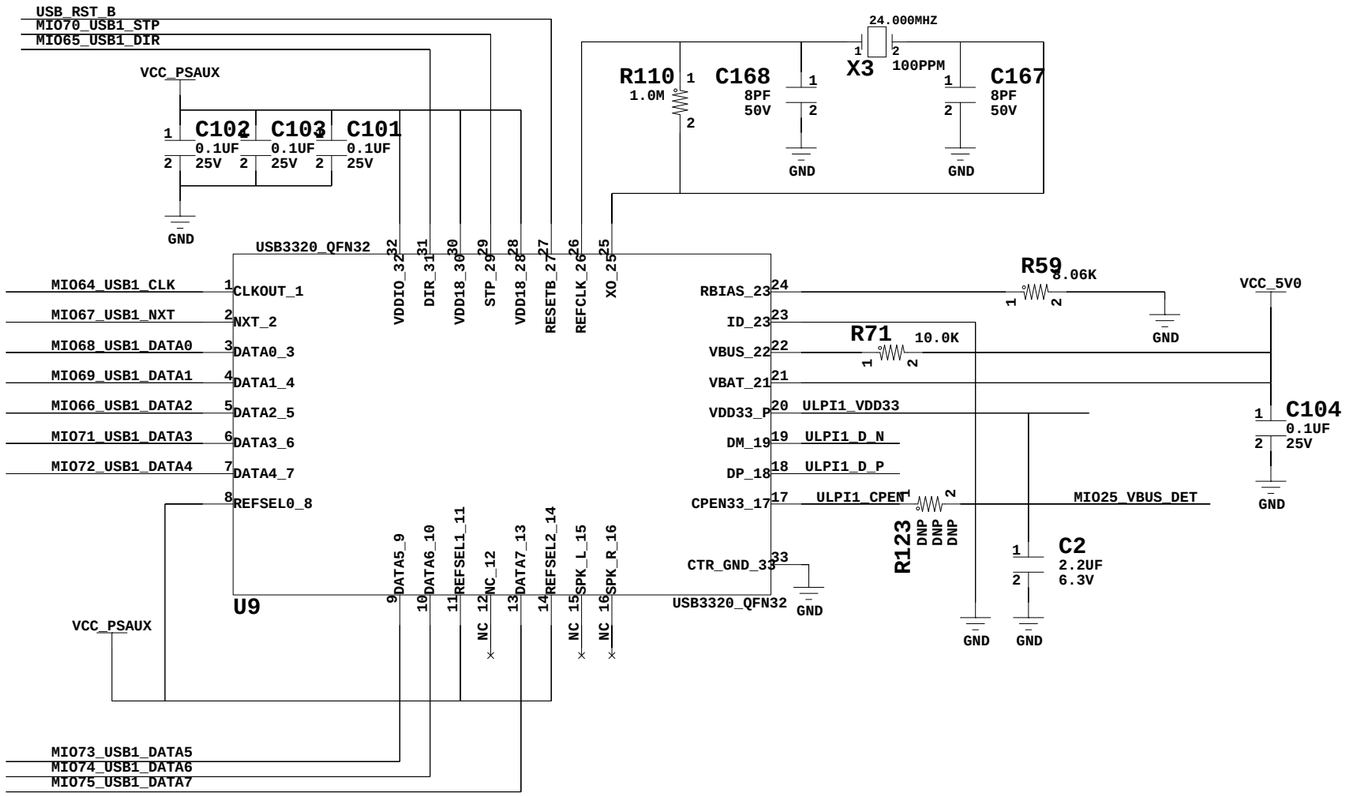
90 ohm impedance for USB 2.0 ULPI_D_P/N,

100 ohm for USB 3.0 USB_SSTX_P/N, USB_SSRX_P/N

Thick trace for ULPI_VBUS and related nets

PS USB 3_0 ULPI Upstream

AVNET Avnet Design Services			
Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: PS USB 3_0 ULPI Upstream	Size: B	Sheet: 22 of 27	



90 ohm impedance for USB 2.0 ULPI_D_P/N

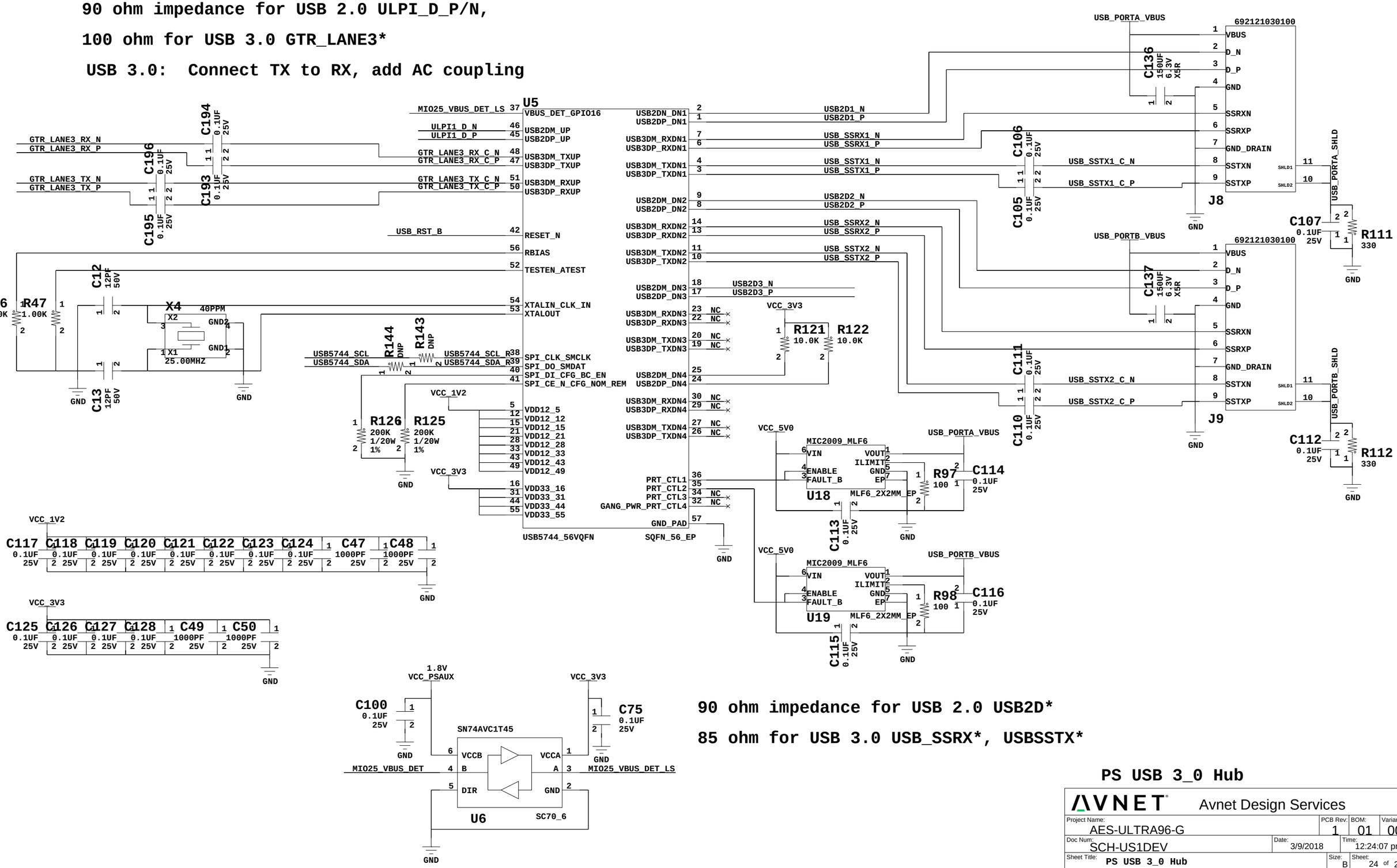
PS USB 3_0 ULPI Downstream

AVNET Avnet Design Services			
Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: PS USB 3_0 ULPI Downstream	Size: B	Sheet: 23 of 27	

90 ohm impedance for USB 2.0 ULPI_D_P/N,

100 ohm for USB 3.0 GTR_LANE3*

USB 3.0: Connect TX to RX, add AC coupling



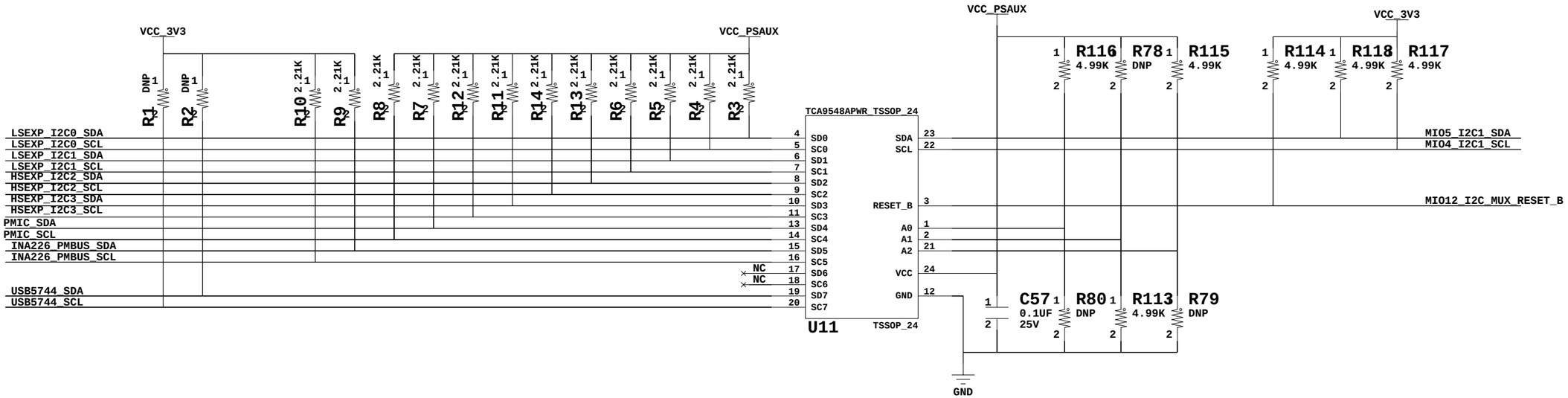
90 ohm impedance for USB 2.0 USB2D*

85 ohm for USB 3.0 USB_SSRX*, USBSSTX*

PS USB 3_0 Hub

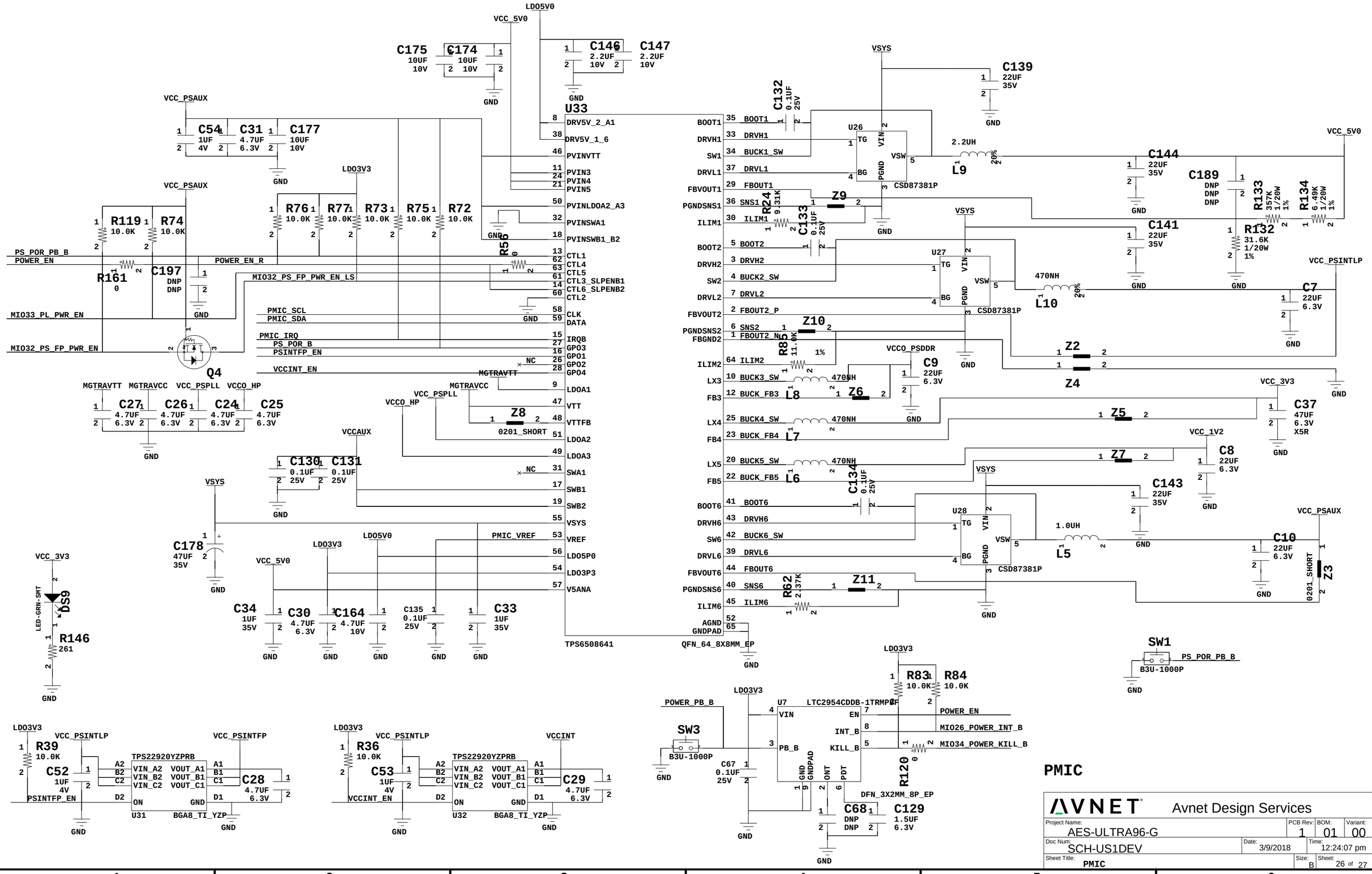
AVNET Avnet Design Services

Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: PS USB 3_0 Hub	Size: B	Sheet: 24 of 27	



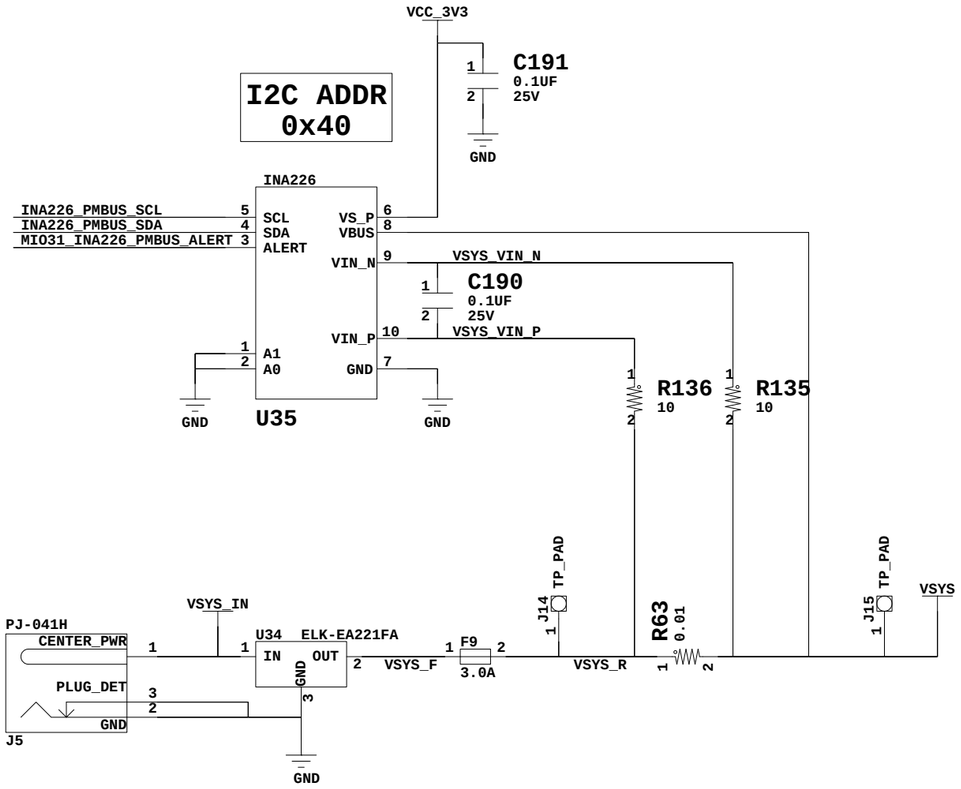
I2C MUX

Avnet Design Services			
Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: I2C MUX	Size: B	Sheet: 25 of 27	

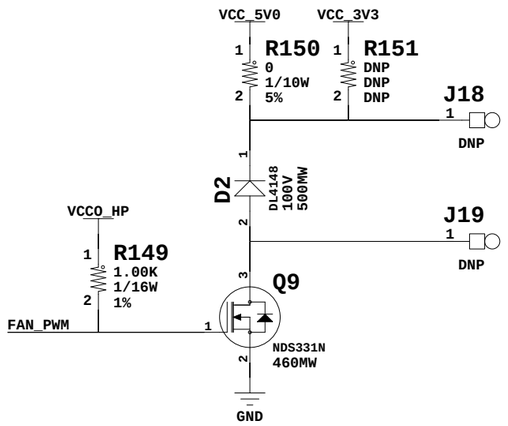


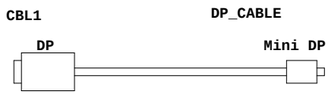
Project Name:	AES-ULTRA96-G
PCB Rev:	1
BOM:	01
Variant:	00
Doc Num:	SCH-US1DEV
Date:	3/9/2018
Time:	12:24:07 pm
Sheet Title:	PMIC
Size:	B
Sheet:	26 of 27

Avnet Design Services



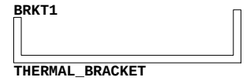
Fan wires, place near board edge

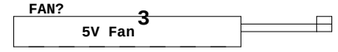


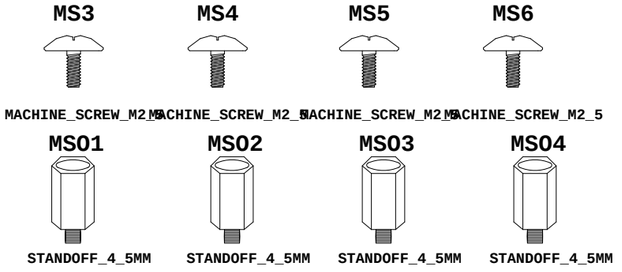


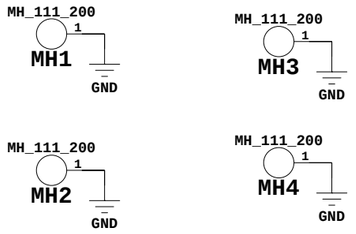
Display Port Cable

RAIL	VOLTAGE
VCC_PSINTFP	0.85V
VCC_PSINTLP	0.85V
VCC_PSPLL	1.20V
VCC_PSAUX	1.80V
VCC_PSDDR	1.10V
MGTRAVCC	0.90V
MGTRAVTT	1.80V
VCCINT	0.85V
VCCAUX	1.80V
VCCO_HP	1.20V
VCC_5V0	5.00V
VCC_3V3	3.30V
VCC_1V2	1.20V
LDO5V0	5.00V
LDO3V3	3.30V
USB_PORTA_VBUS	5.00V
USB_PORTB_VBUS	5.00V
DP_VCC3V3	3.30V









Power Connector - Mounting Holes

AVNET Avnet Design Services			
Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: Power Connector - Mounting Holes	Size: B	Sheet: 27 of 27	