

SYSMON I2C Address selection

Zynq Bank 0

<b>AVNET</b>		Avnet Design Services	
Project Name:	AES-ULTRA96-G	PCB Rev:	BOM: Variant:
Doc Num:	SCH-US1DEV	1	01 00
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XCZU3-SBVA484B

**BANK 26  
XCZU3SBVA484**

IO_L12N_AD0N_26_A6	A6	HD GPIO 6
IO_L12P_AD0P_26_B7	B7	BT HCI RTS
IO_L11N_AD1N_26_B5	B5	BT HCI CTS
IO_L11P_AD1P_26_B6	B6	HD GPIO 14
IO_L10N_AD2N_26_A7	A7	HD GPIO 7
IO_L10P_AD2P_26_A8	A8	BT AUD FSYNC
IO_L9N_AD3N_26_A9	A9	BT AUD IN
IO_L9P_AD3P_26_B9	B9	BT AUD OUT
IO_L8N_HDGC_AD4N_26_C7	C7	HD GPIO 13
IO_L8P_HDGC_AD4P_26_C8	C8	BT AUD CLK
IO_L7N_HDGC_AD5N_26_C5	C5	HD GPIO 15
IO_L7P_HDGC_AD5P_26_D5	D5	HD GPIO 12
IO_L6N_HDGC_AD6N_26_D8	D8	CST1 MCLK
IO_L6P_HDGC_AD6P_26_E8	E8	CST0 MCLK
IO_L5N_HDGC_AD7N_26_D6	D6	HD GPIO 11
IO_L5P_HDGC_AD7P_26_D7	D7	HD GPIO 0
IO_L4N_AD8N_26_F7	F7	HD GPIO 2
IO_L4P_AD8P_26_F8	F8	HD GPIO 1
IO_L3N_AD9N_26_E5	E5	HD GPIO 10
IO_L3P_AD9P_26_E6	E6	HD GPIO 9
IO_L2N_AD10N_26_F6	F6	HD GPIO 4
IO_L2P_AD10P_26_G7	G7	HD GPIO 3
IO_L1N_AD11N_26_G5	G5	HD GPIO 5
IO_L1P_AD11P_26_G6	G6	HD GPIO 8

VCCAUX

B8 VCCO\_26\_B8  
E7 VCCO\_26\_E7

U1

FBGA\_484\_0P8MM

**Zynq Banks 26 - HD**



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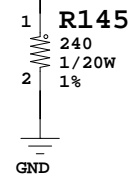
**BANK 65**  
**XCZU3SBVA484**

IO\_T3U\_N12\_65\_F4  
 IO\_L24N\_T3U\_N11\_PERSTN0\_65\_C2  
 IO\_L24P\_T3U\_N10\_PERSTN1\_I2C\_SDA\_65\_D2  
 IO\_L23N\_T3U\_N9\_65\_F2  
 IO\_L23P\_T3U\_N8\_I2C\_SCLK\_65\_F3  
 IO\_L22N\_T3U\_N7\_DBC\_AD0N\_65\_C3  
 IO\_L22P\_T3U\_N6\_DBC\_AD0P\_65\_D3  
 IO\_L21N\_T3L\_N5\_AD8N\_65\_D1  
 IO\_L21P\_T3L\_N4\_AD8P\_65\_E1  
 IO\_L20N\_T3L\_N3\_AD1N\_65\_E3  
 IO\_L20P\_T3L\_N2\_AD1P\_65\_E4  
 IO\_L19N\_T3L\_N1\_DBC\_AD9N\_65\_F1  
 IO\_L19P\_T3L\_N0\_DBC\_AD9P\_65\_G1  
 IO\_T2U\_N12\_65\_H3  
 IO\_L18N\_T2U\_N11\_AD2N\_65\_G4  
 IO\_L18P\_T2U\_N10\_AD2P\_65\_H4  
 IO\_L17N\_T2U\_N9\_AD10N\_65\_G2  
 IO\_L17P\_T2U\_N8\_AD10P\_65\_H2  
 IO\_L16N\_T2U\_N7\_QBC\_AD3N\_65\_H5  
 IO\_L16P\_T2U\_N6\_QBC\_AD3P\_65\_J5  
 IO\_L15N\_T2L\_N5\_AD11N\_65\_J1  
 IO\_L15P\_T2L\_N4\_AD11P\_65\_K1  
 IO\_L14N\_T2L\_N3\_GC\_65\_K3  
 IO\_L14P\_T2L\_N2\_GC\_65\_K4  
 IO\_L13N\_T2L\_N1\_GC\_QBC\_65\_J2  
 IO\_L13P\_T2L\_N0\_GC\_QBC\_65\_J3  
 IO\_T1U\_N12\_65\_N3  
 IO\_L12N\_T1U\_N11\_GC\_65\_L3  
 IO\_L12P\_T1U\_N10\_GC\_65\_L4  
 IO\_L11N\_T1U\_N9\_GC\_65\_L1  
 IO\_L11P\_T1U\_N8\_GC\_65\_L2  
 IO\_L10N\_T1U\_N7\_QBC\_AD4N\_65\_M4  
 IO\_L10P\_T1U\_N6\_QBC\_AD4P\_65\_M5  
 IO\_L9N\_T1L\_N5\_AD12N\_65\_M1  
 IO\_L9P\_T1L\_N4\_AD12P\_65\_M2  
 IO\_L8N\_T1L\_N3\_AD5N\_65\_N4  
 IO\_L8P\_T1L\_N2\_AD5P\_65\_N5  
 IO\_L7N\_T1L\_N1\_QBC\_AD13N\_65\_P1  
 IO\_L7P\_T1L\_N0\_QBC\_AD13P\_65\_N2  
 IO\_T0U\_N12\_VRP\_65\_P2  
 IO\_L6N\_T0U\_N11\_AD6N\_65\_R5  
 IO\_L6P\_T0U\_N10\_AD6P\_65\_P5  
 IO\_L5N\_T0U\_N9\_AD14N\_65\_T1  
 IO\_L5P\_T0U\_N8\_AD14P\_65\_R1  
 IO\_L4N\_T0U\_N7\_DBC\_AD7N\_65\_T4  
 IO\_L4P\_T0U\_N6\_DBC\_AD7P\_SMBALERT\_65\_R4  
 IO\_L3N\_T0L\_N5\_AD15N\_65\_U1  
 IO\_L3P\_T0L\_N4\_AD15P\_65\_U2  
 IO\_L2N\_T0L\_N3\_65\_R3  
 IO\_L2P\_T0L\_N2\_65\_P3  
 IO\_L1N\_T0L\_N1\_DBC\_65\_T2  
 IO\_L1P\_T0L\_N0\_DBC\_65\_T3  
 VREF\_65\_K5

F4 FAN\_PWM  
 C2 HSIC\_DATA  
 D2 NC x  
 F2 NC x  
 F3 NC x  
 C3 DSI\_D3\_N  
 D3 DSI\_D3\_P  
 D1 DSI\_D2\_N  
 E1 DSI\_D2\_P  
 E3 DSI\_D1\_N  
 E4 DSI\_D1\_P  
 F1 DSI\_D0\_N  
 G1 DSI\_D0\_P  
 H3 NC x  
 G4 NC x  
 H4 NC x  
 G2 NC x  
 H2 NC x  
 H5 DSI\_CLK\_N  
 J5 DSI\_CLK\_P  
 J1 NC x  
 K1 NC x  
 K3 NC x  
 K4 NC x  
 J2 NC x  
 J3 NC x  
 N3 NC x  
 L3 NC x  
 L4 NC x  
 L1 CSIO\_D3\_N  
 L2 CSIO\_D3\_P  
 M4 CSIO\_D2\_N  
 M5 CSIO\_D2\_P  
 M1 CSIO\_D1\_N  
 M2 CSIO\_D1\_P  
 N4 CSIO\_D0\_N  
 N5 CSIO\_D0\_P  
 P1 CSIO\_C\_N  
 N2 CSIO\_C\_P  
 P2 NC x  
 R5 NC x  
 P5 NC x  
 T1 NC x  
 R1 NC x  
 T4 NC x  
 R4 NC x  
 U1 CSI1\_D1\_N  
 U2 CSI1\_D1\_P  
 R3 CSI1\_D0\_N  
 P3 CSI1\_D0\_P  
 T2 CSI1\_C\_N  
 T3 CSI1\_C\_P  
 K5 NC x

VCCO\_HP  
 B3 VCCO\_65\_B3  
 G3 VCCO\_65\_G3  
 K2 VCCO\_65\_K2  
 P4 VCCO\_65\_P4

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XCZU3-SBVA484B

**BANK 66**  
**XCZU3SBVA484**

IO\_T3U\_N12\_66\_A2  
 IO\_L12N\_T1U\_N11\_GC\_66\_A3  
 IO\_L12P\_T1U\_N10\_GC\_66\_A4  
 IO\_L11N\_T1U\_N9\_GC\_66\_B1  
 IO\_L11P\_T1U\_N8\_GC\_66\_B2  
 IO\_T0U\_N12\_VRP\_66\_B4  
 VREF\_66\_C4

A2 HSIC\_STR  
 A3 NC x  
 A4 NC x  
 B1 NC x  
 B2 NC x  
 B4 NC x  
 C4 NC x

U1 FBGA\_484\_0P8MM

**Zynq Banks 65 66 - HP**

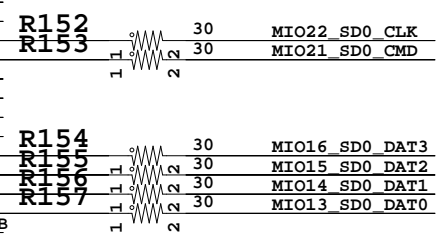
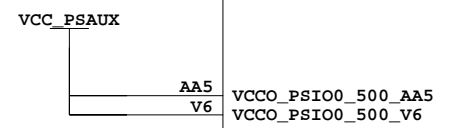
**AVNET** Avnet Design Services

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**BANK 500**  
**XCZU3SBVA484**

PS_MIO25_Y6	Y6	MIO25 VBUS DET
PS_MIO24_AB6	AB6	MIO24 SD0 DETECT
PS_MIO23_AB5	AB5	MIO23 GPIO PB
PS_MIO22_AA6	AA6	MIO22 SD0 CLK R
PS_MIO21_W6	W6	MIO21 SD0 CMD R
PS_MIO20_AB4	AB4	MIO20 PS LED0
PS_MIO19_AA4	AA4	MIO19 PS LED1
PS_MIO18_Y5	Y5	MIO18 PS LED2
PS_MIO17_AA3	AA3	MIO17 PS LED3
PS_MIO16_Y3	Y3	MIO16 SD0 DAT3 R
PS_MIO15_Y4	Y4	MIO15 SD0 DAT2 R
PS_MIO14_W5	W5	MIO14 SD0 DAT1 R
PS_MIO13_W3	W3	MIO13 SD0 DAT0 R
PS_MIO12_AB2	AB2	MIO12 I2C MUX RESET B
PS_MIO11_W2	W2	MIO11 SPI1 MOSI
PS_MIO10_AA2	AA2	MIO10 SPI1 MISO
PS_MIO9_V5	V5	MIO9 SPI1 CS
PS_MIO8_V3	V3	MIO8 BT EN
PS_MIO7_V4	V4	MIO7 WLAN EN
PS_MIO6_Y1	Y1	MIO6 SPI1 SCLK
PS_MIO5_AA1	AA1	MIO5 I2C1 SDA
PS_MIO4_U6	U6	MIO4 I2C1 SCL
PS_MIO3_U5	U5	MIO3 UART0 TX BT HCI_RX
PS_MIO2_V2	V2	MIO2 UART0 RX BT HCI_TX
PS_MIO1_W1	W1	MIO1 UART1_RX
PS_MIO0_U4	U4	MIO0 UART1_TX

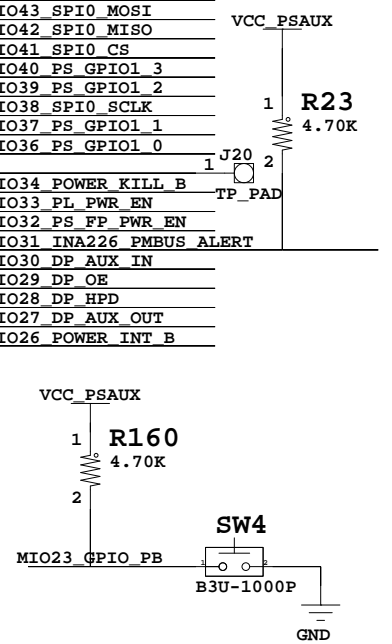
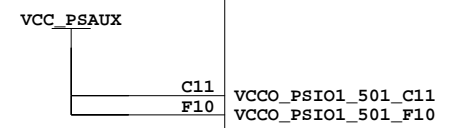


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XCZU3-SBVA484B

**BANK 501**  
**XCZU3SBVA484**

PS_MIO51_C13	C13	MIO51 SD1_CLK
PS_MIO50_A13	A13	MIO50 SD1_CMD
PS_MIO49_D13	D13	MIO49 SD1_D3
PS_MIO48_A12	A12	MIO48 SD1_D2
PS_MIO47_B12	B12	MIO47 SD1_D1
PS_MIO46_C12	C12	MIO46 SD1_D0
PS_MIO45_A11	A11	MIO45 PS GPIO1_5
PS_MIO44_B11	B11	MIO44 PS GPIO1_4
PS_MIO43_E13	E13	MIO43 SPI0 MOSI
PS_MIO42_D12	D12	MIO42 SPI0 MISO
PS_MIO41_B10	B10	MIO41 SPI0 CS
PS_MIO40_D11	D11	MIO40 PS GPIO1_3
PS_MIO39_C10	C10	MIO39 PS GPIO1_2
PS_MIO38_C9	C9	MIO38 SPI0 SCLK
PS_MIO37_E11	E11	MIO37 PS GPIO1_1
PS_MIO36_D10	D10	MIO36 PS GPIO1_0
PS_MIO35_E10	E10	MIO35 E10
PS_MIO34_F13	F13	MIO34 POWER KILL B
PS_MIO33_E9	E9	MIO33 PL PWR EN
PS_MIO32_F12	F12	MIO32 PS FP PWR EN
PS_MIO31_F11	F11	MIO31 INA226 PMBUS ALERT
PS_MIO30_G10	G10	MIO30 DP AUX_IN
PS_MIO29_F9	F9	MIO29 DP OE
PS_MIO28_G12	G12	MIO28 DP HPD
PS_MIO27_G11	G11	MIO27 DP AUX_OUT
PS_MIO26_G9	G9	MIO26 POWER INT_B

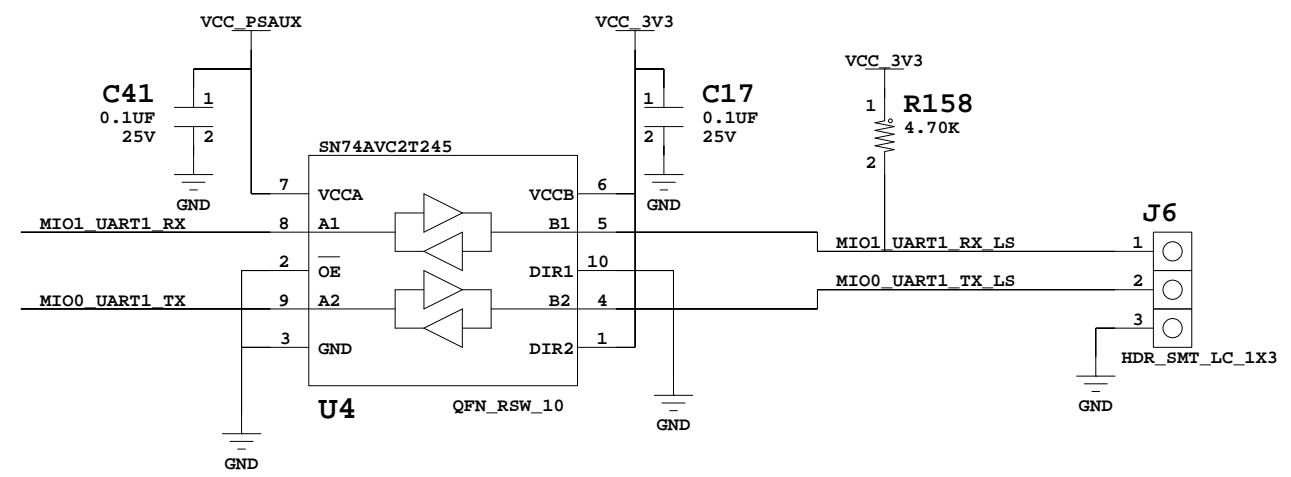
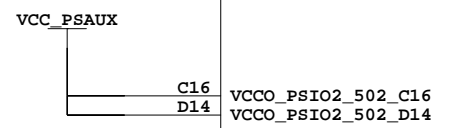


U1 FBGA\_484\_0P8MM

XCZU3-SBVA484B

**BANK 502**  
**XCZU3SBVA484**

PS_MIO77_B18	B18	PMIC IRQ
PS_MIO76_F18	F18	MIO76 WLAN_IRQ
PS_MIO75_B17	B17	MIO75 USB1_DATA7
PS_MIO74_D18	D18	MIO74 USB1_DATA6
PS_MIO73_D17	D17	MIO73 USB1_DATA5
PS_MIO72_C17	C17	MIO72 USB1_DATA4
PS_MIO71_F17	F17	MIO71 USB1_DATA3
PS_MIO70_A17	A17	MIO70 USB1_STP
PS_MIO69_A16	A16	MIO69 USB1_DATA1
PS_MIO68_B16	B16	MIO68 USB1_DATA0
PS_MIO67_G17	G17	MIO67 USB1_NXT
PS_MIO66_D16	D16	MIO66 USB1_DATA2
PS_MIO65_B15	B15	MIO65 USB1_DIR
PS_MIO64_E16	E16	MIO64 USB1_CLK
PS_MIO63_F16	F16	MIO63 USB0_DATA7
PS_MIO62_C15	C15	MIO62 USB0_DATA6
PS_MIO61_G16	G16	MIO61 USB0_DATA5
PS_MIO60_D15	D15	MIO60 USB0_DATA4
PS_MIO59_E15	E15	MIO59 USB0_DATA3
PS_MIO58_A14	A14	MIO58 USB0_STP
PS_MIO57_B14	B14	MIO57 USB0_DATA1
PS_MIO56_E14	E14	MIO56 USB0_DATA0
PS_MIO55_C14	C14	MIO55 USB0_NXT
PS_MIO54_G15	G15	MIO54 USB0_DATA2
PS_MIO53_F14	F14	MIO53 USB0_DIR
PS_MIO52_G14	G14	MIO52 USB0_CLK

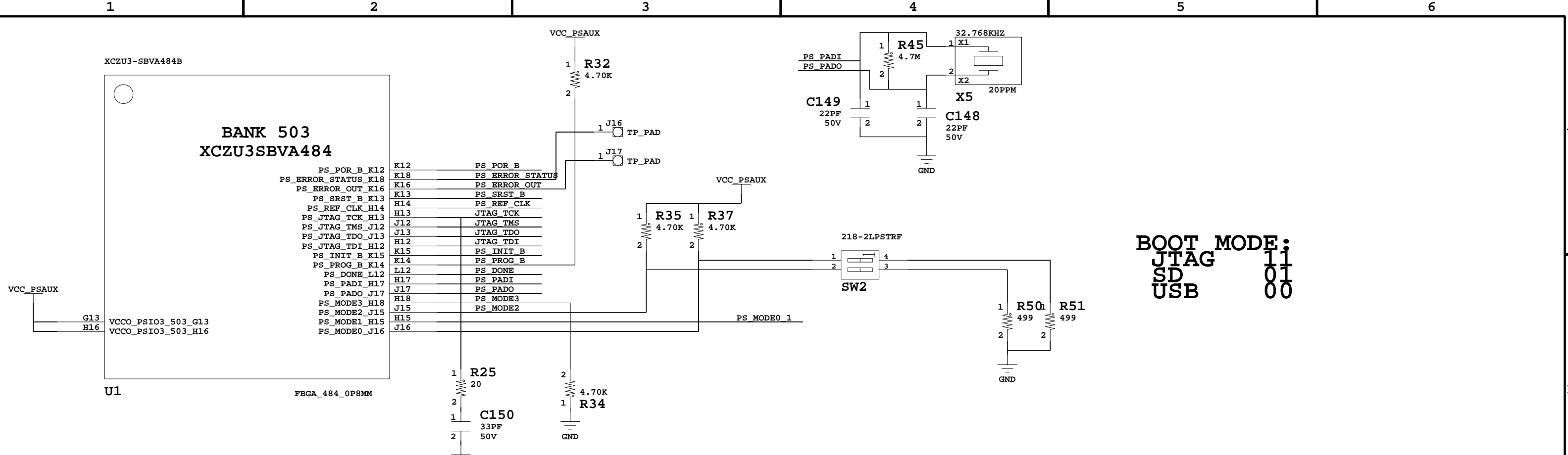


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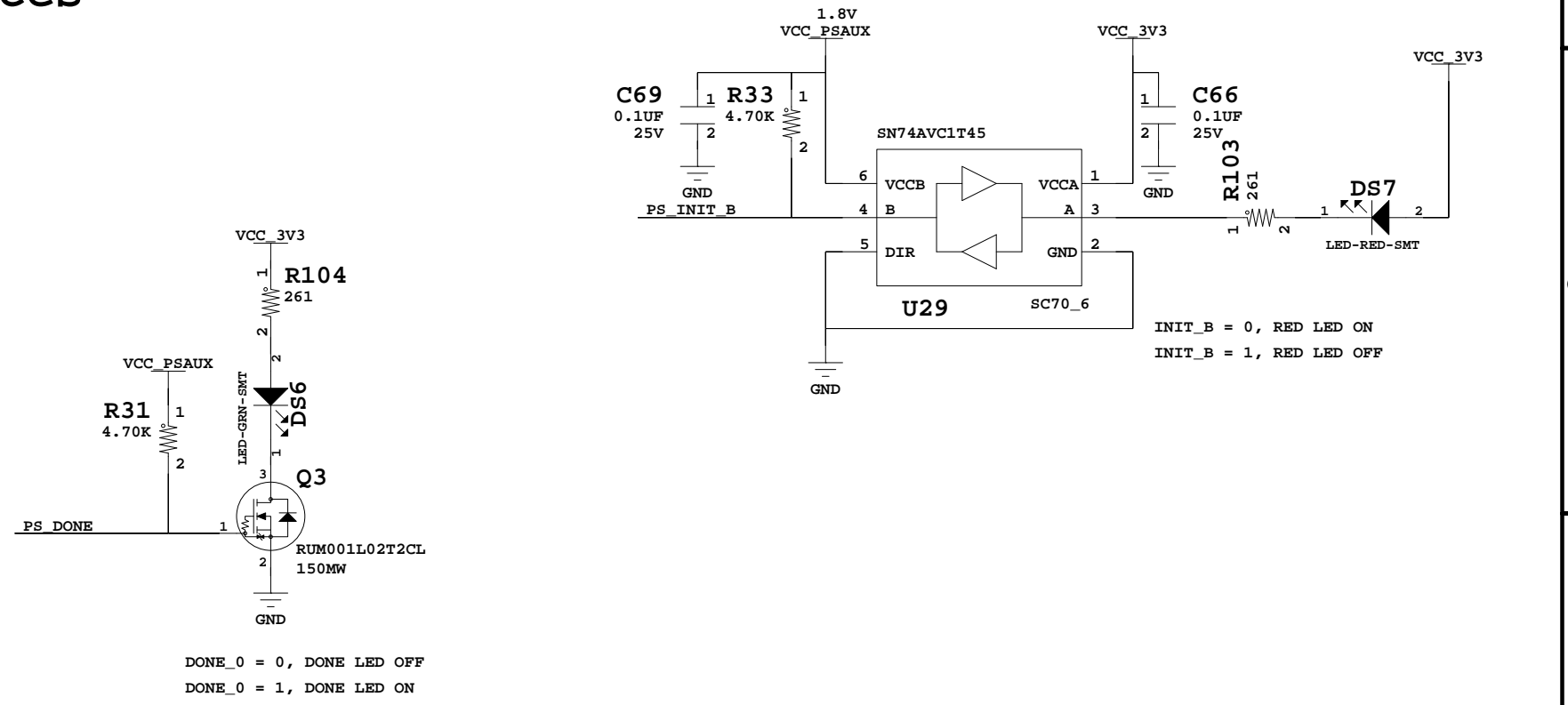
**Zynq Banks 500 501 502 - MIO**

**AVNET** Avnet Design Services

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PS\_MODE0\_1 is used to reset USB devices



Zynq Banks 503 - Config

XCZU3-SBVA484B

### BANK 504 XCZU3SBVA484

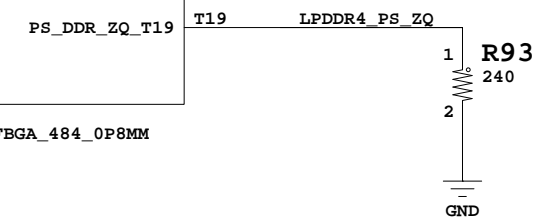
PS_DDR_CAA0	AA22	PS_DDR_A0_AA22	PS_DDR_DQ0_AB11	AB11	PS_DDR_DQ0
PS_DDR_CAA1	AB20	PS_DDR_A1_AB20	PS_DDR_DQ1_Y10	Y10	PS_DDR_DQ1
PS_DDR_CAA2	AB17	PS_DDR_A2_AB17	PS_DDR_DQ2_AB10	AB10	PS_DDR_DQ2
PS_DDR_CAA3	AB19	PS_DDR_A3_AB19	PS_DDR_DQ3_W10	W10	PS_DDR_DQ3
PS_DDR_CAA4	AB21	PS_DDR_A4_AB21	PS_DDR_DQ4_AA8	AA8	PS_DDR_DQ4
PS_DDR_CAA5	AB16	PS_DDR_A5_AB16	PS_DDR_DQ5_Y8	Y8	PS_DDR_DQ5
	NC	Y20	PS_DDR_DQ6_AB7	AB7	PS_DDR_DQ6
	NC	Y19	PS_DDR_DQ7_AA7	AA7	PS_DDR_DQ7
	NC	W17	PS_DDR_DQ8_AA11	AA11	PS_DDR_DQ8
	NC	Y18	PS_DDR_DQ9_Y11	Y11	PS_DDR_DQ9
PS_DDR_CAB0	Y21	PS_DDR_A10_Y21	PS_DDR_DQ10_AA12	AA12	PS_DDR_DQ10
PS_DDR_CAB1	AA21	PS_DDR_A11_AA21	PS_DDR_DQ11_AB12	AB12	PS_DDR_DQ11
PS_DDR_CAB2	AA18	PS_DDR_A12_AA18	PS_DDR_DQ12_Y14	Y14	PS_DDR_DQ12
PS_DDR_CAB3	AA19	PS_DDR_A13_AA19	PS_DDR_DQ13_AA14	AA14	PS_DDR_DQ13
PS_DDR_CAB4	AA17	PS_DDR_A14_AA17	PS_DDR_DQ14_Y15	Y15	PS_DDR_DQ14
PS_DDR_CAB5	AA16	PS_DDR_A15_AA16	PS_DDR_DQ15_AB15	AB15	PS_DDR_DQ15
	NC	Y16	PS_DDR_DQ16_W8	W8	PS_DDR_DQ16
	NC	W16	PS_DDR_DQ17_W7	W7	PS_DDR_DQ17
	NC	U17	PS_DDR_DQ18_V7	V7	PS_DDR_DQ18
	NC	V17	PS_DDR_DQ19_V10	V10	PS_DDR_DQ19
	NC	U15	PS_DDR_DQ20_U7	U7	PS_DDR_DQ20
	NC	T21	PS_DDR_DQ21_T9	T9	PS_DDR_DQ21
	NC	U19	PS_DDR_DQ22_U10	U10	PS_DDR_DQ22
PS_DDR_RST_B	T18	PS_DDR_RAM_RST_N_T18	PS_DDR_DQ23_T10	T10	PS_DDR_DQ23
	NC	U16	PS_DDR_DQ24_U11	U11	PS_DDR_DQ24
	NC	W18	PS_DDR_DQ25_U12	U12	PS_DDR_DQ25
PS_DDR_CS0_N	V22	PS_DDR_CS_N0_V22	PS_DDR_DQ26_W12	W12	PS_DDR_DQ26
PS_DDR_CS1_N	U20	PS_DDR_CS_N1_U20	PS_DDR_DQ27_W11	W11	PS_DDR_DQ27
PS_DDR_CKA_T	V20	PS_DDR_CK0_V20	PS_DDR_DQ28_V14	V14	PS_DDR_DQ28
PS_DDR_CKA_C	W20	PS_DDR_CK_N0_W20	PS_DDR_DQ29_U14	U14	PS_DDR_DQ29
PS_DDR_CKB_T	V18	PS_DDR_CK1_V18	PS_DDR_DQ30_W15	W15	PS_DDR_DQ30
PS_DDR_CKB_C	V19	PS_DDR_CK_N1_V19	PS_DDR_DQ31_V15	V15	PS_DDR_DQ31
PS_DDR_CKE0	U22	PS_DDR_CKE0_U22			
PS_DDR_CKE1	U21	PS_DDR_CKE1_U21			
	NC	W22	PS_DDR_DQ64_T22	T22	NC
	NC	W21	PS_DDR_DQ65_P22	P22	NC
	NC	W21	PS_DDR_DQ66_R21	R21	NC
PS_DDR_DQSA0_T	Y9	PS_DDR_DQS_P0_Y9	PS_DDR_DQ67_P21	P21	NC
PS_DDR_DQSA0_C	AA9	PS_DDR_DQS_N0_AA9	PS_DDR_DQ68_R18	R18	NC
PS_DDR_DQSA1_T	Y13	PS_DDR_DQS_P1_Y13	PS_DDR_DQ69_P18	P18	NC
PS_DDR_DQSA1_C	AA13	PS_DDR_DQS_N1_AA13	PS_DDR_DQ70_N18	N18	NC
PS_DDR_DQSB0_T	V9	PS_DDR_DQS_P2_V9	PS_DDR_DQ71_N19	N19	NC
PS_DDR_DQSB0_C	V8	PS_DDR_DQS_N2_V8			
PS_DDR_DQSB1_T	V12	PS_DDR_DQS_P3_V12			
PS_DDR_DQSB1_C	V13	PS_DDR_DQS_N3_V13			
	NC	P20	PS_DDR_DM0_AB9	AB9	PS_DDR_DMA0
	NC	R20	PS_DDR_DM1_AB14	AB14	PS_DDR_DMA1
	NC	R20	PS_DDR_DM2_U9	U9	PS_DDR_DMB0
	NC	R20	PS_DDR_DM3_W13	W13	PS_DDR_DMB1
	NC	R20	PS_DDR_DM8_R19	R19	NC

VCCO\_PSDDR

Y22	VCCO_PSDDR_504_Y22
Y17	VCCO_PSDDR_504_Y17
V21	VCCO_PSDDR_504_V21
V16	VCCO_PSDDR_504_V16
T20	VCCO_PSDDR_504_T20
P19	VCCO_PSDDR_504_P19
AB18	VCCO_PSDDR_504_AB18

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FBGA\_484\_0P8MM



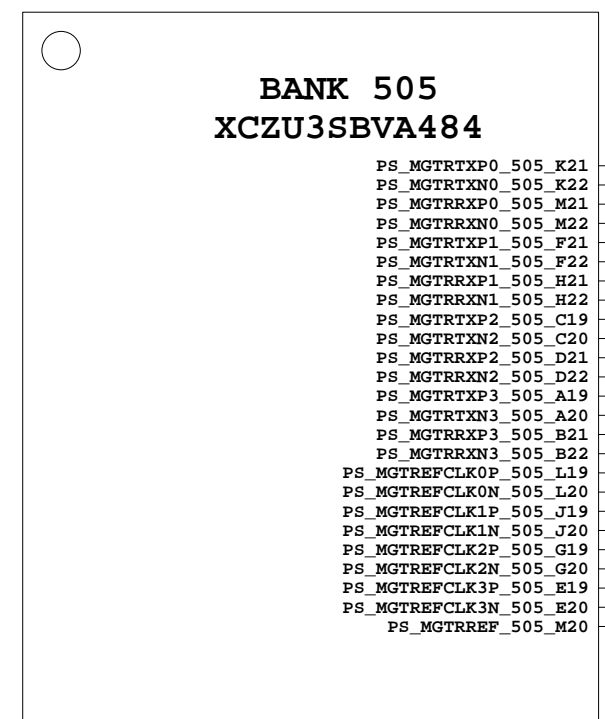
### Zynq Bank 504 - Memory

**AVNET** Avnet Design Services

Project Name:	AES-ULTRA96-G	PCB Rev:	BOM:	Variant:
Doc Num:	SCH-US1DEV	1	01	00
Date:	3/9/2018	Time:	12:24:07 pm	
Sheet Title:	Zynq Bank 504 - Memory	Size:	B	Sheet: 8 of 27



XCZU3-SBVA484B

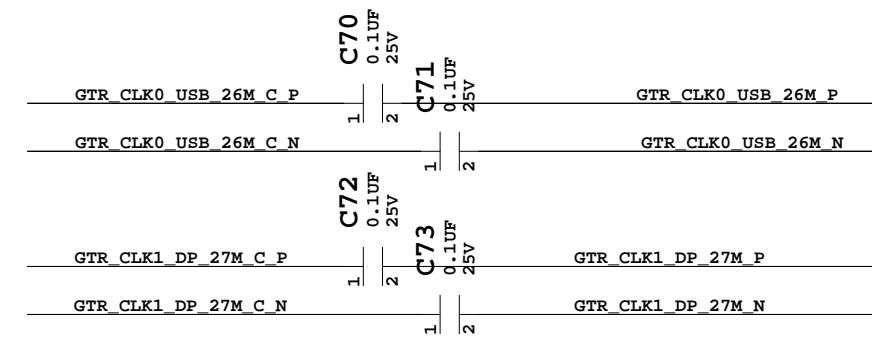
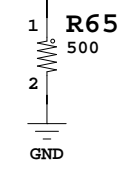


**BANK 505**  
**XCZU3SBVA484**

PS_MGTRTXP0_505_K21	K21	GTR_LANE0_TX_P
PS_MGTRTXN0_505_K22	K22	GTR_LANE0_TX_N
PS_MGTRRXFP0_505_M21	M21	NC
PS_MGTRRXNP0_505_M22	M22	NC
PS_MGTRRXN0_505_M21	F21	GTR_LANE1_TX_P
PS_MGTRTXN1_505_F22	F22	GTR_LANE1_TX_N
PS_MGTRRXFP1_505_H21	H21	NC
PS_MGTRRXNP1_505_H22	H22	NC
PS_MGTRRXN1_505_H22	C19	GTR_LANE2_TX_P
PS_MGTRTXP2_505_C19	C20	GTR_LANE2_TX_N
PS_MGTRTXN2_505_C20	D21	GTR_LANE2_RX_P
PS_MGTRRXFP2_505_D21	D22	GTR_LANE2_RX_N
PS_MGTRRXN2_505_D22	A19	GTR_LANE3_TX_P
PS_MGTRTXP3_505_A19	A20	GTR_LANE3_TX_N
PS_MGTRTXN3_505_A20	B21	GTR_LANE3_RX_P
PS_MGTRRXFP3_505_B21	B22	GTR_LANE3_RX_N
PS_MGTRRXN3_505_B22	L19	GTR_CLK0_USB_26M_C_P
PS_MGTREFCLK0P_505_L19	L20	GTR_CLK0_USB_26M_C_N
PS_MGTREFCLK0N_505_L20	J19	GTR_CLK1_DP_27M_C_P
PS_MGTREFCLK1P_505_J19	J20	GTR_CLK1_DP_27M_C_N
PS_MGTREFCLK1N_505_J20	G19	NC
PS_MGTREFCLK2P_505_G19	G20	NC
PS_MGTREFCLK2N_505_G20	E19	NC
PS_MGTREFCLK3P_505_E19	E20	NC
PS_MGTREFCLK3N_505_E20	M20	NC
PS_MGTREFREF_505_M20		

U1

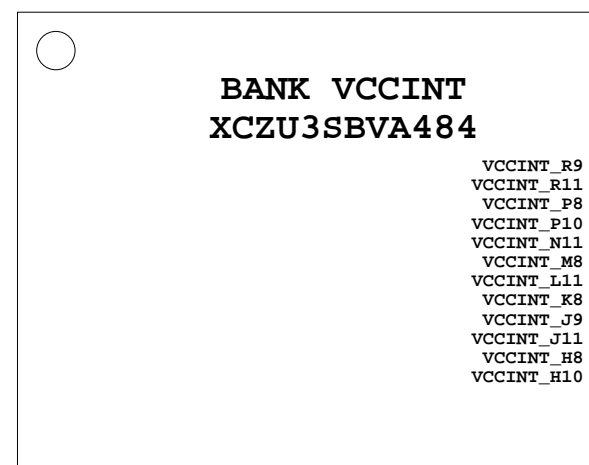
FBGA\_484\_0P8MM



**Zynq Banks 505 - GTR**

<b>AVNET</b>		Avnet Design Services	
Project Name:	AES-ULTRA96-G	PCB Rev:	1 01 00
Doc Num:	SCH-US1DEV	Date:	3/9/2018
Sheet Title:	Zynq Banks 505 - GTR	Time:	12:24:07 pm
		Size:	B
		Sheet:	9 of 27

XCZU3-SBVA484B

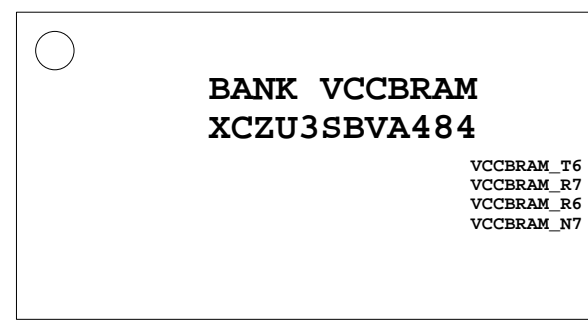


U1

FBGA\_484\_0P8MM

VCCINT

XCZU3-SBVA484B

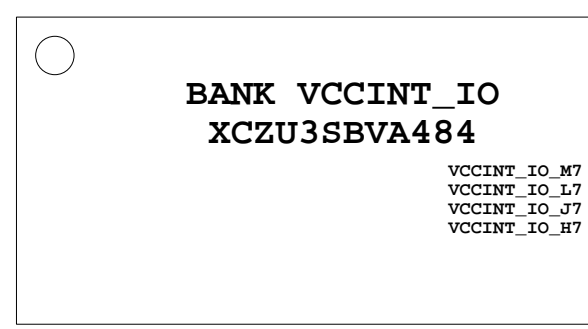


U1

FBGA\_484\_0P8MM

VCCINT

XCZU3-SBVA484B

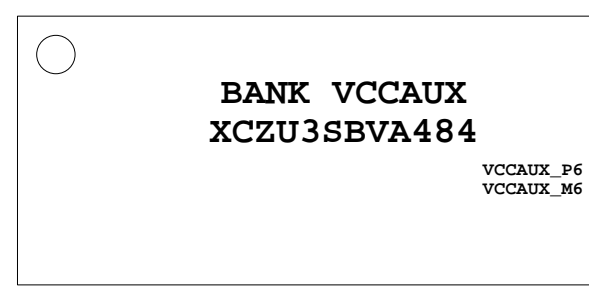


U1

FBGA\_484\_0P8MM

VCCINT

XCZU3-SBVA484B

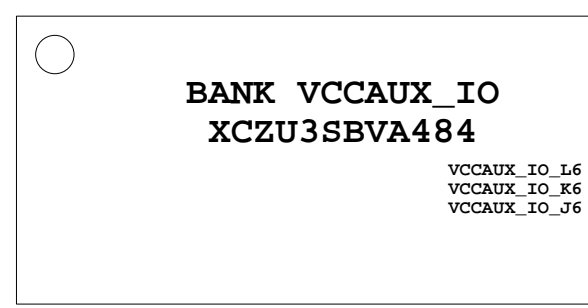


U1

FBGA\_484\_0P8MM

VCCAUX

XCZU3-SBVA484B



U1

FBGA\_484\_0P8MM

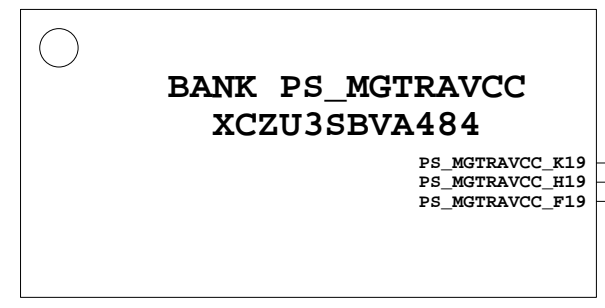
VCCAUX

Zynq Power 1

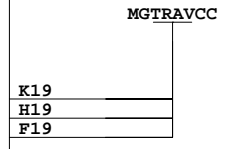
**AVNET** Avnet Design Services

Project Name:	AES-ULTRA96-G	PCB Rev:	1	BOM:	01	Variant:	00
Doc Num:	SCH-US1DEV	Date:	3/9/2018	Time:	12:24:07 pm		
Sheet Title:	Zynq Power 1	Size:	B	Sheet:	10	of 27	

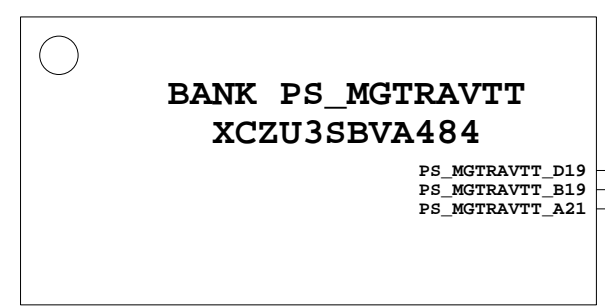
XCZU3-SBVA484B



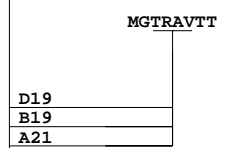
U1 FBGA\_484\_0P8MM



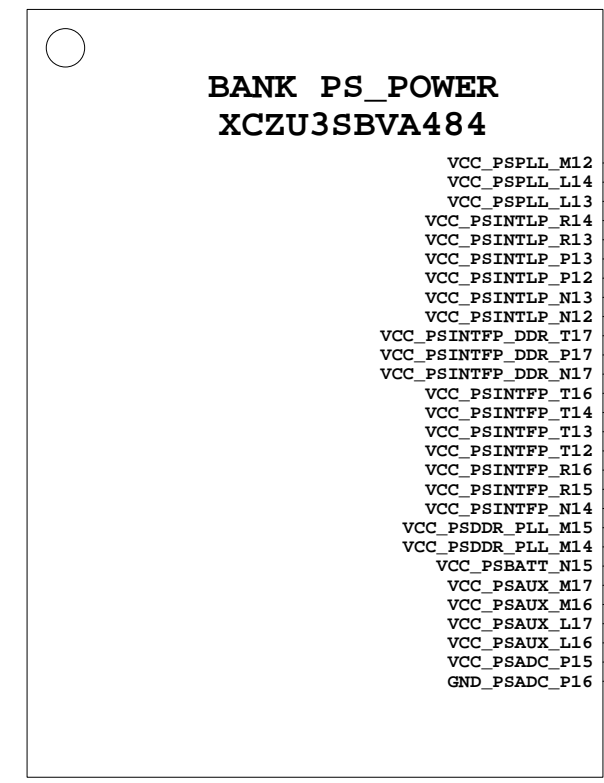
XCZU3-SBVA484B



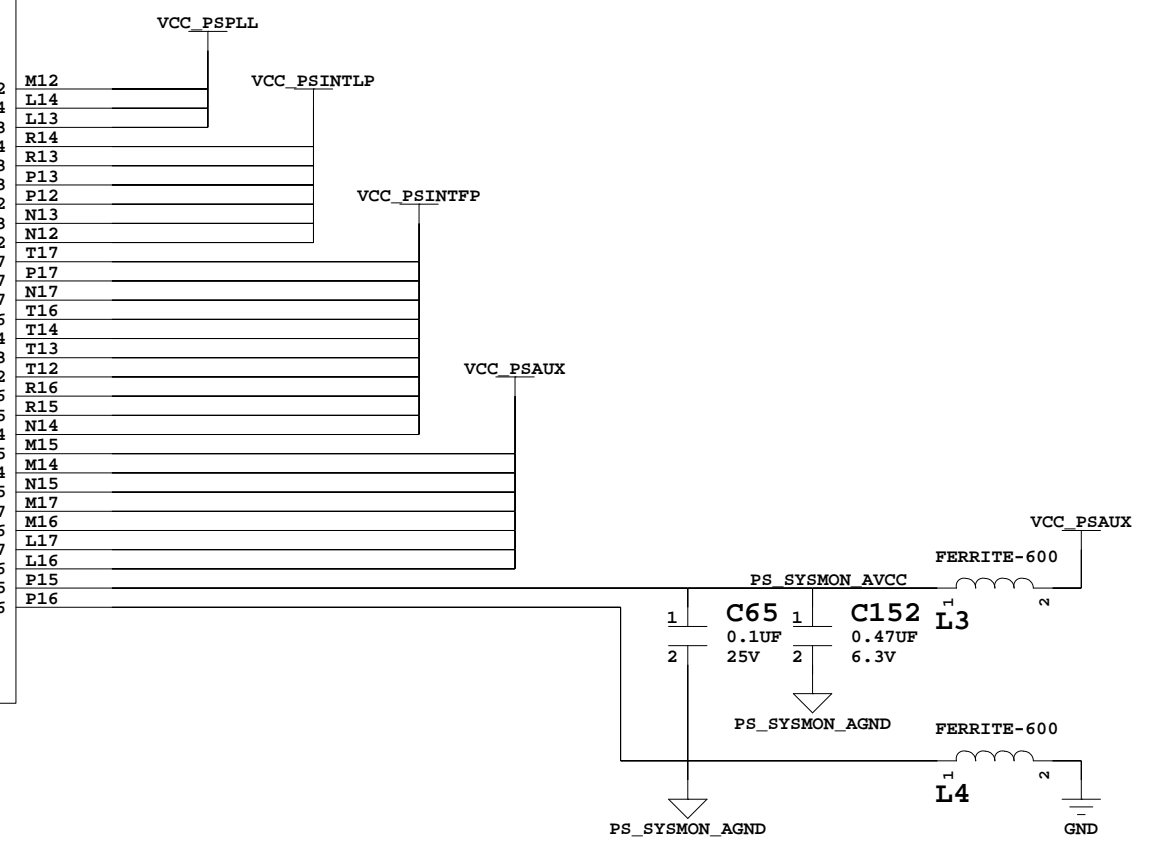
U1 FBGA\_484\_0P8MM



XCZU3-SBVA484B



U1 FBGA\_484\_0P8MM



Zynq Power 2

**AVNET** Avnet Design Services

Project Name:	AES-ULTRA96-G	PCB Rev:	BOM:	Variant:
Doc Num:	SCH-US1DEV	Date:	3/9/2018	Time:
Sheet Title:	Zynq Power 2	Size:	B	Sheet:
				11 of 27

U1  
FPGA\_484\_0P8MM

- AJ GND\_A1
- A10 GND\_A10
- A15 GND\_A15
- A18 GND\_A18
- A22 GND\_A22
- A5 GND\_A5
- AA10 GND\_AA10
- AA15 GND\_AA15
- AA20 GND\_AA20
- AB1 GND\_AB1
- AB13 GND\_AB13
- AB22 GND\_AB22
- AB3 GND\_AB3
- AB8 GND\_AB8
- B13 GND\_B13
- B20 GND\_B20
- C1 GND\_C1
- C18 GND\_C18
- C21 GND\_C21
- C22 GND\_C22
- C6 GND\_C6
- D20 GND\_D20
- D4 GND\_D4
- D9 GND\_D9
- E12 GND\_E12
- E17 GND\_E17
- E18 GND\_E18
- E2 GND\_E2
- E21 GND\_E21
- E22 GND\_E22
- F15 GND\_F15
- F20 GND\_F20
- F5 GND\_F5
- G18 GND\_G18
- G21 GND\_G21
- G22 GND\_G22
- G8 GND\_G8
- H1 GND\_H1
- H11 GND\_H11
- H20 GND\_H20
- H6 GND\_H6
- H9 GND\_H9
- J10 GND\_J10
- J14 GND\_J14
- J18 GND\_J18
- J21 GND\_J21
- J22 GND\_J22
- J4 GND\_J4
- J8 GND\_J8
- K11 GND\_K11
- K17 GND\_K17
- K20 GND\_K20
- K7 GND\_K7
- L15 GND\_L15
- L18 GND\_L18
- L21 GND\_L21
- L22 GND\_L22
- L5 GND\_L5
- L8 GND\_L8
- M11 GND\_M11
- M13 GND\_M13
- M18 GND\_M18
- M19 GND\_M19
- M3 GND\_M3
- N1 GND\_N1
- N16 GND\_N16
- N20 GND\_N20
- N21 GND\_N21
- N22 GND\_N22
- N6 GND\_N6
- N8 GND\_N8
- P11 GND\_P11
- P14 GND\_P14
- P7 GND\_P7
- P9 GND\_P9
- R10 GND\_R10
- R12 GND\_R12
- R17 GND\_R17
- R2 GND\_R2
- R22 GND\_R22
- R8 GND\_R8
- T11 GND\_T11
- T15 GND\_T15
- T5 GND\_T5
- U13 GND\_U13
- U18 GND\_U18
- U3 GND\_U3
- U8 GND\_U8
- V1 GND\_V1
- V11 GND\_V11
- W14 GND\_W14
- W19 GND\_W19
- W4 GND\_W4
- W9 GND\_W9
- Y12 GND\_Y12
- Y2 GND\_Y2
- Y7 GND\_Y7

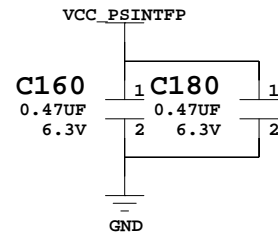


**XCZU3SBVA484**  
**BANK GND**

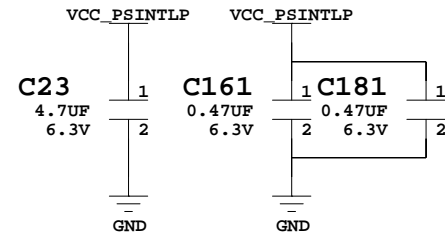
XCZU3-SBVA484B

Zynq GND

<b>AVNET</b>		Avnet Design Services	
Project Name:	AES-ULTRA96-G	PCB Rev:	BOM: Variant:
		1	01 00
Doc Num:	SCH-US1DEV	Date:	Time:
		3/9/2018	12:24:07 pm
Sheet Title:	Zynq GND	Size:	Sheet:
		R	12 of 27

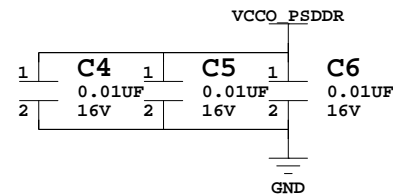
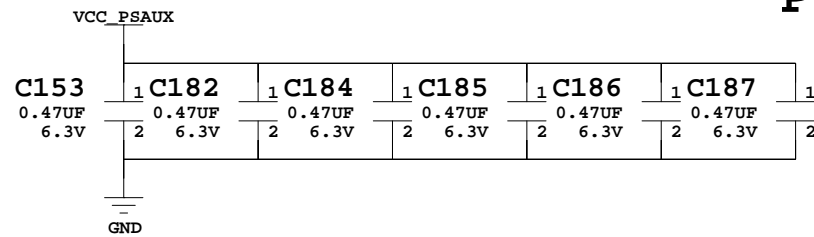


VCCPSINTFP



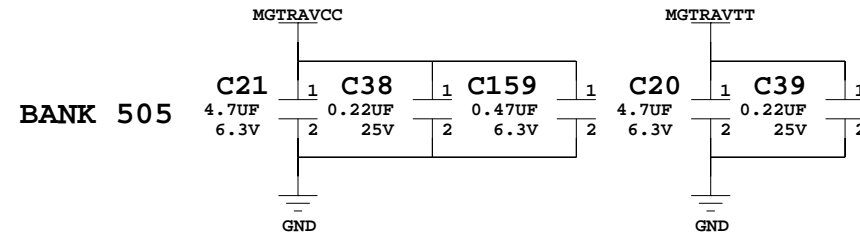
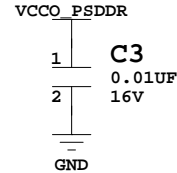
VCCPSINTLP

VCCPSAUX/PSADC/PSDDRPLL  
PSIO1-3

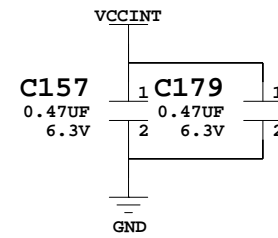


VCCPSDDR

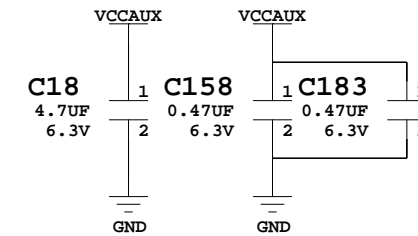
Place this cap directly under U1



MGTRAVCC/AVTT



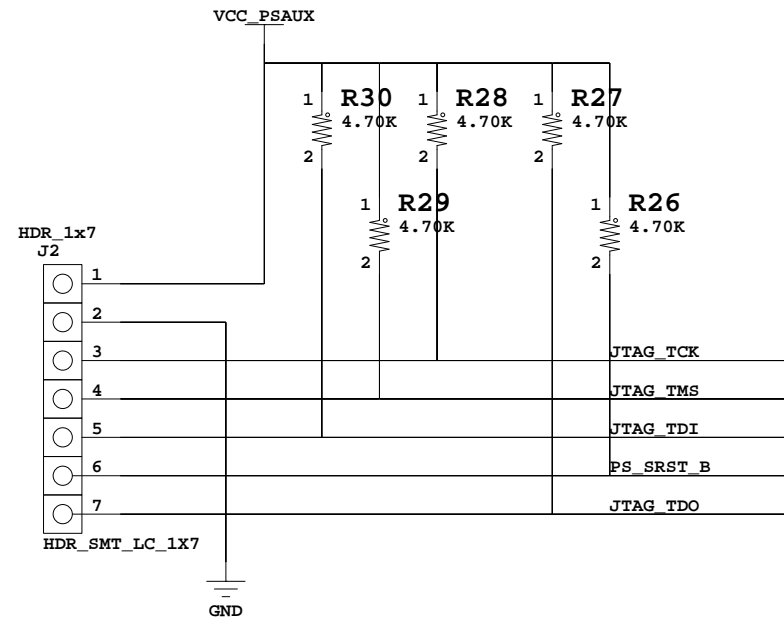
PL VCCINT/VCCBRAM



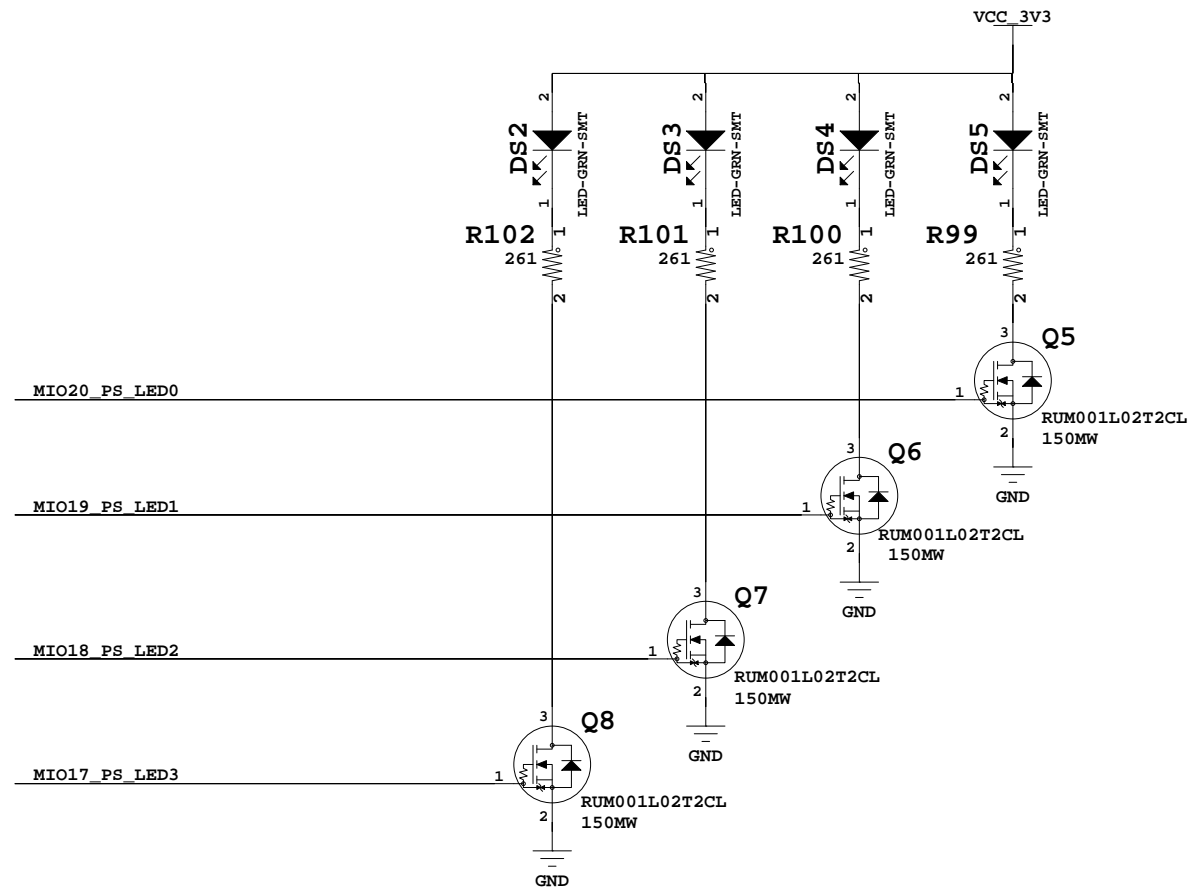
PL VCCAUX / VCCAUX\_IO

Zynq Decoupling

<b>AVNET</b>		Avnet Design Services	
Project Name:	AES-ULTRA96-G	PCB Rev:	1
Doc Num:	SCH-US1DEV	BOM:	01
Sheet Title:	Zynq Decoupling	Variant:	00
		Date:	3/9/2018
		Time:	12:24:07 pm
		Size:	B
		Sheet:	13 of 27



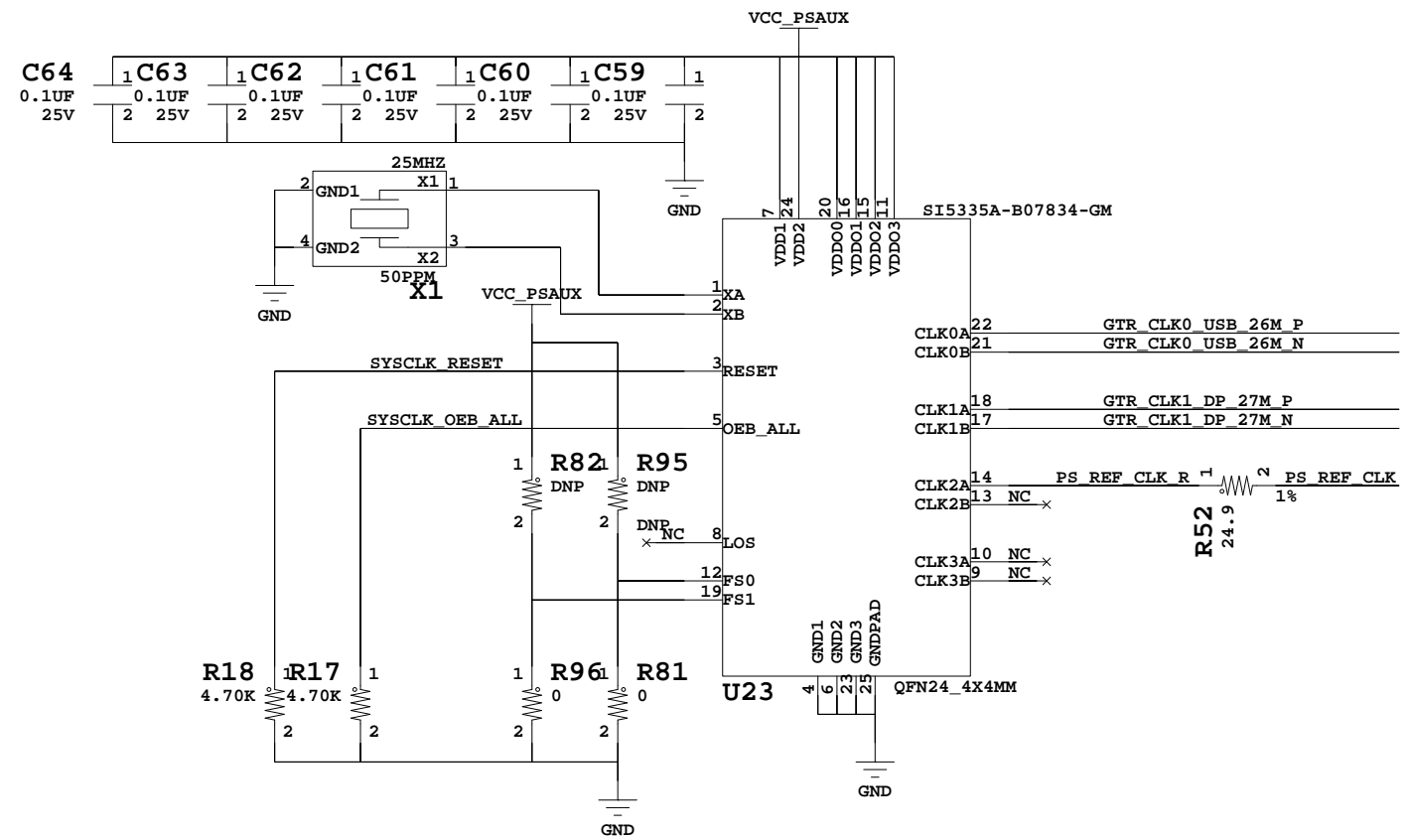
# JTAG on Bottomside



## JTAG Headers - LEDs

<b>AVNET</b> Avnet Design Services		PCB Rev:	BOM:	Variant:
Project Name: AES-ULTRA96-G		1	01	00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm		
Sheet Title: JTAG Headers - LEDs		Size: B	Sheet: 14 of 27	





26MHz LVDS

27MHz LVDS

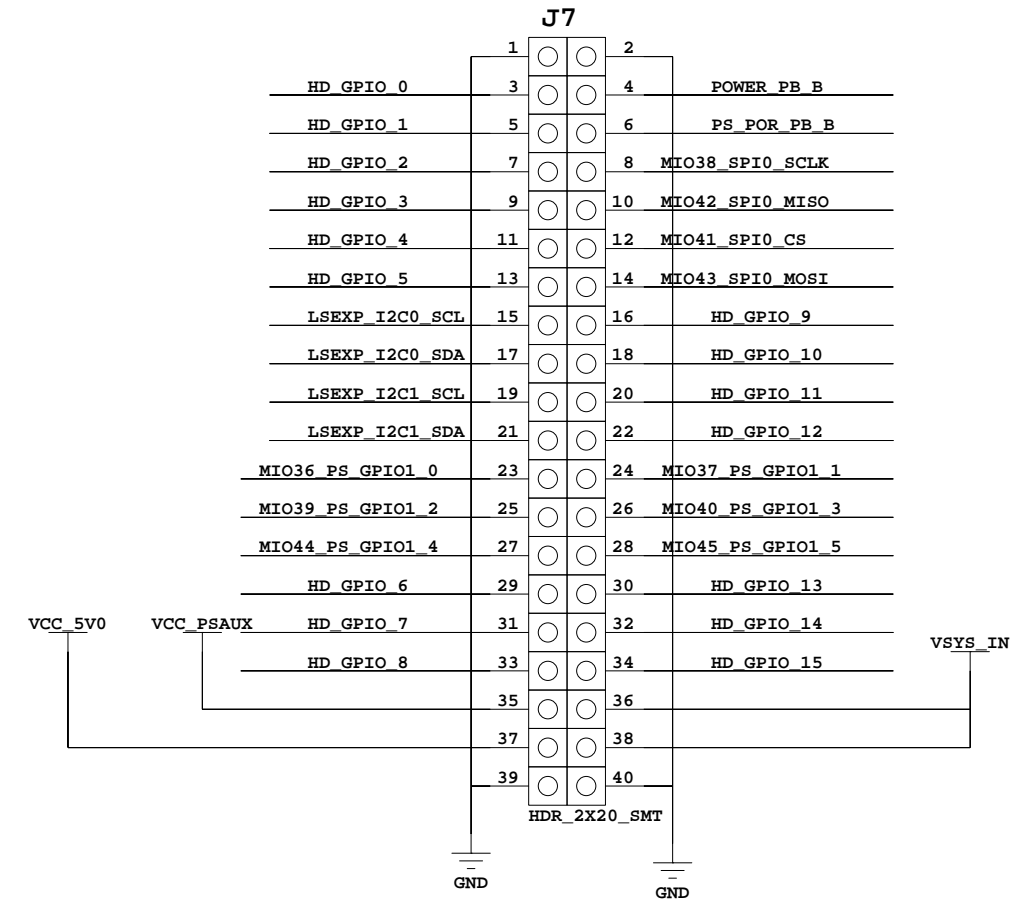
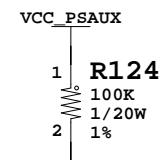
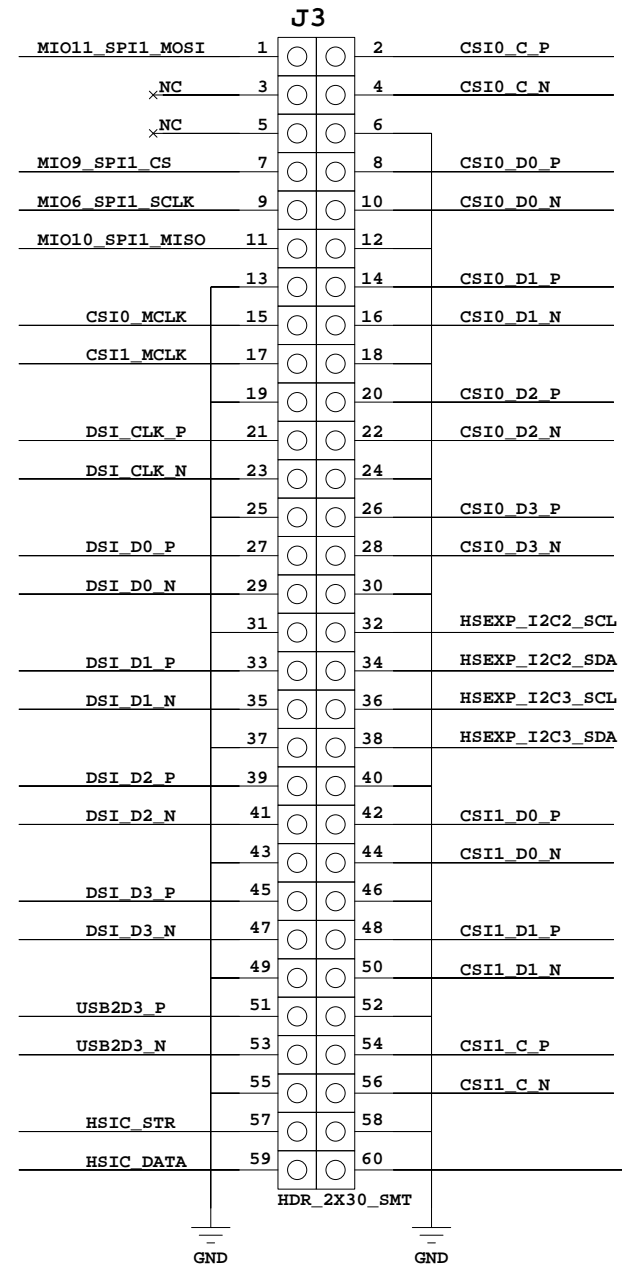
33.33333333MHz LVCMOS  
(100/3)

**Fixed Clocks**

<b>AVNET</b>		Avnet Design Services	
Project Name:	AES-ULTRA96-G	PCB Rev:	BOM: 1 01 00
Doc Num:	SCH-US1DEV	Date:	3/9/2018
Sheet Title:	Fixed Clocks	Time:	12:24:07 pm
		Size:	B
		Sheet:	16 of 27



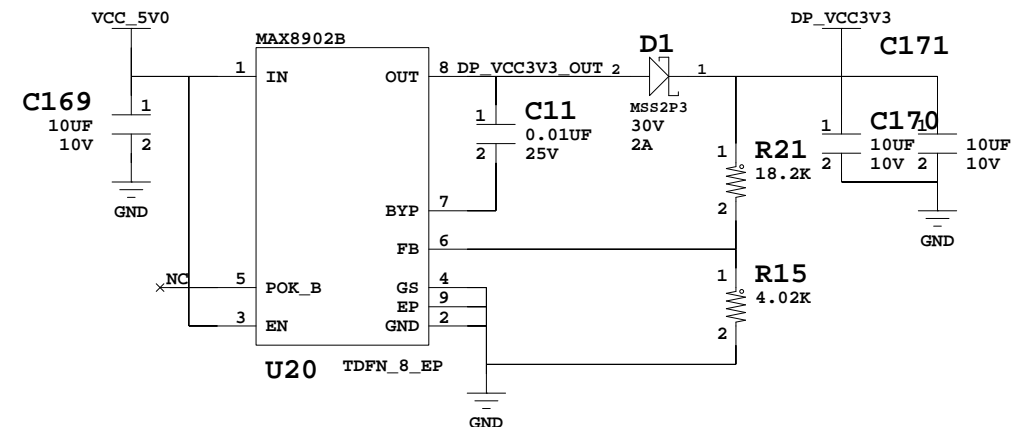
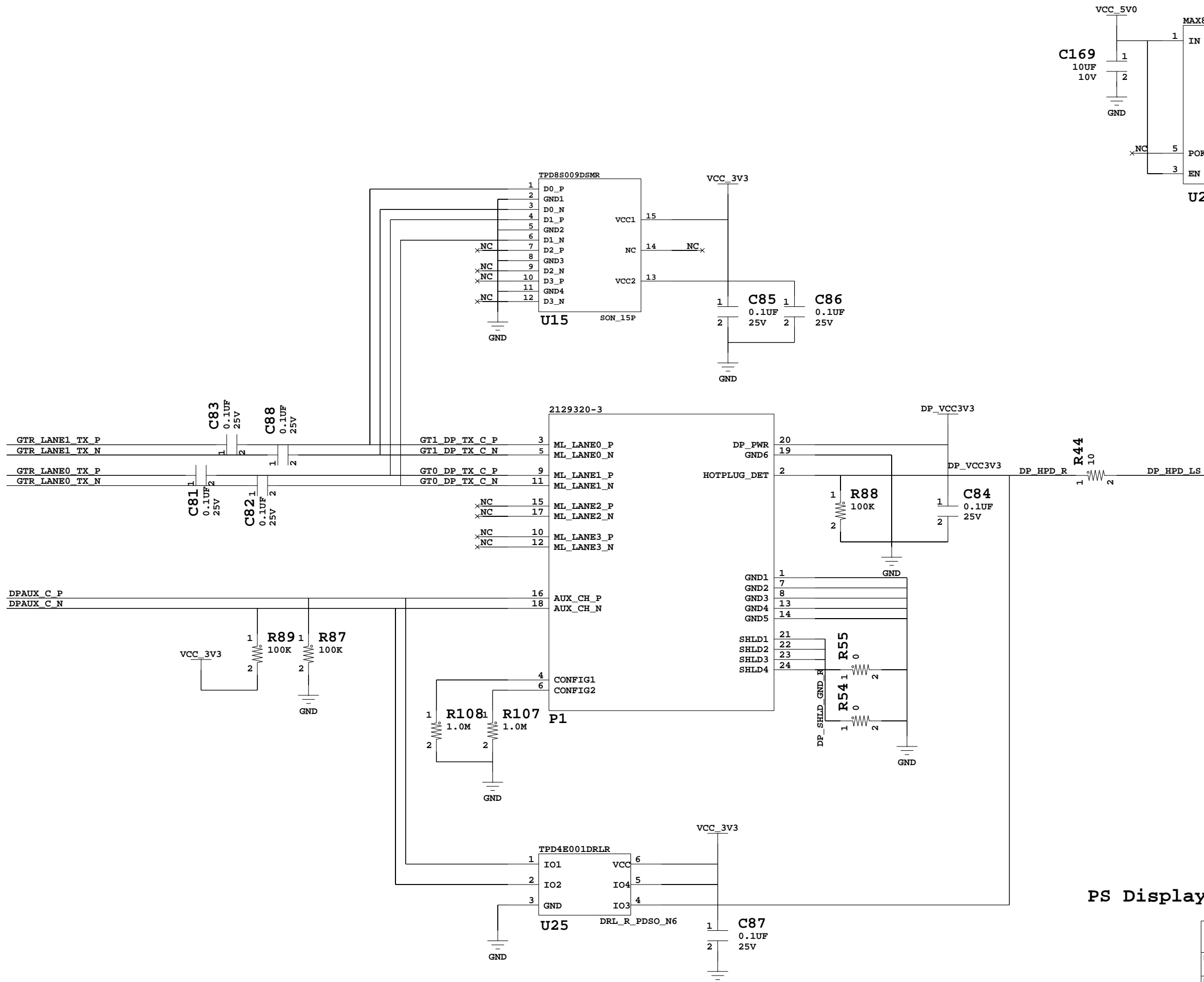
SPI shared with HS header  
Different CS signals



Expansion Headers

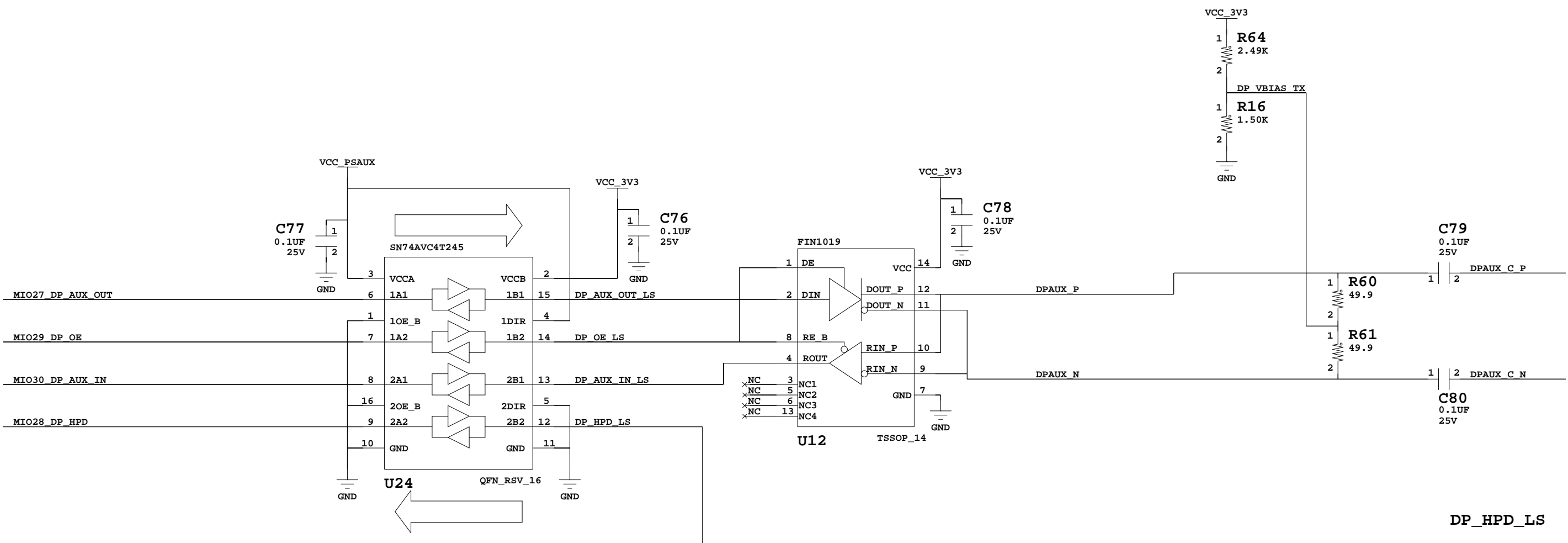
**AVNET** Avnet Design Services

Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: Expansion Headers	Size: B	Sheet: 17 of 27	



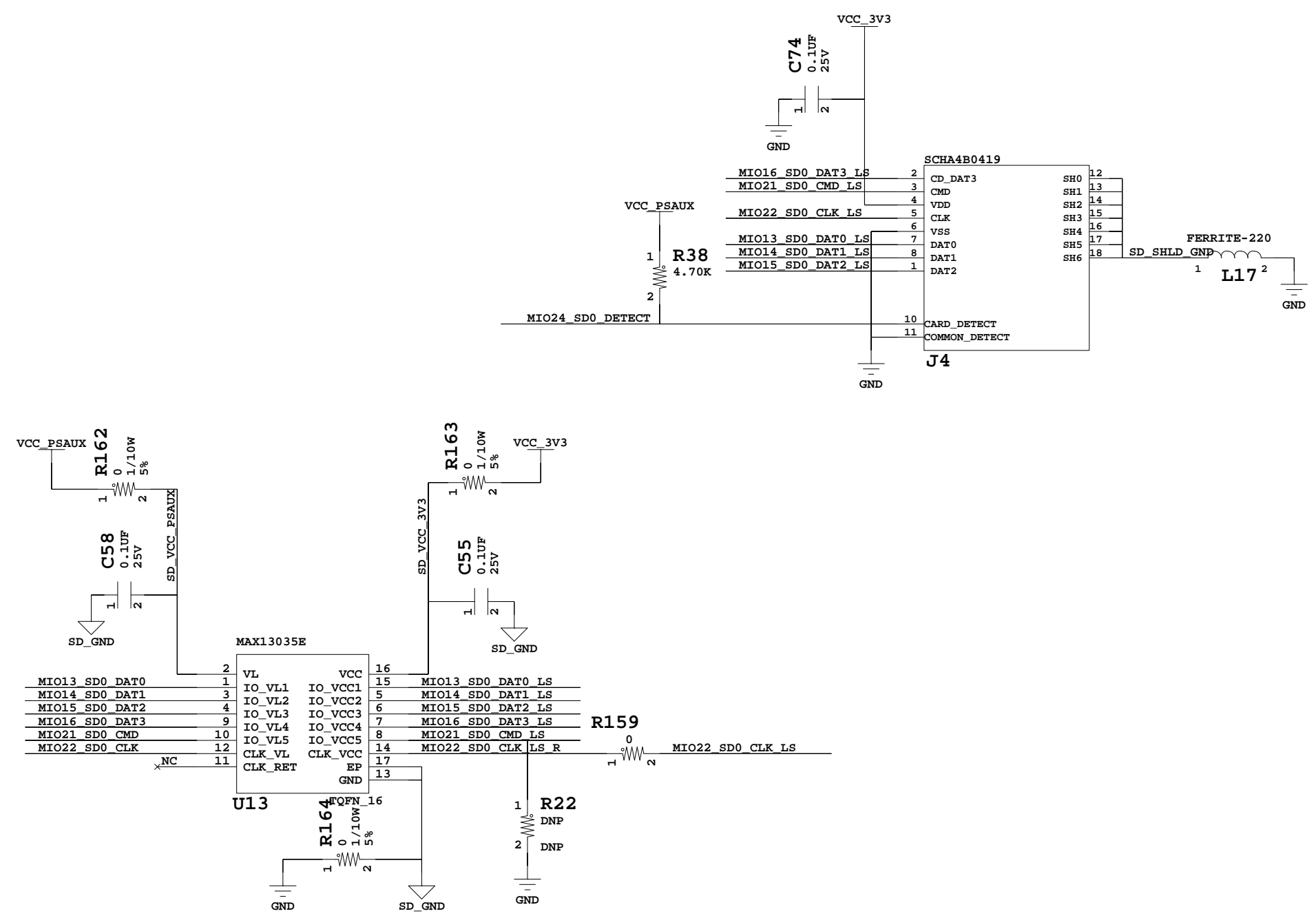
PS Display Port Connector

<b>AVNET</b> Avnet Design Services		PCB Rev:	BOM:	Variant:
Project Name: AES-ULTRA96-G		1	01	00
Doc Num: SCH-US1DEV		Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: PS Display Port Connector		Size: B	Sheet: 18 of 27	



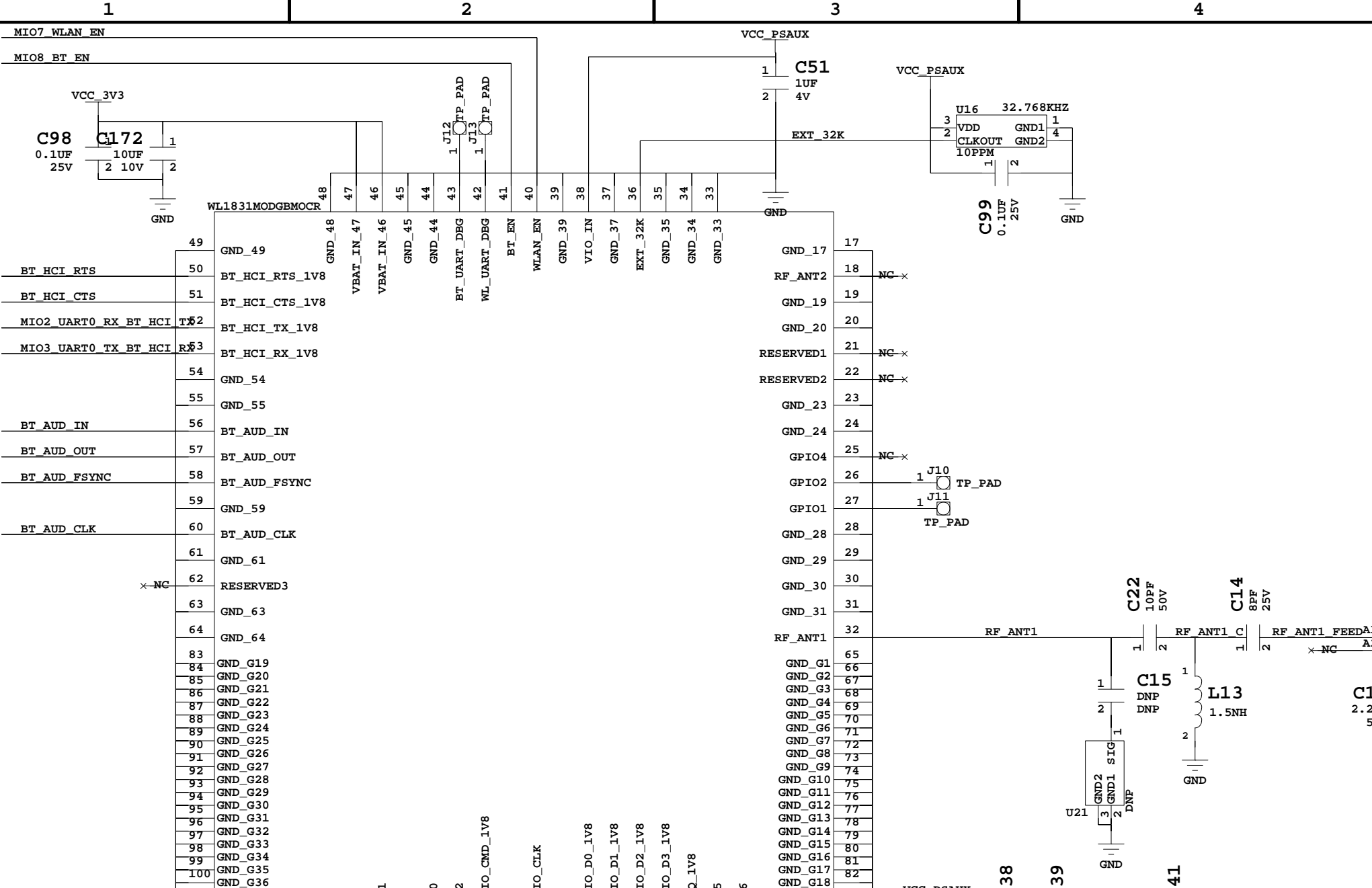
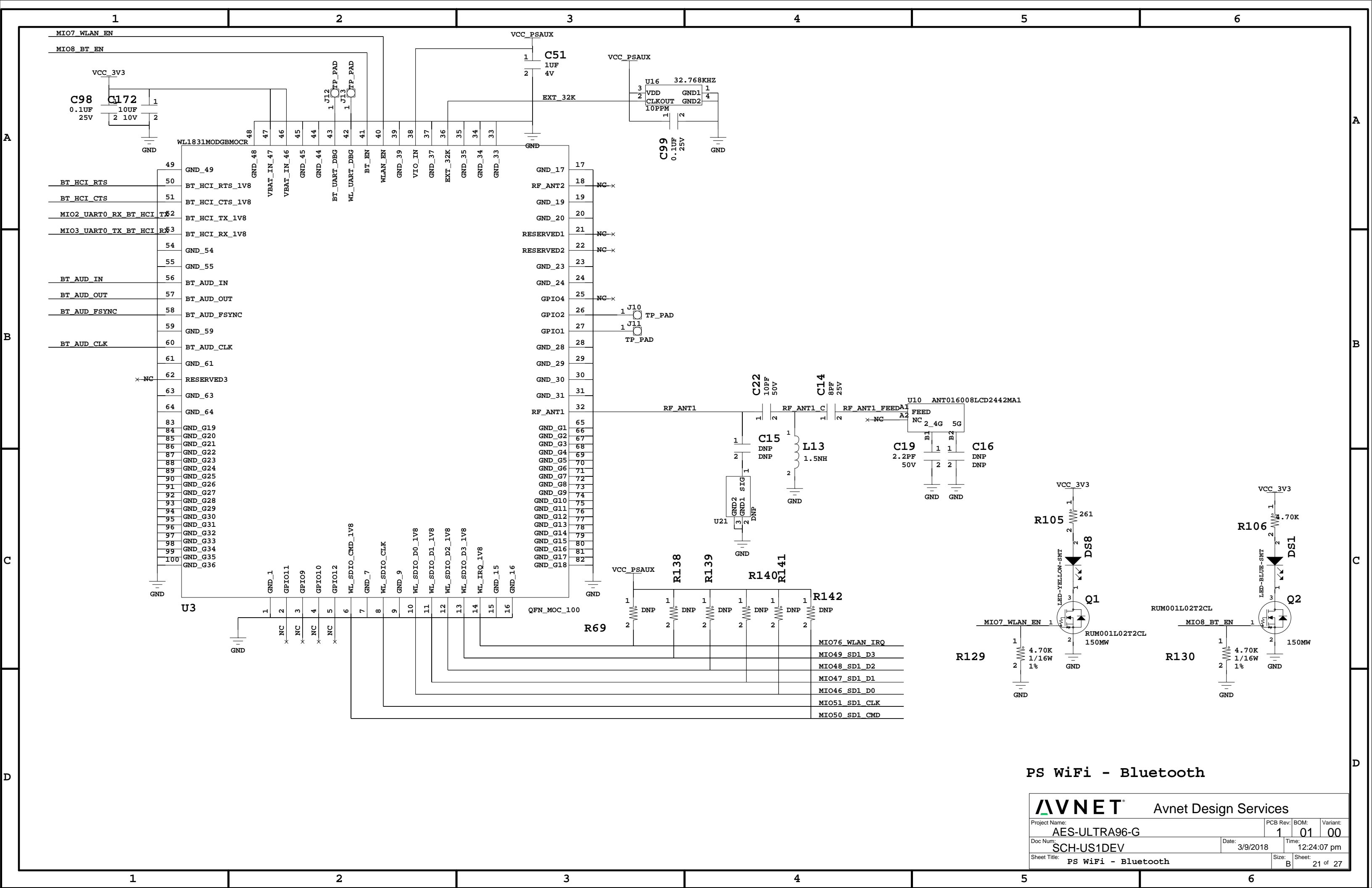
PS Display Port IO

<b>AVNET</b>		Avnet Design Services	
Project Name:	AES-ULTRA96-G	PCB Rev:	BOM: 1 01 00
Doc Num:	SCH-US1DEV	Date:	3/9/2018
Sheet Title:	PS Display Port IO	Time:	12:24:07 pm
		Size:	Sheet: 19 of 27



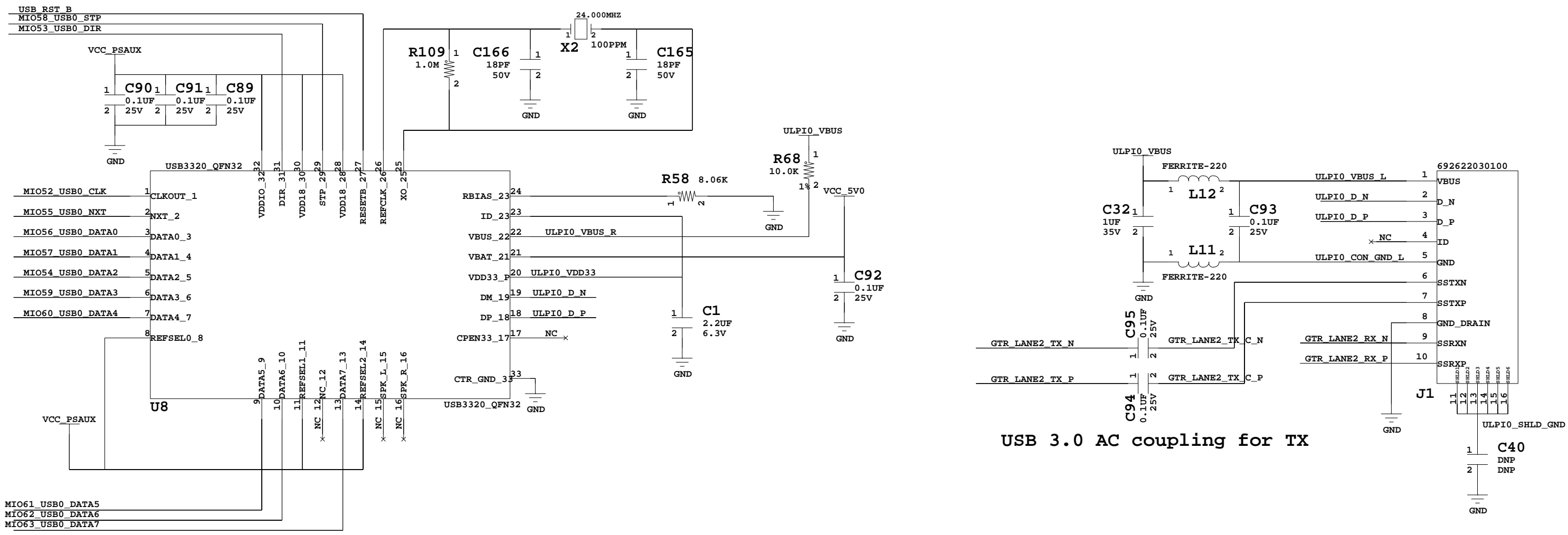
PS Micro SD Card

<b>AVNET</b> Avnet Design Services	
Project Name: AES-ULTRA96-G	PCB Rev: 1 BOM: 01 Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018 Time: 12:24:07 pm
Sheet Title: PS Micro SD Card	Size: B Sheet: 20 of 27



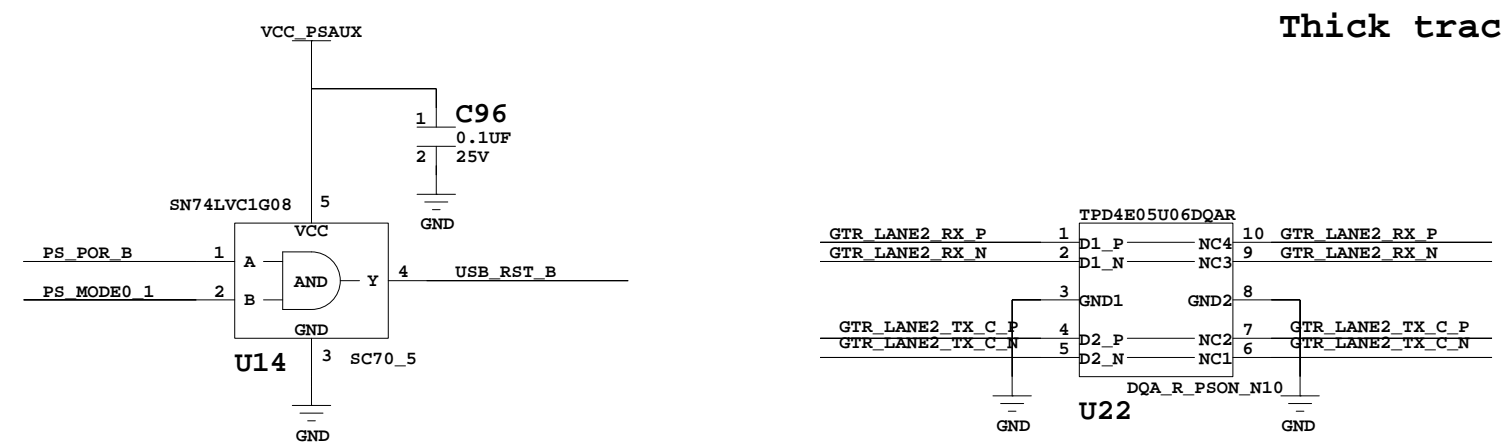
PS WiFi - Bluetooth

<b>AVNET</b> Avnet Design Services		PCB Rev:	BOM:	Variant:
Project Name: AES-ULTRA96-G		1	01	00
Doc Num: SCH-US1DEV		Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: PS WiFi - Bluetooth		Size: B	Sheet: 21 of 27	

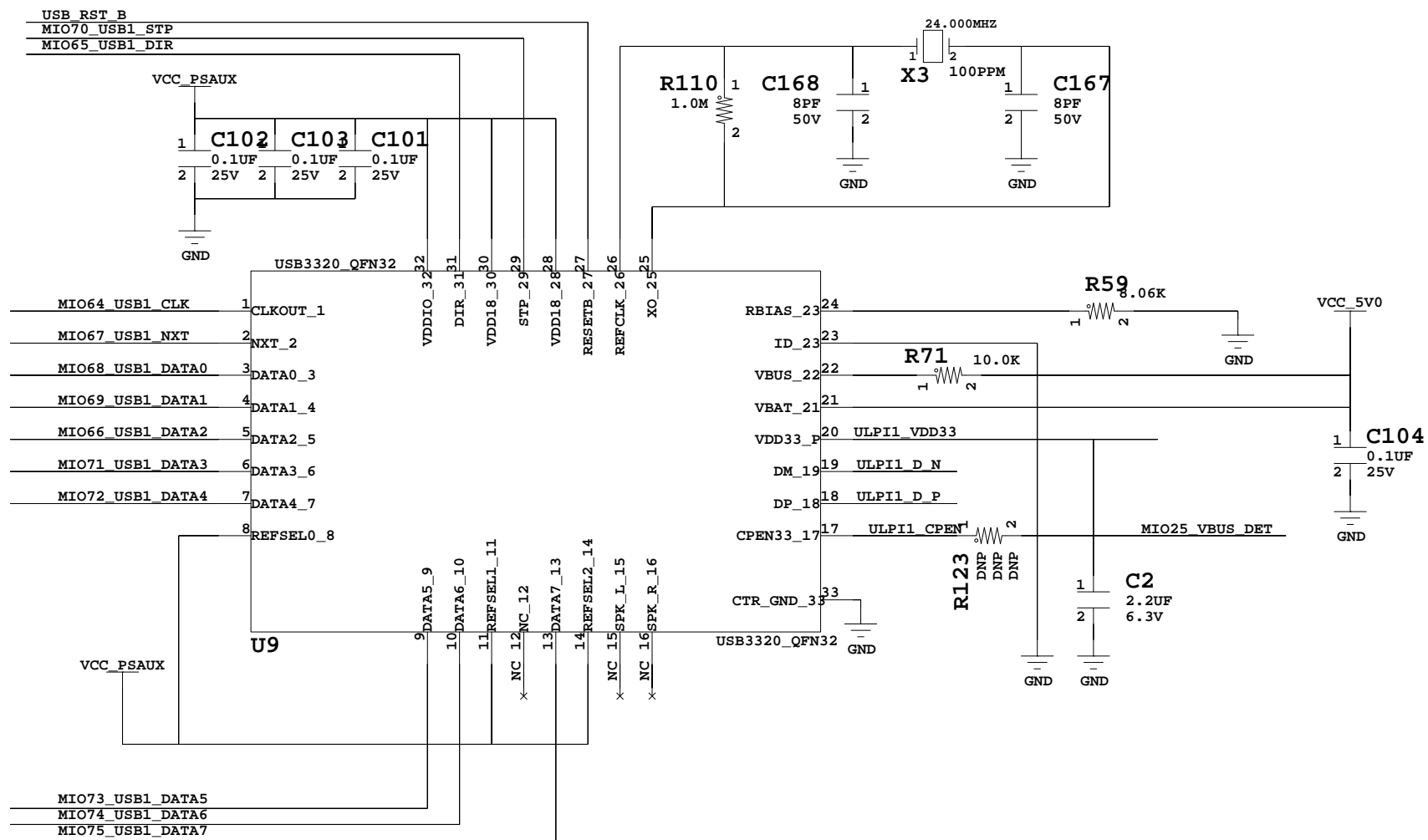


USB 3.0 AC coupling for TX

90 ohm impedance for USB 2.0 ULPI\_D\_P/N,  
 100 ohm for USB 3.0 USB\_SSTX\_P/N, USB\_SSRX\_P/N  
 Thick trace for ULPI\_VBUS and related nets



PS USB 3\_0 ULPI Upstream



90 ohm impedance for USB 2.0 ULPI\_D\_P/N

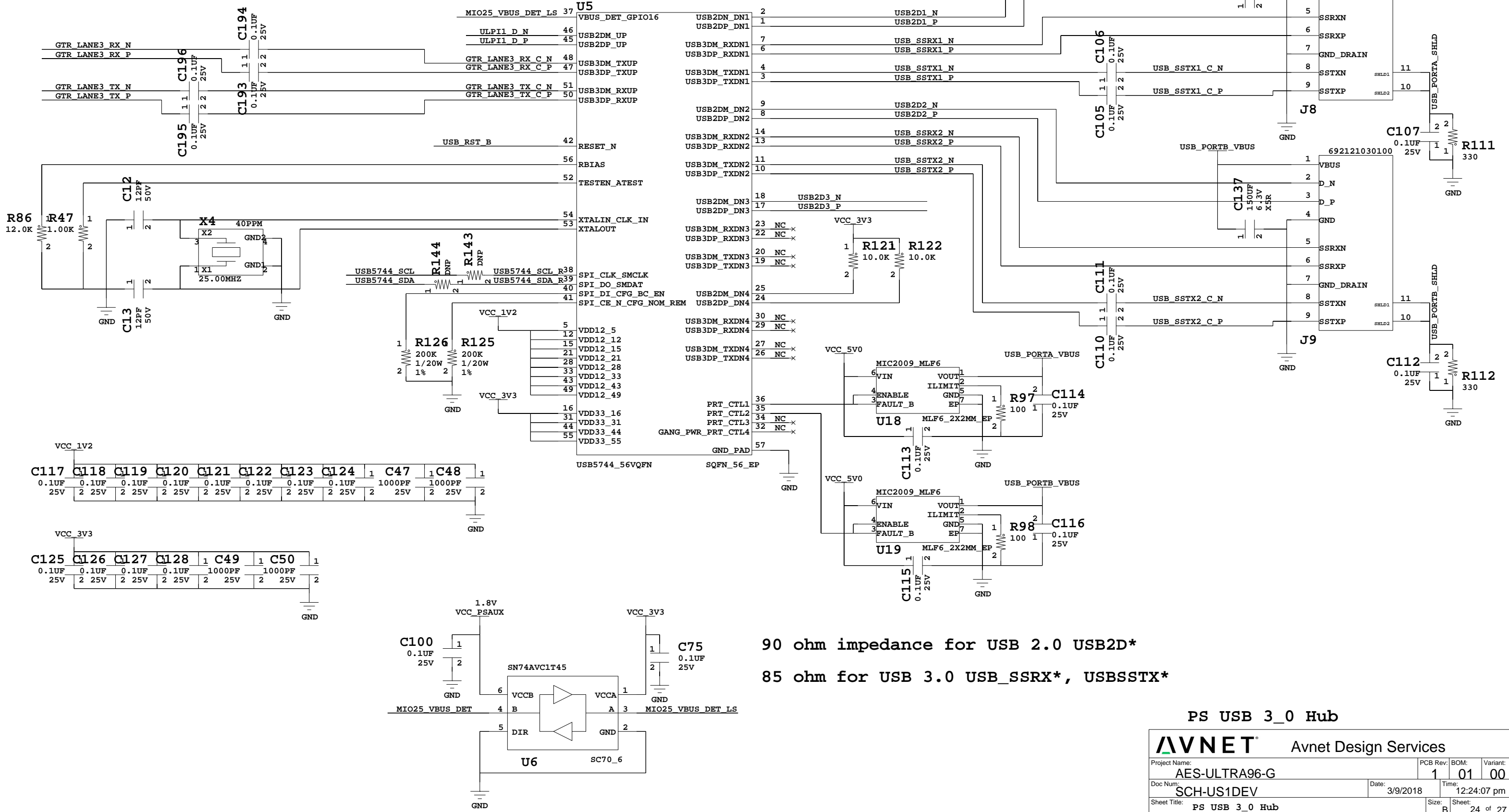
PS USB 3\_0 ULPI Downstream

<b>AVNET</b>		Avnet Design Services	
Project Name:	AES-ULTRA96-G	PCB Rev:	BOM: Variant:
		1	01 00
Doc Num:	SCH-US1DEV	Date:	Time:
		3/9/2018	12:24:07 pm
Sheet Title:	PS USB 3_0 ULPI Downstream	Size:	Sheet:
		B	23 of 27

90 ohm impedance for USB 2.0 ULPI\_D\_P/N,

100 ohm for USB 3.0 GTR\_LANE3\*

USB 3.0: Connect TX to RX, add AC coupling



90 ohm impedance for USB 2.0 USB2D\*

85 ohm for USB 3.0 USB\_SSRX\*, USB\_SSTX\*

PS USB 3\_0 Hub

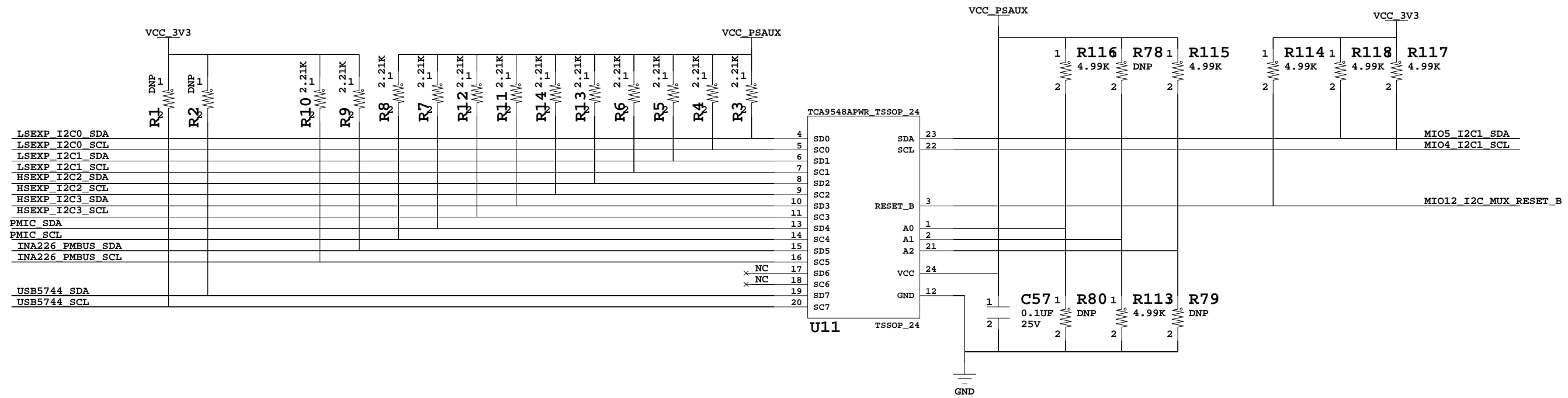
**AVNET** Avnet Design Services

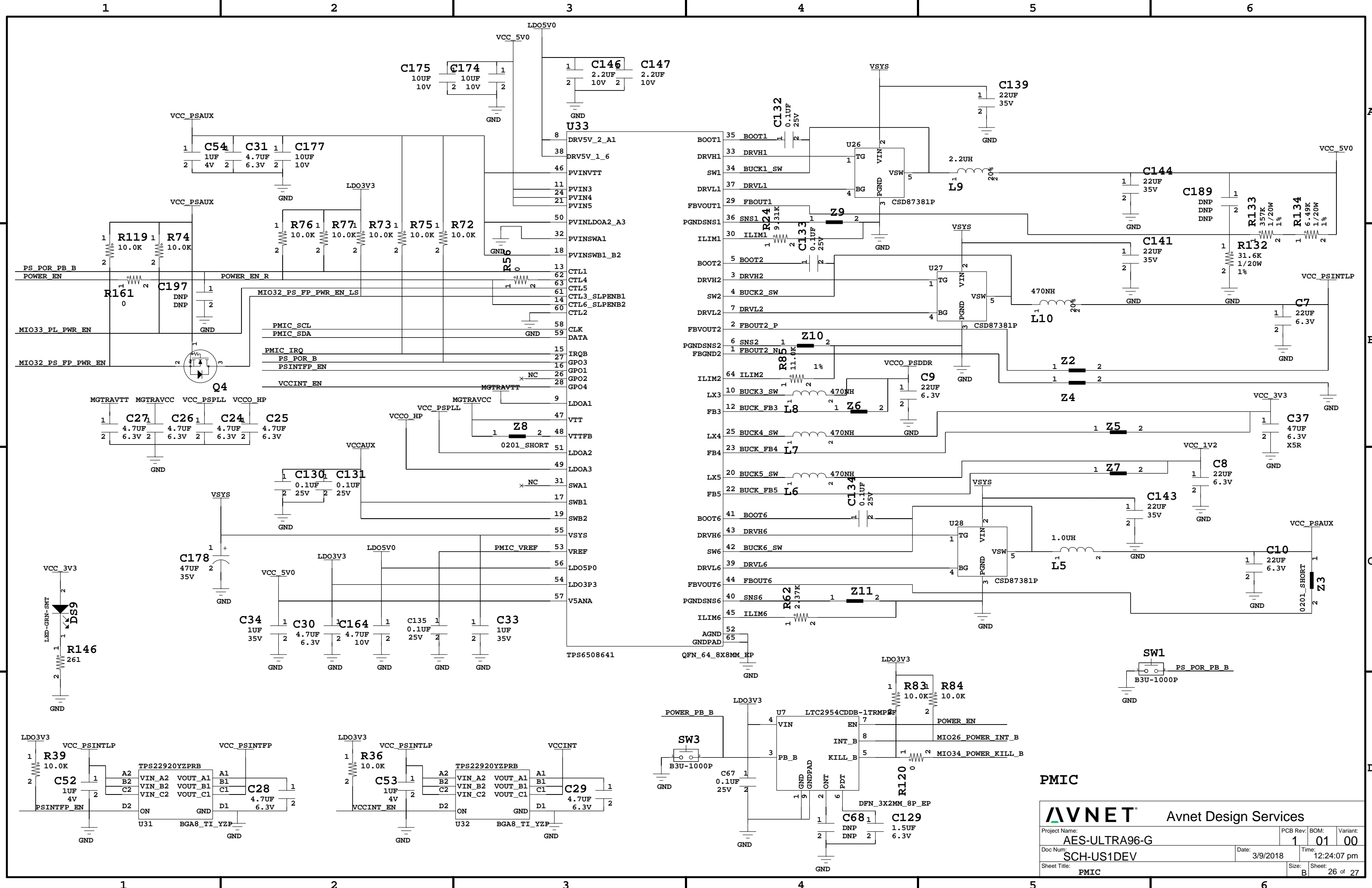
Project Name:	AES-ULTRA96-G	PCB Rev:	BOM:	Variant:	
Doc Num:	SCH-US1DEV	Date:	3/9/2018	Time:	12:24:07 pm
Sheet Title:	PS USB 3_0 Hub	Size:	B	Sheet:	24 of 27



A

A

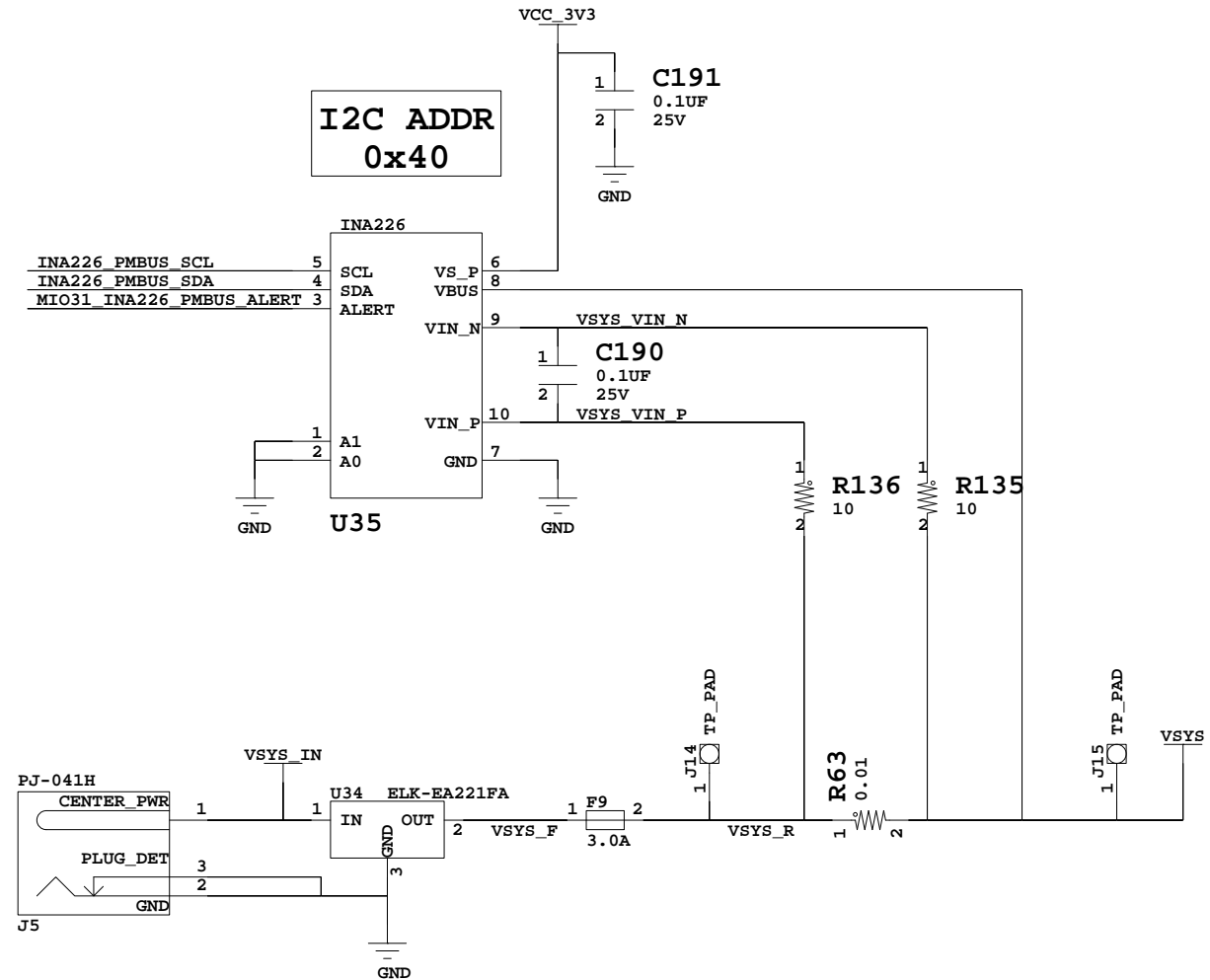




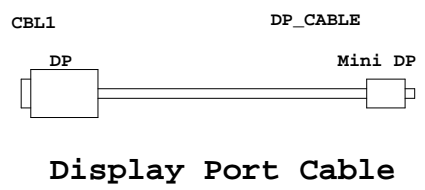
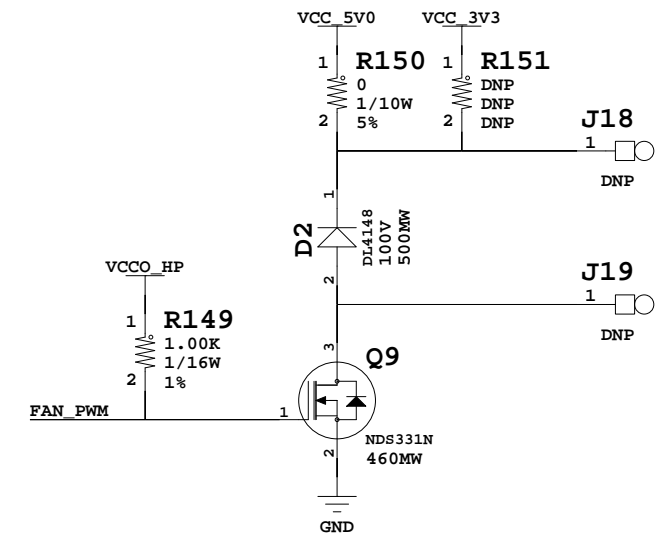
**PMIC**

**AVNET** Avnet Design Services

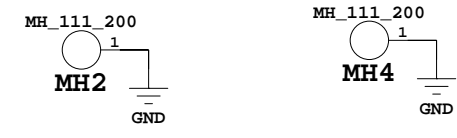
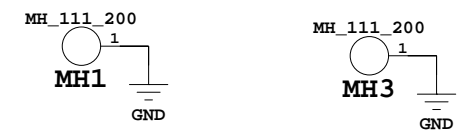
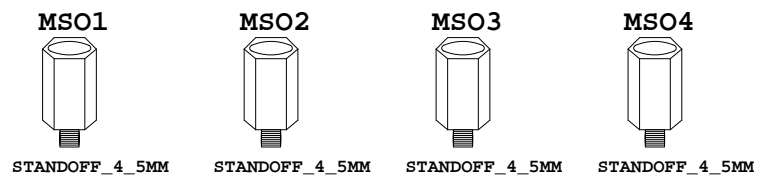
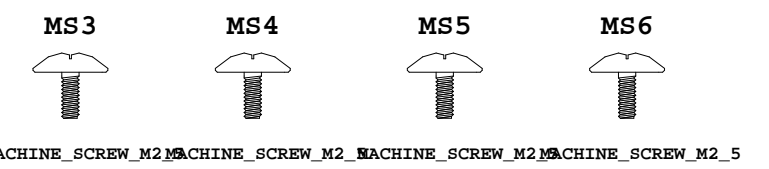
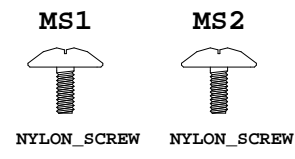
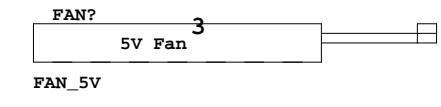
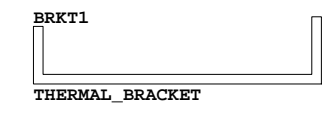
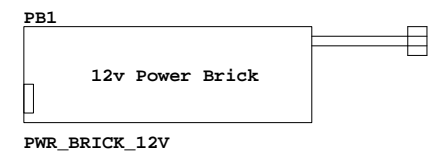
Project Name:	AES-ULTRA96-G	PCB Rev:	BOM:	Variant:
Doc Num:	SCH-US1DEV	Date:	3/9/2018	Time:
Sheet Title:	PMIC	Size:	B	Sheet:
				26 of 27



Fan wires, place near board edge



RAIL	VOLTAGE
VCC_PSINTFP	0.85V
VCC_PSINTLP	0.85V
VCC_PSPLL	1.20V
VCC_PSAUX	1.80V
VCC_PSDDR	1.10V
MGTRAVCC	0.90V
MGTRAVTT	1.80V
VCCINT	0.85V
VCCAUX	1.80V
VCCO_HP	1.20V
VCC_5V0	5.00V
VCC_3V3	3.30V
VCC_1V2	1.20V
LDO5V0	5.00V
LDO3V3	3.30V
USB_PORTA_VBUS	5.00V
USB_PORTB_VBUS	5.00V
DP_VCC3V3	3.30V



Power Connector - Mounting Holes