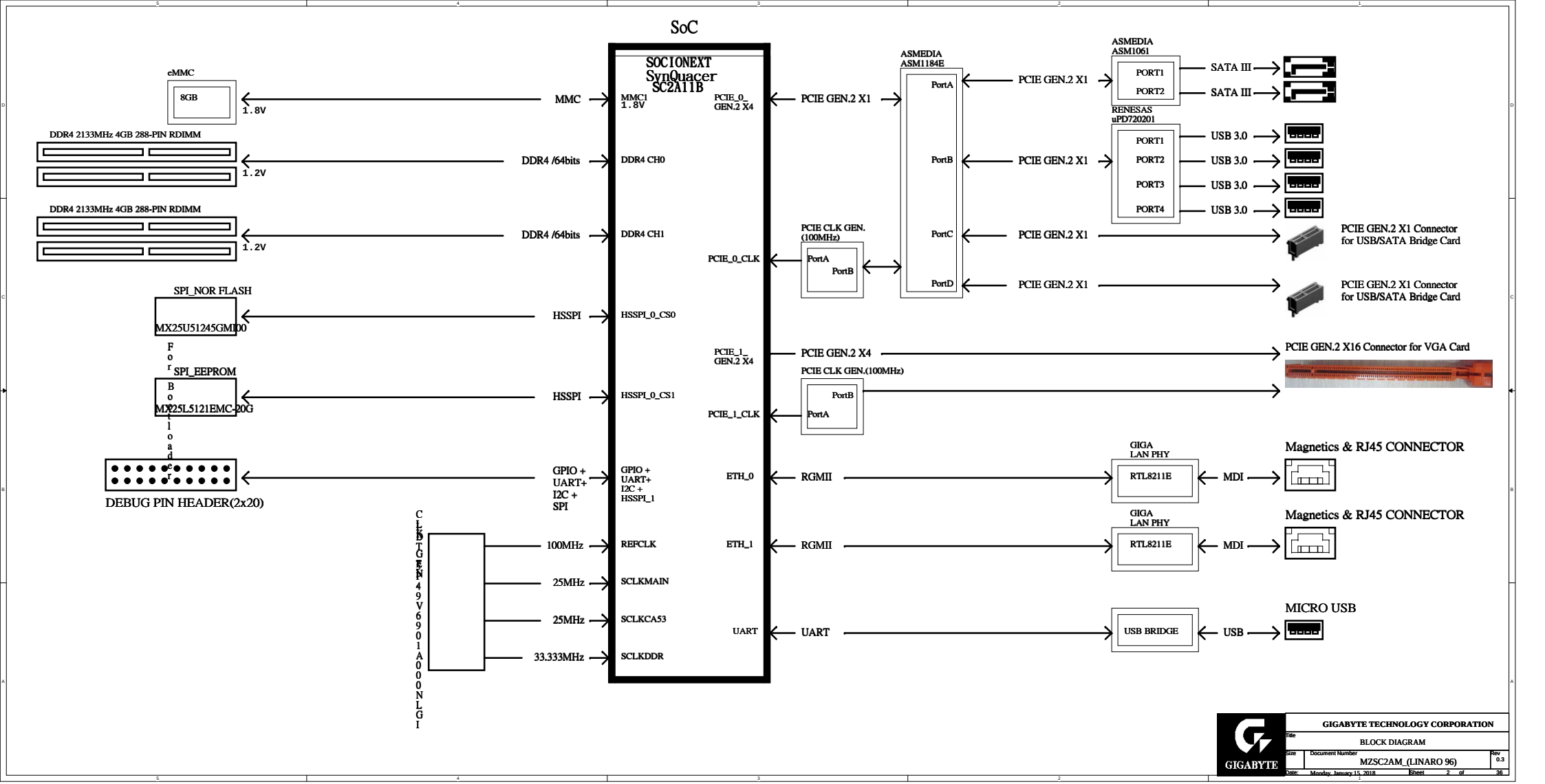
MZSC2AM_(LINARO 96) Rev:0.3

GIGABYTE

GIGABYTE TECHNOLOGY CORPORATION

Title: COVER		
Size	Document Number: MZSC2AM_(LINARO 96)	Rev: 0.3
Date: Monday, January 15, 2018	Sheet 1 of 36	



GIGABYTE

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Title: BLOCK DIAGRAM

Size | Document Number: MZSC2AM_(LINARO 96) | Rev: 0.3

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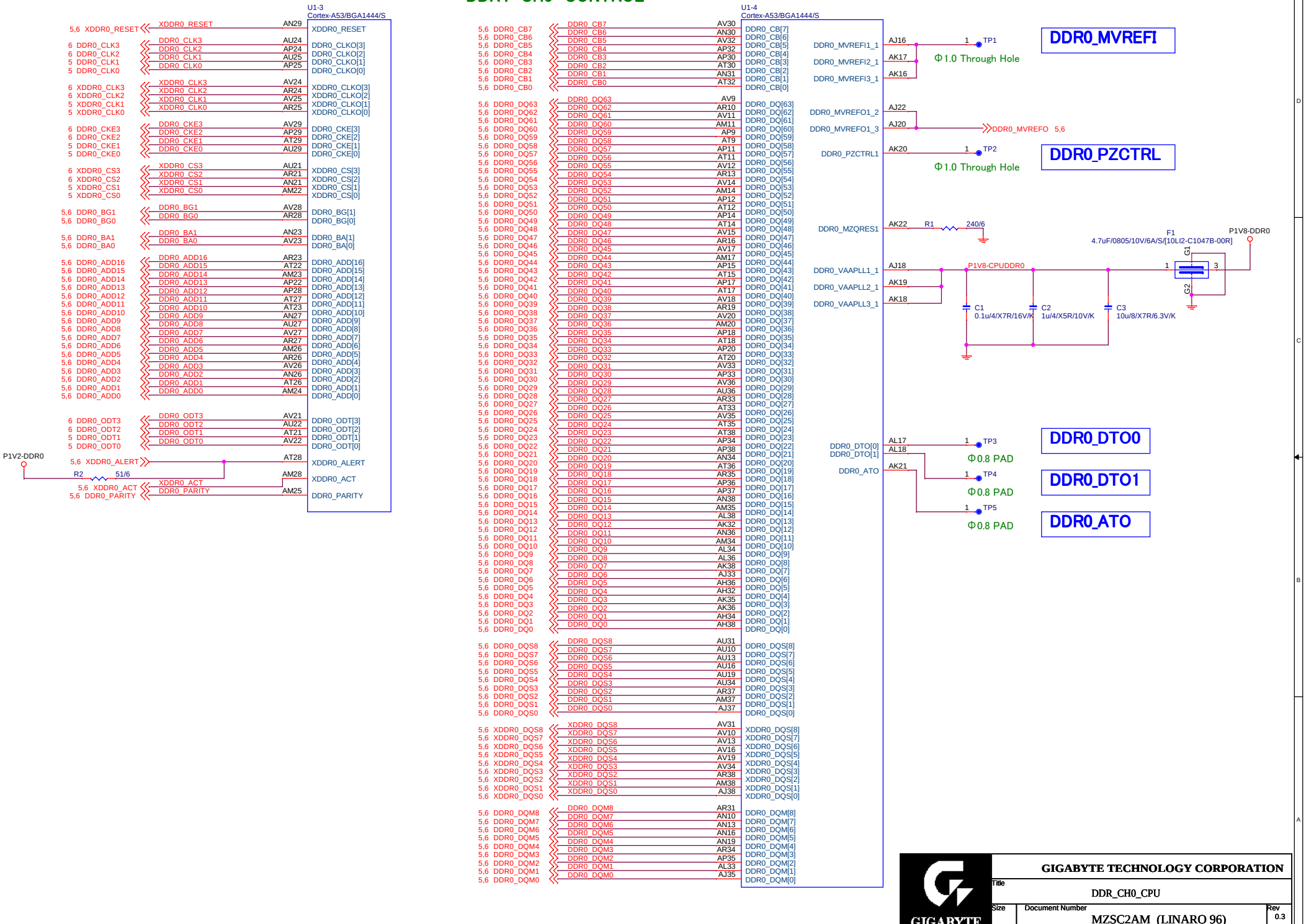
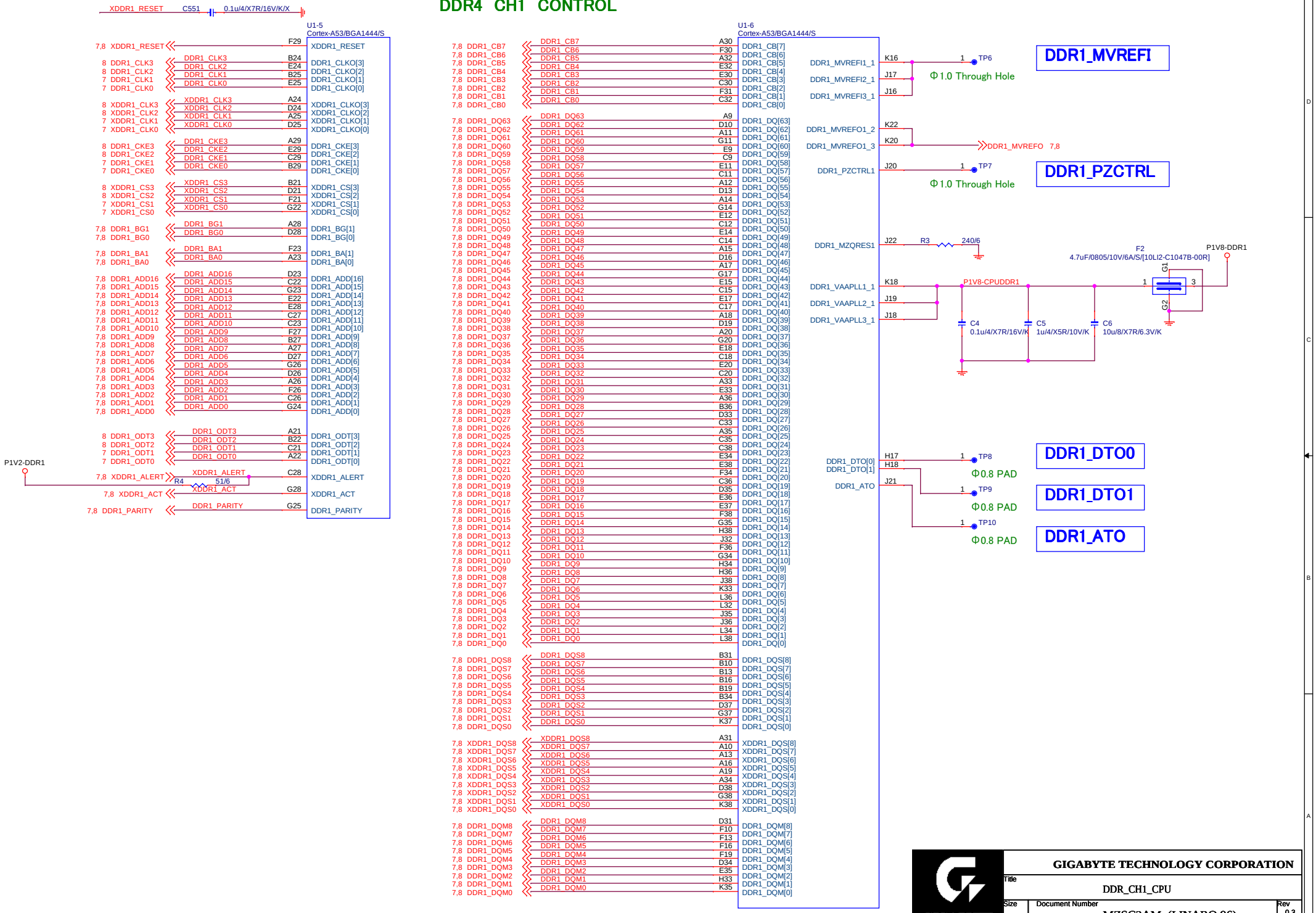
DDR4 CH0 CONTROL



GIGABYTE TECHNOLOGY CORPORATION	
Title	DDR_CH0_CPU
Size	Document Number: MZSC2AM_(LINARO 96) — Rev: 0.3
Date: Monday, January 15, 2018	Sheet 3 of 36

DDR4 CH1 CONTROL



Title	DDR_CH1_CPU
Size	Document Number: MZSC2AM_(LINARO 96)
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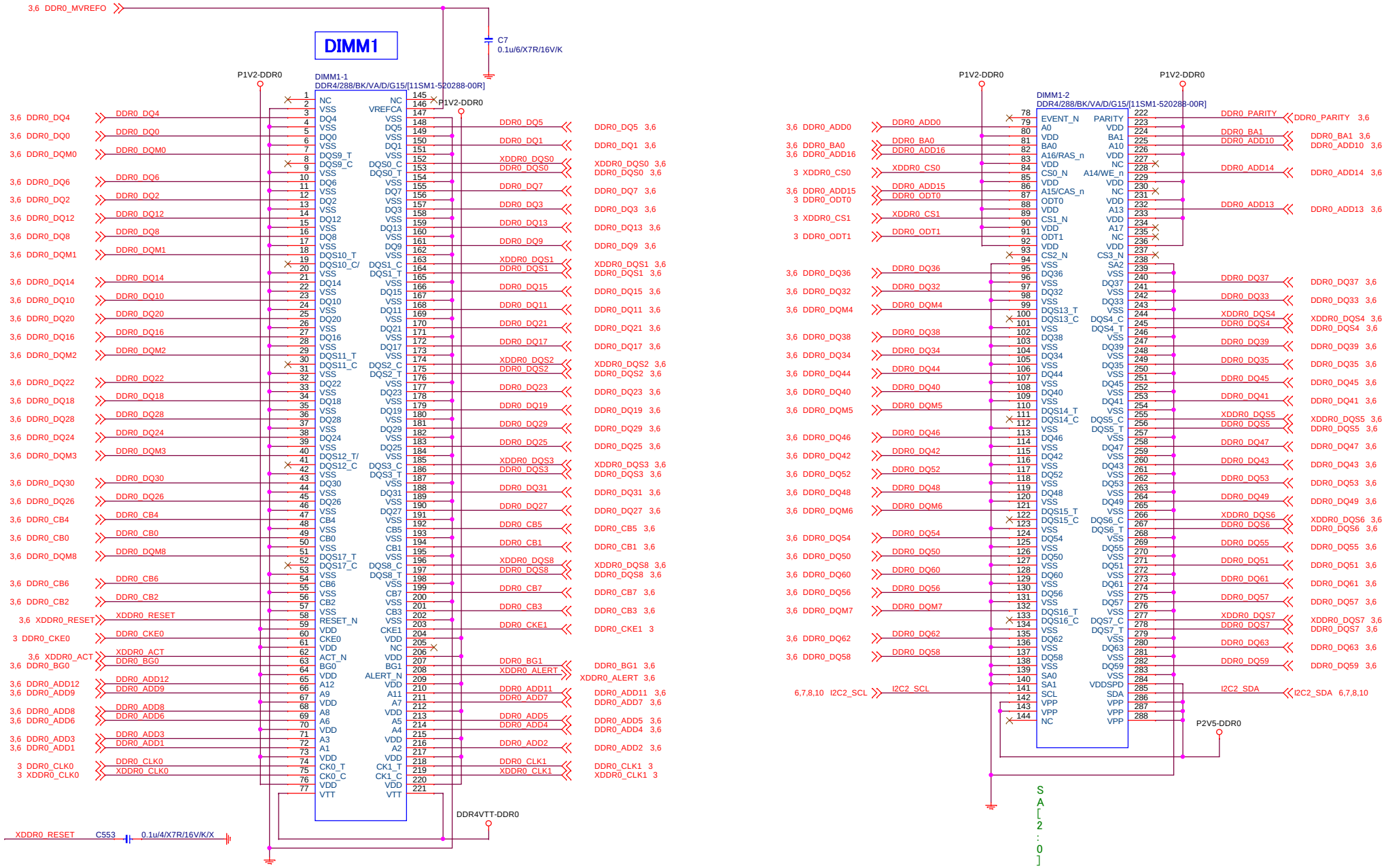
GIGABYTE TECHNOLOGY CORPORATION



Company	GIGABYTE TECHNOLOGY CORPORATION
Title	DDR_CH0_DIMM_1
Size	
Document Number	MZSC2AM_(LINARO 96)
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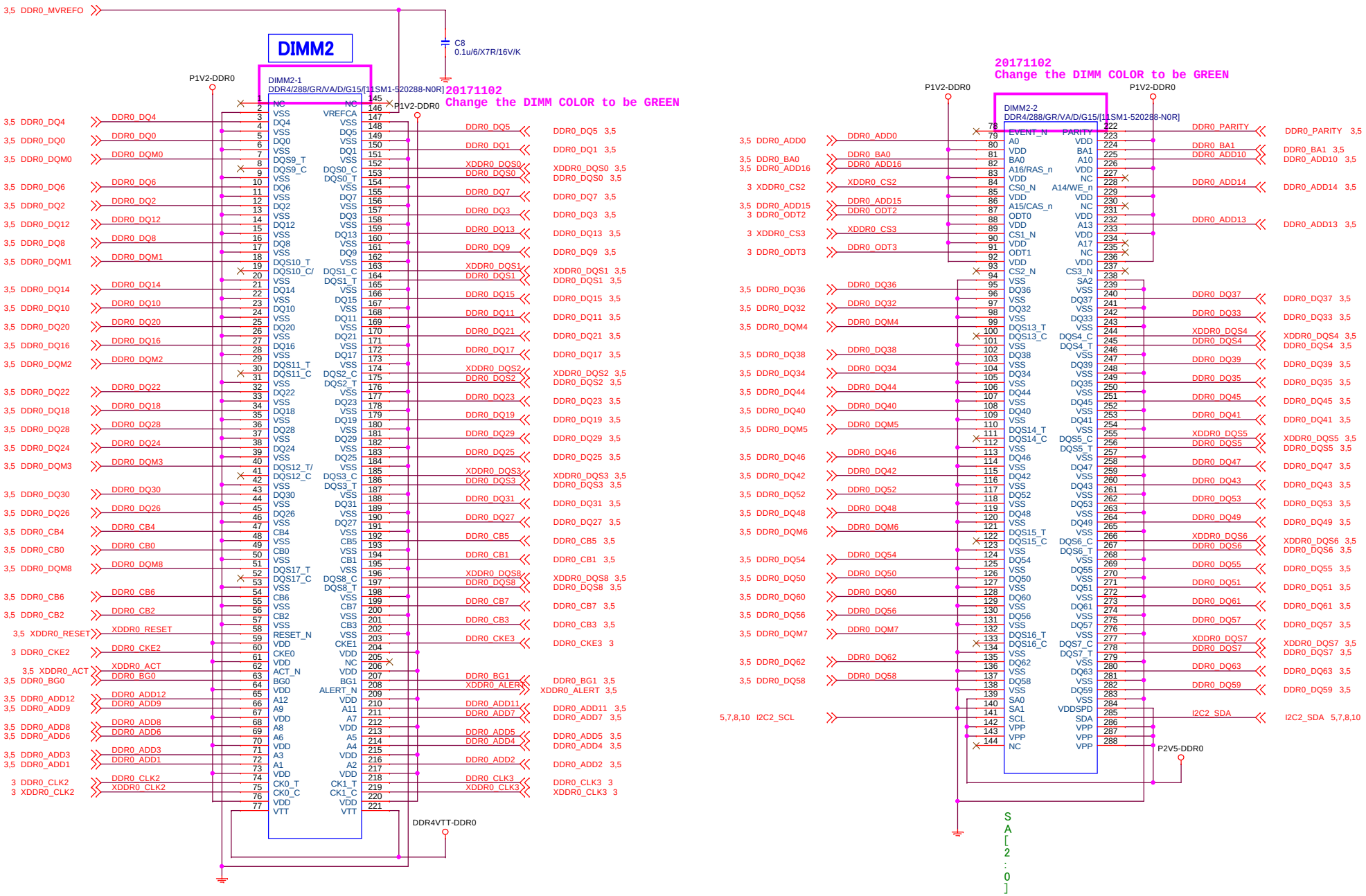
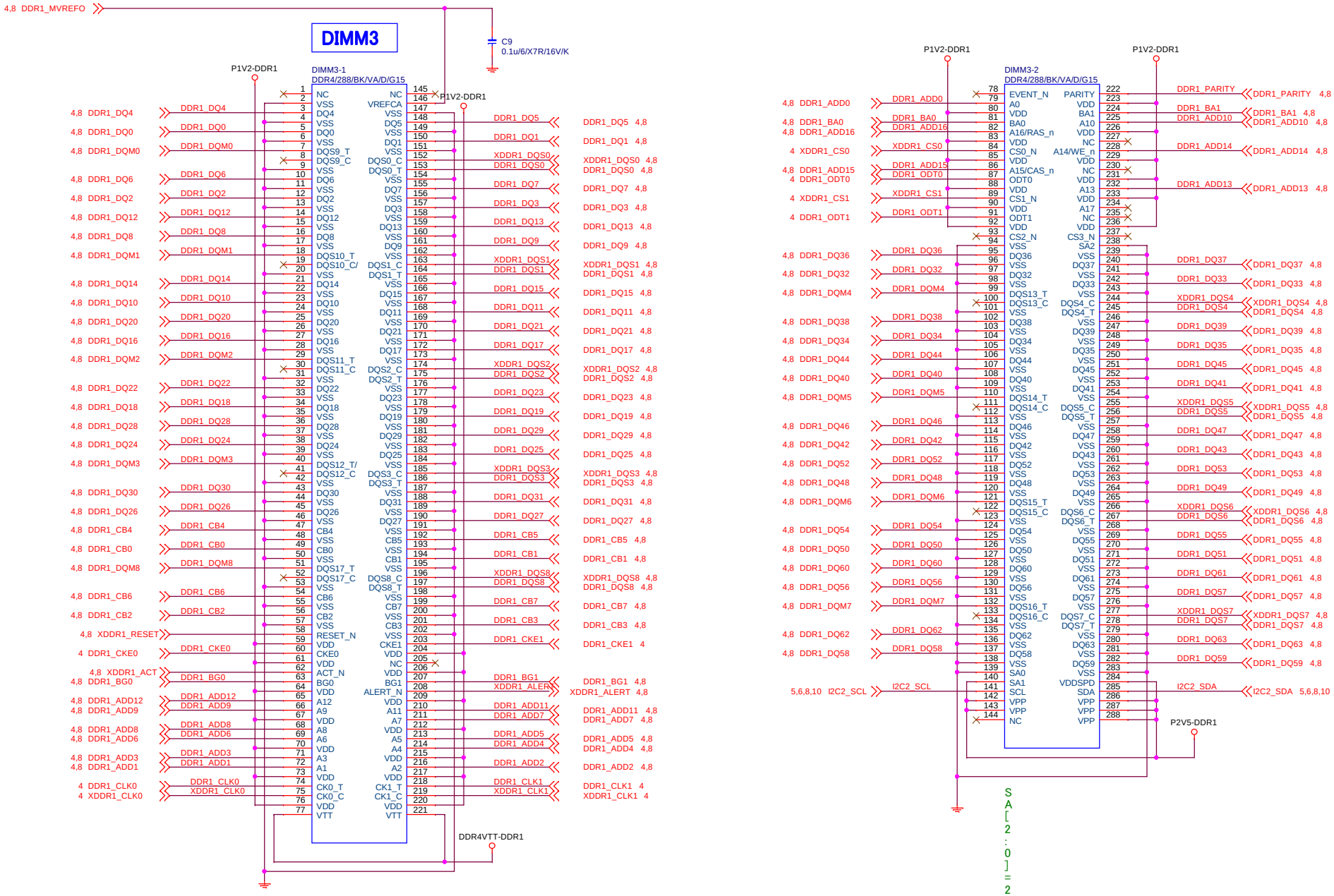
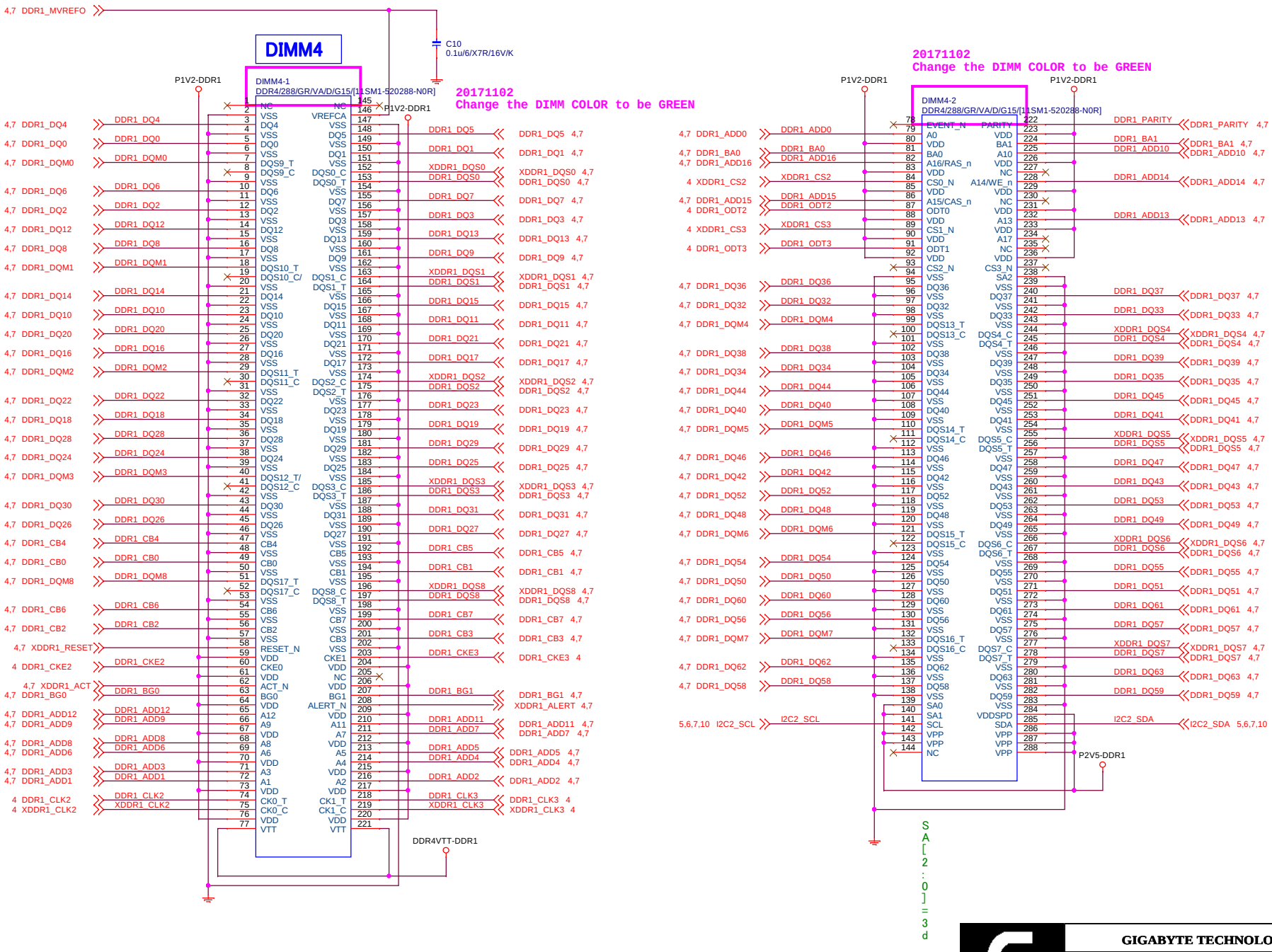


GIGABYTE TECHNOLOGY CORPORATION		
Title: DDR_CH0_DIMM_2		
Size	Document Number: MZSC2AM_(LINARO 96)	Rev: 0.3
Date: Monday, January 15, 2018	Sheet 6 of 36	



GIGABYTE TECHNOLOGY CORPORATION

Title	DDR_CH1_DIMM_1	
Size	Document Number: MZSC2AM_(LINARO 96)	Rev: 0.3
Date: Monday, January 15, 2018	Sheet 7 of 36	



GIGABYTE	GIGABYTE TECHNOLOGY CORPORATION	
	Title: DDR_CH1_DIMM_2	
	Size	Document Number: MZSC2AM_(LINARO 96) Rev: 0.3
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20171102
Modify the HSSPI0&CSO1,
and connect them to EEPROM

20171102
Add pull high resistor

20171117
Modify SPI

20171102
PIN3 modify to be pull high.

20171117
Modify SPI

20171102
DELETE TP38~TP41,
and connect these signals to LS connector

20171102
Add SPI EEPROM
(MX25L5121EMC-20G or MX25L512EMI-10G)

MX25U51245GMI00 1.8V, 512Mbit, x1/x2/x4, 16pin-SOP(300mil)

SPI- NOR FLASH

J-TAG

eMMC-NAND

20171102
BOM MODIFY to be 8GB EMMC

Title	SPI Flash_eMMC
Size	Document Number: MZSC2AM_(LINARO 96) Rev: 0.3
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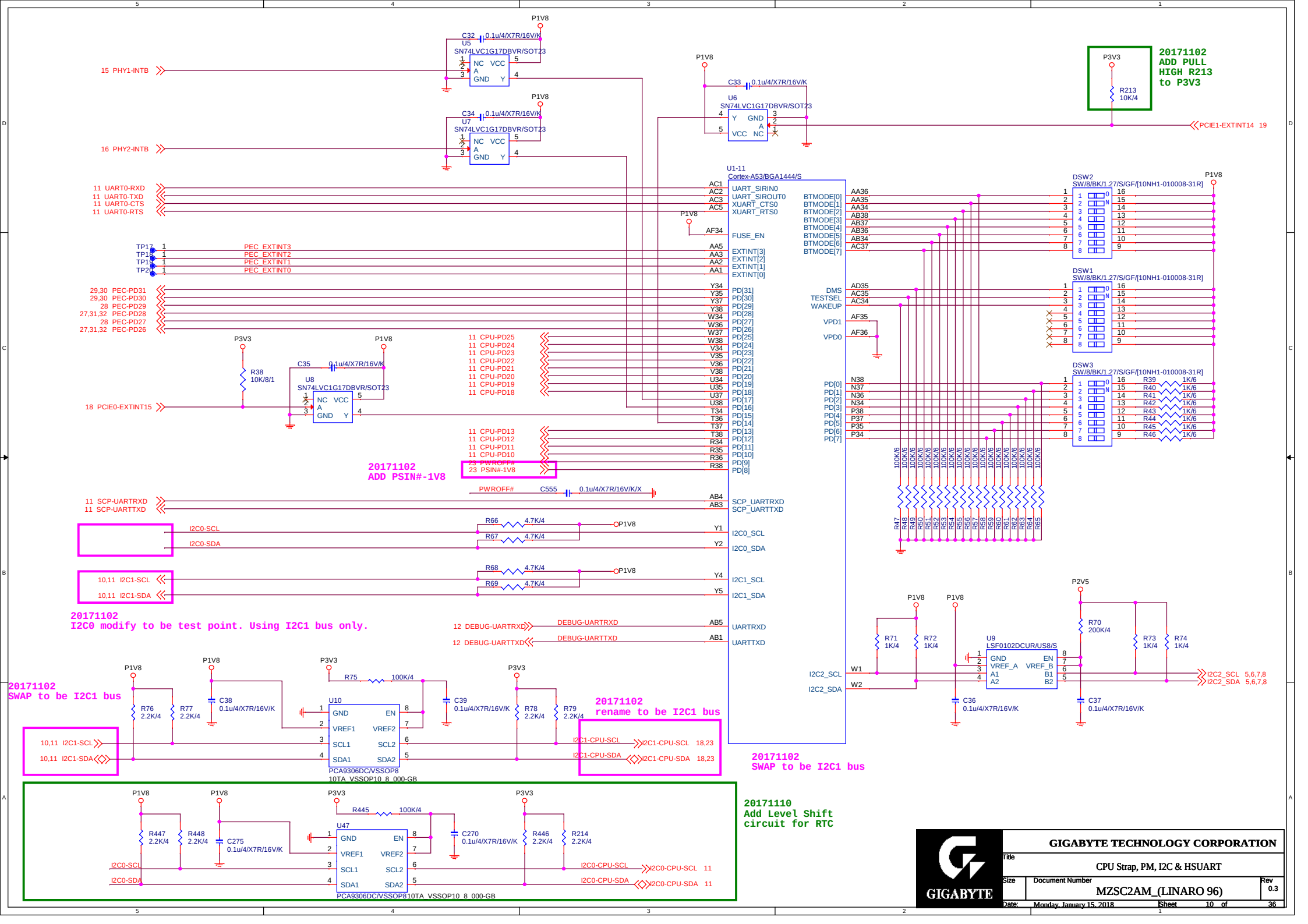
GIGABYTE TECHNOLOGY CORPORATION


20171102
ADD PULL HIGH R213 to P3V3
20171102
ADD PSIN#-1V8
20171102
I2C0 modify to be test point. Using I2C1 bus only.
20171102
SWAP to be I2C1 bus
20171102
rename to be I2C1 bus
20171102
SWAP to be I2C1 bus
20171110
Add Level Shift circuit for RTC
U1-11
Cortex-A53/BGA1444/S
SN74LVC1G17DBVR/SOT23
PCA9306DC/VSSOP8
10TA_VSSOP10_8_000-GB
LSF0102DCUR/US8/S
DSW1
DSW2
DSW3
SW/8/BK/1.27/S/GF/[10NH1-010008-31R]
GIGABYTE TECHNOLOGY CORPORATION
Title
CPU Strap, PM, I2C & HSUART
Size
Document Number
MZSC2AM_(LINARO 96)
Rev
0.3
Date:
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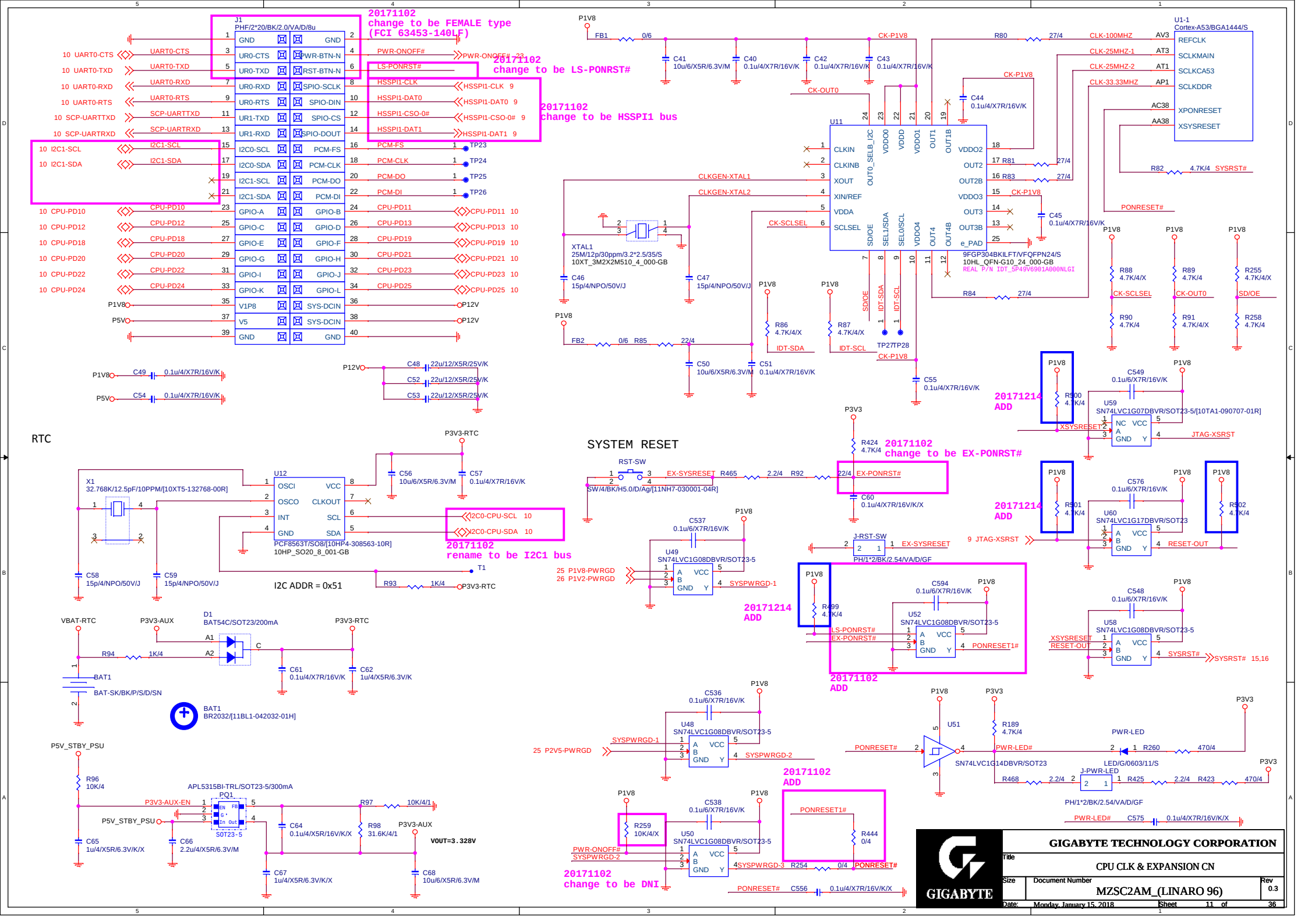
36


J1
PHF/2*20/BK/2.0/VA/D/8u
20171102
change to be FEMALE type
(FCI 63453-140LF)
20171102
change to be LS-PONRST#
20171102
change to be HSSPI1 bus
20171102
rename to be I2C1 bus
RTC
I2C ADDR = 0x51
SYSTEM RESET
20171102
change to be EX-PONRST#
20171214
ADD
20171102
ADD
20171102
change to be DNI
U1-1
Cortex-A53/BGA1444/S
U11
9FGP304BKILFT/VFQFPN24/S
10HL_QFN-G10_24_000-GB
REAL P/N IDT_5P49V6901A000NLGI
XTAL1
25M/12p/30ppm/3.2*2.5/35/S
10XT_3M2X2M510_4_000-GB
U12
PCF8563T/SO8/[10HP4-308563-10R]
10HP_SO20_8_001-GB
X1
32.768K/12.5pF/10PPM/[10XT5-132768-00R]
D1
BAT54C/SOT23/200mA
BAT1
BR2032/[11BL1-042032-01H]
BAT-SK/BK/P/S/D/SN
PQ1
APL5315BI-TRL/SOT23-5/300mA
VOUT=3.328V
RST-SW
SW/4/BK/H5.0/D/Ag/[11NH7-030001-04R]
J-RST-SW
PH/1*2/BK/2.54/VA/D/GF
J-PWR-LED
U59
SN74LVC1G07DBVR/SOT23-5/[10TA1-090707-01R]
U60
SN74LVC1G17DBVR/SOT23
U49
SN74LVC1G08DBVR/SOT23-5
U52
SN74LVC1G08DBVR/SOT23-5
U48
SN74LVC1G08DBVR/SOT23-5
U50
SN74LVC1G08DBVR/SOT23-5
U58
SN74LVC1G08DBVR/SOT23-5
U51
SN74LVC1G14DBVR/SOT23
LED/G/0603/11/S
GIGABYTE TECHNOLOGY CORPORATION
Title
CPU CLK & EXPANSION CN
Size
Document Number
MZSC2AM_(LINARO 96)
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0.3
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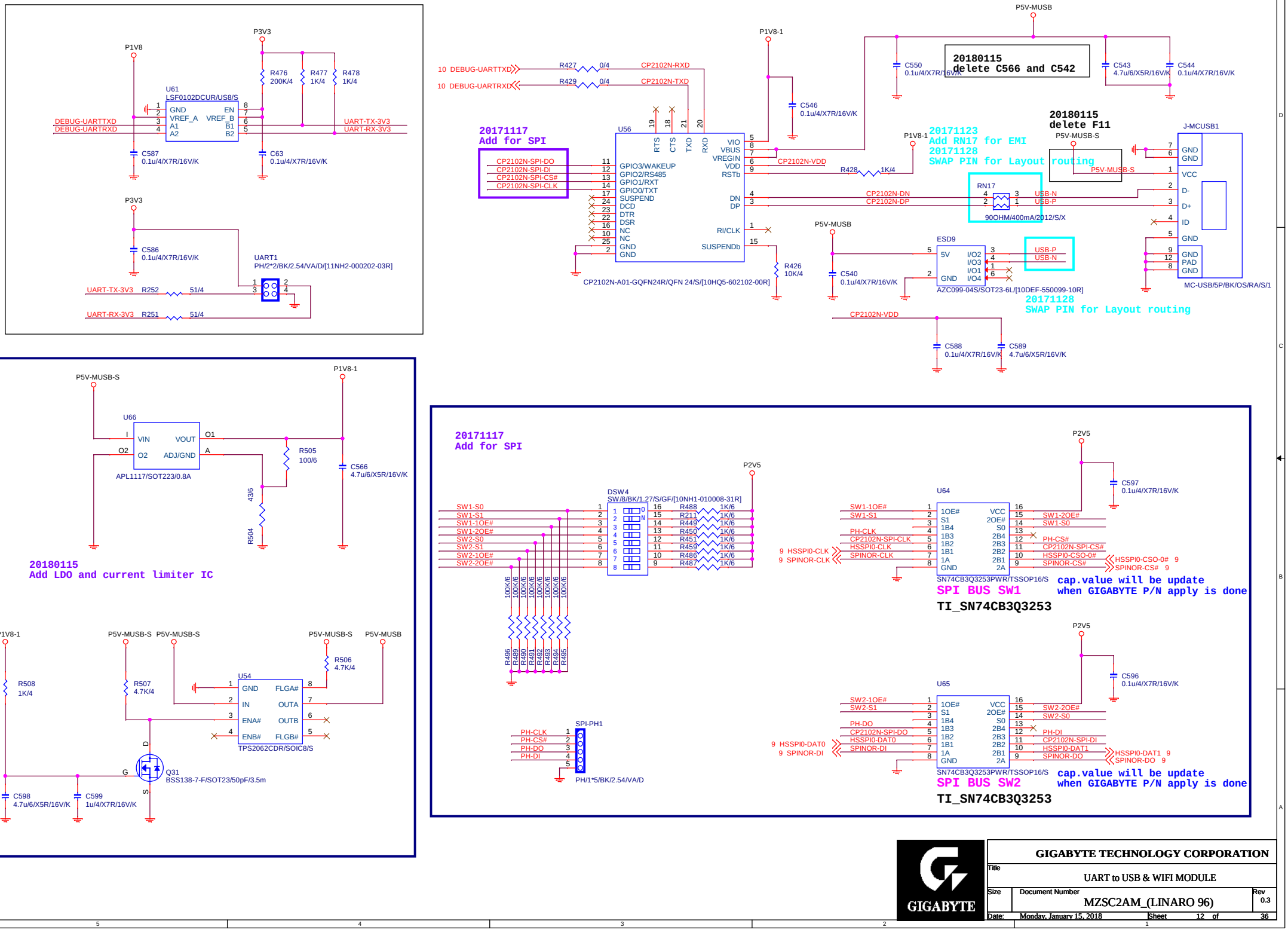

GIGABYTE TECHNOLOGY CORPORATION	
Title	UART to USB & WIFI MODULE
Size	Document Number: MZSC2AM_(LINARO 96) — Rev: 0.3
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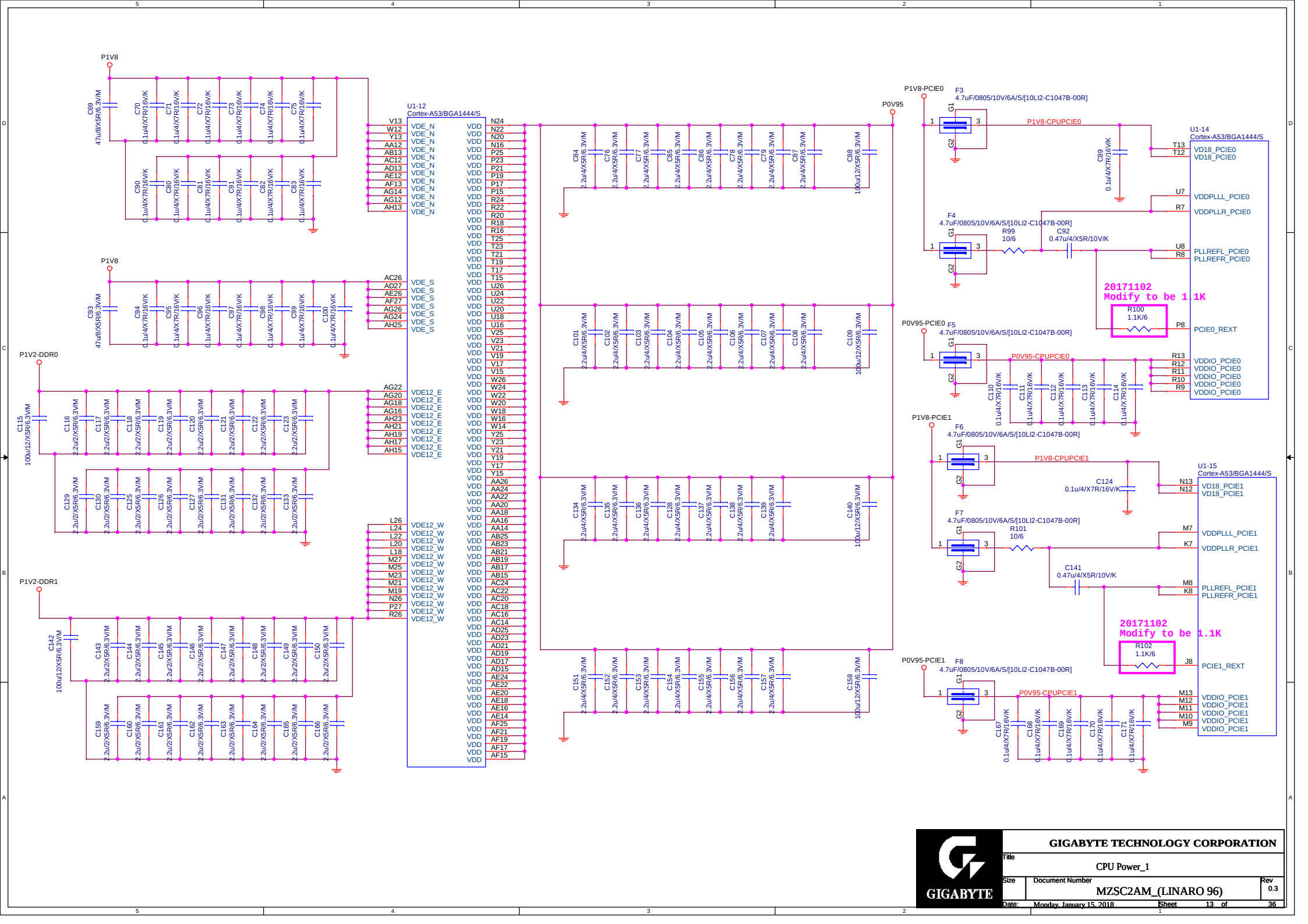
P1V8
C69 47u/8/X5R/6.3V/M
C70 0.1u/4/X7R/16V/K
C71 0.1u/4/X7R/16V/K
C72 0.1u/4/X7R/16V/K
C73 0.1u/4/X7R/16V/K
C74 0.1u/4/X7R/16V/K
C75 0.1u/4/X7R/16V/K
C90 0.1u/4/X7R/16V/K
C80 0.1u/4/X7R/16V/K
C81 0.1u/4/X7R/16V/K
C91 0.1u/4/X7R/16V/K
C82 0.1u/4/X7R/16V/K
C83 0.1u/4/X7R/16V/K
U1-12
Cortex-A53/BGA1444/S
V13 W12 Y13 AA12 AB13 AC12 AD13 AE12 AF13 AG14 AG12 AH13
VDE_N
P1V8
C93 47u/8/X5R/6.3V/M
C94 0.1u/4/X7R/16V/K
C95 0.1u/4/X7R/16V/K
C96 0.1u/4/X7R/16V/K
C97 0.1u/4/X7R/16V/K
C98 0.1u/4/X7R/16V/K
C99 0.1u/4/X7R/16V/K
C100 0.1u/4/X7R/16V/K
AC26 AD27 AE26 AF27 AG26 AG24 AH25
VDE_S
P1V2-DDR0
C115 100u/12/X5R/6.3V/M
C116 C117 C118 C119 C120 C121 C122 C123 2.2u/2/X5R/6.3V/M
C129 C130 C125 C126 C127 C131 C132 C133 2.2u/2/X5R/6.3V/M
AG22 AG20 AG18 AG16 AH23 AH21 AH19 AH17 AH15
VDE12_E
P1V2-DDR1
C142 100u/12/X5R/6.3V/M
C143 C144 C145 C146 C147 C148 C149 C150 2.2u/2/X5R/6.3V/M
C159 C160 C161 C162 C163 C164 C165 C166 2.2u/2/X5R/6.3V/M
L26 L24 L22 L20 L18 M27 M25 M23 M21 M19 N26 P27 R26
VDE12_W
VDD
N24 N22 N20 N16 P25 P23 P21 P19 P17 P15 R24 R22 R20 R18 R16 T25 T23 T21 T19 T17 T15 U26 U24 U22 U20 U18 U16 V25 V23 V21 V19 V17 V15 W26 W24 W22 W20 W18 W16 W14 Y25 Y23 Y21 Y19 Y17 Y15 AA26 AA24 AA22 AA20 AA18 AA16 AA14 AB25 AB23 AB21 AB19 AB17 AB15 AC24 AC22 AC20 AC18 AC16 AC14 AD25 AD23 AD21 AD19 AD17 AD15 AE24 AE22 AE20 AE18 AE16 AE14 AF25 AF21 AF19 AF17 AF15
P0V95
C84 C76 C77 C85 C86 C78 C79 C87 2.2u/4/X5R/6.3V/M
C88 100u/12/X5R/6.3V/M
C101 C102 C103 C104 C105 C106 C107 C108 2.2u/4/X5R/6.3V/M
C109 100u/12/X5R/6.3V/M
C134 C135 C136 C128 C137 C138 C139 2.2u/4/X5R/6.3V/M
C140 100u/12/X5R/6.3V/M
C151 C152 C153 C154 C155 C156 C157 2.2u/4/X5R/6.3V/M
C158 100u/12/X5R/6.3V/M
P1V8-PCIE0
F3 4.7uF/0805/10V/6A/S/[10LI2-C1047B-00R]
P1V8-CPUPCIE0
C89 0.1u/4/X7R/16V/K
U1-14
Cortex-A53/BGA1444/S
T13 T12
VD18_PCIE0
U7
VDDPLLL_PCIE0
R7
VDDPLLR_PCIE0
F4 4.7uF/0805/10V/6A/S/[10LI2-C1047B-00R]
R99 10/6
C92 0.47u/4/X5R/10V/K
U8 R8
PLLREFL_PCIE0
PLLREFR_PCIE0
20171102
Modify to be 1 1K
R100 1.1K/6
P8
PCIE0_REXT
P0V95-PCIE0
F5 4.7uF/0805/10V/6A/S/[10LI2-C1047B-00R]
P0V95-CPUPCIE0
C110 C111 C112 C113 C114 0.1u/4/X7R/16V/K
R13 R12 R11 R10 R9
VDDIO_PCIE0
P1V8-PCIE1
F6 4.7uF/0805/10V/6A/S/[10LI2-C1047B-00R]
P1V8-CPUPCIE1
C124 0.1u/4/X7R/16V/K
U1-15
Cortex-A53/BGA1444/S
N13 N12
VD18_PCIE1
F7 4.7uF/0805/10V/6A/S/[10LI2-C1047B-00R]
R101 10/6
M7
VDDPLLL_PCIE1
K7
VDDPLLR_PCIE1
C141 0.47u/4/X5R/10V/K
M8 K8
PLLREFL_PCIE1
PLLREFR_PCIE1
20171102
Modify to be 1.1K
R102 1.1K/6
J8
PCIE1_REXT
P0V95-PCIE1
F8 4.7uF/0805/10V/6A/S/[10LI2-C1047B-00R]
P0V95-CPUPCIE1
C167 C168 C169 C170 C171 0.1u/4/X7R/16V/K
M13 M12 M11 M10 M9
VDDIO_PCIE1
GIGABYTE TECHNOLOGY CORPORATION
Title
CPU Power_1
Size
Document Number
MZSC2AM_(LINARO 96)
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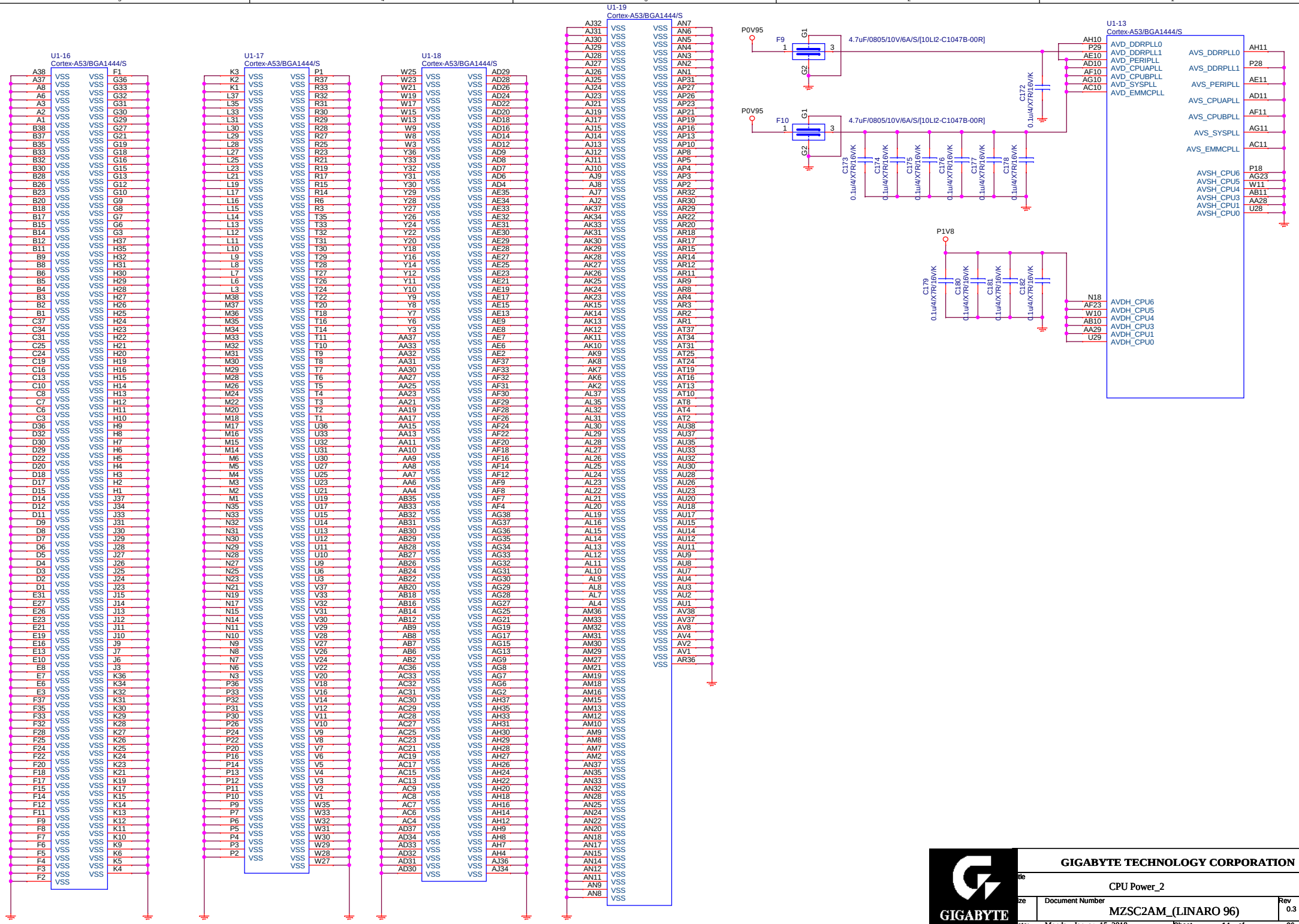

Company	GIGABYTE TECHNOLOGY CORPORATION
Title	CPU Power_2
Size	Document Number: MZSC2AM_(LINARO 96) Rev: 0.3
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PHY ADDRESS(AD2AD1AD0):011
TXDLY/RXDLY: 11 for Enable Delay
Auto-Negotiation(AN1AN0):11 for NWay. Advertise all capabilities
SELRGV:1 for RTL8211E-VL RGMII 1.8V

P3V3

R103 4.7K/4/X PHY1-LINK1000-AD1 R104 4.7K/4
R105 4.7K/4/X PHY1-LINK100-AD0 R106 4.7K/4
R107 4.7K/4/X PHY1-ACT-RXDLY R108 4.7K/4
R109 4.7K/4/X PHY1-RXD0-SELRGV R110 4.7K/4
R111 4.7K/4 PHY1-RXCTL-AD2 R112 4.7K/4/X
R113 4.7K/4/X PHY1-RXD2-AN0 R114 4.7K/4
R119 4.7K/4/X PHY1-RXD3-AN1 R115 4.7K/4
R117 4.7K/4/X PHY1-RXD1-TXDLY R118 4.7K/4

P1V8

P1V8
PHY1-AVDD33
PHY1-DVDD10
C183 0.1u/4/X7R/16V/K
C184 0.1u/4/X7R/16V/K
C185 0.1u/4/X7R/16V/K
C186 0.1u/4/X7R/16V/K
C187 0.1u/4/X7R/16V/K
C188 0.1u/4/X7R/16V/K
C189 0.1u/4/X7R/16V/K
C190 0.1u/4/X7R/16V/K
C191 0.1u/4/X7R/16V/K
PHY1-AVDD10

ET0-TXCLK C547 22p/4/NPO/50V/J/X
ET1-TXCLK C577 22p/4/NPO/50V/J/X

CPU I/F Level: 1.8V

U14
RTL8211E
RTL8211E-VL/QFN48/S

VDDREG 45,44
DVDD33 37,21,15
AVDD33 41,6
DVDD10 36,28
AVDD10 40,9,3

MDI[3]- 11
MDI[3]+ 10
MDI[2]- 8
MDI[2]+ 7
MDI[1]- 5
MDI[1]+ 4
MDI[0]- 2
MDI[0]+ 1

17 LAN1-MDI3N
17 LAN1-MDI3P
17 LAN1-MDI2N
17 LAN1-MDI2P
17 LAN1-MDI1N
17 LAN1-MDI1P
17 LAN1-MDI0N
17 LAN1-MDI0P

LED2_RXDLY 32
LED1/PHYAD1 34
LED0/PHYAD0 20
INTB

17 PHY1-ACT-RXDLY
17 PHY1-LINK1000-AD1
TP11
10 PHY1-INTB

CKXTAL1 42
CKXTAL2 43

XTAL2
25M/12p/30ppm/3.2*2.5/35/S
10XT_3M2X2M510_4_000-GB

C193 27p/4/NPO/50V/J
C194 27p/4/NPO/50V/J

GND 47
GND(EPAD) 49

CLK125 46
NC 12
ENSWREG 38

TXC 22 PHY1-TXCLK R116 22/4 ET0-TXCLK AM1 ET0_GTXCLK
TXD3 26 PHY1-TXD3 R120 22/4 ET0-TXD3 AM3 ET0_TXD[3]
TXD2 25 PHY1-TXD2 R129 22/4 ET0-TXD2 AM4 ET0_TXD[2]
TXD1 24 PHY1-TXD1 R121 22/4 ET0-TXD1 AM5 ET0_TXD[1]
TXD0 23 PHY1-TXD0 R122 22/4 ET0-TXD0 AM6 ET0_TXD[0]
TXCTL 27 PHY1-TXCTL R123 22/4 ET0-TXCTL AL6 ET0_TXEN
RXC 19 PHY1-RX-CLK R124 22/4 ET0-RXCLK AL1 ET0_RXCLK
RXD3/AN1 18 PHY1-RXD3-AN1 R125 22/4 ET0-RXD3 AL2 ET0_RXD[3]
RXD2/AN0 17 PHY1-RXD2-AN0 R130 22/4 ET0-RXD2 AL3 ET0_RXD[2]
RXD1/TXDLY 16 PHY1-RXD1-TXDLY R126 22/4 ET0-RXD1 AL5 ET0_RXD[1]
RXD0/SELRGV 14 PHY1-RXD0-SELRGV R127 22/4 ET0-RXD0 AK5 ET0_RXD[0]
RXCTL/PHYAD2 13 PHY1-RXCTL-AD2 R131 22/4 ET0-RXDV AK4 ET0_RXDV
MDC 30 PHY1-MDC-1V8 R128 0/4 ET0-MDC-1V8 AK1 ET0_MDCLK
MDIO 31 PHY1-MDIO-1V8 R134 0/4 ET0-MDIO-1V8 AK3 ET0_MDIO
PMEB 33 PHY1-PMEB R135 4.7K/4 P3V3
REGOUT 48 PHY1-REGOUT
PHYRSTB 29 PHY1-RSTB R137 0/4 SYSRST# 11,16
RSET 39 PHY1-RSET R139 2.49K/4/1

R253 1.5K/4 P1V8
R136 4.7K/4 P3V3

PHY1-RSTB C256 0.1u/4/X7R/16V/K/X

U1-9
Cortex-A53/BGA1444/S
ET0_GTXCLK
ET0_TXD[3]
ET0_TXD[2]
ET0_TXD[1]
ET0_TXD[0]
ET0_TXEN
ET0_RXCLK
ET0_RXD[3]
ET0_RXD[2]
ET0_RXD[1]
ET0_RXD[0]
ET0_RXDV
ET0_MDCLK
ET0_MDIO

16 PHY2-TXCLK R140 22/4 ET1-TXCLK AJ1 ET1_GTXCLK
16 PHY2-TXD3 R141 22/4 ET1-TXD3 AJ3 ET1_TXD[3]
16 PHY2-TXD2 R142 22/4 ET1-TXD2 AJ4 ET1_TXD[2]
16 PHY2-TXD1 R143 22/4 ET1-TXD1 AJ5 ET1_TXD[1]
16 PHY2-TXD0 R144 22/4 ET1-TXD0 AJ6 ET1_TXD[0]
16 PHY2-TXCTL R145 22/4 ET1-TXCTL AH6 ET1_TXEN
16 ET1-RXCLK ET1-RXCLK AH1 ET1_RXCLK
16 ET1-RXD3 ET1-RXD3 AH2 ET1_RXD[3]
16 ET1-RXD2 ET1-RXD2 AH3 ET1_RXD[2]
16 ET1-RXD1 ET1-RXD1 AH5 ET1_RXD[1]
16 ET1-RXD0 ET1-RXD0 AG5 ET1_RXD[0]
16 ET1-RXCTL ET1-RXCTL AG4 ET1_RXDV
16 ET1-MDC-1V8 ET1-MDC-1V8 AG1 ET1_MDCLK
16 ET1-MDIO-1V8 ET1-MDIO-1V8 AG3 ET1_MDIO

PHY1-RX-CLK C202 22p/4/NPO/50V/J/X

R435 1.5K/4 P1V8

FB3 0/6
C192 0.1u/4/X7R/16V/K
R132 4.7K/4
PHY1-INTB
C557 0.1u/4/X7R/16V/K/X
R133 1M/4/1/X

1.05V Power

Note 1: The Trace length between L1 and PHY's Pin48 must be within 0.5 cm. C841 and C842 to L1 must be within 0.5cm.

L1 2.2uH/1.44A/S/60m/F
RTL8211D:C2546= 22uF(X5R)
RTL8211E:C2546= 4.7/22uF(X5R)
PHY1-REGOUT
R146 0/6
C195 4.7u/6/X5R/16V/K
C196 0.1u/4/X7R/16V/K

RTL8211D: L1= 4.7uH
RTL8211E: L1= 2.2/4.7uH

3.3V Power

BC1 22u/8/X5R/6.3V/M
C197 0.1u/4/X7R/16V/K
C198
C199
C200
C201
0.1u/4/X7R/16V/K

R147 0/6

VDDREG

Note 2: The Trace length from C2251, C2252 to Pin 44,45(VDDREG) must be within 0.5 cm. The trace width from AVDD33 to Pin 44,45 should>40mils

R148 0/6
C204 4.7u/6/X5R/16V/K
C205 0.1u/4/X7R/16V/K

GIGABYTE TECHNOLOGY CORPORATION

Title: ETHERNET RTL8211E_1

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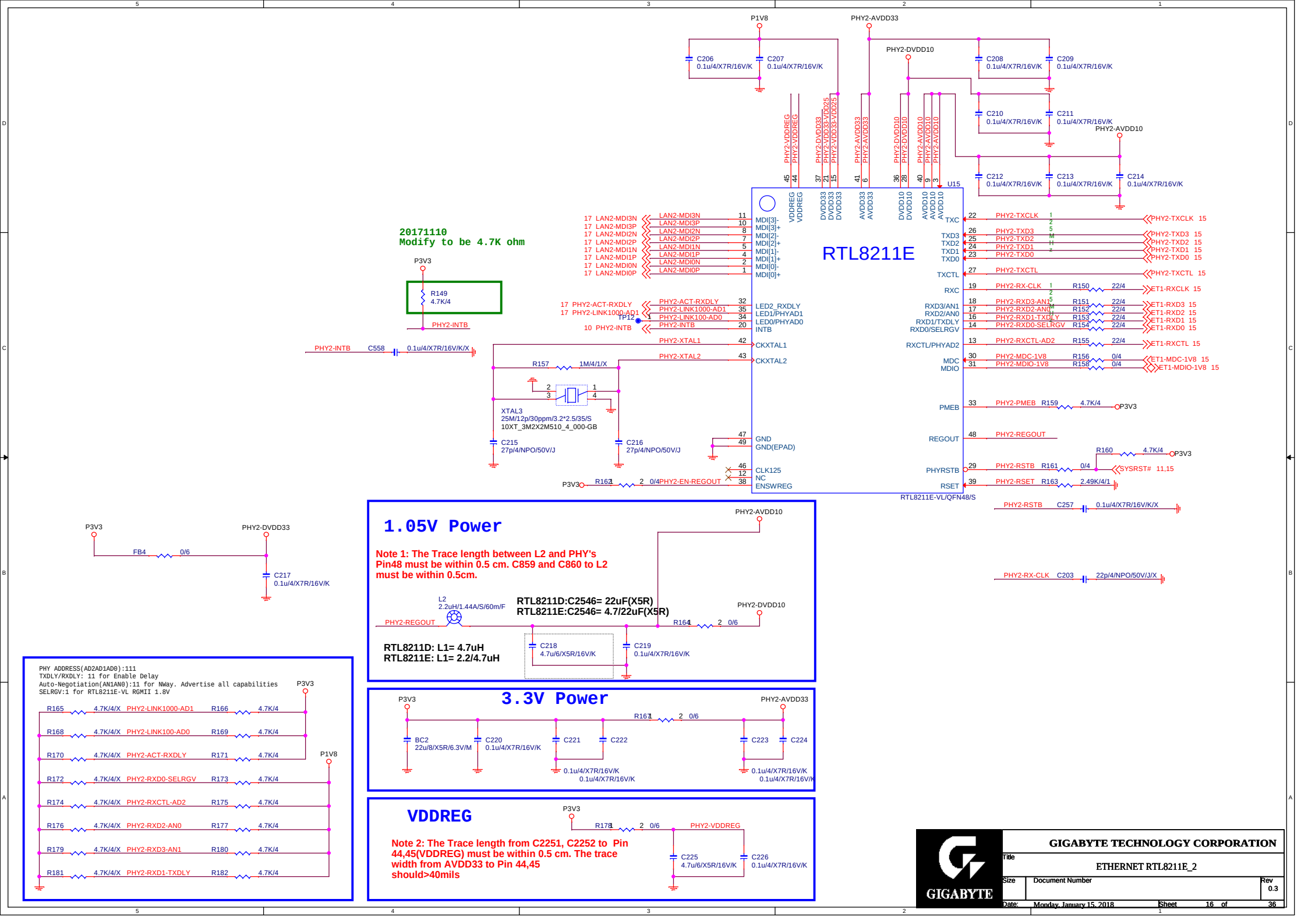
20171110
Modify to be 4.7K ohm
RTL8211E
RTL8211E-VL/QFN48/S
1.05V Power
Note 1: The Trace length between L2 and PHY's Pin48 must be within 0.5 cm. C859 and C860 to L2 must be within 0.5cm.
RTL8211D:C2546= 22uF(X5R)
RTL8211E:C2546= 4.7/22uF(X5R)
RTL8211D: L1= 4.7uH
RTL8211E: L1= 2.2/4.7uH
3.3V Power
VDDREG
Note 2: The Trace length from C2251, C2252 to Pin 44,45(VDDREG) must be within 0.5 cm. The trace width from AVDD33 to Pin 44,45 should>40mils
PHY ADDRESS(AD2AD1AD0):111
TXDLY/RXDLY: 11 for Enable Delay
Auto-Negotiation(AN1AN0):11 for NWay. Advertise all capabilities
SELRGV:1 for RTL8211E-VL RGMII 1.8V
GIGABYTE TECHNOLOGY CORPORATION
ETHERNET RTL8211E_2
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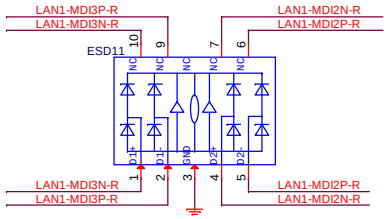
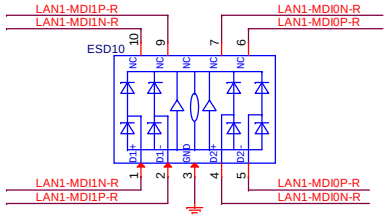
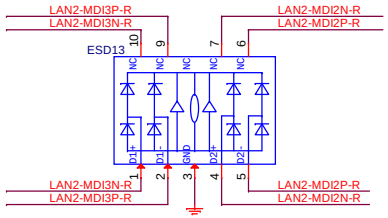


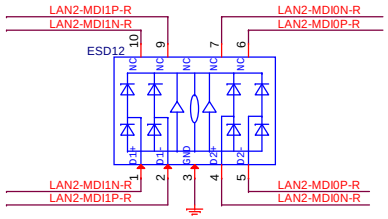
AZ1045-04F/MSOP10/[10DE2-501045-10R_10DE2-543012-00R_10DE2-551004-00R]



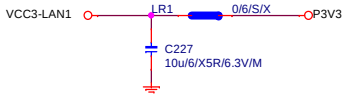
AZ1045-04F/MSOP10/[10DE2-501045-10R_10DE2-543012-00R_10DE2-551004-00R]

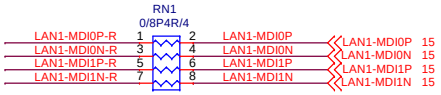


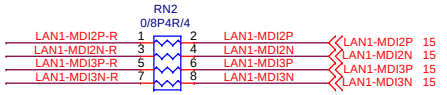
AZ1045-04F/MSOP10/[10DE2-501045-10R_10DE2-543012-00R_10DE2-551004-00R]

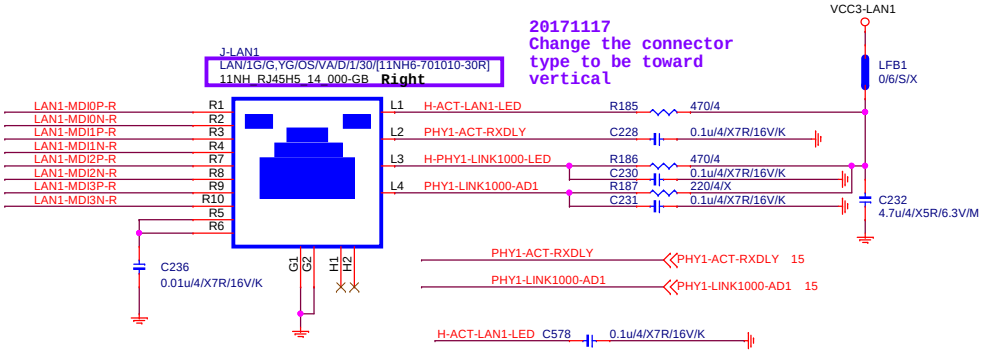


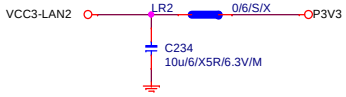
AZ1045-04F/MSOP10/[10DE2-501045-10R_10DE2-543012-00R_10DE2-551004-00R]

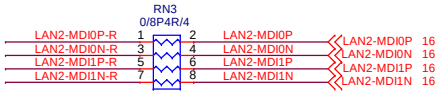


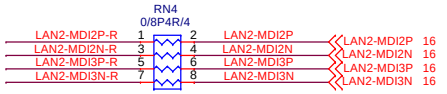


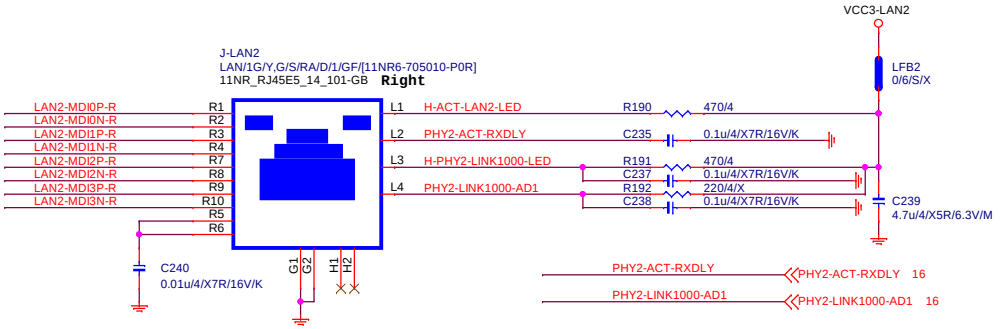












GIGABYTE TECHNOLOGY CORPORATION

Title	ETHERNET RTL8211E_3	
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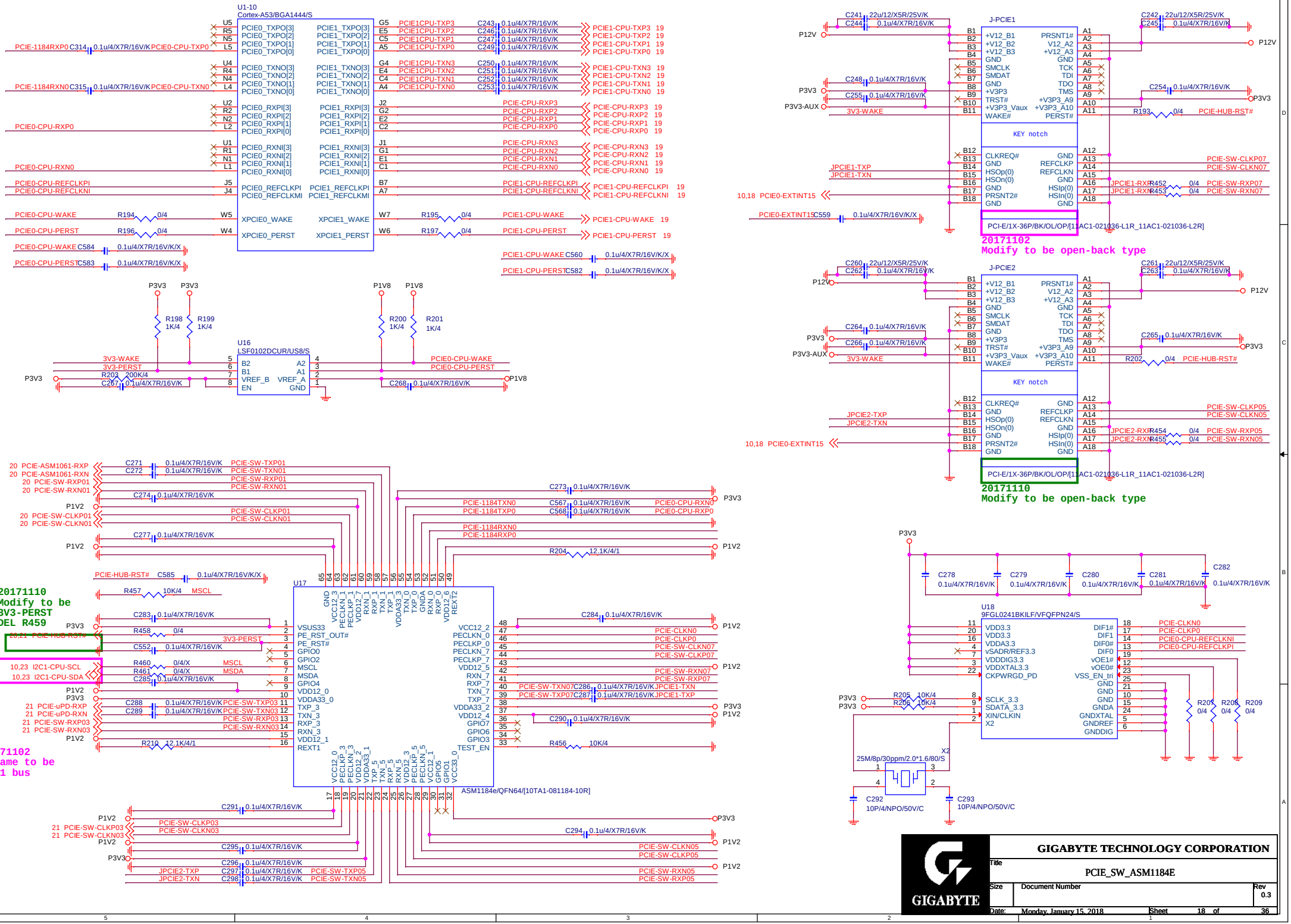
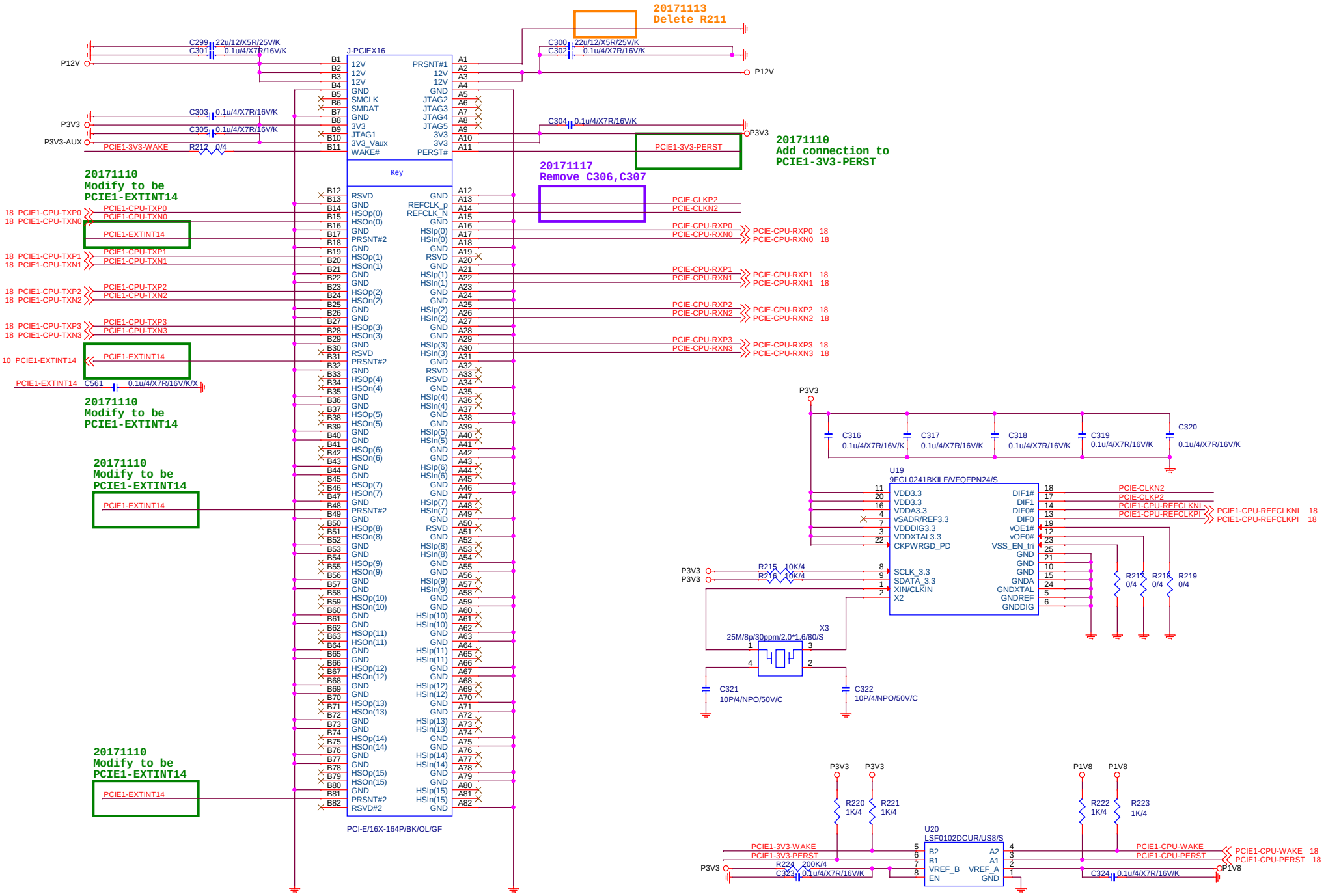

U1-10
Cortex-A53/BGA1444/S
PCIE-1184RXP0 C314 0.1u/4/X7R/16V/K PCIE0-CPU-TXP0
PCIE-1184RXN0 C315 0.1u/4/X7R/16V/K PCIE0-CPU-TXN0
PCIE0-CPU-RXP0
PCIE0-CPU-RXN0
PCIE0-CPU-REFCLKPI
PCIE0-CPU-REFCLKNI
PCIE0-CPU-WAKE R194 0/4
PCIE0-CPU-PERST R196 0/4
PCIE0-CPU-WAKE C584 0.1u/4/X7R/16V/K/X
PCIE0-CPU-PERST C583 0.1u/4/X7R/16V/K/X
PCIE1-CPU-WAKE C560 0.1u/4/X7R/16V/K/X
PCIE1-CPU-PERST C582 0.1u/4/X7R/16V/K/X
PCIE1-CPU-TXP3 C243 0.1u/4/X7R/16V/K PCIE1-CPU-TXP3 19
PCIE1-CPU-TXP2 C246 0.1u/4/X7R/16V/K PCIE1-CPU-TXP2 19
PCIE1-CPU-TXP1 C247 0.1u/4/X7R/16V/K PCIE1-CPU-TXP1 19
PCIE1-CPU-TXP0 C249 0.1u/4/X7R/16V/K PCIE1-CPU-TXP0 19
PCIE1-CPU-TXN3 C250 0.1u/4/X7R/16V/K PCIE1-CPU-TXN3 19
PCIE1-CPU-TXN2 C251 0.1u/4/X7R/16V/K PCIE1-CPU-TXN2 19
PCIE1-CPU-TXN1 C252 0.1u/4/X7R/16V/K PCIE1-CPU-TXN1 19
PCIE1-CPU-TXN0 C253 0.1u/4/X7R/16V/K PCIE1-CPU-TXN0 19
PCIE-CPU-RXP3 PCIE-CPU-RXP3 19
PCIE-CPU-RXP2 PCIE-CPU-RXP2 19
PCIE-CPU-RXP1 PCIE-CPU-RXP1 19
PCIE-CPU-RXP0 PCIE-CPU-RXP0 19
PCIE-CPU-RXN3 PCIE-CPU-RXN3 19
PCIE-CPU-RXN2 PCIE-CPU-RXN2 19
PCIE-CPU-RXN1 PCIE-CPU-RXN1 19
PCIE-CPU-RXN0 PCIE-CPU-RXN0 19
PCIE1-CPU-REFCLKPI PCIE1-CPU-REFCLKPI 19
PCIE1-CPU-REFCLKNI PCIE1-CPU-REFCLKNI 19
PCIE1-CPU-WAKE R195 0/4 PCIE1-CPU-WAKE PCIE1-CPU-WAKE 19
PCIE1-CPU-PERST R197 0/4 PCIE1-CPU-PERST PCIE1-CPU-PERST 19
U16
LSF0102DCUR/US8/S
3V3-WAKE
3V3-PERST
R203 200K/4
C267 0.1u/4/X7R/16V/K
R198 1K/4
R199 1K/4
R200 1K/4
R201 1K/4
C268 0.1u/4/X7R/16V/K
PCIE0-CPU-WAKE
PCIE0-CPU-PERST
J-PCIE1
C241 22u/12/X5R/25V/K
C244 0.1u/4/X7R/16V/K
C242 22u/12/X5R/25V/K
C245 0.1u/4/X7R/16V/K
C248 0.1u/4/X7R/16V/K
C255 0.1u/4/X7R/16V/K
C254 0.1u/4/X7R/16V/K
R193 0/4 PCIE-HUB-RST#
KEY notch
JPCIE1-TXP
JPCIE1-TXN
JPCIE1-RXP R452 0/4 PCIE-SW-RXP07
JPCIE1-RXN R453 0/4 PCIE-SW-RXN07
PCIE-SW-CLKP07
PCIE-SW-CLKN07
10,18 PCIE0-EXTINT15
PCIE0-EXTINT15 C559 0.1u/4/X7R/16V/K/X
PCI-E/1X-36P/BK/OL/OP/[11AC1-021AC1-L1R_11AC1-L2R]
20171102
Modify to be open-back type
J-PCIE2
C260 22u/12/X5R/25V/K
C262 0.1u/4/X7R/16V/K
C261 22u/12/X5R/25V/K
C263 0.1u/4/X7R/16V/K
C264 0.1u/4/X7R/16V/K
C266 0.1u/4/X7R/16V/K
C265 0.1u/4/X7R/16V/K
R202 0/4 PCIE-HUB-RST#
KEY notch
JPCIE2-TXP
JPCIE2-TXN
JPCIE2-RXP R454 0/4 PCIE-SW-RXP05
JPCIE2-RXN R455 0/4 PCIE-SW-RXN05
PCIE-SW-CLKP05
PCIE-SW-CLKN05
10,18 PCIE0-EXTINT15
PCI-E/1X-36P/BK/OL/OP/[11AC1-021AC1-L1R_11AC1-L2R]
20171110
Modify to be open-back type
20 PCIE-ASM1061-RXP
20 PCIE-ASM1061-RXN
20 PCIE-SW-RXP01
20 PCIE-SW-RXN01
20 PCIE-SW-CLKP01
20 PCIE-SW-CLKN01
C271 0.1u/4/X7R/16V/K PCIE-SW-TXP01
C272 0.1u/4/X7R/16V/K PCIE-SW-TXN01
PCIE-SW-RXP01
PCIE-SW-RXN01
C274 0.1u/4/X7R/16V/K
PCIE-SW-CLKP01
PCIE-SW-CLKN01
C277 0.1u/4/X7R/16V/K
PCIE-HUB-RST# C585 0.1u/4/X7R/16V/K/X
20171110
Modify to be
3V3-PERST
DEL R459
R457 10K/4 MSCL
C283 0.1u/4/X7R/16V/K
R458 0/4
3V3-PERST
C552 0.1u/4/X7R/16V/K
10,23 I2C1-CPU-SCL
10,23 I2C1-CPU-SDA
R460 0/4/X MSCL
R461 0/4/X MSDA
C285 0.1u/4/X7R/16V/K
C288 0.1u/4/X7R/16V/K PCIE-SW-TXP03
C289 0.1u/4/X7R/16V/K PCIE-SW-TXN03
PCIE-SW-RXP03
PCIE-SW-RXN03
21 PCIE-uPD-RXP
21 PCIE-uPD-RXN
21 PCIE-SW-RXP03
21 PCIE-SW-RXN03
R210 12.1K/4/1
20171102
rename to be
I2C1 bus
U17
VSUS33
PE_RST_OUT#
PE_RST#
GPIO0
GPIO2
MSCL
MSDA
GPIO4
VDD12_0
VDDA33_0
TXP_3
TXN_3
RXP_3
RXN_3
VDD12_1
REXT1
VCC12_2
PECLKN_0
PECLKP_0
PECLKN_7
PECLKP_7
VDD12_5
RXN_7
RXP_7
TXN_7
TXP_7
VDDA33_2
VDD12_4
GPIO7
GPIO6
GPIO3
TEST_EN
ASM1184e/QFN64/[10TA1-081184-10R]
C273 0.1u/4/X7R/16V/K
PCIE-1184TXN0 C567 0.1u/4/X7R/16V/K PCIE0-CPU-RXN0
PCIE-1184TXP0 C568 0.1u/4/X7R/16V/K PCIE0-CPU-RXP0
PCIE-1184RXN0
PCIE-1184RXP0
R204 12.1K/4/1
C284 0.1u/4/X7R/16V/K
PCIE-CLKN0
PCIE-CLKP0
PCIE-SW-CLKN07
PCIE-SW-CLKP07
PCIE-SW-RXN07
PCIE-SW-RXP07
PCIE-SW-TXN07 C286 0.1u/4/X7R/16V/K JPCIE1-TXN
PCIE-SW-TXP07 C287 0.1u/4/X7R/16V/K JPCIE1-TXP
C290 0.1u/4/X7R/16V/K
R456 10K/4
C291 0.1u/4/X7R/16V/K
PCIE-SW-CLKP03
PCIE-SW-CLKN03
C295 0.1u/4/X7R/16V/K
C296 0.1u/4/X7R/16V/K
C297 0.1u/4/X7R/16V/K PCIE-SW-TXP05
C298 0.1u/4/X7R/16V/K PCIE-SW-TXN05
C294 0.1u/4/X7R/16V/K
PCIE-SW-CLKN05
PCIE-SW-CLKP05
PCIE-SW-RXN05
PCIE-SW-RXP05
C278 0.1u/4/X7R/16V/K
C279 0.1u/4/X7R/16V/K
C280 0.1u/4/X7R/16V/K
C281 0.1u/4/X7R/16V/K
C282 0.1u/4/X7R/16V/K
U18
9FGL0241BKILF/VFQFPN24/S
VDD3.3
VDD3.3
VDDA3.3
vSADR/REF3.3
VDDDIG3.3
VDDXTAL3.3
CKPWRGD_PD
SCLK_3.3
SDATA_3.3
XIN/CLKIN
X2
DIF1#
DIF1
DIF0#
DIF0
vOE1#
vOE0#
VSS_EN_tri
GNDA
GNDXTAL
GNDREF
GNDDIG
PCIE-CLKN0
PCIE-CLKP0
PCIE0-CPU-REFCLKNI
PCIE0-CPU-REFCLKPI
R205 10K/4
R206 10K/4
R207 0/4
R208 0/4
R209 0/4
X2
25M/8p/30ppm/2.0*1.6/80/S
C292 10P/4/NPO/50V/C
C293 10P/4/NPO/50V/C
GIGABYTE TECHNOLOGY CORPORATION
Title
PCIE_SW_ASM1184E
Size
Document Number
Rev 0.3
Date: Monday, January 15, 2018
Sheet 18 of 36



GIGABYTE TECHNOLOGY CORPORATION	
Title	PCIEx16 Connector
Size	Document Number: MZSC2AM_(LINARO 96)
Rev	0.3
Date:	Monday, January 15, 2018
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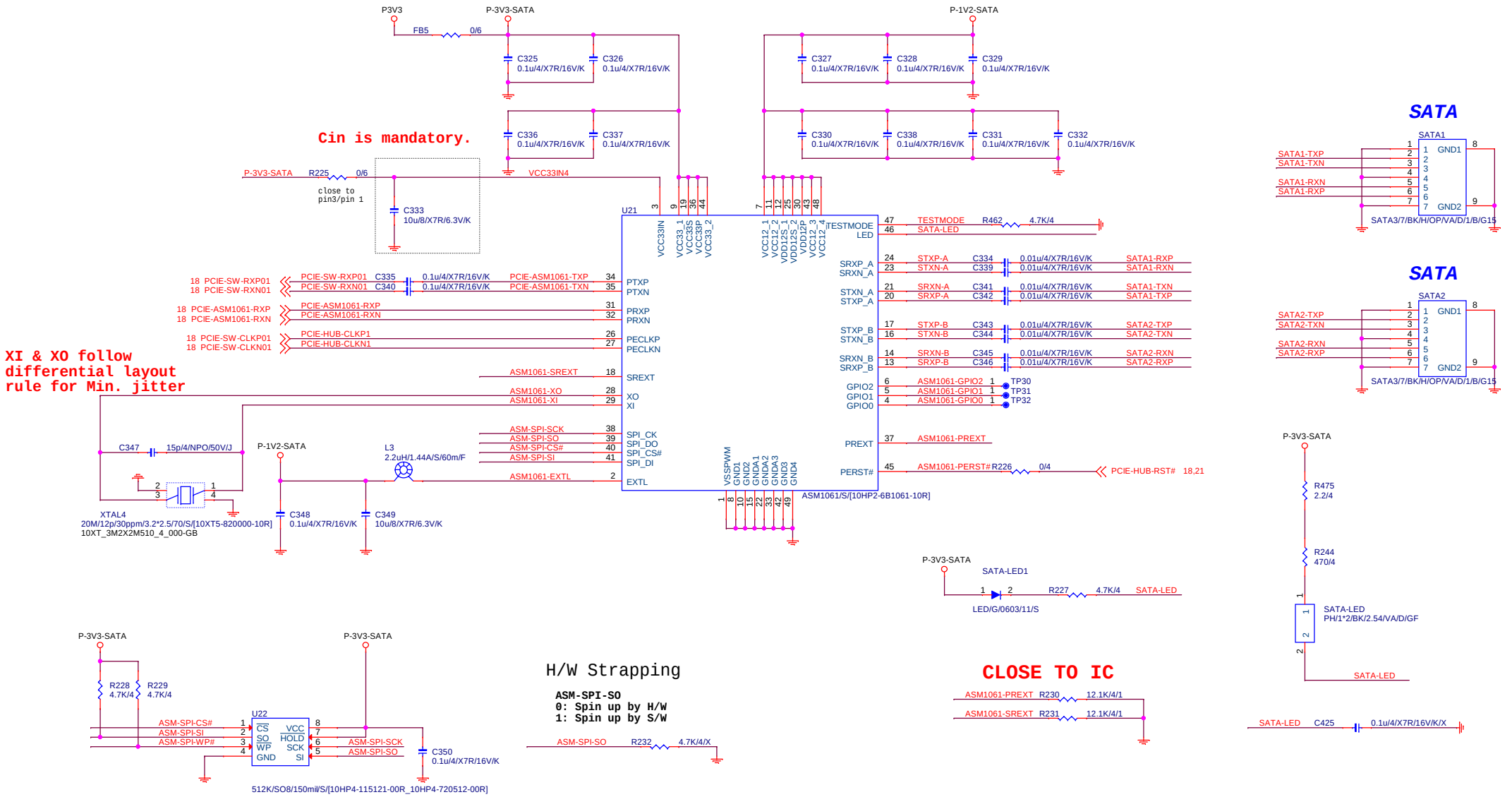
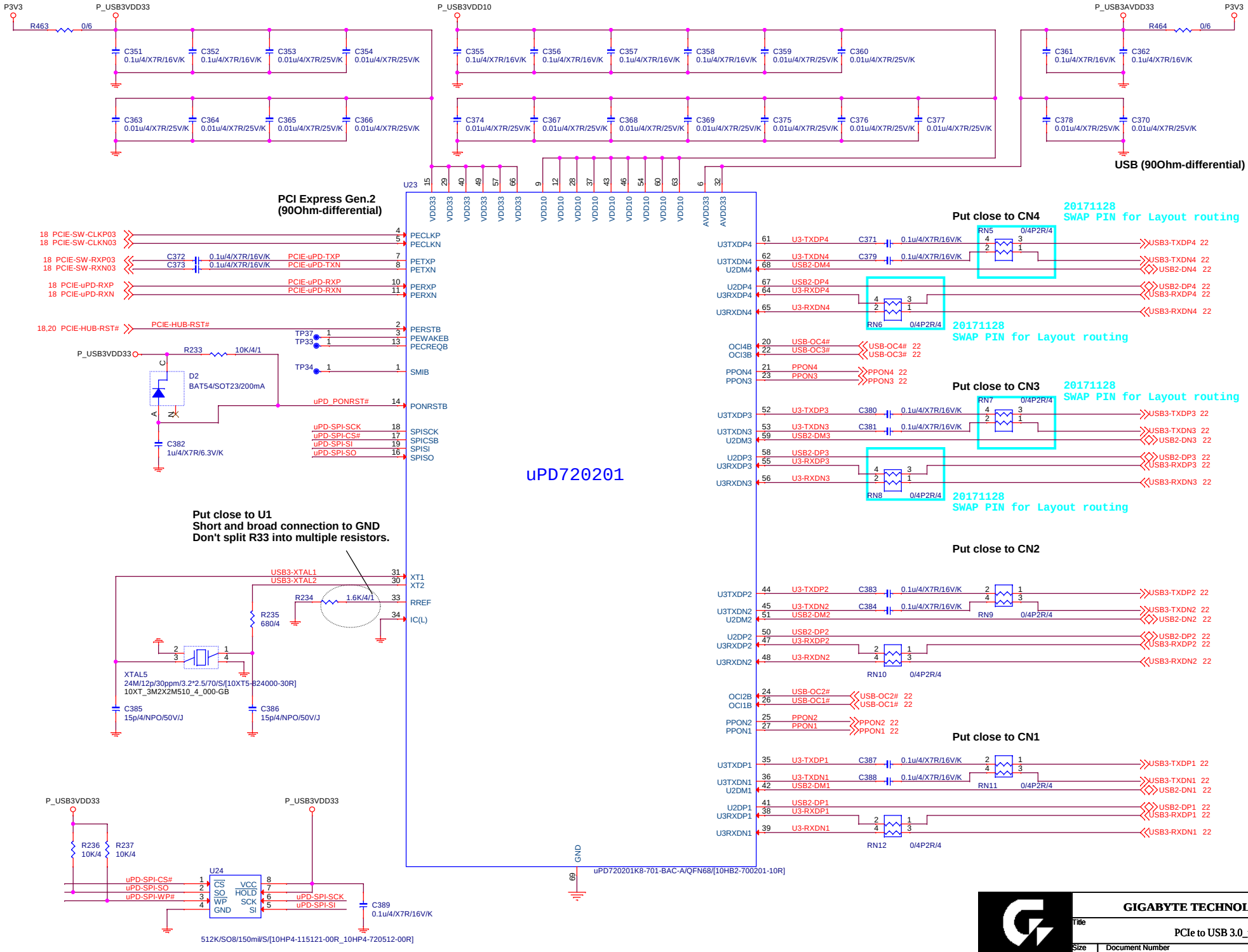


GIGABYTE TECHNOLOGY CORPORATION	
Title	PCIe to SATA_ASM1061
Size	Document Number: MZSC2AM_(LINARO 96) — Rev: 0.3
Date: Monday, January 15, 2018	Sheet 20 of 36


P3V3
P_USB3VDD33
P_USB3VDD10
P_USB3AVDD33
R463 0/6
R464 0/6
C351 0.1u/4/X7R/16V/K
C352 0.1u/4/X7R/16V/K
C353 0.01u/4/X7R/25V/K
C354 0.01u/4/X7R/25V/K
C355 0.1u/4/X7R/16V/K
C356 0.1u/4/X7R/16V/K
C357 0.1u/4/X7R/16V/K
C358 0.1u/4/X7R/16V/K
C359 0.01u/4/X7R/25V/K
C360 0.01u/4/X7R/25V/K
C361 0.1u/4/X7R/16V/K
C362 0.1u/4/X7R/16V/K
C363 0.01u/4/X7R/25V/K
C364 0.01u/4/X7R/25V/K
C365 0.01u/4/X7R/25V/K
C366 0.01u/4/X7R/25V/K
C374 0.01u/4/X7R/25V/K
C367 0.01u/4/X7R/25V/K
C368 0.01u/4/X7R/25V/K
C369 0.01u/4/X7R/25V/K
C375 0.01u/4/X7R/25V/K
C376 0.01u/4/X7R/25V/K
C377 0.01u/4/X7R/25V/K
C378 0.01u/4/X7R/25V/K
C370 0.01u/4/X7R/25V/K
USB (90Ohm-differential)
U23
VDD33
VDD10
AVDD33
PCI Express Gen.2
(90Ohm-differential)
18 PCIE-SW-CLKP03
18 PCIE-SW-CLKN03
PECLKP
PECLKN
18 PCIE-SW-RXP03
18 PCIE-SW-RXN03
C372 0.1u/4/X7R/16V/K
C373 0.1u/4/X7R/16V/K
PCIE-uPD-TXP
PCIE-uPD-TXN
PETXP
PETXN
18 PCIE-uPD-RXP
18 PCIE-uPD-RXN
PCIE-uPD-RXP
PCIE-uPD-RXN
PERXP
PERXN
18,20 PCIE-HUB-RST#
PCIE-HUB-RST#
PERSTB
TP37
TP33
PEWAKEB
PECREQB
P_USB3VDD33
R233 10K/4/1
D2
BAT54/SOT23/200mA
TP34
SMIB
uPD_PONRST#
PONRSTB
C382 1u/4/X7R/6.3V/K
uPD-SPI-SCK
uPD-SPI-CS#
uPD-SPI-SI
uPD-SPI-SO
SPISCK
SPICSB
SPISI
SPISO
uPD720201
Put close to U1
Short and broad connection to GND
Don't split R33 into multiple resistors.
USB3-XTALI
USB3-XTALO
XT1
XT2
R234 1.6K/4/1
RREF
R235 680/4
IC(L)
XTAL5
24M/12p/30ppm/3.2*2.5/70/S/[10XT5-824000-30R]
10XT_3M2X2M510_4_000-GB
C385 15p/4/NPO/50V/J
C386 15p/4/NPO/50V/J
U3TXDP4
U3TXDN4
U2DM4
U2DP4
U3RXDP4
U3RXDN4
U3-TXDP4
U3-TXDN4
USB2-DM4
USB2-DP4
U3-RXDP4
U3-RXDN4
C371 0.1u/4/X7R/16V/K
C379 0.1u/4/X7R/16V/K
RN5 0/4P2R/4
RN6 0/4P2R/4
USB3-TXDP4 22
USB3-TXDN4 22
USB2-DM4 22
USB2-DP4 22
USB3-RXDP4 22
USB3-RXDN4 22
20171128
SWAP PIN for Layout routing
Put close to CN4
OCI4B
OCI3B
USB-OC4#
USB-OC3#
PPON4
PPON3
U3TXDP3
U3TXDN3
U2DM3
U2DP3
U3RXDP3
U3RXDN3
U3-TXDP3
U3-TXDN3
USB2-DM3
USB2-DP3
U3-RXDP3
U3-RXDN3
C380 0.1u/4/X7R/16V/K
C381 0.1u/4/X7R/16V/K
RN7 0/4P2R/4
RN8 0/4P2R/4
USB3-TXDP3 22
USB3-TXDN3 22
USB2-DN3 22
USB2-DP3 22
USB3-RXDP3 22
USB3-RXDN3 22
Put close to CN3
Put close to CN2
U3TXDP2
U3TXDN2
U2DM2
U2DP2
U3RXDP2
U3RXDN2
U3-TXDP2
U3-TXDN2
USB2-DM2
USB2-DP2
U3-RXDP2
U3-RXDN2
C383 0.1u/4/X7R/16V/K
C384 0.1u/4/X7R/16V/K
RN9 0/4P2R/4
RN10 0/4P2R/4
USB3-TXDP2 22
USB3-TXDN2 22
USB2-DN2 22
USB2-DP2 22
USB3-RXDP2 22
USB3-RXDN2 22
OCI2B
OCI1B
USB-OC2#
USB-OC1#
PPON2
PPON1
Put close to CN1
U3TXDP1
U3TXDN1
U2DM1
U2DP1
U3RXDP1
U3RXDN1
U3-TXDP1
U3-TXDN1
USB2-DM1
USB2-DP1
U3-RXDP1
U3-RXDN1
C387 0.1u/4/X7R/16V/K
C388 0.1u/4/X7R/16V/K
RN11 0/4P2R/4
RN12 0/4P2R/4
USB3-TXDP1 22
USB3-TXDN1 22
USB2-DN1 22
USB2-DP1 22
USB3-RXDP1 22
USB3-RXDN1 22
GND
uPD720201K8-701-BAC-A/QFN68/[10HB2-700201-10R]
P_USB3VDD33
R236 10K/4
R237 10K/4
U24
CS
SO
WP
GND
VCC
HOLD
SCK
SI
C389 0.1u/4/X7R/16V/K
512K/SO8/150mil/S/[10HP4-115121-00R_10HP4-720512-00R]
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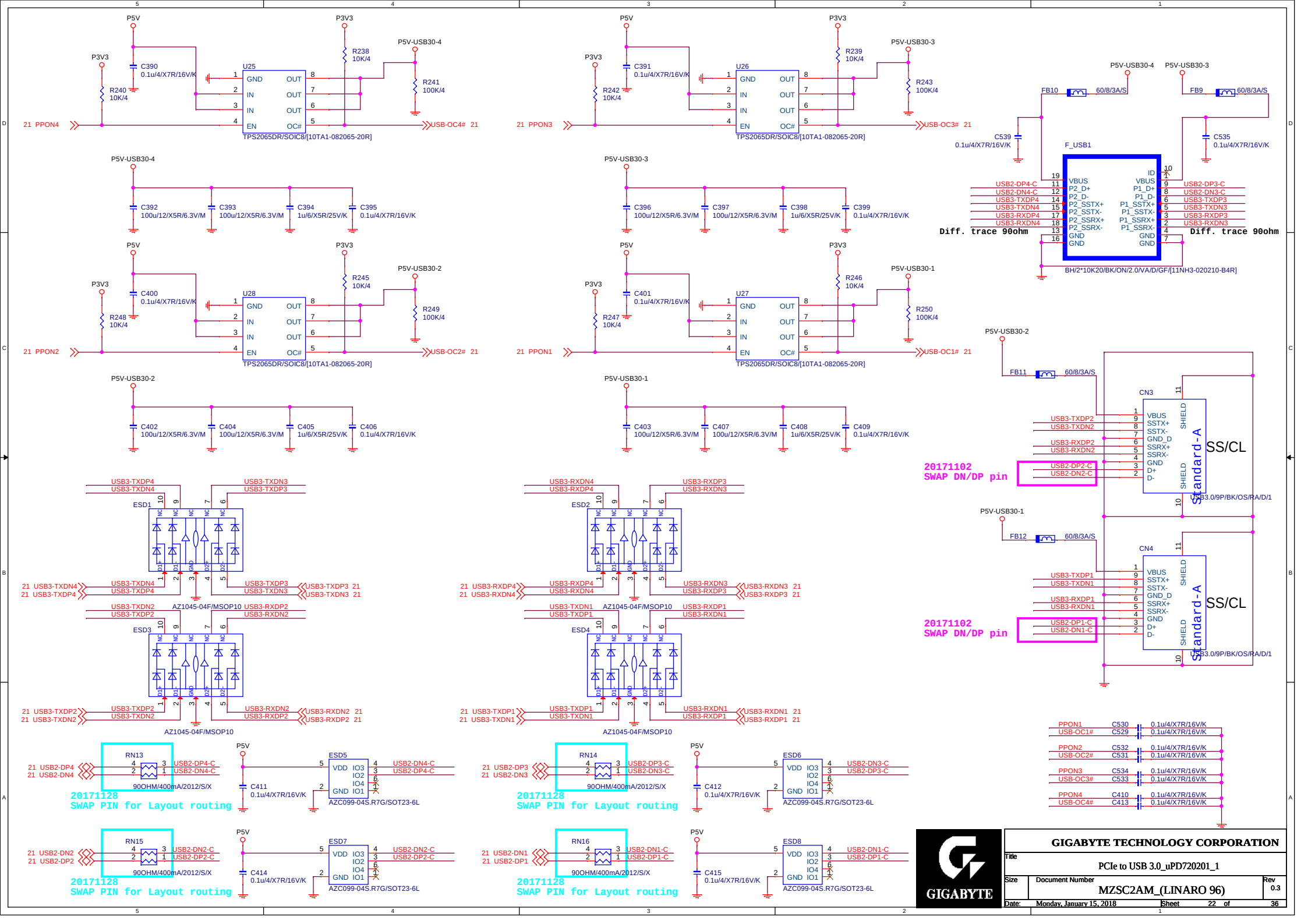
P5V
P3V3
C390 0.1u/4/X7R/16V/K
R240 10K/4
U25
GND OUT
IN OUT
IN OUT
EN OC#
R238 10K/4
P5V-USB30-4
R241 100K/4
21 PPON4
USB-OC4# 21
TPS2065DR/SOIC8/[10TA1-082065-20R]
C391 0.1u/4/X7R/16V/K
R242 10K/4
U26
R239 10K/4
P5V-USB30-3
R243 100K/4
21 PPON3
USB-OC3# 21
C392 100u/12/X5R/6.3V/M
C393 100u/12/X5R/6.3V/M
C394 1u/6/X5R/25V/K
C395 0.1u/4/X7R/16V/K
C396 100u/12/X5R/6.3V/M
C397 100u/12/X5R/6.3V/M
C398 1u/6/X5R/25V/K
C399 0.1u/4/X7R/16V/K
C400 0.1u/4/X7R/16V/K
R248 10K/4
U28
R245 10K/4
P5V-USB30-2
R249 100K/4
21 PPON2
USB-OC2# 21
C401 0.1u/4/X7R/16V/K
R247 10K/4
U27
R246 10K/4
P5V-USB30-1
R250 100K/4
21 PPON1
USB-OC1# 21
C402 100u/12/X5R/6.3V/M
C404 100u/12/X5R/6.3V/M
C405 1u/6/X5R/25V/K
C406 0.1u/4/X7R/16V/K
C403 100u/12/X5R/6.3V/M
C407 100u/12/X5R/6.3V/M
C408 1u/6/X5R/25V/K
C409 0.1u/4/X7R/16V/K
FB10 60/8/3A/S
FB9 60/8/3A/S
C539 0.1u/4/X7R/16V/K
C535 0.1u/4/X7R/16V/K
F_USB1
USB2-DP4-C
USB2-DN4-C
USB3-TXDP4
USB3-TXDN4
USB3-RXDP4
USB3-RXDN4
VBUS
P2_D+
P2_D-
P2_SSTX+
P2_SSTX-
P2_SSRX+
P2_SSRX-
GND
ID
P1_D+
P1_D-
P1_SSTX+
P1_SSTX-
P1_SSRX+
P1_SSRX-
USB2-DP3-C
USB2-DN3-C
USB3-TXDP3
USB3-TXDN3
USB3-RXDP3
USB3-RXDN3
Diff. trace 90ohm
Diff. trace 90ohm
BH/2*10K20/BK/ON/2.0/VA/D/GF/[11NH3-020210-B4R]
FB11 60/8/3A/S
FB12 60/8/3A/S
CN3
CN4
SHIELD
SS/CL
Standard-A
USB3.0/9P/BK/OS/RA/D/1
20171102
SWAP DN/DP pin
ESD1
ESD2
ESD3
ESD4
AZ1045-04F/MSOP10
21 USB3-TXDP4
21 USB3-TXDN4
21 USB3-TXDP2
21 USB3-TXDN2
21 USB3-RXDP4
21 USB3-RXDN4
21 USB3-TXDP1
21 USB3-TXDN1
RN13
RN14
RN15
RN16
90OHM/400mA/2012/S/X
21 USB2-DP4
21 USB2-DN4
21 USB2-DP3
21 USB2-DN3
21 USB2-DN2
21 USB2-DP2
21 USB2-DN1
21 USB2-DP1
20171128
SWAP PIN for Layout routing
ESD5
ESD6
ESD7
ESD8
AZC099-04S.R7G/SOT23-6L
C411 0.1u/4/X7R/16V/K
C412 0.1u/4/X7R/16V/K
C414 0.1u/4/X7R/16V/K
C415 0.1u/4/X7R/16V/K
PPON1 C530 0.1u/4/X7R/16V/K
USB-OC1# C529 0.1u/4/X7R/16V/K
PPON2 C532 0.1u/4/X7R/16V/K
USB-OC2# C531 0.1u/4/X7R/16V/K
PPON3 C534 0.1u/4/X7R/16V/K
USB-OC3# C533 0.1u/4/X7R/16V/K
PPON4 C410 0.1u/4/X7R/16V/K
USB-OC4# C413 0.1u/4/X7R/16V/K
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20171102
Add NUT Location for HS(TOP side)

HEAT SINK
HS1
heat sink/screw/[12SP2-060059-00H]

HS2
M2.5/UD5.0/BD3.5/H2.0/L1.2/SN
HS3
M2.5/UD5.0/BD3.5/H2.0/L1.2/SN

20171102
Add LEVEL Shift for CPU

U62
SN74LVC1G07DBVR/SOT23-5/[10TA1-090707-01R]
C595 0.1u/6/X7R/16V/K
R443 10K/4
PSIN#
PSIN#-1V8
PSIN#-1V8 10

P5V_STBY_PSU
R421 100K/4
ATX-PSON#
N12V
C416 4.7n/6/X7R/50V/K
P3V3
ATX1
3.3V 3.3V
-12V 3.3V
GND GND
PSON 5V
GND GND
GND 5V
GND GND
-5V POK
5V 5VSB
5V 12V
5V 12V
GND 3.3V
P5V
P12V
N5V
C418 0.1u/4/X7R/16V/K
C419 0.1u/4/X7R/16V/K
C420 0.1u/4/X7R/16V/K
C421 0.022u/4/X7R/16V/K
C422 0.1u/4/X7R/16V/K
APW/2*12/IV/OC/OP/4.2/VA/SN/SK/2H/[11NH4-020024-06R_11NH4-020024-08R]

C562 4.7n/4/X7R/25V/K
C563 0.022u/4/X7R/25V/K
C564 4.7u/8/X5R/25V/K
R256 2.7K/4
R257 0/4/X
PWRGD-PS-R1
PWRGD-PS-PWROK
PWRGD-PS-PWROK 24
C417 0.1u/4/X7R/16V/K

P5V_STBY_PSU
R188 10K/4
APL5315BI-TRL/SOT23-5/300mA
PQ14
P3V3-AUX-EN
R184 10K/4/1
R183 31.6K/4/1
P3V3-STBY
VOUT=3.328V
C572 1u/4/X5R/6.3V/K/X
C541 2.2u/4/X5R/6.3V/M
C545 0.1u/4/X5R/16V/K/X
C570 1u/4/X5R/6.3V/K/X
C571 10u/6/X5R/6.3V/M

20171102
Connect pin3 and pin4 together

POWER BUTTON
PWR-SW
SW/4/BK/H5.0/D/Ag/[11NH1-030001-04R]
R466 33/4
R467 33/4
R262 10K/4
R263 2.2/4
PSIN#
C423 0.1u/4/X7R/16V/K/X
11 PWR-ONOFF#

J-PWR-SW
PH/1*2/BK/2.54/VA/D/GF

P5V_STBY_PSU
R261 1K/4
PWRGD-PS-PWROK
R264 2.7K/4
Q2 2N7002KT1G/SOT23/24.5pF/2.5/ESD/[*10IF1-037002-00R]
SOT23
P3V3
R265 10K/4
Q3 2N7002KT1G/SOT23/24.5pF/2.5/ESD/[*10IF1-037002-00R]
R266 0/4/X
C424 1u/4/X5R/16V/K
P5V
R267 10K/4
Q4 2N7002KT1G/SOT23/24.5pF/2.5/ESD/[*10IF1-037002-00R]
C426 1u/4/X5R/16V/K
P12V
R268 10K/4
Q5 2N7002KT1G/SOT23/24.5pF/2.5/ESD/[*10IF1-037002-00R]
R269 4.7K/4/X
C427 1u/4/X5R/16V/K
Q6 2N7002KT1G/SOT23/24.5pF/2.5/ESD/[*10IF1-037002-00R]
PWRGD-PS-R1

ATX-PSON#
PSIN#
FAN-PWM
MCU-SDA R479 0/4/X
MCU-SCL R480 0/4/X
I2C1-CPU-SDA 10,18
I2C1-CPU-SCL 10,18
20171102
rename to be I2C1 bus

20171102
Modify to be DNI

U57
EFM8BB10F2G-A-QFN20R/QFN20/S
10TA_QFN-G10_20_200-GB
CPU-PWROFF-3V3
TP36 1MCU-P00
EFM8BB1-RST#
R469 1K/4
C574 0.1u/4/X7R/16V/K
C573 0.1u/4/X7R/16V/K/X
MCU-P07 TP13
AUTO-BOOT
MCU-P11 TP15
20171102
DELETE TP14
MCU-P13 TP16
MCU-P14 TP21
MCU-P15 TP22
MCU-P16 TP29
C2D
C2CK
R470 0/4

20171117
Modify to be 1K
20171117
Modify to be DNI
20171117
Add R498

P3V3-STBY
P1V8
U53
SN74LVC1G07DBVR/SOT23-5/[10TA1-090707-01R]
R422 10K/4
R498 10K/4
R431 0/4
CPU-PWROFF-3V3
PWROFF#

20171110
Modify to be 2X3, ADD R497
J-MCU
C2CK
C2D
AUTO-BOOT
R497 1K/4
P3V3-STBY
PH/2*3/BK/2.54/VA/D/[11NH2-000203-03R]

J-MCU
JP/1*2/BU/OH/2.54/O/GF
J-MCU-1
3-5 closed, autoboot disable
5-6 closed, autoboot enable

20171110
Add Jumper for
auto boot setting

P3V3
MMBT2222A/SOT23/600mA/40
Q96
R472 1K/4
FAN-PWM
R471 0/4
R473 8.2K/4
R474 51/6
P5V
P12V
80mil
C579 10u/8/X5R/16V/K
C580 10u/8/X5R/16V/K
SYS FAN
SYS_FAN
FAN/1*4/WH/A3/2.54/VA/D/SN/[11NH5-060104-C1R_11NH5-060104-E0R]

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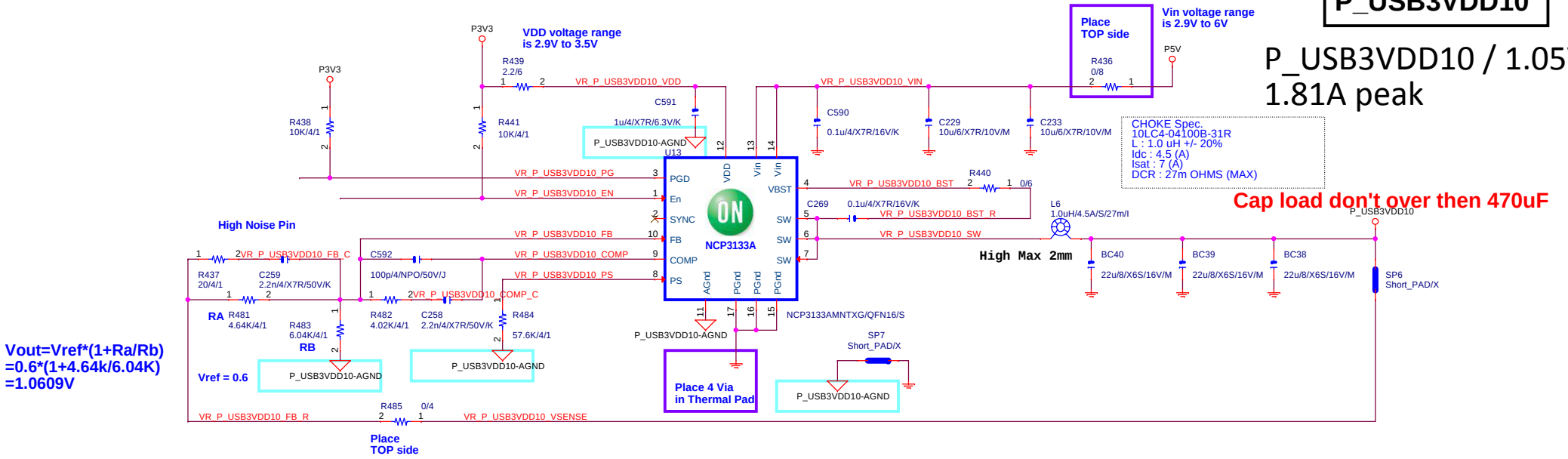
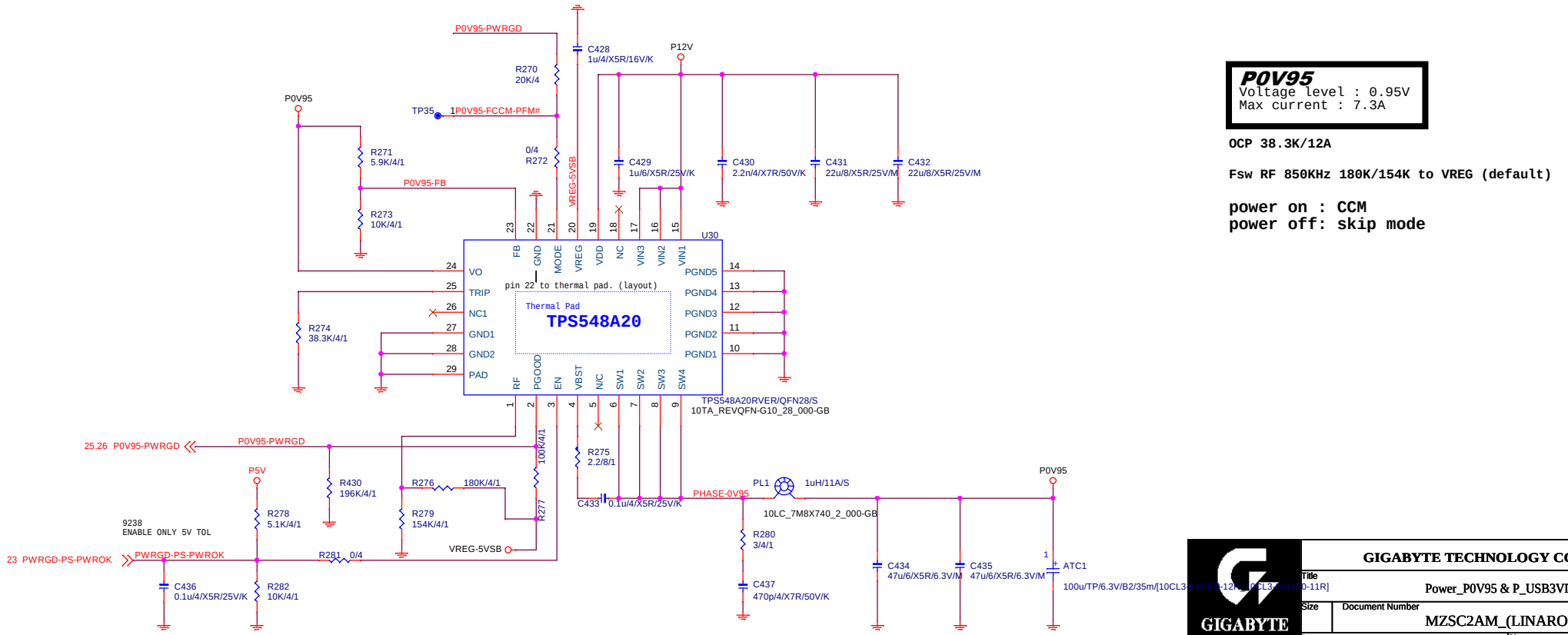
P_USB3VDD10

P_USB3VDD10 / 1.05V
1.81A peak





P0V95
Voltage level : 0.95V
Max current : 7.3A

OCP 38.3K/12A

Fsw RF 850KHz 180K/154K to VREG (default)

power on : CCM
power off: skip mode

GIGABYTE TECHNOLOGY CORPORATION	
Title	Power_P0V95 & P_USB3VDD10
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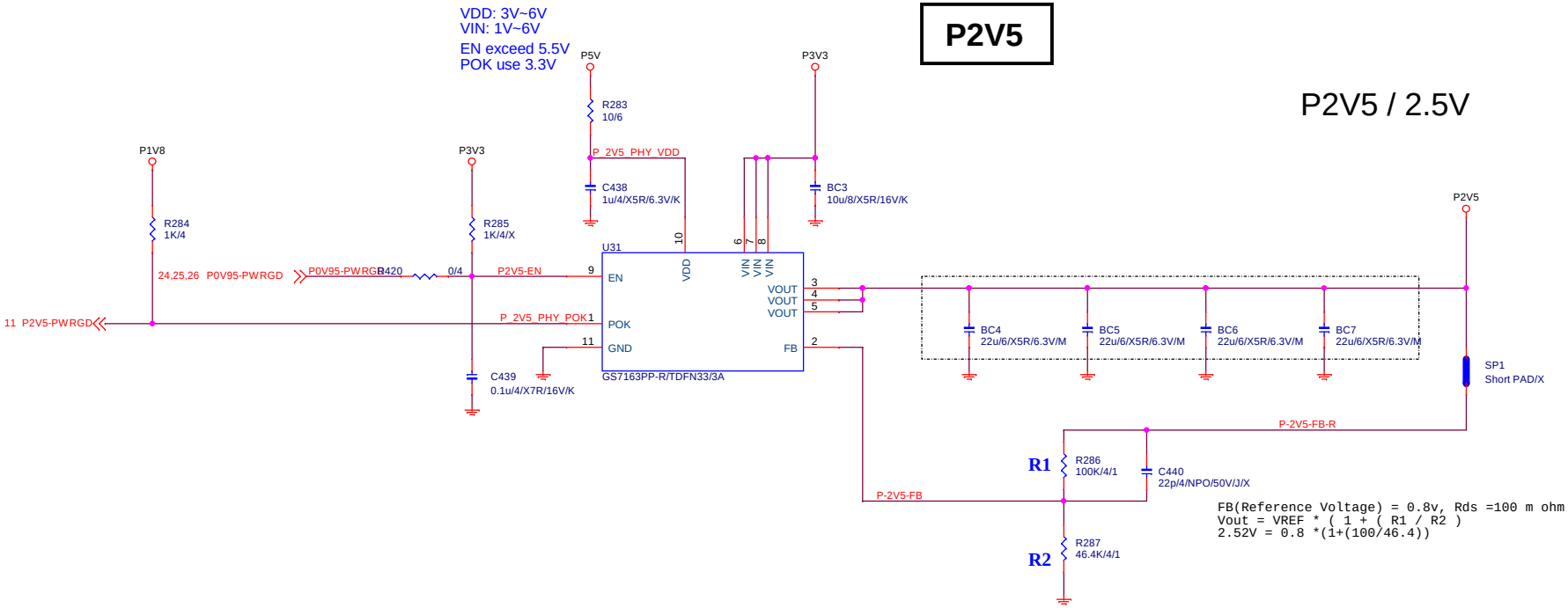
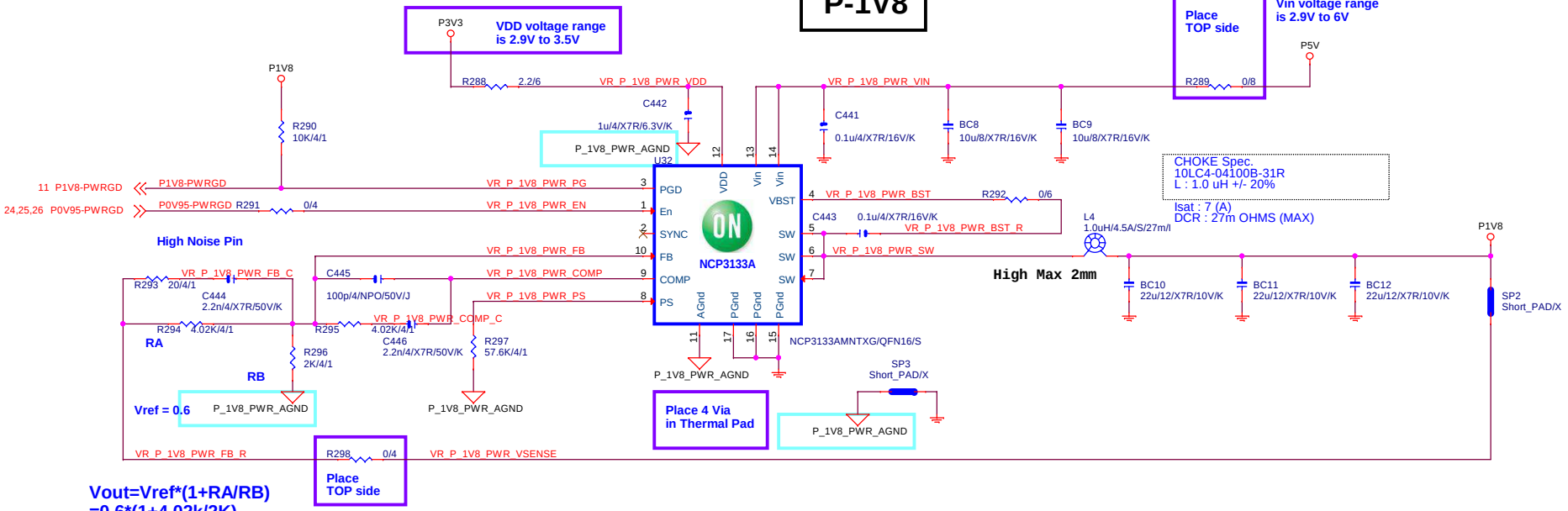
P2V5

VDD: 3V~6V
VIN: 1V~6V
EN exceed 5.5V
POK use 3.3V

P2V5 / 2.5V



P-1V8



GIGABYTE	GIGABYTE TECHNOLOGY CORPORATION	
	Title: Power_P2V5 & P1V8	
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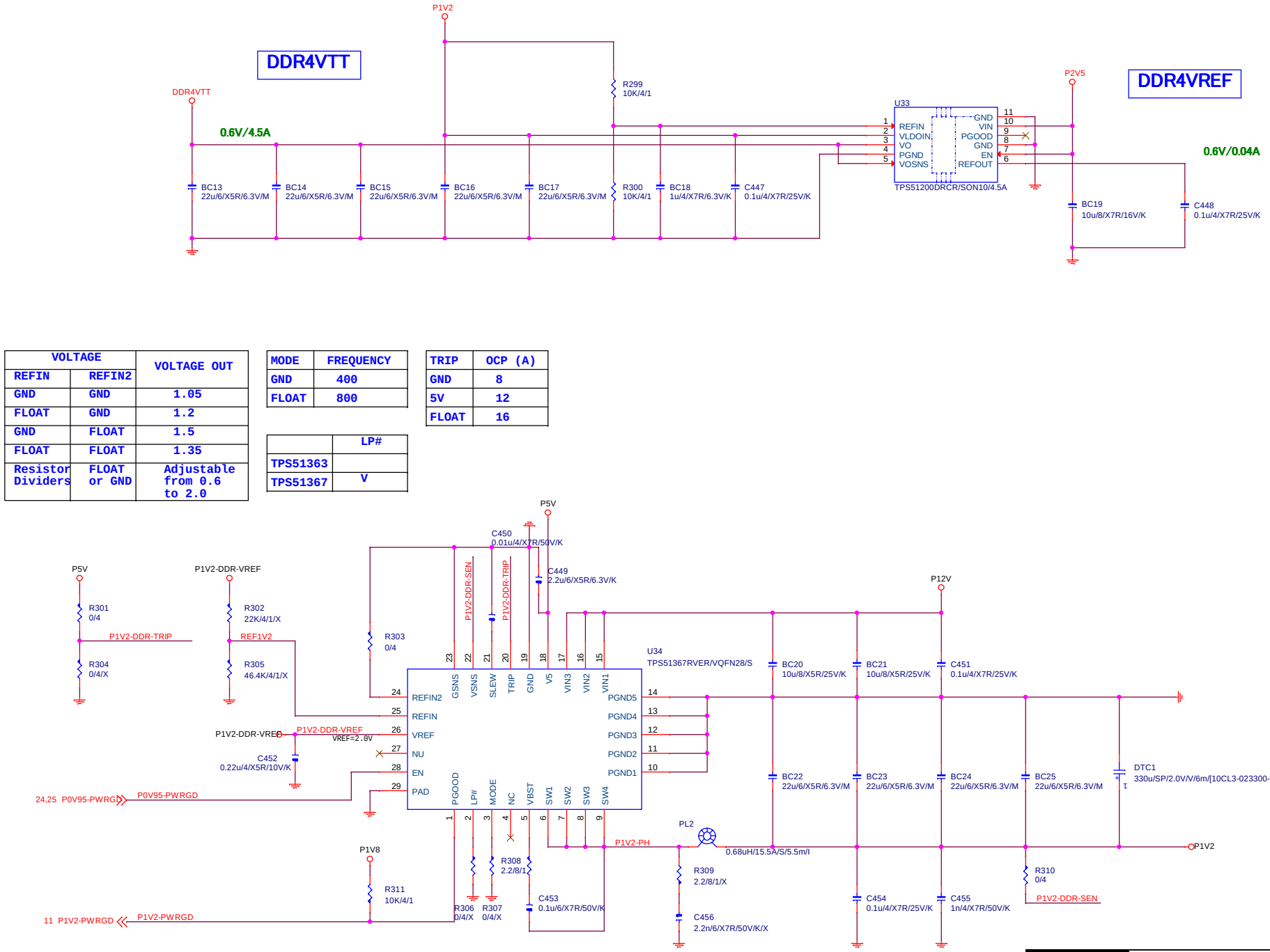

VOLTAGE		VOLTAGE OUT
REFIN	REFIN2	
GND	GND	1.05
FLOAT	GND	1.2
GND	FLOAT	1.5
FLOAT	FLOAT	1.35
Resistor Dividers	FLOAT or GND	Adjustable from 0.6 to 2.0

MODE	FREQUENCY
GND	400
FLOAT	800

TRIP	OCP (A)
GND	8
5V	12
FLOAT	16

	LP#
TPS51363	
TPS51367	V

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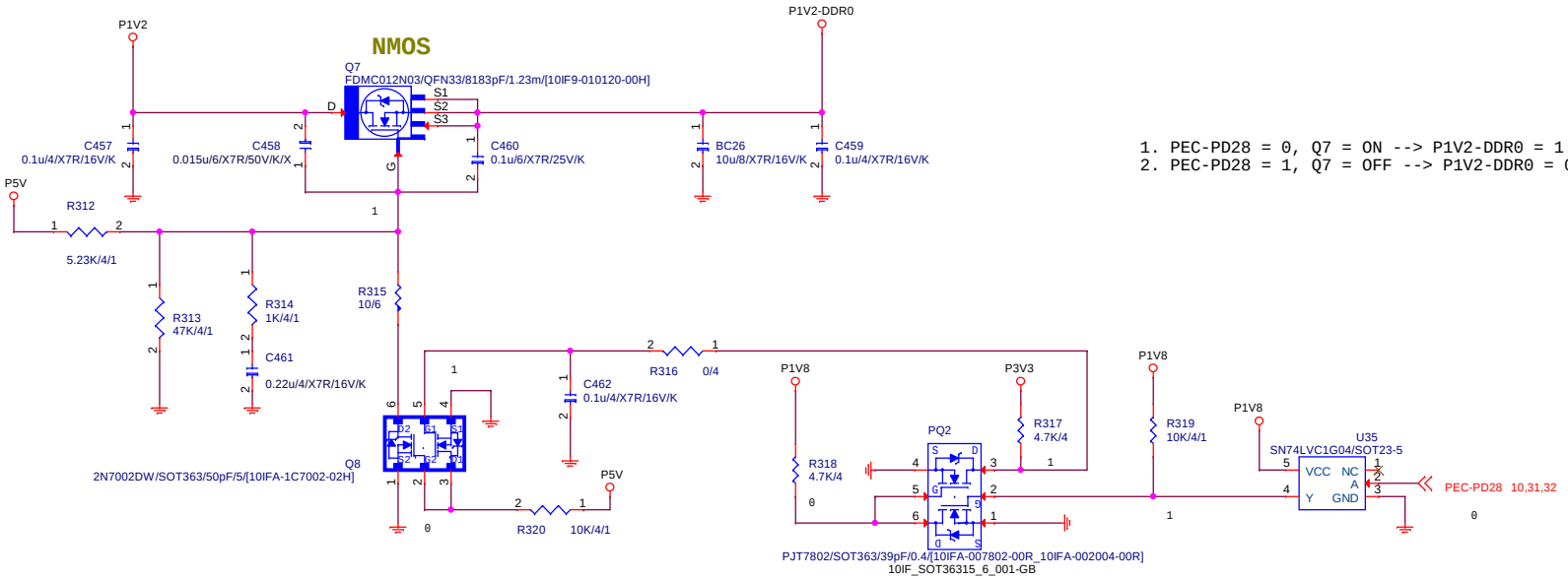
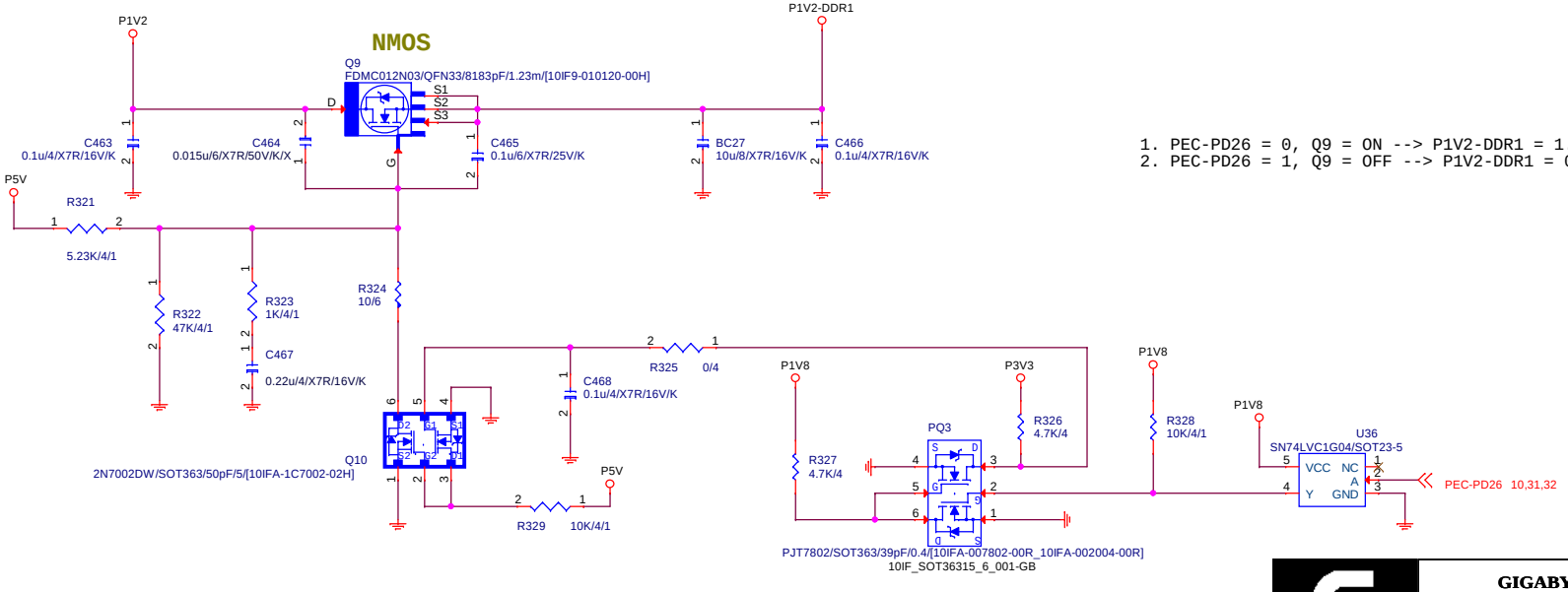
P1V2-DDR0



1. PEC-PD28 = 0, Q7 = ON --> P1V2-DDR0 = 1.2V
2. PEC-PD28 = 1, Q7 = OFF --> P1V2-DDR0 = 0V

P1V2-DDR1



1. PEC-PD26 = 0, Q9 = ON --> P1V2-DDR1 = 1.2V
2. PEC-PD26 = 1, Q9 = OFF --> P1V2-DDR1 = 0V

GIGABYTE	GIGABYTE TECHNOLOGY CORPORATION	
	Title: Power_P1V2-DDR	
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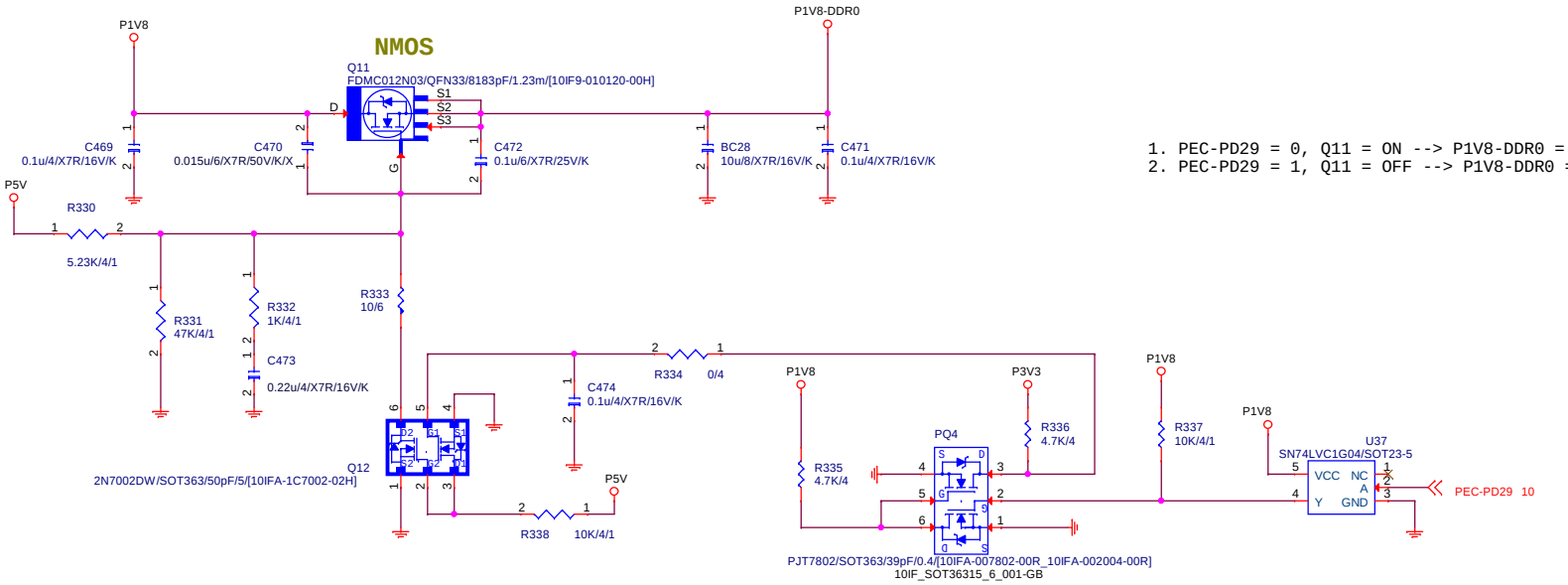
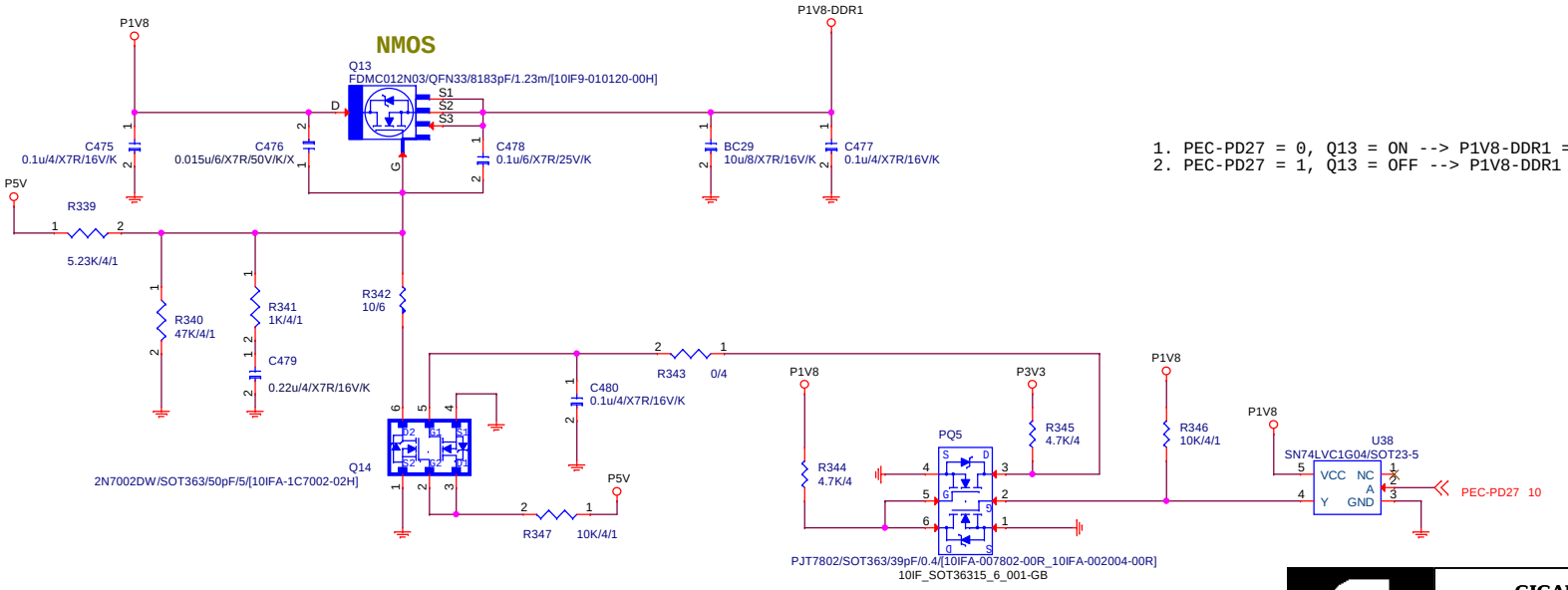
P1V8-DDR0



1. PEC-PD29 = 0, Q11 = ON --> P1V8-DDR0 = 1.8V
2. PEC-PD29 = 1, Q11 = OFF --> P1V8-DDR0 = 0V

P1V8-DDR1



1. PEC-PD27 = 0, Q13 = ON --> P1V8-DDR1 = 1.8V
2. PEC-PD27 = 1, Q13 = OFF --> P1V8-DDR1 = 0V

GIGABYTE	GIGABYTE TECHNOLOGY CORPORATION	
	Title: Power_P1V8-DDR	
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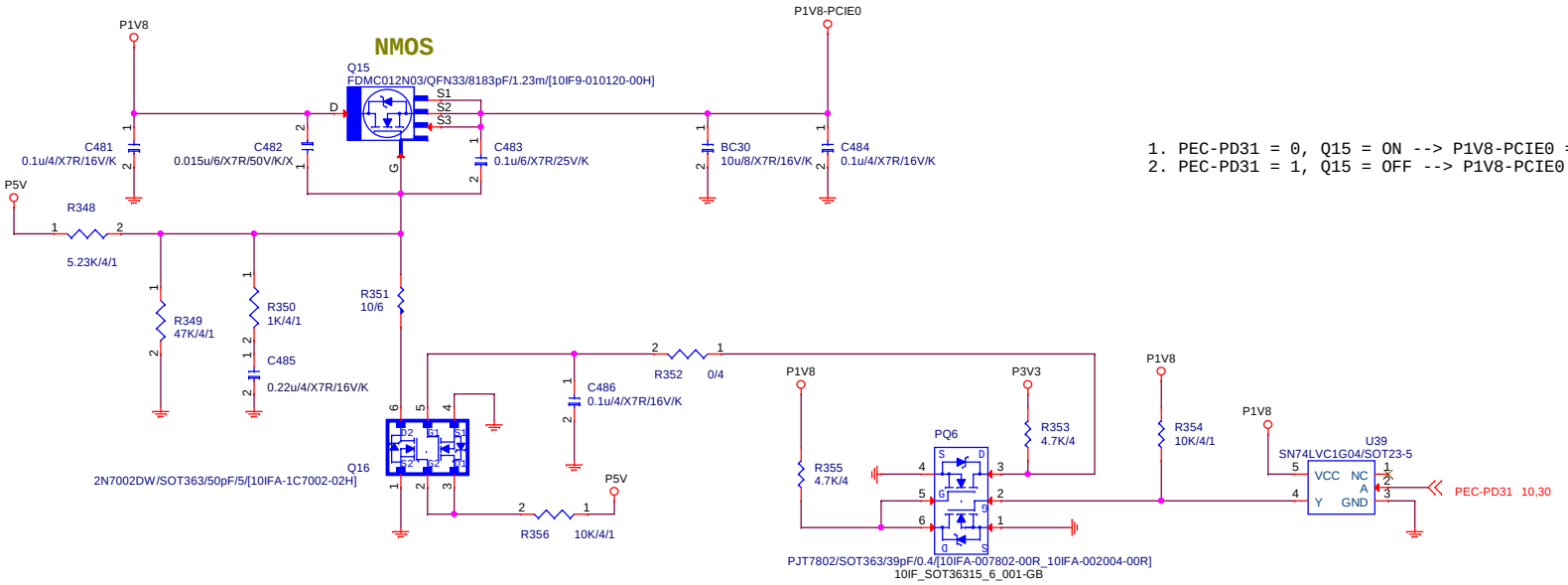
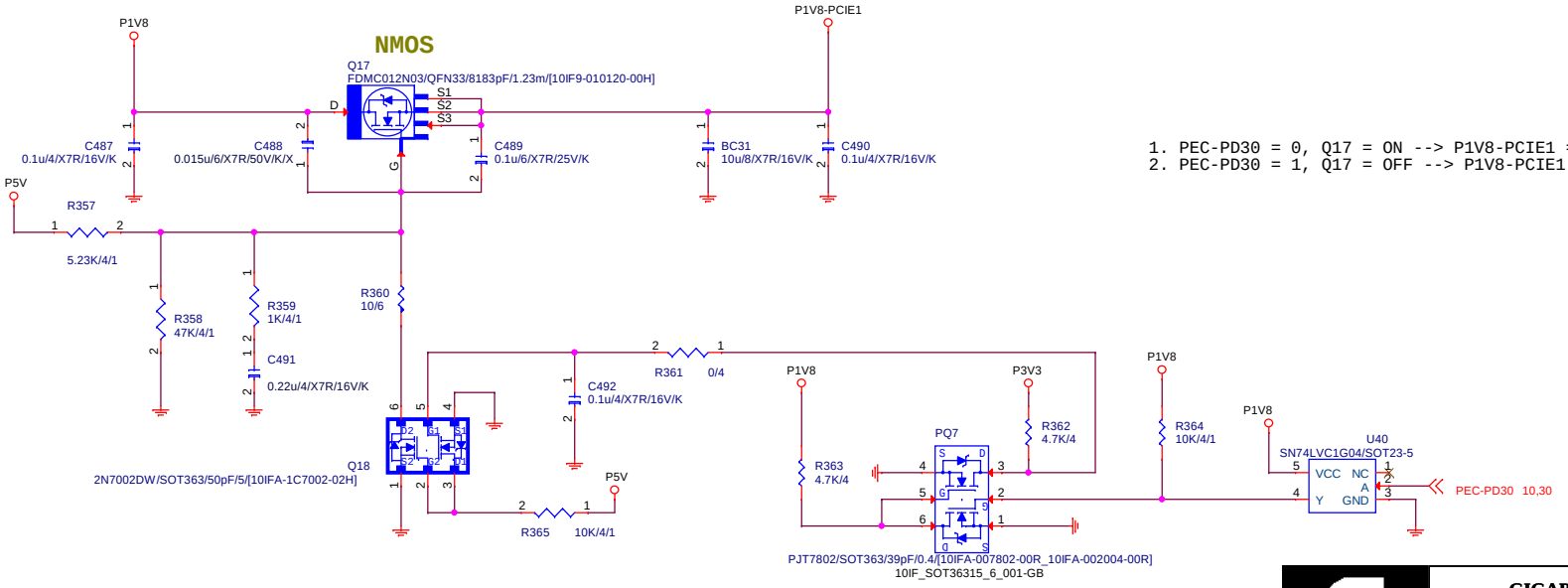
P1V8-PCIE0



1. PEC-PD31 = 0, Q15 = ON --> P1V8-PCIE0 = 1.8V
2. PEC-PD31 = 1, Q15 = OFF --> P1V8-PCIE0 = 0V

P1V8-PCIE1



1. PEC-PD30 = 0, Q17 = ON --> P1V8-PCIE1 = 1.8V
2. PEC-PD30 = 1, Q17 = OFF --> P1V8-PCIE1 = 0V

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Title	Power_P1V8-PCIE	
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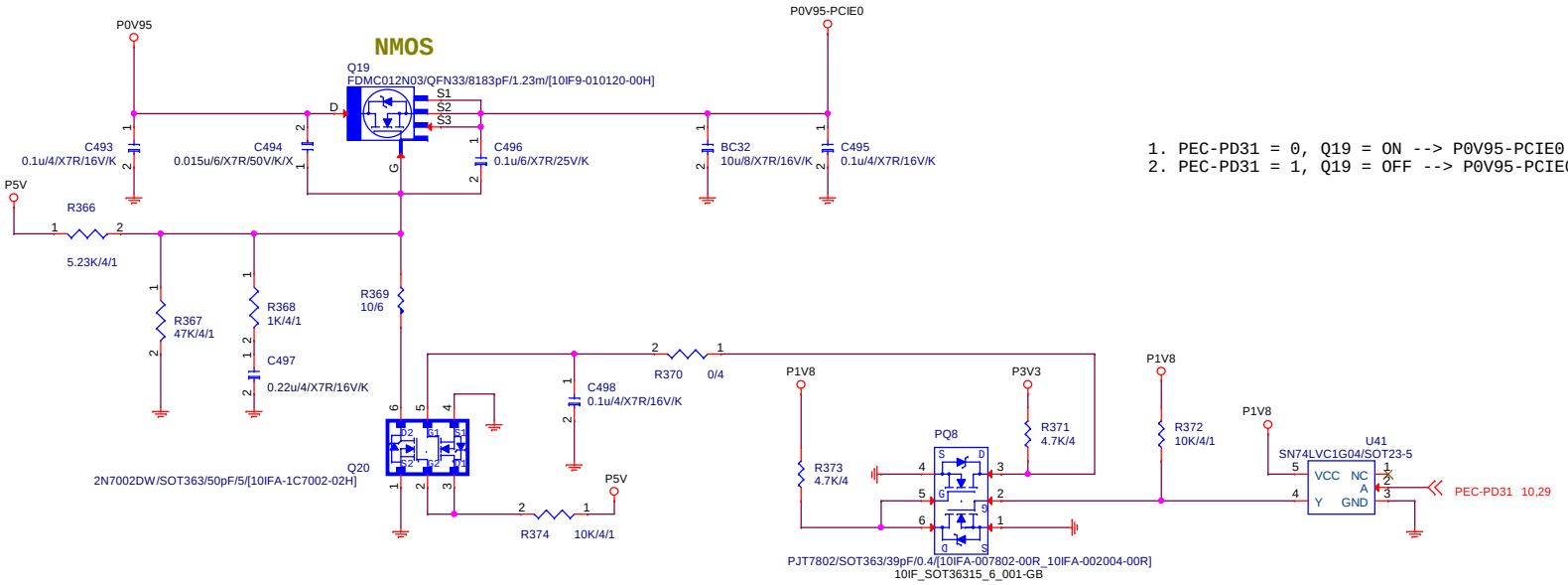
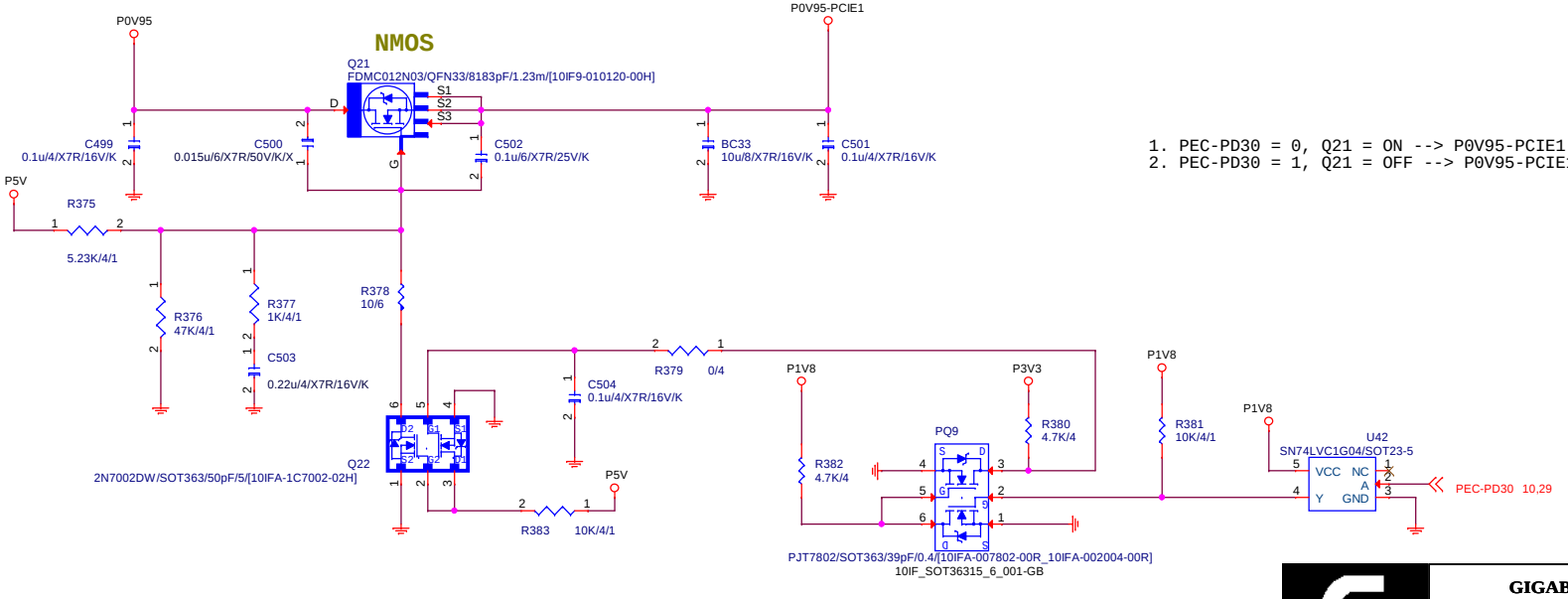
P0V95-VDDIO-PCIE0



1. PEC-PD31 = 0, Q19 = ON --> P0V95-PCIE0 = 0.95V
2. PEC-PD31 = 1, Q19 = OFF --> P0V95-PCIE0 = 0V

P0V95-VDDIO-PCIE1



1. PEC-PD30 = 0, Q21 = ON --> P0V95-PCIE1 = 0.95V
2. PEC-PD30 = 1, Q21 = OFF --> P0V95-PCIE1 = 0V

GIGABYTE	GIGABYTE TECHNOLOGY CORPORATION	
	Title: Power_P0V95-PCIE	
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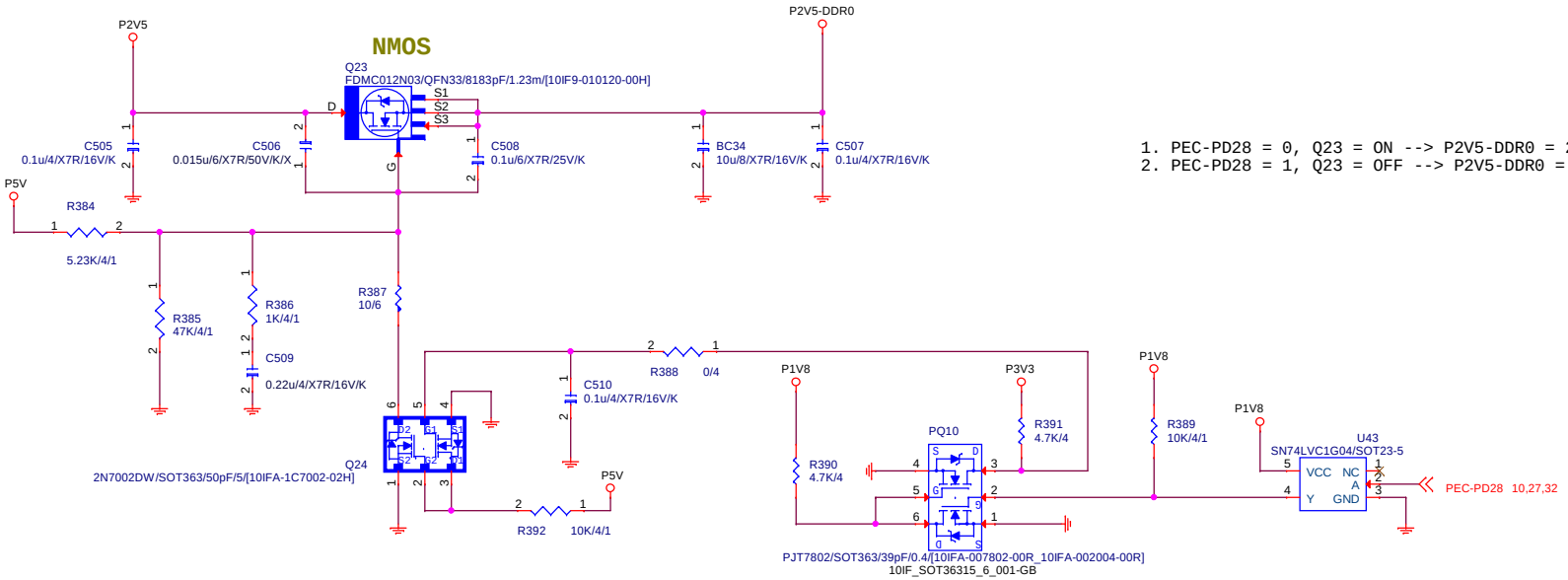
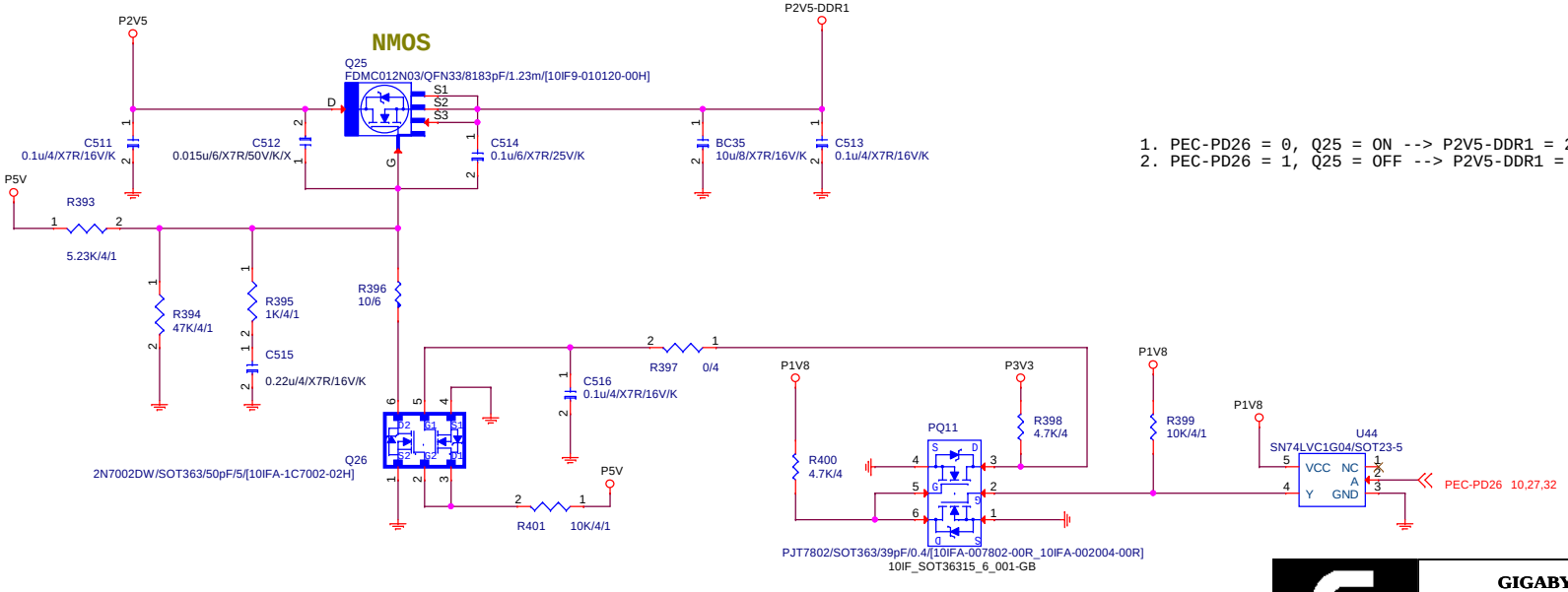
P2V5-DDR0



1. PEC-PD28 = 0, Q23 = ON --> P2V5-DDR0 = 2.5V
2. PEC-PD28 = 1, Q23 = OFF --> P2V5-DDR0 = 0V

P2V5-DDR1



1. PEC-PD26 = 0, Q25 = ON --> P2V5-DDR1 = 2.5V
2. PEC-PD26 = 1, Q25 = OFF --> P2V5-DDR1 = 0V

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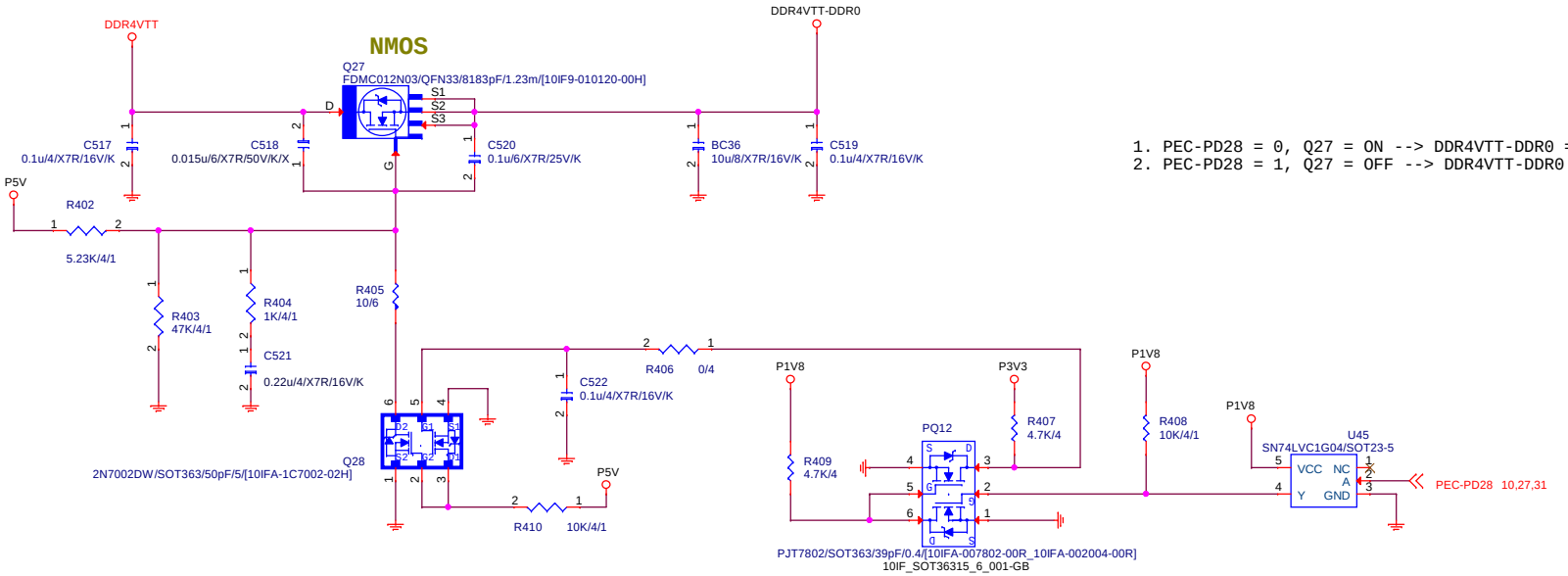
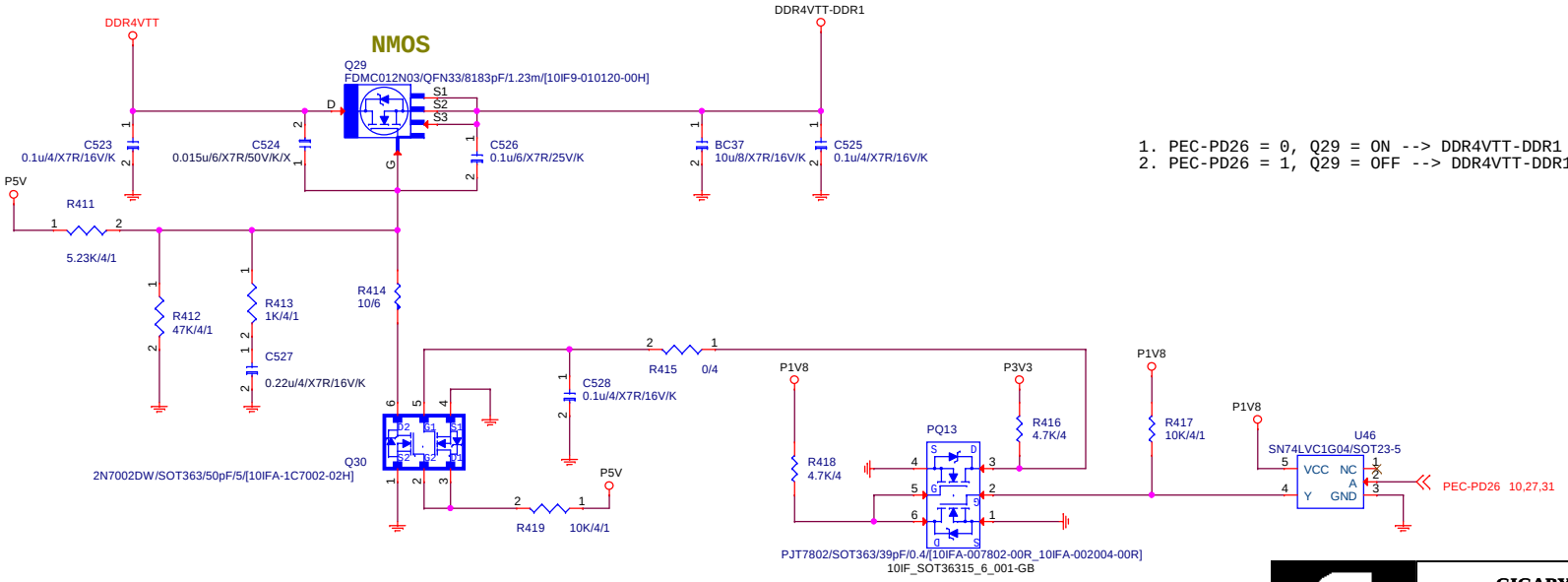
DDR4VTT-DDR0



1. PEC-PD28 = 0, Q27 = ON --> DDR4VTT-DDR0 = 0.6V
2. PEC-PD28 = 1, Q27 = OFF --> DDR4VTT-DDR0 = 0V

DDR4VTT-DDR1



1. PEC-PD26 = 0, Q29 = ON --> DDR4VTT-DDR1 = 0.6V
2. PEC-PD26 = 1, Q29 = OFF --> DDR4VTT-DDR1 = 0V

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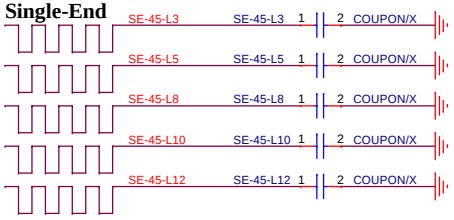
GPIO Table(SIO)

SIO Pin Out (pin number)	Net Name	I/O	Usage(Hi/Lo/Chipset Default)
PD0(N38)		INPUT	CONNECT TO DSW3_PIN1
PD1(N37)		INPUT	CONNECT TO DSW3_PIN2
PD2(N36)		INPUT	CONNECT TO DSW3_PIN3
PD3(N34)		INPUT	CONNECT TO DSW3_PIN4
PD4(P38)		INPUT	CONNECT TO DSW3_PIN5
PD5(P37)		INPUT	CONNECT TO DSW3_PIN6
PD6(P35)		INPUT	CONNECT TO DSW3_PIN7
PD7(P34)		INPUT	CONNECT TO DSW3_PIN8
PD8(R38)	PSIN#-1V8	INPUT	POWER BUTTOM PUSH 4sec. for POWEROFF REQUEST
PD9(R36)	PWROFF#	OUTPUT	TURN OFF ATX POWER SUPPLY (ACTIVE:LOW)
PD10(R35)	CPU-PD10	I/O	GPIO
PD11(R34)	CPU-PD11	I/O	GPIO
PD12(T38)	CPU-PD12	I/O	GPIO
PD13(T37)	CPU-PD13	I/O	GPIO
PD14(T36)	PCIE1EXTINT	INPUT	PCIE1 PRESET DETECT(ACTIVE:LOW)
PD15(T34)	PCIE0EXTINT	INPUT	PCIE0 PRESET DETECT(ACTIVE:LOW)
PD16(U38)	PHY2-INT#	INPUT	PHY2 INTERRUPT
PD17(U37)	PHY1-INT#	INPUT	PHY1 INTERRUPT
PD18(U35)	CPU-PD18	I/O	GPIO
PD19(U34)	CPU-PD19	I/O	GPIO
PD20(V38)	CPU-PD20	I/O	GPIO
PD21(V36)	CPU-PD21	I/O	GPIO
PD22(V35)	CPU-PD22	I/O	GPIO
PD23(V34)	CPU-PD23	I/O	GPIO
PD24(W38)	CPU-PD24	I/O	GPIO
PD25(W37)	CPU-PD25	I/O	GPIO
PD26(W36)	PEC-PD26	OUTPUT	P2V5-DDR1/P1V2-DDR1/DDR4VTT-DDR1 POWER ENABLE CONTROL(ACTIVE:LOW)
PD27(W34)	PEC-PD27	OUTPUT	P1V8-DDR1 POWER ENABLE CONTROL(ACTIVE:LOW)
PD28(Y38)	PEC-PD28	OUTPUT	P2V5-DDR0/P1V2-DDR0/DDR4VTT-DDR0 POWER ENABLE CONTROL(ACTIVE:LOW)
PD29(Y37)	PEC-PD29	OUTPUT	P1V8-DDR0 POWER ENABLE CONTROL(ACTIVE:LOW)
PD30(Y35)	PEC-PD30	OUTPUT	P0V95-PCIE1/P1V8-PCIE1 POWER ENABLE CONTROL(ACTIVE:LOW)
PD31(Y34)	PEC-PD31	OUTPUT	P0V95-PCIE0/P1V8-PCIE0 POWER ENABLE CONTROL(ACTIVE:LOW)

Single-End



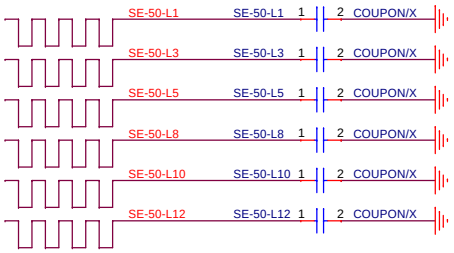
L3 5 mils = 45Ω ± 10%

L5 5 mils = 45Ω ± 10%

L8 5 mils = 45Ω ± 10%

L10 5 mils = 50Ω ± 10%

L12 6 mils = 50Ω ± 10%



L1 5 mils = 50Ω ± 10%

L3 4 mils = 50Ω ± 10%

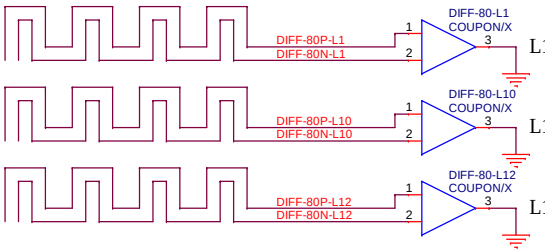
L5 4 mils = 50Ω ± 10%

L8 4 mils = 50Ω ± 10%

L10 4 mils = 50Ω ± 10%

L12 5 mils = 50Ω ± 10%

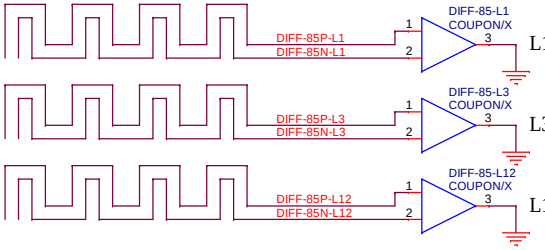
Differential



L1 5.5 / 4.5 / 5.5 mils = 80Ω ± 10%

L10 5 / 4.5 / 5 mils = 80Ω ± 10%

L12 5.5 / 4.5 / 5.5 mils = 80Ω ± 10%

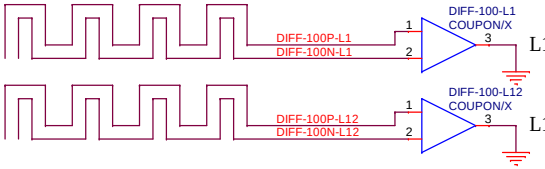


L1 4.5 / 4.5 / 4.5 mils = 85Ω ± 10%

L3 4.5 / 4.5 / 4.5 mils = 85Ω ± 10%

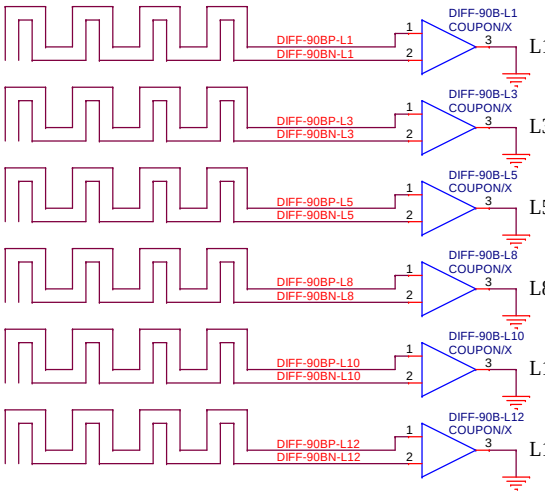
L12 4.5 / 4.5 / 4.5 mils = 85Ω ± 10%

L1 4 / 6 / 4 mils = 95Ω ± 10%



L1 3.5 / 6.5 / 3.5 mils = 100Ω ± 10%

L12 3.5 / 6.5 / 3.5 mils = 100Ω ± 10%



L1 4 / 4.5 / 4 mils = 90Ω ± 10%

L3 5 / 12 / 5 mils = 90Ω ± 10%

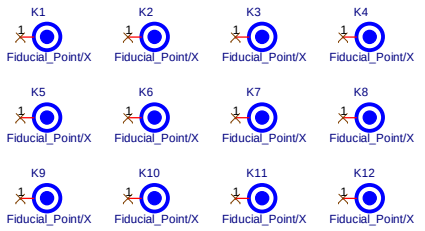
L5 5 / 12 / 5 mils = 90Ω ± 10%

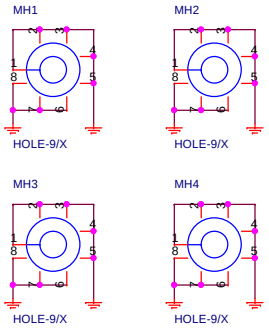
L8 5 / 12 / 5 mils = 90Ω ± 10%

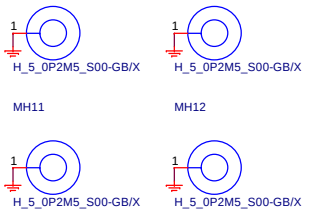
L10 5 / 12 / 5 mils = 90Ω ± 10%

L12 4 / 4.5 / 4 mils = 90Ω ± 10%

MOUNTING HOLE







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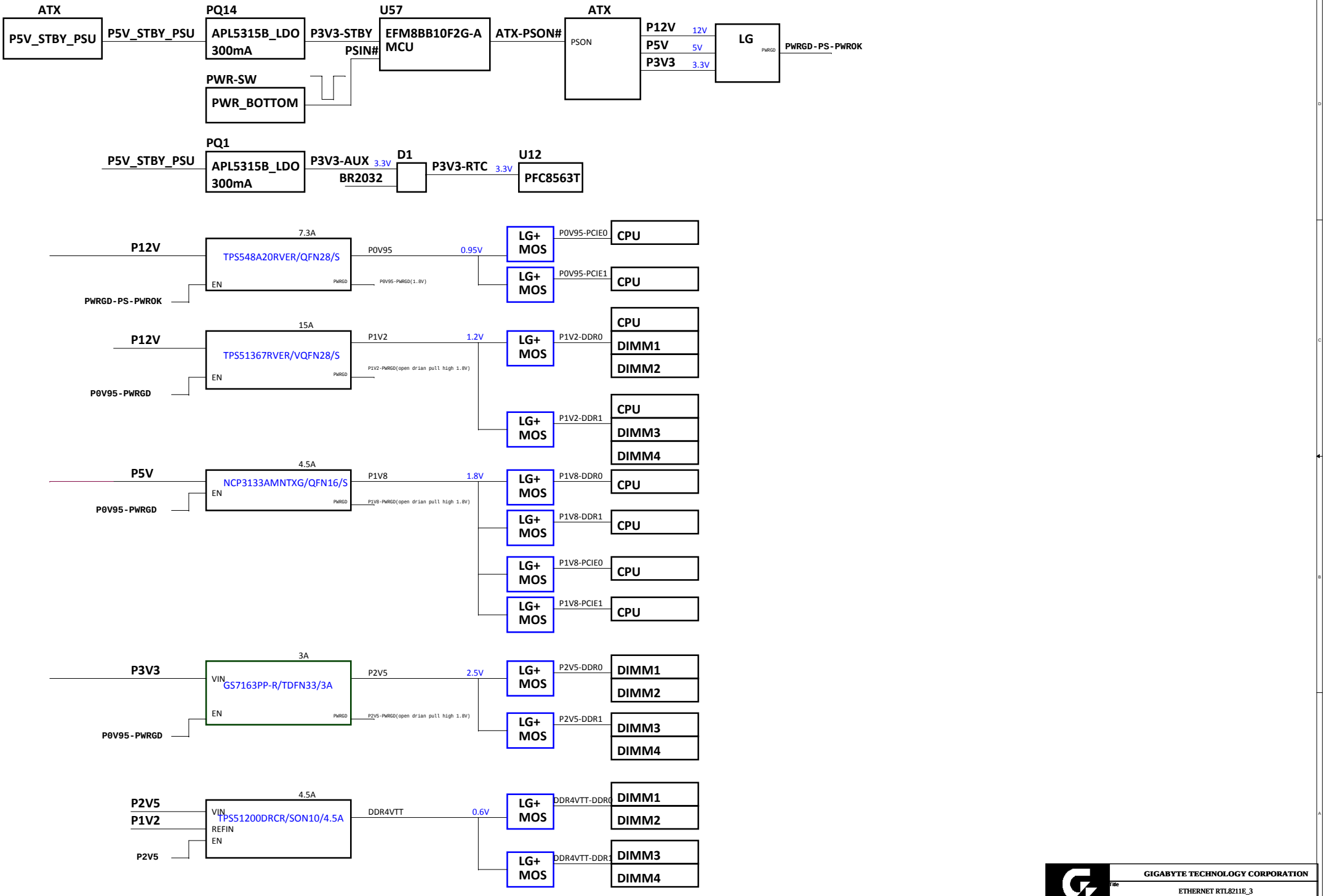

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