Hi3798CV2OPB VER.B

Hi3798CV200 Open Source Board

4 layers PCB with DDR3 8bit x 4

Board Size:160mm x 120mm x 1.6mm

Hi3798CV2OPB VER.B_V1.0.0.0

Hoperun Technology Corporation

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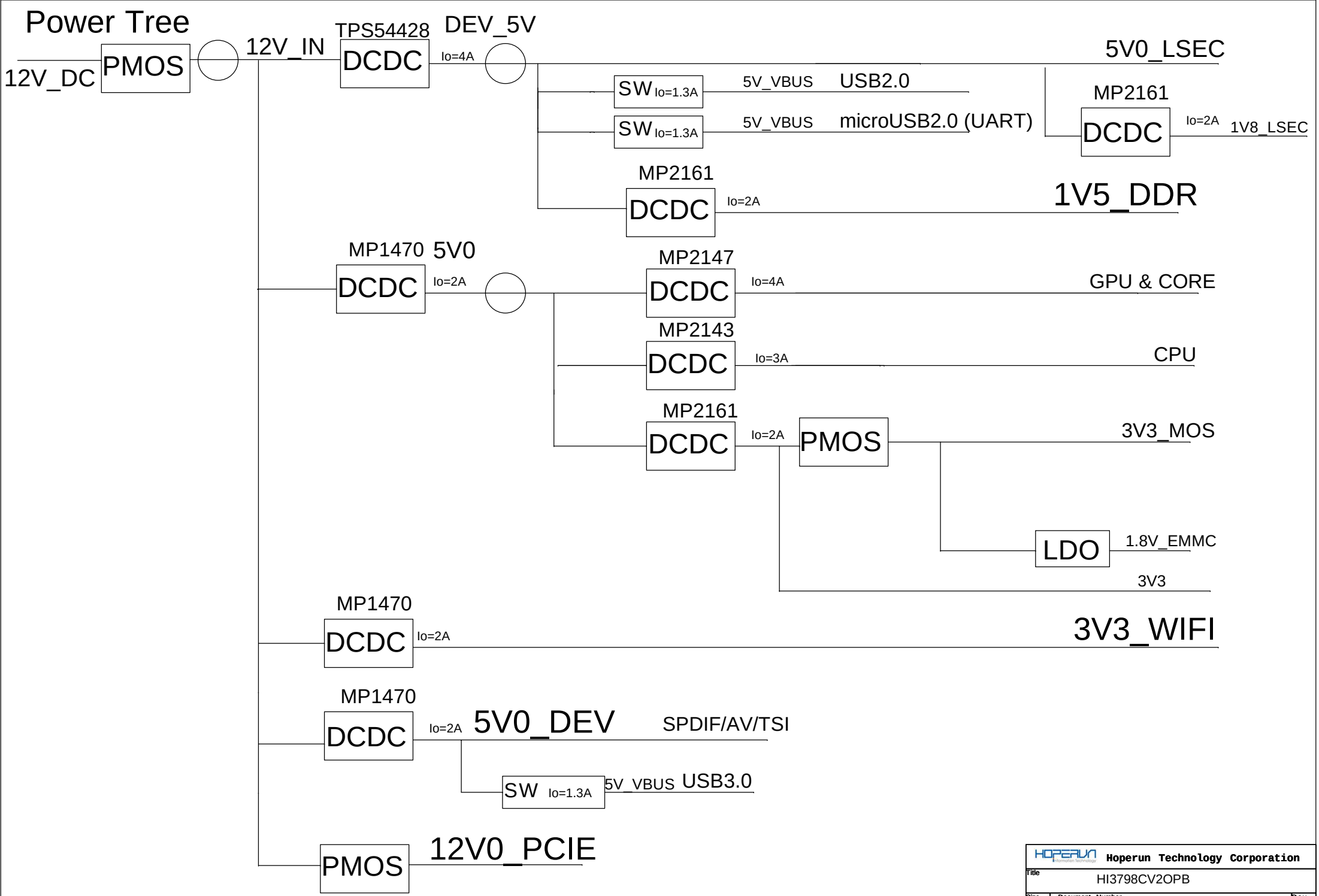
Power Tree



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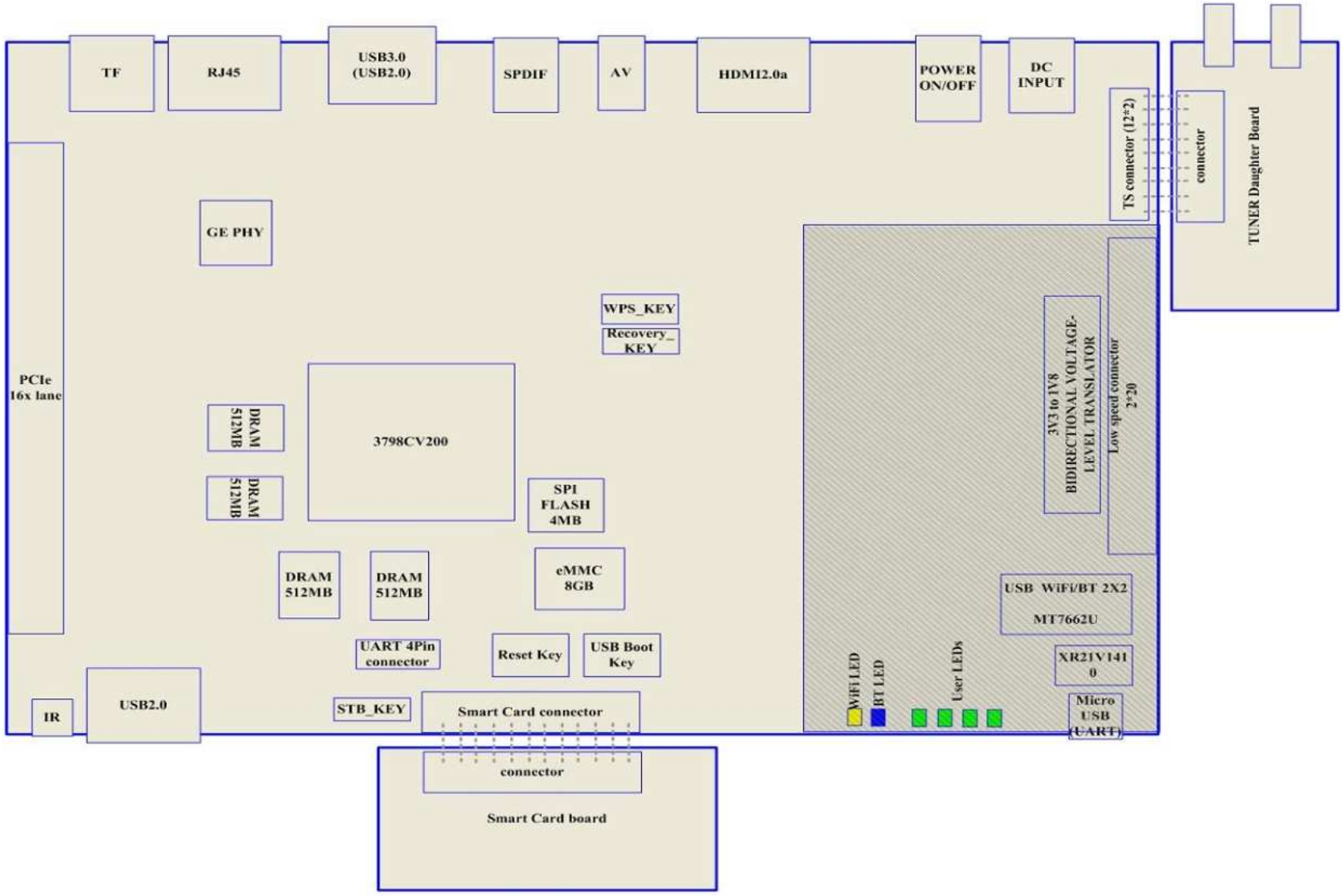
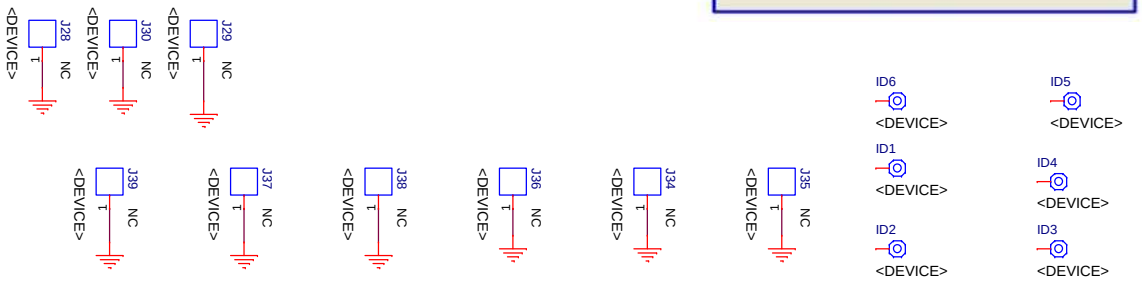
Block Diagram





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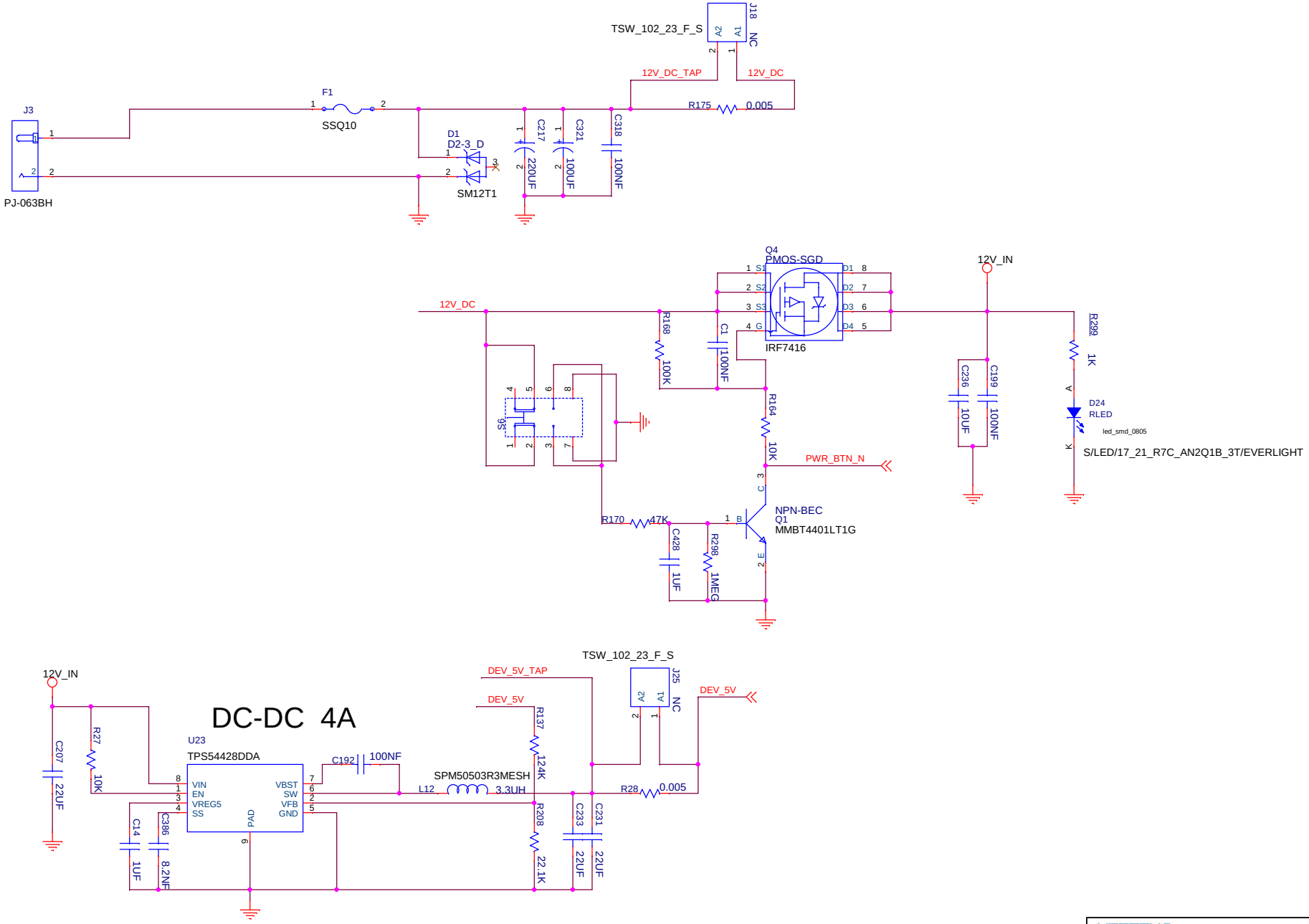
Power on board



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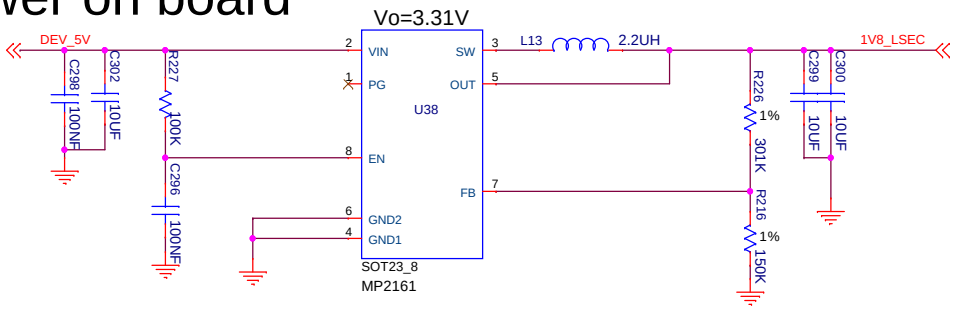
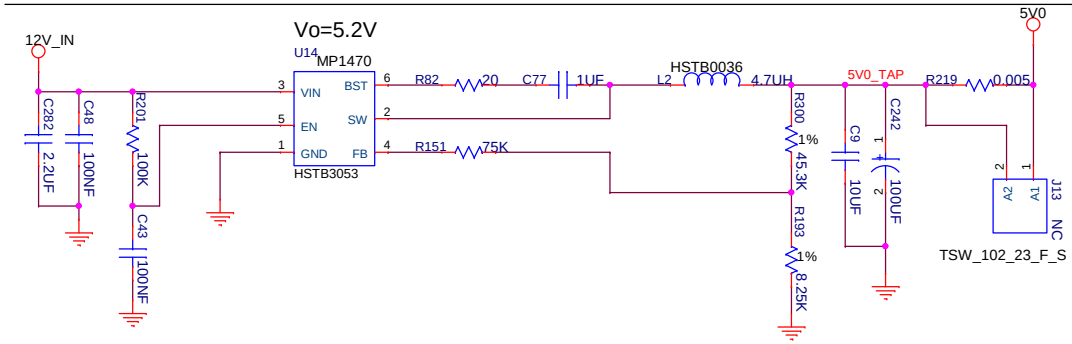
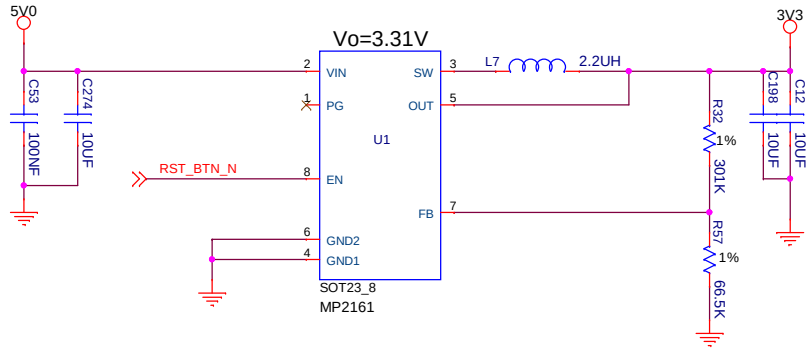
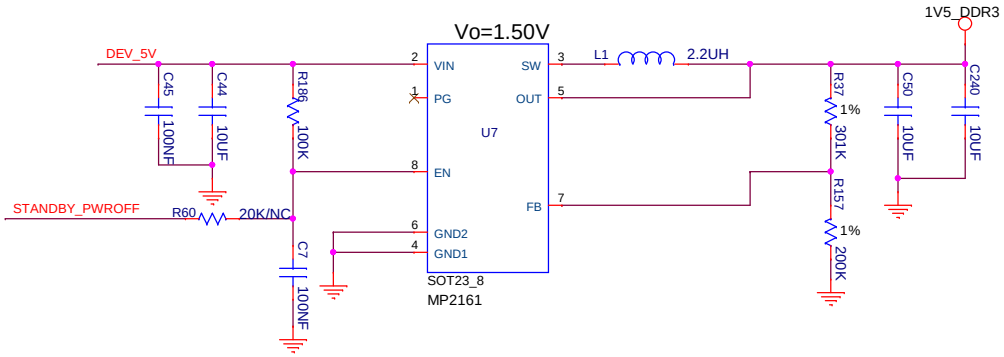
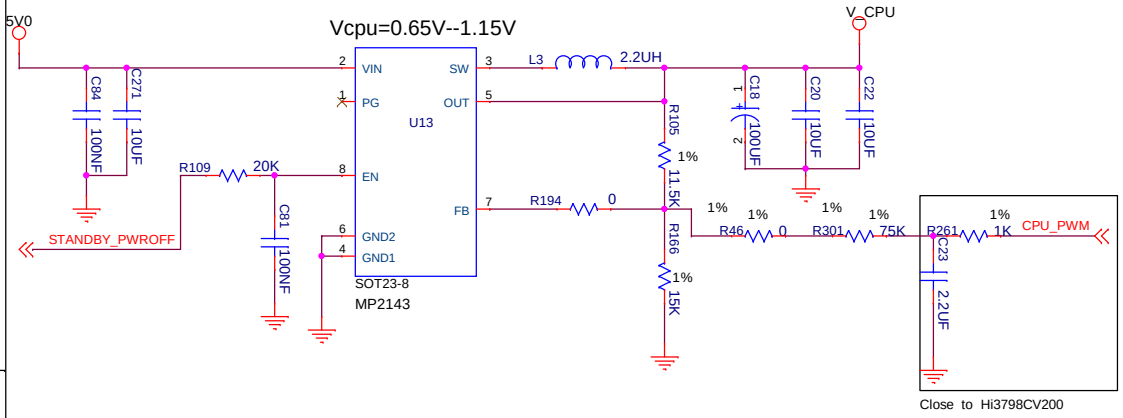
Power on board



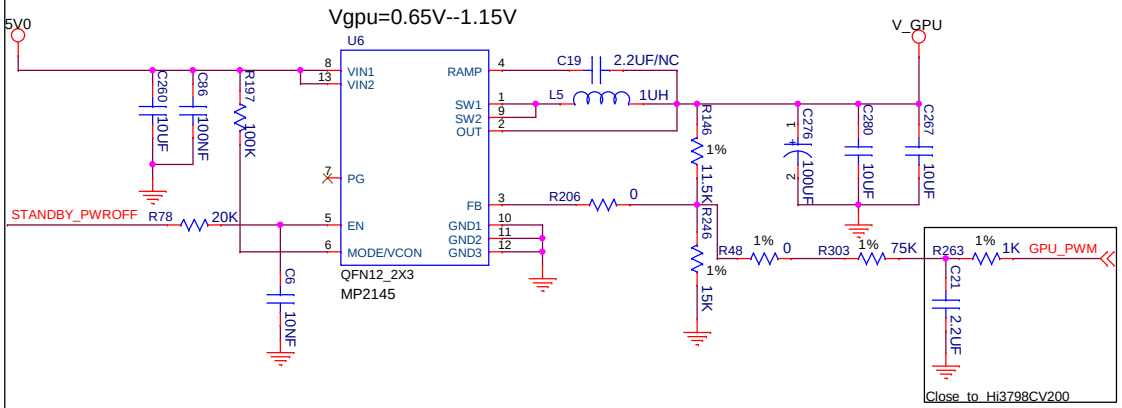








The 3A DC-DC with fast transient response(such as COT or ACOT control) must be selected for the CPU power.



The 4A DC-DC with fast transient response(such as COT or ACOT control) must be selected for the GPU power.

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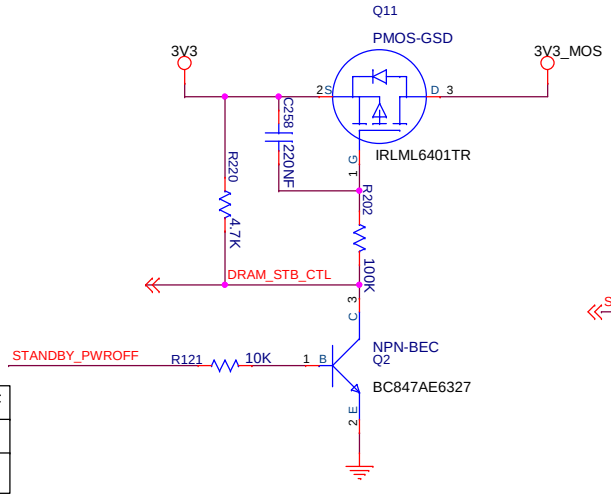
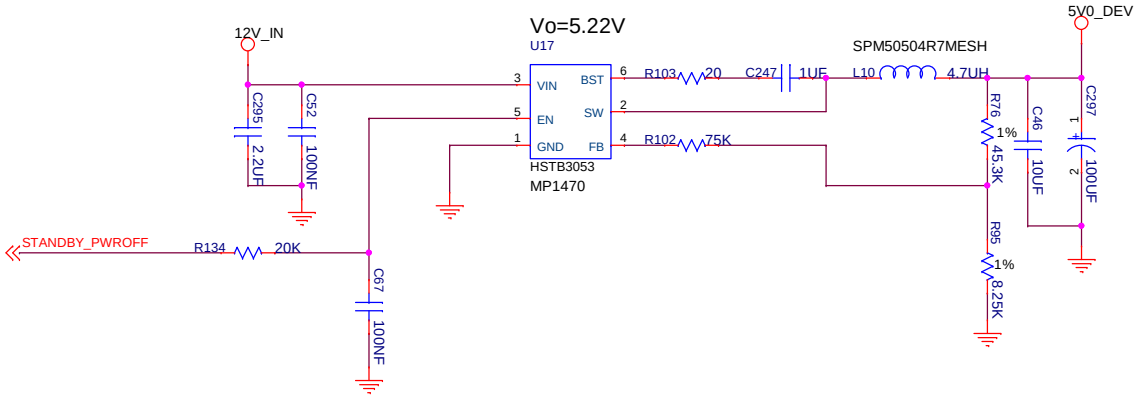
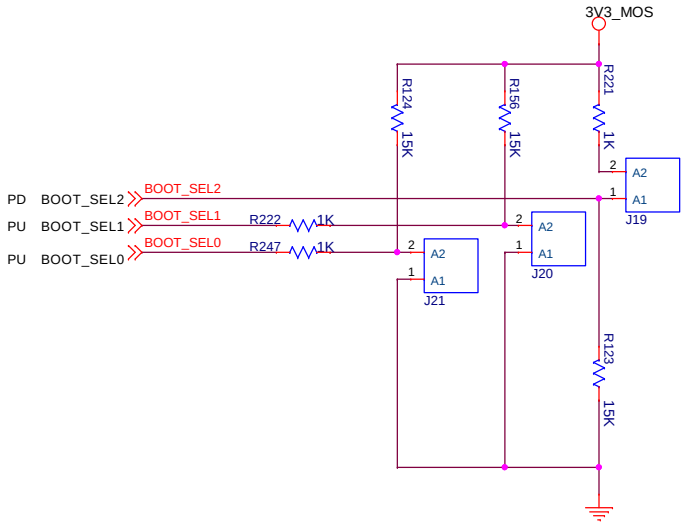
Power Ctrl



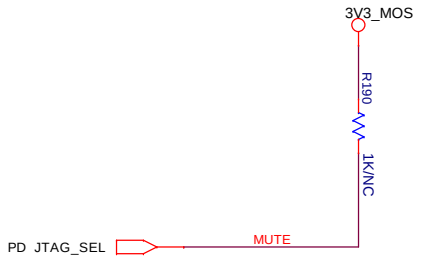
STANDBY_PWROFF	
0	Power Off
1	Power On



BOOT_SEL[2:0]	BOOT FROM
000	SPI NOR
001	NAND FLASH
010	tSD
011	eMMC(default)
100	SPI NAND
Others	Reserved



JTAG_SEL	Function
0	JTAG/TSI SEL By PIN_MUX (default)
1	JTAG



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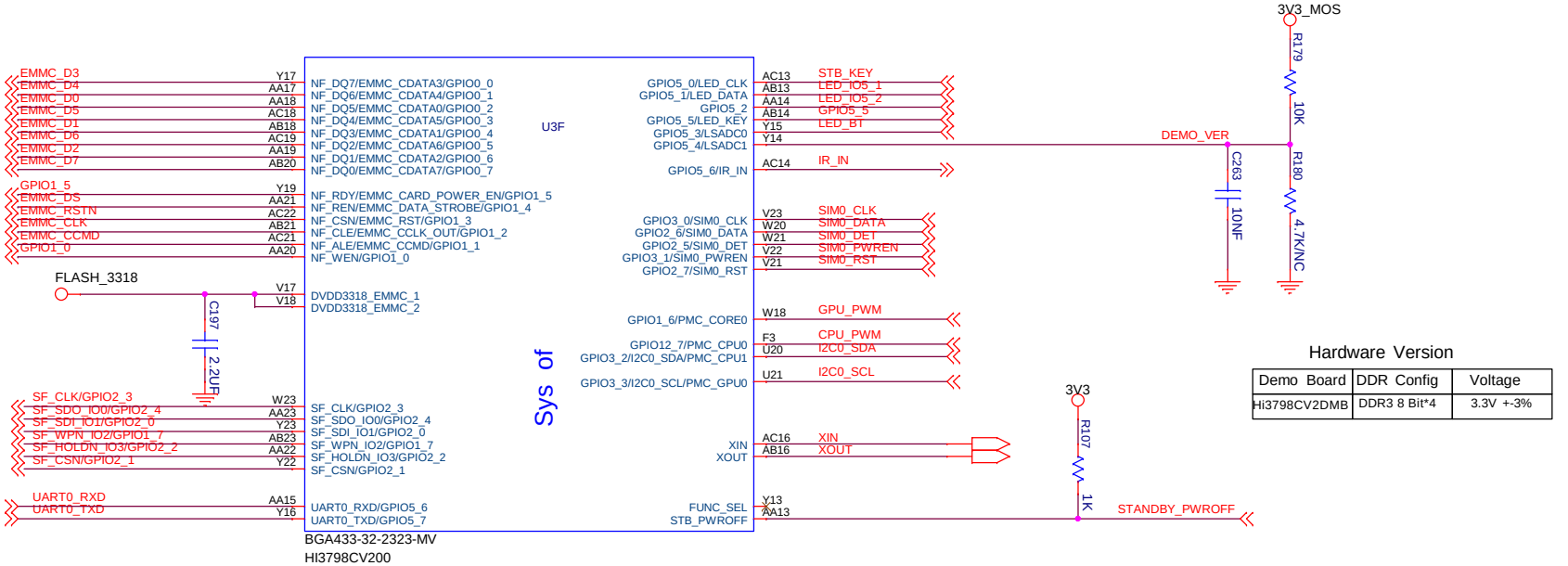
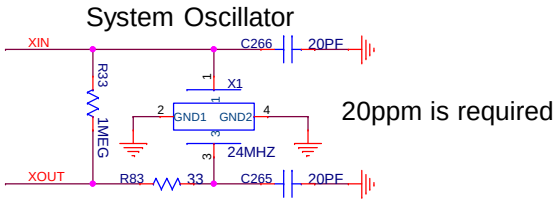
Unit 1 of Hi3798CV200(FLASH/UART/IR/PWM/XTAL)

*****Low Speed ADC Information*****
Input Voltage Range: 0V - 3.3V(> 3.63V is forbidden)
LSADC0: used as Key input or Power detected
LSADC1: used as Hardware Version detected



Hardware Version

Demo Board	DDR Config	Voltage
Hi3798CV2DMB	DDR3 8 Bit*4	3.3V +-3%



20ppm is required

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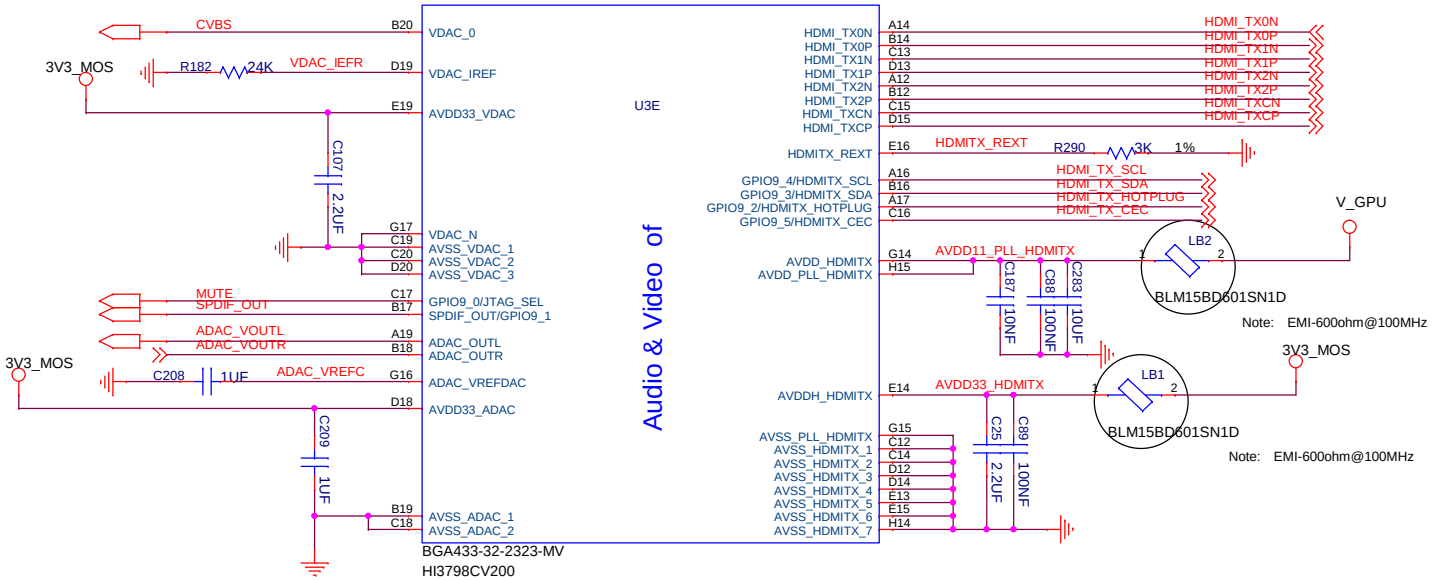
Unit 2 of Hi3798CV200(HDMI TX/VDAC/ADAC)

** HDMI Design guideline **

A.routing
1.Route as 100 Ohm differential impedance.
2.Differential pairs should be routed on TOP layer only.

B.trace length
1.The length for the differential pairs should be less than 5 inches.
2.Match trace length of differential pairs, 5 mils max within a pair.

C.component selection
1.REXT resistor should be 3K Ohm +/-1%.
2.ESD components are suggested for ports protection.
3.All equivalent capacitance of ESD components should be < 0.35pF.



** Audio & Video Design guideline **

A.VIDEO
1.VIDEO REXT resistor should be 12K +/-1% precision for full current model, and 24K +/-1% precision for quarter current model
2.REXT/COMP should be traced as short as possible, and isolated from all other traces.

B.AUDIO
1.VREF should be traced as short as possible, and isolated from all other traces.

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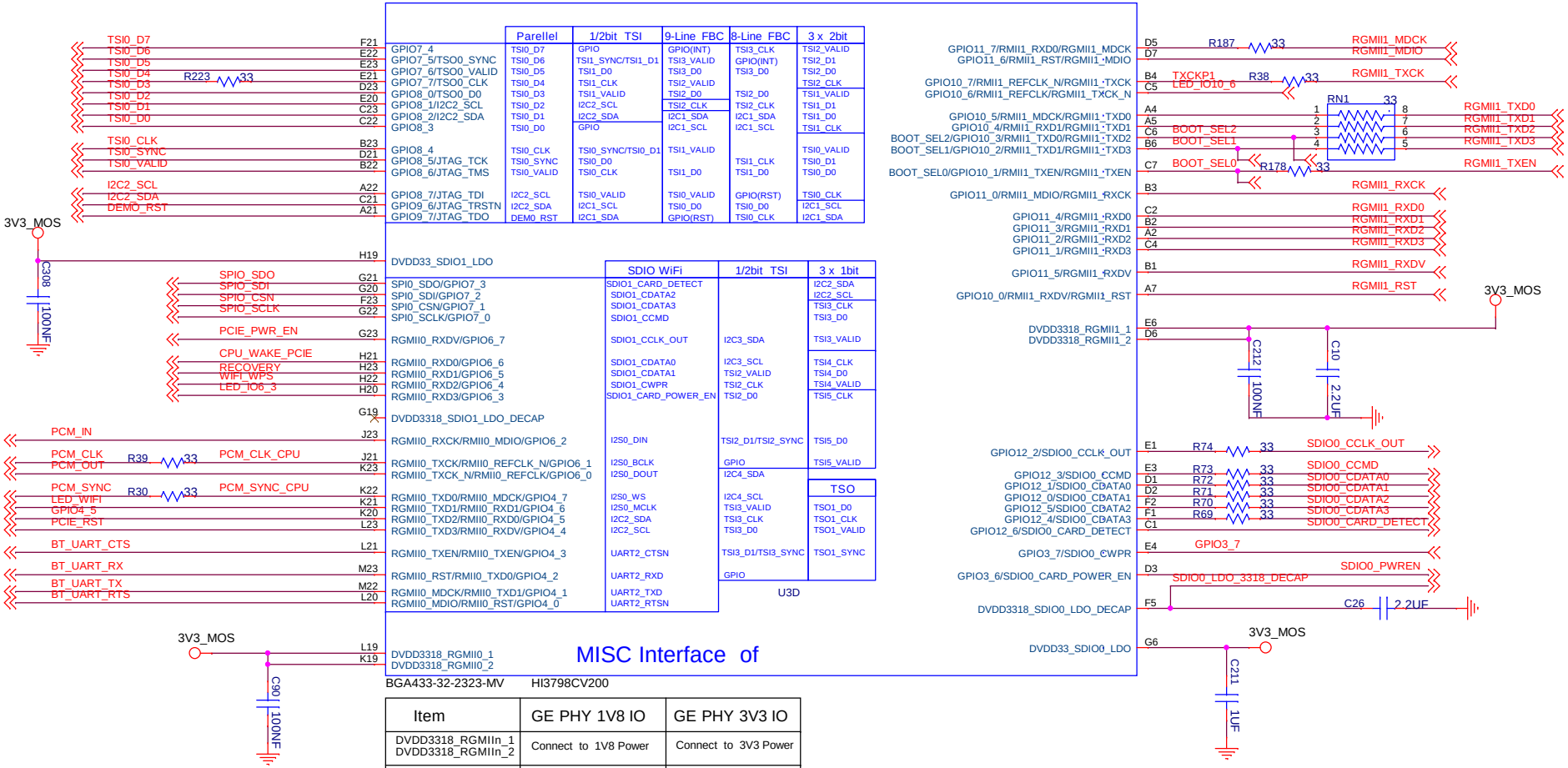
Unit 3 of Hi3798CV200(RGMII/RMII/SDIO/TS)



Item	GE PHY 1V8 IO	GE PHY 3V3 IO
DVDD3318_RGMIIn_1 DVDD3318_RGMIIn_2	Connect to 1V8 Power	Connect to 3V3 Power
Pin Mux Setting in HiRegBin Tool	RGMIIn_TXEN_1V8 RGMIIn_TXD3_1V8 RGMIIn_TXD2_1V8 RGMIIn_TXD1_1V8 RGMIIn_TXD0_1V8 RGMIIn_TXCK_1V8	RGMIIn_TXEN RGMIIn_TXD3 RGMIIn_TXD2 RGMIIn_TXD1 RGMIIn_TXD0 RGMIIn_TXCK

Note: n=0,1 for RGMII0 & RGMII1

***** Design Notes *****

1. DVDD33_SDIO1_LDO is the Input of the inside LDO which is power supply for IO of SDIO1, and DVDD3318_SDIO1_LDO_DECAP is the decap pin of the LDO, connect 2.2uF to GND if 1V8 IOs are needed, others NC is OK.
2. DVDD3318_RGMII0 is the power supply pin of J23/J21/K23/K22/K21/K20/L23/L21/M23/M22/L20, connect to 1V8 power if 1V8 IOs are needed, or connect to 3V3 power.

eg1. if SDIO1 is used as SDIO3.0, DVDD33_SDIO1_LDO should be connected to 3V3 power, DVDD3318_SDIO1_LDO_DECAP should be connect 2.2uF to GND.

eg2. if RGMII0 in 1V8 IOs is used, DVDD33_SDIO1_LDO should be connected to 3V3 power, DVDD3318_SDIO1_LDO_DECAP should be connect 2.2uF to GND, DVDD3318_RGMII0 should be connect to 1V8.

eg3. All IOs are used as 3V3 IOs, DVDD33_SDIO1_LDO and DVDD3318_RGMII0 should be both connected to 3V3 power, DVDD3318_SDIO1_LDO_DECAP needn't be care, NC is OK.

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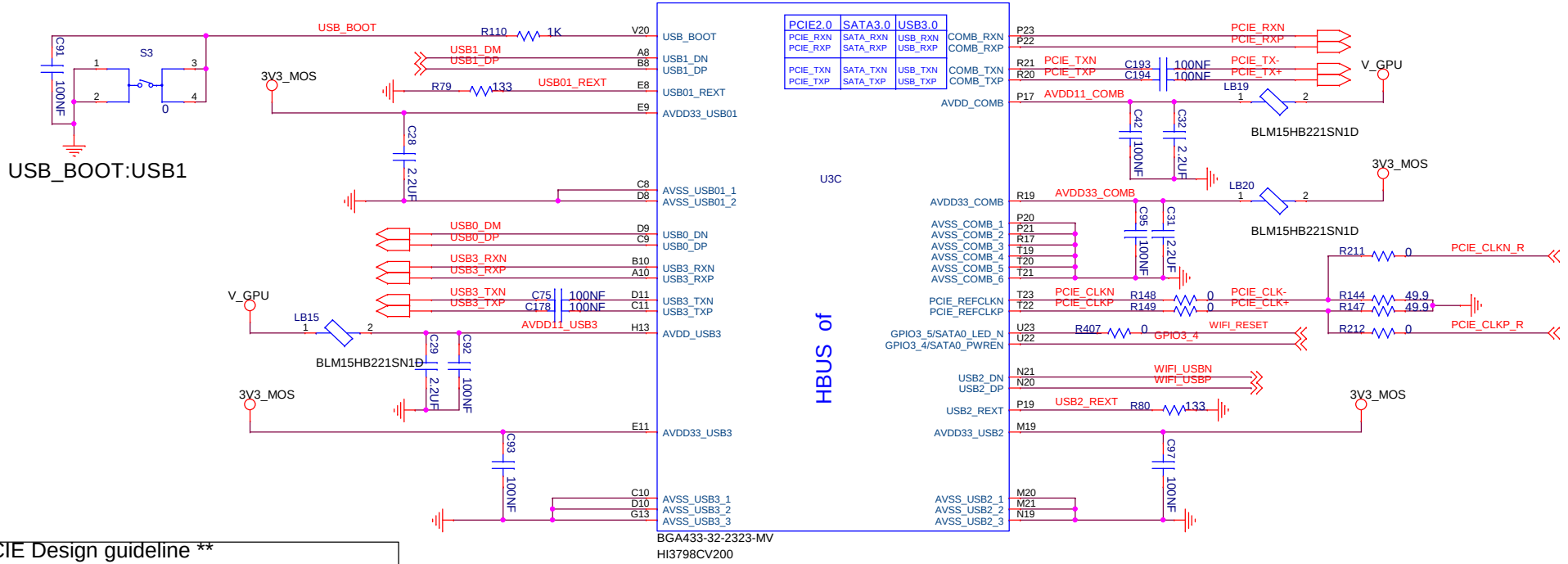
Unit 4 of Hi3798CV200(USB2.0/USB3.0/COMBPHY(SATA/U3/PCIE))



** SATA&PCIE Design guideline **

A.routing

1.Route as 100 Ohm differential impedance.
2.Differential pairs should be routed on TOP layer only.

B.trace length

1.The length for the differential pairs should be less than 5 inches.
2.Match trace length of DP and DM differential pairs, 10 mils max within a pair.

C.component selection

1.SATA:The value of capacitors for AC coupling should be <=12nF,default 10nF
2.PCIE:The value of capacitors for AC coupling should be <=200nF,default 100nF

** USB Design guideline **

A.routing

1.Route as 90 Ohm differential impedance.
2.Differential pairs should be routed on TOP layer only.

B.trace length

1.The length for the differential pairs should be less than 5 inches.
2.Match trace length of DP and DM differential pairs, 10 mils max within a pair.

C.component selection

1.USB2.0 REXT resistor should be 133 ohm +/-1% and USB3.0 133 ohm +/-1%
2.ESD components are suggested for ports protection.
3.Equivalent capacitance of ESD component should be < 1.5pF.

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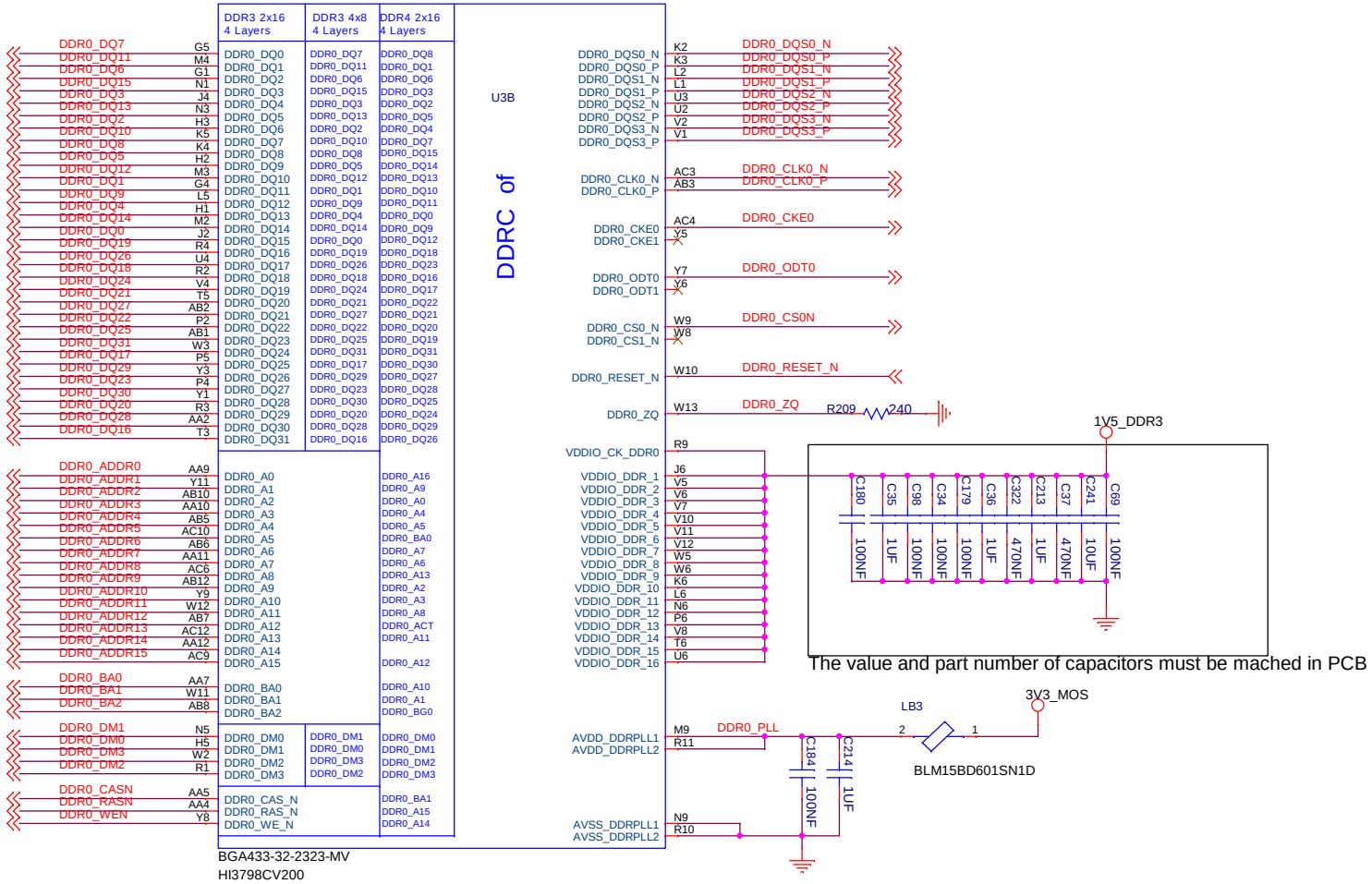
Unit 5 of Hi3798CV200(DDRC)



** DDR Design guideline **

A.general suggestion

1.Hi3798CV200 supports DDR3/DDR3L/DDR4
2.Hi3798CV200 supports up to 2GB DDR3.
3.The ciruit of DDR_VREF_CA and DDR_VREF_DQ must be independent.
4.Please copy the decoupling capacitor design from hisilicon demo board.
5.3V3 DDRPLL is needed.

B.Layout suggestion

1. Please copy hisilicon demo board completely

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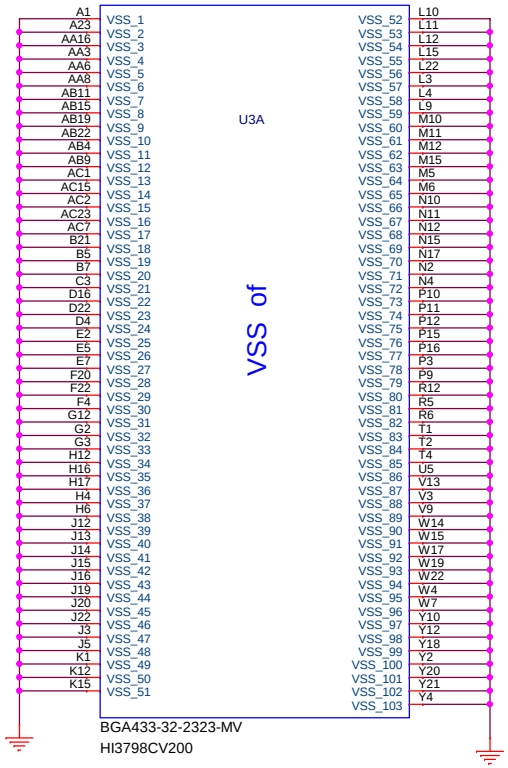
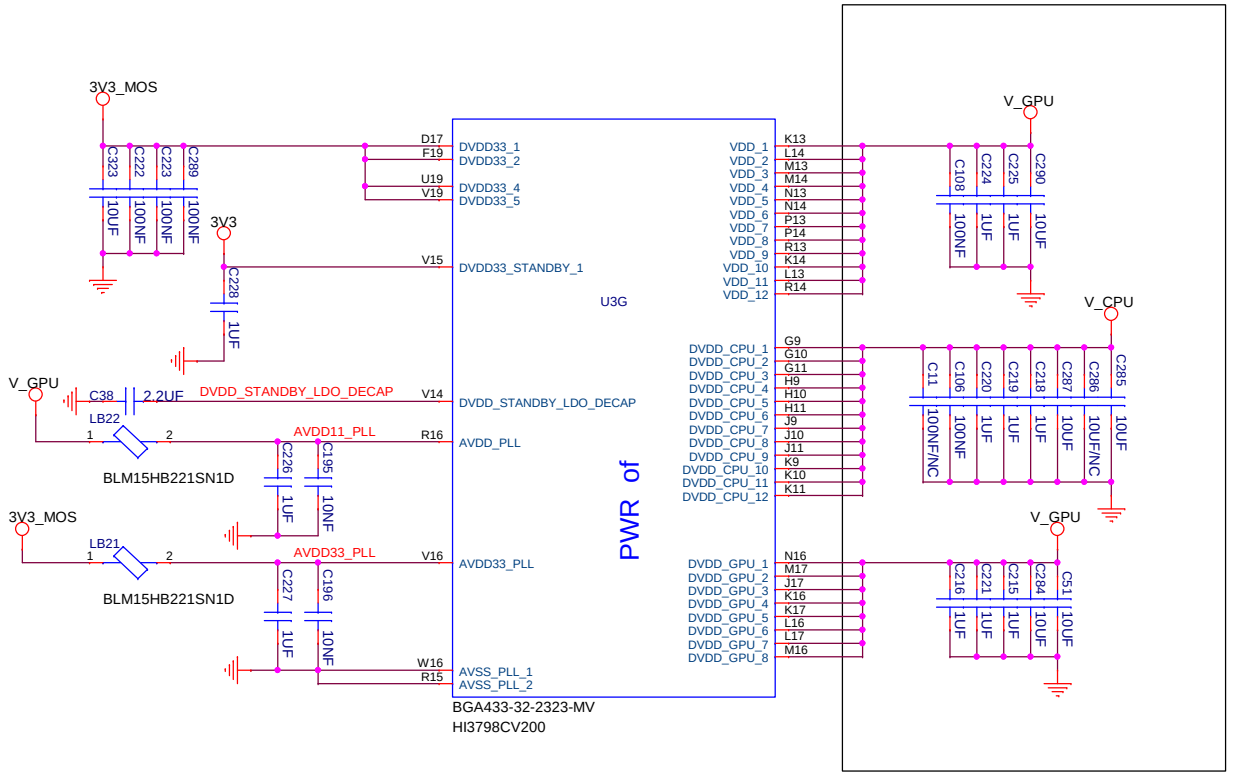
Unit 6 of Hi3798CV200(POWER/VSS)





The value and part number of capacitors must be mached in PCB

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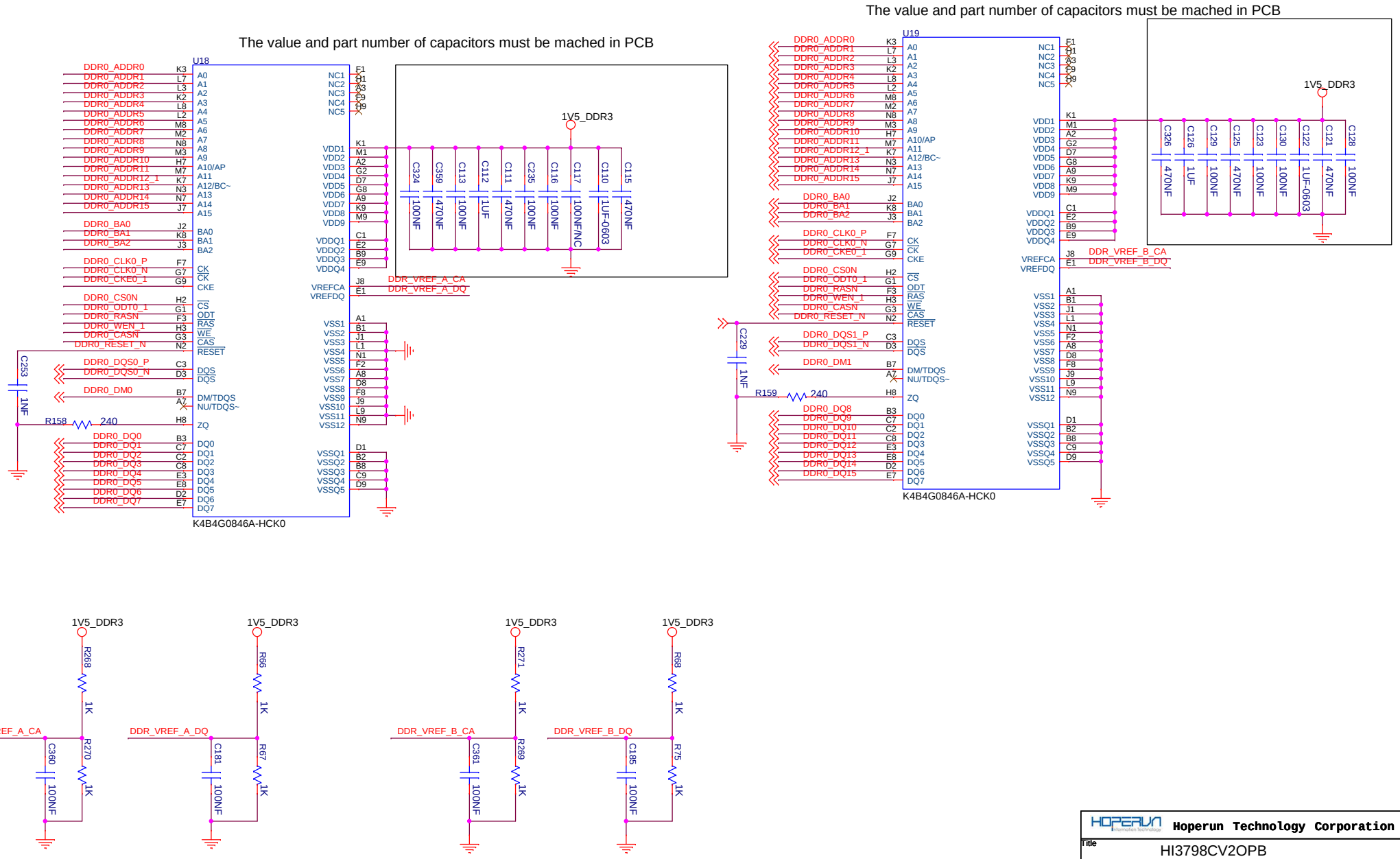
DDR Byte0 & Byte1



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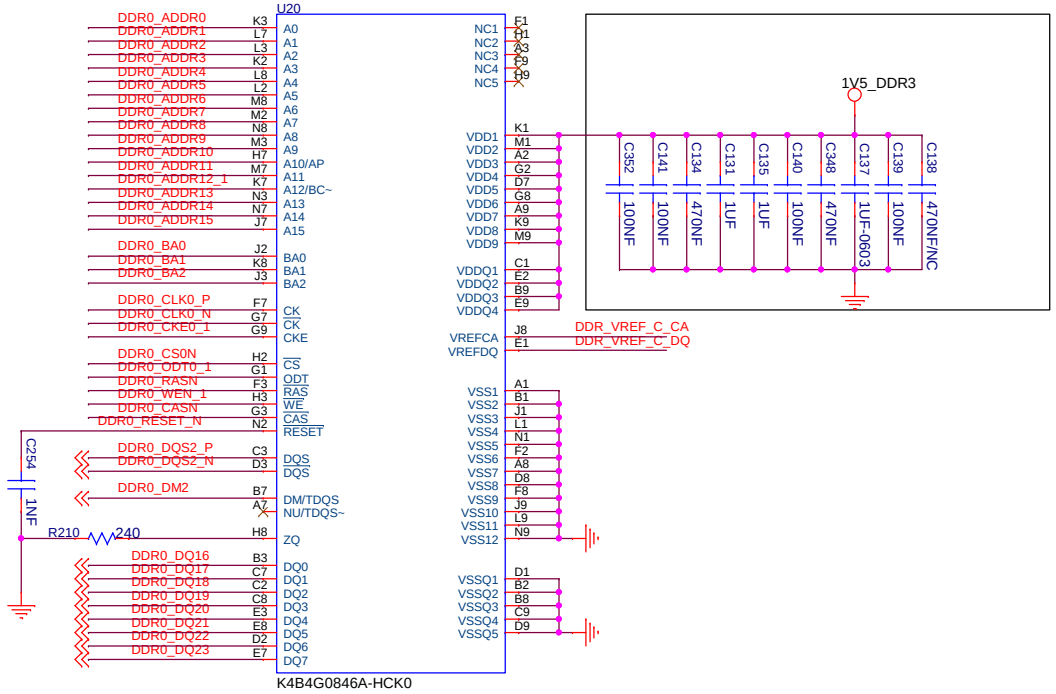
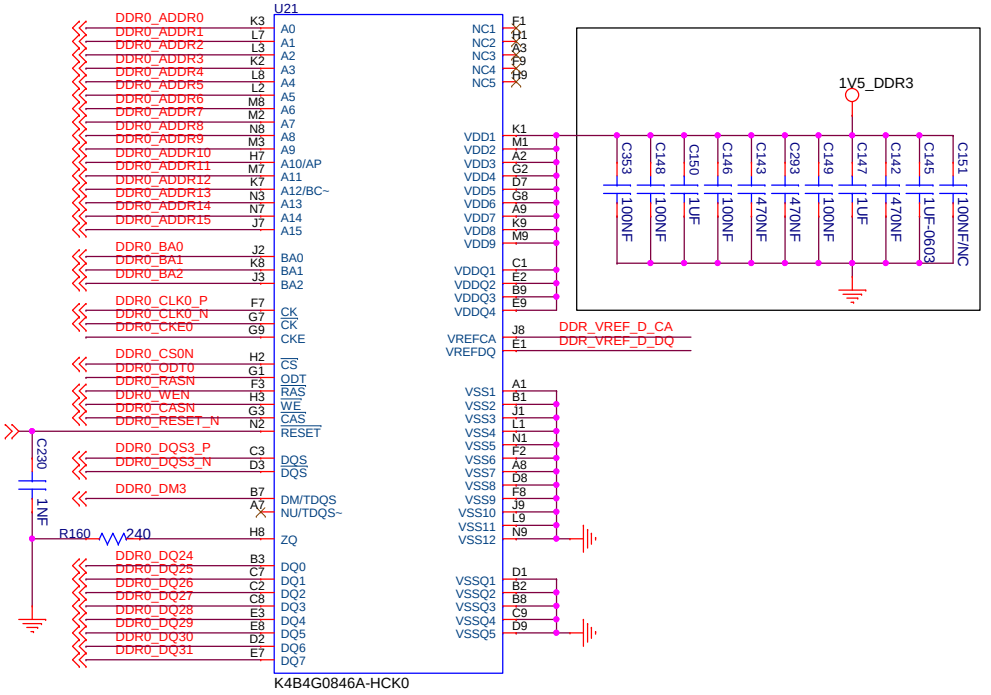
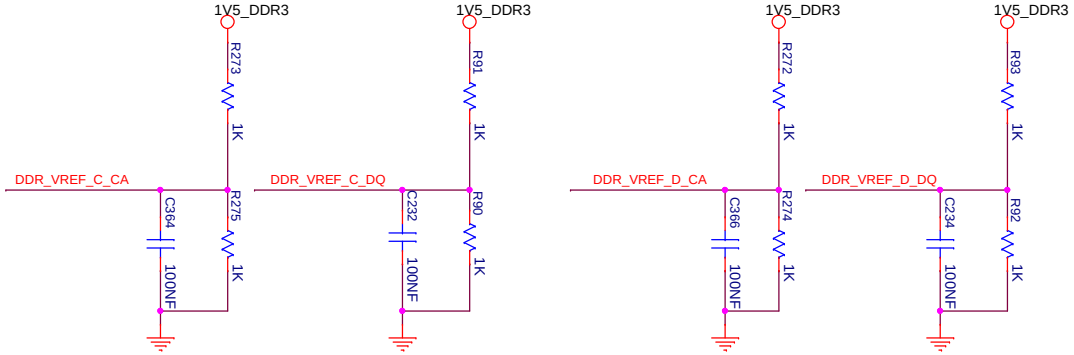
DDR Byte2 & Byte3

The value and part number of capacitors must be mached in PCB



The value and part number of capacitors must be mached in PCB





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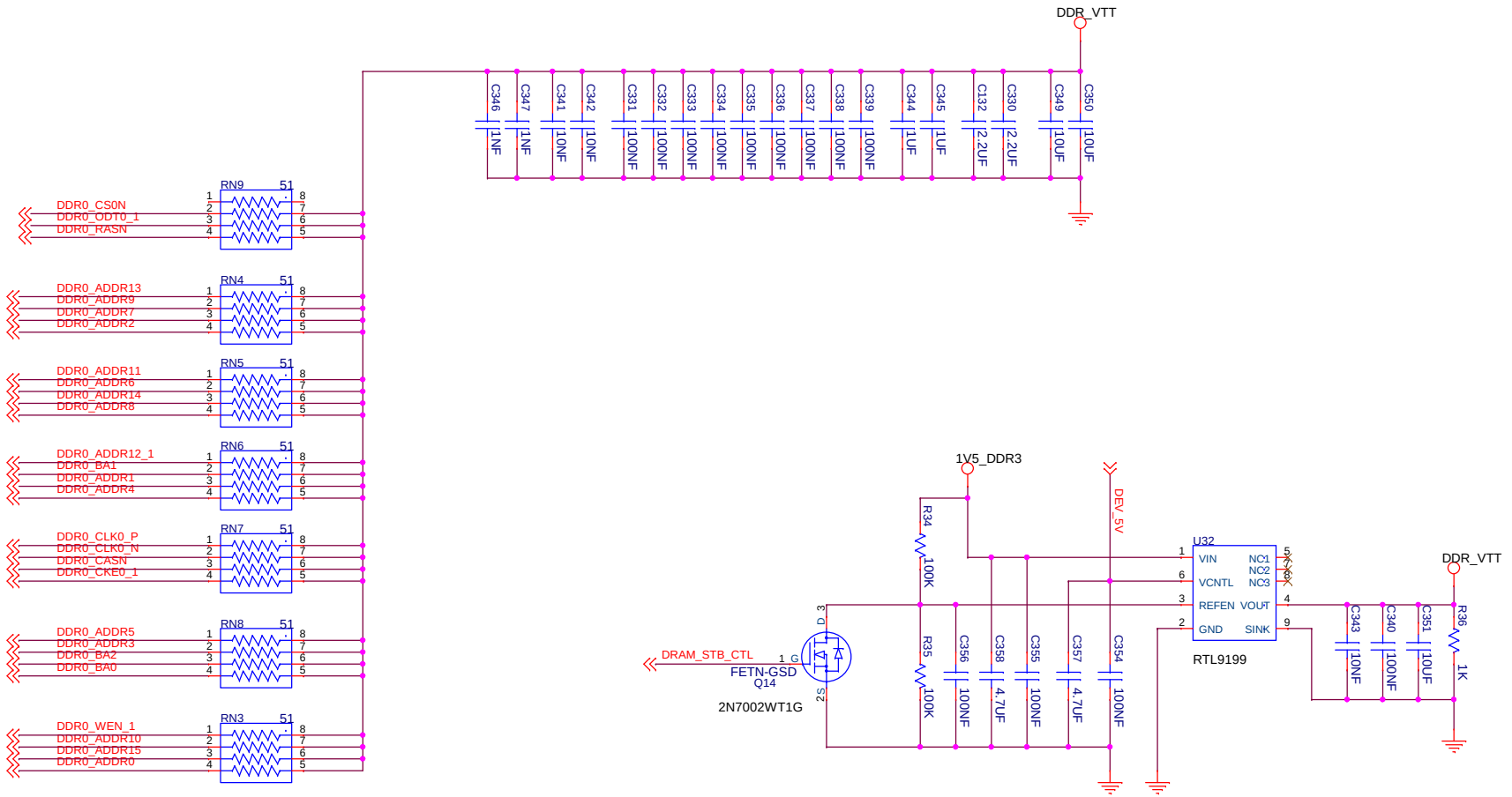
DDR VTT



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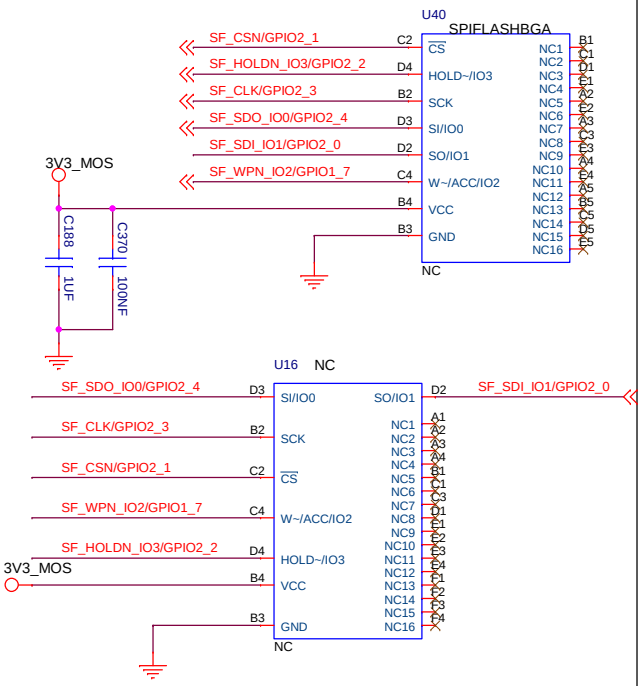
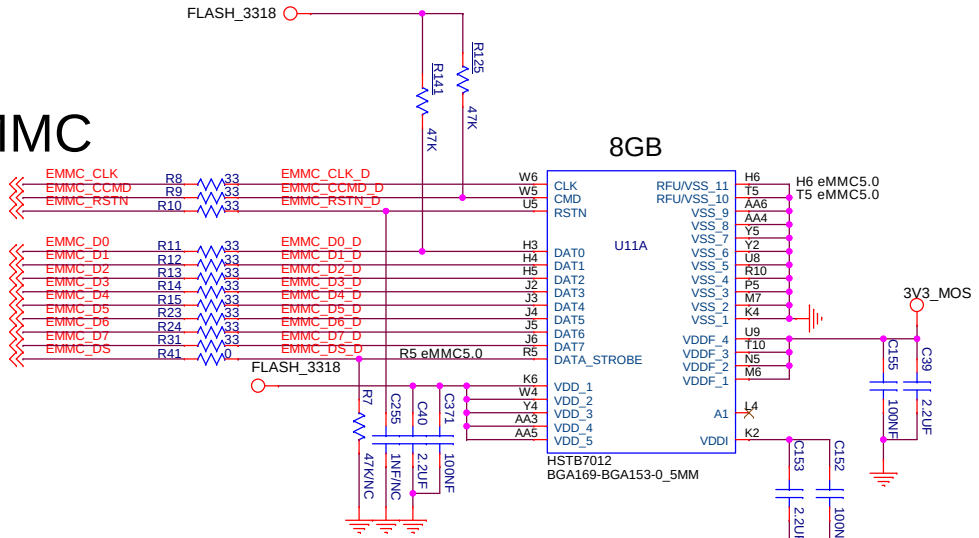
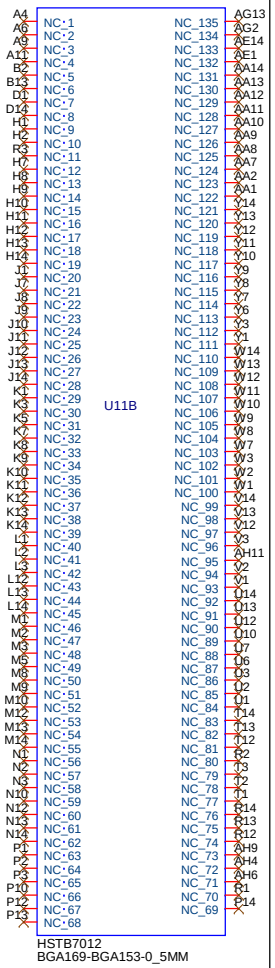
NOR



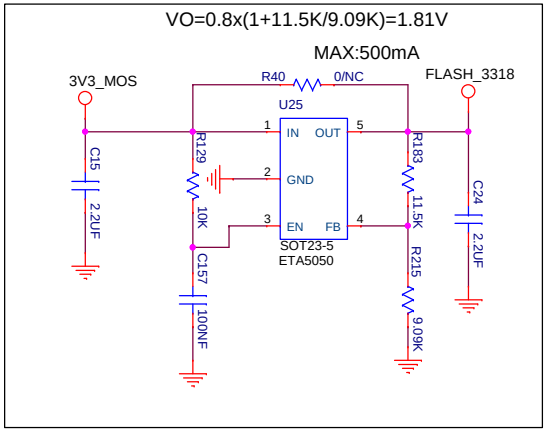
NOR/EMMC





** eMMC design guideline **

1. The different length of CLK, CMD, DAT0-7 and DATA_STROBE must be kept within 200mil.
2. The value of R9 in CMD line must follow the corresponding datasheet for detail



3.3V IO only For eMMC DDR50 Mode

R40 = 0 ohm
others = NC

eMMC5.0(1.8V) default

1.8V IO For eMMC HS200\HS400 Mode

R40 = NC
Others Mounted

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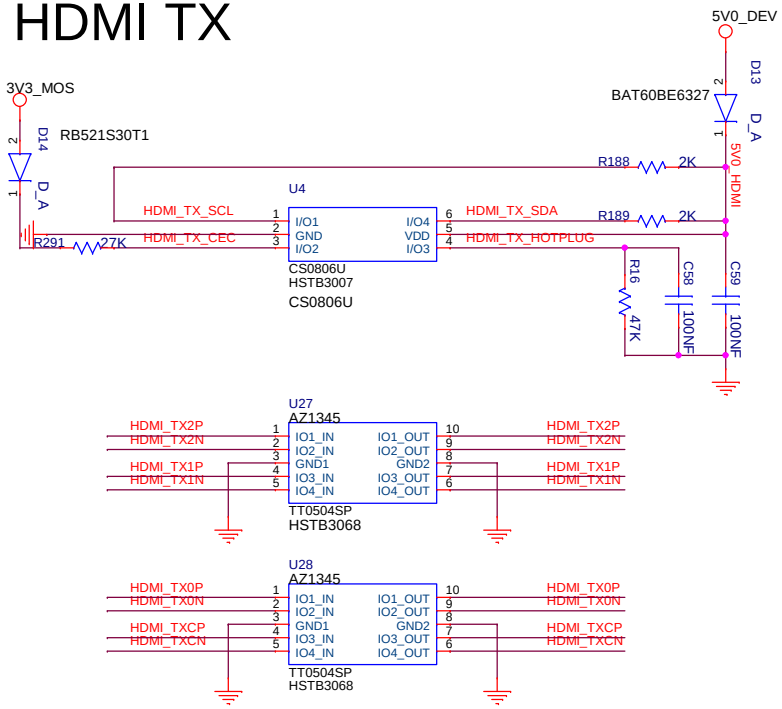
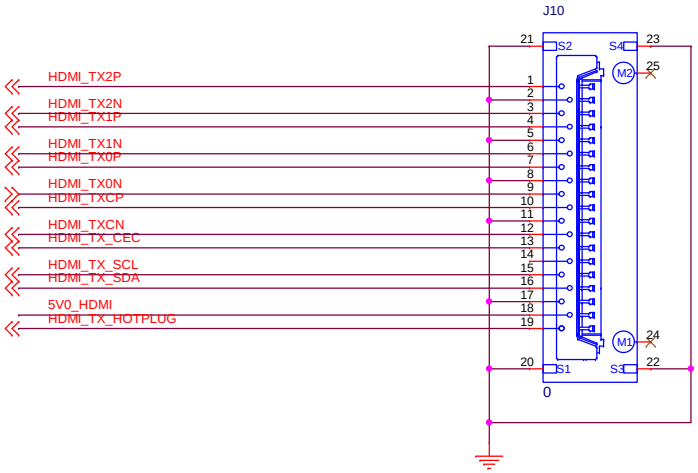
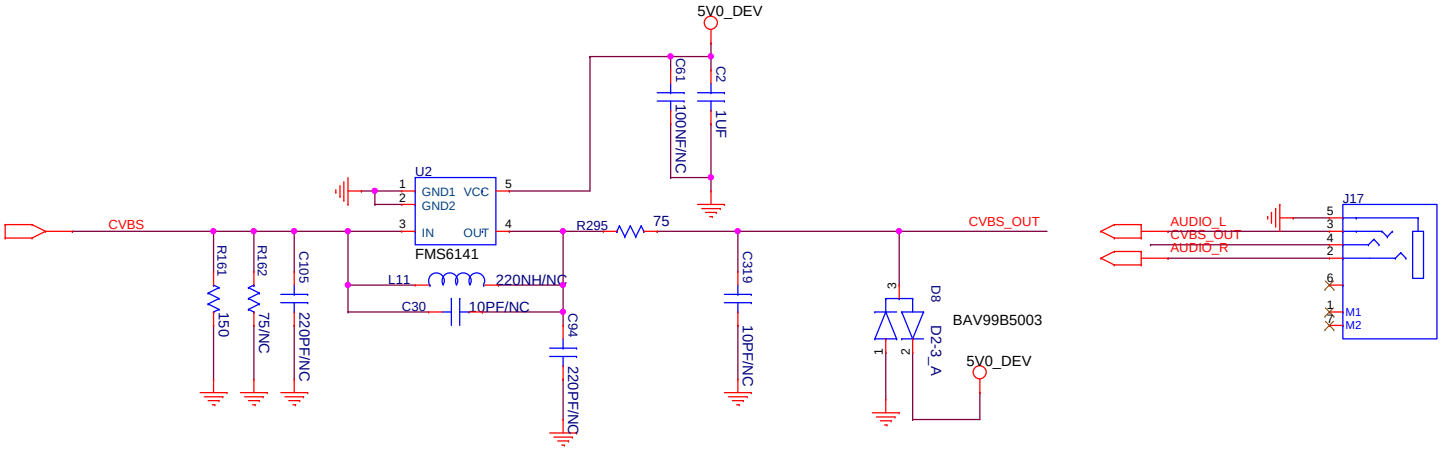
HDMI TX





VIDEO OUTPUT

VIDEO BUFFER	LC Filter
R182 = 24K 1%	R182 = 12K 1%
R161 = 150 1%	R161 = 75 1%
R162 = NC	R162 = NC
C105 = NC	C105 = NC
C30 = NC	C30 = 10PF
L11 = NC	L11 = 220NH
C94 = NC	C94 = 220PF
R295 = 75 1%	R295 = 0
C319 = NC	C319 = NC
C61 = NC	C61 = NC
C2 = 1UF	C2 = NC
U2 = FMS6141	U2 = NC



** Design guideline **

1.All channel traces should be separated from other traces by GND.
2.ESD components are suggested for ports protection, default BAV99.

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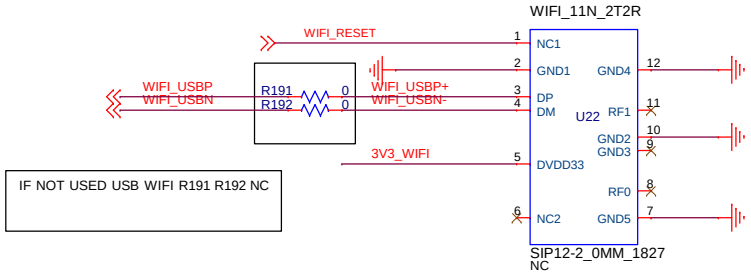
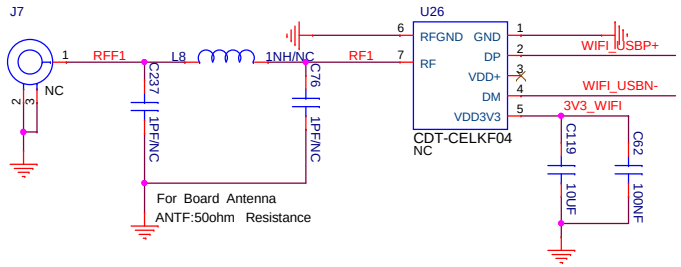
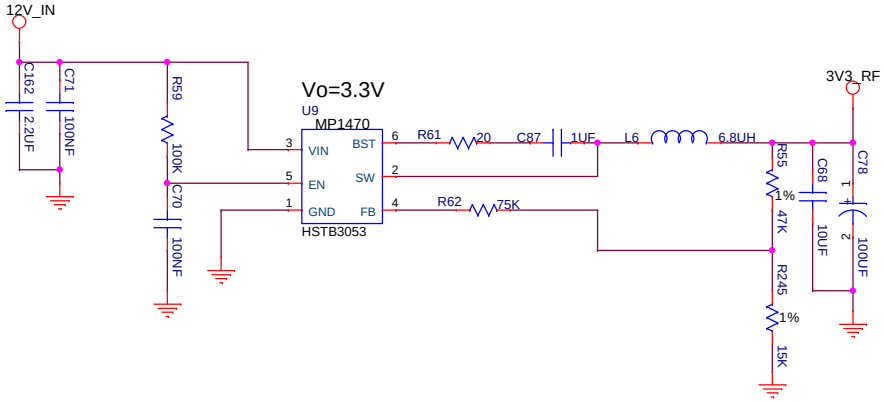
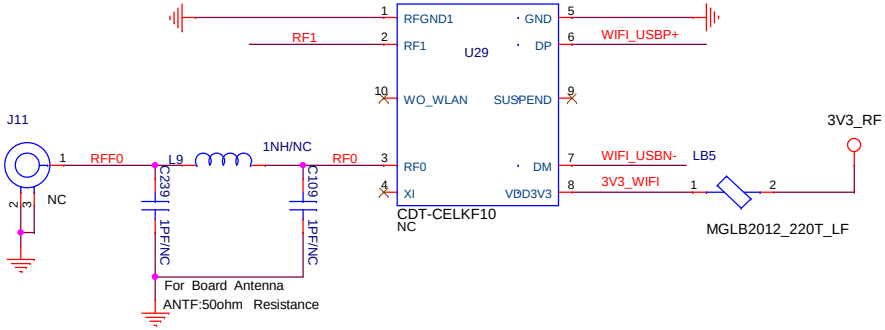
USB WIFI





POWER OF WIFI





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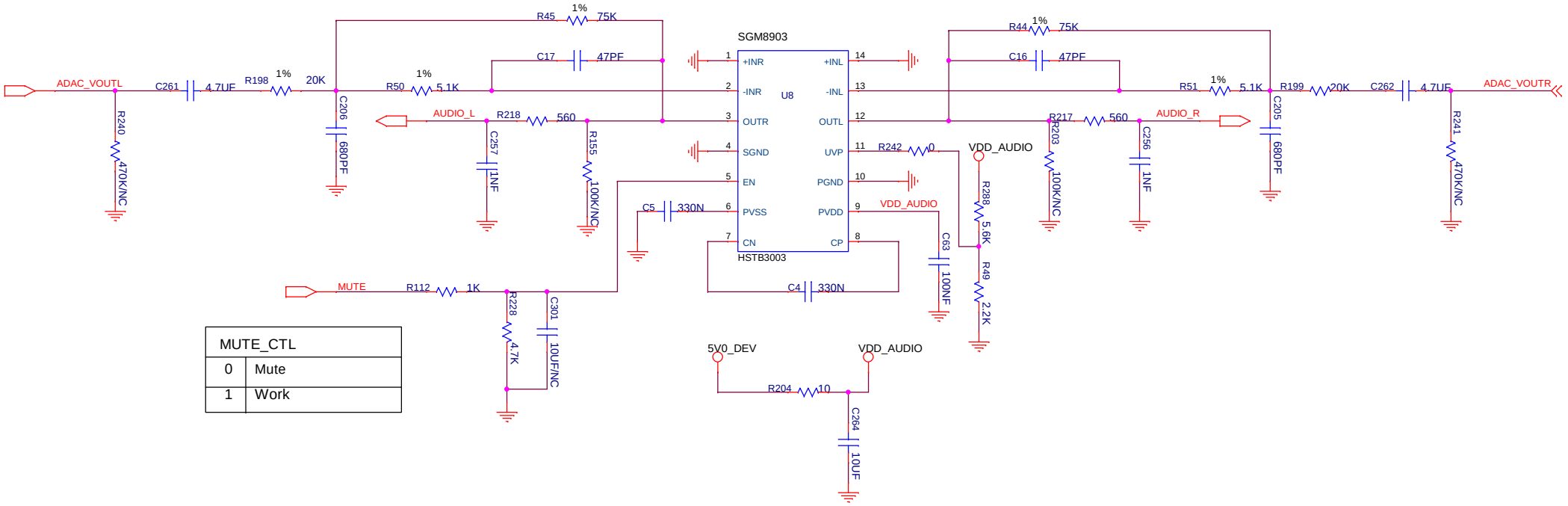
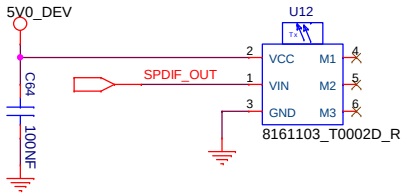
AUDIO OUTPUT



MUTE_CTL	
0	Mute
1	Work

SPDIF



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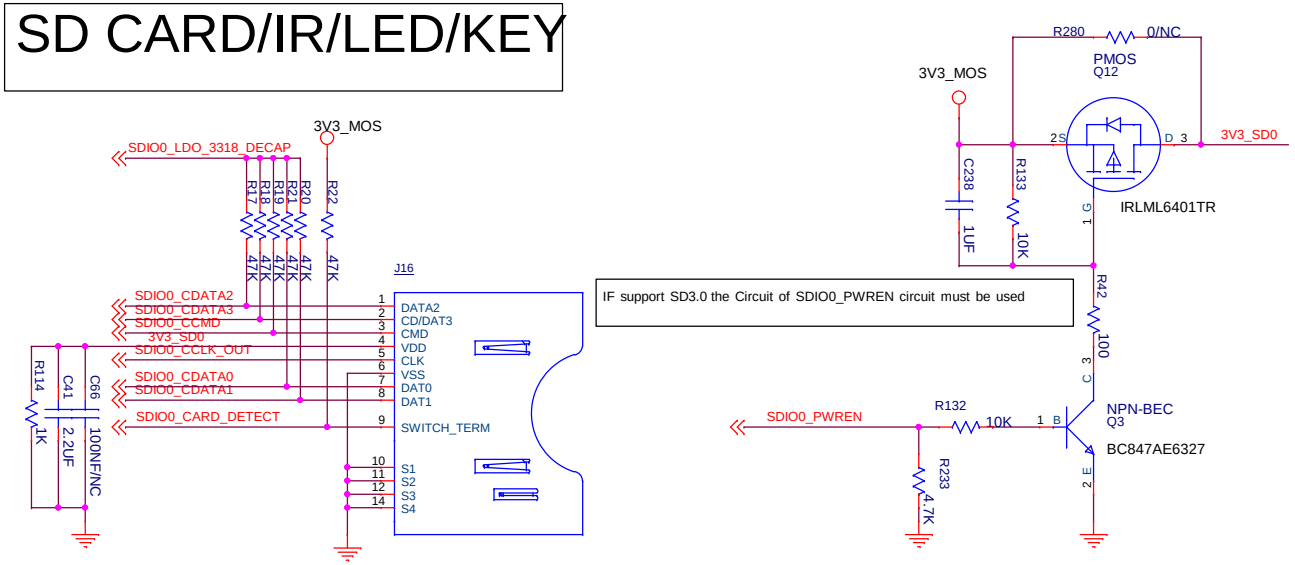
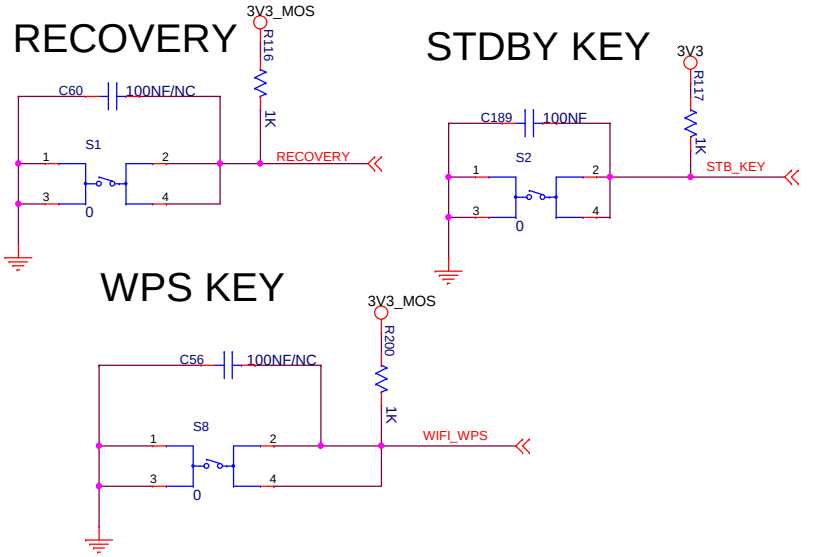
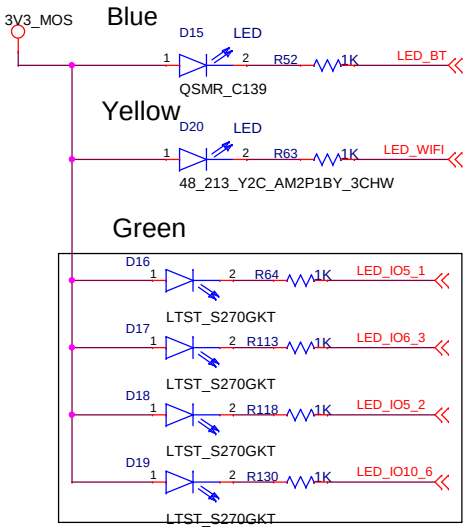
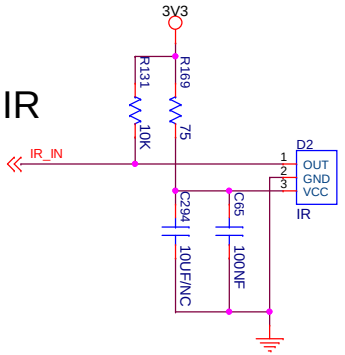
SD CARD/IR/LED/KEY









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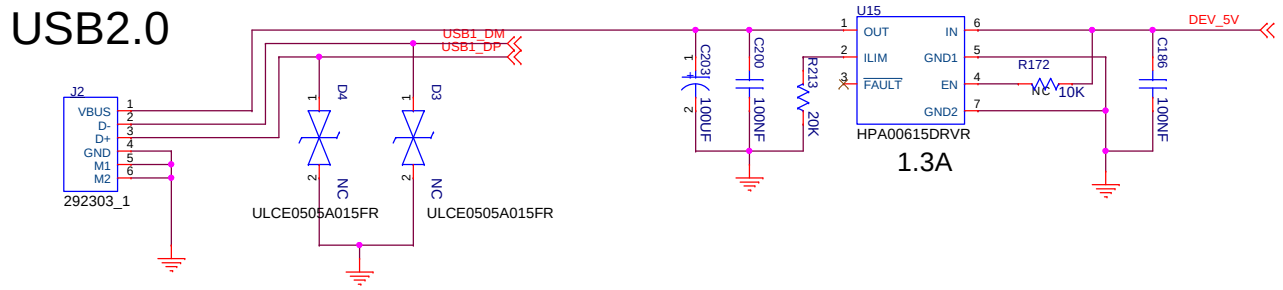
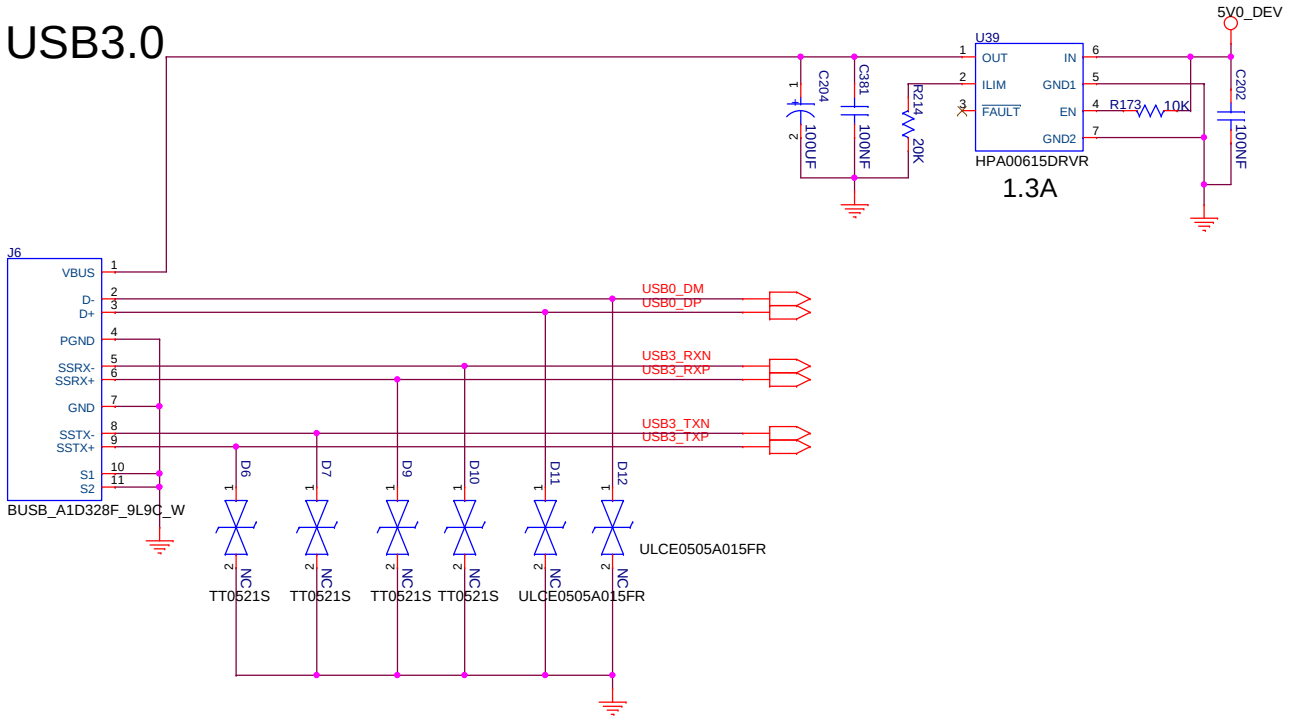
USB2.0 & USB3.0

USB2.0



USB3.0



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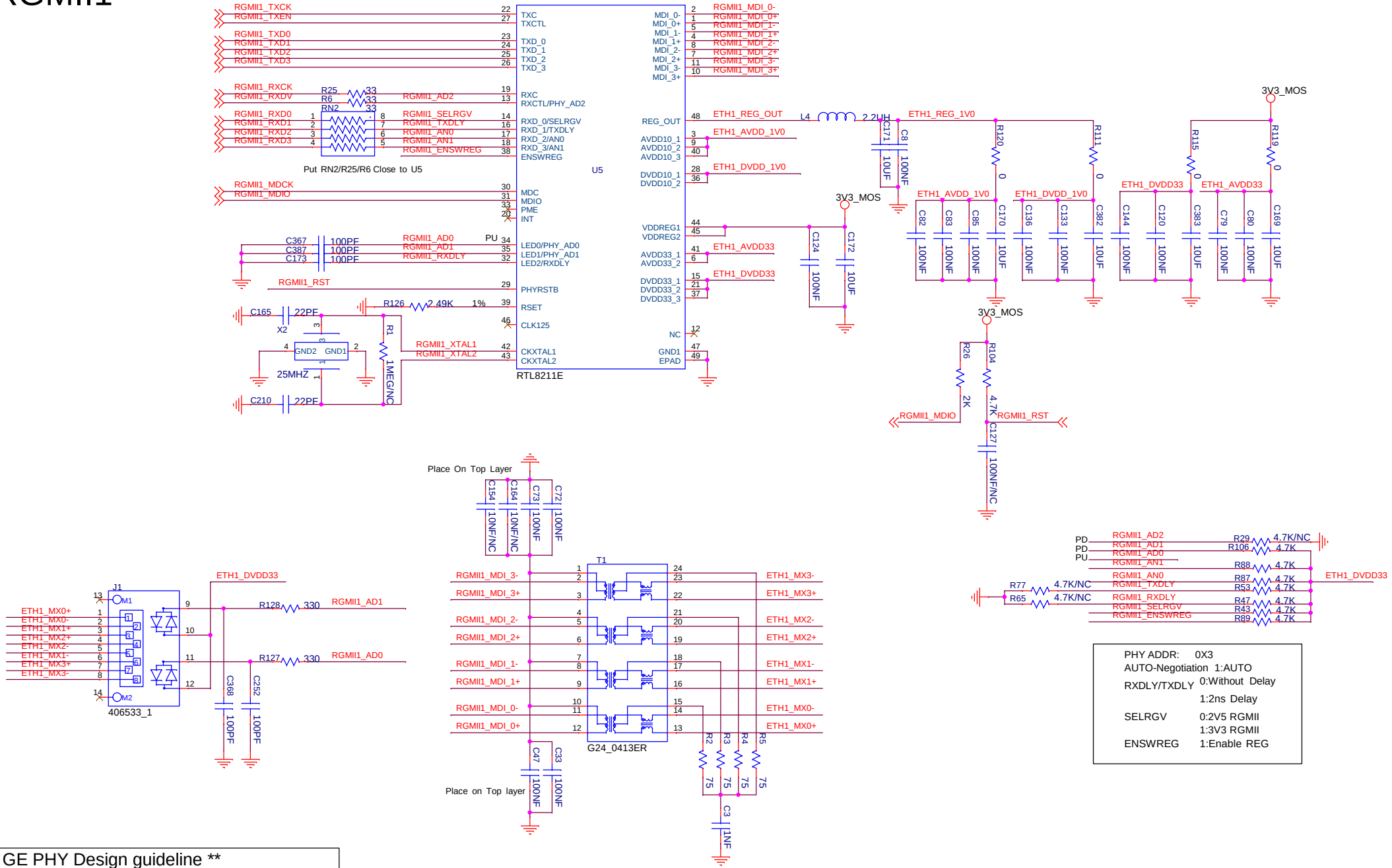
RGMII1



** GE PHY Design guideline **

A.RGMII interface

1.The TXCK and RXCK trace should be separated from other traces by GND.

2.The Power layout of GE PHY should copy Hisilicon demo completely.

3.The RXD[3:0] and TXD[3:0] should be separated from other traces by GND.

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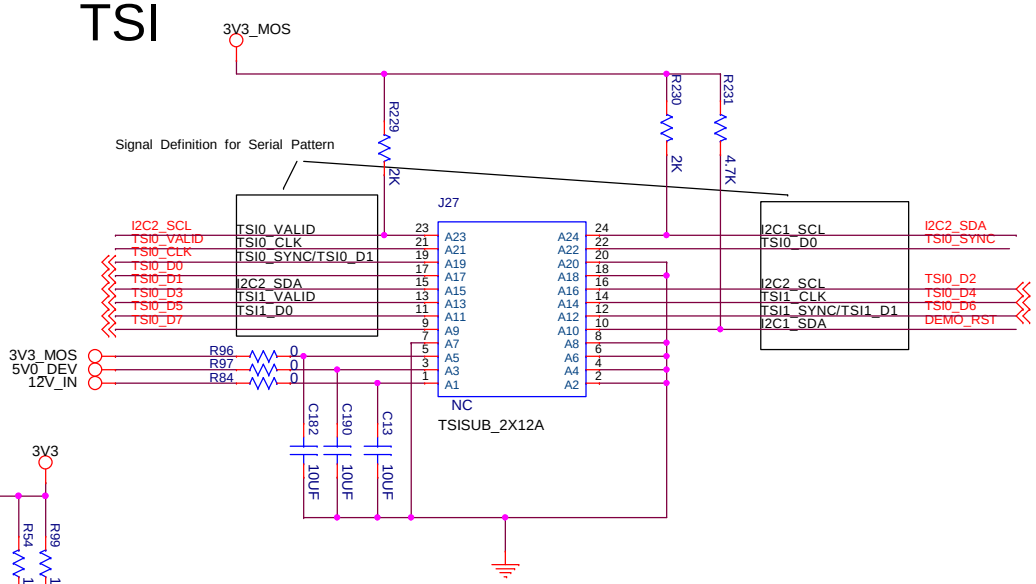
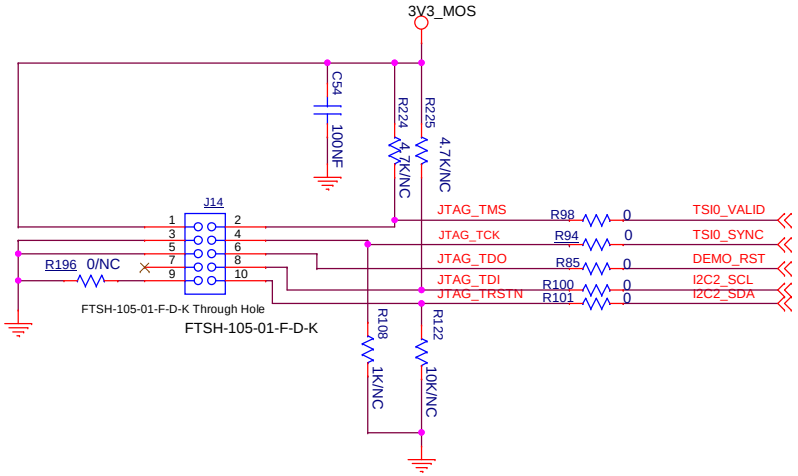
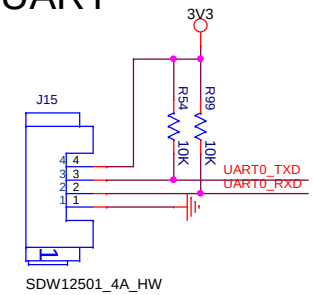
TSI

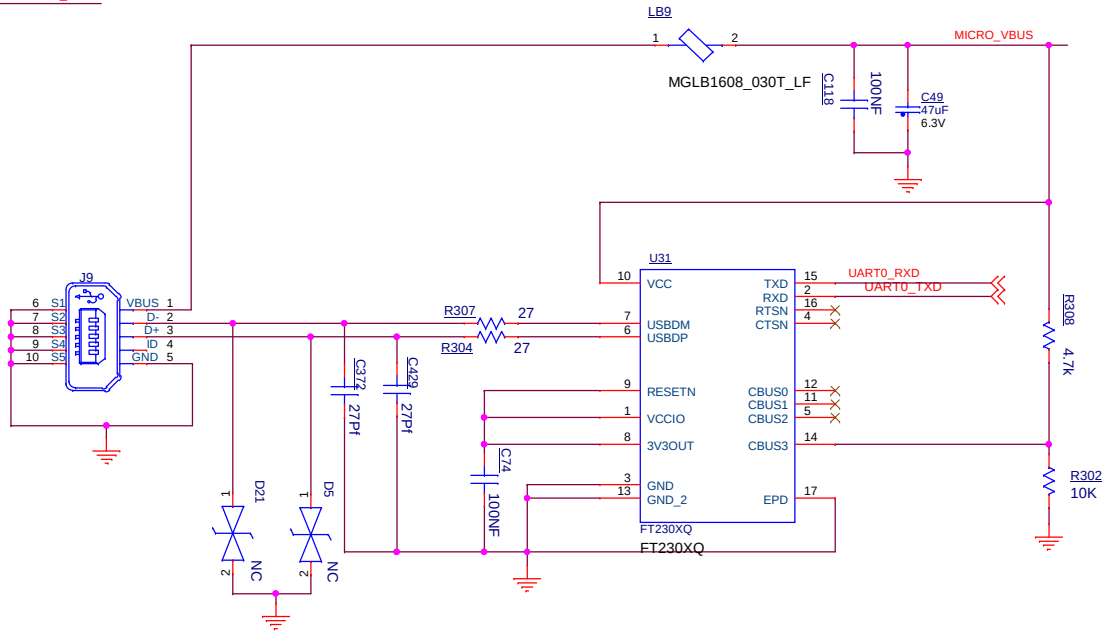


JTAG

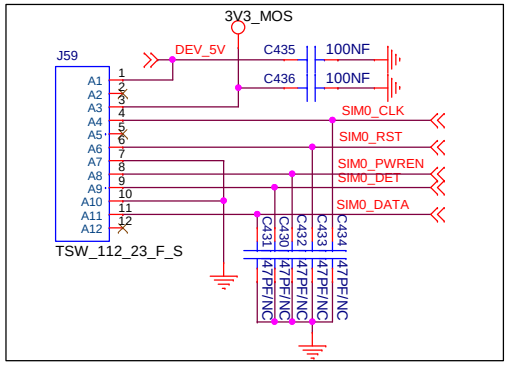


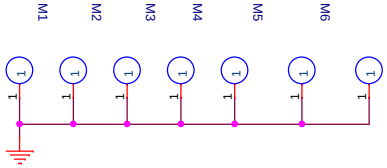
UART





Connector for Smart Card Board





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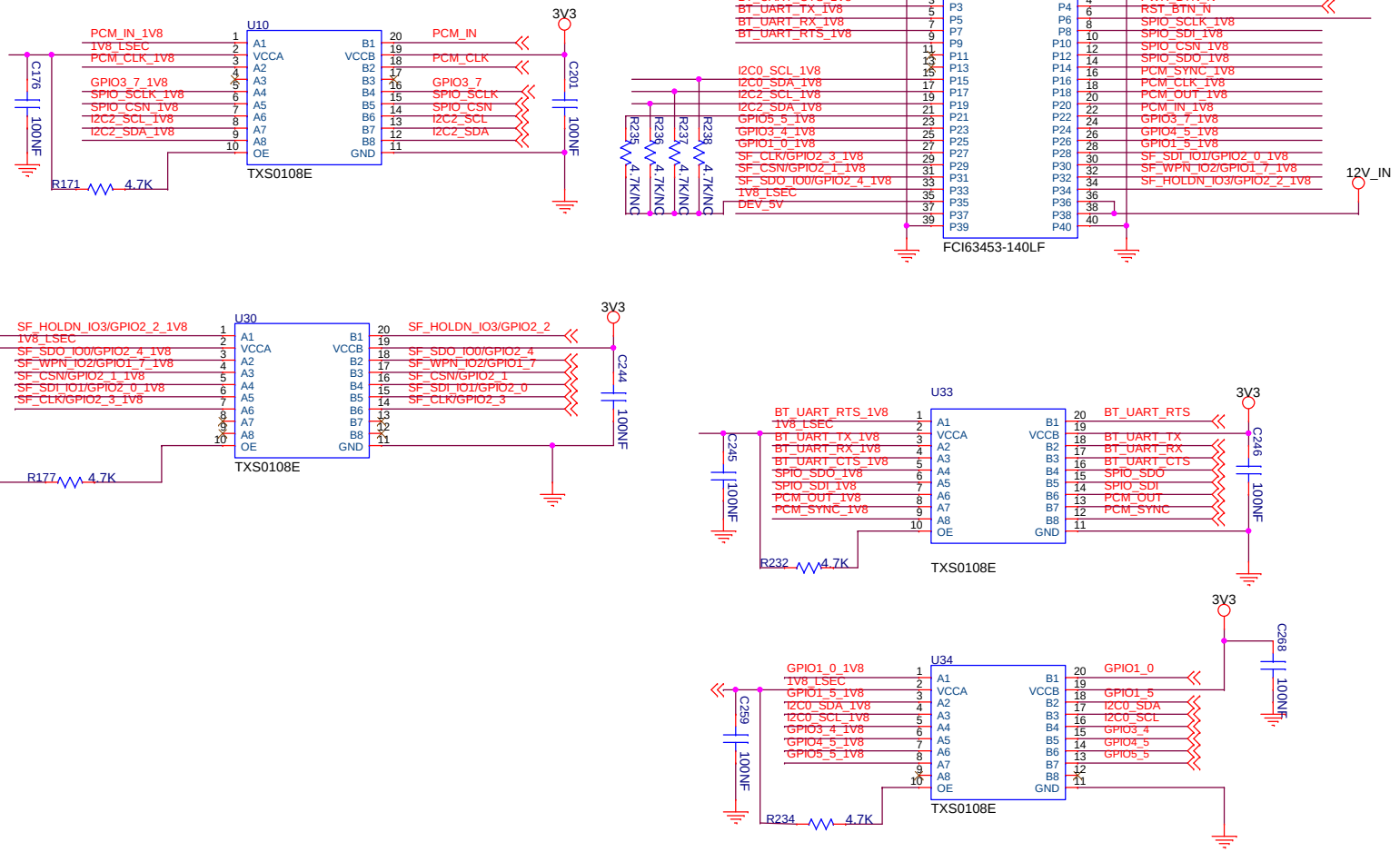
Low Speed Expansion Connector(LSEC)



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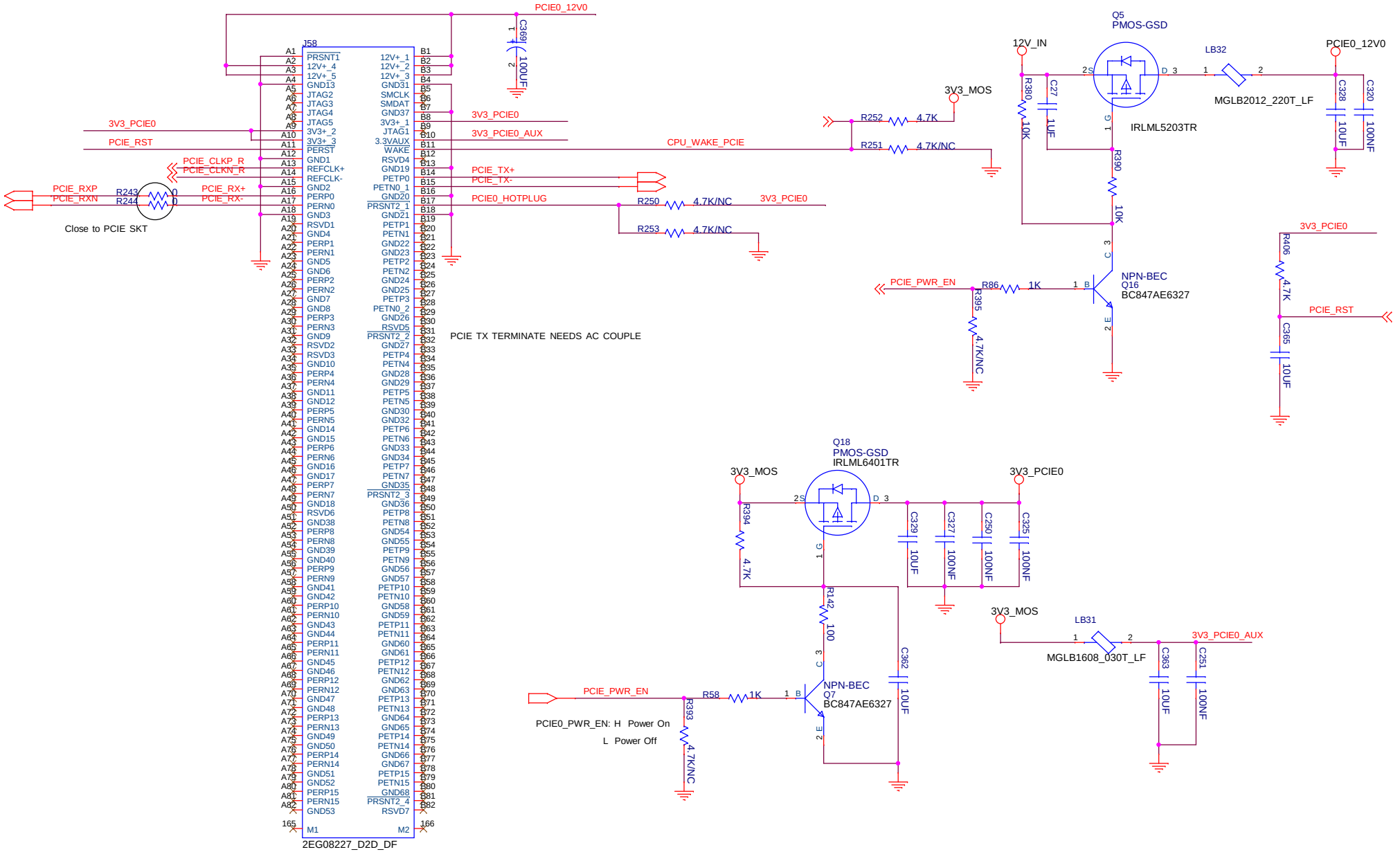
PCIe 1 lane



PCIe_Socket

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Schematic Update Record

Version	Date	Author	Change Note	Note
V0.1	20160308	HEMINGXIAO	The 1st Version	
V0.2	20170828	HEMINGXIAO ZhangBingFeng	1. Add R299=1K and D24 Red LED indicator. 2. Add R125=47K and R141= 47K pull up resister。 3. Change J14 from 8 Pin connector to 10 Pin connector 。 4. Change power supply of USB to UART circuits。	
V0.3	20180311	ZhangJiaYue	1.Update the version to VER.B。 2.Add R407=0ohm to connect GPIO3_5 for WIFI_RST. 3. Remove DTV turner board and smrart card ciruits.	

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