96Boards Compute SoM Edition

Hardware Platform Specification

Version 1.0, March 2019

IMPORTANT INFORMATION

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Background

The 96Boards Compute SoM Edition is intended to support:

1. Industrial application development and production deployment with system-on-module approach
2. Android Things
3. Open Source community software development
4. Maker community
5. System ODMs/OEMs requiring off-the-shelf production ready CPU modules with Upstream and/or Long Term Support
6. Community engineering activities, including
    - Upstream Development
    - Integration into an automated test farm
    - 96Boards Community program run by Linaro

In all cases key design and distribution goals are:

- Easy to purchase globally (for example, via Amazon, Alibaba, Farnell, Digikey, Mouser etc.)
- Enable a third party ecosystem to develop around base/expansion/mezzanine boards/peripherals/displays etc.

A key objective is to encourage multiple SoC vendors to build modules to this specification.

The 96Boards SoM specification is designed to enable an ecosystem to evolve that will support multiple SoCs over a period of years.

The specification is completely open - that is anyone may build a module to the specification without payment of any fees or any licensing requirements. Use of the 96Boards logo and compliance program requires a small per unit contribution.

96Boards Compute SoM Edition

Introduction

The 96Boards Compute SoM Edition (SoM-C) specifies a system-on-module with generic module-to-carrier board interface, independent of SoC choices on module. The Compute module is targeted to support SoCs with different capability whilst maintaining a unified interface through defined module to board connectors.

The 96Boards Compute module addresses the application domains such as industrial PCs, automation, smart devices, gateway systems, automotive, medical, Robotics and retail etc. It offers a reliable and cost-effective platform for building end-products.

Platforms built to 96Boards Compute SoM specifications are expected to be used in conjunction with carrier board. To increase the interoperability between SoMs built with different SoCs is the goal of this specification. It is expected that multiple such carrier board designs will be made available for prototype and production purposes. Carrier board design also are expected to vary to address different target markets.

1. Hardware

The 96Boards SoM specification defines the hardware requirements for the System-on-Module (SoM) as well as the interface between the SoM and a carrier board. The specification intends to offer flexibility for developers and product designers, to have good support for different carrier board options, whilst enabling easy to produce SoMs.

To provide the flexibility in module design, development and deployment, the 96Boards SoM specification defines two profiles. The module and carrier board design is SoC independent.

1.1 Compute Module Profiles

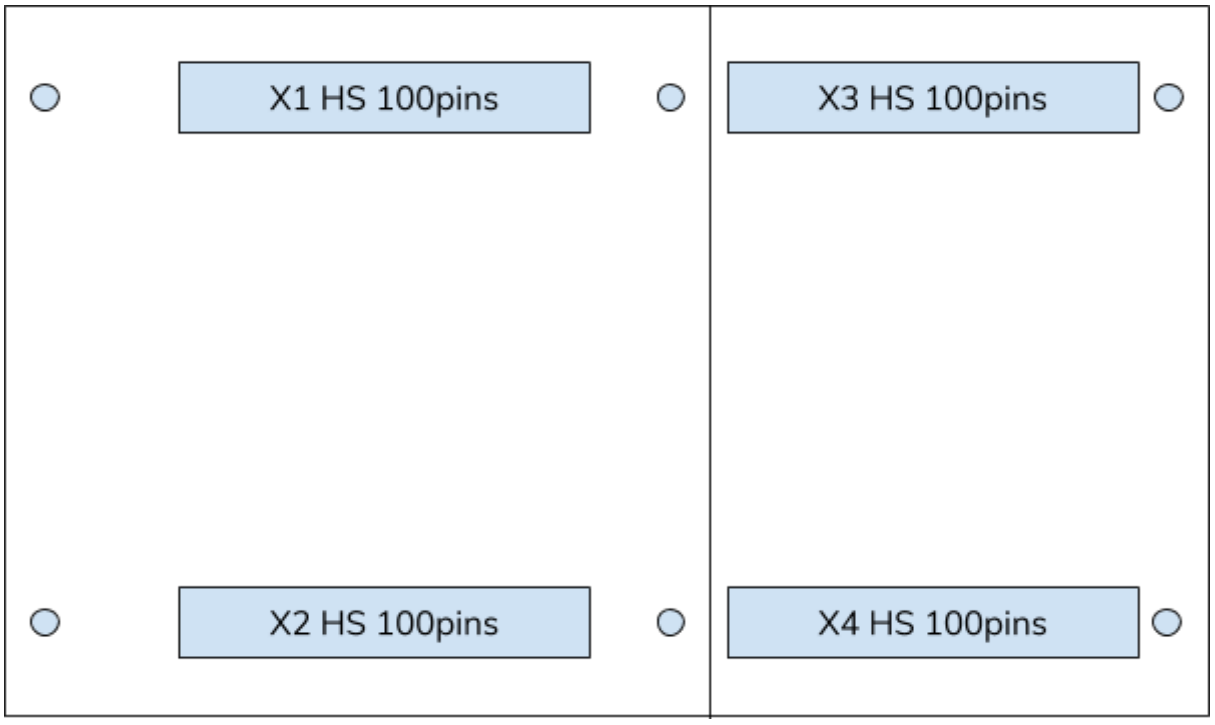
SoM-CA

50 x 50 x 6 mm with one or two 100 pin impedance controlled board to board connector(s) suitable for rugged applications. Type A modules shall implement the X1 100 pin Connector and may implement the X2 100 pin Connector.

Note that is is permitted to have extra functionality on any 96Boards product. For example, a vendor could choose to deliver a SoM-CA module for a display application with an on-board HDMI socket.

SoM-CB

85 x 50 x 6 mm with one, two or four 100 pin impedance controlled board to board connector(s) suitable for rugged applications. Type B modules will implement at least the X1 100 pin Connector. Below is viewed from carrier Boards top side.



Note: A general purpose development baseboard can support either Type A only SoMs, or any Type A or B module. Production baseboards will normally be configured for the end application to support applicable SoM-C configuration(s).

1.2 96Boards Compute Module Features

The following table provides a summary of the interfaces available on each of the four 100 pin Connectors. The X1 connector is mandatory on all SoMs. On each connector, interfaces if not implemented **shall** remain not connected. The supported multiplexing configurations **shall** be on designated pins.

Feature	X1	X2	X3	X4
SoM Management	1			
UART	1			2
I2C	2			2
I2S		1+1(mux with PCIe)		1(mux with SATA)
GPIO		6(mux with Analog Audio)	7	7(mux with ADC/SPI)
SD	1			1(mux with UHS-II)
SPI	2			2
CAN	1			2(1 mux)
MIPI CSI		1(mux with DSI)	4(1 mux with DSI)	
MIPI DSI	1(DSI/eDP/LVDS mux)	1(mux with CSI)	1(mux with CSI)	
MIPI Audio (SLIMbus, SoundWire)		1(mux with DSI/CSI)		
Ethernet		1	1	
PCIe		1 (x4)		1 (x4)
USB (2.0) OTG/HOST	2	1		1
USB (2.0/3.0) HOST	1	1（Device）		1
SmartCard		1(mux with PCIe)		
HDMI			1	
SATA		1		1(mux with I2S)
eDP	1(DSI/eDP/LVDS mux)			
LVDS	1(DSI/eDP/LVDS mux)			

X1 Connector Example Use Cases

- Simple embedded control system
- Sensory control system
- Robotics and automotive control subsystem

X2 Connector Example Use Cases

- Smart Audio
- Storage
- Embedded control system
- Edge computing
- Industrial gateway
- Computer Vision
- Mobile platform

X3 Connector Example Use Cases

- Security system
- Smart home and set top box
- Robotics
- Automotives
- AI applications

X4 Connector Example Use Cases

- Storage
- Industrial PC
- Automotive
- Sensory control system

Signal Voltage Levels

Unless otherwise specified all pins **shall** use 1.8V switching levels.

Power Supplies

The 96Boards Compute Module SoM specification allows flexibility in power supply configuration. A 5V nominal regulated power supply is provided for module power. Modules should specify their maximum power requirement.

- Input Voltage

  96Boards SoM-C Modules **shall** operate from a 5V regulated supply.

- Maximum Power

  The maximum power consumption of an SoM-C module **shall** be 50W from the 5V supply. There are 8 VDD1 pins on X1, 12 VDD2 pins on X4 with each supply up to 0.5A rated current.

All modules **shall** include suitable on-board regulators and/or PMIC devices.

Interface definition

X1

Pin	Description		Description	Pin
1	GND		GND	51
2	GND		VDD1(IN)	52
3	BOOT_CS1		VDD1(IN)	53
4	BOOT_CS2		VDD1(IN)	54
5	BOOT_CS0		VDD1(IN)	55
6	GND		VDD1(IN)	56
7	CAN0_TX/ TypeC_SBU1/GPIO		VDD1(IN)	57
8	CAN0_RX/ TypeC_SBU2/GPIO		VDD1(IN)	58
9	GND		VDD1(IN)	59
10	USB2_HOST0_D_P/TypeC_CC1		VDD1(3V3)(OUT)	60
11	USB2_HOST0_D_N/TypeC_CC2		VDD1(1V8)(OUT)	61
12	GND		GPIO	62
13	CAN0_L/GPIO		SD0_CMD	63
14	CAN0_H/GPIO		SD0_CLK	64
15	UART0_TX		SD0_D0	65
16	UART0_RX		SD0_D1	66
17	SOC_POR_RST		SD0_D2	67
18	UART0_RTS/GPIO		SD0_D3	68
19	UART0_CTS/GPIO		GND	69
20	SOM_ON_RST_REQ		LVDS_VDD_EN/ EDP_PWR_EN/DSI_PWR_EN	70
21	GPIO		EDP_HPD/DSI_RST	71
22	CB_PGOOD		LVDS_BKLT/EDP_BKLT/DSI_BLCTL	72
23	SOM_PGOOD		LVDS_BKLT_PWM/EDP_BKLT_PWM/DSI_VSYNC	73
24	SOM_PWR		GND	74

25	SOM_STBY_REQ		LVDS_D0_N/EDP_TX0_N/DSI0_TX0_N	75
26	GWDOG_RST		LVDS_D0_P/EDP_TX0_P/DSI0_TX0_P	76
27	SOC_PWR		GND	77
28	RTC_LICELL		LVDS_D1_N/EDP_TX1_N/DSI0_TX1_N	78
29	CB_PWR_EN		LVDS_D1_P/EDP_TX1_P/DSI0_TX1_P	79
30	SPI0_MISO		GND	80
31	SPI0_MOSI		LVDS_D2_N/EDP_TX2_N/DSI0_TX2_N	81
32	SPI0_CS0		LVDS_D2_P/EDP_TX2_P/DSI0_TX2_P	82
33	SPI0_CS1/GPIO		GND	83
34	SPI0_CLK		LVDS_CLK_N/EDP_AUX_N/DSI0_CLK_N	84
35	GND		LVDS_CLK_P/EDP_AUX_P/DSI0_CLK_P	85
36	SPI1_MISO		GND	86
37	SPI1_MOSI		LVDS_D3_N/EDP_TX3_N/DSI0_TX3_N	87
38	SPI1_CS0		LVDS_D3_P/EDP_TX3_P/DSI0_TX3_P	88
39	SPI1_CS1/GPIO		GND	89
40	SPI1_CLK		I2C0_DATA/DSI0_DATA	90
41	GND		I2C0_CLK/DSI0_SCL	91
42	USB3_HOST0_PWR		I2C1_DATA	92
43	USB3_HOST0_D_P		I2C1_CLK	93
44	USB3_HOST0_D_N		GPIO	94
45	USB3_SS0_TX_P		USB_OTG0_D_P/USB3_SS0_TX1_P	95
46	USB3_SS0_TX_N		USB_OTG0_D_N/USB3_SS0_TX1_N	96
47	GND		GND	97
48	USB3_SS0_RX_P		USB_OTG0_ID/USB3_SS0_RX1_P	98
49	USB3_SS0_RX_N		USB_OTG0_PWR/USB3_SS0_RX1_N	99
50	GND		GND	100

Notes :

- USB3 TypeC Pins are MUXed with CAN0/USB2/USB_OTG0
- LVDS/eDP/DSI0 ports are MUXed

X2

Pin	Description		Description	Pin
1	GND		GND	51
2	I2S1_BCLK		DSI1_CLK_P/CSI4_CLK_P	52
3	I2S1_DIN		DSI1_CLK_N/CSI4_CLK_N	53
4	I2S1_DOUT		GND	54
5	I2S1_LRCLK		DSI1_D0_P/CSI4_D0_P	55
6	I2S1_MCLK		DSI1_D0_N/CSI4_D0_N	56
7	GND		GND	57
8	I2S0_BCLK/PCIE0_TX3_P		DSI1_D1_P/CSI4_D1_P	58
9	I2S0_DIN/PCIE0_TX3_N		DSI1_D1_N/CSI4_D1_N	59
10	I2S0_DOUT /GND		GND	60
11	I2S0_LRCLK/PCIE0_RX3_P		DSI1_D2_P/CSI4_D2_P	61
12	I2S0_MCLK/PCIE0_RX3_N		DSI1_D2_N/CSI4_D2_N	62
13	GND		GND	63
14	SIM_PORT_CLK /PCIE0_TX2_P		DSI1_D3_P/CSI4_D3_P	64
15	SIM_PORT_CLK /PCIE0_TX2_N		DSI1_D3_N/CSI4_D3_N	65
16	SIM_PORT_CLK /GND		GND	66
17	SIM_PORT_SVEN/PCIE0_RX2_P		USB_OTG1_PWR	67
18	SIM_PORT_TRXD/PCIE0_RX2_N		USB_OTG1_ID	68
19	GND		USB_OTG1_D_P	69
20	PCIE0_TX0_P		USB_OTG1_D_N	70
21	PCIE0_TX0_N		GND	71
22	GND		SATA0_TX_P/PCIE0_TX1_P	72

23	PCIE0_RX0_P		SATA0_TX_N/PCIE0_TX1_N	73
24	PCIE0_RX0_N		GND	74
25	GND		SATA0_RX_P/PCIE0_RX1_P	75
26	PCIE0_CLK_P		SATA0_RX_N/PCIE0_RX1_N	76
`27	PCIE0_CLK_N		GND	77
28	PCIE0_PWR_EN		SATA0_PWR_EN/PCIE0_WAKE	78
29	PCIE0_RST		GPIO/TS_Y_P/GND	79
30	GND		GPIO/TS_X_N/SPKN	80
31	ETH0_MDI0_P		GPIO/TS_Y_N/SPKP	81
32	ETH0_MDI0_N		GPIO/TS_X_P/GND	82
33	GND		GPIO/MIC1_IN	83
34	ETH0_MDI1_P		GPIO/ADC/MIC2_IN	84
35	ETH0_MDI1_N		GPIO/GND	85
36	GND		GPIO/HPL	86
37	ETH0_MDI2_P		GPIO/HP_SENS	87
38	ETH0_MDI2_N		GPIO/HPR	88
39	GND		GND	89
40	ETH0_MDI3_P		I2C4_CLK	90
41	ETH0_MDI3_N		I2C4_DATA	91
42	GND		USB3_HOST1_D_P	92
43	ETH0_VREF		USB3_HOST1_D_N	93
44	ETH0_LINK_ACT/LED_GREEN		USB3_HOST1_PWR	94
45	ETH0_LINK100/LED_YELLOW		USB3_SS1_TX_P	95
46	ETH0_LINK1000/DSI1_BLCTL/CSI4_MCLK/ADC		USB3_SS1_TX_N	96
47	GND		GND	97
48	DSI1_RST/CSI4_RST/ADC/AUDIO_MIPI_CLK		USB3_SS1_RX_P	98
49	DSI1_VSYNC/CSI4_PWDN/ADC/AUDIO_MIIPI_DAT		USB3_SS1_RX_N	99

50	GND		GND	100

Notes:

- DSI1 and CSI4 are MUXed
- PCIE0 are MUXed with I2S0/SIM Card/SATA0
- GPIOs are MUXed with Analog Audio pins

X3

Pin	Description		Description	Pin
1	GND		GND	51
2	CSI0_D2_P		CSI0_C_P	52
3	CSI0_D2_N		CSI0_C_N	53
4	GND		GND	54
5	CSI0_D3_P		CSI0_D1_P	55
6	CSI0_D3_N		CSI0_D1_N	56
7	GND		GND	57
8	CSI1_D0_P/CSI3_D3_P		CSI0_D0_P	58
9	CSI1_D0_N/CSI3_D3_N		CSI0_D0_N	59
10	GND		GND	60
11	CSI1_D1_P/CSI3_D2_P		HDMI0_D2_P	61
12	CSI1_D1_N/CSI3_D2_N		HDMI0_D2_N	62
13	GND		GND	63
14	CSI3_C_P		HDMI0_D1_P	64
15	CSI3_C_N		HDMI0_D1_N	65
16	GND		GND	66
17	CSI3_D1_P		HDMI0_CLK_P	67
18	CSI3_D1_N		HDMI0_CLK_N	68
19	GND		GND	69
20	CSI3_D0_P		HDMI0_D0_P	70

21	CSI3_D0_N		HDMI0_D0_N	71
22	GND		GND	72
23	CSI2_D0_P /DSI2_D0_P		HDMI0_DDC_SCL	73
24	CSI2_D0_N /DSI2_D0_N		HDMI0_DDC_SDA	74
25	GND		HDMI0_CEC	75
26	CSI2_D1_P /DSI2_D1_P		HDMI0_HPD	76
27	CSI2_D1_N /DSI2_D1_N		ETH1_VREF	77
28	GND		ETH1_LINK_ACT/LED_GREEN	78
29	CSI2_C_P /DSI2_C_P		ETH1_LINK100/LED_YELLOW	79
30	CSI2_C_N /DSI2_C_N		ETH1_LINK1000/CSI2_PWDN/DSI2_BL CTL	80
31	GND		GND	81
32	CSI2_SDA /DSI2_D2_P		ETH1_MDI0_P	82
33	CSI2_SCL /DSI2_D2_N		ETH1_MDI0_N	83
34	GND		GND	84
35	CSI2_MCLK /DSI2_D3_P		ETH1_MDI1_P	85
36	CSI2__RST /DSI2_D3_N		ETH1_MDI1_N	86
37	GND		GND	87
38	CSI1_C_P		ETH1_MDI2_P	88
39	CSI1_C_N		ETH1_MDI2_N	89
40	GND		GND	90
41	CSI1_RST		ETH1_MDI3_P	91
42	CSI1_MCLK		ETH1_MDI3_N	92
43	CSI1_SCL		GND	93
44	CSI1_SDA		CSI3_SCL	94
45	CSI0_SDA		CSI3_SDA	95
46	CSI0_SCL		CSI3_MCLK	96

47	CSI0_MCLK		CSI3_RST/GPIO	97
48	CSI0_RST		CSI3_PWDN/GPIO	98
49	CSI0_PWDN/GPIO		CSI1_PWDN/GPIO	99
50	GND		GND	100

Notes：

- CSI and DSI can be MUXed

  Fun1: CSI0*4Lanes+CSI1*2Lanes+CSI2*2Lanes+CSI3*2Lanes

  Fun2:CSI0*4Lanes+CSI2*2Lanes+CSI3*4Lanes

  Fun3:CSI0*4Lanes+DSI2*2Lanes+CSI3*4Lanes

X4

Pin	Description		Description	Pin
1	GND		GND	51
2	USB3_HOST2_D_P		PCIE2_TX1_P	52
3	USB3_HOST2_D_N		PCIE2_TX1_N	53
4	USB3_HOST2_PWR		GND	54
5	USB3_SS2_TX_P		PCIE2_RX1_P	55
6	USB3_SS2_TX_N		PCIE2_RX1_N	56
7	GND		GND	57
8	USB3_SS2_RX_P		PCIE2_TX2_P	58
9	USB3_SS2_RX_N		PCIE2_TX2_N	59
10	USB3_SS2_CC1/GPIO		GND	60
11	USB3_SS2_CC2/GPIO		PCIE2_RX2_P	61
12	GND		PCIE2_RX2_N	62
13	SATA1_TX_P/I2S3_BCLK/GPIO		GND	63
14	SATA1_TX_N/I2S3_DIN/GPIO		PCIE2_TX3_P	64
15	GND/I2S3_DOUT/GPIO		PCIE2_TX3_N	65
16	SATA1_RX_P/I2S3_LRCLK/GPIO		GND	66

17	SATA1_RX_N/I2S3_MCLK/GPIO		PCIE2_RX3_P	67
18	GND		PCIE2_RX3_N	68
19	SATA1_PWR_EN/GPIO		GND	69
20	GPIO/ADC1		PCIE2_TX0_P	70
21	GPIO/ADC2		PCIE2_TX0_N	71
22	GPIO/ADC3		GND	72
23	GPIO/SPI3_MISOI		PCIE2_RX0_P	73
24	GPIO/SPI3_MOSI		PCIE2_RX0_N	74
25	GPIO/SPI3_CS		GND	75
26	GPIO/SPI3_SCLK		PCIE2_CLK_P	76
27	UART1_TX		PCIE2_CLK_N	77
28	UART1_RX		PCIE2_PWR_EN	78
29	GND		PCIE2_RST	79
30	GND		PCIE2_WAKE	80
31	GND		GND	81
32	GND		USB2_HOST2_D_P	82
33	GND		USB2_HOST2_D_N	83
34	VDD2(IN)		GND	84
35	VDD2(IN)		GPIO/UHSII_RCLK_P /SD1_CMD	85
36	VDD2(IN)		GPIO/UHSII_D0_N/SD1_D0	86
37	VDD2(IN)		GPIO/UHSII_D0_P/SD1_CLK	87
38	VDD2(IN)		GPIO/UHSII_D1_N/SD1_D1	88
39	VDD2(IN)		GPIO/UHSII_D1_PS/SD1_D2	89
40	VDD2(IN)		GPIO/UHSII_RCLK_N/SD1_D3	90
41	VDD2(IN)		GND/SD1_DET	91
42	VDD2(IN)		I2C4_DATA/SPI2_CS	92
43	VDD2(IN)		I2C4_CLK/SPI2_SCLK	93

44	VDD2(IN)		I2C3_DATA/SPI2_MISO/GPIO	94
45	VDD2(IN)		I2C3_CLK/SPI2_MOSI/GPIO	95
46	GND		CAN1_L	96
47	UART2_TX		CAN1_H	97
48	UART2_RX		CAN2_TX /GPIO/SD1_VDD	98
49	GPIO/UART2_CTS		CAN2_RX/UART2_RTS/GPIO	99
50	GND		GND	100

Notes:

- GPIO and SPI3 are MUXed
- GPIO/UHSI/SD Card are MUXed
- I2C4/I2C3 and SPI2 are MUXed
- UART2 and GPIO/CAN are MUXed
- SATA1 and I2S3 are MUXed

1.3 Pin MUX Description

X1

Pin	Description	Fun1 Typ）	Fun2	Fun3
1	GND	GND	GND	GND
2	GND	GND	GND	GND
3	BOOT_CS1	BOOT_CS1	BOOT_CS1	BOOT_CS1
4	BOOT_CS2	BOOT_CS2	BOOT_CS2	BOOT_CS2
5	BOOT_CS0	BOOT_CS0	BOOT_CS0	BOOT_CS0
6	GND	GND	GND	GND
7	CAN0_TX/ TypeC_SBU1/GPIO	CAN0_TX	TypeC_SBU1	GPIO
8	CAN0_RX/ TypeC_SBU2/GPIO	CAN0_RX	TypeC_SBU2	GPIO
9	GND	GND	GND	GND
10	USB2_HOST0_D_P/TypeC_CC1	USB2_HOST0_D_P	TypeC_CC1	
11	USB2_HOST0_D_N/TypeC_CC2	USB2_HOST0_D_N	TypeC_CC2	
12	GND	GND	GND	GND
13	CAN0_L/GPIO	CAN0_L	GPIO	
14	CAN0_H/GPIO	CAN0_H	GPIO	
15	UART0_TX	UART0_TX	UART0_TX	UART0_TX
16	UART0_RX	UART0_RX	UART0_RX	UART0_RX
17	SOC_POR_RST	SOC_POR_RST	SOC_POR_RST	SOC_POR_RST
18	UART0_RTS/GPIO	UART0_RTS	GPIO	
19	UART0_CTS/GPIO	UART0_CTS	GPIO	
20	SOM_ON_RST_REQ	SOM_ON_RST_REQ	SOM_ON_RST_REQ	SOM_ON_RST_REQ
21	GPIO	GPIO	GPIO	GPIO
22	CB_PGOOD	CB_PGOOD	CB_PGOOD	CB_PGOOD
23	SOM_PGOOD	SOM_PGOOD	SOM_PGOOD	SOM_PGOOD

24	SOM_PWR	SOM_PWR	SOM_PWR	SOM_PWR
25	SOM_STBY_REQ	SOM_STBY_REQ	SOM_STBY_REQ	SOM_STBY_REQ
26	GWDOG_RST	GWDOG_RST	GWDOG_RST	GWDOG_RST
27	SOC_PWR	SOC_PWR	SOC_PWR	SOC_PWR
28	RTC_LICELL	RTC_LICELL	RTC_LICELL	RTC_LICELL
29	CB_PWR_EN	CB_PWR_EN	CB_PWR_EN	CB_PWR_EN
30	SPI0_MISO	SPI0_MISO	SPI0_MISO	SPI0_MISO
31	SPI0_MOSI	SPI0_MOSI	SPI0_MOSI	SPI0_MOSI
32	SPI0_CS0	SPI0_CS0	SPI0_CS0	SPI0_CS0
33	SPI0_CS1/GPIO	SPI0_CS1/GPIO	SPI0_CS1/GPIO	SPI0_CS1/GPIO
34	SPI0_CLK	SPI0_CLK	SPI0_CLK	SPI0_CLK
35	GND	GND	GND	GND
36	SPI1_MISO	SPI1_MISO	SPI1_MISO	SPI1_MISO
37	SPI1_MOSI	SPI1_MOSI	SPI1_MOSI	SPI1_MOSI
38	SPI1_CS0	SPI1_CS0	SPI1_CS0	SPI1_CS0
39	SPI1_CS1/GPIO	SPI1_CS1/GPIO	SPI1_CS1/GPIO	SPI1_CS1/GPIO
40	SPI1_CLK	SPI1_CLK	SPI1_CLK	SPI1_CLK
41	GND	GND	GND	GND
42	USB3_HOST0_PWR	USB3_HOST0_PWR	USB3_HOST0_PWR	USB3_HOST0_PWR
43	USB3_HOST0_D_P	USB3_HOST0_D_P	USB3_HOST0_D_P	USB3_HOST0_D_P
44	USB3_HOST0_D_N	USB3_HOST0_D_N	USB3_HOST0_D_N	USB3_HOST0_D_N
45	USB3_SS0_TX_P	USB3_SS0_TX_P	USB3_SS0_TX_P	USB3_SS0_TX_P
46	USB3_SS0_TX_N	USB3_SS0_TX_N	USB3_SS0_TX_N	USB3_SS0_TX_N
47	GND	GND	GND	GND
48	USB3_SS0_RX_P	USB3_SS0_RX_P	USB3_SS0_RX_P	USB3_SS0_RX_P
49	USB3_SS0_RX_N	USB3_SS0_RX_N	USB3_SS0_RX_N	USB3_SS0_RX_N
50	GND	GND	GND	GND
51	GND	GND	GND	GND

52	VDD(IN)	VDD(IN)	VDD(IN)	VDD(IN)
53	VDD(IN)	VDD(IN)	VDD(IN)	VDD(IN)
54	VDD(IN)	VDD(IN)	VDD(IN)	VDD(IN)
55	VDD(IN)	VDD(IN)	VDD(IN)	VDD(IN)
56	VDD(IN)	VDD(IN)	VDD(IN)	VDD(IN)
57	VDD(IN)	VDD(IN)	VDD(IN)	VDD(IN)
58	VDD(IN)	VDD(IN)	VDD(IN)	VDD(IN)
59	VDD(IN)	VDD(IN)	VDD(IN)	VDD(IN)
60	VDD3V3)	VDD3V3)	VDD3V3)	VDD3V3)
61	VDD(1V8)	VDD(1V8)	VDD(1V8)	VDD(1V8)
62	GPIO	GPIO	GPIO	GPIO
63	SD0_CMD	SD0_CMD	SD0_CMD	SD0_CMD
64	SD0_CLK	SD0_CLK	SD0_CLK	SD0_CLK
65	SD0_D0	SD0_D0	SD0_D0	SD0_D0
66	SD0_D1	SD0_D1	SD0_D1	SD0_D1
67	SD0_D2	SD0_D2	SD0_D2	SD0_D2
68	SD0_D3	SD0_D3	SD0_D3	SD0_D3
69	GND	GND	GND	GND
70	LVDS_VDD_EN/ EDP_PWR_EN/DSI_PWR_EN	LVDS_VDD_EN	EDP_PWR_EN	DSI_PWR_EN
71	EDP_HPD/DSI_RST		EDP_HPD	DSI_RST
72	LVDS_BKLT/EDP_BKLT/DSI_BLCTL	LVDS_BKLT	EDP_BKLT	DSI_BLCTL
73	LVDS_BKLT_PWM/EDP_BKLT_PWM/ DSI_VSYNC	LVDS_BKLT_PWM	EDP_BKLT_PWM	DSI_VSYNC
74	GND			
75	LVDS_D0_N/EDP_TX0_N/DSI0_TX0_ N	LVDS_D0_N	EDP_TX0_N	DSI0_TX0_N
76	LVDS_D0_P/EDP_TX0_P/DSI0_TX0_P	LVDS_D0_P	EDP_TX0_P	DSI0_TX0_P
77	GND			
78	LVDS_D1_N/EDP_TX1_N/DSI0_TX1_ N	LVDS_D1_N	EDP_TX1_N	DSI0_TX1_N

79	LVDS_D1_P/EDP_TX1_P/DSI0_TX1_P	LVDS_D1_P	EDP_TX1_P	DSI0_TX1_P
80	GND			
81	LVDS_D2_N/EDP_TX2_N/DSI0_TX2_N	LVDS_D2_N	EDP_TX2_N	DSI0_TX2_N
82	LVDS_D2_P/EDP_TX2_P/DSI0_TX2_P	LVDS_D2_P	EDP_TX2_P	DSI0_TX2_P
83	GND			
84	LVDS_CLK_N/EDP_AUX_N/DSI0_CLK_N	LVDS_CLK_N	EDP_AUX_	DSI0_CLK_N
85	LVDS_CLK_P/EDP_AUX_P/DSI0_CLK_P	LVDS_CLK_P	EDP_AUX_P	DSI0_CLK_P
86	GND			
87	LVDS_D3_N/EDP_TX3_N/DSI0_TX3_N	LVDS_D3_N	EDP_TX3_N	DSI0_TX3_N
88	LVDS_D3_P/EDP_TX3_P/DSI0_TX3_P	LVDS_D3_P	EDP_TX3_P	DSI0_TX3_P
89	GND			
90	I2C0_DATA/DSI0_DATA	I2C0_DATA	I2C0_DATA	DSI0_DATA
91	I2C0_CLK/DSI0_SCL	I2C0_CLK	I2C0_CLK	DSI0_SCL
92	I2C1_DATA _	I2C1_DATA _	I2C1_DATA _	I2C1_DATA _
93	I2C1_CLK	I2C1_CLK	I2C1_CLK	I2C1_CLK
94	GPIO	GPIO	GPIO	GPIO
95	USB_OTG0_D_P/USB3_SS0_TX1_P	USB_OTG0_D_P	USB3_SS0_TX1_P	
96	USB_OTG0_D_N/USB3_SS0_TX1_N	USB_OTG0_D_N	USB3_SS0_TX1_N	
97	GND			
98	USB_OTG0_ID/USB3_SS0_RX1_P	USB_OTG0_ID	USB3_SS0_RX1_P	
99	USB_OTG0_PWR/USB3_SS0_RX1_N	USB_OTG0_PWR	USB3_SS0_RX1_N	
100	GND			

X2

Pin	Description	Fun1 Typ）	Fun2	Fun3	Fun4
1	GND	GND	GND	GND	
2	I2S1_BCLK	I2S1_BCLK	I2S1_BCLK	I2S1_BCLK	
3	I2S1_DIN	I2S1_DIN	I2S1_DIN	I2S1_DIN	
4	I2S1_DOUT	I2S1_DOUT	I2S1_DOUT	I2S1_DOUT	
5	I2S1_LRCLK	I2S1_LRCLK	I2S1_LRCLK	I2S1_LRCLK	
6	I2S1_MCLK	I2S1_MCLK	I2S1_MCLK	I2S1_MCLK	
7	GND	GND	GND	GND	
8	I2S0_BCLK/PCIE0_TX3_P	I2S0_BCLK	PCIE0_TX3_P		
9	I2S0_DIN/PCIE0_TX3_N	I2S0_DIN	PCIE0_TX3_N		
10	I2S0_DOUT /GND	I2S0_DOUT	GND		
11	I2S0_LRCLK/PCIE0_RX3_P	I2S0_LRCLK	PCIE0_RX3_P		
12	I2S0_MCLK/PCIE0_RX3_N	I2S0_MCLK	PCIE0_RX3_N		
13	GND	GND	GND		
14	SIM_PORT_CLK /PCIE0_TX2_P	SIM_PORT_CLK	PCIE0_TX2_P		
15	SIM_PORT_PD /PCIE0_TX2_N	SIM_PORT_PD	PCIE0_TX2_N		
16	SIM_PORT_RSTB /GND	SIM_PORT_RSTB	GND		
17	SIM_PORT_SVEN/PCIE0_RX2_P	SIM_PORT_SVEN	PCIE0_RX2_P		
18	SIM_PORT_TRXD/PCIE0_RX2_N	SIM_PORT_TRXD	PCIE0_RX2_N		
19	GND	GND	GND	GND	
20	PCIE0_TX0_P	PCIE0_TX0_P	PCIE0_TX0_P	PCIE0_TX0_P	
21	PCIE0_TX0_N	PCIE0_TX0_N	PCIE0_TX0_N	PCIE0_TX0_N	
22	GND	GND	GND	GND	
23	PCIE0_RX0_P	PCIE0_RX0_P	PCIE0_RX0_P	PCIE0_RX0_P	

24	PCIE0_RX0_N	PCIE0_RX0_N	PCIE0_RX0_N	PCIE0_RX0_N	
25	GND	GND	GND	GND	
26	PCIE0_CLK_P	PCIE0_CLK_P	PCIE0_CLK_P	PCIE0_CLK_P	
`27	PCIE0_CLK_N	PCIE0_CLK_N	PCIE0_CLK_N	PCIE0_CLK_N	
28	PCIE0_PWR_EN	PCIE0_PWR_EN	PCIE0_PWR_EN	PCIE0_PWR_EN	
29	PCIE0_RST	PCIE0_RST	PCIE0_RST	PCIE0_RST	
30	GND	GND	GND	GND	
31	ETH0_MDI0_P	ETH0_MDI0_P	ETH0_MDI0_P	ETH0_MDI0_P	
32	ETH0_MDI0_N	ETH0_MDI0_N	ETH0_MDI0_N	ETH0_MDI0_N	
33	GND	GND	GND	GND	
34	ETH0_MDI1_P	ETH0_MDI1_P	ETH0_MDI1_P	ETH0_MDI1_P	
35	ETH0_MDI1_N	ETH0_MDI1_N	ETH0_MDI1_N	ETH0_MDI1_N	
36	GND	GND	GND	GND	
37	ETH0_MDI2_P	ETH0_MDI2_P	ETH0_MDI2_P	ETH0_MDI2_P	
38	ETH0_MDI2_N	ETH0_MDI2_N	ETH0_MDI2_N	ETH0_MDI2_N	
39	GND	GND	GND	GND	
40	ETH0_MDI3_P	ETH0_MDI3_P	ETH0_MDI3_P	ETH0_MDI3_P	
41	ETH0_MDI3_N	ETH0_MDI3_N	ETH0_MDI3_N	ETH0_MDI3_N	
42	GND	GND	GND	GND	
43	ETH0_VREF	ETH0_VREF	ETH0_VREF		
44	ETH0_LINK_ACT/LED_GREEN	ETH0_LINK_ACT	LED_GREEN		
45	ETH0_LINK100/LED_YELLOW	ETH0_LINK100	LED_YELLOW		
46	ETH0_LINK1000/DSI1_BLCTL/CSI4_MCLK/ADC	DSI1_BLCTL	CSI4_MCLK	ADC	
47	GND	GND	GND	GND	
48	DSI1_RST/CSI4_RST/ADC/AUDIO_MIPI_CLK	DSI1_RST	CSI4_RST	ADC	AUDIO_MIPI_CLK
49	DSI1_VSYNC/CSI4_PWDN/ADC/AUDIO_MIIPI_DAT	DSI1_VSYNC	CSI4_PWDN	ADC	AUDIO_MIIPI_DAT

50	GND	GND	GND	GND	
51	GND	GND	GND	GND	
52	DSI1_CLK_P/CSI4_CLK_P	DSI1_CLK_P	CSI4_CLK_P		
53	DSI1_CLK_N/CSI4_CLK_N	DSI1_CLK_N	CSI4_CLK_N		
54	GND	GND	GND	GND	
55	DSI1_D0_P/CSI4_D0_P	DSI1_D0_P	CSI4_D0_P		
56	DSI1_D0_N/CSI4_D0_N	DSI1_D0_N	CSI4_D0_N		
57	GND	GND	GND	GND	
58	DSI1_D1_P/CSI4_D1_P	DSI1_D1_P	CSI4_D1_P		
59	DSI1_D1_N/CSI4_D1_N	DSI1_D1_N	CSI4_D1_N		
60	GND	GND	GND	GND	
61	DSI1_D2_P/CSI4_D2_P	DSI1_D2_P	CSI4_D2_P		
62	DSI1_D2_N/CSI4_D2_N	DSI1_D2_N	CSI4_D2_N		
63	GND	GND	GND	GND	
64	DSI1_D3_P/CSI4_D3_P	DSI1_D3_P	CSI4_D3_P		
65	DSI1_D3_N/CSI4_D3_N	DSI1_D3_N	CSI4_D3_N		
66	GND	GND	GND	GND	
67	USB_OTG1_PWR	USB_OTG1_PWR	USB_OTG1_PWR	USB_OTG1_PWR	
68	USB_OTG1_ID	USB_OTG1_ID	USB_OTG1_ID	USB_OTG1_ID	
69	USB_OTG1_D_P	USB_OTG1_D_P	USB_OTG1_D_P	USB_OTG1_D_P	
70	USB_OTG1_D_N	USB_OTG1_D_N	USB_OTG1_D_N	USB_OTG1_D_N	
71	GND	GND	GND	GND	
72	SATA0_TX_P/PCIE0_TX1_P	SATA0_TX_P	PCIE0_TX1_P		
73	SATA0_TX_N/PCIE0_TX1_N	SATA0_TX_N	PCIE0_TX1_N		
74	GND				
75	SATA0_RX_P/PCIE0_RX1_P	SATA0_RX_P	PCIE0_RX1_P		
76	SATA0_RX_N/PCIE0_RX1_N	SATA0_RX_N	PCIE0_RX1_N		

77	GND	GND	GND	GND	
78	SATA0_PWR_EN/PCIE0_WAKE	SATA0_PWR_EN	PCIE0_WAKE	SATA0_PWR_EN	
79	GPIO/TS_Y_P/GND	GPIO	TS_Y_P	GND	
80	GPIO/TS_X_N/SPKN	GPIO	TS_X_N	SPKN	
81	GPIO/TS_Y_N/SPKP	GPIO	TS_Y_N	SPKP	
82	GPIO/TS_X_P/GND	GPIO	TS_X_P	GND	
83	GPIO/MIC1_IN	GPIO	GPIO	MIC1_IN	
84	GPIO/ADC/MIC2_IN	GPIO	ADC	MIC2_IN	
85	GPIO/GND	GPIO	GPIO	GND	
86	GPIO/HPL	GPIO	GPIO	HPL	
87	GPIO/HP_SENS	GPIO	GPIO	HP_SENS	
88	GPIO/HPR	GPIO	GPIO	HPR	
89	GND				
90	I2C4_CLK	I2C4_CLK	I2C4_CLK	I2C4_CLK	
91	I2C4_DATA	I2C4_DATA	I2C4_DATA	I2C4_DATA	
92	USB3_HOST1_D_P	USB3_HOST1_D_P	USB3_HOST1_D_P	USB3_HOST1_D_P	USB3_HOST1_D_P
93	USB3_HOST1_D_N	USB3_HOST1_D_N	USB3_HOST1_D_N	USB3_HOST1_D_N	USB3_HOST1_D_N
94	USB3_HOST1_PWR	USB3_HOST1_PWR	USB3_HOST1_PWR	USB3_HOST1_PWR	USB3_HOST1_PWR
95	USB3_SS1_TX_P	USB3_SS1_TX_P	USB3_SS1_TX_P	USB3_SS1_TX_P	USB3_SS1_TX_P
96	USB3_SS1_TX_N	USB3_SS1_TX_N	USB3_SS1_TX_N	USB3_SS1_TX_N	USB3_SS1_TX_N
97	GND	GND	GND	GND	GND
98	USB3_SS1_RX_P	USB3_SS1_RX_P	USB3_SS1_RX_P	USB3_SS1_RX_P	USB3_SS1_RX_P
99	USB3_SS1_RX_N	USB3_SS1_RX_N	USB3_SS1_RX_N	USB3_SS1_RX_N	USB3_SS1_RX_N
100	GND	GND	GND	GND	GND

X3

Pin	Description	Fun1 Typ）	Fun2	Fun3
1	GND	GND	GND	GND
2	CSI0_D2_P	CSI0_D2_P	CSI0_D2_P	CSI0_D2_P
3	CSI0_D2_N	CSI0_D2_N	CSI0_D2_N	CSI0_D2_N
4	GND	GND	GND	GND
5	CSI0_D3_P	CSI0_D3_P	CSI0_D3_P	CSI0_D3_P
6	CSI0_D3_N	CSI0_D3_N	CSI0_D3_N	CSI0_D3_N
7	GND	GND	GND	GND
8	CSI1_D0_P/CSI3_D3_P	CSI1_D0_P	CSI3_D3_P	
9	CSI1_D0_N/CSI3_D3_N	CSI1_D0_N	CSI3_D3_N	
10	GND	GND	GND	GND
11	CSI1_D1_P/CSI3_D2_P	CSI1_D1_P	CSI3_D2_P	
12	CSI1_D1_N/CSI3_D2_N	CSI1_D1_N	CSI3_D2_N	
13	GND	GND	GND	GND
14	CSI3_C_P	CSI3_C_P	CSI3_C_P	CSI3_C_P
15	CSI3_C_N	CSI3_C_N	CSI3_C_N	CSI3_C_N
16	GND	GND	GND	GND
17	CSI3_D1_P	CSI3_D1_P	CSI3_D1_P	CSI3_D1_P
18	CSI3_D1_N	CSI3_D1_N	CSI3_D1_N	CSI3_D1_N
19	GND	GND	GND	GND
20	CSI3_D0_P	CSI3_D0_P	CSI3_D0_P	CSI3_D0_P
21	CSI3_D0_N	CSI3_D0_N	CSI3_D0_N	CSI3_D0_N
22	GND	GND	GND	GND
23	CSI2_D0_P	CSI2_D0_P		DSI2_D0_P

	/DSI2_D0_P			
24	CSI2_D0_N /DSI2_D0_N	CSI2_D0_N		DSI2_D0_N
25	GND	GND	GND	GND
26	CSI2_D1_P /DSI2_D1_P	CSI2_D1_P		DSI2_D1_P
27	CSI2_D1_N /DSI2_D1_N	CSI2_D1_N		DSI2_D1_N
28	GND	GND	GND	GND
29	CSI2_C_P /DSI2_C_P	CSI2_C_P		DSI2_C_P
30	CSI2_C_N /DSI2_C_N	CSI2_C_N		DSI2_C_N
31	GND	GND	GND	GND
32	CSI2_SDA /DSI2_D2_P	CSI2_SDA		DSI2_SDA
33	CSI2_SCL /DSI2_D2_N	CSI2_SCL		DSI2_SCL
34	GND	GND	GND	GND
35	CSI2_MCLK /DSI2_D3_P	CSI2_MCLK		DSI2_VSYNC
36	CSI2__RST /DSI2_D3_N	CSI2__RST		DSI2_RST
37	GND	GND	GND	GND
38	CSI1_C_P	CSI1_C_P	CSI1_C_P	CSI1_C_P
39	CSI1_C_N	CSI1_C_N	CSI1_C_N	CSI1_C_N
40	GND	GND	GND	GND
41	CSI1_RST	CSI1_RST	CSI1_RST	CSI1_RST
42	CSI1_MCLK	CSI1_MCLK	CSI1_MCLK	CSI1_MCLK
43	CSI1_SCL	CSI1_SCL	CSI1_SCL	CSI1_SCL
44	CSI1_SDA	CSI1_SDA	CSI1_SDA	CSI1_SDA
45	CSI0_SDA	CSI0_SDA	CSI0_SDA	CSI0_SDA
46	CSI0_SCL	CSI0_SCL	CSI0_SCL	CSI0_SCL
47	CSI0_MCLK	CSI0_MCLK	CSI0_MCLK	CSI0_MCLK
48	CSI0_RST	CSI0_RST	CSI0_RST	CSI0_RST

49	CSI0_PWDN/GPIO	CSI0_PWDN	GPIO	
50	GND	GND	GND	GND
51	GND	GND	GND	GND
52	CSI0_C_P	CSI0_C_P	CSI0_C_P	CSI0_C_P
53	CSI0_C_N	CSI0_C_N	CSI0_C_N	CSI0_C_N
54	GND	GND	GND	GND
55	CSI0_D1_P	CSI0_D1_P	CSI0_D1_P	CSI0_D1_P
56	CSI0_D1_N	CSI0_D1_N	CSI0_D1_N	CSI0_D1_N
57	GND	GND	GND	GND
58	CSI0_D0_P	CSI0_D0_P	CSI0_D0_P	CSI0_D0_P
59	CSI0_D0_N	CSI0_D0_N	CSI0_D0_N	CSI0_D0_N
60	GND	GND	GND	GND
61	HDMI0_D2_P	HDMI0_D2_P	HDMI0_D2_P	HDMI0_D2_P
62	HDMI0_D2_N	HDMI0_D2_N	HDMI0_D2_N	HDMI0_D2_N
63	GND	GND	GND	GND
64	HDMI0_D1_P	HDMI0_D1_P	HDMI0_D1_P	HDMI0_D1_P
65	HDMI0_D1_N	HDMI0_D1_N	HDMI0_D1_N	HDMI0_D1_N
66	GND	GND	GND	GND
67	HDMI0_CLK_P	HDMI0_CLK_P	HDMI0_CLK_P	HDMI0_CLK_P
68	HDMI0_CLK_N	HDMI0_CLK_N	HDMI0_CLK_N	HDMI0_CLK_N
69	GND	GND	GND	GND
70	HDMI0_D0_P	HDMI0_D0_P	HDMI0_D0_P	HDMI0_D0_P
71	HDMI0_D0_N	HDMI0_D0_N	HDMI0_D0_N	HDMI0_D0_N
72	GND	GND	GND	GND
73	HDMI0_DDC_SCL	HDMI0_DDC_SCL	HDMI0_DDC_SCL	HDMI0_DDC_SCL
74	HDMI0_DDC_SDA	HDMI0_DDC_SDA	HDMI0_DDC_SDA	HDMI0_DDC_SDA
75	HDMI0_CEC	HDMI0_CEC	HDMI0_CEC	HDMI0_CEC
76	HDMI0_HPD	HDMI0_HPD	HDMI0_HPD	HDMI0_HPD

77	ETH1_VREF	ETH1_VREF	ETH1_VREF	ETH1_VREF
78	ETH1_LINK_ACT/LED_GREEN	ETH1_LINK_ACT	LED_GREEN	
79	ETH1_LINK100/LED_YELLOW	ETH1_LINK100/	LED_YELLOW	
80	ETH1_LINK1000/CSI2_PWDN/DSI2_BLCTL	CSI2_PWDN		DSI2_BLCTL
81	GND	GND	GND	GND
82	ETH1_MDI0_P	ETH1_MDI0_P	ETH1_MDI0_P	ETH1_MDI0_P
83	ETH1_MDI0_N	ETH1_MDI0_N	ETH1_MDI0_N	ETH1_MDI0_N
84	GND	GND	GND	GND
85	ETH1_MDI1_P	ETH1_MDI1_P	ETH1_MDI1_P	ETH1_MDI1_P
86	ETH1_MDI1_N	ETH1_MDI1_N	ETH1_MDI1_N	ETH1_MDI1_N
87	GND	GND	GND	GND
88	ETH1_MDI2_P	ETH1_MDI2_P	ETH1_MDI2_P	ETH1_MDI2_P
89	ETH1_MDI2_N	ETH1_MDI2_N	ETH1_MDI2_N	ETH1_MDI2_N
90	GND	GND	GND	GND
91	ETH1_MDI3_P	ETH1_MDI3_P	ETH1_MDI3_P	ETH1_MDI3_P
92	ETH1_MDI3_N	ETH1_MDI3_N	ETH1_MDI3_N	ETH1_MDI3_N
93	GND	GND	GND	GND
94	CSI3_SCL	CSI3_SCL	CSI3_SCL	CSI3_SCL
95	CSI3_SDA	CSI3_SDA	CSI3_SDA	CSI3_SDA
96	CSI3_MCLK	CSI3_MCLK	CSI3_MCLK	CSI3_MCLK
97	CSI3_RST/GPIO	CSI3_RST	GPIO	
98	CSI3_PWDN/GPIO	CSI3_PWDN	GPIO	
99	CSI1_PWDN/GPIO	CSI1_PWDN	GPIO	
100	GND			

X4

Pin	Description	Fun1 Typ）	Fun2	Fun3
1	GND	GND	GND	GND
2	USB3_HOST2_D_P	USB3_HOST2_D_P	USB3_HOST2_D_P	USB3_HOST2_D_P
3	USB3_HOST2_D_N	USB3_HOST2_D_N	USB3_HOST2_D_N	USB3_HOST2_D_N
4	USB3_HOST2_PWR	USB3_HOST2_PWR	USB3_HOST2_PWR	USB3_HOST2_PWR
5	USB3_SS2_TX_P	USB3_SS2_TX_P	USB3_SS2_TX_P	USB3_SS2_TX_P
6	USB3_SS2_TX_N	USB3_SS2_TX_N	USB3_SS2_TX_N	USB3_SS2_TX_N
7	GND	GND	GND	GND
8	USB3_SS2_RX_P	USB3_SS2_RX_P	USB3_SS2_RX_P	USB3_SS2_RX_P
9	USB3_SS2_RX_N	USB3_SS2_RX_N	USB3_SS2_RX_N	USB3_SS2_RX_N
10	USB3_SS2_CC1(O)/GPIO	USB3_SS2_CC1(O)	GPIO	
11	USB3_SS2_CC2(O)/GPIO	USB3_SS2_CC2(O)	GPIO	
12	GND			
13	SATA1_TX_P/I2S3_BCLK/GPIO	SATA1_TX_P	I2S3_BCLK	GPIO
14	SATA1_TX_N/I2S3_DIN/GPIO	SATA1_TX_N	I2S3_DIN	GPIO
15	GND/I2S3_DOUT/GPIO	GND	I2S3_DOUT	GPIO
16	SATA1_RX_P/I2S3_LRCLK/GPIO	SATA1_RX_P	I2S3_LRCLK	GPIO
17	SATA1_RX_N/I2S3_MCLK/GPIO	SATA1_RX_N	I2S3_MCLK	GPIO
18	GND			
19	SATA1_PWR_EN/GPIO	SATA1_PWR_EN		GPIO
20	GPIO/ADC1	GPIO	ADC1	
21	GPIO/ADC2	GPIO	ADC2	
22	GPIO/ADC3	GPIO	ADC3	

23	GPIO/SPI3_MISOI	GPIO	SPI3_MISOI	
24	GPIO/SPI3_MOSI	GPIO	SPI3_MOSI	
25	GPIO/SPI3_CS	GPIO	SPI3_CS	
26	GPIO/SPI3_SCLK	GPIO	SPI3_SCLK	
27	UART1_TX	UART1_TX	UART1_TX	UART1_TX
28	UART1_RX	UART1_RX	UART1_RX	UART1_RX
29	GND	GND	GND	GND
30	GND	GND	GND	GND
31	GND	GND	GND	GND
32	GND	GND	GND	GND
33	GND	GND	GND	GND
34	VDD(IN)	VDD(IN)	VDD(IN)	VDD(IN)
35	VDD(IN)	VDD(IN)	VDD(IN)	VDD(IN)
36	VDD(IN)	VDD(IN)	VDD(IN)	VDD(IN)
37	VDD(IN)	VDD(IN)	VDD(IN)	VDD(IN)
38	VDD(IN)	VDD(IN)	VDD(IN)	VDD(IN)
39	VDD(IN)	VDD(IN)	VDD(IN)	VDD(IN)
40	VDD(IN)	VDD(IN)	VDD(IN)	VDD(IN)
41	VDD(IN)	VDD(IN)	VDD(IN)	VDD(IN)
42	VDD(IN)	VDD(IN)	VDD(IN)	VDD(IN)
43	VDD(IN)	VDD(IN)	VDD(IN)	VDD(IN)
44	VDD(IN)	VDD(IN)	VDD(IN)	VDD(IN)
45	VDD(IN)	VDD(IN)	VDD(IN)	VDD(IN)
46	GND	GND	GND	GND
47	UART2_TX	UART2_TX	UART2_TX	UART2_TX
48	UART2_RX	UART2_RX	UART2_RX	UART2_RX
49	UART2_CTS/GPIO		UART2_CTS	GPIO
50	GND	GND	GND	GND

51	GND	GND	GND	GND
52	PCIE2_TX1_P	PCIE2_TX1_P	PCIE2_TX1_P	PCIE2_TX1_P
53	PCIE2_TX1_N	PCIE2_TX1_N	PCIE2_TX1_N	PCIE2_TX1_N
54	GND	GND	GND	GND
55	PCIE2_RX1_P	PCIE2_RX1_P	PCIE2_RX1_P	PCIE2_RX1_P
56	PCIE2_RX1_N	PCIE2_RX1_N	PCIE2_RX1_N	PCIE2_RX1_N
57	GND	GND	GND	GND
58	PCIE2_TX2_P	PCIE2_TX2_P	PCIE2_TX2_P	PCIE2_TX2_P
59	PCIE2_TX2_N	PCIE2_TX2_N	PCIE2_TX2_N	PCIE2_TX2_N
60	GND	GND	GND	GND
61	PCIE2_RX2_P	PCIE2_RX2_P	PCIE2_RX2_P	PCIE2_RX2_P
62	PCIE2_RX2_N	PCIE2_RX2_N	PCIE2_RX2_N	PCIE2_RX2_N
63	GND	GND	GND	GND
64	PCIE2_TX3_P	PCIE2_TX3_P	PCIE2_TX3_P	PCIE2_TX3_P
65	PCIE2_TX3_N	PCIE2_TX3_N	PCIE2_TX3_N	PCIE2_TX3_N
66	GND	GND	GND	GND
67	PCIE2_RX3_P	PCIE2_RX3_P	PCIE2_RX3_P	PCIE2_RX3_P
68	PCIE2_RX3_N	PCIE2_RX3_N	PCIE2_RX3_N	PCIE2_RX3_N
69	GND	GND	GND	GND
70	PCIE2_TX0_P	PCIE2_TX0_P	PCIE2_TX0_P	PCIE2_TX0_P
71	PCIE2_TX0_N	PCIE2_TX0_N	PCIE2_TX0_N	PCIE2_TX0_N
72	GND	GND	GND	GND
73	PCIE2_RX0_P	PCIE2_RX0_P	PCIE2_RX0_P	PCIE2_RX0_P
74	PCIE2_RX0_N	PCIE2_RX0_N	PCIE2_RX0_N	PCIE2_RX0_N
75	GND	GND	GND	GND
76	PCIE2_CLK_P	PCIE2_CLK_P	PCIE2_CLK_P	PCIE2_CLK_P
77	PCIE2_CLK_N	PCIE2_CLK_N	PCIE2_CLK_N	PCIE2_CLK_N
78	PCIE2_PWR_EN	PCIE2_PWR_EN	PCIE2_PWR_EN	PCIE2_PWR_EN

79	PCIE2_RST	PCIE2_RST	PCIE2_RST	PCIE2_RST
80	PCIE2_WAKE	PCIE2_WAKE	PCIE2_WAKE	PCIE2_WAKE
81	GND	GND	GND	GND
82	USB2_HOST2_D_P	USB2_HOST2_D_P	USB2_HOST2_D_P	USB2_HOST2_D_P
83	USB2_HOST2_D_N	USB2_HOST2_D_N	USB2_HOST2_D_N	USB2_HOST2_D_N
84	GND	GND	GND	GND
85	GPIO/UHSII_RCLK_P /SD1_CMD	GPIO	UHSII_RCLK_P	SD1_CMD
86	GPIO/UHSII_D0_N/SD1_D0	GPIO	UHSII_D0_N	SD1_D0
87	GPIO/UHSII_D0_P/SD1_CLK	GPIO	UHSII_D0_P	SD1_CLK
88	GPIO/UHSII_D1_N/SD1_D1	GPIO	UHSII_D1_N	SD1_D1
89	GPIO/UHSII_D1_P/SD1_D2	GPIO	UHSII_D1_P	SD1_D2
90	GPIO/UHSII_RCLK_N/SD1_D3	GPIO	UHSII_RCLK_N	SD1_D3
91	GND/SD1_DET	GND	GND	SD1_DET
92	I2C4_DATA/SPI2_CS	I2C4_DATA	SPI2_CS	
93	I2C4_CLK/SPI2_SCLK	I2C4_CLK	SPI2_SCLK	
94	I2C3_DATA/SPI2_MISO/GPIO	I2C3_DATA	SPI2_MISO	GPIO
95	I2C3_CLK/SPI2_MOSI/GPIO	I2C3_CLK	SPI2_MOSI	GPIO
96	CAN1_L	CAN1_L	CAN1_L	CAN1_L
97	CAN1_H	CAN1_H	CAN1_H	CAN1_H
98	CAN2_TX /GPIO/SD1_VDD	CAN2_TX	GPIO	SD1_VDD
99	CAN2_RX/UART2_RTS/GPIO	CAN2_RX	UART2_RTS	GPIO
100	GND			

1.4 Interface Definition

1. Boot select

Signal	V	Type
BOOT_CS0	1.8V	I
BOOT_CS1	1.8V	I
BOOT_CS2	1.8V	I

BOOT_CS0	BOOT_CS1	BOOT_CS2	Boot Source
GND	GND	GND	Carrier SATA and/or NVME(O)
GND	GND	Float	Carrier SD Card
GND	Float	GND	Carrier eMMC
GND	Float	Float	Carrier SPI (O)
Float	GND	GND	Module device (NAND, NOR) (O)
Float	GND	Float	Remote boot (ETH) (O)
Float	Float	GND	Module eMMC/UFS
Float	Float	Float	Module SPI (O)

2. UART

Signal	Description	V	Type
UART_CTS	Clear to Send control	1.8V	I
UART_TxD	Transmit serial data	1.8V	O
UART_RxD	Receive serial data	1.8V	I
UART_RTS	Request to Send control	1.8V	O

3. I2C

Signal	Description	V	Type
I2C_SCL	Serial Clock	1.8V	OD/PU

I2C_SDA	Serial Data	1.8V	OD/PU

4. I2S/PCM

Signal	Description	V	Type
AUDIO_I2S_SCK	I2S Clock	1.8V	O
AUDIO_I2S_MCLK/PCM_CLK	PCM/I2S Bit clock	1.8V	O
AUDIO_I2S_WS/PCM_FS	PCM/I2S Word Clock	1.8V	O
AUDIO_I2S_D0/PCM_DO	PCM/I2S Serial data out	1.8V	O
AUDIO_I2S_D1 /PCM_DI	PCM/I2S Serial data in	1.8V	I

5. SPI

Signal	Description	V	Type
SPI_SCLK	Clock	1.8V	O
SPI_MISO	Master In Slave Out	1.8V	I
SPI_MOSI	Master Out Slave In	1.8V	O
SPI_CS	Chip select	1.8V	O

6. SD/SDIO/MMC

Signal	Description	V	Type
SD_DAT[0-3]	Serial Data	1.8V	I/O
SD_SCLK	Serial Clock	1.8V	O
SD_CMD	Command	1.8V	I/O

7. UHS-II

Signal	Description	V	Type
UHSII_D0_P	Lane 0 differential Data Positive	1.8V	I/O
UHSII_D0_N	Lane 0 differential Data Negative	1.8V	I/O
UHSII_D1_P	Lane 1 differential Data Positive	1.8V	I/O

UHSII_D1_N	Lane 1 differential Data Negative	1.8V	I/O
UHSII_RCLK_P	Reference Clock Positive	1.8V	O
UHSII_RCLK_N	Reference Clock Negative	1.8V	O

8. CAN

Signal	Description	V	
CAN_TX	Data Transmit	1.8V	O
CAN_RX	Data Receive	1.8V	I
CAN_L	Transceiver Dominant Low	1.8V	IO
CAN_H	Transceiver Dominant High	1.8V	IO

9. USB 2.x Host

Signal	Description	V	Spec
USB_HOST_D_P	Differential USB data	USB	I/O
USB_HOST_D_N	Differential USB data	USB	I/O

10. USB 3.x Host

Signal	Description	V	Spec
USB_HOST_D_P	Differential USB data	USB	O
USB_HOST_D_N	Differential USB data	USB	O
USB_SS_RX_D_P	Superspeed receiver differential USB data	USB	I
USB_SS_RX_D_N	Superspeed receiver differential USB data	USB	I
USB_SS_TX_D_P	Superspeed transmitter differential USB data	USB	O
USB_SS_TX_D_N	Superspeed transmitter differential USB data	USB	O
USB_HOST_PWR	USB Power		I

11. USB 2.x OTG

Signal	Description	Voltage	Spec

USB_OTG_D_P	differential USB data	USB	O
USB_OTG_D_N	differential USB data	USB	O
USB_OTG_ID	ID for identifying lines	1.8V	I
USB_OTG_PWR	USB Power	5V	O

12. PCIe

96Boards Compute SoM Module **may** implement PCIe links as PCIe Gen 1, 2 or 3 depending on SoC capability. 96Boards Compute Module PCIe links are primarily PCIe Root Complexes. They **may** be configured as a PCIe target(s) at designer's choice.

Signal	Description	Voltage	Spec
PCIE_TX_P	Differential PCIe transmit positive data	1.8V	O
PCIE_TX_N	Differential PCIe transmit negative data	1.8V	O
PCIE_RX_P	Differential PCIe receive positive data	1.8V	I
PCIE_RX_N	Differential PCIe receive negative data	1.8V	I
PCIE_PWR_EN	PCIe power enable	1.8V	I
PCIE_RST	PCIe reset output	1.8V	O
PCIE_WAKE	PCIe wake up interrupt output	1.8V	O
PCIE_CLK_N	Differential PCIe reference negative clock output	1.8V	O
PCIE_CLK_P	Differential PCIe reference positive clock output	1.8V	O

13. Timers (Optional)
    - General Purpose Timer

    General purpose timer is capable of generating an event on SoM carrier board interface and/or a system interrupt when the timer reaches a programmed value. Additional GPT functionality includes capturing the counter value in a register. These depend on the availability from the SoC and can be made available via the SoM interface by re-purposing GPIOs.

    - Watchdog Timer

    Watchdog timers can be used to protect system from failures by providing a method of escaping from unexpected events or programming errors. Once the WDOG is activated, it must be serviced by the software on a periodic basis. If servicing does not take place, the timer times out. Upon a time out, the WDOG will assert the internal

system reset signal. An optional, programmable interrupt can be generated prior to watchdog timer timeout. These depend on the availability from the SoC and can be made available via the SoM interface by re-purposing GPIOs.

14. Ethernet

Signal	Description	Voltage	Spec
ETH_VREF	Reference voltage for Carrier Board Ethernet Controller	1.8V	REF
ETH_LINK_ACT	Gigabit Ethernet Activity LED	1.8V	O
ETH_LINK_1000	Gigabit Ethernet Link 1000 LED	1.8V	O
ETH_LINK_100	Gigabit Ethernet Link 10/100 LED	1.8V	O
ETH_MDI0_P	Ethernet Media Dependent Interface Differential Pairs 0 positive data	1.8V	I/O
ETH_MDI0_N	Ethernet Media Dependent Interface Differential Pairs 0 negative data	1.8V	I/O
ETH_MDI1_P	Ethernet Media Dependent Interface Differential Pairs 1 positive data	1.8V	I/O
ETH_MDI1_N	Ethernet Media Dependent Interface Differential Pairs 1 negative data	1.8V	I/O
ETH_MDI2_P	Ethernet Media Dependent Interface Differential Pairs 2 positive data	1.8V	I/O
ETH_MDI2_N	Ethernet Media Dependent Interface Differential Pairs 2 negative data	1.8V	I/O
ETH_MDI3_P	Ethernet Media Dependent Interface Differential Pairs 3 positive data	1.8V	I/O
ETH_MDI3_N	Ethernet Media Dependent Interface Differential Pairs 3 negative data	1.8V	I/O

15. DSI Display

Signal	Description	Voltage	Spec
DSI_CLK_N	Negative DSI clock differential	1.8V	O
DSI_CLK_P	Positive DSI clock differential	1.8V	O

DSI_D0_N	Negative DSI data 0 differential	1.8V	I/O
DSI_D0_P	Positive DSI data 0 differential	1.8V	I/O
DSI_D1_N	Negative DSI data 1 differential	1.8V	I/O
DSI_D1_P	Positive DSI data 1 differential	1.8V	I/O
DSI_D2_N	Negative DSI data 0 differential	1.8V	I/O
DSI_D2_P	Positive DSI data 0 differential	1.8V	I/O
DSI_D3_N	Negative DSI data 1 differential	1.8V	I/O
DSI_D3_P	Positive DSI data 1 differential	1.8V	I/O

16. HDMI

Signal	Description	Voltage	Spec
HDMI_D2_P	HDMI differential positive data 2	1.8V	O
HDMI_D2_N	HDMI differential negative data 2	1.8V	O
HDMI_D1_P	HDMI differential positive data 1	1.8V	O
HDMI_D1_N	HDMI differential negative data 1	1.8V	O
HDMI_D0_P	HDMI differential positive data 0	1.8V	O
HDMI_D0_N	HDMI differential negative data 0	1.8V	O
HDMI_CLK_P	HDMI differential positive clock	1.8V	O
HDMI_HPD	Hot Plug Detect	1.8V	I
HDMI_CLK_N	HDMI differential negative clock	1.8V	O
HDMI_DDC_SDA	I2C data for HDMI use	1.8V	I/O
HDMI_DDC_SCL	I2C clock for HDMI use	1.8V	I/O
HDMI_CEC	General Purpose 1-Wire bus interface, consumer electronics control bus	1.8V	I/O

17. LVDS

Signal	Description	Voltage	Spec
LVDS_D0_N	LVDS Channel differential negative data 0	1.8V	O
LVDS_D0_P	LVDS Channel differential positive data 0	1.8V	O

LVDS_D1_N	LVDS Channel differential negative data 1	1.8V	O
LVDS_D1_P	LVDS Channel differential positive data 1	1.8V	O
LVDS_D2_N	LVDS Channel differential negative data 2	1.8V	O
LVDS_D2_P	LVDS Channel differential positive data 2	1.8V	O
LVDS_D3_N	LVDS Channel differential negative data 3	1.8V	O
LVDS_D3_P	LVDS Channel differential positive data 3	1.8V	O
LVDS_CLK_N	LVDS Channel differential negative clock	1.8V	O
LVDS_CLK_P	LVDS Channel differential positive clock	1.8V	O
LVDS_VDD_EN	LVDS panel power enable	1.8V	O
LVDS_BKLT	Backlight On/Off	1.8V	O
LVDS_BKLT_PWM	Backlight brightness control	1.8V	O

18. eDP

Signal	Description	Voltage	Spec
EDP_TX0_N	eDP signal link	1.8V	O
EDP_TX0_P	eDP signal link	1.8V	O
EDP_TX1_N	eDP signal link	1.8V	O
EDP_TX1_P	eDP signal link	1.8V	O
EDP_TX2_N	eDP signal link	1.8V	O
EDP_TX2_P	eDP signal link	1.8V	O
EDP_TX3_N	eDP signal link	1.8V	O
EDP_TX3_P	eDP signal link	1.8V	O
EDP_AUX_N	eDP auxiliary channel	1.8V	O
EDP_AUX_P	eDP auxiliary channel	1.8V	O
EDP_PWR_EN	eDP Power On/Off	1.8V	O
EDP_HPD	Hot plug detection	1.8V	I
EDP_BKLT	Backlight On/Off	1.8V	O
EDP_BKLT_PW	Backlight brightness control	1.8V	O

M			

19. MIPI Audio Interface (2 pins)
    - SLIMbus
    - SoundWire

Signal	Description	Voltage	Spec
AUDIO_MIPI_CLK	MIPI Audio clock	1.8V	I
AUDIO_MIIPI_DAT	MIPI Audio data	1.8V	I/O

20. Touchscreen

Signal	Description	Voltage	Spec
TS_Y_P	Touch screen Y positive	1.8V	I
TS_X_N	Touch screen Y negative	1.8V	I
TS_Y_N	Touch screen Y negative	1.8V	I
TS_X_P	Touch screen X positive	1.8V	I

21. SmartCard
    - Smart card interface is designed to facilitate communication to SIM cards, compatible with ISO/IEC 7816-3.

Signal	Description	Voltage	Spec
SIM_PORT_CLK	Clock for the smartcard	1.8V	I
SIM_PORT_PD	Card insertion detect	1.8V	O
SIM_PORT_RST_B	Reset signal	1.8V	I
SIM_PORT_SVEN	Vcc enable	1.8V	I
SIM_PORT_TRXD	Transmit/receive data	1.8V	I/O

22. Keypad
    - 4 x 4
    - Using general purpose GPIOs

Signal	Description	Voltage	Spec

KPP_COL[0-3]	Column	1.8V	I
KPP_ROW[0-3]	Row	1.8V	I

23. System Management (5 pins)

Signal	Description	Voltage	Spec
SOC_RST	SoC SoC Power On Reset	1.8V	I
SOM_PWR	Module/PMIC power on. Carrier board should not be powered up until the Module asserts the SOM_PWR signal.	1.8V	I
SOC_PWR	SoC power on	1.8V	I
SOM_STBY	Module/PMIC stand by request. The Module shall drive this signal low when the system is in a standby power state.	1.8V	O
SOM_RST	Module Power on reset. Reset input from Carrier board. Carrier drives low to force a Module reset.	1.8V	O
GWDOG_RST	WatchDog Reset Input, GPIO	1.8V	I
CB_PWR_EN	Carrier board power enable, input from Carrier board.	1.8V	O
CB_PGOOD	Carrier board power good indication	1.8V	I
SOM_PGOOD	SoM module power good indication	1.8V	O

24. RTC
    - RTC backup battery supply input is available to keep the RTC running if the main supply is not present.

Signal	Description	Voltage	Spec
RTC_LICELL	RTC backup battery supply input	1.8V	I

25. JTAG
    - JTAG facilities **may** be provided on a SoM-C
    - If implemented the JTAG interface **shall** use the 10 pin JTAG connector (0.05" pitch)
26. Camera - MIPI CSI

Signal	Description	Voltage	Spec
GND	GND (crosstalk isolation)	1.8V	
CSI_C_N	CSI differential negative clock inputs	1.8V	I
CSI_C_P	CSI differential positive clock inputs	1.8V	I
GND	GND (crosstalk isolation)	1.8V	
CSI_D3_N	CSI differential negative data 3 inputs	1.8V	I
CSI_D3_P	CSI differential positive data 3 inputs	1.8V	I
GND	GND (crosstalk isolation)	1.8V	
CSI_D2_N	CSI differential negative data 2 inputs	1.8V	I
CSI_D2_P	CSI differential positive data 2 inputs	1.8V	I
GND	GND (crosstalk isolation)	1.8V	
CSI_D1_N	CSI differential negative data 1 inputs	1.8V	I
CSI_D1_P	CSI differential positive data 1 inputs	1.8V	I
GND	GND (crosstalk isolation)	1.8V	
CSI_D0_N	CSI differential negative data 0 inputs	1.8V	I
CSI_D0_P	CSI differential positive data 0 inputs	1.8V	I
GND	GND (crosstalk isolation)	1.8V	
CSI_MCLK	Master clock output for CSI camera	1.8V	O
CSI_GPIO	CSI Camera GPIO	1.8V	O
CSI_SCL	I2C clock	1.8V	OD/PU
CSI_SDA	I2C data	1.8V	OD/PU

27. SATA

Signal	Description	Voltage	Spec
SATA_RX_N	Differential SATA receive positive data	1.8V	I
SATA_RX_P	Differential SATA receive negative data	1.8V	I
SATA_TX_P	Differential SATA transmit positive data	1.8V	O

SATA_TX_N	Differential SATA transmit negative data	1.8V	O
SATA_PWR_EN	SATA port power enable	1.8V	O

2. Hardware Feature Details

Carrier Board Interface

96Boards Compute SoMs will be connected to the Carrier board using 1-4 100 pin connector pairs and nut and bolt spacers for ruggedized/vibration environments.

Connectors

96Boards Compute SoM specification uses 0.5mm pitch connectors resulting in a small footprint. It is **recommended** that the designer choose from several below options. Samtec and Panasonic/Matsushita manufacture suitable connectors.

Please do note different connector choice has different board to board separation, which restricts components underside the board to low profile and low power for thermal reasons.

Example part numbers:

Family	SoM Part no	Baseboard Part no
Samtec Rugged Edge-Rate	ERF5-050-05.0-L-DV	ERM5-050-02.0-L-DV
Panasonic AXK	AXK600337YG	AXK500137YG
Panasonic AXKS	AXK6S00437YG	AXK5S00337YG

Comparison

Connector Series	Multi Source	Rugged	Size (mm)	B2B (mm)	Stack (mm)
Samtec Edge-Rate	N	Y	29.1 x 5.6	7	7.0
Panasonic AXK	N	Y	28.2 x 5	3	3.0
Panasonic AXKS	N	Y	28.2 x 5	7	7.0*

96Boards Compute SoM Carrier Board

The carrier board for 96Boards Compute SoM is **strongly recommended** to be implemented to any of the existing 96Boards specification.

3. Software

96Boards SoM-C modules **shall** meet the following requirements:

Users **shall** be able to install their own applications on the module. This requires the supply and support of a software development environment. It is **strongly recommended t**hat vendors provide upstream support for a SoM-C in one or more of the following projects:

a. Open Source firmware
   Embedded Base Boot Requirements (EBBR) specification compliant. Such specification defines an interface between platform firmware and an operating system.
   Implementation can be UBoot or UEFI using device tree.
b. Kernel
   Latest Android AOSP Common kernel
   Latest LTS or stable upstream Linux kernel
c. Operating System
   Latest Android AOSP
   Latest Linux distribution (e.g. OE/Yocto, Debian, Ubuntu, Fedora etc.)

Support for new versions of the supported kernels and operating systems **shall** be made within 6 months of their release for a minimum of 3 years after SoM product release. All 96Boards branded modules **shall** be able to boot an upstream Linux or AOSP kernel to a shell prompt on a serial connection to UART0 off X1 connector.

All module firmware and software shall be updateable from the baseboard without requiring JTAG.

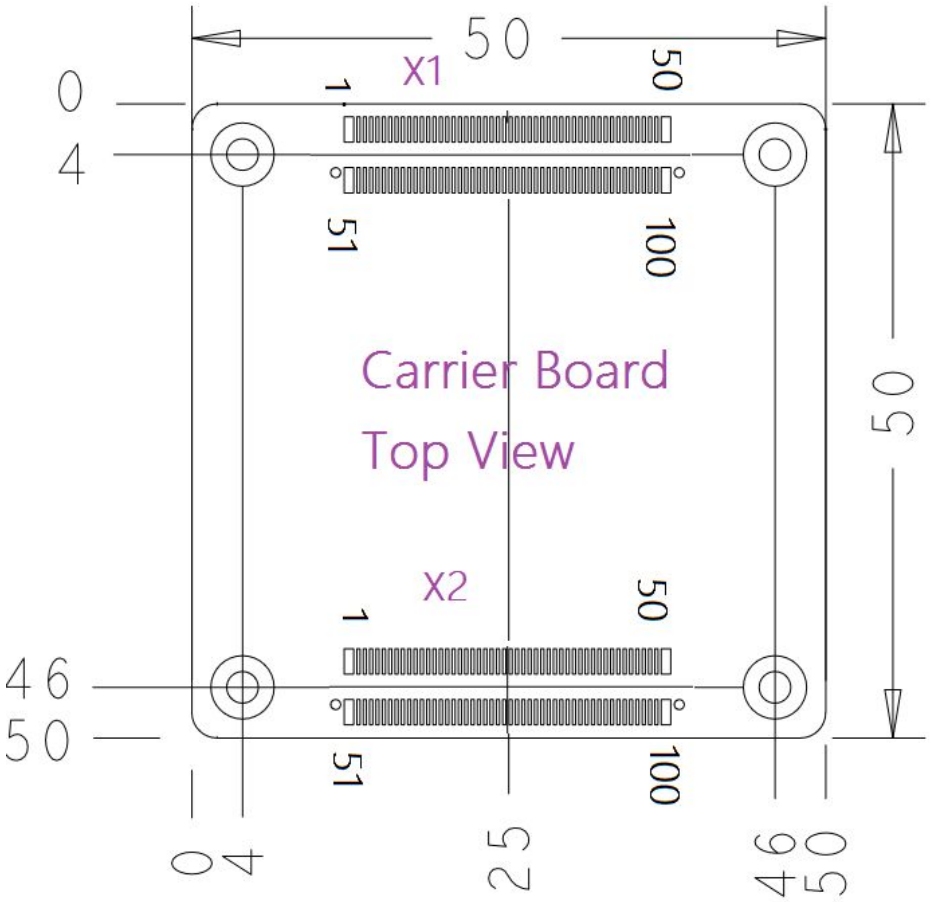
4. Security Requirements

All modules shall have a unique hardware ID that can be read by the user. All modules shall have built-in security features including (but not limited to):

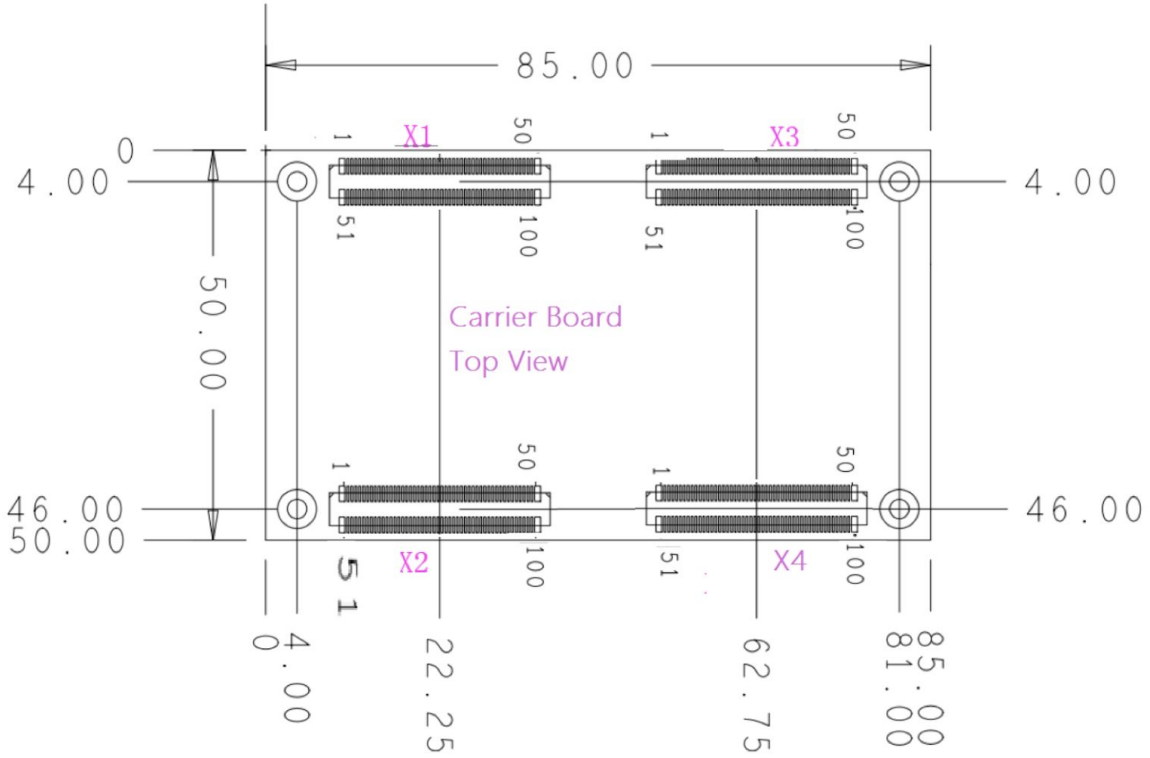
- Pre-installation or ability to install a unique and immutable public key or hash of a public key with a known secret private key
- A TRNG or suitable source of strong entropy

APPENDIX

2D Reference Drawing（SoM-CA）



2D Reference Drawing（SoM-CB）



Change History

v0.1	May 2017	Initial Specification
v0.2	Dec 2017	Specify multiple connectors with multiple profiles
V0.3	Jan 2018	Reduce module size Need to select vendor for 0.5mm pitch rugged connectors
V0.4	Sep 2018	Update interfaces
V0.9.5	Jan 2019	Update interfaces with MUX definitions
V0.9.6	Feb 2019	Finalise pin layout and carrier board recommendations
V0.9.7	March 2019	Remove HDMI from X4 replaced with additional DC power
V0.9.8	March 2019	Added software requirement with recommendation to EBBR
V1.0	March 2019	Added reference drawings

-------SPECIFICATION ENDS-------