AI_ML

Hardware User Manual

Powered by:

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1 DOCUMENT DETAILS

1.1 Document History

Version	Author		Description Of Changes
	Name	Date	
1.0	*eInfochips*	*25-June-2019*	*Initial release*

Table 1: Document History

1.2 Definition, Acronyms and Abbreviations

Acronyms and abbreviation definitions

Acronym / Abbreviation	Definition
AI	Artificial Intelligence
BOM	Bill of Materials
BT	Bluetooth
BLE	Bluetooth Low Energy
CLK	Clock
CPU	Central Processing Unit
CS	Chip Select
CSI	Camera Serial Interface
DSI	Display Serial Interface
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
EN	Enable
ESD	Electro-Static Discharge
GND	Ground
GPIO	General Purpose I/O
GPS	Global Positioning System
HDMI	High Definition Multimedia Interface
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
INT	Interrupt
LDO	Low Drop-Out
LPDDR	Low Power Double Data Rate
LTE	Long-Term Evolution
MIPI	Mobile Industry Processor Interface
ML	Machine Learning
PCB	Printed Circuit Board
PCIE	Peripheral Component Interconnect Express
PMIC	Power Management IC
PWM	Pulse-Width Modulation
RAM	Random Access Memory
RGMII	Reduced Gigabit Media Independent Interface
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RX	Receive
SCL	Serial Clock
SD	Secure Digital
SDA	Serial Data

SDI	Secure Digital Interface
SOM	System On Module
SPI	Serial Peripheral Interface
TX	Transmit
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WLAN	Wireless Local Area Network

Table 2: Definition, Acronyms and Abbreviation

2 PREFACE

This document provides an overview of the iMX8X ML (AI_ML) development kit based on NXP's iMX8 Quad X Plus SoC. It provides step-by-step information about hardware components and associated software release.

2.1 Intended Audience

This document is intended for technically qualified personnel. It is not intended for general audiences.

2.2 Intended Use

The development platform supports a wide range of industry interfaces and offers a comprehensive hardware and software design. This platform enables developers to evaluate and create solutions targeted at various market segments while customers and OEMs can build their products based on these designs directly or with customizations.

3 OVERVIEW

The AI_ML board is a 96Boards compliant community board based on NXP i.MX 8QuadXPlus Quad core Processor.

AI_ML provides an ideal building block for simple integration in target markets requiring rich multimedia functionality, powerful graphics processing and video capabilities, as well as high-processing power which can be capable for AI (Artificial Intelligence) & ML (Machine Learning), RoHS compliant, cost effective with low power consumption.

3.1 Key features

The following table lists its key features:

<table>
<tr>
<td>
CPU

i.MX 8QuadXPlus of NXP
Four ARM Cortex-A35 (1.2 GHz) support ARM virtualization extensions
One ARM Cortex-M4F (264 MHz) for real-time applications
1x HiFi4 DSP
All devices include separate GPU and VPU subsystems as well as a failover-ready display controller
Advanced multicore audio processing is supported by the ARM cores
High performance Tensilica® HiFi 4 DSP
AArch64 for 64-bit support and new architectural features

GPU

16 execution units optimized for higher performance
Supports OpenGL 3.0, 2.1 ; OpenGL ES 3.1, 3.0, 2.0, and 1.1; OpenCL 1.2 Full Profile and 1.1; OpenVG 1.1; and Vulkan
High-performance 2D Blit Engine

VPU

H.264 encode (1080p30)

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Connectivity

WiFi 5 GHz & 2.4GHz IEEE 802.11a/b/g/n/ac (FCC Certified On-Board WiFi-BT Module # 450-0169C)
Bluetooth® v4.2 (BLE)
Gigabit Ethernet (10/100/1000 Mbit/s IEEE 802.3)
LTE Module (EC25 series) on mini-PCIe connector

I/O Interface

One 40-pin Low Speed (LS) expansion connector
UARTx2, SPI, I2S, I2C x2, GPIO x12, DC power (12V, 5V, 1.8V)
One 60-pin High Speed (HS) expansion connector
4L-MIPI DSI, 2L+4L-MIPI CSI, SPI, USB, I2C x2, DC power (1.8V)
AI_ML board can be made compatible with Camera, Display, Sensors, LTE Module and Audio interface as an add-on mezzanine.

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Memory

RAM:
2GB LPDDR4 at up to 1200 MHz clock
Storage:
SD 3.0 (UHS-I)
512 Mb NOR FLASH on Octal-SPI
256 Kb EEPROM

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USB

1 x USB 2.0 micro AB OTG
2 x USB 3.0 type A

Debug

Debug USB type AB (UART to USB)
JTAG (10 pin)

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Video

1080p30 HD video play on HDMI 3.0 (DSI to HDMI using MIPI Switch)

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<td>
Switches

Power ON/OFF
Processor RESET
Boot Mode (x4) selection

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Camera

4 lane MIPI port

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LEDs

4 x User LEDs
2 x LEDs for BT and WLAN activity

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Audio

4 - MEMS Digital Microphones on I2S for Audio Input

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Miscellaneous
2x UART, 1x I2C, 2x MI2S, 1x SPI, 2x GPIO’s on LS-Expansion Connector.
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Power Input & Consumption	Physical & Operating Characteristics
Voltage In: +8V to 18V@5A through DC jack	• **Dimension:** 85 x 100 mm meeting 96Boards™ Consumer Edition 'extended' B Form Factor • **Number of Layers:** 12 Layers • **Operating Temperature:** 0° C to +55° C • RoHS and Reach compliant

Table 3: AI_ML Key Features

3.2 Applications

The AI_ML can used in a wide range of products across many different target markets. Some of the typical applications are:

- Consumer Electronics
- Internet of Things
- Artificial Intelligence
- Machine Learning
- Domestic Robot
- Digital signage
- Security & Surveillance
- Biometric Access Control Systems
- Home and Health Hub
- Human-machine interface
- Home energy management systems
- In-flight entertainment

3.3 Board overview

Figure 1: AI_Ml Board Top View

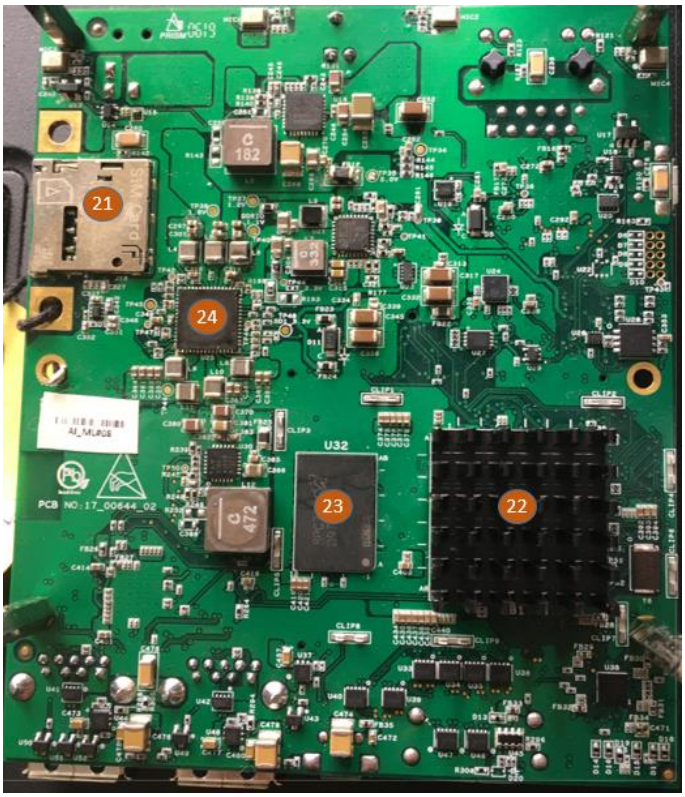

Figure 2: AI_Ml Board Bottom View

#	Description
1	RESET Switch
2	Power Jack
3	Ethernet connector
4	ON/OFF Switch
5	USB Debug connector
6	LTE mini-PCIe connector
7	JTAG connector
8	Boot Mode Selection Switch
9	LS Expansion connector
10	FAN connector
11	WiFi-BT Module
12	HS Expansion connector
13	microSD connector
14	HDMI connector
15	Micro AB USB OTG connector
16	User LEDs 1-2
17	USB Type A connector
18	User LEDs 3-6
19	USB Type A connector
20	Digital MICs
21	SIM card slot
22	Heatsink on Processor
23	LPDDR4
24	PMIC

Table 4: Board Overview

4 UNPACKING THE KIT

The AI_ML is shipped with the items listed in below Table. Ensure the items are available in the AI_ML Box.

ITEM	DESCRIPTION
CPU board	CPU board with i.MX 8QuadXPlus application processor, WiFi/BT Module, Memory and PMIC
Power supply Adapter	Universal Power Adapter, 12V DC@5A, with 96 board compatible Power Connector
AC Power cord	Cable assembly with US version
SD Card with BSP image	Micro SD Card, 32Gb, Class-10 with BSP Image
Heat Sink	Mounted Bottom Side on Processor: 24.5 C/W, 9 mm x 21 mm x 21 mm
Base Plate	Mounting Bracket on which CPU Board Is Mounted
Micro USB Cable	USB Cable, USB A Male to Micro B, for interface to debug port
Studs/Screws	Mounted with Base Plate
QSG	Quik Start Guide

Table 5: Contents of the AI_ML Kit

4.1 Optional Accessories

Below Table lists additional equipment not included with the AI_ML Box.

ITEM	DESCRIPTION
FAN	Supports # MC25060V1-000U-A99, Placement location on Mounting Bracket
FAN accessories	FAN supporting accessories to be provided along with the FAN as per customer order

Table 6: Optional Accessories for AI_ML Kit

5 SETTING UP THE SYSTEM

1 SD Card

- Insert the Micro-SD card into socket J11 on the AI_ML CPU Board

2 Connect USB Debug Cable

- Connect the micro-B end of a USB cable into debug port J5. Connect the other end of the cable to a PC acting as a host terminal.
- Open the terminal window (i.e., Hyper Terminal or Tera Term) and apply the following configuration.
  - Baud rate: 115200
  - Data bits: 8
  - Stop bit: 1
  - Parity: None
  - Flow control: None

3 Connect HDMI Display (Optional)

- Connect the HDMI cable one end into HDMI port J14. Connect the other end of the cable to HDMI supported Display.

4 Connect Ethernet Cable (Optional)

- Connect the Ethernet cable to the Ethernet Jack J4 (near to Debug Connector).

5 Connect Key-Board & Mouse (Optional)

- Insert USB Key-board & USB Mouse to J12 & J13 USB 3.0 ports on Top side of CPU
- Mouse & Key-board can be observed/Tracked on HDMI Display

6 Connect LTE Module (Optional)

- Insert LTE module (Quectel – EC25) on Mini-PCIe connector J6 located near Power jack
- Also Insert SIM card to get connectivity on J16 at Bottom side of CPU below LTE Module.

7 Connect D3 Camera Mezzanine (Optional)

- Connect D3 camera Mezzanine (96 standard compliant Board) on J10 & J8 from Top side of AI_ML CPU to operate the 4-lane CSI Camera

8 Connect Power Supply

- Connect the plug of the 12V power supply to the “8V-18V DC IN” on connector J9. When power is connected to the AI_ML, it will automatically begin the boot sequence.

5.1 BOOT PROCESS FOR LINUX IMAGE

5.1.1 Boot Process

Switch SW3 to ON, ON, OFF, OFF (from 1-4 bit) to boot from the SD card, as shown in Figure.

Figure 3: BOOT MODE selection Switch Position

- Power on the AI_ML board.
- During the boot process, there will be console prints on the terminal window of the PC (if connected).
- To work from the terminal window on the host PC, press 'Enter' at the terminal window to get the command prompt. Account name: **root**, password none.

5.1.2 DIP SWITCH CONFIGURATION

Below Table shows the switch (SW3) configuration of boot mode for AI_ML.

BOOT_MODE 3	BOOT_MODE 2	BOOT_MODE 1	BOOT_MODE 0	Boot Source
0	0	0	0	Boot From Fuses
0	0	0	1	Serial Downloader
0	0	1	0	Internal Boot
0	**0**	**1**	**1**	**SD1 Boot (Default)**
0	1	1	0	Boot From Octal-SPI

Table 7: BOOT MODE Selection Switch configuration

5.2 BUTTON FUNCTIONS

Below table shows the functions of the push buttons and switches on the board.

ITEM	DESCRIPTION
SW1	ON/OFF Switch; • Long press/hold: While the device is awake, pressing and holding the ON/OFF Switch for longer than 5 seconds will result in the device powering off. • Short press/hold: Once powered off, pressing and holding the ON/OFF Switch for longer than 0.5 seconds will result in the device powering on.
SW2	RESET Switch; • While the device is awake, pressing the RESET Switch will force a hard reset of AI_ML Board.
SW3	BOOT Mode selection Switch; • Used for boot configuration according to SCU boot mode

Table 8: BUTTON configurations

5.3 LED STATUS

Below table shows the status of LEDs on the board

ITEM	DESCRIPTION
LED1	Indication to check the LTE Module network status. Location near Boot mode switch
LED2	BT Status LED in Blue color
LED3	WiFi Status LED in Yellow Color
LED4	USER LED-1; Green Color
LED5	USER LED-2; Green Color
LED6	USER LED-3; Green Color
LED7	USER LED-4; Green Color

Table 9: Status LED configurations

6 AI_ML BOARD OVERVIEW

6.1 System Block Diagram

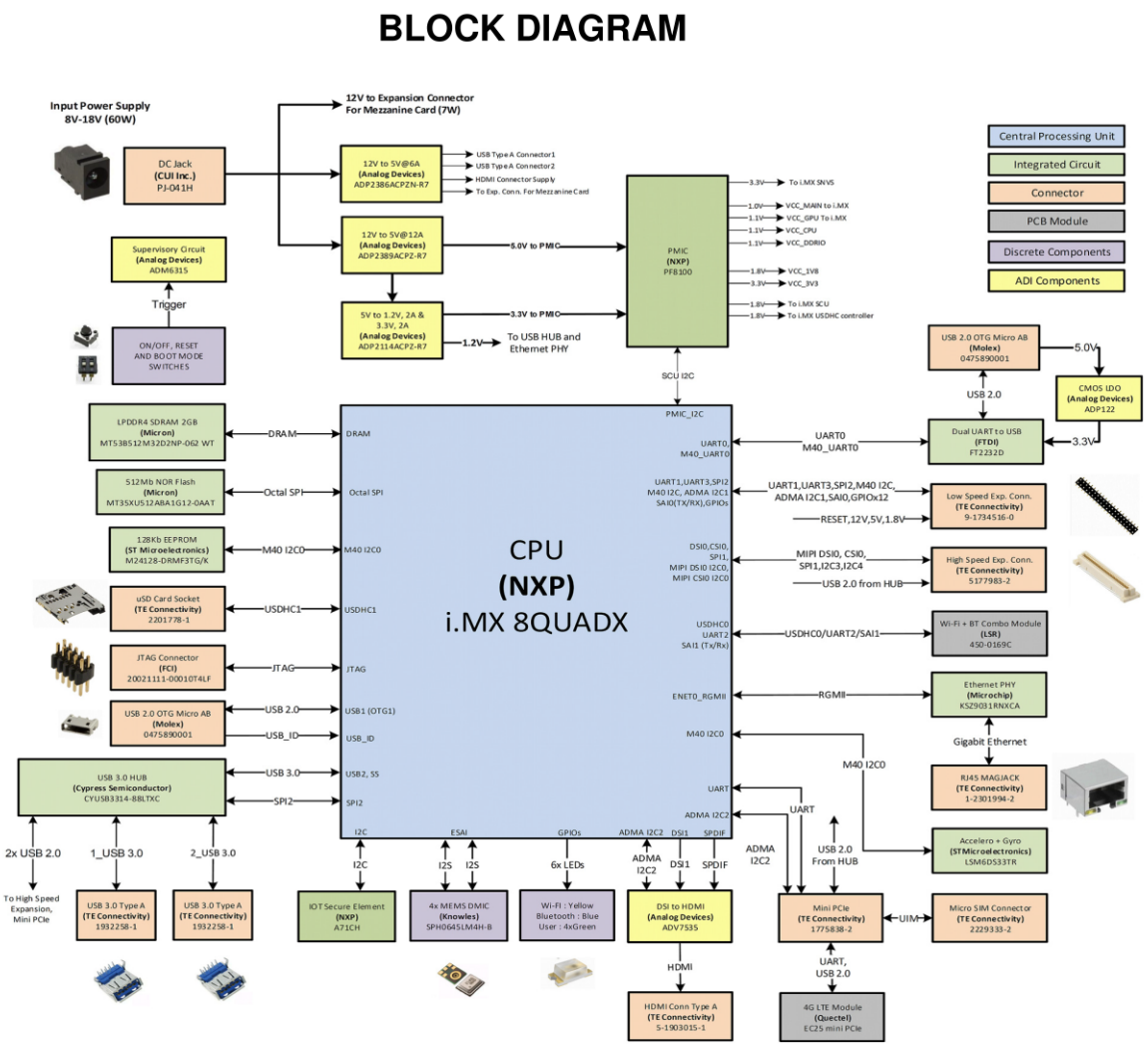

Figure 4: AI_ML CPU System Level Block Diagram

6.2 Processor

The i.MX 8X processors consist of three to five ARM®cores (two to four ARM Cortex®-A35 and one Cortex-M4F). All devices include separate Video Processing Unit (VPU) and Graphics Processing Unit (GPU) subsystems as well as a failover-ready display controller. Advanced multicore audio processing is supported by the ARM cores and a high performance Tensilica® HiFi 4 DSP for pre- and post-audio processing as well as voice recognition. The i.MX 8X Family supports up to three displays with multiple display output options, including parallel, MIPI-DSI, and LVDS.

6.3 Memory

- The LPDDR4 2GB (512Mbit x 32) is a 16bit width bus implementation interfacing directly to the iMX8X Processor build-in LPDDR controller.
- The 96Boards specification calls for microSD port to be on the board. The microSD card is used to flash the board interfacing with iMX8X QUAD Core Processor USDHC1 interface supporting SDIO 3.0 specifications. The size supports up to 64 GB. The maximum SDIO clock is 200 MHz.
- The NOR flash is given as option to flash the board in absence of microSD card. NOR flash is interfacing directly to iMX8X QUAD Core Processor Octal-SPI interface. The size supports 512Mb. The maximum Octal-SPI clock is 80 MHz.

- The EEPROM is interfacing directly to iMX8X QUAD Core Processor I2C interface. The size supports 256Kb.

6.4 Video

- The 96Boards specification calls for a DSI port on High Speed connector and HDMI port to be on the board. The AI_ML provides native support for HDMI interface.
- In AI_ML,
    1. **DSI0** port connected to **High speed connector**
    2. **DSI1** port converted to HDMI through ADV7535 for **HDMI display**
- **DSI0:** It supports a resolution from 480i to 1080p at 30Hz.
- **DSI1 to HDMI:** It supports a resolution 1080p via DSI to HDMI Bridge Chip (ADV7535).

6.5 Camera Support

- AI_ML supports one **4-lane CSI0** port which used to connect high speed expansion connector as per 96boards standard.

6.6 Audio

- AI_ML supports the requirement of Audio Input with **4 - MEMS Digital Micro-phones** (with internal Digital Filters) on I2S interface.
- HDMI Audio supports **SPDIF** (single line interface) with HDMI Bridge chip.

6.7 Connectivity

6.7.1 WiFi

- The 96Boards specification calls for WiFi module to be on the board.
- AI_ML supports **Wi-Fi (802.11 a/b/g/n/ac, 2.4GHz and 5GHz)** over **450-0169C (EC-25)** certified module with Chip Antenna on Module.
- Wi-Fi will be mainly used for cloud connectivity.
- The WiFi module is interfacing with iMX8X Processor USDHC0 interface supporting SDIO 3.0 specifications.
- The maximum SDIO clock is 200 MHz.
- Module# 450-0169C is the **Certified with Chip antenna on Module**.

6.7.2 Bluetooth

- The 96Boards specification calls for Bluetooth to be on the board.
- AI_ML supports **Bluetooth 4.2** over **450-0169C** module.
- Bluetooth is used for Audio streaming and BLE sensor communication.
- Full UART communication is used to transfer data between processor and connected Bluetooth device.
- UART interface is used for Audio streaming over Bluetooth.
- **BLE** is also supported in the Module.

6.7.3 RGMII

- AI_ML supports 1Gbps Ethernet connection.
- Single chip 10/100/1000 Mbps Ethernet Transceiver Suitable for IEEE 802.3 Applications.
- Programmable LED Outputs for Link, Activity and Speed.
- Power-Down and Power-Saving Modes.

6.7.4 USB 2.0

- AI_ML supports USB2.0 OTG port with micro-AB connector.
- USB OTG supports either USB as Host or USB as Device.

6.7.5 USB 3.0

- AI_ML have one USB 3.0 HUB (CYUSB3304-68LTXI - Cypress) connected to USB 3.0 port of iMX8X Processor.
- Two downstream port used as USB 3.0 Host port with USB 3.0 Type-A connectors.
- Separate load switches on the board will limit USB current on USB 3.0 ports as per USB specifications.
- USB bandwidth will be shared between devices if more than one devices are attached to USB HUB.

6.7.6 LTE Module on Mini-PCIe

- AI_ML have provision of on Board mini-PCIe connector to support QUECTEL EC25 series of LTE Module.
- EC25 Mini PCIe module provides data connectivity on FDD-LTE, TDD-LTE, WCDMA, TD-SCDMA and GSM networks with PCI Express Mini Card 1.2 standard interface.
- EC25 module provides audio, high-speed data transmission and GPS/GLONASS functionality for your application.
- SIM card slot is provided on bottom side of the Board to get the connectivity
- UART interface is given to support for AT commands
- USB 2.0 interface used for data transmission, firmware upgrade, software debug and GNSS NMEA output
- PCM interface doesn't support on AI_ML board.
- I2C2 is provided to the Mini-PCIe connector.
- LED output to see the network status of the Module.

6.8 Debug

6.8.1 Debug USB

- AI_ML console is supported through debug USB connector which is converted from debug UART.

6.8.2 Debug JTAG

- AI_ML can be programmed through JTAG emulator.
- JTAG 10 pin connector provision is provided for JTAG debug and programming.

6.9 I/O Interfaces

6.9.1 40-pin Low Speed (LS) expansion connector

The following tables show the Low Speed Expansion Connector pin out:

Pin No.	96Boards Signals	AI_ML Signals	Remarks
1	GND	GND	
2	GND	GND	
3	UART0_CTS	LS_EXP_UART_1_CTS	
4	PWR_BTN_N	IMX8_ON_OFF_BUTTON	
5	UART0_TxD	LS_EXP_UART_1_TX	
6	RST_BTN_N	PMIC_POR_B_1V8	
7	UART0_RxD	LS_EXP_UART_1_RX	
8	SPI0_SCLK	LS_SPI3_SCK	
9	UART0_RTS	LS_EXP_UART_1_RTS	
10	SPI0_DIN	LS_SPI3_MISO	
11	UART1_TxD	NC	
12	SPI0_CS	LS_SPI3_CS0	
13	UART1_RxD	NC	
14	SPI0_DOUT	LS_SPI3_MOSI	
15	I2C0_SCL	LS_EXP_I2C0_SCL	
16	PCM_FS	LS_EXP_I2S_WS	

17	I2C0_SDA	LS_EXP_I2C0_SDA	
18	PCM_CLK	LS_EXP_I2S_SCLK	
19	I2C1_SCL	LS_EXP_I2C1_SCL	
20	PCM_DO	LS_EXP_I2S_DOUT	
21	I2C1_SDA	LS_EXP_I2C1_SDA	
22	PCM_DI	LS_EXP_I2S_DIN	
23	GPIO-A	LS_GPIO0_29	
24	GPIO-B	LS_GPIO1_03	
25	GPIO-C	LS_GPIO1_07	
26	GPIO-D	LS_GPIO1_31	
27	GPIO-E	LS_GPIO0_20	
28	GPIO-F	LS_GPIO2_00	
29	GPIO-G	LS_GPIO1_00	
30	GPIO-H	LS_GPIO1_13	
31	GPIO-I	LS_GPIO0_19	
32	GPIO-J	LS_GPIO1_14	
33	GPIO-K	LS_GPIO1_01	
34	GPIO-L	LS_GPIO3_07	
35	+1V8	VCC_1V8	1.8V
36	SYS_DCIN	VCC_12V0	12V
37	+5V	EXT_VCC_5V0	5V
38	SYS_DCIN	VCC_12V0	12V
39	GND	GND	
40	GND	GND	

Table 10: Low Speed Expansion Connector pin out

UART 1

- The 96Boards specifications calls for a 4-wire UART implementation (UART1) on the Low Speed Expansion Connector.
- The AI_ML implements UART1 as a 4-wire UART that connects directly to the IMX8X Processor. These signals are driven at 1.8V.

I2C {0/1}

- The 96Boards specification calls for two I2C interfaces to be implemented on the Low Speed Expansion Connector.
- The AI_ML implements both interfaces, I2C0 and I2C1 that connects directly to the IMX8X Processor.
- A 2.2K resistor is provided as pull-up for each of the I2C lines per the I2C specifications, these pull-ups are connected to the 1.8V voltage rail.

GPIO {A-L}

- The 96Boards specifications calls for 12 GPIO lines to be implemented on the Low Speed Expansion Connector.
- These signals are driven at 1.8V.

SPI 0

- The 96Boards specification calls for one SPI bus master to be provided on the Low Speed Expansion Connector.
- The AI_ML implements a full SPI master with 4 wires, CLK, CS, MOSI and MISO all connect directly to the IMX8X Processor. These signals are driven at 1.8V.

PCM/I2S

- The 96Boards specification calls for one PCM/I2S bus to be provided on the Low Speed Expansion Connector.
- The CLK, FS and DO signals are required while the DI is optional.
- The AI_ML implements a PCM/I2S with 4 wires, TXFC, TXC, TXD and RXD. The I2S signals are connected directly to the IMX8X Processor. These signals are driven at 1.8V.

6.9.2 60-pin High Speed (HS) expansion connector

The following table shows the High Speed Expansion Connector pin out:

Pin No.	96Boards Signals	AI_ML Signals	Remarks
1	SD_DAT0/SPI1_DOUT	HS_SPI0_MOSI	
2	CSI0_C+	CSI_MCP_CONN	
3	SD_DAT1	NC	
4	CSI0_C-	CSI_MCN_CONN	
5	SD_DAT2	NC	
6	GND	GND	
7	SD_DAT3/SPI1_CS	HS_SPI0_CS0	
8	CSI0_D0+	CSI_MDP0_CONN	
9	SD_SCLK/SPI1_SCLK	HS_SPI0_SCK	
10	CSI0_D0-	CSI_MDN0_CONN	
11	SD_CMD/SPI1_DIN	HS_SPI0_MISO	
12	GND	GND	
13	GND	GND	
14	CSI0_D1+	CSI_MDP1_CONN	
15	CLK0/CSI0_MCLK	MIPI_CSI0_MCLK_OUT	
16	CSI0_D1-	CSI_MDN1_CONN	
17	CLK1/CSI1_MCLK	CLOCK_GPIO3_8	
18	GND	GND	
19	GND	GND	
20	CSI0_D2+	CSI_MDP2_CONN	
21	DSI_CLK+	DSI_MCP_CONN	
22	CSI0_D2-	CSI_MDN2_CONN	
23	DSI_CLK-	DSI_MCN_CONN	
24	GND	GND	
25	GND	GND	
26	CSI0_D3+	CSI_MDP3_CONN	
27	DSI_D0+	DSI_MDP0_CONN	
28	CSI0_D3-	CSI_MDN3_CONN	
29	DSI_D0-	DSI_MDN0_CONN	
30	GND	GND	
31	GND	GND	
32	I2C2_SCL	HS_MIPI_CSI0_I2C0_SCL	
33	DSI_D1+	DSI_MDP1_CONN	
34	I2C2_SDA	HS_MIPI_CSI0_I2C0_SDA	
35	DSI_D1-	DSI_MDN1_CONN	
36	I2C3_SCL	HS_MIPI_DSI0_I2C_SCL	
37	GND	GND	
38	I2C3_SDA	HS_MIPI_DSI0_I2C_SDA	
39	DSI_D2+	DSI_MDP2_CONN	
40	GND	GND	
41	DSI_D2-	DSI_MDN2_CONN	
42	CSI1_D0+	NC	
43	GND	GND	
44	CSI1_D0-	NC	
45	DSI_D3+	DSI_MDP3_CONN	
46	GND	GND	
47	DSI_D3-	DSI_MDN3_CONN	
48	CSI1_D1+	NC	
49	GND	GND	
50	CSI1_D1-	NC	
51	USB_D+	N19835886	

52	GND	GND	
53	USB_D-	N19835894	
54	CSI1_C+	NC	
55	GND	GND	
56	CSI1_C-	NC	
57	HSIC_STR	NC	
58	GND	GND	
59	HSIC_DATA	NC	
60	RESERVED	VCC_1V8	Pull up by 100k Resistor

Table 11: High Speed Expansion Connector pin out

MIPI DSI 0

- The 96Boards specification calls for a MIPI-DSI to be present on the High Speed Expansion Connector.
- A minimum of one lane is required and up to four lanes can be accommodated on the connector.
- The AI_ML implementation supports a full four lane MIPI-DSI interface that is routed to the High Speed Expansion Connector.

MIPI CSI 0

- The 96Boards specification calls for two MIPI-CSI interfaces to be present on the High Speed Expansion Connector.
- Both interfaces are optional. CSI0 interface can be up to four lanes while CSI1 is up to two lanes.
- The AI_ML implementation supports a full four lane MIPI-CSI interface on CSI0. All MIPI-CSI signals are routed directly to/from the Processor.
- The AI_ML doesn't support for two lane CSI1 optional requirement.

I2C {CSI/DSI}

- The 96Boards specification calls for two I2C interfaces to be present on the High Speed Expansion Connector.
- Both interfaces are optional unless a MIPI-CSI & MIPI-DSI interfaces have been implemented. Then an I2C interface shall be implemented.
- For MIPI-CSI0 the companion CSI0_I2C0 is routed directly from the Processor.
- For MIPI-DSI0, the companion DSI0_I2C0 is routed directly from Processor.

HSIC

- The 96Boards specification calls for an optional MIPI-HSIC interface to be present on the High Speed Expansion Connector.
- The AI_ML implementation doesn't support this optional requirement.

Reserved

- The 96Boards specification calls for a 100K pull-up to 1.8V to be connected to pin 60 of the High Speed Expansion Connector.
- The AI_ML utilizes a 100K pull-up (R220) on pin 60.

SD/SPI

- The 96Boards specification calls for an SD interface or a SPI port to be part of the High Speed Expansion Connector.
- The AI_ML implements a full SPI master with 4 wires (96Boards SPI Configuration). CLK, CS, MOSI and MISO all connect directly to the iMX8X Processor. These signals are driven at 1.8V.

Clocks

- The 96Boards specification calls for one or two programmable clock interfaces to be provided on the High Speed Expansion Connector.
- These clocks may have a secondary function of being CSI0_MCLK. Clock provision of CLOCK_GPIO3_8 directly from Processor is provided to pin 17. These signals are driven at 1.8V.

USB

- The 96Boards specification calls for a USB Data line interface to be present on the High Speed Expansion Connector.
- The AI_ML implements this requirement by routing USB channel 2 from the USB HUB to the High Speed Expansion Connector.

6.10 Power management

AI_ML supports 12VDC (+8V to 18V @60W) for the input supply to power up processor and all its peripherals.

The processor and peripherals requires different voltage supplies and current for their normal functionality. The power supply section is designed to generate all required voltage rails with respective current requirements.

6.10.1 Input Power Supply

For protection of input power supply, below components are used

1. Fuse
2. TVS Diodes

For EMI EMC protection, below components are used

1. Common mode choke

For Input current sensing, below components are used

1. 0.01E Sense Resistor in series of input supply path
2. Two pins header across sense resistor

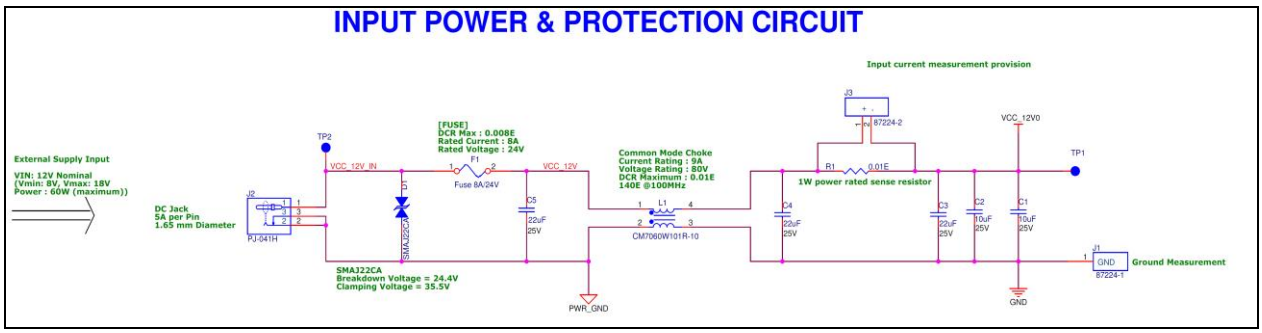

Figure 5: AI_MI Input Power & Protection Circuit

6.10.2 12V to 5V@6A Regulator ADP2386ACPZN-R7

- Regulator ADP2386ACPZN-R7 is selected to convert 5V (EXT_VCC_5V0) from 8-18V input power supply.
- This Regulator is in always in ON condition.

6.10.3 12V to 5V@8A Regulator ADP2389ACPZ-R7

- Regulator ADP2389ACPZ-R7 is selected to convert 5V (VCC_EXT_5V0) from 8-18V input power supply.
- This Regulator is in always in ON condition.

6.10.4 5V to 3.3V@2A , 1.2V@1A Regulator ADP2114ACPZ-R7

- Regulator LT8642SEV#PBF is selected to convert 3.3V and 1.2V from 5V generated DC power supply.
- This Regulator 3.3V supply is in always in ON condition.
- Enable of 1.2V power supply by PMIC.

6.10.5 PMIC (PC33PF8100PCES)

- PF8100 is used to provide sequencing to the processor and it is controlled through I2C.

- PMIC provides a highly programmable/configurable architecture with fully integrated power devices and minimal external components.
- PMIC provides up to Seven high efficiency buck converters, Four linear regulators with load switch options, RTC supply and a coin cell charger, Watchdog timer/monitor, Monitoring circuit to fit ASIL B safety level.
- PMIC designed as per datasheet.

Below are the features of PF8100:

- Seven buck converters,
  - ⇨ Single/dual phase/parallel options
  - ⇨ DDR termination tracking mode option
  - ⇨ Variable Switching Frequency option which helps in EMI/EMC radiations
- Four general purpose linear regulators
- Programmable output voltage, sequence, and timing
- OTP (one-time programmable) memory for device configuration

6.11 Switches and status LED's

6.11.1 Switches

- **ON-OFF Switch**
  Option 1: Long press/hold
  - ⇨ While the device is awake, pressing and holding the ON/OFF Switch for longer than 5 seconds will result in the device powering off.

  Option 2: Short press/hold
  - ⇨ Once powered off, pressing and holding the ON/OFF Switch for longer than 0.5 seconds will result in the device powering on.

- **RESET Switch:**
  - ⇨ While the device is awake, pressing the RESET Switch will force a hard reset of AI_ML Board.

6.11.2 Status LED's

- **User LEDs (LED4 to LED7)**
  - ⇨ The Four user LEDs are surface mount Green LEDs, 0603 size, located between the two USB type A connectors.

- **Bluetooth status LED (LED2)**
  - ⇨ The BT LED on the AI_ML is located next to the USBOTG connector, this LED reflects the status of the Bluetooth device in Blue color.

- **WiFi status LED (LED3)**
  - ⇨ The WiFi LED on the AI_ML is located beside the BT LED, this LED reflects the status of the Wi-Fi device in Yellow color.

6.12 Other Parts

- FAN and Heatsink are used to overcome thermal issue

7 MECHANICAL SPECIFICATION

As per 96boards Consumer Edition Extended B specification, connector Placement has to be followed as per below Figure.

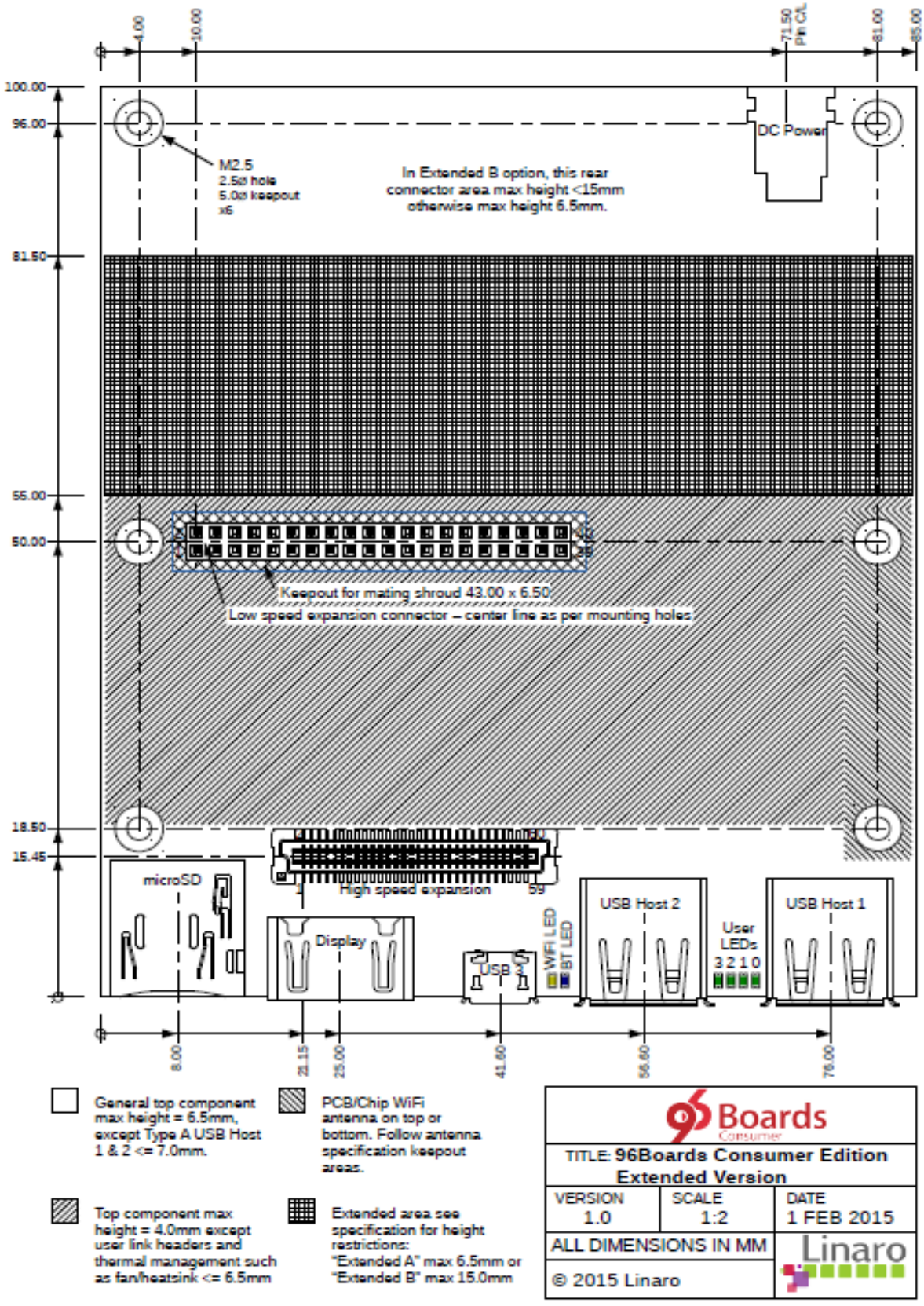

Figure 6: 96boards Consumer Edition Extended B specification for Placement

7.1 Additional interfaces to 96 Boards Compliance:

AI_ML includes interfaces which are in addition to the base 96boards CE Extended B specification. These include below mentioned interfaces.

- Digital MICs (MIC IN)
- Debug UART
- LTE on Mini-PCIe connector
- JTAG Debug
- RGMII Ethernet

Locations of these connectors are noted on the following drawing.

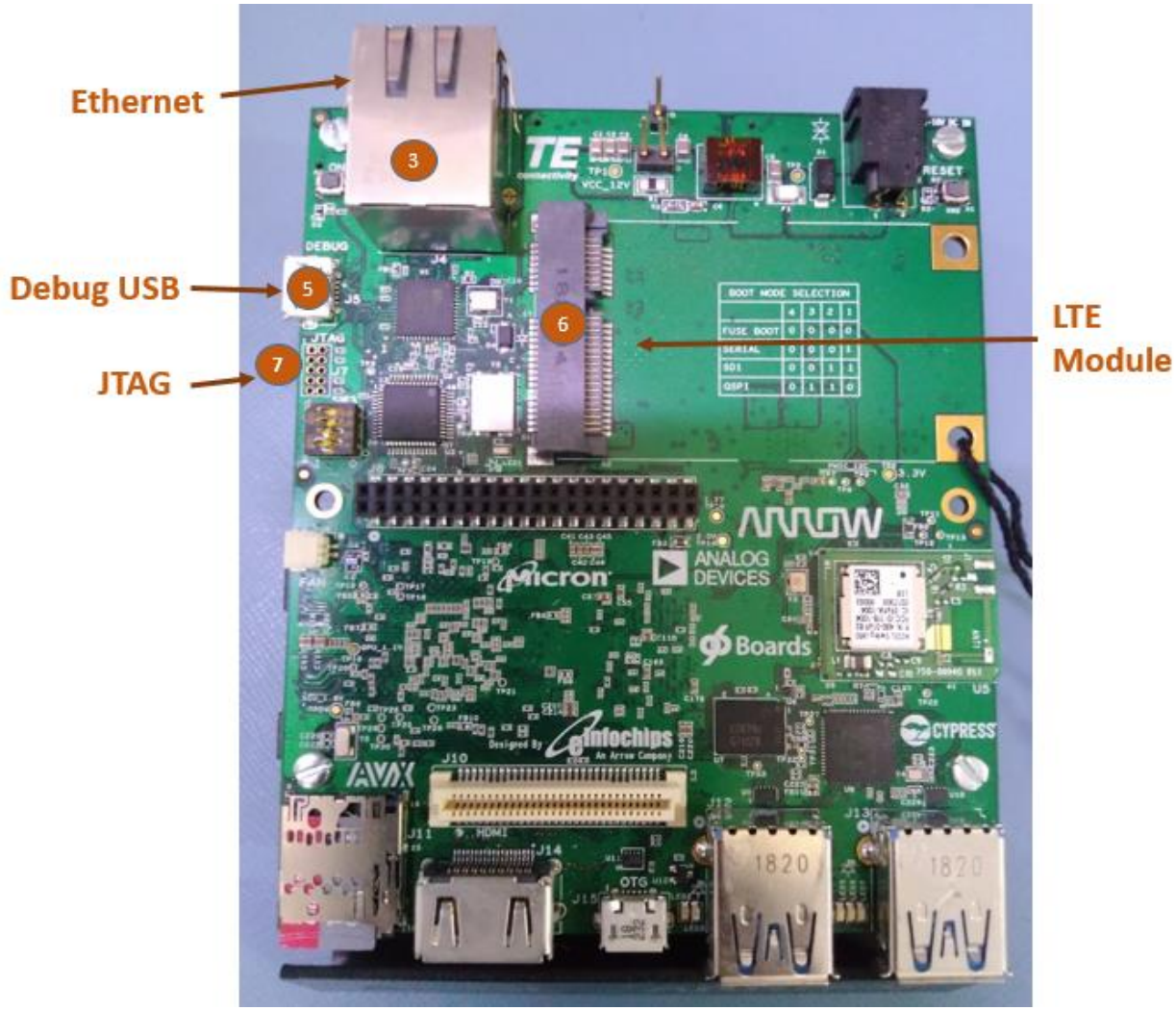

Figure 7: Additional interfaces Location on AI_ML