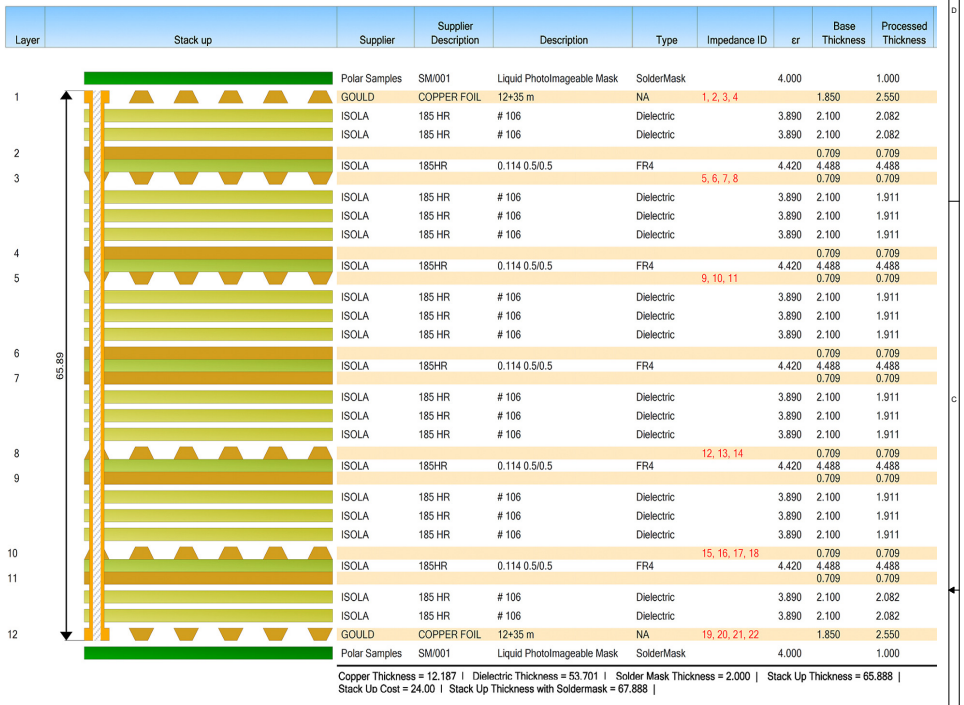
i.MX 8X ML Reference Design

MAJOR REVISION HISTORY :

PCB REV.	SCH. REV.	DESCRIPTION	DATE
1.0	1.0	REVIEW COMMENTS IMPLEMENTED DETAILED INFORMATION IN REV. HISTORY	04-OCT-2018
2.0	2.0	BETA CHANGES IMPLEMENTED AS PER DESIGN CHANGE TRACKER DOCUMENT.	24-DEC-2018
3.0	3.0	PROD. CHANGES IMPLEMENTED AS PER DESIGN CHANGE TRACKER DOCUMENT.	15-APR-2019

PAGE DESCRIPTION

PCB LAYER STACK-UP DETAILS :



Layer	Stack up	Supplier	Supplier Description	Description	Type	Impedance ID	εr	Base Thickness	Processed Thickness
		Polar Samples	SM/001	Liquid PhotoImageable Mask	SolderMask		4.000		1.000
1		GOULD	COPPER FOIL	12+35 m	NA	1, 2, 3, 4		1.850	2.550
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	2.082
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	2.082
2								0.709	0.709
		ISOLA	185HR	0.114 0.5/0.5	FR4		4.420	4.488	4.488
3						5, 6, 7, 8		0.709	0.709
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
4								0.709	0.709
		ISOLA	185HR	0.114 0.5/0.5	FR4		4.420	4.488	4.488
5						9, 10, 11		0.709	0.709
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
6								0.709	0.709
		ISOLA	185HR	0.114 0.5/0.5	FR4		4.420	4.488	4.488
7								0.709	0.709
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
8						12, 13, 14		0.709	0.709
		ISOLA	185HR	0.114 0.5/0.5	FR4		4.420	4.488	4.488
9								0.709	0.709
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
10						15, 16, 17, 18		0.709	0.709
		ISOLA	185HR	0.114 0.5/0.5	FR4		4.420	4.488	4.488
11								0.709	0.709
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	2.082
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	2.082
12		GOULD	COPPER FOIL	12+35 m	NA	19, 20, 21, 22		1.850	2.550
		Polar Samples	SM/001	Liquid PhotoImageable Mask	SolderMask		4.000		1.000

65.89

Copper Thickness = 12.187 | Dielectric Thickness = 53.701 | Solder Mask Thickness = 2.000 | Stack Up Thickness = 65.888 |
Stack Up Cost = 24.00 | Stack Up Thickness with Soldermask = 67.888 |

NOTES, UNLESS OTHERWISE SPECIFIED :

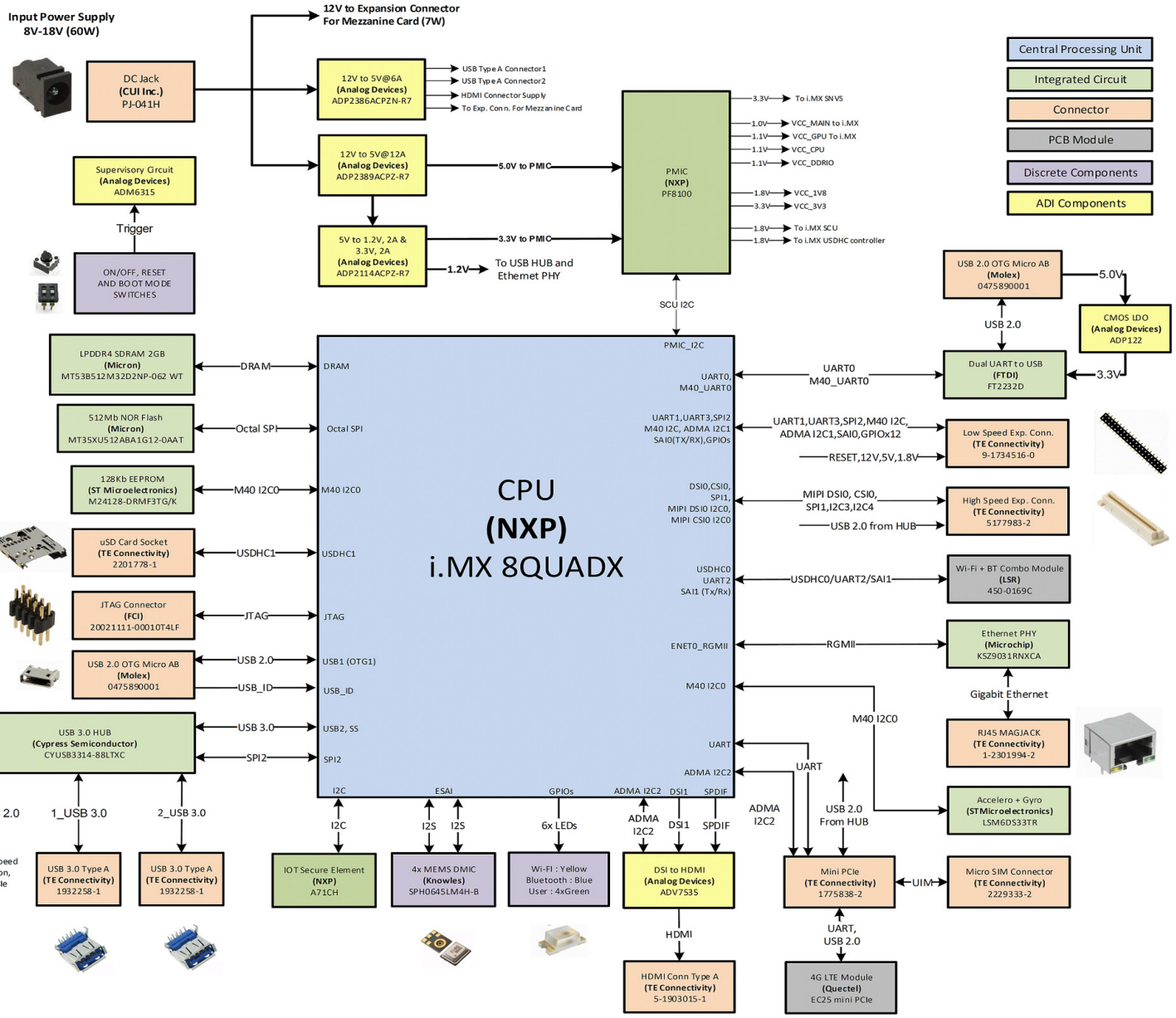
1. RESISTANCE VALUES ARE IN OHM.
2. PARTS NOT INSTALLED ARE INDICATED WITH 'DNP'.

PCB MECHANICAL DETAILS :

1. PCB SIZE: 85 mm X 100 mm
2. PCB THICKNESS: 1.62 mm
3. NUMBER OF LAYERS: 12
4. IMPEDANCE CONTROL: YES

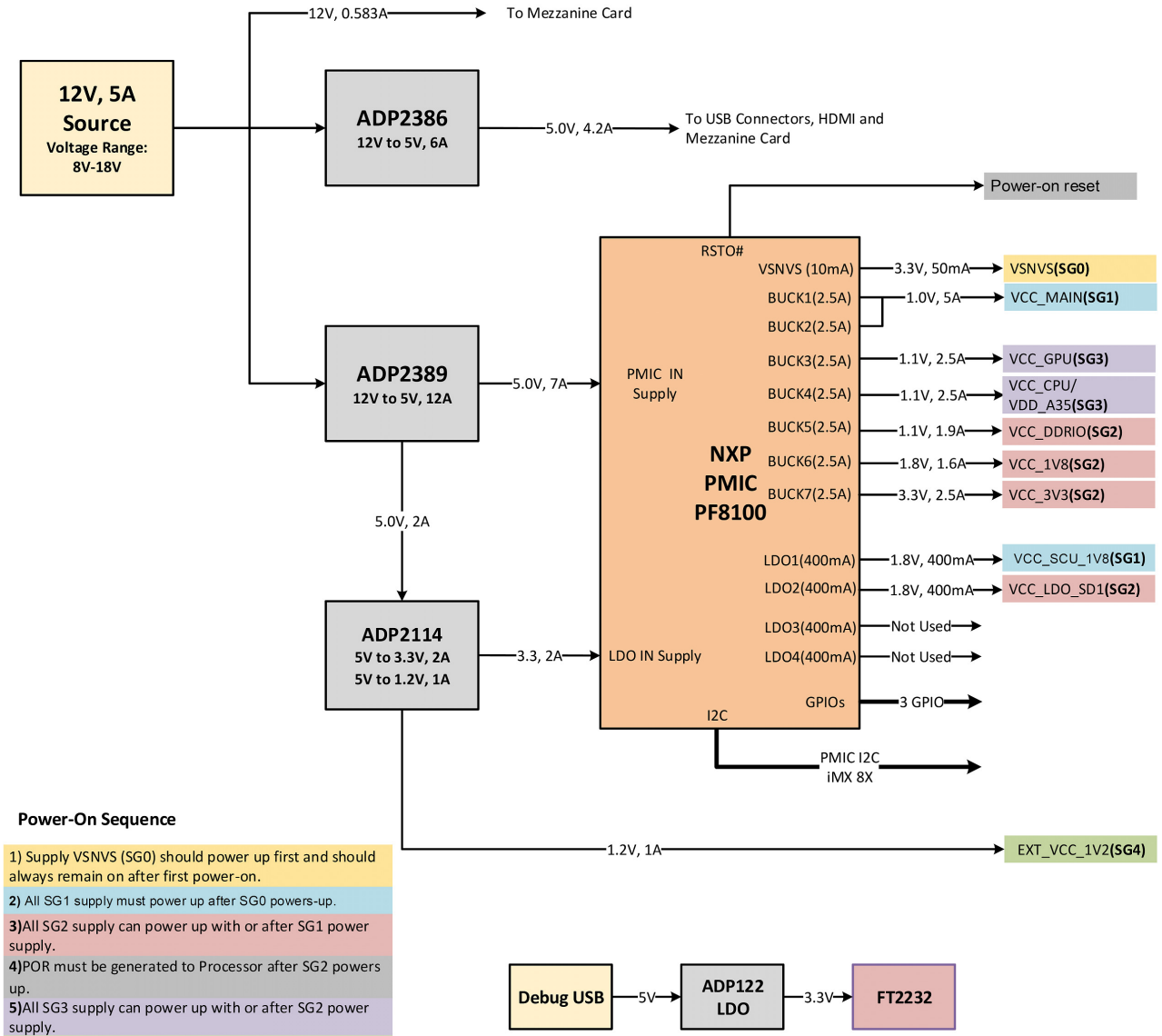
Project Arrow_iMX8XML_RD		Designed by eInfochips eInfochips An Arrow Company | The Solutions People
Title i.MX 8X ML Reference Design		
Size C	eInfochips#: 16_00644_03	Rev 3.0
Date: Monday, April 15, 2019	Sheet 1 of 30	

BLOCK DIAGRAM



Project: Arrow_iMX8XML_RD	Designed by eInfochips	
Title: BLOCK DIAGRAM		
Size: E	eInfochips#: 16_00644_03	Rev: 3.0
Date: Monday, April 15, 2019	Sheet 2 of 30	

POWER SCHEME



Power-On Sequence

1) Supply VSNVS (SG0) should power up first and should always remain on after first power-on.

2) All SG1 supply must power up after SG0 powers-up.

3)All SG2 supply can power up with or after SG1 power supply.

4)POR must be generated to Processor after SG2 powers up.

5)All SG3 supply can power up with or after SG2 power supply.

6)All SG4 supply can power up with or after SG3 power supply.

Project: Arrow_iMX8XML_RD	Designed by eInfochips	
Title: POWER SCHEME		
Size: E	eInfochips#: 16_00644_03	Rev: 3.0
Date: Monday, April 15, 2019	Sheet 3 of 30	

I2C ADDRESS TABLE

DEVICE	DEVICE ADDRESS	I2C	IO LEVEL	BOARD
NXP PMIC #PF8100	0x08	PMIC_I2C	1.8V/3.3V	CPU
EXPANSION CONN (LS)	NOT FIX	M40.I2C0	1.8V	MEZZANINE
EXPANSION CONN (LS)	NOT FIX	ADMA.I2C2	1.8V	MEZZANINE
EXPANSION CONN (HS)	NOT FIX	MIPI_DSI0_I2C0	1.8V	MEZZANINE
EXPANSION CONN (HS)	NOT FIX	MIPI_CSI0_I2C0	1.8V	MEZZANINE
SENSOR ACCEL+GYRO	0x6D	M40.I2C0	1.8V	CPU
EEPROM	0xA0	M40.I2C0	1.8V	CPU
DSI TO HDMI BRIDGE	0x3C	ADMA_I2C1	3.3V	CPU
QUECTEL PCIe CONN	TBD	ADMA_I2C2	1.8V	MODULE
USB 3.0 HUB	0X60	ADMA_I2C1	3.3V	CPU
A71CH SECURITY IC	0X93	ADMA_I2C2	1.8V	CPU

i.MX 8X GPIO TABLE

GREEN HIGHLIGHTED GPIOS ARE THE CHANGES FROM ALPHA TO BETA

D2P: MAROON HIGHLIGHTED GPIO IS THE CHANGES FROM BETA TO PRODUCTION

GPIO BANK3

GPIO00	VCC_1V2_EN_GPIO3_0
GPIO01	HDMI_INT
GPIO02	WAKE_HOST_GPIO3_2
GPIO03	SIM_DETECT
GPIO07	**TO LOW SPEED EXPANSION CONNECTOR PIN#34**
GPIO08	CLOCK TO HIGH SPEED EXPANSION CONNECTOR
GPIO15	INPUT ETHERENT INTERRUPT
GPIO17	BT_DEV_WAKE FOR Wi-Fi+BT MODULE
GPIO22	INPUT BT_HOST_WAKE FROM Wi-Fi+BT MODULE
GPIO23	INPUT WLAN_HOST_WAKE FROM Wi-Fi+BT MODULE
GPIO24	WLREG_ON

GPIO BANK4

GPIO00	FUNCTIONAL RESET OF CELLULAR MODULE_3.3V
GPIO01	SLEEP CONTROL GPIO
GPIO02	PCIE_WAKE_LTE TO CELLULAR MODULE_3.3V
GPIO04	USB_HUB_RST_N_3V3
GPIO06	W_DISABLE_GPIO
GPIO13	OUTPUT WRITE PROTECTION TO EEPROM
GPIO14	OUTPUT ETHERNET RESET
GPIO15	RF_SW_CONTROL
GPIO16	OUTPUT USER LED1 CONTROL
GPIO17	OUTPUT Wi-Fi LED CONTROL
GPIO18	OUTPUT BLUETOOTH LED CONTROL
GPIO21	OUTPUT_USER LED4 CONTROL

GPIO BANK0

GPIO01	OUTPUT BTREG_ON TO Wi-Fi+BT MODULE
GPIO04	FAN_CONTROL_GPIO0_04
GPIO05	SW_CTRL FROM Wi-Fi+BT MODULE
GPIO06	OUTPUT_USER LED2 CONTROL
GPIO07	OUTPUT_USER LED3 CONTROL
GPIO19	**TO LOW SPEED EXPANSION CONNECTOR PIN#31**
GPIO20	**TO LOW SPEED EXPANSION CONNECTOR PIN#27**
GPIO29	**TO LOW SPEED EXPANSION CONNECTOR PIN#23**

GPIO BANK1

GPIO00	**TO LOW SPEED EXPANSION CONNECTOR PIN#29**
GPIO01	**TO LOW SPEED EXPANSION CONNECTOR PIN#33**
GPIO02	INTERRUPT FROM ACCELERO + GYRO SENSOR
GPIO03	**TO LOW SPEED EXPANSION CONNECTOR PIN#24**
GPIO07	**TO LOW SPEED EXPANSION CONNECTOR PIN#25**
GPIO13	**TO LOW SPEED EXPANSION CONNECTOR PIN#30**
GPIO14	**TO LOW SPEED EXPANSION CONNECTOR PIN#32**
GPIO27	WL_BT_GPIO1_Wi-Fi+BT MODULE
GPIO28	WL_BT_GPIO2_Wi-Fi+BT MODULE
GPIO31	**TO LOW SPEED EXPANSION CONNECTOR PIN#26**

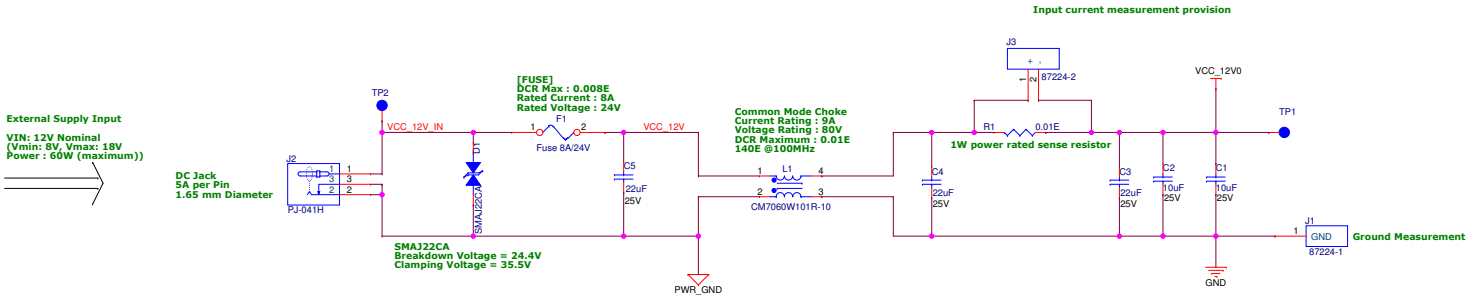
GPIO BANK2

GPIO00	**TO LOW SPEED EXPANSION CONNECTOR PIN#28**
GPIO03	OTG POWER ENABLE GPIO

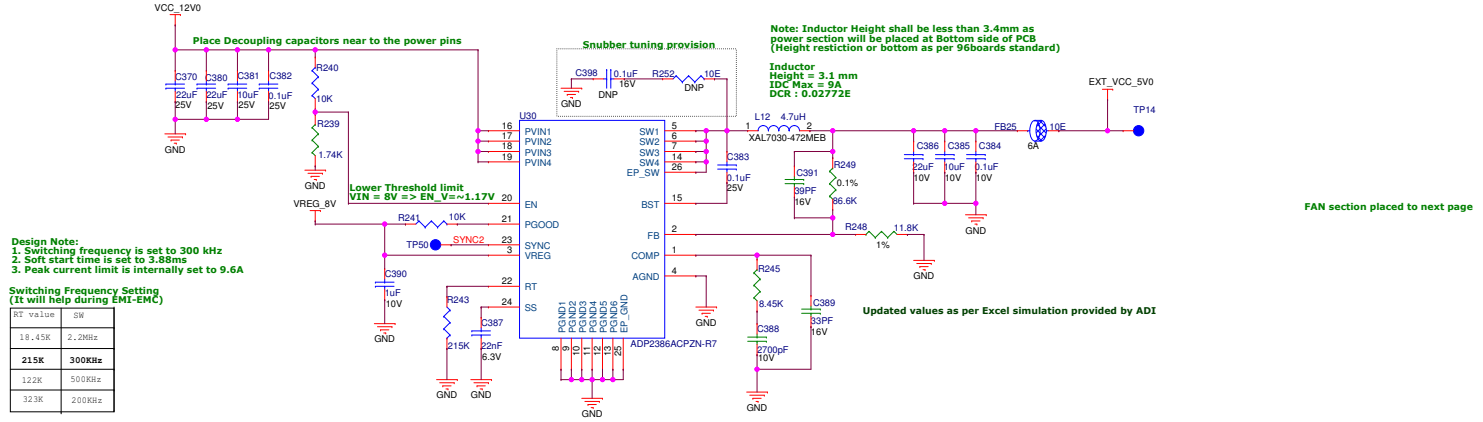
Project: Arrow_iMX8XML_RD	Designed by eInfochips	
Title: i.MX 8X GPIO TABLE 1		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
Date:Monday, April 15, 2019	Sheet 5 of 30	

INPUT POWER SUPPLY

INPUT POWER & PROTECTION CIRCUIT



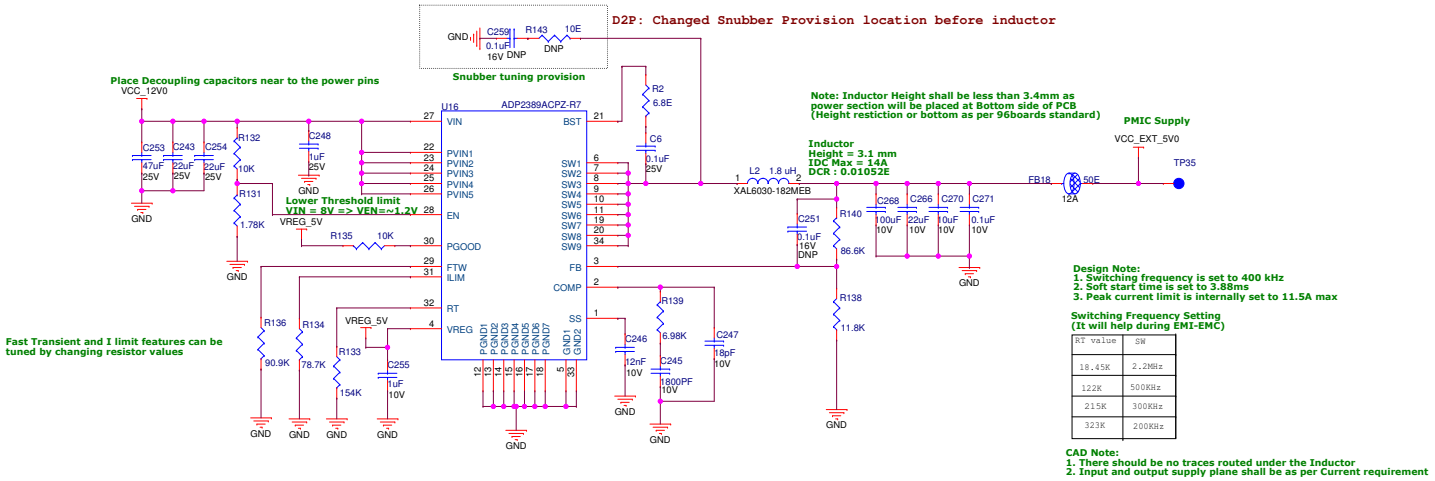
12V TO 5V @6A DC/DC CONVERTER



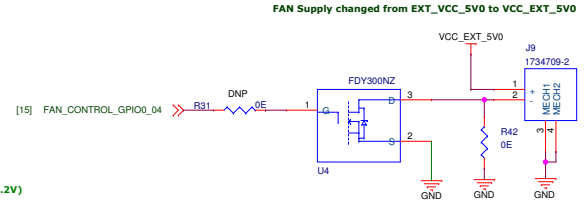
Project: Arrow_iMX8XML_RD	Designed by eInfochips	
Title: INPUT POWER SUPPLY		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
Date: Monday, April 15, 2019	Sheet 6 of 30	

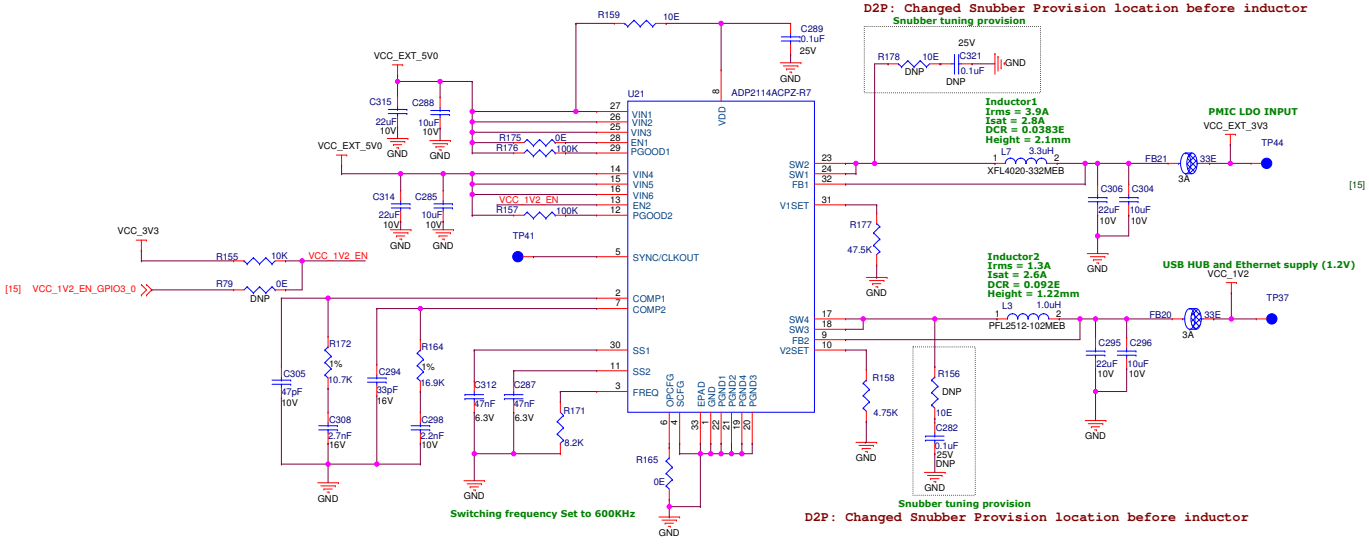
POWER REGULATORS

12V TO 5V @12A DC/DC CONVERTER



FAN CONNNECTOR





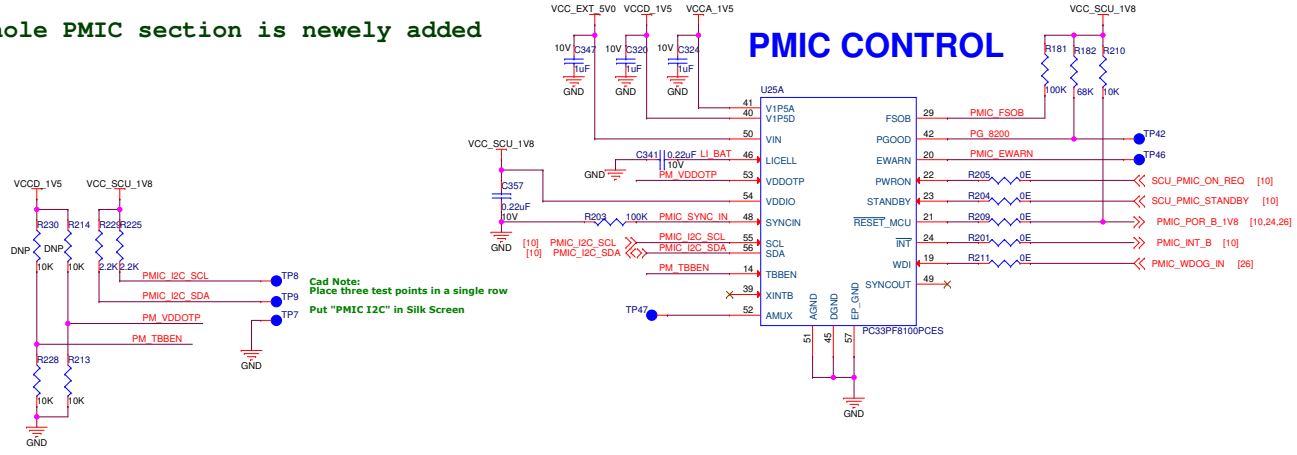
5V TO 3.3V@2A AND 1.2V@1A DUAL BUCK REGULATOR

Project: Arrow_iMX8XML_RD		Designed by eInfochips
Title: POWER REGULATORS		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
Date: Monday, April 15, 2019	Sheet 7 of 30	

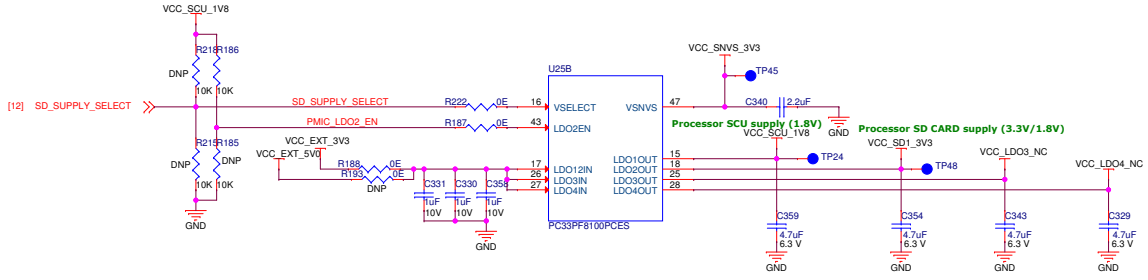
PMIC POWER SUPPLY AND LDOS

Whole PMIC section is newely added

PMIC CONTROL

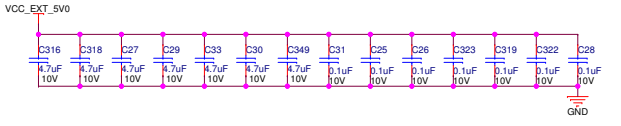


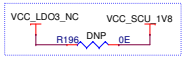
PMIC LDOs

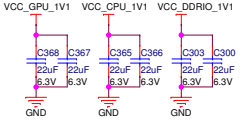


SD Supply Feedback circuit removed
SD_SELECT pin given to PMIC

CAD Note: Place decoupling capacitors near to the PMIC power pins

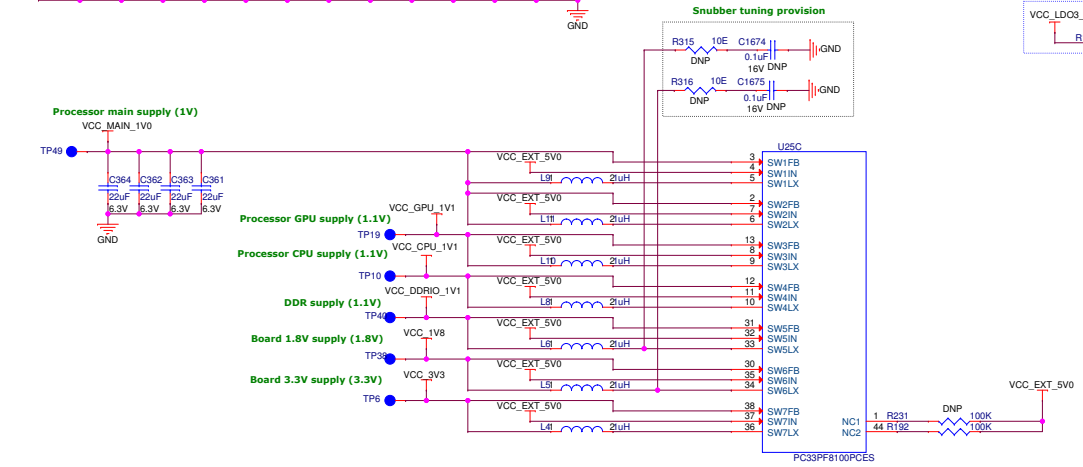






CAD Note: Place decoupling capacitors near to the PMIC power pins

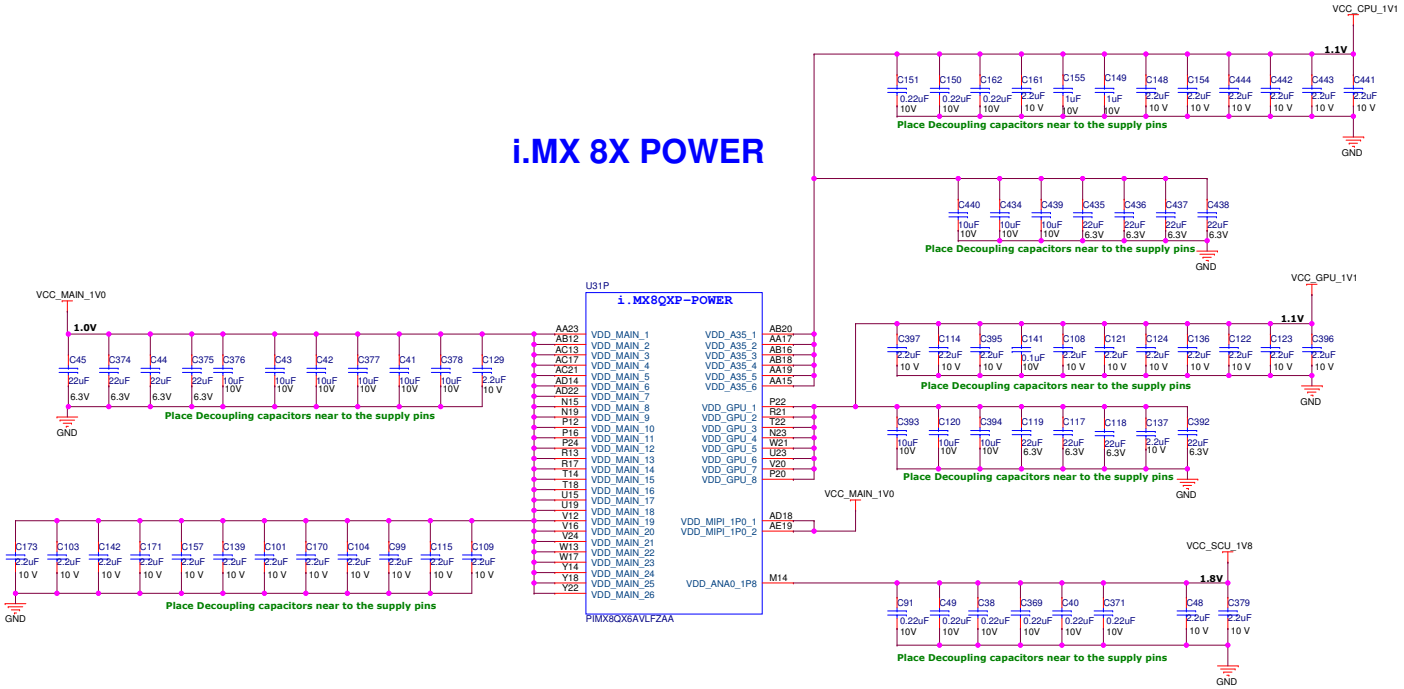
PMIC SWITCHING REGULATORS



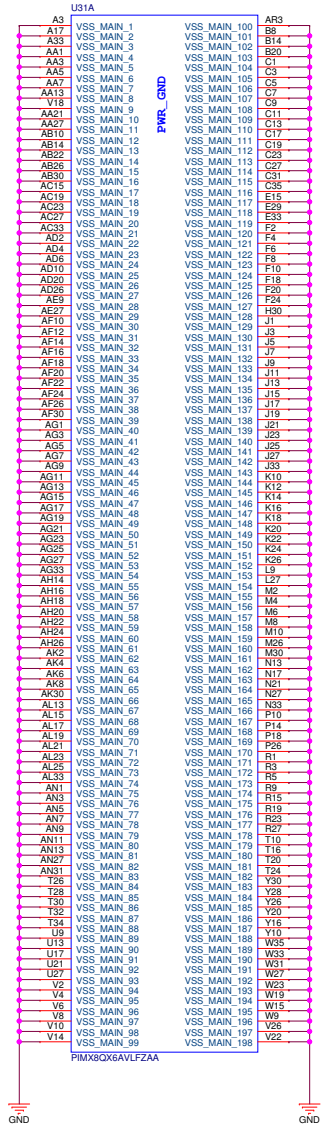
Project: Arrow_iMX8XML_RD	Designed by eInfochips	
Title: PMIC POWER SUPPLY AND LDOS		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
Date: Thursday, April 25, 2019	Sheet 8 of 30	

i.MX 8X POWER GROUND

i.MX 8X POWER

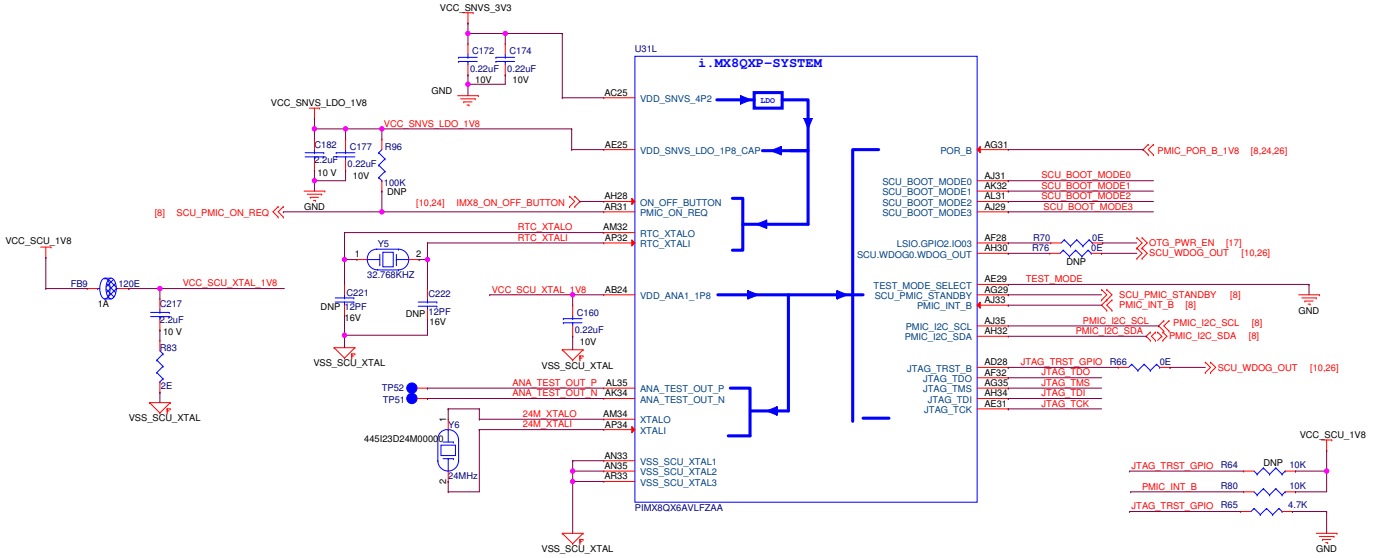


i.MX 8X GROUND



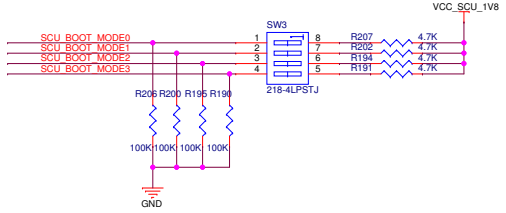
Project: Arrow_iMX8XML_RD	Designed by eInfochips	
Title: i.MX 8X POWER GROUND		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
Date: Monday, April 15, 2019	Sheet 9 of 30	

i.MX 8X CONTROL



I2C level shifter removed

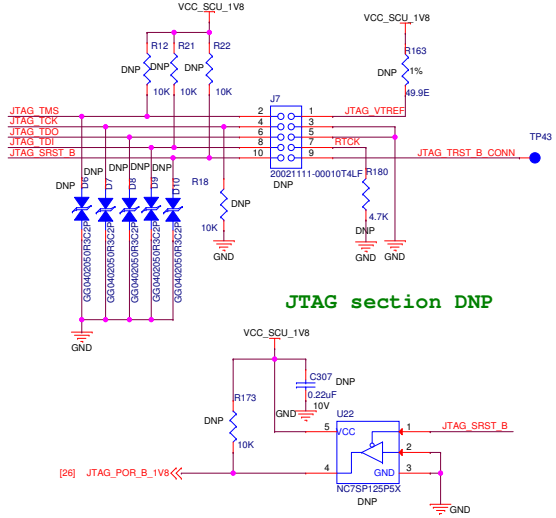
BOOT MODE SWITCH



Keep By Default SD1 boot ---------- 0 0 1 1

SCU_Boot_Mode	3	2	1	0
BOOT From Fuse -------	0	0	0	0
Serial Download ------	0	0	0	1
eMMC0 ----------------	0	0	1	0
SD1 boot -------------	0	0	1	1
NAND 8-bit 128page----	0	1	0	0
NAND 8-bit 32page-----	0	1	0	1
QSPI 3B READ ---------	0	1	1	0
QSPI Hyperflash3.3V---	0	1	1	1
SCU_PRIVATE_BOOT_I2C-	1	1	0	0
Reserved ------------	1	1	0	1
Infinite LoopMode----	1	1	1	0
TEST MODE -----------	1	1	1	1

JTAG

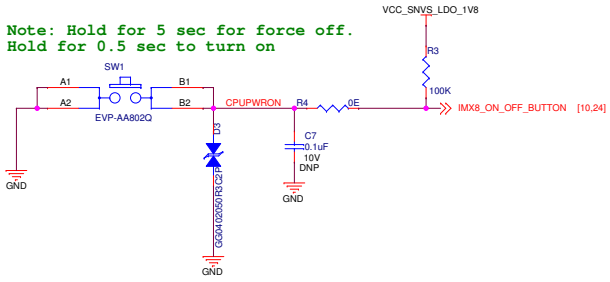


JTAG section DNP

MX8QX On-Chip 50 kohm Pulls

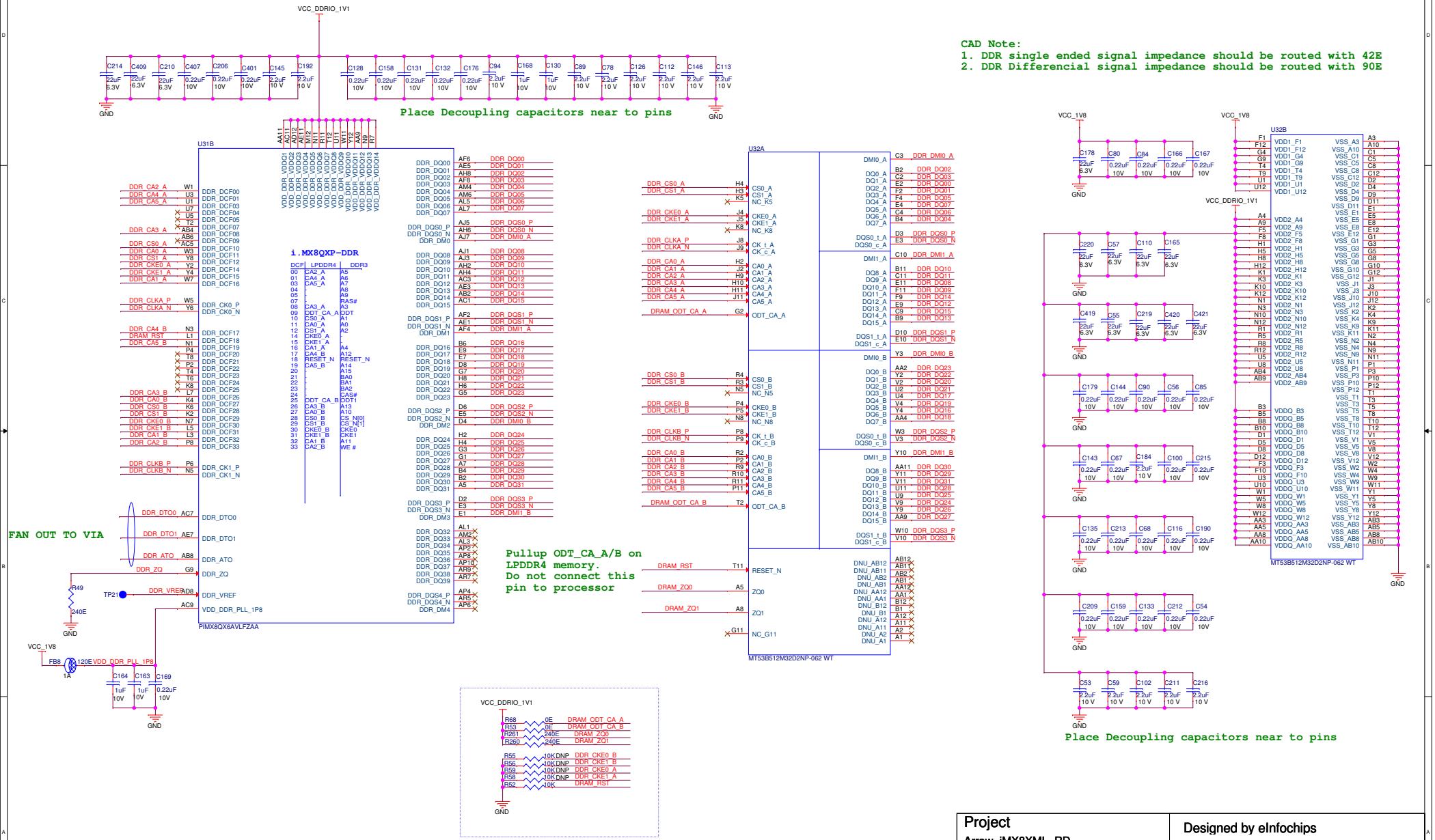
JTAG_TMS = PU
JTAG_TCK = PD
JTAG_TDI = PU
TEST_MODE_SELECT = PD

POWER ON SWITCH



Project: Arrow_iMX8XML_RD	Designed by eInfochips	
Title: i.MX 8X CONTROL		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
Date: Monday, April 15, 2019	Sheet 10 of 30	

DDR DRAM INTERFACE



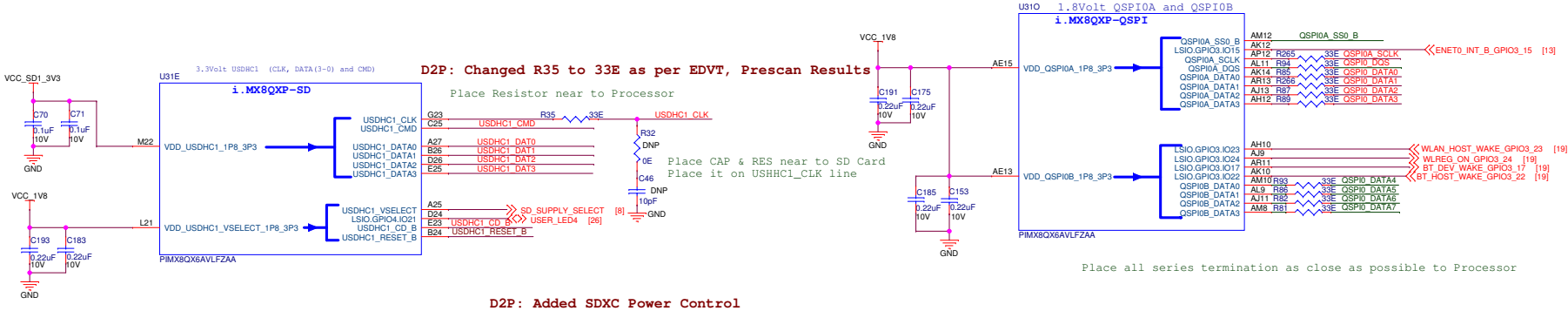
CAD Note:
1. DDR single ended signal impedance should be routed with 42E
2. DDR Differencial signal impedance should be routed with 90E

Note : LPDDR4 4GB and 2GB parts are pin to pin compatible

Project: Arrow_iMX8XML_RD	Designed by eInfochips	
Title: DDR INTERFACE		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
Date: Monday, April 15, 2019	Sheet 11 of 30	

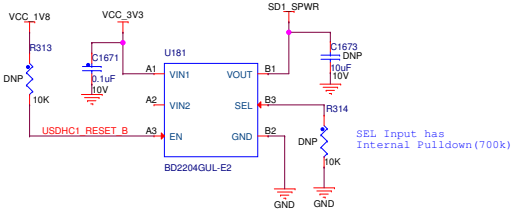
SD CARD, NOR FLASH AND EEPROM

Replaced QUAD NOR to OCTAL NOR

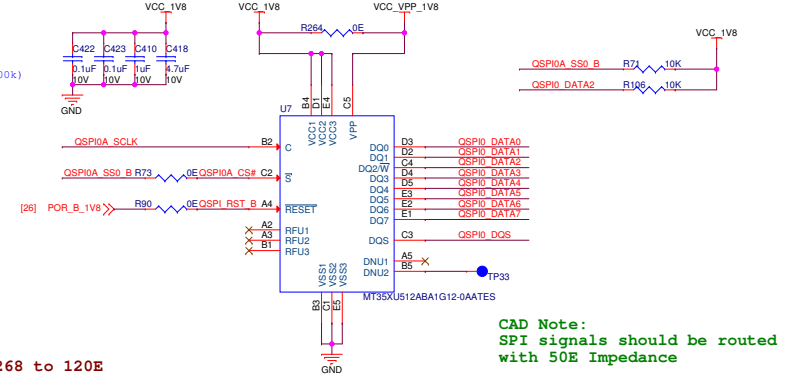


D2P: Added SDXC Power Control
Switch to support for UHS mode

SDXC Power Control



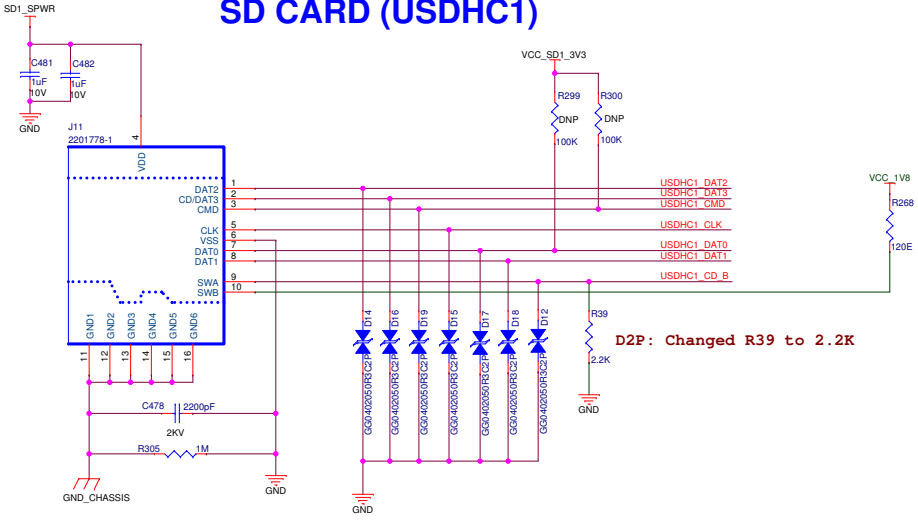
OCTAL SPI NOR FLASH



CAD Note:
SPI signals should be routed with 50E Impedance

Select Boot mode 0110 to make processor boot through QUAD SPI

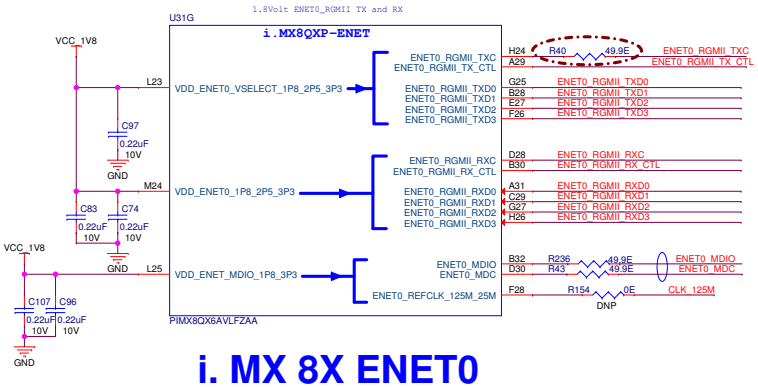
SD CARD (USDHC1)



CAD Note:
SD card signals should be routed with 50E Impedance

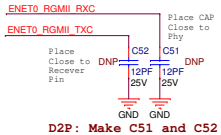
Project: Arrow_iMX8XML_RD	Designed by eInfochips	
Title: SD CARD, NOR FLASH		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
Date: Monday, April 15, 2019	Sheet 12 of 30	

i. MX 8X RGMII ENET0

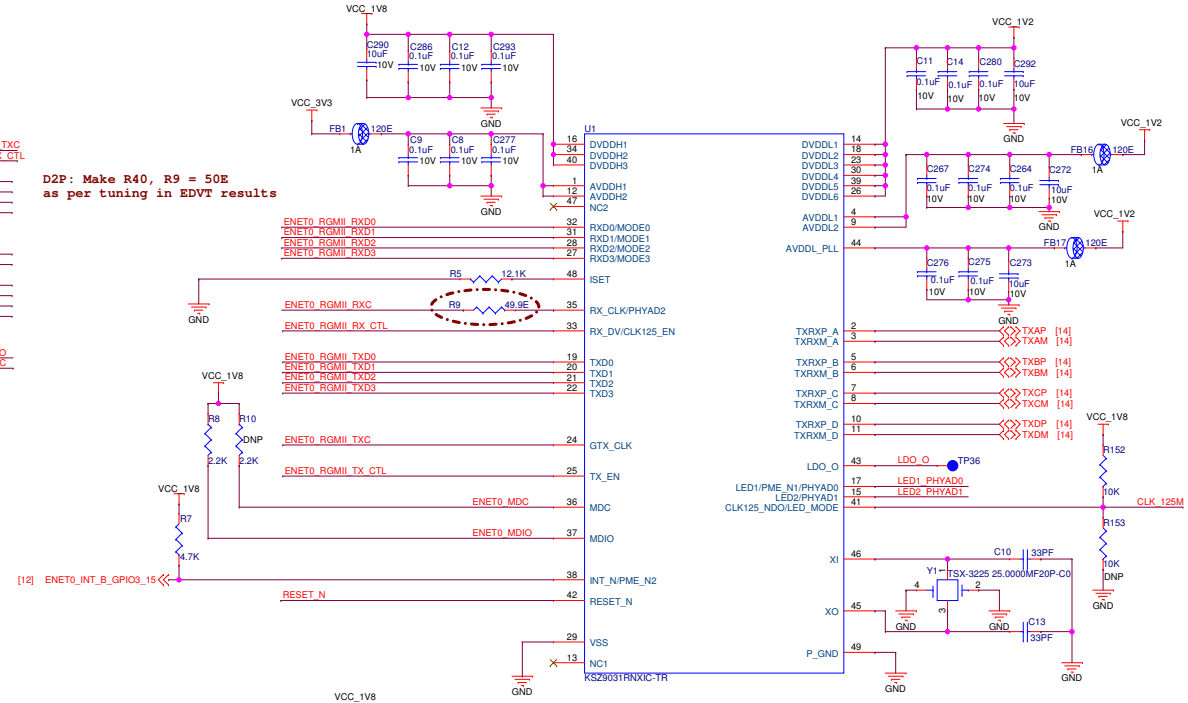


i. MX 8X ENET0

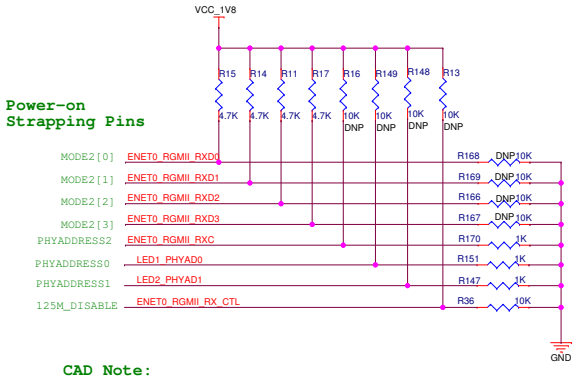
D2P: Make R40, R9 = 50E
as per tuning in EDVT results

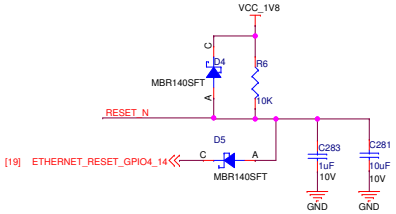


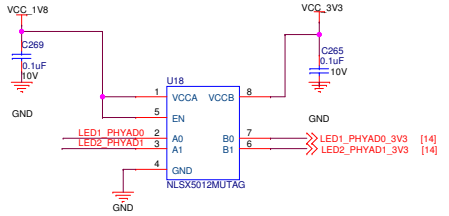
D2P: Make C51 and C52 DNP
as per EDVT results



ETHERNET PHY







CAD Note:
RGMII signals should be routed with 50E Impedance

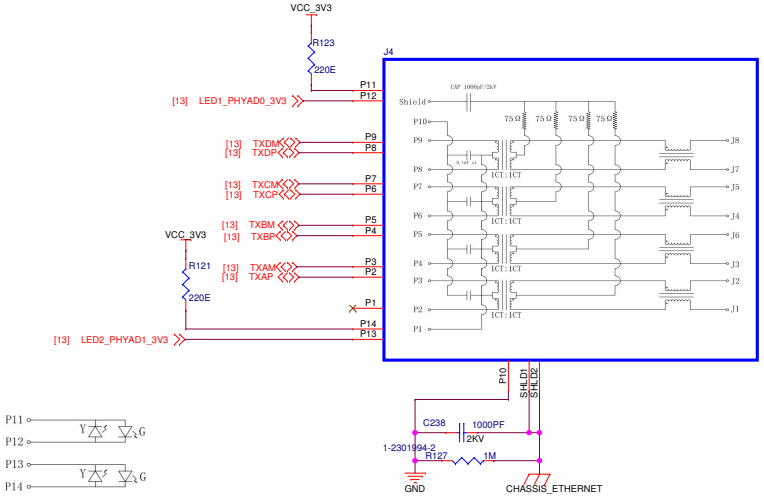
MODE2[3:0]

(Default assemble: 1111)
0100 NAND tree mode
0111 Chip power-down mode
1100 RGMII mode - Advertise 1000BASE-T full-duplex only
1101 RGMII mode - Advertise 1000BASE-T full- and halfduplex only
1110 RGMII mode - Advertise all capabilities (10/100/1000 speed half-/full-duplex), except 1000BASE-T halfduplex
1111 RGMII mode - Advertise all capabilities (10/100/1000 speed half-/full-duplex)

Others Reserved

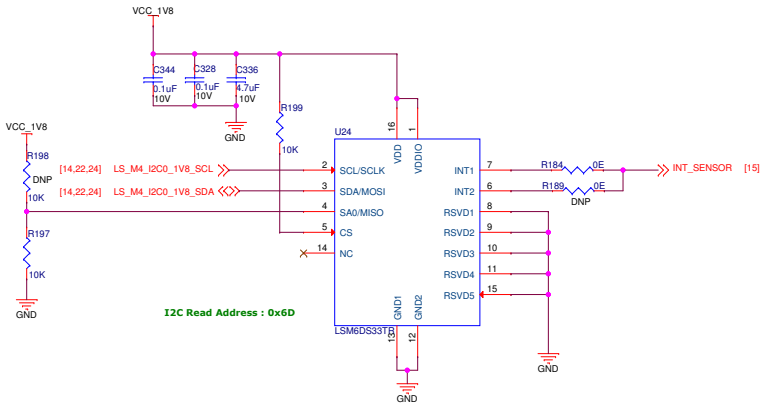
Project: Arrow_iMX8XML_RD	Designed by eInfochips	
Title: i. MX 8X RGMII ENET0		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
Date: Monday, April 15, 2019	Sheet 13 of 30	

RJ45 MAGJACK, IMU SENSOR AND SECURITY IC

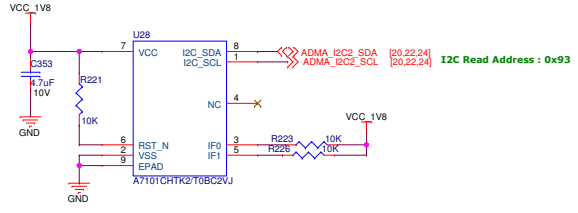


Pin	Green	Yellow	Pin	Green	Yellow
P11	+	−	P13	+	−
P12	−	+	P14	−	+

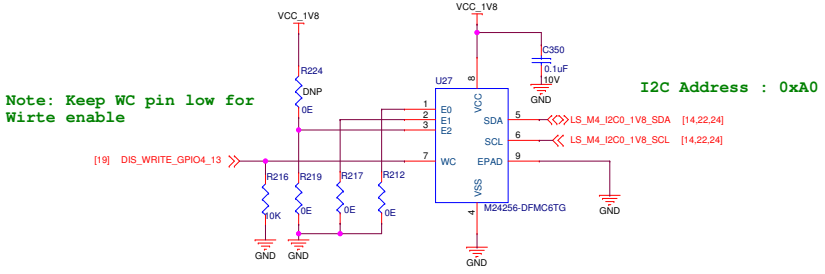
RJ45 MAG JACK



iNEMO INERTIAL MODULE



A71CH SECURE ELEMENT

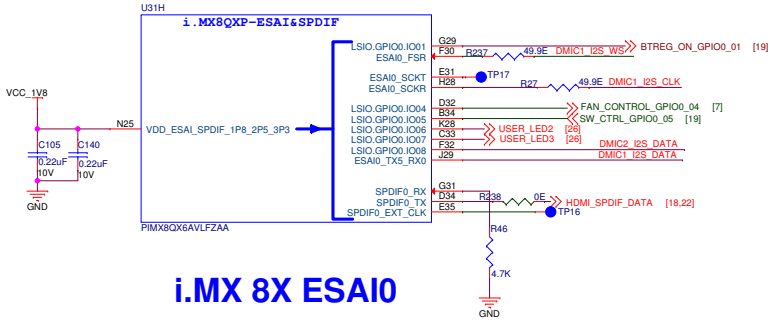


I2C EEPROM

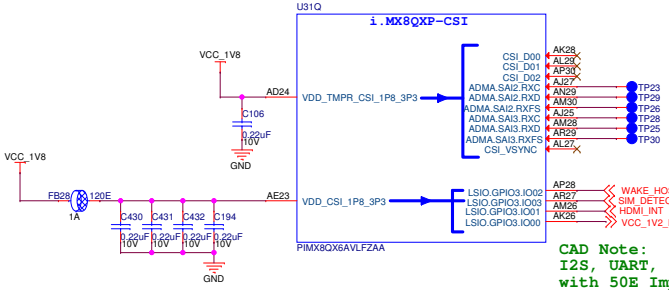
Project: Arrow_iMX8XML_RD		Designed by eInfochips
Title: RJ45 MAGJACK		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
Date: Monday, April 15, 2019	Sheet 14 of 30	

MICROPHONE INTERFACE

D2P: TP18 removed, placed BTREG_ON GPIO assigned

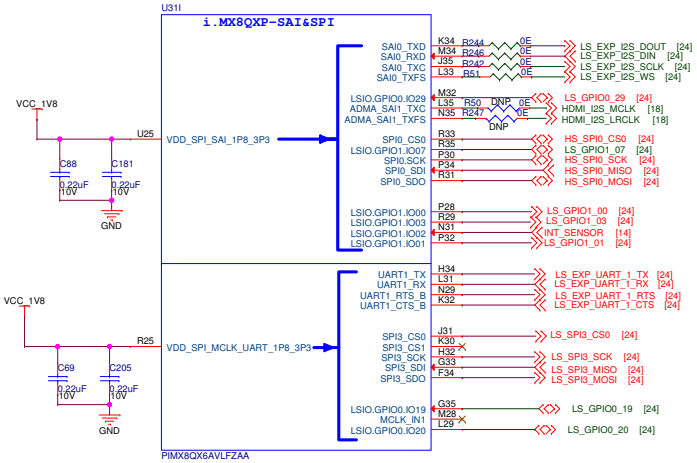


i.MX 8X ESAI0



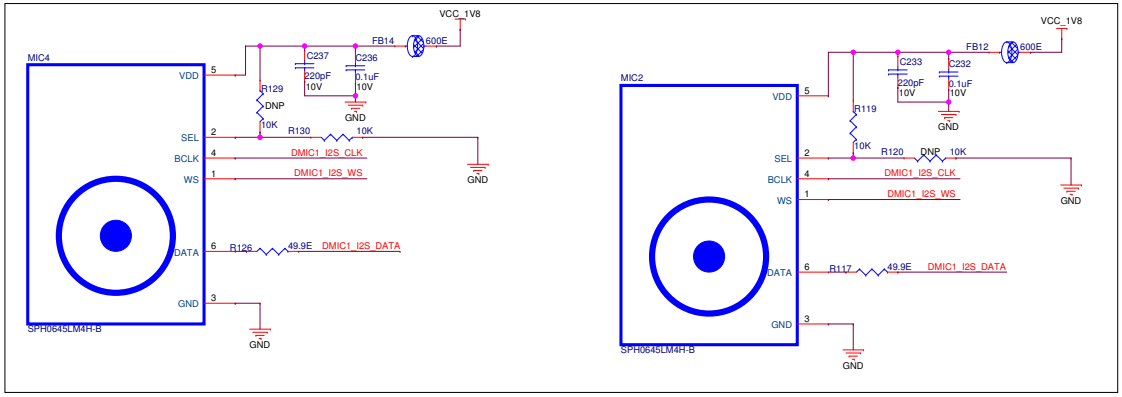
CAD Note:
I2S, UART, I2C and GPIO signals should be routed with 50E Impedance

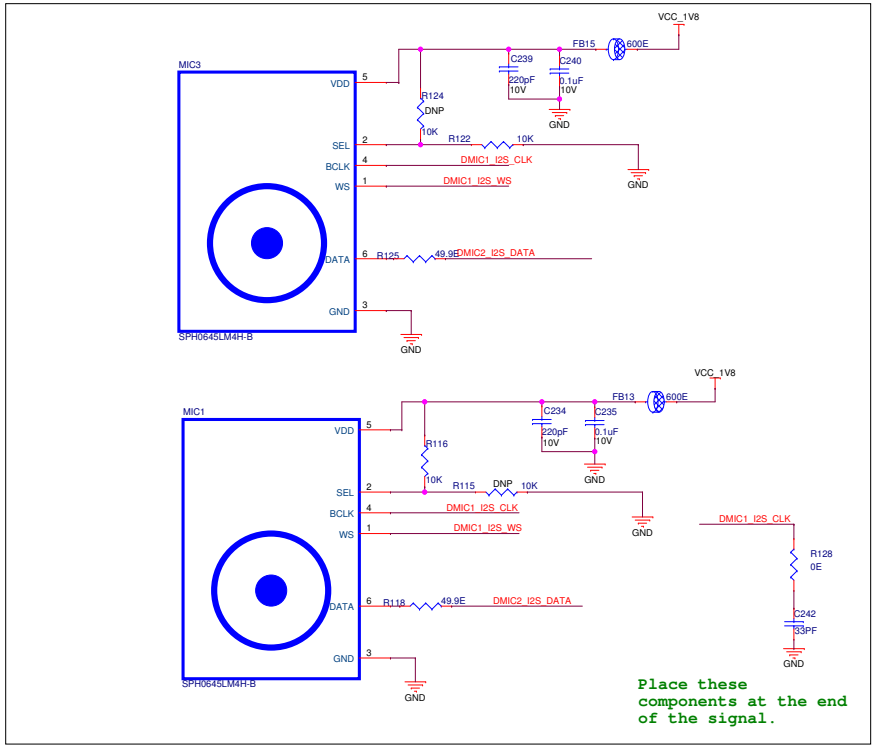
i.MX 8X SAI2, SAI3



i.MX 8X SAI0, SPI1, SPI3, UART1 and GPIO

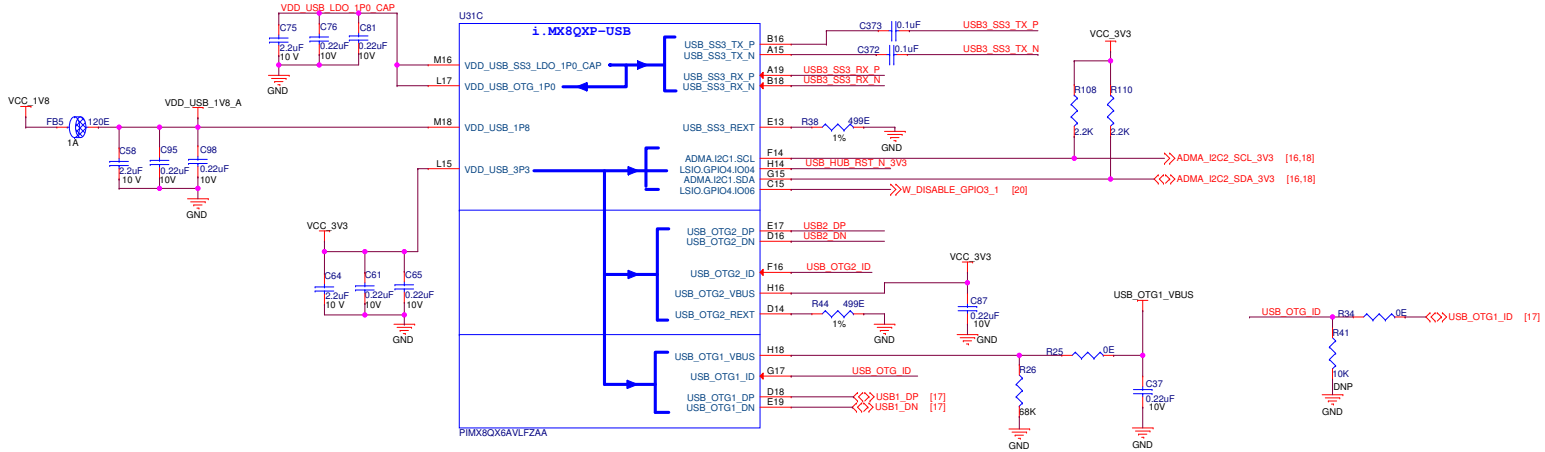
MEMS I2S MICROPHONES



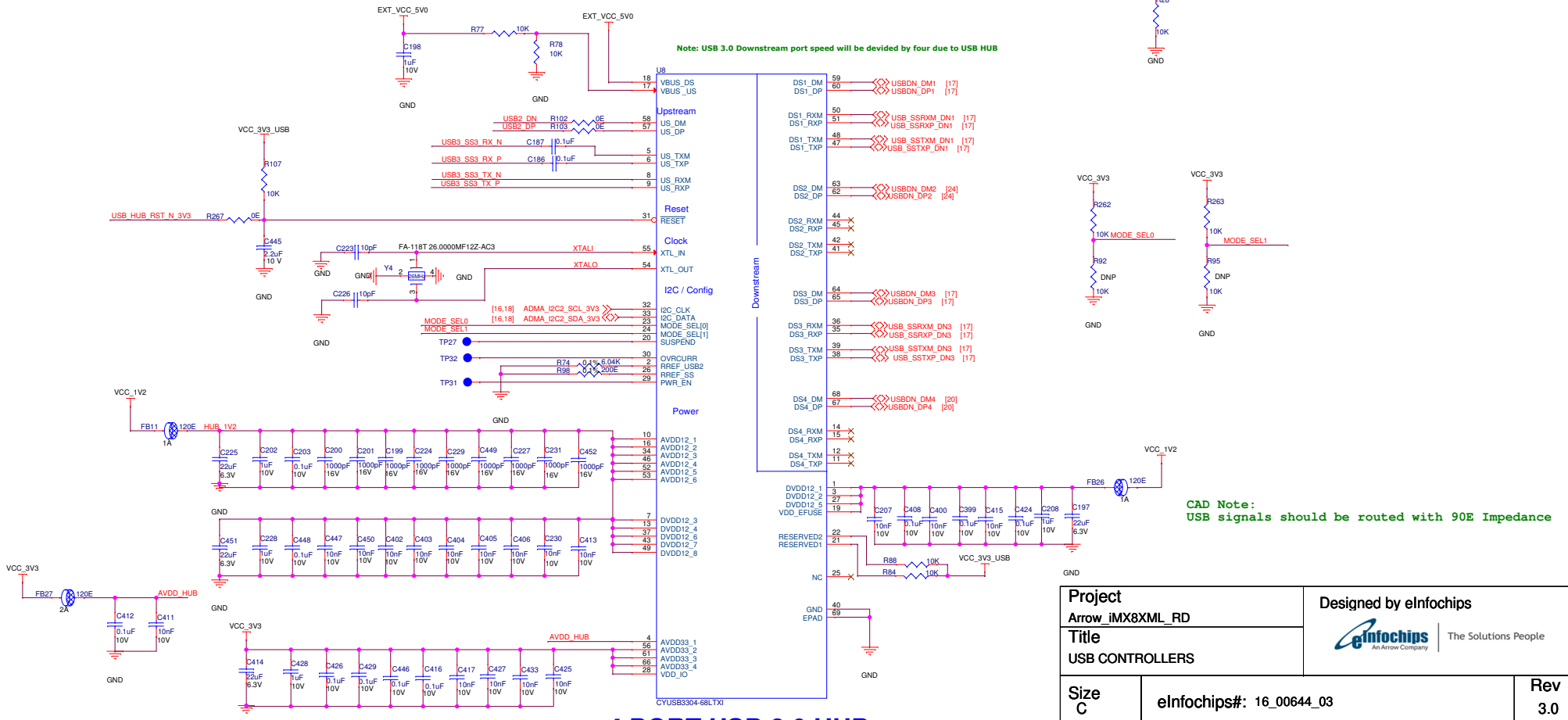


Project: Arrow_iMX8XML_RD	Designed by eInfochips	
Title: MICROPHONE INTERFACE		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
Date: Monday, April 15, 2019	Sheet 15 of 30	

USB CONTROLLERS



i.MX 8X USB PORTS

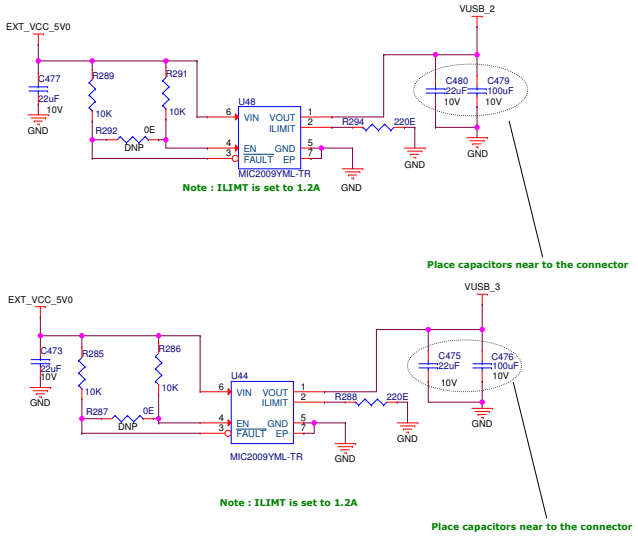


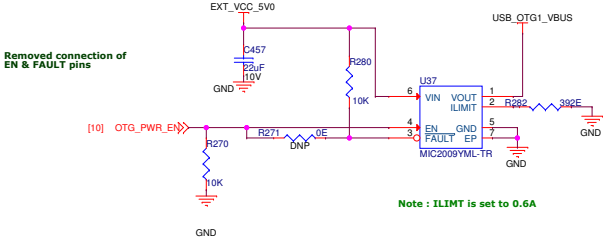
4 PORT USB 3.0 HUB

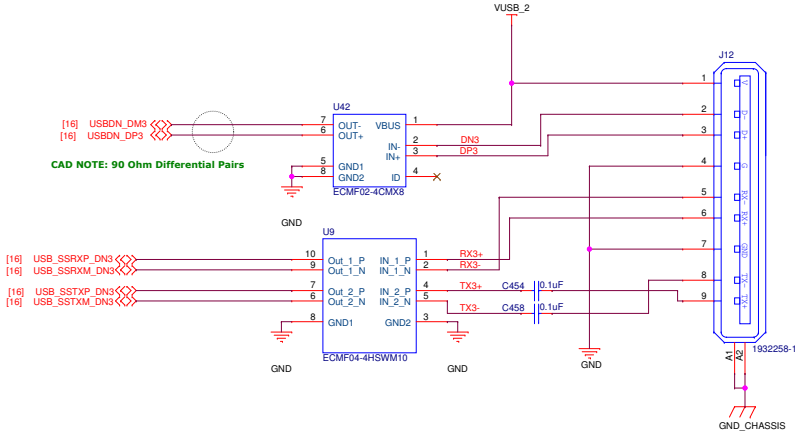
CAD Note:
USB signals should be routed with 90E Impedance

Project: Arrow_iMX8XML_RD	Designed by eInfochips	
Title: USB CONTROLLERS		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
Date: Monday, April 15, 2019	Sheet 16 of 30	

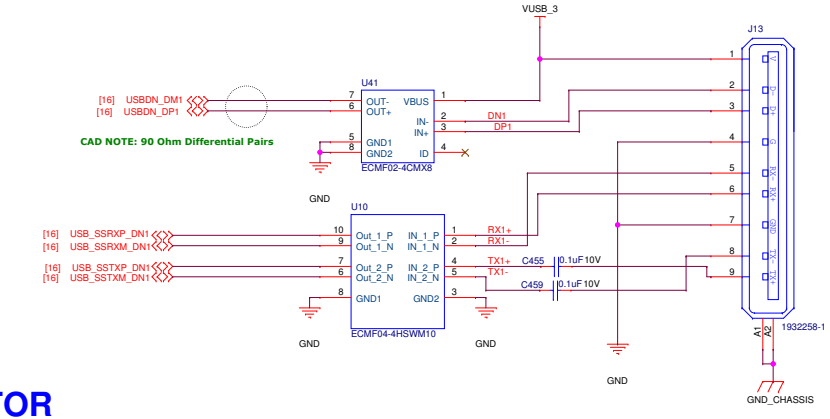
USB CONNECTORS



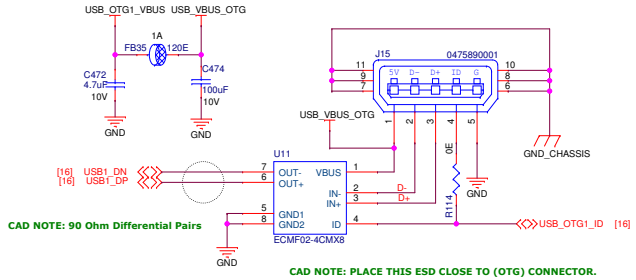




CAD Note:
USB signals should be routed with 90E Impedance



USB 2.0 MICRO-AB OTG CONNECTOR

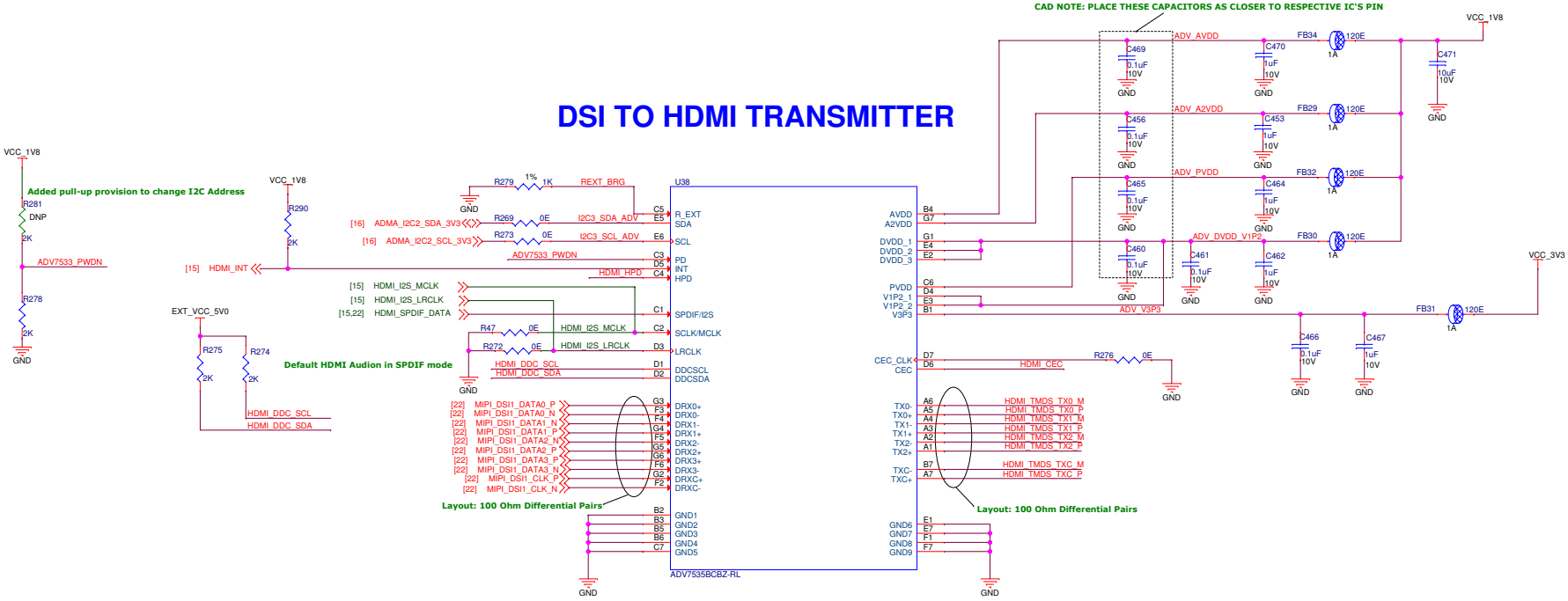


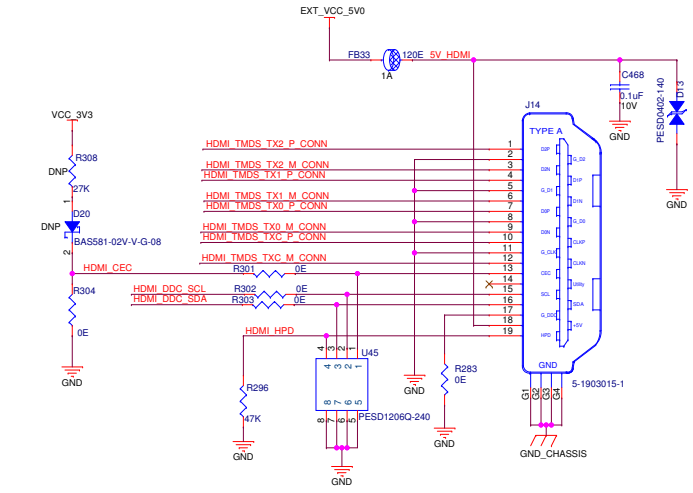
USB 3.0 TYPE A CONNECTORS

Project: Arrow_iMX8XML_RD	Designed by eInfochips	
Title: USB CONNECTORS		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
Date: Monday, April 15, 2019	Sheet 17 of 30	

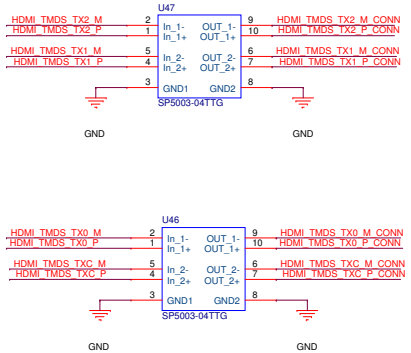
DSI TO HDMI CONVERSION

DSI TO HDMI TRANSMITTER



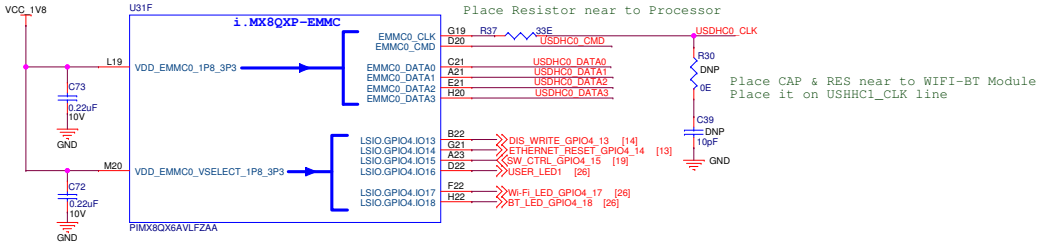


HDMI TYPE A CONNECTOR

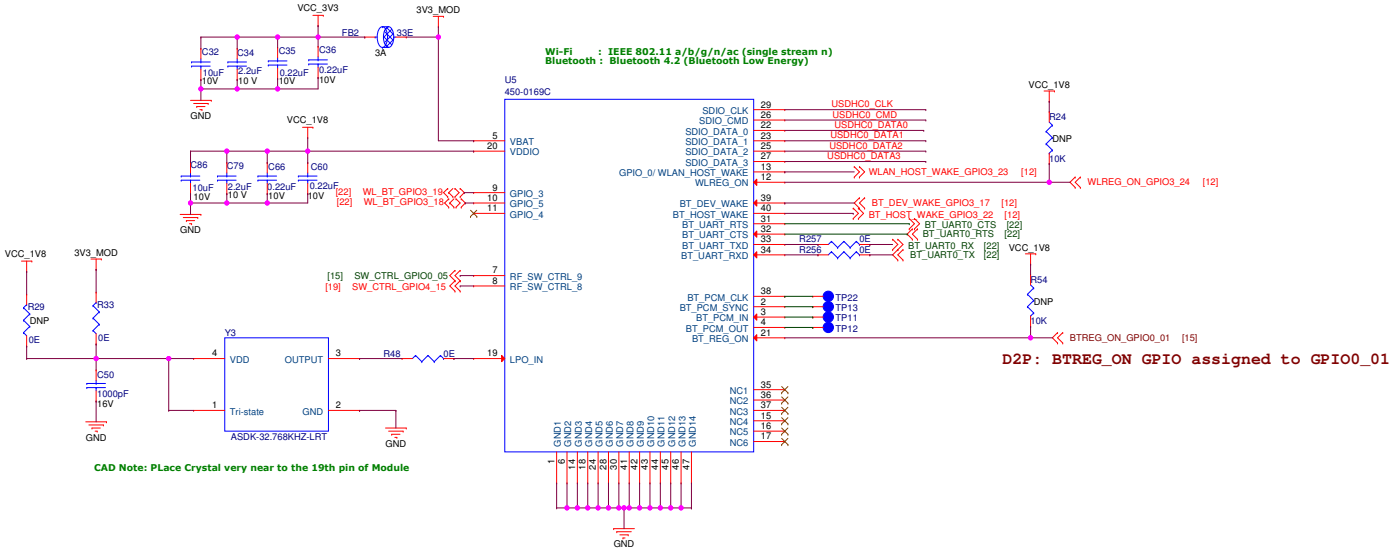


Project: Arrow_iMX8XML_RD	Designed by eInfochips	
Title: DSI TO HDMI CONVERSION		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
Date: Monday, April 15, 2019	Sheet 18 of 30	

Wi-Fi BLUETOOTH INTERFACE



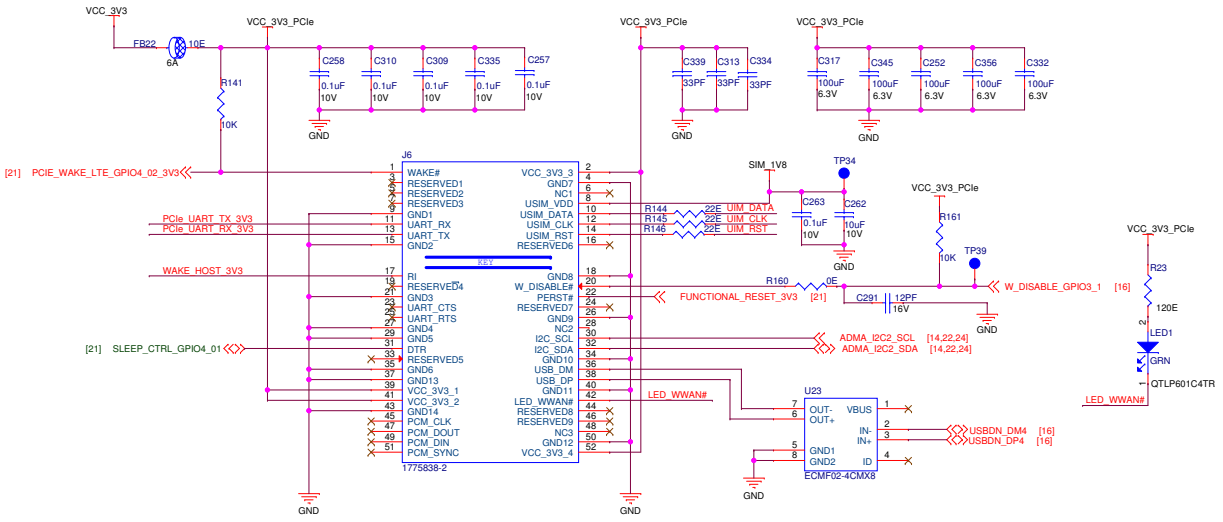
USDHC0 SDIO PORT



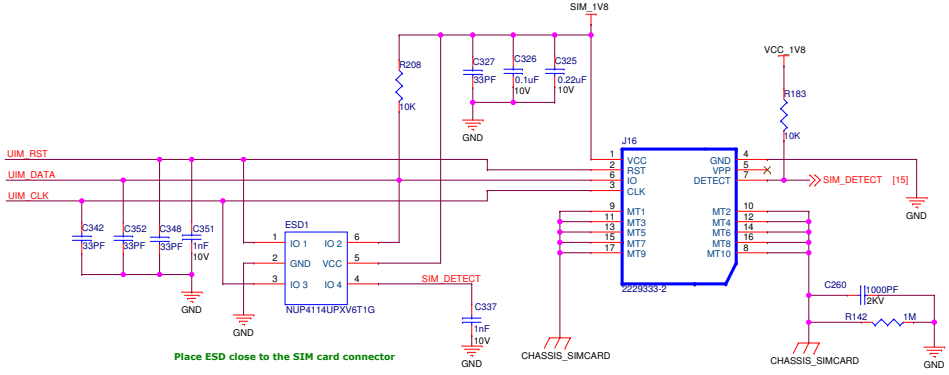
Wi-Fi + BT MODULE

Project: Arrow_iMX8XML_RD		Designed by eInfochips
Title: Wi-Fi BLUETOOTH INTERFACE		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
Date: Monday, April 15, 2019	Sheet 19 of 30	

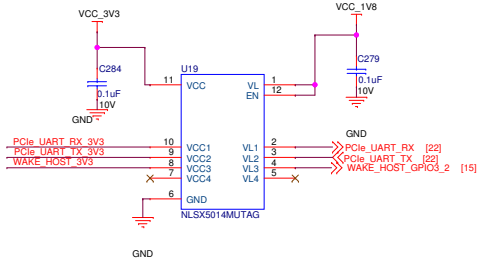
LTE MODULE INTERFACE



QUECTEL EC25 mini PCIE



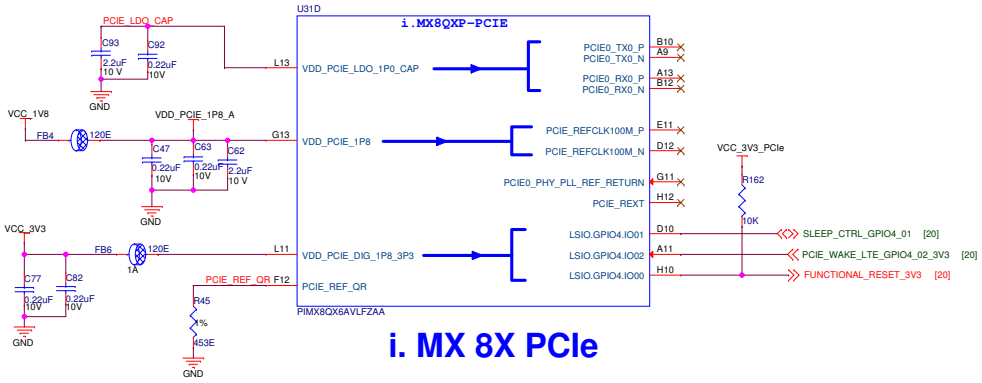
MICRO SIM CARD CONNECTOR



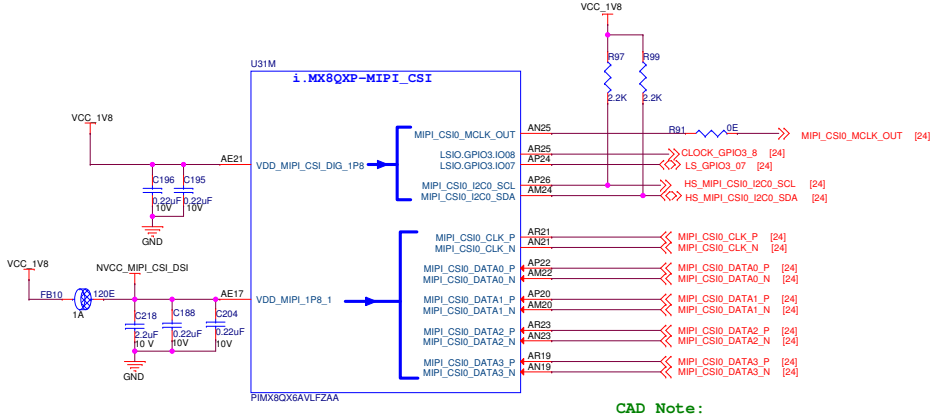
VOLTAGE LEVEL TRANSLATOR

Project: Arrow_iMX8XML_RD	Designed by eInfochips	
Title: LTE MODULE INTERFACE		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
Date: Monday, April 15, 2019	Sheet 20 of 30	

i.MX 8X PCIe, MIPI CSI



i. MX 8X PCIe

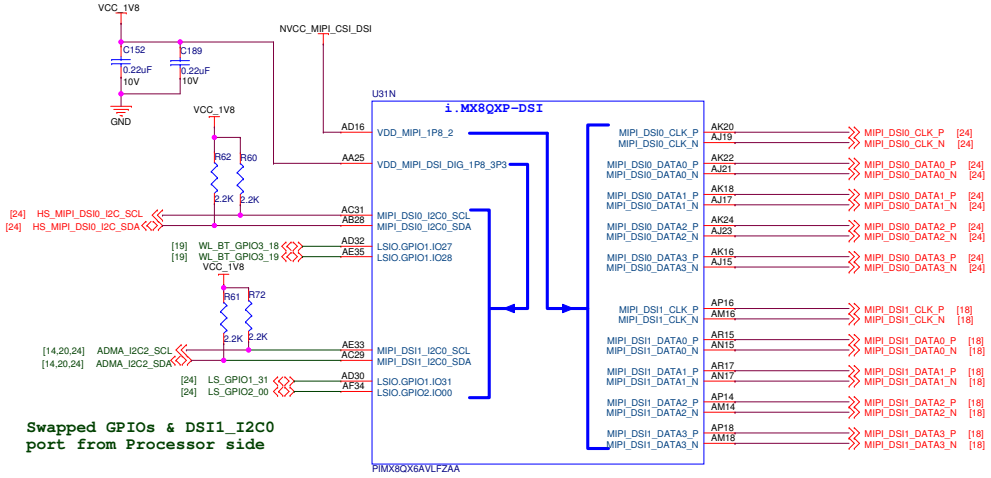


CAD Note:
MIPI CSI signals should be routed with 100E Impedance

i. MX 8X MIPI CSI

Project: Arrow_iMX8XML_RD	Designed by eInfochips	
Title: i.MX 8X PCIe, MIPI CSI		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
Date: Monday, April 15, 2019	Sheet 21 of 30	

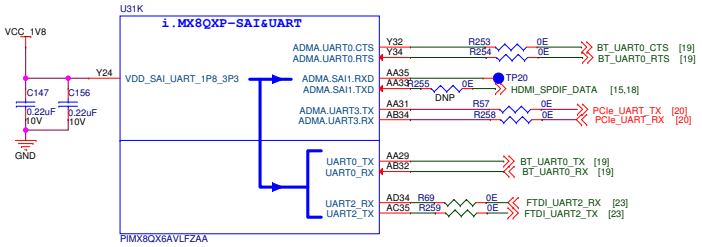
i. MX 8X MIPI DSI, SAI, UART



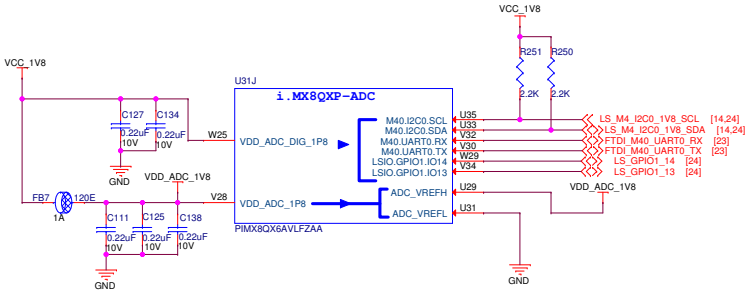
CAD Note:
MIPI DSI signals should be routed with 100E Impedance

Add Test points for via opening for all MIPI signals

i. MX 8X MIPI DSI



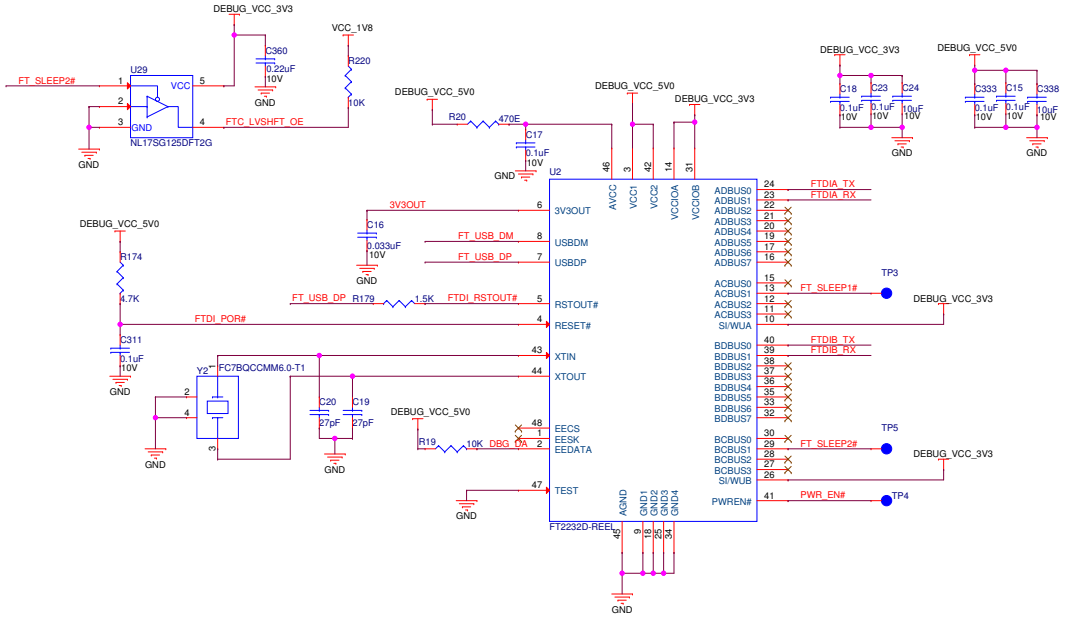
i. MX 8X SAI1, UART



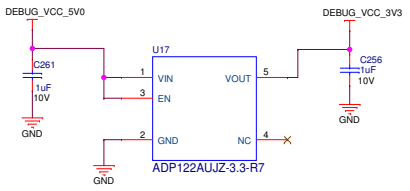
i. MX 8X GPIOs, UART

Project: Arrow_iMX8XML_RD		Designed by eInfochips
Title: i. MX 8X MIPI DSI, SAI, UART		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
Date: Monday, April 15, 2019	Sheet 22 of 30	

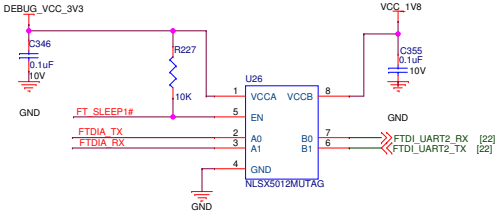
DEBUG UART AND USB

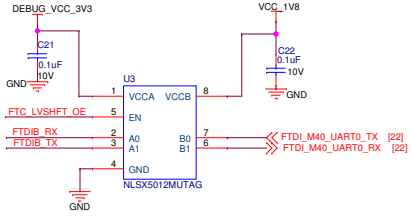


UART TO USB CONVERTER

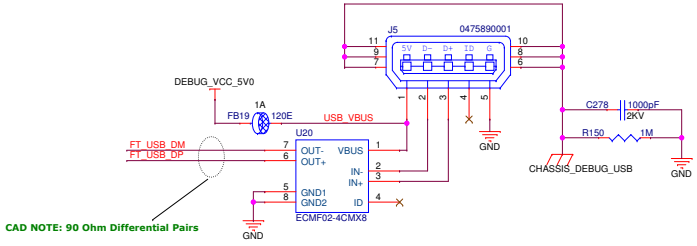


DEBUG 3.3V SUPPLY





UART VOLTAGE LEVEL TRANSLATORS

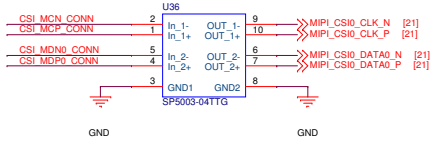


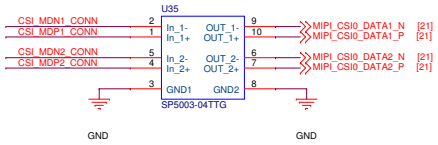
CAD NOTE: PLACE THIS ESD CLOSE TO USB CONNECTOR.

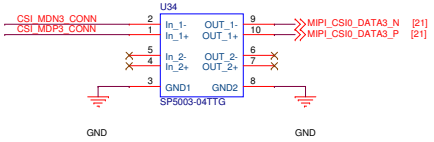
DEBUG USB CONNECTOR

Project: Arrow_iMX8XML_RD		Designed by eInfochips
Title: DEBUG UART AND USB		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
Date: Monday, April 15, 2019	Sheet 23 of 30	

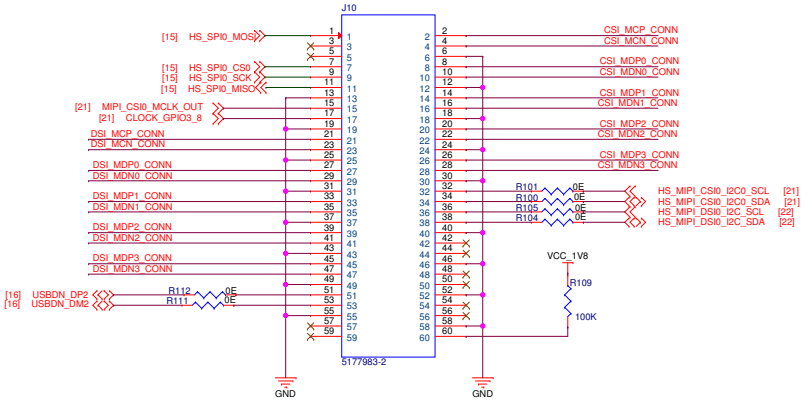
EXPANSION CONNECTORS



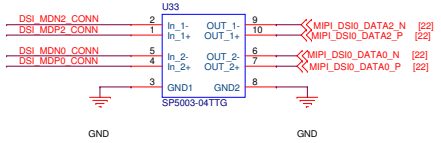


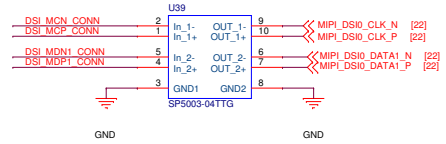


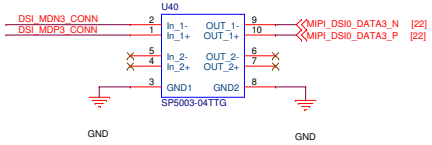
CSI0 EMI+ESD



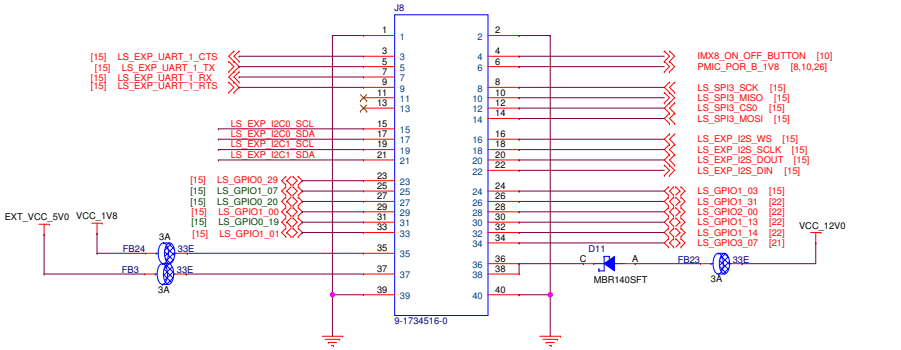
HIGH SPEED EXPANSION CONNECTOR







DSI0 EMI+ESD



LOW SPEED EXPANSION CONNECTOR

Project: Arrow_iMX8XML_RD	Designed by eInfochips	
Title: EXPANSION CONNECTORS		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
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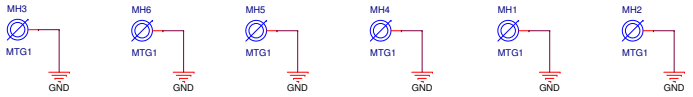
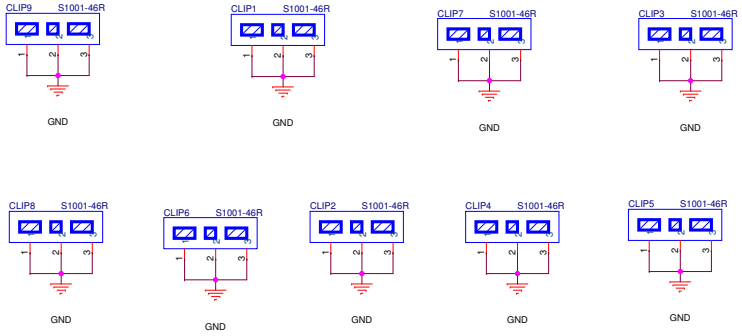
MISCELLANEOUS

MOUNTING HOLES



SHIELD CLIPS



Project: Arrow_iMX8XML_RD	Designed by eInfochips	
Title: MISCELLANEOUS		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
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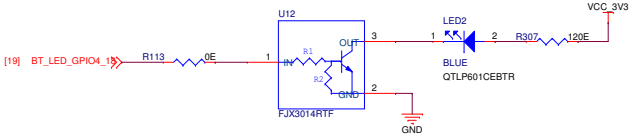
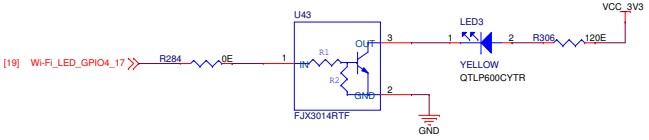
RESET SCHEME AND LEDs

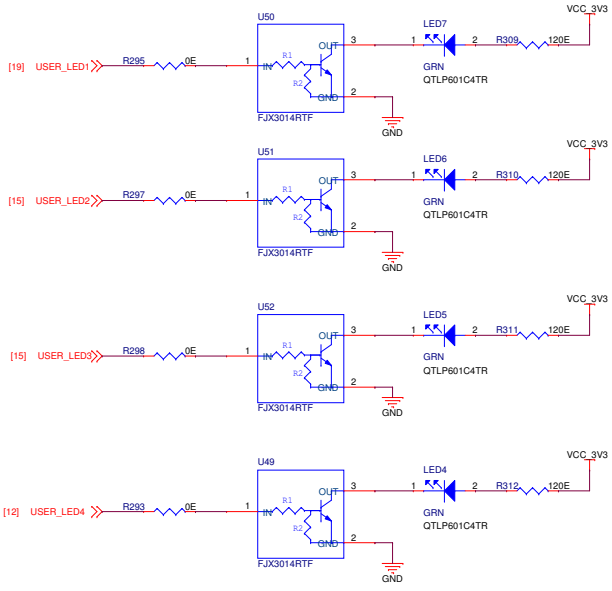
BLUE LED



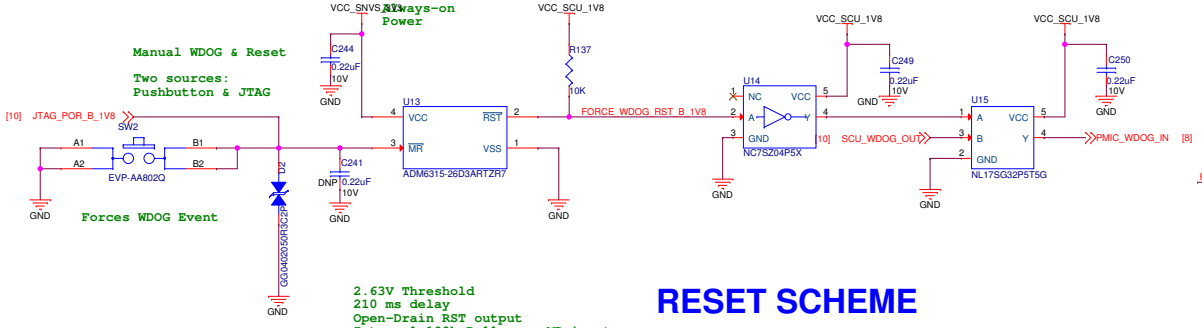
YELLOW LED



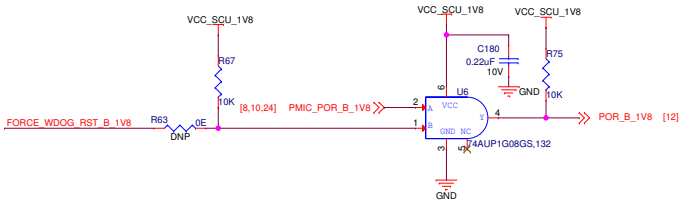
4X GREEN LEDs



RESET SCHEME



SPI-NOR RESET



Project: Arrow_iMX8XML_RD	Designed by eInfochips	
Title: RESET Scheme and LEDs		
Size: C	eInfochips#: 16_00644_03	Rev: 3.0
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RIVISION HISTORY 1

PCB REV	SCH REV	CHANGE DESCRIPTION	DATE	AUTHOR
1.0	0.1	Initial draft version created for internal review	19/07/2018	eInfochips
	0.2	DRC error generated and corrected Net name duplication removed TVS diode added at Swtich-3 for protection Series termination provision added on clock signals Pull up provision removed for SD card signals 2.2K pull up replaced for all I2C going to expansion connector Voltage input changed to 1.8V for Ethernet section of processor Pull up provision removed for SD card signals Block diagram replaced with version 0.7 PMIC replaced with tow LTM4643 devices ADM1266 power sequencer and monitor added Power supply rail name changed at entire design as per new power scheme USB 3.0 HUB replaced with Cypress part CYUSB3304-68LTXI SPI is replaced with I2C for USB HUB and I2C table updated accordingly GPIO4_0 used for communication between processor and ADM1266 Arrow Approved Power Scheme added DSI to HDMI chip is replaced with LVDS to HDMI chip so that blind burried vias will not be required in layout Processor symbol updated with LVDS instead of DSI port Review comment number 80 to 128 of Design review tracker implemented Reverse protection diode for 12V mezzanine supply added 27MHz crystal added for LVDS to HDMI converter Level translator added for communication between processor and ADM1266	01/08/2018	eInfochips
	0.3	R7696 pull down added at HPD pin of HDMI USB_OTG2_ID pin grounded as per unused pin recommendation from processor Hardware guideline PMIC_POR_B_3V3 added at U241 and ON_OFF_SWITCH_3V3 provided to directly at the gate of U238 C7875 is made DNP and will be mounted if any issue in programming of ADM1266 R7698 and R7699 added at processor side ADM_I2C As per Linaro comment, ADM_I2C pull up supply changed to AVDD_CAP instead of VCC_SCU_1V8 Pull up supply for U240 and U241 changed to AVDD_CAP Pull up provision and series resistor at enable pin location shifted near switcher As per ADI comment, C1792 value changed to 2.2pF instead of 2.2nF As per ADI comment, C7931 updated to 10uF and C7988 0.1uF added As per ADI comment, R7630 and R7634 swapped As per ADI comment, 100pF capacitors added between output and FB pin of LTM4643 As per ADI comment, Supply rail use case note added Test point TP111 for ground added and voltage level added in power net names R7588 mounted for POR, R7700 provision added	03/08/2018	eInfochips

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RIVISION HISTORY 2

PCB REV	SCH REV	CHANGE DESCRIPTION	DATE	AUTHOR
1.0	0.4	Debug LED indication from page 25 removed (D10,D11,D28,D29) Cover page modified for revision and I2C table updated with part name instead of part number At GPIO table, GPIO with 3.3V level highlighted in Bold text Mode pin pull down provision added at U227 and U228 C9796 added for more filtering and proper current sensing U16 and U243 added for I2C level translator ESD added on JTAG connector and U227, U228, U203, U229 symbol updated Net name updated for CSI signals at page 24 10K Pull up added at ADMA_I2C2_SCL_3V3, Duplicate pull up at ADMA_I2C2_SCL removed L11 power changed to 3.3V for GPIO, one level translator from page 8 removed Security IC U244 added, I2C table updated accordingly As per 96boards recommendation, FAN connector J5018 added Six mounting holes added instead of four GPIO location updated at processor pin no D10,H10 and A11 ADI comments(8 August) implemented, Level translators updated with new parts Cypress Comments (9 August) implemented - Decoupling cap added and crystal changed FB1712 removed as not required As per ADI comment, Inductor L34 value and related component values are changed	13/08/2018	eInfochips
	0.5	Cypress Review comment(14Aug) implemented, GPIO table updated Chassis ground seperated for each Metal connector, FAN connector part changed and MOSFET added ADP2386 regulator updated as per desing fille calculator provided by ADI I2C level translator and GPIO level tranlator removed and 3.3V level signals from porcessor used ITE comments for LVDS to HDMI section implemented, J5.11 and J5.13 UART removed ADP2386 ground separated for AGND and DGND as per ADI comment, 12pF at Y6 added' SW_CTRL_GPIO4_15 added at page number 20 for firmware control, ETH LED indication logic changed GPIO3_08 used for extra clock on high speed connector, U13.p1 pin maded NC DSI to HDMI chip replaced at LVDS to HDMI section, More capacitors at DMIC supply added at page 16 VDD_A35 and VDD_GPU decoupling cap added as per MEK design, USB Mirco-AB connector part changed R249 made DNP, Crystal Y7 added and CTS of module is grounded as per LSR comment Connector J13 part number and symbol updated, R7795 added, J1001 part number changed USB port connection swapped for easy layout, shield clips added, OTG power added through Q18 and Q19 One more DMIC added at ESAI port as SAI2 and SAI3 ports is not confirmed for clock generation	20/09/2018	eInfochips
	0.6	U40 part changed, All DMIC connection changed to ESAI port, Shield clip10,12 and 14 removed R317 and R318 position changed, R327 and TP42 added, 33pF added on SIM lines,U11 symbol changed USB Switch protection provision from HUB added, J17,U47,U54 symbol updated, SS cap location changed Grounding scheme at ADP5023 and LTM4643 changed, R325,R326 added, U40 nets changed, R187 mounted R100,R198,R199,R202,R203 value changed, DSI0 ESD connection changed, EMI filter on HDMI added	04/10/2018	eInfochips
	1.0	Gerber released to the fabricator	04/10/2018	eInfochips

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RIVISION HISTORY 3

PCB REV	SCH REV	CHANGE DESCRIPTION	DATE	AUTHOR
2.0	2.0	USB HUB resistor R24 made DNP and R148 mounted SD Card Detection logic corrected, Pulled down CD pin and Pulled up SWB FAN Drain and Source pin swaped MIC signal DMIC1_I2S_WS swapped to FSR of processor, TP49 added for FST Added PMIC in schematic. Level translators, ON/OFF Transistor (U55) & associated resistors removed Replaced QUAD NOR to OCTAL NOR and corrected Processor side pins nets to get Data4 to Data7 lines Removed SD_SELECT MOSFET due to addition of PMIC Assigned new location to 5 GPIOs Added 12 to 5V and 5V to 1.2V,3.3V Power converter section Updated GPIO details in Processor Symbol and match with the net name Make JTAG to be DNP Updated necessary correction for UART, Assigned full UART to BT. USB ILIMIT: R125, R128 removed, added Pull-ups to /FAULT pins I2S interface provision added for HDMI Audio EN & FAULT connection is removed for OTG ILIMIT IC GPIO tables are updated Removed R3588, R3587 & R129 pull-ups of USB ILIMIT USB_FAULT Used 0603 package resistors for R355 and R356, Removed R37, C33, R117 Changed R32 package from 0201 to 0402	20/12/2018	eInfochips
		Placed capacitors at SDIO clock of WIFI-BT & SD Card Added 50 Ohm series termination for Ethernet MDC/MDIO signals	08/01/2019	eInfochips
		R3584 changed to 100K & R74 changed to 4.7K FAN Supply changed from EXT_VCC_5V0 to VCC_EXT_5V0 and placed FAN to next page Changed USB OTG shield name Removed connection between USBHUB & ILIMIT ICs & assigned TPs at Hub side Removed senseing signals form USB ILIMIT & pulled /FAULT up. EN connected directly to 5V Changes from Alpha to Beta are highlighted with Green color in GPIO table Value changed for R297 to have correct input low voltage limit Added pull-up at PD of ADV7535 IC Updated R/C values in Buck Regulator as per sheet shared by ADI	11/01/2019	eInfochips
		Added SPI NOR 33E series termination resistors as per SI simulation Updated MIC series termination resistor values to 49E as per datasheet Comboned Shiled GND of All High-speed Connectors Part Number of D13 updated. Updated PMIC LDO output caps from 2.2uF to 4.7uF as per comments form NXP	25/01/2019	eInfochips

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Title: REVISION HISTORY 2		eInfochips An Arrow Company | The Solutions People
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RIVISION HISTORY 4

PCB REV	SCH REV	CHANGE DESCRIPTION	DATE	AUTHOR
3.0	3.0	Change R39 to 2.2K ohm and R268 to 120 ohm to have higher current to SD card FAN resistor R31 made DNP, R42 made populated Snubber provisions of ADI regulators U16 and U21 are placed before inductors Ethernet RXC/TXC series terminations R40, R9 =50E & Made C51 and C52 DNP. Need to place C51 near PHY as per tuning in EDVT, Prescan results. SD card RESET pin is utilised with Reset logic as per MEK. Changed GPIO BTREG_ON_GPIO4_19 to BTREG_ON_GPIO0_01 due to SD CARD RESET pin used Removed TP18 from ESAI and free the GPIO for BTREG Changed SD card clock R35 to 33E as per EDVT, Prescan Results Added snubbers for PMIC supplies DDRIO_1V1 & VCC_1V8	05/04/2019	eInfochips

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Title: REVISION HISTORY 2		eInfochips An Arrow Company | The Solutions People
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