## REF_LD20_96 BOARD

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### Notes
- EU: Europe
- NA: North America
- ASIA: Asia
- CHN: China
CHI#0
DDR3 4Gb 1866

CHI#1
DDR3 4Gb 1866

LD20 DDR3
5220 DDR3
IF
LD20 Initial SETUP

The LSI boot mode on the BE side will be changed.
Please refer to the sheet of "LD6b boot mode" for the detail specification.

USB Boot Port Select
- 4'b1111 = Normal
- 4'b0111 = USB Port3
- 4'b1011 = USB Port2
- 4'b1101 = USB Port1
- 4'b1110 = USB Port0

boot mode select
- 0 = debugPU(Reg/enable)
- 1 = BE boot

STM boot mode select
- Debug BOOT[11111] = Support card

PIN_NAME Internal PU/PD Function
- P_NFCLE [6]
- P_NFALE [6]
- P_XNFWE [6]
- P_XERWE1 [6]
- P_XNFWE [6]
- P_ERXW [6]

USB Boot Port Select
- PIN_NAME Internal PU/PD Function
- P_USB2OD [6, 20]
- P_MAINPWRON [6, 17]
- SW_XRSTSTM [17]
- SW_XRST [17]

Select USB Port
- 1 = default
- 4'b1111 = Normal
- 4'b0111 = USB Port3
- 4'b1011 = USB Port2
- 4'b1101 = USB Port1
- 4'b1110 = USB Port0

boot mode select
- 0 = debugPU(Reg/enable)
- 1 = BE boot

STM boot mode select
- Debug BOOT[11111] = Support card

The LSI boot mode on the BE side will be changed.
Please refer to the sheet of "LD6b boot mode" for the detail specification.
USER LEDS
The reference layout is traced according to MICRON eMMC layout guide. So when we mount TOSHIBA or others Flash, some of the pattern are traced on RFU ball. Please change layout pattern if use without MICRON eMMC.
SoC

 Ether PHY

[Diagram of EtherPHY Common]

- Various labeled components and connections are shown, including P_RGMII_TXD0[6], P_RGMII_TXD1[6], P_RGMII_TXCTL[6], P_MDC[6], P_MDIO[6], P_WOLPWRON[6], PHY_RGMII_TXD0 [22], PHY_RGMII_TXD1 [22], PHY_RGMII_TXCTL [22], PHY_MDC [22], PHY_MDIO [22], P_RGMII_TXD2[6], P_RGMII_TXD3[6], PHY_RGMII_TXD2 [22], PHY_RGMII_TXD3 [22], P_RGMII_TXCLK[6], PHY_RGMII_TXCLK [22], PHY_RGMII_TXD2 [22], PHY_RGMII_TXD3 [22], WOL3.3V, VDDWOL33, SUB3.3V, STB3.3V, WOL1.8V, VDDWOL18, SUB1.8V, STB1.8V, WOL1.8V, SUB3.3V, STB5V, WOL3.3V, and various resistor values such as R3705 (33K), R3709 (6.3K), R3711 (0), C3703 (1uF/16V), C3705 (1uF/16V), C3700 (0.33uF/16V), C3704 (0.1uF/16V), R3707 (56K), R3708 (NC/0/0603), R3706 (0/0603), R3716 (2.2M), R3713 (0/0603), R3712 (10K), R3710 (15K), R3702 (33), R3701 (15), R3700 (33), R9417 (10K).

- The diagram includes labeled connections and components typical of an EtherPHY Common circuit, showing various logic levels and power supplies.

- The diagram is marked as "CONFIDENTIAL" and includes the date 16/05/16 as well as other dates 16/05/20 and 16/06/06, indicating changes to resistor values.

- The diagram is labeled "Ether PHY" at the top.

- The diagram includes footnotes and labels such as "<GUARD>" and "<GUARD>".

- The diagram also includes component identification numbers such as U3701, U3700, Q3700, Q3701, FPF1006, PMBT3904, and "TO SOCIONEXT & LINARO."
SPDIF Out

SPDIF out

HOPERUN
TO SOCIONEXT & LINARO

CONFIDENTIAL
Add P_XIRQ19 and P_XIRQ20 to correspond nets of P.25.

Add R2447, R2448, D2403 and D2404 for power supply LED indicator.

Add U2502 (FT230X) for micro USB circuits for USB ADB.

Change CN5400 SPDIF output pin with current part number.

Change CN6002 1X12Pin connector package with FH2.0X4.6R-1X12P.

Add SPI to USB circuits with MAX3421E.

Change UART to USB circuits with flow control for USB ADB.

Add MCU-PIC24FJ256GB106 circuits to control HV2.

Remove CN2502 all related circuits.

Add 4 User LEDs and related circuits.

Add LEDs for WiFi and BT, be controlled by PWMs of SoC.

Remove IR related circuits, Page 23 becomes page 18.

Remove smartcard related circuits.

Modified U6002 Pin-B5 connection from net P_XIRQ1 to P_XIRQ3.