Hi3798CV2OPB VER.B

Hi3798CV200 Open Source Board

4 layers PCB with DDR3 8bit x 4

Board Size: 160mm x 120mm x 1.6mm

Hi3798CV2OPB VER.B_V1.0.0.0
Block Diagram
Power on board
Power on board

Vo=3.31V

The 4A DC-DC with fast transient response (such as COT or ACOT control) must be selected for the GPU power.

Vo=0.65V--1.15V

The 3A DC-DC with fast transient response (such as COT or ACOT control) must be selected for the CPU power.

Vo=5.2V

Vo=3.31V

Vo=1.50V

The 4A DC-DC with fast transient response (such as COT or ACOT control) must be selected for the GPU power.
Unit 1 of Hi3798CV200(FLASH_UART/IR/PWM/XTAL)

-----Low Speed ADC Information-----

Input Voltage Range: 0V - 3.3V ( > 3.63V is forbidden)

LSADC0: used as Key input or Power detected

LSADC1: used as Hardware Version detected

System Oscillator

20ppm is required
3. All equivalent capacitance of ESD components should be < 0.35pF.

2. Differential pairs should be routed on TOP layer only.

A. Routing
1. Route as 100 Ohm differential impedance.

Note: EMI-600ohm@100MHz and 24K ±1% precision for quarter current model

1. VIDEO REXT resistor should be 12K ±1% precision for full current model, and isolated from all other traces.

2. REXT/COMP should be traced as short as possible, and isolated from all other traces.

C. Component selection
1. REXT resistor should be 3K Ohm ±1%.
2. ESD components are suggested for ports protection.

2. Match trace length of differential pairs, 5 mils max within a pair.

** HDMI Design guideline **

A. Routing
1. Route as 100 Ohm differential impedance.
2. Differential pairs should be routed on TOP layer only.

B. Trace Length
1. The length for the differential pairs should be less than 5 inches.
2. Match trace length of differential pairs, 5 mils max within a pair.

C. Component Selection
1. REXT resistor should be 3K Ohm ±1%.
2. ESD components are suggested for ports protection.
3. All equivalent capacitance of ESD components should be < 0.35pF.

Audio & Video Design guideline

A. VIDEO
1. VIDEO REXT resistor should be 12K ±1% precision for full current model, and 24K ±1% precision for quarter current model.
2. REXT/COMP should be traced as short as possible, and isolated from all other traces.

B. AUDIO
1. VREF should be traced as short as possible, and isolated from all other traces.

** HDMI Design guideline **

A. Routing
1. Route as 100 Ohm differential impedance.
2. Differential pairs should be routed on TOP layer only.

B. Trace Length
1. The length for the differential pairs should be less than 5 inches.
2. Match trace length of differential pairs, 5 mils max within a pair.

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### MISC Interface of RGMII, RMII, SDIO, TS

#### Item

<table>
<thead>
<tr>
<th>Item</th>
<th>GE PHY 1V8 ID</th>
<th>GE PHY 3V3 ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>DVDD318_RGMm</td>
<td>Connect to 1V8 Power</td>
<td>Connect to 3V3 Power</td>
</tr>
<tr>
<td>DVDD318_RGM2i</td>
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</tr>
</tbody>
</table>

#### Pin Mux Setting in HiRegBin Tool

- RGMm, TXEN_1V8
- RGMm, TXDO_1V8
- RGMm, RXDO_1V8
- RGMm, RXD0_1V8
- RGMm, RXD2_1V8
- RGMm, TCK_1V8
- RGMm, TDO_1V8

#### Notes

1. **Design Notes**: The MISC Interface of RGMII, RMII, SDIO, TS includes connections and power supply considerations for various interfaces, including the RGM-II and RMII. The table and notes provide a comprehensive guide for setting up the interfaces correctly.

2. **Connect to 1V8 Power**: If the interface is connected to a 1V8 power supply, it should follow the specified connections and settings.

3. **Connect to 3V3 Power**: If the interface is connected to a 3V3 power supply, it should follow the specified connections and settings.

4. **Pin Mux Setting**: The table lists specific pinmux settings for the RGMm interfaces to ensure proper operation.

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**USB Design guideline**

A. **routing**
1. Route as 100 Ohm differential impedance.
2. Differential pairs should be routed on TOP layer only.

B. **trace length**
1. The length for the differential pairs should be less than 5 inches.
2. Match trace length of DP and DM differential pairs, 10 mils max within a pair.

C. **component selection**
1. USB: REXT resistor should be 133 ohm +/-1% and USB3.0 133 ohm +/-1%
2. ESD components are suggested for ports protection.
3. Equivalent capacitance of ESD component should be < 1.5pF.

**SATA & PCIe Design guideline**

A. **routing**
1. Route as 90 Ohm differential impedance.
2. Differential pairs should be routed on TOP layer only.

B. **trace length**
1. The length for the differential pairs should be less than 5 inches.
2. Match trace length of DP and DM differential pairs, 10 mils max within a pair.

C. **component selection**
1. SATA: The value of capacitors for AC coupling should be <=12nF, default 10nF
2. PCIe: The value of capacitors for AC coupling should be <=200nF, default 100nF
**DDR Design guideline**

A. General suggestion
1. Hi3798CV200 supports DDR3/DDR3L/DDR4
2. Hi3798CV200 supports up to 2GB DDR3.
3. The circuit of DDR_VREF_CA and DDR_VREF_DQ must be independent.
4. Please copy the decoupling capacitor design from HiSilicon demo board.
5. 5.3V DDRPLL is needed.

B. Layout suggestion
1. Please copy HiSilicon demo board completely
The value and part number of capacitors must be mached in PCB.
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**eMMC design guideline**

1. The different length of CLK, CMD, DAT0-7 and DATA_STROBE must be kept within 200mil.
2. The value of R9 in CMD line must follow the corresponding datasheet for detail

3.3V IO only For eMMC DDR50 Mode
   - R40 = 0 ohm
   - others = NC

eMMC5.0 (1.8V) default
   - 1.8V IO For eMMC HS200/HS400 Mode
     - R40 = NC
     - Others Mounted
** DESIGN GUIDELINE **

1. All channel traces should be separated from other traces by GND.
2. ESD components are suggested for ports protection, default BAV99.
USB WIFI

POWER OF WIFI
IF support SD3.0 the Circuit of SDIO0_PWREN circuit must be used.
USB2.0 & USB3.0

USB2.0

USB3.0
**GE PHY Design guideline**

A. RGMII interface

1. The TXCK and RXCK trace should be separated from other traces by GND.
2. The Power layout of GE PHY should copy Hisilicon demo completely.
3. The RXD(0:3) and TXD(0:3) should be separated from other traces by GND.

**GE PHY Design guideline**

A. RGMII interface

1. The TXCK and RXCK trace should be separated from other traces by GND.
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**GE PHY Design guideline**

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3. The RXD(0:3) and TXD(0:3) should be separated from other traces by GND.

**GE PHY Design guideline**

A. RGMII interface

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2. The Power layout of GE PHY should copy Hisilicon demo completely.
3. The RXD(0:3) and TXD(0:3) should be separated from other traces by GND.
Low Speed Expansion Connector (LSEC)
<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Author</th>
<th>Change Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>V0.1</td>
<td>20160308</td>
<td>HEMINGXIAO</td>
<td>The 1st Version</td>
</tr>
</tbody>
</table>
| V0.2    | 20170828  | HEMINGXIAO            | 1. Add R299=1K and D24 Red LED indicator.  
2. Add R125=47K and R141= 47K pull up resister.  
3. Change J14 from 8 Pin connector to 10 Pin connector.  
4. Change power supply of USB to UART circuits. |
| V0.3    | 20180311  | ZhangJiaYue           | 1. Update the version to VER.B.  
2. Add R407=0ohm to connect GPIO3_5 for WIFI_RST.  
3. Remove DTV turner board and smarat card circuits. |