ON Semiconductor®

1/2.7-Inch 2.3 Mp Digital Image Sensor

AR0231 Datasheet, Rev. 3

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Features

- Key technologies:
  - Automotive grade Backside Illuminated Pixel
  - LED Flicker Mitigation mode
  - Sensor Fault Detection for ASIL-B Compliance
  - Up to 4-exposure HDR at 1928x1208 and 30 fps or 3-exposure HDR at 1928x1208 and 40 fps.
- Latest 3.0 μm Back Side Illuminated (BSI) pixel with ON Semiconductor DR-Pix™ technology
- Data interfaces: up to 4-lane MIPI CSI-2, Parallel, or up t0 4-lane high speed pixel interface (HiSPi) serial interface (SLVS and HiVCM)
- Advanced HDR with flexible exposure ratio control
- LED Flicker Mitigation (LFM) mode
- Selectable automatic or user controlled black level control
- Frame to frame switching among up to 4 contexts to enable multi-function systems
- Spread-spectrum input clock support
- Multi-Camera synchronization support
- Multiple CFA options including RGB, mono and RCCC

Applications

- Automotive ADAS
- 1080p30 video applications
- High dynamic range imaging
- Mirror Replacement
- ADAS + Viewing Fusion

General Description

ON Semiconductor's AR0231AT is a 1/2.7-inch CMOS digital image sensor with a 1928Hx1208V active-pixel array. It captures images in either linear, high dynamic range, or LFM modes, with a rolling-shutter readout. The LFM mode eliminates high frequency LED flicker in the image allowing Traffic Sign Reading (TSR) algorithms to operate in all lighting conditions. It includes sophisticated camera functions such as in-pixel binning, windowing and both video and single frame modes. It is designed for both low light and high dynamic range scene performance. sensor fault detection features to enable camera ASIL B compliance. It is

programmable through a simple two-wire serial interface. The AR0231AT produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of applications, including automotive ADAS, automotive scene viewing, and 1080p HDR video.

Table 1:   Key Parameters

Parameter	Value
Optical format	1/2.7-inch (6.82 mm)
Maximum resolution	1928 x 1208 (2.3 Mp)
Shutter type	Electronic Rolling Shutter (ERS)
Pixel size	3 μm x 3 μm
Pixel output interfaces	Up to 4-lane HiSPi with SLVS and HiVCM MIPI CSI-2 14-bit parallel
Output formats	12-bit Uncompressed Linear 20-bit Uncompressed HDR 10-bit, or 8 -bit Companded Linear 16-bit, 14-bit, or 12-bit Companded HDR
Control interface	2-wire, Serial Control 100 kHz/1 MHz
Input clock range	6-64 MHz in PLL mode 6-88 MHz Max in PLL-bypass Mode
Maximum frame rate	Up to 40 fps at 1928 x 1208 / 3-exposure Up to 60fps at 1928x1208 / 2-exposures and Linear
Output pixel clock maximum	88 MHz
Responsivity	TBD
SNRmax	TBD
Max Dynamic Range	>120 dB
Packaging options	11 x 10 iBGA Bare die
Operating temp. range	−40°C to 105°C ambient
Supply voltage	I/O 1.8 V or 2.8 V Digital 1.2 V Analog 2.8 V HiSPi 0.4 V or 1.8 V
Power consumption	<680 mW typical (1928 x 1208, 30 fps)

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Ordering Information

Table 2: Available Part Numbers

Part Number	Product Description	Orderable Product Attribute Description
AR0231ATSC00XPEA0-DPBR-E	0deg CRA, RGB iBGA	Dry Pack with Protective Film, Double Side BBAR Glass
AR0231ATSC00XPD20-E	0deg CRA, RGB Die	
AR0231ATSG00XPEA0-DPBR-E	0deg CRA, RGBC iBGA	Dry Pack with Protective Film, Double Side BBAR Glass
AR0231ATSG00XPD20-E	0deg CRA, RGBC Die	
AR0231ATSR00XPEA0-DPBR-E	0deg CRA, RCCC iBGA	Dry Pack with Protective Film, Double Side BBAR Glass
AR0231ATSR00XPD20-E	0deg CRA, RCCC Die	
AR0231ATSC00XPEAH3-GEVB	RGB, Headboard	
AR0231ATSG00XPEAH3-GEVB	RGBC, Headboard	
AR0231ATSR00XPEAH3-GEVB	RCCC, Headboard	
AR0231ATSC00XPEAD3-GEVK	RGB, Demo Kit	
AR0231ATSG00XPEAD3-GEVK	RGBC, Demo Kit	
AR0231ATSR00XPEAD3-GEVK	RCCC, Demo Kit	

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General Description

The ON Semiconductor AR0231AT can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a 1080p-resolution image at 40 frames per second (fps) in 3-exposure HDR mode and 30 fps in 4-exposure HDR mode through the HiSPi or MIPI ports. In linear mode, it outputs 12-bit uncompressed, or 10-bit, or 8-bit A-Law compressed raw data, using either the parallel or serial (HiSPi) output ports. In high dynamic range (HDR) mode, it outputs 12, 14-, or 16-bit compressed data using parallel output. In HiSPi or MIPI mode, 12-, 14-, 16-bit compressed, or 20-bit linearized data may be output. The device may be operated in video (master) mode or in single frame trigger mode. The LFM mode is used to minimize the impact of LED flicker for applications where there is dynamic LED lighting, such as TSR, and is output in linear mode.

FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a synchronized pixel clock in parallel mode.

The AR0231AT includes additional ASIL features: two on-board independent temperature sensor, startup tests, memory BIST, analog and digital CRC, and test patterns.

Optional register information and histogram statistic information can be embedded in the first and last 2 lines of the image frame.

Functional Overview

The AR0231AT is a 1/2.7 inch progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 6 and 64 MHz. The PLL can also be bypassed in parallel mode, which allows for the input clock to run between 6 and 88 MHz. The maximum output pixel rate is 750 Mp/s, corresponding to a clock rate of 88 MHz. Figure 1 on page 7 to Figure 3 on page 9 show a configuration diagram of the sensor in parallel, HiSPi and MIPI interfaces.

Figure 1:   Typical Configuration, Parallel
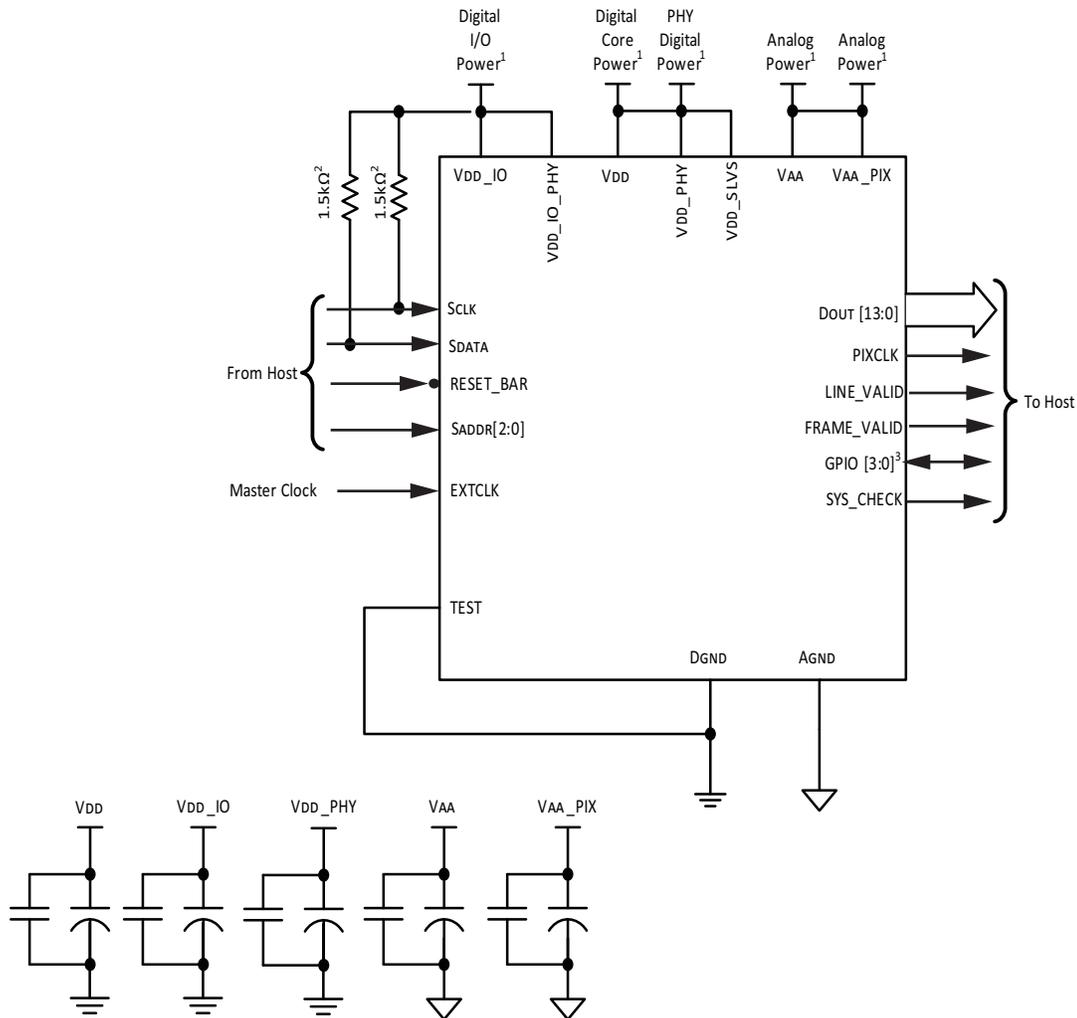
Notes: 1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5kΩ, but a greater value may be used for slower two-wire speed.
3. GPIO[2:0] can be left unconnected if not used. GPIO3 should be tied to DGND if not used.
4. The serial interface output pads can be left unconnected when the parallel output interface is used.
5. ON Semiconductor recommends that 0.1μF and 10μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0231AT demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
7. I/O signals voltage must be configured to match V_{DD}_IO voltage to minimize any leakage currents.
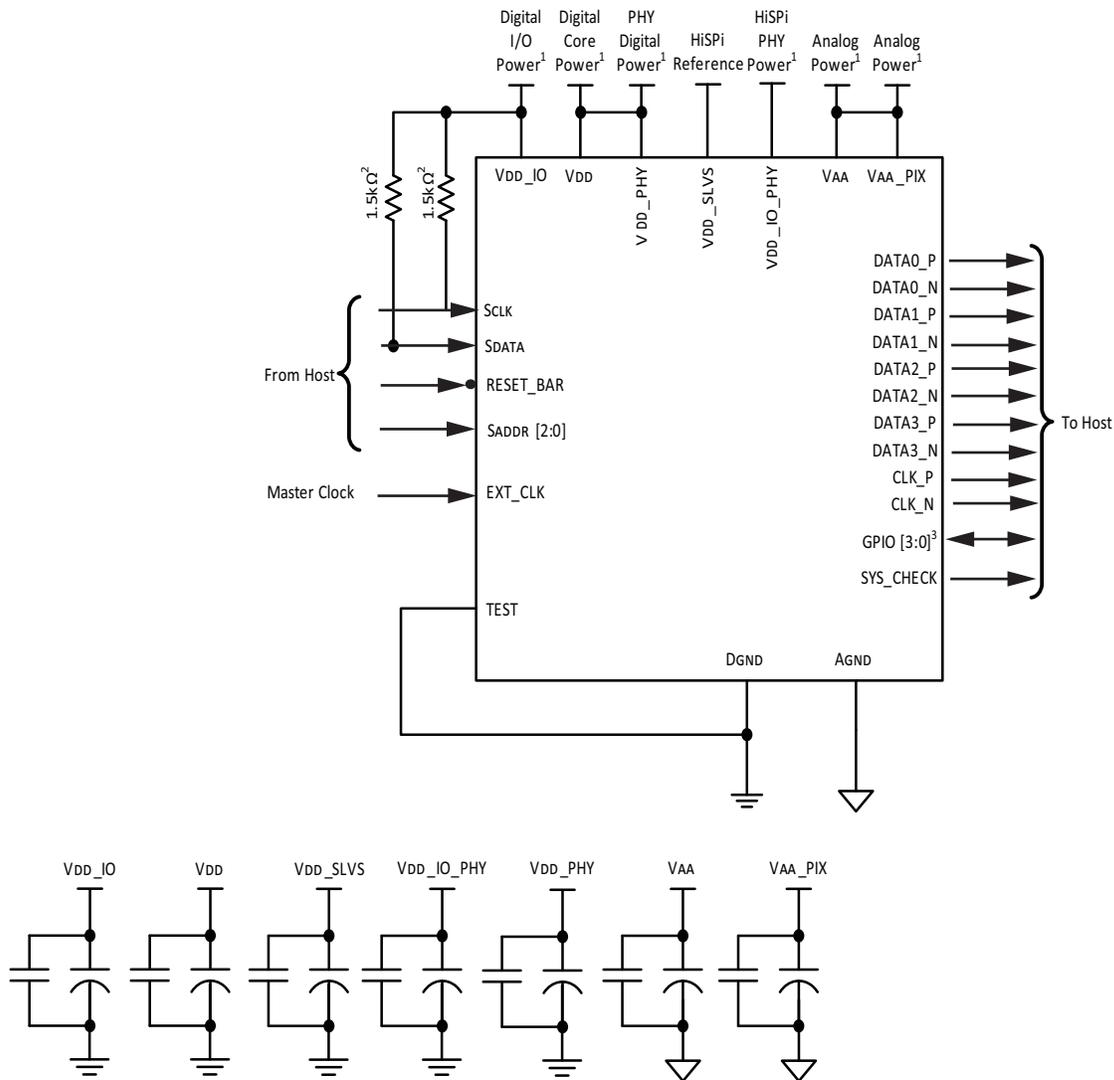
Figure 2:   Typical Configuration, 4-Lane HiSPi

Notes: 1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. GPIO[2:0] can be left unconnected if not used. GPIO3 should be tied to DGND if not used.
4. The parallel interface output pads can be left unconnected when the serial output interface is used.
5. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0231AT demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
7. I/O signals voltage must be configured to match VDD_IO voltage to minimize any leakage currents.
8. If Vdd_IO is 1.8 V, then Vdd_IO_PHY cannot equal 2.8 V.

Figure 3:   Typical Configuration, 4-Lane MIPI
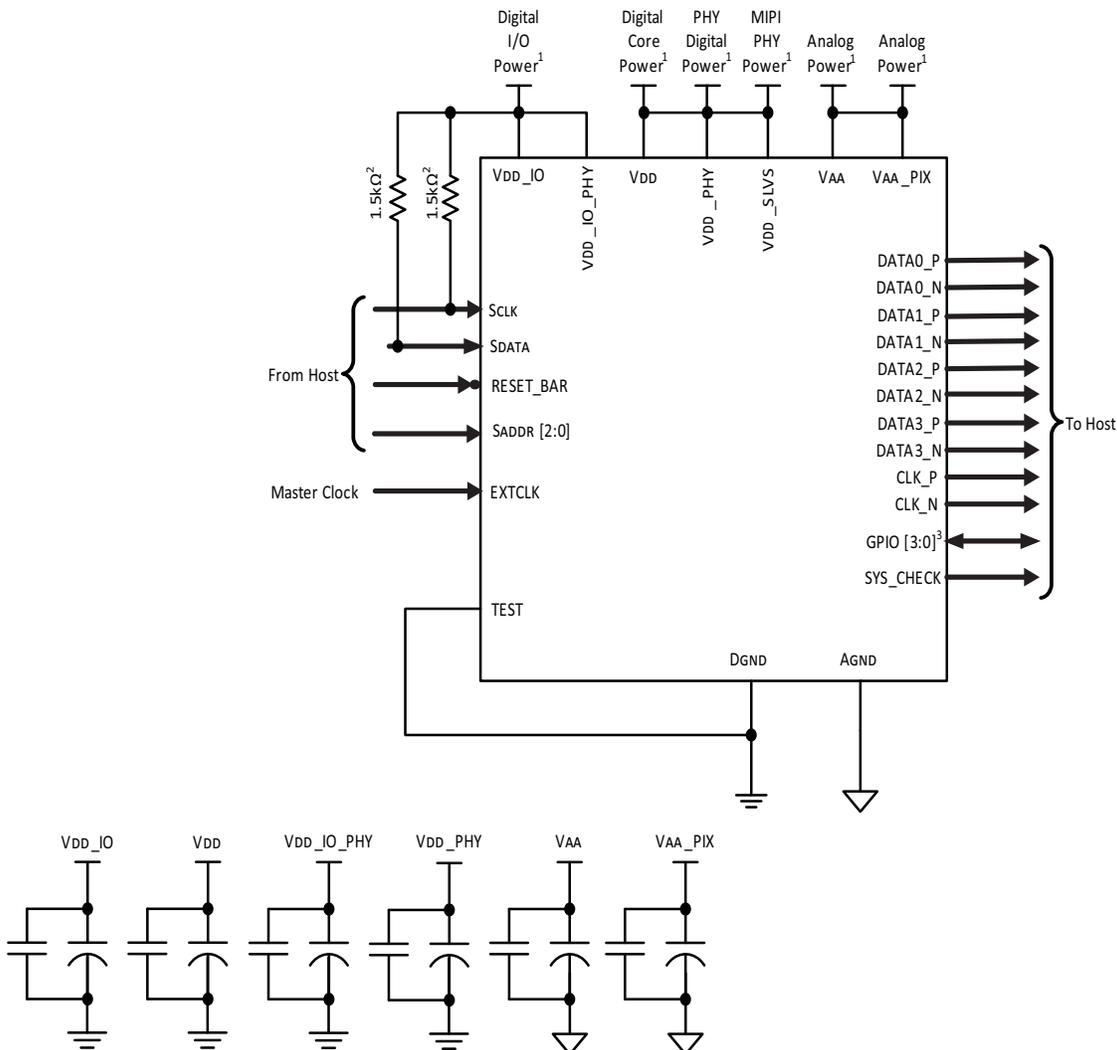

Notes: 1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. GPIO[2:0] can be left unconnected if not used. GPIO3 should be tied to DGND if not used.
4. The parallel interface output pads can be left unconnected if the serial output interface is used.
5. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on lay-out and design considerations. Refer to the AR0231 demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
7. I/O signals voltage must be configured to match V_{DD}_IO voltage to minimize any leakage currents.

Pixel Data Format

Pixel Array Structure

While the sensor's format is 1928x1208, additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for mono-chrome or color versions. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out.

Figure 4:   **Pixel Array Description**

1944

10 barrier + 4 border pixels

1928^1 x 1208
5.78 mm x 3.62 mm

1236

2 barrier + 6 border pixels

2 barrier + 6 border pixels

10 barrier + 4 border pixels

Light dummy pixel   Active pixel
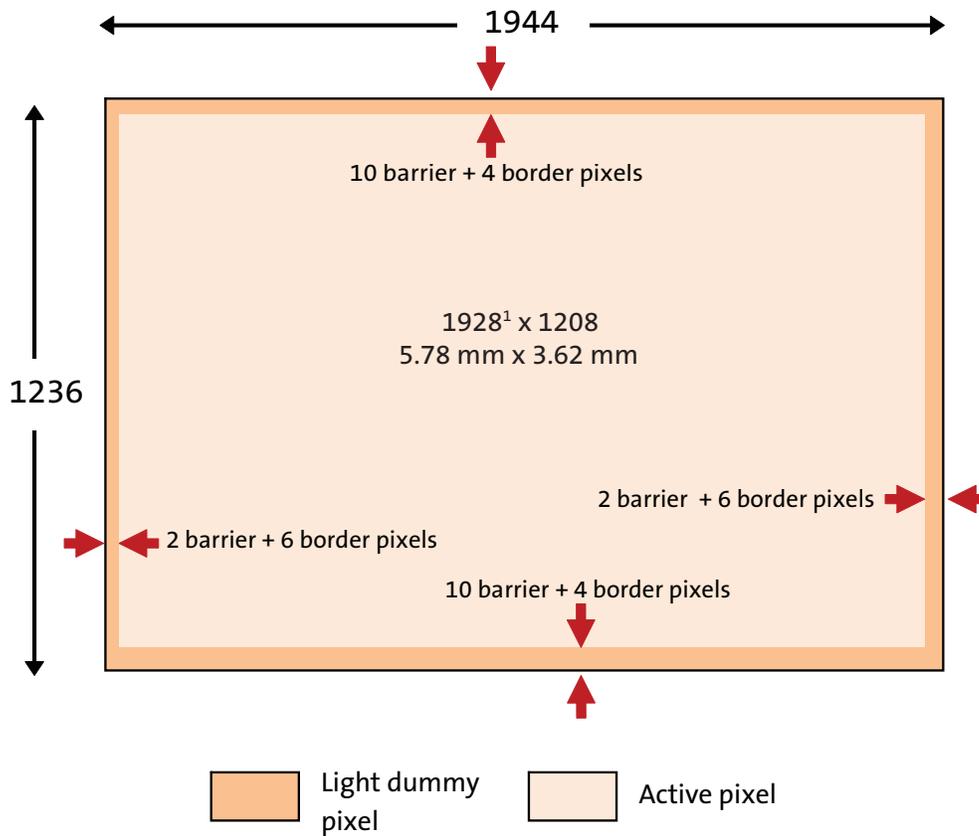
Figure 5:   Pixel Color Pattern Detail (Top Right Corner)
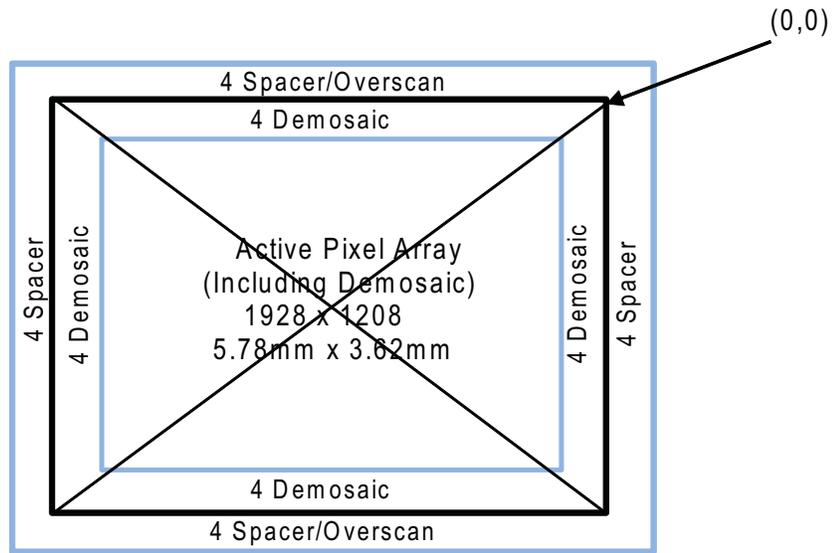
Default Readout Order

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 5). This reflects the actual layout of the array on the die. Also, the first pixel data read out of the sensor in default condition is that of pixel (7, 7).

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 6. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 6.

Figure 6:   Imaging a Scene
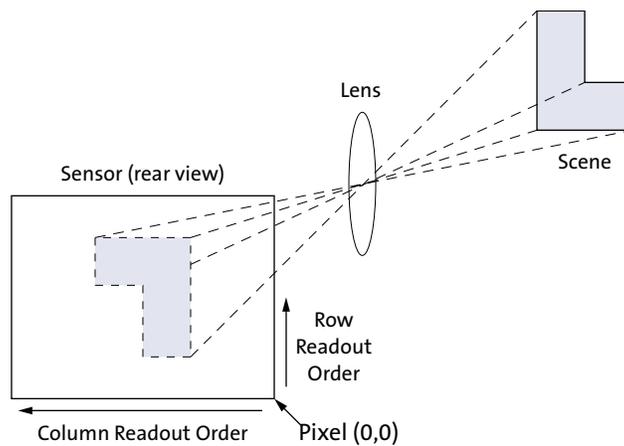
Operating Modes and Features

3.0 μm Dual Conversion Gain Pixel

To improve the low light performance and keep the high dynamic range, a large (3.0μm) dual conversion gain pixel is implemented for better image optimization. With a dual conversion gain pixel, the conversion gain of the pixel may be dynamically changed to better adapt the pixel response based on dynamic range of the scene. This gain can be switched manually or automatically by an auto exposure control module.

Resolution

The active array supports a maximum of 1928 x 1208 pixels to support 1080p resolution. Utilizing a 3.0μm pixel will result in an optical format of 1/2.7-inch (approximately 6.82 mm diagonal).

Frame Rate

At full resolution, the AR0231AT is capable of running up to 30 fps in parallel mode and 40 fps in MIPI or HiSPi modes, depending on the number of exposures. The AR0231AT has a maximum frame rate of 60fps at full resolution in 2-exposure HDR and linear modes.

High Dynamic Range

The AR0231AT can operate in an HDR mode to acquire video data using ON Semiconductor's multi-exposure technology. This allows the sensor to handle >120 dB of intrascene dynamic range. The sensor also features a linear or standard dynamic range (SDR) mode where a single image is captured. In HDR mode, the sensor sequentially captures multiple exposures by maintaining separate read and reset pointers that are interleaved within the rolling shutter readout. The intermediate pixel values are stored in line buffers while waiting for all the exposure values to be present. As soon as all exposure values are available, they are combined to create a linearized 20-bit value for each pixel's response. This 20-bit value may be output directly or optionally compressed before output.

Individual control for T1, T2, T3, and T4 exposures is possible, allowing a wide range of exposure ratios within the maximum limits of each exposure line buffers allocated.

Individual T1, T2, T3 and T4 exposures can be output (depending on resolution/frame rate used) when in HDR mode for applications that require these to be processed individually.

The dual conversion gain (LCG and HCG) can be controlled independently for each HDR exposure. For example, it is now possible to have an HDR frame where T1 uses HCG, but T2, T3 and T4 use LCG.

Motion Compensation

In typical multi-exposure HDR systems, motion artifacts can be created when objects move during the integration time of the exposures used to construct the image. When this happens, edge artifacts can potentially be visible and might look like a tearing or ghosting effect. To correct for this issue, the AR0231AT incorporates the digital lateral overflow (DLO) algorithm as implemented in the AR0132, but with the addition of individual color knee points, as well as an additional knee point for the fourth exposure.

LED Flicker Mitigation (LFM)

LED sign flicker causes traffic signs to be incorrectly read in bright daylight conditions as the LEDs may be illuminated when the sensor is not integrating. The AR0231AT includes a new mode, LFM, for reading these signs. In LFM mode, pixels are floating-diffusion (FD) color merged in the vertical direction, and the effective sensitivity of the pixel pairs can be controlled and reduced, enabling exposure times to be extended. On AR0231AT variants with color CFAs, color will be maintained in the sensor output to aid in sign discrimination. HDR output is not available during LFM operation. LFM mode is intended for machine vision applications and should not be used for viewing. A typical use case would be to capture 3 frames of HDR data, context switch to LFM for 1 frame, and then switch back HDR for video captured at 40fps.

In addition to LFM operation the AR0231AT will also support fractional gain down to 0.125x during normal operation.

Dual Conversion Gain (DCG)

To improve the low light performance and keep the high dynamic range, the AR0231AT has a dual conversion gain pixel implemented for better image optimization. With a dual conversion gain pixel, the conversion gain of the pixel may be dynamically changed to better adapt the pixel response based on dynamic range of the scene. This gain can be switched manually or automatically by an auto exposure control module.

Multi-camera Synchronization

AR0231AT supports multi-camera synchronization Slave modes. The Slave modes support synchronization of multiple cameras within 8 pixel clocks from the beginning of FRAME_VALID/LINE_VALID from sensors without reducing the maximum frame rate. This feature saves the line memory buffer at the host system to combine a multiple of video input streams from the sensors.

Figure 7 on page 14 shows typical stereo camera systems using SLAVE mode.

Figure 7:   Typical Stereo Camera Configuration
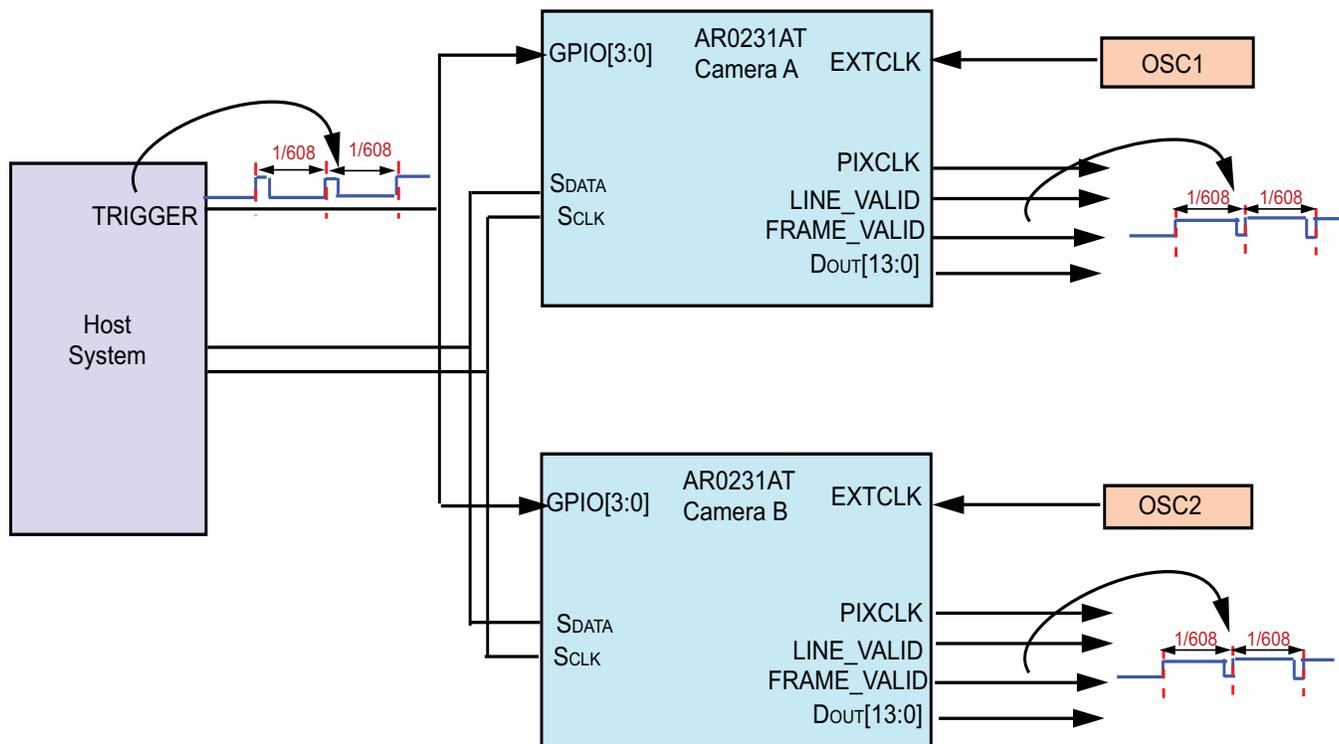
Slave Mode

The slave mode feature of the AR0231AT supports triggering the start of a frame readout from an input signal that is supplied from an external ASIC. The slave mode signal allows for precise control of frame rate and register change updates.

Context Switching and Register Updates

The user has the option of using the highly configurable context memory, or a simplified implementation in which only a subset of registers is available for switching. The AR0231AT supports a highly configurable context switching RAM of size 256 x 16. Within this Context Memory, changes to registers within the chip may be stored. The register set for each context must be the same, but the number of contexts and registers per context are limited only by the size of the context memory.

Alternatively, the user may switch between two predefined register sets A and B by writing to a context switch change bit. When the context switch is configured to context A the sensor will reference the context A registers. If the context switch is changed from A to B during the readout of frame n, the sensor will then reference the context B coarse_integration_time registers in frame n+1 and all other context B registers at the beginning of reading frame n+2. The sensor will show the same behavior when changing from context B to context A. The following registers are context switchable:

Table 3:   List of Configurable Registers for Context A and Context B

Context A Register Description	Context B Register Description
coarse_integration_time	coarse_integration_time_cb
line_length_pck	line_length_pck_cb
frame_length_lines	frame_length_lines_cb
row_bin	row_bin_cb
col_bin	col_bin_cb
fine_gain	fine_gain_cb
coarse_gain	coarse_gain_cb
x_addr_start	x_addr_start_cb
y_addr_start	y_addr_start_cb
x_addr_end	x_addr_end_cb
y_addr_end	y_addr_end_cb
y_odd_inc	y_odd_inc_cb
x_odd_inc	x_odd_inc_cb
green1_gain	green1_gain_cb
blue_gain	blue_gain_cb
red_gain	red_gain_cb
green2_gain	green2_gain_cb
global_gain	global_gain_cb
operation_mode_ctrl	operation_mode_ctrl_cb
bypass_pix_comb	bypass_pix_comb_cb

Embedded Data and Statistics

The AR0231AT can append embedded statistics to an output image frame, including frame identifiers and histogram information for that image. This can be used by downstream auto-exposure blocks to make decisions about exposure adjustment.

Histograms for up to three independent regions of interest (ROIs) can be tracked per frame, with programmable registers determining their size and location. Two compression methods are available for the histogram data. The legacy mode is the same histogram compression implemented in the AR0132 and AR0333 parts. The AR0231AT also provides an alternate logarithmic compression scheme for the histogram data that allocates more bins for the lower pixel values, enabling more detailed data for the dark portions of the image. Note that histogram information can be output for only one pixel plane at a time.

In addition to histograms, the output image frame can be split into a virtual grid of up to 16 ROIs that can each provide the average pixel value for that region. The grid for ROIs is defined by four offset pointers for each axis (X and Y), as shown in Figure 8. Each of these averages can be included with the statistics embedded in the output image, allowing a simple exposure metric for each region to be generated.

Figure 8:   Grid-ROI, Configuration 1; x_grid_status=0x3; y_grid_status=0x3
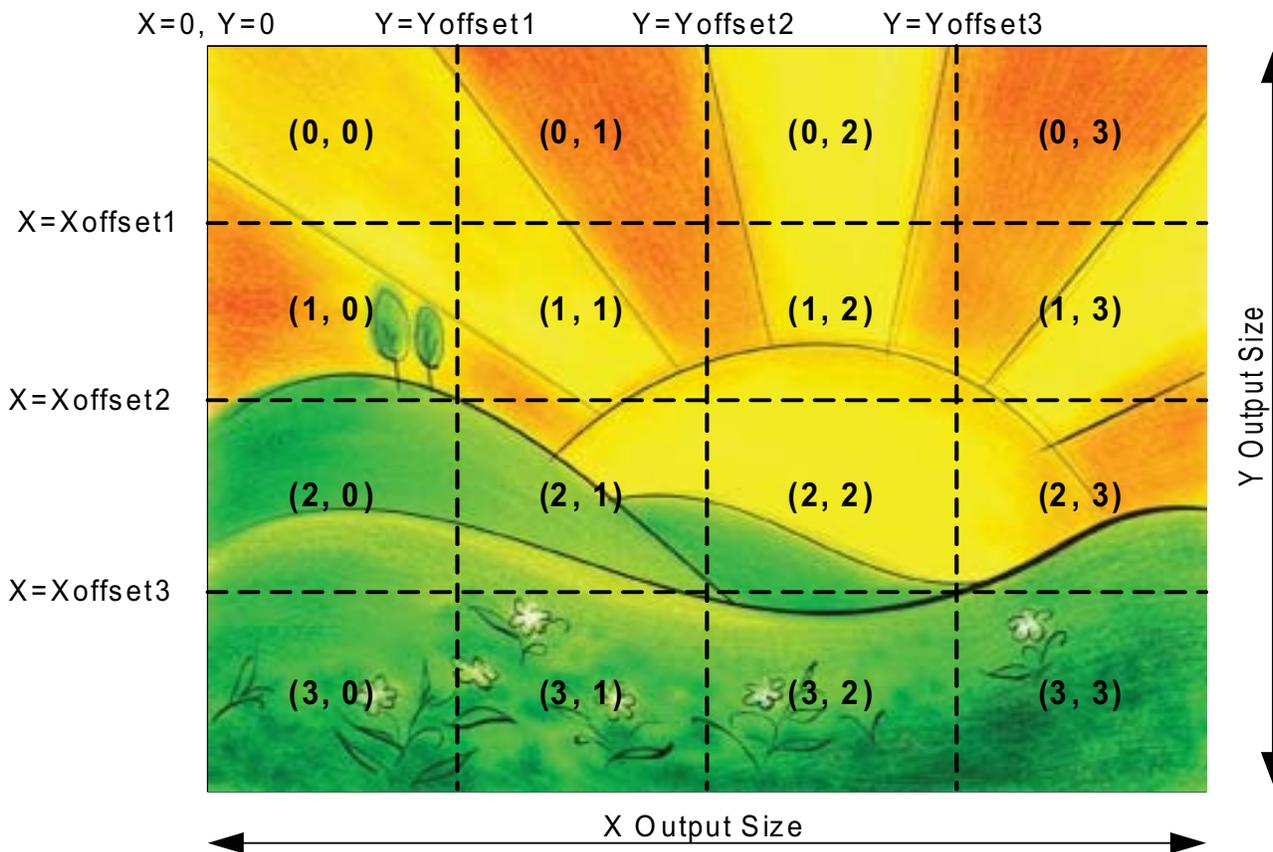
Black Level Control/Correction

Black level correction can optionally be automatically controlled by the AR0231AT; the default setting is for automatic black level calibration to be enabled. The automatic black level correction measures the average value of pixels from a set of optically black lines in the image sensor. The pixels are averaged as if they were light sensitive and passed through the appropriate gain. This line average is then digitally low-pass filtered over many frames to remove temporal noise and random instabilities associated with this measurement.The optically black lines may be read out, bypassing the datapath, for off-chip analysis. The automatic black level correction can be disabled and the black level set manually via register settings. Manual black level settings are frame synchronized to the next start of frame.

Row and Column Correction

Row and column noise correction is applied automatically by the image sensor on a frame by frame basis. Re-triggering of correction circuits due to settings or temperature changes are not necessary. No adjustments are provided for these correction circuits but they may be individually enabled/disabled.

Defective Pixel Tracking/Correction

Defective Pixel Correction (DPC) is intended to compensate or tag defective pixels by replacing their value with a value based on the surrounding pixels, or tagging them by assigning them a '0' value. The defect pixel correction feature supports up to 200 defects. The locations of defective pixels are stored in a table on chip during the manufacturing process; this table is accessible through the two-wire serial interface. There is no provision for later augmenting the defect table entries. The DPC algorithm is one-dimensional, calculating the resulting averaged pixel value based on nearby pixels within a row. The algorithm distinguishes between color and monochrome parts; for color parts, the algorithm uses nearest neighbor in the same color plane. The defect pixel correction algorithm may be disabled. (Note that the outgoing defect specification for the AR0231AT assumes the defect correction is disabled). The defect pixels identified during manufacture can be read from on-chip ROM via the 2-wire control interface.

Analog/Digital Gains

A programmable analog gain of 0.125x to 8x applied simultaneously to all color channels will be featured along with a digital gain of 1x to 16x that may be configured on a per color channel basis. Future releases will have an option to separate the digital gain for use as an AWB function and as a global gain.

Skipping/Binning Modes

The AR0231AT supports subsampling. Subsampling allows the sensor to read out a smaller set of active pixels by either skipping, binning, or summing pixels within the readout window. Horizontal binning is achieved in the digital readout. The sensor will sample the combined two adjacent pixels within the same color plane. Vertical row binning is applied in the pixel readout. Row binning can be configured as two rows within the same color plane. Pixel skipping can be configured up to two in both the x-direction and y-direction. Skipping pixels in the x-direction will not reduce the row time. Skipping pixels in the y direction will reduce the number of rows from the sensor effectively reducing the frame time. Skipping will introduce image artifacts from aliasing. The AR0231AT supports row wise vertical binning. Row wise vertical summing is not supported.

CFA Type Identification

CFA type (e.g. RGB, mono, etc.) may be determined by reading an identification register via the 2-wire control interface.

ASIL / ISO26262 Support Features

The AR0231AT incorporates many features to assist ASIL-B system compliance to be achieved by a system that integrates it. Table 4, "ASIL Support Features," on page 18 below shows a summary of these features.

Table 4:   ASIL Support Features

Feature	Description
Communication and Interface CRC	The sensor computes a CRC for data transmitted from the sensor to the host, permitting the host to identify transmission errors in such data. The sensor shall also expect a CRC value to be embedded in data transmitted from the host, and if the CRC fails, the sensor shall raise an error flag
Memory BIST	Writes a a pattern into all the bytes of all major SRAM blocks and read backs the values to detect stuck at 1 and stuck at 0 faults
CRC of Image Data	Image data transmission from the imager to the host will contain CRC (Cyclic Redundancy Checks) of data within a row to detect errors in communication (HiSpi).
Embedded Data	There are 2 rows of data which are prepended to the image frame output which are comprised of critical register contents. This allows imager register contents to be logged with each image.
Statistics Data	There are 2 rows of data which are appended to the image frame output which are comprised of critical image statistics information.
Digital Frame Counter	A 64-bit counter keeps track of the frame count and this value is included as part of embedded data.
Analog Frame Counter	There will be one row of data which will be prepended to the image frame output which consists of an analog representation of the Digital Frame Counter.
Column Address	There will be optional one row of data which will be prepended to the image frame output which consists of values which mirror the column address from which the data was read. This is an on-line test which ensures that the column decoder and vertical pixel routes are working properly prior to the output of each frame.
Row Address	There will be optional additional pixels of data prepended to each row of image data which consists of values which mirror the row address from which the data was read. This is an on-line test which ensures that the row decoder and horizontal pixel routes are working properly prior to the output of each frame.
On-line Analog and Digital Test Patterns	There will be a programmable number of rows (digital test pattern) prepended and/or appended to each frame of image data which enables on-line analog and/or digital fault monitoring.
Temperature Sensor	Two independent temperature sensors that report temperature in degrees Celsius from -40 °C to 125°C.

System Interfaces

This section describes the AR0231AT interfaces. Note that all output port options may not be available on all packaging options.

HiSPi Pixel Output Port

The AR0231AT provides a 4-lane HiSPi pixel output port with support for SLVS and HiVCM modes. Supported configurations are described in Table 5. Additional information is provided in the ON Semiconductor HiSPi Protocol and Physical Layer documents.

Table 5:   HiSPi Protocol Support

Lanes	Width	Data type	Protocols	Max. Mbps/lane	Notes
1, 2, or 4	20-bit	Bayer/RAW	SP-packetized SP-streaming Streaming-S	750 Mbps	HDR output mode (uncompressed)
1, 2, or 4	16-bit	Bayer/RAW	SP-packetized SP-streaming Streaming-S	750 Mbps	HDR output mode (compressed)
1, 2, or 4	14-bit	Bayer/RAW	SP-packetized SP-streaming Streaming-S	750 Mbps	HDR output mode (compressed)
1, 2, or 4	12-bit	Bayer/RAW	SP-packetized SP-streaming Streaming-S	750 Mbps	SDR (linear) mode

MIPI CSI-2 Pixel Output Port

The AR0231AT provides a 4-lane MIPI CSI-2 pixel output port. The data protocol support is per Table 6. Please contact ON Semiconductor for additional information.

Table 6:   MIPI Protocol Support

Lanes	Width	Data type	Protocols	Max. Mbps/lane	Notes
1, 2, or 4	20-bit	Bayer/RAW	SP-packetized SP-streaming	750 Mbps	HDR output mode (uncompressed)
1, 2, or 4	16-bit	Bayer/RAW	SP-packetized SP-streaming	750 Mbps	HDR output mode (compressed)
1, 2, or 4	14-bit	Bayer/RAW	SP-packetized SP-streaming	750 Mbps	HDR output mode (compressed)
1, 2, or 4	12-bit	Bayer/RAW	SP-packetized SP-streaming	750 Mbps	SDR (linear) mode

Parallel Pixel Output Port

The AR0231AT provides a 14-bit data pixel output port with frame and line valid signals. HDR data is companded to 14-bit or 12-bit, and 12-bit SDR (non-HDR) data may be output via this port.

Note that the parallel port cannot be used to output combinations of individual T1/T2/T3/T4 exposures on a per frame basis.

Line Interleaved Output

The AR0231AT will have the capability to output the T1, T2, T3, and T4 exposures separately, in a line interleaved format. The purpose of this is to enable off chip HDR linear combination and processing.

This section describes the line interleaved output format for HDR (multiple-exposure) readout.

General Notes:

- Terminology: "SOV" and "EOV" codes are the same as SAV/EAV with V bit = 1 (i.e. VBLANK)
- As with non-HDR readouts, end-of-line (EAV/EOL/EOV) sync codes are not required
- As with non-HDR readouts, explicit SOF and EOF codes are not required if blanking codes (SOV) are sent during VBLANK
- Sets of exposures cannot overlap. i.e. There must be "global VBLANK" period between the last exposure of Frame N and the first exposure of Frame N+1, during which no active data is read out

The AR0231AT will support a line-interleaved mode with active blanking. In this mode, each exposure line is delineated by its own SAV/SOL marker. Padding/Dummy lines for each exposure's individual VBLANK are sent as active lines delineated by their own SAV/SOL markers. See Figure 9 for an example of a three-exposure HDR frame.

Figure 9:   Multi-Exposure Frame Example
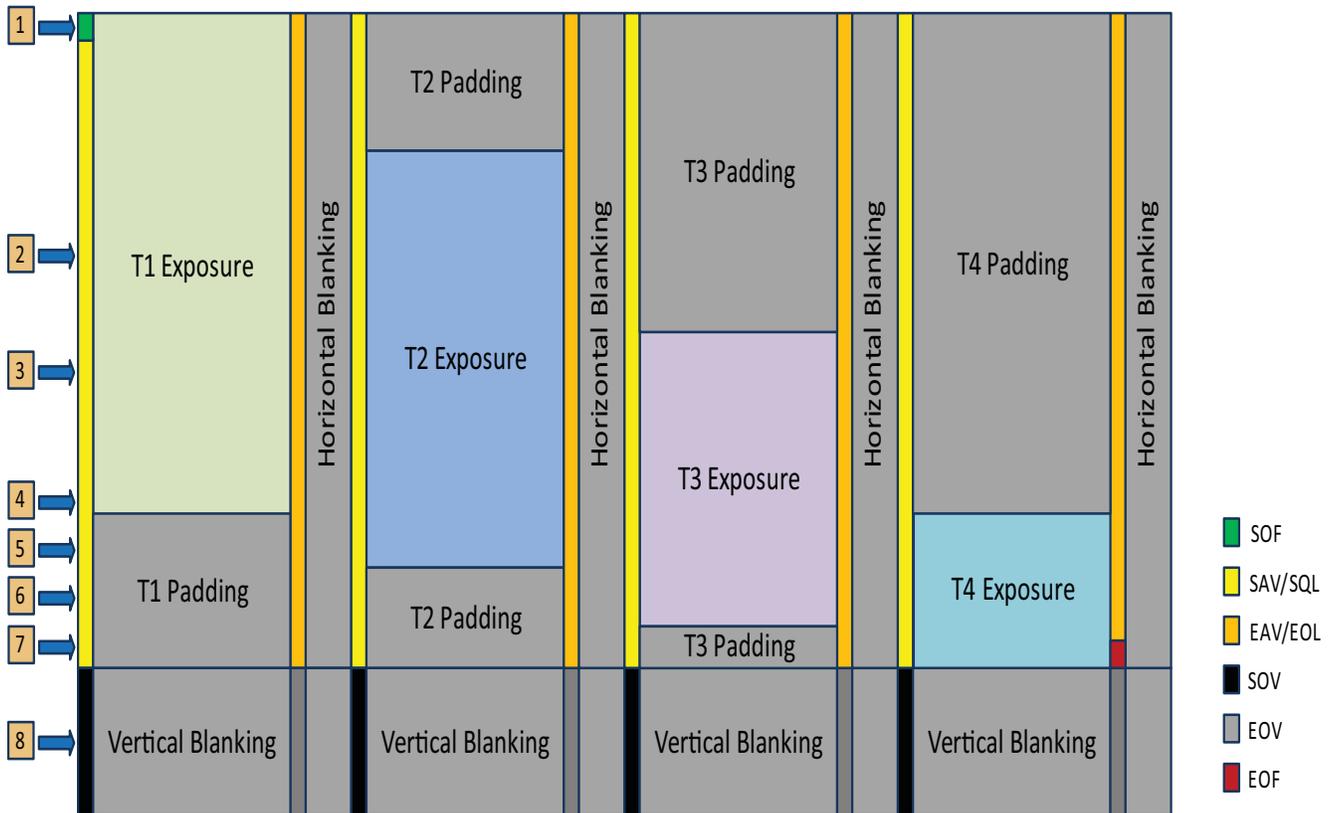
Note: Each row readout happens from left to right (RO: T1>T2>T3>T4, T1>T2>T3>T4, ...)
            Embedded data will be output only on the T1 data frame.
            Stats data will be output only on the T4 data frame.
            RNC is output only for T4 and on the T4 data frame.
            TAR is output only on the T4 data frame.

To more clearly illustrate how blanking data is embedded into the active readout, Figure 10 on page 22 shows the line-by-line readout at different points during the readout (Match the numbers with Figure 9 above). Note that actual vertical blanking occurs only when all exposures are completely read out. T1, T2, T3, or T4 Padding is inserted until all exposures have been read out. The Padding is treated as though it were a line of active video. The padding value is the same for T1, T2, T3, and T4 and is set to 0x0004.

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Figure 10:   Line by Line Readout
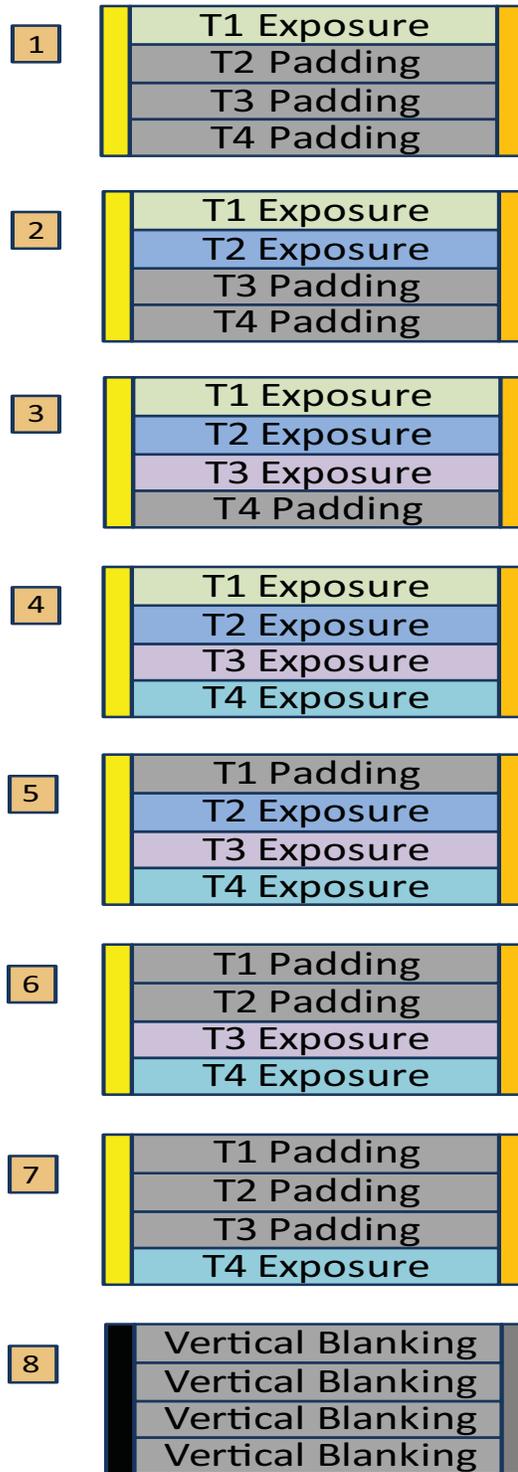
Two-Wire Sensor Control Interface

The two-wire serial interface bus enables read/write access to control and status registers within the AR0231AT. The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD_IO off-chip by a 1.5kΩ resistor. Either the slave or master device can drive SDATA LOW-the interface protocol determines which device is allowed to drive SDATA at any given time. The protocols described in the two-wire serial interface specification allow the slave device to drive SCLK LOW; the AR0231AT uses SCLK as an input only and therefore never drives it LOW.

Electrical Specifications

Table 7:   **Electrical Specifications**

Symbol	Definition	Min	Nominal	Max	Unit
VDD	Core digital voltage	1.14	1.2	1.26	V
VDD_IO	I/O digital voltage	1.7/2.52	1.8/2.8	1.9/3.0	V
VAA	Analog voltage	2.6	2.8	3.0	V
VAA_PIX	Pixel supply voltage	2.6	2.8	3.0	V
VDD_PHY	PHY supply voltage	1.14	1.2	2.16	V
VDD_IO_PHY	Serial PHY supply voltage	1.7 /2.52	1.8/2.8	1.9/3.0	V
VDD_SLVS	HiSPi supply voltage (SLVS)	0.3	0.4	0.6	V
VDD_SLVS	HiSPi supply voltage (HiVCM)	1.7	1.8	1.9	V

Note: VAA_PIX must always be equal to VAA.

Power Up

For controlled power up, RESET_BAR pin must be asserted (low) before supplies can be sequenced up in any order (except VPP). Once all supplies are valid, RESET_BAR is deasserted (high), the part will begin boot-up on EXTCLK.

Power Down

For controlled power down, streaming must be first disabled. The RESET_BAR pin must be asserted (low) before any external supplies are removed. Then the supplies are allowed to be sequenced off in any order.

Typical Power Down Sequence:
1. De-assert Streaming: Set software standby mode (mode_select = 0) register.
2. Wait till the end of the current frame (or end-of-line if so configured).
3. Configure I/O for "hold" if desired. "Hold" state requires maintaining VDD_IO; however.
4. Set RESET_BAR = 0. (Hard Standby, low-leakage state)
5. Wait t0 power-down delay.
6. Power off supplies in any order. For "hold" I/O state, do not power off VDD_IO supply.

Two-Wire Serial Register Interface

The electrical characteristics of the two-wire serial register interface (S_{CLK}, S_{DATA}) are shown in Figure 11 and Table 8.

Figure 11:   Two-Wire Serial Bus Timing Parameters

Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

Table 8:   Two-Wire Serial Bus Characteristics

^{f}EXTCLK = 27 MHz; V_{DD} = 1.8V; V_{DD}_IO = 2.8V; V_{AA} = 2.8V; V_{AA}_PIX = 2.8V; V_{DD}_PLL = 2.8V; T_A = 25°C

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCLK Clock Frequency	^{f}SCL	0	100	0	1000	KHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	^{t}HD;STA	4.0	-	0.6	-	µs
LOW period of the SCLK clock	^{t}LOW	4.7	-	1.3	-	µs
HIGH period of the SCLK clock	^{t}HIGH	4.0	-	0.6	-	µs
Set-up time for a repeated START condition	^{t}SU;STA	4.7	-	0.6	-	µs
Data hold time	^{t}HD;DAT	0^4	3.45^5	0^6	0.9^5	µs
Data set-up time	^{t}SU;DAT	250	-	100^6	-	ns
Rise time of both SDATA and SCLK signals	^{t}r	-	1000	$20 + 0.1Cb^7$	300	ns
Fall time of both SDATA and SCLK signals	^{t}f	-	300	$20 + 0.1Cb^7$	300	ns
Set-up time for STOP condition	^{t}SU;STO	4.0	-	0.6	-	µs
Bus free time between a STOP and START condition	^{t}BUF	4.7	-	1.3	-	µs
Capacitive load for each bus line	Cb	-	400	-	400	pF
Serial interface input pin capacitance	CIN_SI	-	3.3	-	3.3	pF
SDATA max load capacitance	CLOAD_SD	-	30	-	30	pF
SDATA pull-up resistor	RSD	1.5	4.7	1.5	4.7	KΩ

Notes: 1. This table is based on I^{2}C standard (v2.1 January 2000). Philips Semiconductor.
2. Two-wire control is I^{2}C-compatible.
3. All values referred to V_{IHmin} = 0.9 V_{DD} and V_{ILmax} = 0.1V_{DD} levels. Sensor EXCLK = 27 MHz.
4. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
5. The maximum ^{t}HD;DAT has only to be met if the device does not stretch the LOW period (^{t}LOW) of the SCLK signal.
6. A Fast-mode I^{2}C-bus device can be used in a Standard-mode I^{2}C-bus system, but the requirement ^{t}SU;DAT 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line ^{t}r max + ^{t}SU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I^{2}C-bus specification) before the SCLK line is released.
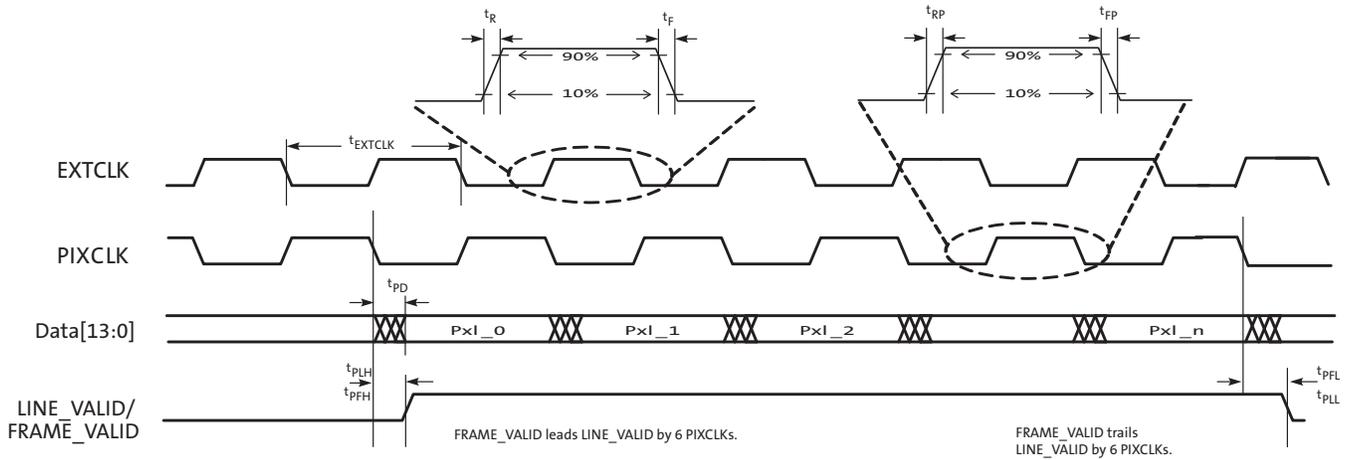7. Cb = total capacitance of one bus line in pF.

I/O Timing

By default, the AR0231AT launches pixel data, FV, and LV with the falling edge of PIXCLK. The expectation is that the user captures DOUT[13:0], FV, and LV using the rising edge of PIXCLK.

See Figure 12 below and Table 9 on page 27 for I/O timing (AC) characteristics.

Figure 12:   I/O Timing Diagram

Table 9: **I/O Timing Characteristics[1]**

Symbol	Definition	Condition	Min	Typ	Max	Unit
$f_{EXTCLK1s}$	Input clock frequency		6[2]	–	64	MHz
$t_{EXTCLK1}$	Input clock period		15.6	–	166	ns
t_R	Input clock rise time		–	3	–	ns
t_F	Input clock fall time		–	3	–	ns
t_{RP}	Pixclk rise time		–	4	–	ns
t_{FP}	Pixclk fall time		–	4	–	ns
	Clock duty cycle		40	50	60	%
$t_{PIX\ JITTER}$	Jitter on PIXCLK		–	1		ns
t_{CP}	EXTCLK to PIXCLK propagation delay	Nominal voltages, PLL Disabled	–	32.4	–	ns
f_{PIXCLK}	PIXCLK frequency	Default, Nominal Voltages	6		88	MHz
t_{PD}	PIXCLK to data valid	Default, Nominal Voltages	–	2.3	–	ns
t_{PFH}	PIXCLK to FV HIGH	Default, Nominal Voltages	–	5.7	–	ns
t_{PLH}	PIXCLK to LV HIGH	Default, Nominal Voltages	–	5.5	–	ns
t_{PFL}	PIXCLK to FV LOW	Default, Nominal Voltages	–	4.3	–	ns
t_{PLL}	PIXCLK to LV LOW	Default, Nominal Voltages	–	4.6	–	ns
C_{LOAD}	Output load capacitance		–	<10	–	pF
C_{IN}	Input pin capacitance		–	2.5	–	pF

Notes: 1. I/O timing characteristics are measured under the following conditions:
   a. Temperature is 25°C ambient
   b. 10 pF load
   c. 1.8 V I/O supply voltage
2. When using a 1 MHz two-wire interface clock, the minimum clock frequency is 16 MHz.

Table 10: **Parallel 12-bit 3-exposure HDR, Tint**
All images taken in midlevel ambient lighting conditions, 2x gain, 1 ms integration time, 25C.

Current Type	Condition	Symbol	Voltage	Min	Typ	Max
Analog Operating Current	Streaming Full Res	IAA	2.8		59.21	
Digital Operating Current	Streaming Full Res	IDD	1.2		134.71	
I/O Supply Current	Streaming Full Res	IDD_IO/ IDD_IO_PHY	1.8		11.02	
PHY Supply Current	Streaming Full Res	IDD_PHY	1.2		3.51	
Pixel Supply Current	Streaming Full Res	IAA_PIX	2.8		12.02	
SLVS Supply Current	Streaming Full Res	IDD_SLVS	1.2		-0.01	

Note: Operating currents measured under the following conditions:
   a. VAA and VAA_PIX are tied together
   b. VDD_IO_PHY and VDD_IO are tied together
   c. PLL enabled and PIXLCK set to 88 MHz
   d. 3-exposure 12-bit Parallel mode at 33 fps
   e. Tj = 25°C

Table 11:   HiSPi HiVCM 16-bit 3-exposure HDR

Current Type	Condition	Symbol	Voltage	Min	Typ	Max
Analog Operating Current	Streaming Full Res	I_{AA}	2.8		65.87	
Digital Operating Current	Streaming Full Res	I_{DD}	1.2		148.35	
I/O Supply Current	Streaming Full Res	I_{DD_IO} / $I_{DD\_IO\_PHY}$	1.8		38.03	
PHY Supply Current	Streaming Full Res	I_{DD_PHY}	1.8		13.05	
Pixel Supply Current	Streaming Full Res	I_{AA_PIX}	2.8		13.75	
SLVS Supply Current	Streaming Full Res	I_{DD_SLVS}	1.2		0.2	

Note: Operating currents measured under the following conditions
a. V_{AA} and V_{AA}_PIX are tied together
b. V_{DD}_IO_PHY and V_{DD}_IO are tied together
c. PLL enabled and PIXLCK set to 88 MHz
d. 4-lane 3-exposure 16-bit HiSPi HiVCM mode at 40 fps
e. Tj = 25°C

Table 12:   HiSPi SLVS 16-bit 3-exposure HDR, 40 FPS, 1 ms tint, 2x gain

Current Type	Condition	Symbol	Voltage	Min	Typ	Max
Analog Operating Current	Streaming Full Res	I_{AA}	2.8		65.87	
Digital Operating Current	Streaming Full Res	I_{DD}	1.2		148.43	
I/O Supply Current	Streaming Full Res	I_{DD_IO} / $I_{DD\_IO\_PHY}$	1.8		31.52	
PHY Supply Current	Streaming Full Res	I_{DD_PHY}	1.2		13.07	
Pixel Supply Current	Streaming Full Res	I_{AA_PIX}	2.8		13.75	
SLVS Supply Current	Streaming Full Res	I_{DD_SLVS}	1.2		-0.01	

Note: Operating currents measured under the following conditions
a. V_{AA} and V_{AA}_PIX are tied together
b. V_{DD}_IO_PHY and V_{DD}_IO are tied together
c. PLL enabled and PIXLCK set to 88 MHz
d. 4-lane 3-exposure 16-bit HiSPi SLVS mode at 40 fps
e. Tj = 25°C

Table 13:   MIPI 16-bit 3-exposure HDR,

Current Type	Condition	Symbol	Voltage	Min	Typ	Max
Analog Operating Current	Streaming Full Res	I_{AA}	2.8		65.89	
Digital Operating Current	Streaming Full Res	I_{DD}	1.2		149.35	
I/O Supply Current	Streaming Full Res	I_{DD_IO} / $I_{DD\_IO\_PHY}$	1.8		0.07	
PHY Supply Current	Streaming Full Res	I_{DD_PHY}	1.8		10.37	
Pixel Supply Current	Streaming Full Res	I_{AA_PIX}	2.8		13.76	
SLVS Supply Current	Streaming Full Res	I_{DD_SLVS}	1.2		8.29	

Note: Operating currents measured under the following conditions
a. V_{AA} and V_{AA}_PIX are tied together
b. V_{DD}_IO_PHY and V_{DD}_IO are tied together
c. PLL enabled and PIXLCK set to 88 MHz
d. 4-lane 3-exposure 16-bit MIPI mode at 40 fps
e. Tj = 25°C

HiSPi Electrical Specifications

The ON Semiconductor AR0231AT sensor supports both SLVS and HiVCM HiSPi modes. Please refer to the High-Speed Serial Pixel (HiSPi) Interface Physical Layer Specification v2.00.00 for electrical definitions, specifications, and timing information. The V_{DD}_SLVS supply in this datasheet corresponds to V_{DD}_TX in the HiSPi Physical Layer Specification. Similarly, V_{DD} is equivalent to V_{DD}_HiSPi as referenced in the specification. The DLL as implemented on AR0231AT is limited in the number of available delay steps and differs from the HiSPi specification as described in this section.

Table 14: Channel Skew
Measurement Conditions: V_{DD}_HiSPi = 1.8V; $V_{DD}\_HiSPi\_TX$ = 0.4V; Data Rate =480 Mbps; DLL set to 0

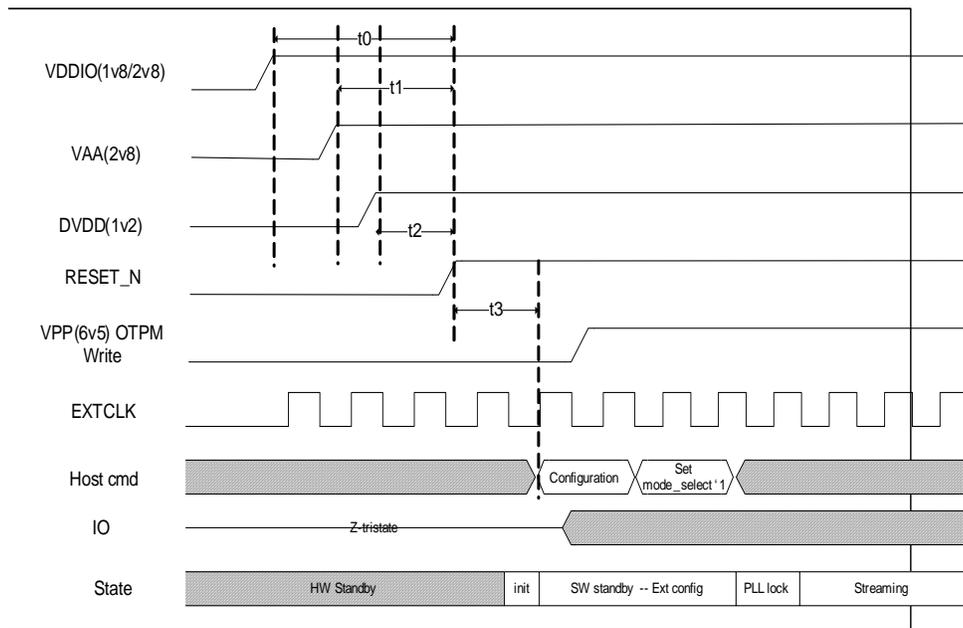| Data Lane Skew in Reference to Clock	tCHSKEW1PHY	-150	ps

Power-On Reset and Standby Timing

Power-Up Sequence

A typical power-up sequence:

1. Set RESET_BAR low
2. Power up supplies (except VPP should be kept low).
3. Wait for current to be applied on t0, t1, t2, controlled by external supply slew rate (See Figure 13).
4. When external supplies valid, set RESET_BAR high.
5. HOST config through IIC.
6. Set STREAMING bit.
7. PLL internally enables and locks.
8. AR0231 enters streaming mode.

Figure 13:   Initial Power-Up Sequence

Table 15:   AR0231 Pin List

PIN Name	iBGA Pin	Type	Descriptions	Comments
EXTCLK	B4	Input	Master input clock. PLL input clock.	Connect to clock source. Min and Max frequency depends upon output port and clocking method.
RESET_BAR	C5	Input	Asynchronous active-low reset.	Connect to host.
S$_{CLK}$	H8	Input	CCI clock for access to control and status registers.	Connect to host.
S$_{DATA}$	H9	Input/Output	CCI data for reads from and writes to control and status registers.	Connect to host.
S$_{ADDR}$0	K9	Input	CCI interface device address select bit 0.	Selects CCI address. 000b sets the address to 0x20/ 0x21. 001b sets the address to 0x30/ 0x31. Connect to V$_{DD}$_IO or D$_{GND}$ accordingly.
S$_{ADDR}$1	K8	Input	CCI interface device address select bit 1.	
S$_{ADDR}$2	K7	Input	CCI interface device address select bit 2.	
PIXCLK	F2	Output	Parallel data output pixel clock.Used to qualify the LINE_VALID, FRAME_VALID and DOUT13 to DOUT0 outputs.	Connect to host/receiver or can be left floating if not used. Use D$_{OUT}$[11:0] for 12-bit parallel configuration.
FRAME_VALID	G3	Output	Parallel data output FRAME_VALID output. Qualified by PIXCLK.	
LINE_VALID	G4	Output	Parallel data output LINE_VALID output. Qualified by PIXCLK.	
D$_{OUT}$13	J2	Output	Parallel data output pixel data bit 13. Qualified by PIXCLK.	Connect to host/receiver or can be left floating if not used. Use D$_{OUT}$[11:0] for 12-bit parallel configuration.
D$_{OUT}$12	J3	Output	Parallel data output pixel data bit 12. Qualified by PIXCLK.	
D$_{OUT}$11	H2	Output	Parallel data output pixel data bit 11. Qualified by PIXCLK.	
D$_{OUT}$10	H3	Output	Parallel data output pixel data bit 10. Qualified by PIXCLK.	
D$_{OUT}$9	G2	Output	Parallel data output pixel data bit 9. Qualified by PIXCLK.	
D$_{OUT}$8	F3	Output	Parallel data output pixel data bit 8. Qualified by PIXCLK.	
D$_{OUT}$7	E3	Output	Parallel data output pixel data bit 7. Qualified by PIXCLK.	
D$_{OUT}$6	E2	Output	Parallel data output pixel data bit 6. Qualified by PIXCLK.	
D$_{OUT}$5	D3	Output	Parallel data output pixel data bit 5. Qualified by PIXCLK.	
D$_{OUT}$4	D2	Output	Parallel data output pixel data bit 4. Qualified by PIXCLK.	
D$_{OUT}$3	C3	Output	Parallel data output pixel data bit 3. Qualified by PIXCLK.	
D$_{OUT}$2	C4	Output	Parallel data output pixel data bit 2. Qualified by PIXCLK.	
D$_{OUT}$1	B3	Output	Parallel data output pixel data bit 1. Qualified by PIXCLK.	

Table 15: **AR0231 Pin List (continued)**

PIN Name	iBGA Pin	Type	Descriptions	Comments
D$_{OUT0}$	B2	Output	Parallel data output pixel data bit 0. Qualified by PIXCLK.	Connect to host/receiver or can be left floating if not used. Use D$_{OUT}$[11:0] for 12-bit parallel configuration.
CLK_P	A8	Output	Differential Mipi/HiSpi serial clock.	Connect to host/receiver or can be left floating if not used. Use DATA0 for 1 lane configuration or DATA0 and DATA1 for 2 lane configuration.
CLK_N	B8	Output	Differential Mipi/HiSpi serial clock.	
DATA3_P	B10	Output	Differential Mipi/HiSpi serial data lane 3.	
DATA3_N	A10	Output	Differential Mipi/HiSpi serial data lane 3.	
DATA2_P	A9	Output	Differential Mipi/HiSpi serial data lane 2.	
DATA2_N	B9	Output	Differential Mipi/HiSpi serial data lane 2.	
DATA1_P	B7	Output	Differential Mipi/HiSpi serial data lane 1.	
DATA1_N	A7	Output	Differential Mipi/HiSpi serial data lane 1.	
DATA0_P	A6	Output	Differential Mipi/HiSpi serial data lane 0.	
DATA0_N	B6	Output	Differential Mipi/HiSpi serial data lane 0.	
TEST	K2	Input	Enable manufacturing test modes.	Tie to D$_{GND}$.
ATEST1	G8	Input/Output	Analog manufacturing test access	Leave unconnected.
ATEST2	G9	Input/Output	Analog manufacturing test access	
ATEST3	G10	Input/Output	Analog manufacturing test access	
ATEST4	G11	Input/Output	Analog manufacturing test access	
GPIO0	J9	Input/Output	GPIO Pin 0	GPIO[2:0] can be left unconnected if not used. GPIO3 should be tied to D$_{GND}$ if not used.
GPIO1	J8	Input/Output	GPIO Pin 1	
GPIO2	K11	Input/Output	GPIO Pin 2	
GPIO3	K10	Input/Output	GPIO Pin 3	
SYS_CHECK	J10	Output	5th GPIO pin is dedicated	Leave unconnected if not used.
TEMP_FLAG	H10	Output	Temperature monitoring flag	Leave unconnected.
D$_{GND}$	E1, G1, J1, A2, K3, L3, D4, E4, F4, H4, J4, K4, B5, D5, E5, F5, G5, H5, J5, K5, D6, E6, F6, G6, H6, J6, K6, L6, D7, E7, F7, G7, H7, J7, C8, D8, E8, F8, L9, C10	Power	Digital ground.	
V$_{DD}$	B1, F1, K1, L2, A3, A4, L5, L8, L10, B11, J11	Power	Core Digital power.	
V$_{DD}$_PHY	C7	Power	PHY Digital power.	Connect to V$_{DD}$

Table 15:   AR0231 Pin List (continued)

PIN Name	iBGA Pin	Type	Descriptions	Comments
V_{DD_IO}	A1, D1, H1, L1, L4, A5, L7, A11, H11, L11	Power	Digital I/O power.	
A_{GND}	C2, D9, E9, F9, F11	Power	Analog ground.	
V_{AA}	C1, D10, E10, F10, E11	Power	Analog power.	
V_{AA_PIX}	D11	Power	Analog pixel array power.	Connect to V_{AA}
$V_{DD\_IO\_PHY}$	C9	Power	Power to MIPI and HiSPi PHYs.	Use 1.8V nominal for HiSPi HiVCM or Sub-LVDS. Use 1.8V or 2.8V nominal for MIPI or HiSPi SLVS. Tie to V_{DD_IO} when Parallel interface is used.
V_{DD_SLVS}	C6	Power	Reference voltage for HiSPi serial interface.	Set according to desired HiSPi output common mode voltage. Use 0.4V nominal for HiSPi SLVS, otherwise use 1.2V nominal. Tie to V_{DD} when MIPI is being used
V_{PP}	C11	Power	High voltage supply for programming OTPM.	Leave unconnected.

Package Drawing

AR0231AT: 1/2.7-Inch 2.3 Mp Digital Image Sensor
Package Drawing

Advance

NOTES

1	DIMENSIONS IN MM. DIMENSIONS IN ( ) ARE FOR REFERENCE ONLY.
2	ENCAPSULANT: EPOXY.
3	SUBSTRATE MATERIAL: EPOXY LAMINATE 0.25 THICKNESS.
4	LID MATERIAL: BOROSILICATE GLASS 0.4 THICKNESS.
5	SOLDER BALL MATERIAL: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu). SOLDER BALL PAD: ø0.4 SMD
6	MAXIMUM ROTATION OF OPTICAL AREA RELATIVE TO PACKAGE EDGES: 1°. MAXIMUM TILT OF OPTICAL AREA RELATIVE TO SUBSTRATE PLANE D: 25 MICRONS MAXIMUM TILT OF COVER GLASS RELATIVE TO OPTICAL AREA PLANE E: 50 MICRONS.

SEATING PLANE

0.4±0.05

121X ø0.5±0.05

11±0.075

BALL A1 ID

0.8 TYP

10±0.075

0.8 TYP

BOTTOM SIDE VIEW

0.475±0.05

0.75±0.05

BALL A1 ID

(0.125)

SECTION A-A

5.5±0.075

(1.150)

(1.150)

5±0.075

FIRST CLEAR PIXEL

(3.636)   7.7±0.10

PACKAGE CENTER = DIE CENTER (0,0)

OPTICAL CENTER = (600um, 165um)

OPTICAL AREA (1932H X 1212V)

(5.796)

8.7±0.10

TOP SIDE VIEW

Revision History

- Updated Table 1, "Key Parameters," on page 1
- Updated "General Description," on page 6
- Added note to Figure 3: "Typical Configuration, 4-Lane MIPI," on page 9
- Updated "Frame Rate" on page 12
- Updated "High Dynamic Range" on page 12
- Updated "LED Flicker Mitigation (LFM)" on page 13
- Updated "Context Switching and Register Updates" on page 14
- Updated "Embedded Data and Statistics" on page 15
- Updated "Defective Pixel Tracking/Correction" on page 17
- Updated "Analog/Digital Gains" on page 17
- Updated "Parallel Pixel Output Port" on page 19
- Added note to Table 9, "I/O Timing Characteristics1," on page 27
- Updated Table 15, "AR0231 Pin List," on page 31

- Converted to ON Semiconductor template
- Changed title
- Updated "Features," on page 1
- Added "Applications," on page 1
- Added "General Description," on page 1
- Updated Table 1, "Key Parameters," on page 1
- Updated Table 2, "Available Part Numbers," on page 2
- Updated "General Description," on page 6
- Updated "Functional Overview," on page 6
- Replaced "Figure 1: Typical Configuration" with "Figure 1: "Typical Configuration, Parallel," on page 7 and Figure 2: "Typical Configuration, 4-Lane HiSPi," on page 8
- Added "Pixel Data Format," on page 10
- Updated "Default Readout Order" on page 11
- Updated "LED Flicker Mitigation (LFM)" on page 13
- Updated "High Dynamic Range" on page 12
- Added "Dual Conversion Gain (DCG)" on page 13
- Updated "Multi-camera Synchronization" on page 13
- Updated Figure 7: "Typical Stereo Camera Configuration," on page 14
- Added "Slave Mode" on page 14
- Updated "Context Switching and Register Updates" on page 14
- Updated "Embedded Data and Statistics" on page 15
- Added "Analog/Digital Gains" on page 17
- Added "Skipping/Binning Modes" on page 17
- Updated Table 4, "ASIL Support Features," on page 18
- Updated Table 5, "HiSPi Protocol Support," on page 19
- Updated "MIPI CSI-2 Pixel Output Port" on page 19
- Added Table 6, "MIPI Protocol Support," on page 19
- Updated "Parallel Pixel Output Port" on page 19
- Updated "Line Interleaved Output" on page 20
- Updated Figure 9: "Multi-Exposure Frame Example," on page 20

- Updated Figure 10: "Line by Line Readout," on page 22
- Updated Table 7, "Electrical Specifications," on page 23
- Updated "Power Up" on page 23
- Added "Two-Wire Serial Register Interface" on page 24
- Added "I/O Timing" on page 26
- Updated Table 9, "I/O Timing Characteristics1," on page 27
- Updated Table 10, "Parallel 12-bit 3-exposure HDR, Tint," on page 27
- Updated Table 11, "HiSPi HiVCM 16-bit 3-exposure HDR," on page 28
- Updated Table 12, "HiSPi SLVS 16-bit 3-exposure HDR, 40 FPS, 1 ms tint, 2x gain," on page 28
- Updated Table 13, "MIPI 16-bit 3-exposure HDR,," on page 28
- Added "HiSPi Electrical Specifications" on page 29
- Added "Power-On Reset and Standby Timing" on page 30
- Added "Power-Up Sequence" on page 30
- Added Table 15, "AR0231 Pin List," on page 31
- Added "Package Drawing" on page 34

Rev. 1 . . . . **8/19/13**

- Initial release