AGV Vision Perception kits
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1. Introduction

The AGV Vision Perception kits enable the 360 degree Surround View and Front smart camera functions for ADAS applications, which consists of 96Boards CE based Ultr96, 96Boards Vision Mezzanine Boards and up to 6pcs Automotive Grade GMSL Camera modules and cables. The total solution hardware design and source code are open and can be accessed from the 96Boards websites. The whole kit is shown as image 1 and 2.

1. AGV Vision Perception Kit image Top View
2. AGV Vision Perception Kit image Bottom View

The other one or 2 smart front cameras can identify road markings, traffic signals, and traffic lights, even recognize objects and provide data that facilitates their identification. The 96Boards Vision Mezzanine Board has 2*Maxim Deserializer Max9286 which can support up to 6* 1.3M pixel camera modules, the HS/LS interface is compliant with 96Boards Mezzanine Boards High speed and low speed connector which can match other 96Boards.AI boards such as
Ultra96, RB3 (Qualcomm Snapdragon845), TB-96 (Rockchip RK3399Pro) and so on. This Vision Board kit adapts Ultra96 for reference. The camera modules with Fakra interface modules can be Onsemi AR0143RGGB (720P), and AR0231AT (1080P) etc.

2. Vision Board Specifications and features

2.1 Specification

The Caiqi and AutoCore Multi-Camera Vision Boards is compliant with 96Board Mezzanine standards, supporting up to 6 high definition resolution (720p) camera modules using MAXIM Integrated’s MAX9286 GMSL (Gigabit Multimedia Serial Link) technology. GMSL is being widely used in the automotive industry for in-vehicle high speed communication of video streams. Making use of low-cost coax cable customized in length, GMSL meets the electromagnetic compatibility (EMC) requirements of the automotive industry.

The design supports 2 four-channel-Fakra Camera connectors. The whole board image is as below.

- **Input**:
  a. 2*4Ports input High-Speed FAKRA Mini (HSFM) connectors
  b. DC12V@2A DC Jack input
- **2*Quad GMSL Deserializer by MAXIM Integrated (MAX9286)**
  a. Support for 2*4 ON Semiconductor image sensors modules (AR0231AT+AP0202+MAX96705)
- Connect with 96Boards through HS/LS connector using the 60pin and 40 pin connector.
- **Output**:
  a. Connect with 96Boards through HS/LS connector using the 60pin and a 40 pin connector.
  b. 2*FD CAN ports output (converting the two SPI (SPI ports form HS/LS connector) to CAN bridge)
  d. UART to USB debug connector
  e. ETH port (converting from USB2.0 of the HS connector to ETH bridge)
  f. Two CSI-2 connector interface: two 4Lanes CSI-2 connector from MAX9286 output
2.2. Vision Mezzanine Kit

The Vision Boards kit include below items:
Vision Board: CES-FMC-MULTICAM 1PCS
12V@2A AC-DC adaptor: 1pcs
FAKRA Cable: LM4-CA1434-1700-Z-ZZZZ 2pcs
Camera Module: SG1-AR0143RGB-0101-GMSL-HXXX
(Modular Automotive Reference System) based Sensing-world camera modules,
Integrated MAXIM MAX96705 GMSL Serializer board and the ON Semiconductor
AR0143RGB image sensor board and also ISP AP0202(The ISP inside the
Camera Modules can be optional).
2.3 system architecture

The system architecture is as below diagram 1

1. Vision Board system diagram
3. Vision board Hardware design

3.1 Schematics

Detailed schematics is as Vision_GMSL_2_CSI_Final.pdf
4. Ultra96

Ultra96 is 96Boards AI version which works as the sensor perception Board using Xilinx ZU3EG, For more detailed information please refer to https://www.96boards.org/product/ultra96/
5. AGV perception Boards user guide

5.1 Source code:

e. Integration with Vision perception unit supporting up to 6 channel independent camera sensors, the Linux kernel build up on Ultra96 Boards is as below:

Kernel branch: https://github.com/xlnx-hyunkwon/linux-xlnx/tree/hyunk/vision-wip-5.4-next

Following modules are used on the vision board:

ISP - AP0101
Serializer - MAX9286
De-serializer - MAX96705

Drivers for the above modules can be found below:

MAX9286: https://github.com/xlnx-hyunkwon/linux-xlnx/blob/hyunk/vision-wip-5.4-next/drivers/media/i2c/max9286.c

MAX96705: https://github.com/xlnx-hyunkwon/linux-xlnx/blob/hyunk/vision-wip-5.4-next/drivers/media/i2c/max96705.c

AP0202AT: https://github.com/xlnx-hyunkwon/linux-xlnx/blob/hyunk/vision-wip-5.4-next/drivers/media/i2c/ap0202at.c
AP0101: need to be added

The devicetree reference can be found here:
https://github.com/xlnx-hyunkwon/linux-xlnx/blob/hyunk/vision-wip-5.4-next/arch/arm64/boot/dts/xilinx/pl-mipi-4chan.dts#L394

For integrating the software stack with any 96Boards, the MIPI CSI node of the SoC needs to be passed to the remote-endpoint property of the max9286_out node in dts. Also the lane count needs to be specified as per the SoC limitations in data-lanes property.
The sensor, serializer, deserializer nodes need to be listed under corresponding i2c nodes in devicetree. For connecting 6 cameras, 4 needs to be specified under LS-I2C0 and remaining 2 under LS-I2C1.

The vision board outputs **YV422** images at 50MHz pixel rate.

**Upstream Status:**

Currently MAX9286 driver is submitted and getting reviewed in LKML [1]. Rest of the drivers will be submitted once MAX9286 finds its way.

5.2 How to start

The Vision Board is designed to work with 96Boards CE standard development platforms such as Ultra96/RK3399Pro platforms/Snapdragon845/HiKey etc. compliant to 96Boards Consumer Edition specification. Vision Mezzanine board converts 6 channel GMSL camera modules to two CSI-2 interfaces through HS and LS connector to 96Boards CE platforms. Here is the example of

a. Power and cameras module connections

- Connect the dedicated 12V adaptor.
- Connect the 6 Camera modules below.
b. Switch configurations:
The switch SW500/SW400 should be confined as below:
HIM=1(NO), BWS=0(OFF), MODE_SEL=0 (OFF)
c. I2C access for Max9286 Setting

Both I2C0_SCL/I2C0_SDA from Low Speed Expansion Connector and I2C2_SCL/I2C2_SDA can be connected to MAX1_SCL/MAX1_SDA of MAX9286 U500. Both I2C1_SCL/I2C1_SDA from Low Speed Expansion Connector and I2C3_SCL/I2C3_SDA can be connected to MAX2_SCL/MAX1_SDA of MAX9286 U400. Also the I2C0_SCL/I2C0_SCL can be connected to external I2C of MCU for some debug or test. Below are the pictures.
d. Camera Module and Max9286 Initialization:

There are three I2C devices that need to be configured.
MAX9286, 7bit Physical address is 0x6A, single byte register address
MAX96705, 7bit Physical address is 0x40, single byte register address
AP0202, 7bit Physical address is 0x5D, dual bytes register address

/******camera information*******
Camera sensor: Onsemi AR0231AT
Camera ISP: Onsemi AP0202AT
Camera Ser: GMSL Max96705
I2C address: Max96705 is 0x80 (8bit), AP0202 is 0xBA(8bit)
Pclk = 99Mhz
There are two output resolution, 720p/1080p 22fps
**/

/******GMSL configuration*******
It is recommended to delay 50-100ms between two reg operations.
*/

Firstly we need initialize the MAX9286 and MAX96705:

```
    wr9286Reg1 (0x0A,0xFF); // enable forward/reverse control channel
    wr9286Reg1 (0x34,0xB6); // enable I2C local acknowledge
    wr9286Reg1 (0x15,0x03); // disable CSI-2 output
    wr9286Reg1 (0x12,0xF3); // CSI-2 output use YUV422 8bit
    wr9286Reg1 (0x00,0x81); // enable input link 0
```
If we can access the register 0x15 Max96705 successfully, it can approve that the Camera PCLK can work normally, and output a valid image.

/******ISP configuration******
- If the camera outputs 720p by default, the following wrAt0202Reg configurations do not need to be used;
- change the output from 1080p to 720p;
- After GMSL initialization, the AP0202 needs to configure the following registers;
- AP0202 I2C device address : 0x5D (7bit)
*/
Secondly we need config the AP0202 register, each register of AP0202 configuration needs to be delayed for about 50ms’s delay.
AP0202 I2C device address : 0x5D (7bit)

SYNCDELAY;           // Appropriate delay required
    maxAP0202_write(0xC804 , 0x0040 );//# CAM_SENSOR_CFG_Y_ADDR_START
SYNCDELAY;
    maxAP0202_write(0xC806 , 0x0004   );//#
CAM_SENSOR_CFG_X_ADDR_START
SYNCDELAY;
    maxAP0202_write(0xC808 , 0x0477    );//# CAM_SENSOR_CFG_Y_ADDR_END
SYNCDELAY;
    maxAP0202_write(0xC80A , 0x0783    );//# CAM_SENSOR_CFG_X_ADDR_END
SYNCDELAY;
    maxAP0202_write(0xC810 , 0x09C2    );//# CAM_SENSOR_CFG_FINE_INTEG_TIME_MIN
SYNCDELAY;}
maxAP0202_write(0xC812 , 0x09C2 );//
CAM_SENSOR_CFG_FINE_INTEG_TIME_MAX
SYNCDELAY;
maxAP0202_write(0xC814 , 0x048D );//
CAM_SENSOR_CFG_FRAME_LENGTH_LINES
SYNCDELAY;
maxAP0202_write(0xC816 , 0x09C2 );//
CAM_SENSOR_CFG_LINE_LENGTH_PCK
SYNCDELAY;
maxAP0202_write(0xC8A0 , 0x0000 );//# CAM_CROP_WINDOW_XOFFSET
SYNCDELAY;
maxAP0202_write(0xC8A2 , 0x0000 );// CAM_CROP_WINDOW_YOFFSET
SYNCDELAY;
maxAP0202_write(0xC8A4 , 0x0780 );// CAM_CROP_WINDOW_WIDTH
SYNCDELAY;
maxAP0202_write(0xC8A6 , 0x0438 );// CAM_CROP_WINDOW_HEIGHT
SYNCDELAY;
maxAP0202_write(0xCAE4 , 0x0500 );// CAM_OUTPUT_WIDTH
SYNCDELAY;
maxAP0202_write(0xCAE6 , 0x02D0 );// CAM_OUTPUT_HEIGHT
SYNCDELAY;
maxAP0202_write(0xfc00 ,0x2800 );// 16bit reg delay 100ms
SYNCDELAY;
maxAP0202_write(0x0040 ,0x8100 );// 16bit reg delay 100ms
SYNCDELAY;

Some tested waveform for reference:

Read MAX9286(0x00,0x81) :

![Waveform Image]
Read MAX96705 (0x04,0x87) : (MAX9286 response ACK:(0x34,0xBB), enable I2C local acknowledge)

After power on, we can't read Max96705 if not setting MAX9286 0x34 register.
6. Summary
The Vision Boards and 6 Cameras support 96Boards.AI with AI inference
capabilities (such as Ultra96, RK3399Pro, Snapdragon845 etc) for the Visual
perception. This will be integrated to the Heterogeneous computing platform
for AD/ADAS, AGV and Robotics platforms through Ethernet as below.
Please contact contact@autocore.ai for more details.

Limitation:
For the Camera modules selection, it can be changed according to
customer’s requirements.
Here are some options:
AR0231AT (Onsemi sensor) + AP0202 (Onsemi ISP) + MAX96705 modules
with 1080P resolution and low light performance
SG1-AR0143RGB (Onsemi sensor) - AP0101 (Onsemi ISP) - GMSL-HXXX with 720P
resolution and lower price.
Since there are some bandwidth limitation on the MAX9286, which can only
support 1280 width pixels, so even we choose bigger resolution camera module
such as AR0143, we still need to do some limitation, this can only be resolved
using the next De-serializer generations from Maxim or TI.
Frame Combination

The deserializer receives serialized data from up to four input links. The maximum active frame width accepted is 1280 pixels. The input frames are synchronized, and combined into a single (4 x W) x H or W x (4 x H) frame (Figure 12). The output data rate is N times the input data rate where N is the number of active serial links.

Table 26. Suggested Sensor Configurations for GMSL

<table>
<thead>
<tr>
<th>SENSOR</th>
<th>CONFIGURATION</th>
</tr>
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<tbody>
<tr>
<td>OV10635</td>
<td>30Hz, 1280x800p (1905 x 840 with blanking), 10-bit YUV, 96MHz</td>
</tr>
<tr>
<td>OV10640</td>
<td>30Hz, 1280 x 1080p (1476 x 1106 with blanking), 12-bit RAW/12-bit HDR, 75MHz</td>
</tr>
<tr>
<td></td>
<td>60Hz, 1280 x 1080p (1476 x 1106 with blanking), 12-bit RAW, 100MHz</td>
</tr>
<tr>
<td>AR0132</td>
<td>45Hz, 1280 x 960p (1650 x 990) with blanking, 12-bit RAW data type, 74.25MHz</td>
</tr>
</tbody>
</table>