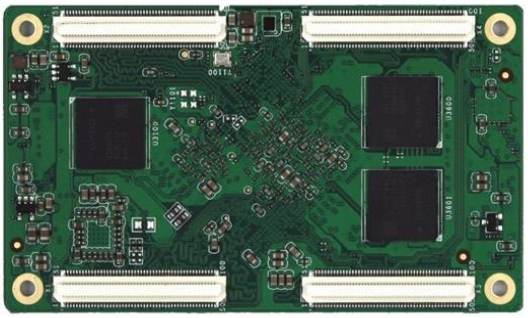
TB-96AI

（RK3399Pro Core Board）

Product SpecificationV1.0



Version	Date of Revision	Content of Revision
V1.0	2019-05-08	The first version officially released

1、Product overview

1.1 Summary

On April 1, 2019, Linaro officially released the 96 Boards System-on-Moudle (SoM) specification V1.0 in Bangkok, Thailand. On this basis, two core modules TB-96AI and TB-96AIoT, developed by Xiamen Beiqi Technology Co., Ltd., which conform to the 96 Boards SoM specification, were solemnly launched. TB-96AI uses RK3399Pro as the main control chip and TB-96AIoT uses RK1808 as the main control chip.

TB-96AI is a powerful core board for artificial intelligence. Carrier Board developed by Xiamen Beiqi Technology Co., Ltd. can form a complete development board or evaluation board; and the board customized by customers according to actual needs can directly form the industry application motherboard, which can meet industrial automation, UAV, image detection, face recognition, edge computing gateway, cluster server, Intelligent Quotient display, automatic driving, medicine. Application needs of market segments such as health care equipment, robots and intelligent retail.

1.2 Features

The following features are quoted from RockChip. If you have any questions, please contact BEIQICLOUD for more technical support.

1.2.1 Six-core 64-bit processor, superior general-purpose computing power

- Dual-core ARM Cortex-A72 MPcore processor and quad-core ARM Cortex-A53 MPcore processor are high-performance, low-power and cache application processors.
- Two CPU clusters. Big cluster with dual-coreCortex-A72 is optimized for high-performance and little cluster with quad-core Cortex-A53 is optimized for low power.
- Full implementation of the ARM architecture v8-A instruction set, ARM Neon Advanced SIMD (single

instruction, multiple data) support for accelerating media and signal processing

See RK3399Pro datasheet for more features.

1.2.2 Built-in Neural Network Processor NPU, Ultra High AI Computing Power

- Supporting 8 bit/16 bit operation, AI computing power up to 3.0 TOPs (INT8 Inference)；

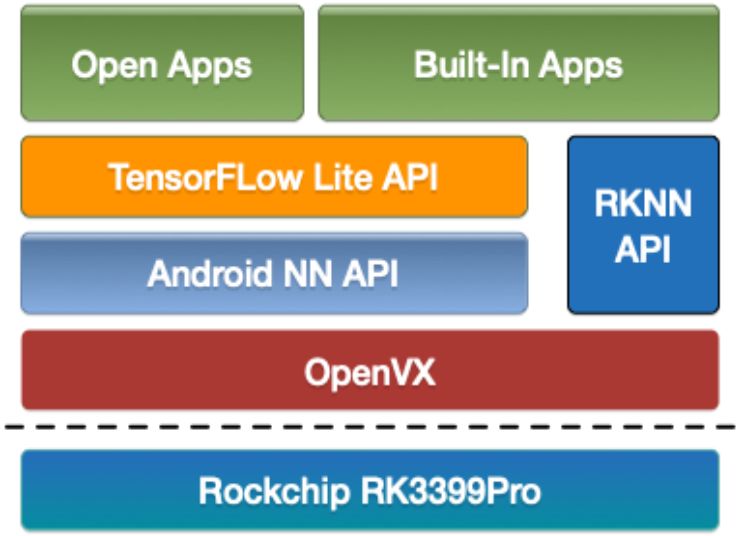
  (300 GOPs for INT16, 100 GFLOPs for FP16)

ModelType	Model Name	FPS
Image Recognition	VGG16	46.4
	ResNet50	81.2
	Inception_v4	21.7
Object Detection	YOLO_v2	43.4

Speech Recognition	DeepSpeech2**	Real time rate	0.167
		accuracy rate WER （LibriSpeech）	16.1

- Full load calculation is strong and light load operation power consumption is low.
- Compatible with Caffe/Mxnet/TensorFlow model, it can support multiple frameworks, support mainstream layer types, and add custom layer easily.
- Provide easy-to-use development tools, PC can complete model conversion, performance prediction, accuracy verification.

- Provide AI application development interface: support Android NN API, RKNN cross-platform API, Linux support TensorFlow development;



1.2.3 Powerful Multimedia Processing Performance

- Integrated quad-core ARM Mali-T860MP4 GPU, support OpenGL ES1.1/2.0/3.0, OpenCL1.2, Directx11.1, etc., with more bandwidth compression technology
- Strong hardware codec capability
  - Support 4K VP9 and 4K 10bits H265/H264 video decoding up to 60fps
  - Support 1080P multi-format video decoding (VC-1, MPEG-1/2/4, VP8)
  - Support 1080P video encoding, support H.264, VP8 format

1.2.4 Multiple video input and output interfaces

- Dual camera interface: two MIPI-CSI input interfaces with two ISP image processors
- Display output interface: Embed two VOPs, support dual-screen simultaneous/dual-screen display, and can choose to output from the following display interface.
  - MIPI-DSI×1
  - eDP×1
  - DP×1（Support progressive/interlaced, support RGB/yuv420/yuv422/yuv44format）

- HDMI×1（Support 480p/480i/576p/576i/720p/1080p/1080i/4k, support RGB format）

1.2.5 Rich expansion interface

A rich set of expansion interfaces for users to choose to support I2C, SPI, UART, ADC, PWM, GPIO, PCIe, USB3.0, I2S, etc.

- Type-C/DP×1，OTG；
- USB2.0×2，HOST；
- USB3.0×1，According to the RK3399Pro design, the NPU needs to be mounted on the USB3.0, so the USB3.0 needs to be connected back to the NPU. If you need to extend the USB3.0 interface, you need to plug in the HUB.
- SDMMC×1；
- SPI×1；
- CPU Debug UART×1，NPU Debug UART×1；
- UART×1；
- I2S×1；
- SDIO×1；
- I2C×1；
- PCIe×1；
- PWM×2；
- GPIO，For detailed GPIO definition, please refer to interface definition.；
- ADC×3，One for buttons, one for headset microphone detection, and one for user-definable use;

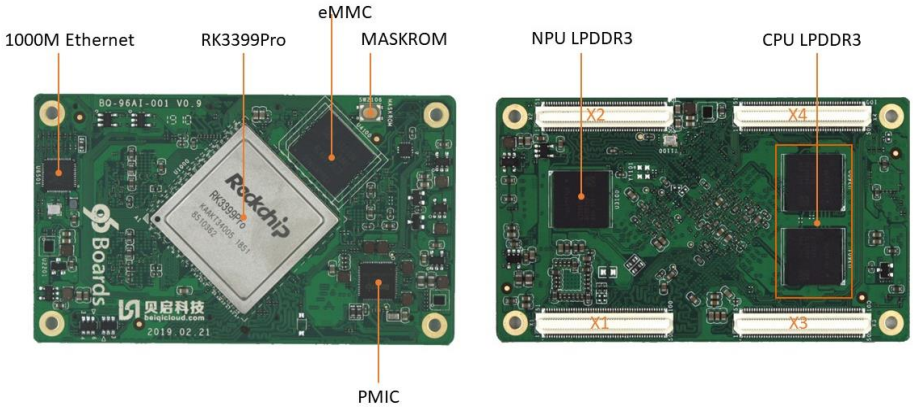
1.2.6 High-speed on-board connector for more stability and reliability

- 4 Panasonic high-speed onboard connectors for higher speed signal stability

The core board can be fixed by 4 screw posts for various working environments.

1.2.7 Ultra-high integration, ultra-small size

- The core board integrates RK3399Pro, CPU DDR, NPU DDR, eMMC, power management module, and Ethernet PHY chip. It has high integration, greatly reduces the design difficulty of the application backplane, and helps enterprises to quickly develop mass production specific application products. .



- The design size is only 85mm × 50mm, which can be more easily and flexibly deployed on various types of application boards.

1.2.8 Support for multiple operating systems

- Support Android, Linux, Ubuntu
- Support U disk upgrade through USB interface

1.2.9 Rich open materials, 96Boards community

The TB-96AI will be officially launched on Linaro's 96Boards, sharing 96Boards' rich software resources and easily communicating with developers around the world. For detailed reports, please visit Linaro's official website：https://www.linaro.org/news/linaro-announces-launch-of-96boards-system-on-module-som-specification/

- Development board / evaluation board. Visit Beiqi Technology official outlet store (Taobao store): https://shop467163226.taobao.com/, you can directly purchase TB-96AI and the matching

CarrierBoard to form a complete RK3399Pro artificial intelligence development board for Algorithm development learning or product early evaluation

- TB-96AI_RK3399Pro Core board_Product Specification.pdf
- Hardware related information.
  - Circuit schematic reference design
  - Connector PCB package
  - Core board size
  - Pin definition, interface package
- Software related information.
  - Software development guide.pdf
  - Tools. RK driver assistant, firmware upgrade tool, etc.
  - Firmware. Android firmware, Linux firmware
  - Source code. Android SDK source code

For more technical support, please contact us at service@beiqicloud.com

2、Specifications

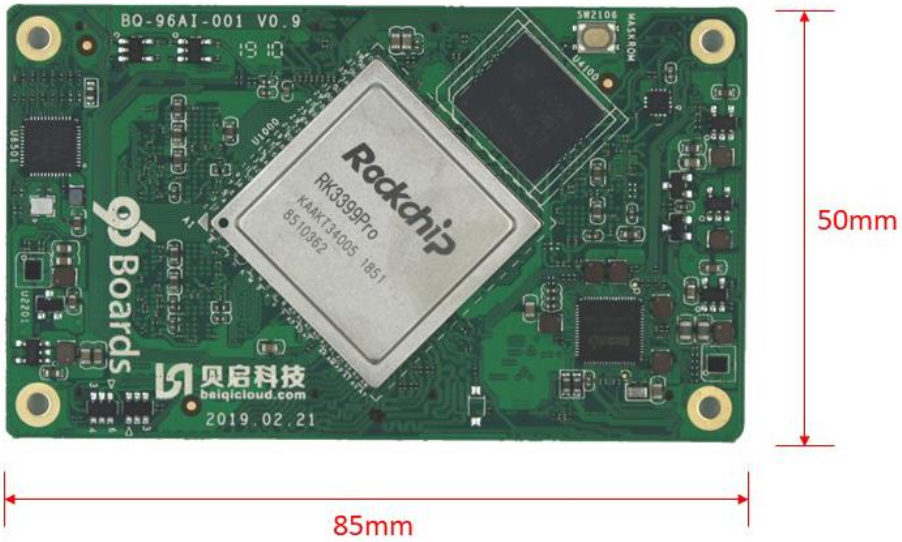
Basic Parameters	
SoC	Rockchip RK3399Pro
CPU	Dual-core Cortex-A72 up to 1.8GHz Quad-core Cortex-A53 up to 1.4GHz
GPU	ARM® Mali-T860 MP4 Quad-core GPU ➢ Support OpenGL ES1.1/2.0/3.0/3.1, OpenVG1.1, OpenCL, DX11 ➢ Support AFBC (frame buffer compression)
NPU	➢ Support 8bit/16bit computing, AI computing power up to 3.0TOPs ➢ Full load computing power, low load operation power consumption is low ➢ Compatible with Caffe/Mxnet/TensorFlow model, support multi-class framework, support mainstream layer type, easy to add custom layer ➢ Provides easy-to-use development tools, PC-based model conversion, performance estimation, and accuracy verification ➢ Provide AI application development interface: support Android NN API, provide RKNN cross-platform API, Linux support TensorFlow development;
VPU	➢ Support 4K VP9 and 4K 10bits H265/H264 video decoding, up to 60fps ➢ 1080P multi-format video decoding (WMV, MPEG-1/2/4, VP8)

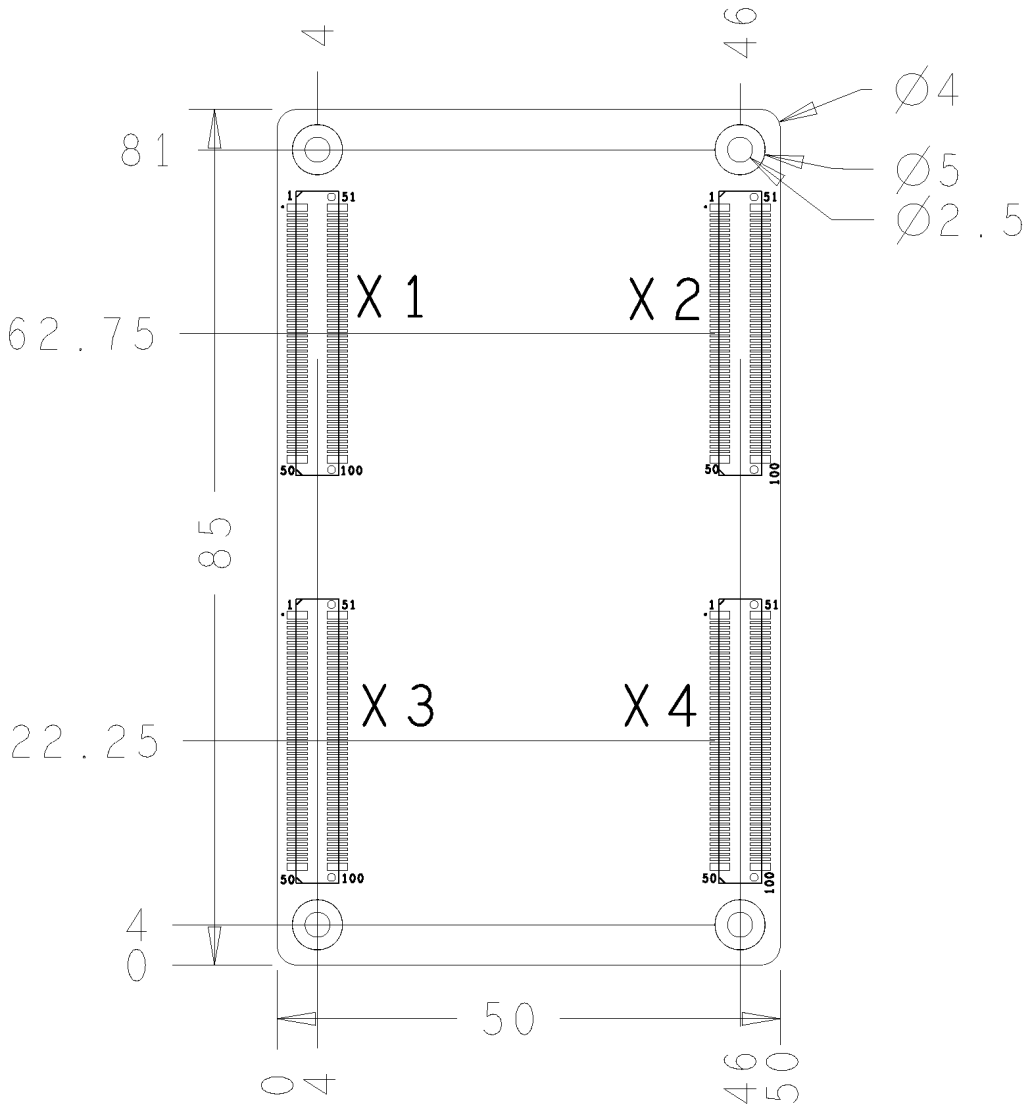
	➢ 1080P video encoding, support H.264, VP8 format ➢ Video post processor: de-interlacing, denoising, edge/detail/color optimization
RAM	Optional configuration with the following two options: ➢ 3GB LPDRR3 (CPU 2GB + NPU 1GB); ➢ 8GB LPDDR3 (CPU 4GB + NPU 4GB);
Flash	Optional configuration with the following options: ➢ 16GB eMMC ➢ 32GB eMMC ➢ 64GB eMMC ➢ 128GB eMMC
Hardware Characteristics	
Ethernet	Built-in Gigabit Ethernet PHY chip, 10/100/1000Mbps adaptive
Camera Interface	MIPI-CSI×2 , Dual camera interface (built-in dual hardware ISP, up to single 13Mpixel or dual 8Mpixel)
Display Interface	Embed two VOPs, support dual-screen simultaneous/dual-screen display, and can choose to output from the following display interface. ➢ MIPI-DSI×1 ➢ eDP×1 ➢ DP×1 ➢ HDMI × 1 (Support 480p/480i/576p/576i/720p/1080p/1080i/4k, support RGB format)

Audio Port	● I2S0： Support user extended use ● I2S1： ➢ Speaker×1 ➢ Headphone×1 ➢ MIC×1 ● I2S2： ➢ HDMI interface audio output; ➢ DP interface audio output;
Type-C	USB3.0/DisplayPort 1.2，OTG
USB	➢ USB3.0×1 (according to RK3399Pro design, NPU needs to be mounted on USB3.0, so USB3.0 needs to connect back to NPU, if you need to expand USB3.0 interface, you need external HUB)； ➢ USB2.0×2, HOST;
Extension Port	➢ SDMMC（TF Card）×1； ➢ SPI×1； ➢ UART×3，One of the CPU Debug UARTs, one NPU Debug UART; ➢ I2C×6； ➢ SDIO×1； ➢ PCIe×1； ➢ PWM×2； ➢ GPIO,For detailed GPIO definitions, please refer to the interface

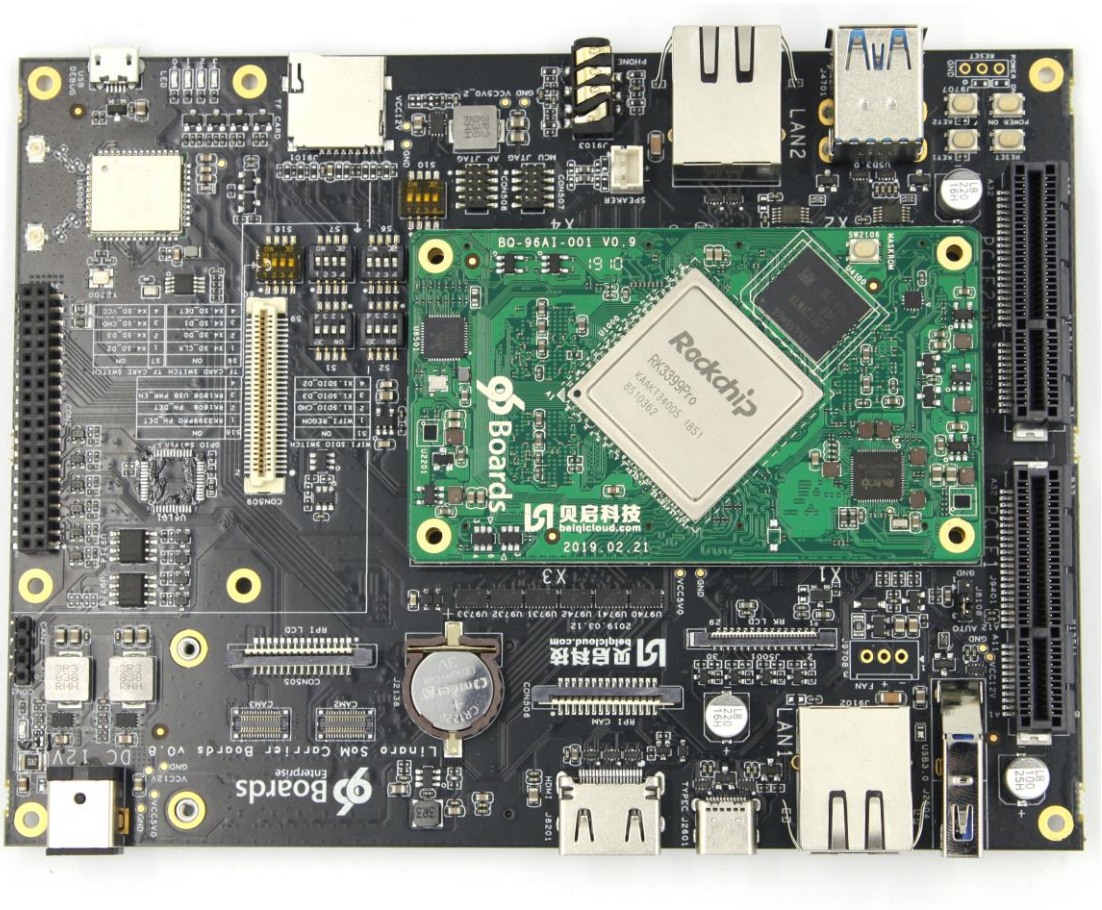
	definition; ➢ ADC×3，One for buttons, one for headset microphone detection, and one for user-definable use;
Power input	DC 5V
System Software	
System Support	Android8.1；Linux version: fedora 2.8, kernel 4.4
Software Support	➢ Support 8bit/16bit computing, AI computing power up to 3.0TOPs; ➢ Full load computing power, low load operation power consumption is low; ➢ Compatible with Caffe/Mxnet/TensorFlow model, support multi-class framework, support mainstream layer type, easy to add custom layer; ➢ Provide easy-to-use development tools, PC-side model conversion, performance estimation, and accuracy verification; ➢ Provide AI application development interface: support Android NN API, provide RKNN cross-platform API, Linux support TensorFlow development;
Other Specifications	
Size	85mm×50mm×1.6mm
PCB Specification	10 laminate
Connector	4 Panasonic 100PIN high speed connectors, type AXK6S00437YG (PIN spacing 0.5mm)

3、Structure Size



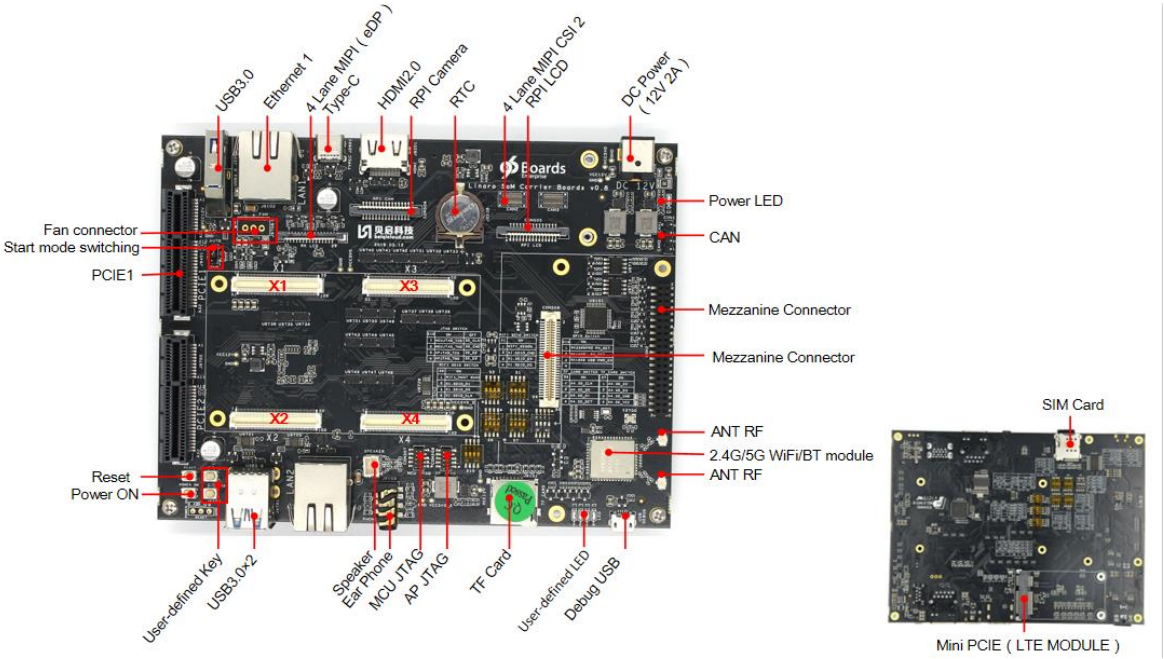


4、TB-96AI+Carrierboard Guide for use



The following figure shows the use of TB-96AI RK3399Pro SOM on the Carrier board.

The following figure shows the interfaces on the board that can be provided to TB-96AI RK3399Pro SOM



Download firmware

Connect the TYPEC to PC

Long press and hold the Maskrom button as shown in the following figure.

Insert power supply.

Interface use

Som connector: Use all of the X1,X2,X3,X4

LAN: Only can use the Ethernet1

Camera: can use CAM2 connector and RPI Camera

Wifi: Use the WIFI module on Carrier board

HDMI: HDMI2.0

PCIE: Only use the PCIE1(Different SOM hardware required)

USB: Use all of the three USB3.0

The TF card,debug usb,power key,reset key,user key,user leds,DC Jacket,Audio Jacket are common connector.

Switch

The switches for TB-96AIoT are configured as follows

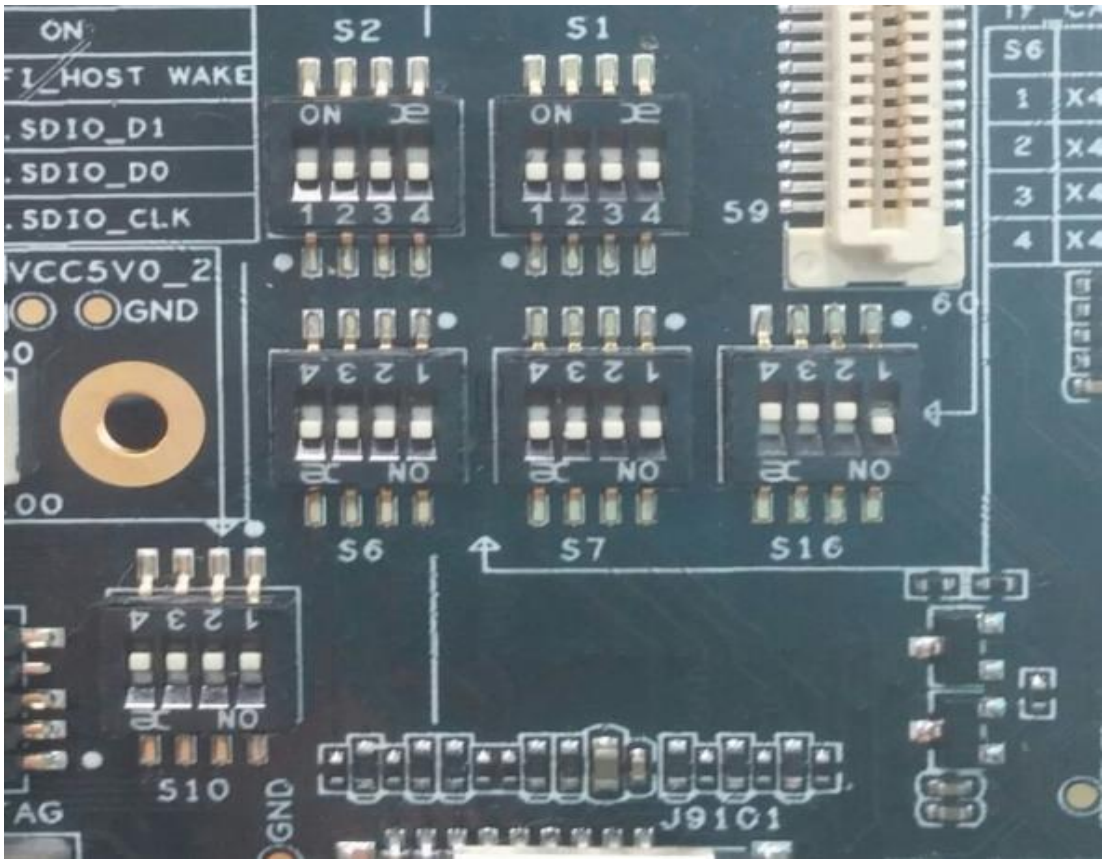
All switch on S1,S2,S8,S9,S10,S11,S12,S14,S15, configure to disconnect.

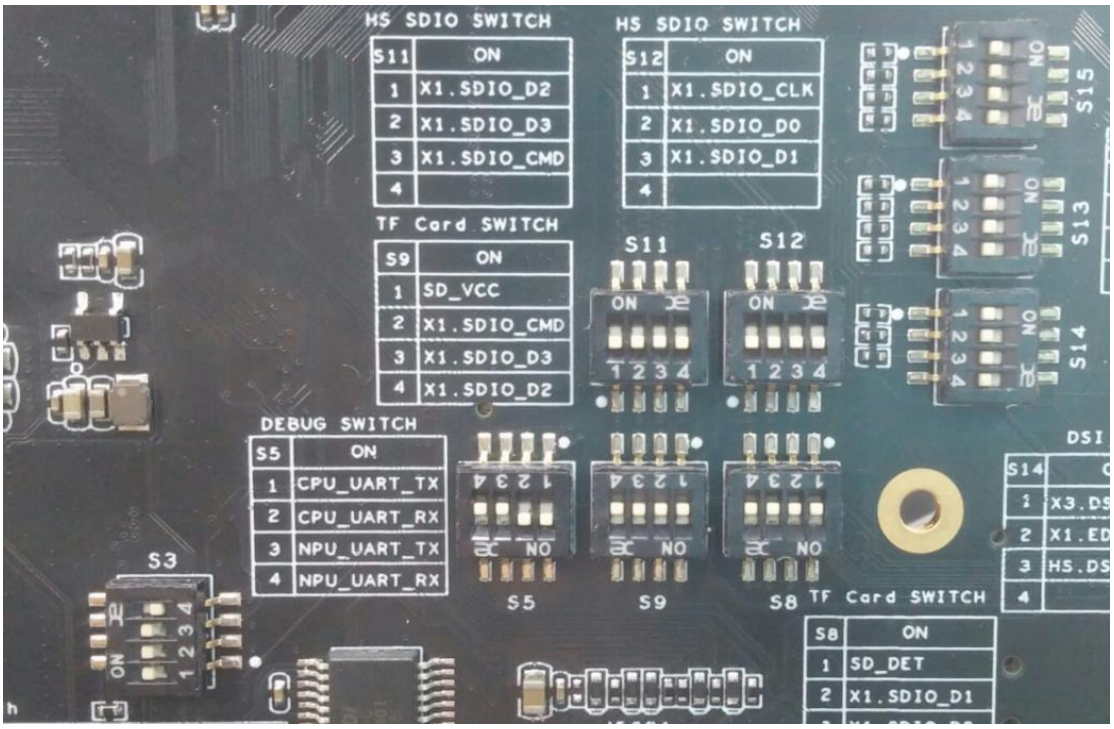
All switch on S6,S7 config to connect for TF card.

Bit1 on S16 config to connect for audio jacket

Bit1,bit2 on S5 config to connect for debug uart

Bit1,bit2,bit3 on S3 config to connect for WIFI and BT





5、Interface definition


X1
AXK6S00437YG
X2
AXK6S00437YG
X3
AXK6S00437YG
X4
AXK6S00437YG

X1 Connector					
PIN	Core board pin definition	Default function	Defual function description	IO Power domain	Pad type IO Pull
1	GND	GND	GND		
2	GND	GND	GND		
3	NC	NC	NC		
4	NC	NC	NC		
5	NC	NC	NC		
6	GND	GND	GND		
7	TYPEC0_AUXP/TYPEC0_AUXP_PD_PU	TYPEC0_SBU1_DC/TYPEC0_SBU1	TYPEC0 AUX differential TX/RX serial data		
8	TYPEC0_AUXM/TYPEC0_AUXM_PU_PD	TYPEC0_SBU2_DC/TYPEC0_SBU2	TYPEC0 AUX differential TX/RX serial data		
9	GND	GND	GND		
10	TYPEC_CC1	TYPEC_CC1	TYPEC_CC1		
11	TYPEC_CC2	TYPEC_CC2	TYPEC_CC1		
12	GND	GND	GND		
13	SDIO0_BKPWR/GPIO2_D4_d	GPIO2_D4	WIFI module power enable	1.8V	I/O DOWN
14	ISP0_SHUTTER_TRIG/ISP1_SHUTTER_TRIG/TCPD_CC0_VCONN_EN/GPIO1_A1_d	GPIO1_A1	typec0 power enable	1.8V	I/O DOWN
15	UART2C_TX/GPIO4_C4_u	UART2_TX_DEBUG	DEBUG_TX	1.8V	I/O UP
16	UART2C_RX/GPIO4_C3_u	UART2_RX_DEBUG	DEBUG_RX	1.8V	I/O UP
17	RESET	RESET_L	system reset signal Input, External connection Reset key, active low	1.8V	I/O UP
18	I2S0_SDI1SDO3/GPIO3_D4_d	GPIO3_D4	reserved GPIO	1.8V	I/O DOWN
19	I2S0_SDI2SDO2/GPIO3_D5_d	GPIO3_D5	reserved GPIO	1.8V	I/O DOWN
20	NC	NC	NC		
21	SPDIF_TX/GPIO4_C5_d	GPIO4_C5	touch reset,active low		I/O DOWN
22	NC	NC	NC		
23	NC	NC	NC		
24	VDC_PWRON	VDC_PWRON	Adapter voltage detect input		
25	PMIC_SLEEP_H	PMIC_SLEEP_H	pmic sleep control,active high		
26	NC	NC	NC		
27	PWRON	PWRON	Power on Signal Input, External connection Power key , active low		
28	VCC_RTC	VCC_RTC_S5	RTC Power supply input,2.7V~5.5V		
29	EXT_EN	EXT_EN_H	Exit DCDC Power enable output		
30	SPI1_RXD/UART4_RX/GPIO1_A7_u	SPI1_RXD	SPI bus port 1		I/O UP
31	SPI1_TXD/UART4_TX/GPIO1_B0_u	SPI1_TXD	SPI bus port 1		I/O UP
32	SPI1_CSN0/PMCU_JTAG_TMS/GPIO1_B2_u	SPI1_CS0	SPI bus port 1		I/O UP
33	NC	NC	NC		
34	SPI1_CLK/PMCU_JTAG_TCK/GPIO1_B1_u	SPI1_CLK	SPI bus port 1		I/O UP
35	GND	GND	GND		
36	NC	NC	NC		
37	NC	NC	NC		
38	NC	NC	NC		
39	NC	NC	NC		
40	NC	NC	NC		
41	GND	GND	GND		
42	VBUS_TYPEC0	VBUS_TYPEC0	Typec0 power Input for Som		
43	TYPEC0_DP	TYPEC0_DP	TYPEC0 Data USB2.0 DP		
44	TYPEC0_DM	TYPEC0_DM	TYPEC0 Data USB2.0 DM		
45	TYPEC0_TX1P	TYPEC0_TX1P	TYPEC0 positive half of second SuperSpeedTX differential pair		
46	TYPEC0_TX1N	TYPEC0_TX1N	TYPEC0 nositive half of second SuperSpeedTX differential pair		
47	GND	GND	GND		
48	TYPEC0_RX1P	TYPEC0_RX1P	TYPEC0 pegative half of second SuperSpeedRX differential pair.		
49	TYPEC0_RX1M	TYPEC0_RX1N	TYPEC0 negative half of second SuperSpeedRX differential pair.		
50	GND	GND	GND		
51	GND	GND	GND		
52	VCC5V0_SYS_S3	VCC5V0_SYS_S3	5V System power supply input		
53	VCC5V0_SYS_S3	VCC5V0_SYS_S3	5V System power supply input		
54	VCC5V0_SYS_S3	VCC5V0_SYS_S3	5V System power supply input		
55	VCC5V0_SYS_S3	VCC5V0_SYS_S3	5V System power supply input		
56	VCC5V0_SYS_S3	VCC5V0_SYS_S3	5V System power supply input		
57	VCC5V0_SYS_S3	VCC5V0_SYS_S3	5V System power supply input		
58	VCC5V0_SYS_S3	VCC5V0_SYS_S3	5V System power supply input		
59	VCC5V0_SYS_S3	VCC5V0_SYS_S3	5V System power supply input		
60	VCC3V3_SYS_S3	VCC3V3_SYS_S3	3.3V System power supply output 500mA max		
61	VCC_1V8_S3	VCC_1V8_S3	1.8V power supply output 500mA max		
62	SDIO0_DETN/PCIE_CLKREQN/GPIO2_D2_u	GPIO2_D2	WIFI module wake up AP	1.8V	I/O UP
63	SDIO0_CMD/GPIO2_D0_u	SDIO0_CMD	SDIO0 command output , for WIFI module	1.8V	I/O UP
64	SDIO0_CLKOUT/TEST_CLKOUT1/GPIO2_D1_u	SDIO0_CLK	SDIO0 clock output, for WIFI module	1.8V	I/O UP
65	SDIO0_D0/SPI5_RXD/GPIO2_C4_u	SDIO0_D0	SDIO0 data port , for WIFI module	1.8V	I/O UP
66	SDIO0_D1/SPI5_TXD/GPIO2_C5_u	SDIO0_D1	SDIO0 data port , for WIFI module	1.8V	I/O UP
67	SDIO0_D2/SPI5_CLK/GPIO2_C6_u	SDIO0_D2	SDIO0 data port , for WIFI module	1.8V	I/O UP
68	SDIO0_D3/SPI5_CSN0/GPIO2_C7_u	SDIO0_D3	SDIO0 data port , for WIFI module	1.8V	I/O UP
69	GND	GND	GND		I/O UP
70	GPIO4_D6_d	LCD_PWREN_H	LCD power enable,active high		I/O DOWN
71	EMMC_PWRON/GPIO0_A5_u	GPIO0_A5	touch controler interrupt input		I/O UP
72	GPIO4_D4_d	LCD_BL_EN_H	LCD backlight enable,active high		I/O DOWN
73	PWM0/VOP0_PWM/VOP1_PWM/GPIO4_C2_d	LCD_BL_PWM	Control the LCD backlight brightness		I/O DOWN
74	GND	GND	GND		
75	EDP_TX0N	EDP_TX0N	eDP differential lane 0 negative output		
76	EDP_TX0P	EDP_TX0P	eDP differential lane 0 positive output		
77	GND	GND	GND		
78	EDP_TX1N	EDP_TX1N	eDP differential lane 1 negative output		
79	EDP_TX1P	EDP_TX1P	eDP differential lane 1 positive output		
80	GND	GND	GND		
81	EDP_TX2N	EDP_TX2N	eDP differential lane 2 negative outpu		
82	EDP_TX2P	EDP_TX2P	eDP differential lane 2 positive output		
83	GND	GND	GND		
84	EDP_AUXP	EDPAUXN	eDP differential AUX channel nositive output		
85	EDP_AUXN	EDPAUXP	eDP differential AUX channel positive output		
86	GND	GND	GND		
87	EDP_TX3N	EDP_TX3N	eDP differential lane 3 negative output		
88	EDP_TX3P	EDP_TX3P	eDP differential lane 3 positive output		
89	GND	GND	GND		
90	I2C4_SDA/GPIO1_B3_u	I2C4_SDA	Touch the i2c interface	1.8V	I/O UP
91	I2C4_SCL/GPIO1_B4_u	I2C4_SCL	Touch the i2c interface	1.8V	I/O UP
92	VOP_D7/CIF_D7/I2C7_SDA/GPIO2_A7_u	I2C7_SDA_1V8	I2C serial port 7	1.8V	I/O UP
93	VOP_CLK/CIF_VSYNC/I2C7_SCL/GPIO2_B0_u	I2C7_SCL_1V8	I2C serial port 7	1.8V	I/O UP
94	DDRIO_PWROFF/TCPD_CCDB_EN/GPIO0_A1_u	GPIO0_A1	Fan power control		I/O UP
95	TYPEC0_TX2P	TYPEC0_TX2P	TYPEC0 positive half of second SuperSpeedTX differential pair		
96	TYPEC0_TX2N	TYPEC0_TX2N	TYPEC0 negative half of second SuperSpeedTX differential pair.		
97	GND	GND	GND		
98	TYPEC0_RX2P	TYPEC0_RX2P	TYPEC0 positive half of second SuperSpeedRX differential pair.		
99	TYPEC0_RX2N	TYPEC0_RX2N	TYPEC0 negative half of second SuperSpeedRX differential pair.		
100	GND	GND	GND		

X2 Connector					
PIN	Core board pin definition	Default function	Defual function description	IO Power domain	Pad type IO Pull
1	GND	GND	GND		
2	NC	NC	NC		
3	NC	NC	NC		
4	NC	NC	NC		
5	NC	NC	NC		
6	NC	NC	NC		
7	GND	GND	GND		
8	PCIE_TX3_P	PCIE_TX3P	PCIE differential lane 3 positive output		
9	PCIE_TX3_N	PCIE_TX3N	PCIE differential lane 3 negative output		
10	GND	GND	GND		
11	PCIE_RX3_P	PCIE_RX3P	PCIE differential lane 3 positive input		
12	PCIE_RX3_N	PCIE_RX3N	PCIE differential lane 3 negative input		
13	GND	GND	GND		
14	PCIE_TX2_P	PCIE_TX2P	PCIE differential lane 2 positive output		
15	PCIE_TX2_N	PCIE_TX2N	PCIE differential lane 2 negative output		
16	GND	GND	GND		
17	PCIE_RX2_P	PCIE_RX2P	PCIE differential lane 2 positive input		
18	PCIE_RX2_N	PCIE_RX2N	PCIE differential lane 2 negative input		
19	GND	GND	GND		
20	PCIE_TX0_P	PCIE_TX0P	PCIE differential lane 0 positive output		
21	PCIE_TX0_N	PCIE_TX0N	PCIE differential lane 0 negative output		
22	GND	GND	GND		
23	PCIE_RX0_P	PCIE_RX0P	PCIE differential lane 0 positive input		
24	PCIE_RX0_N	PCIE_RX0N	PCIE differential lane 0 negative input		
25	GND	GND	GND		
26	PCIE_RCLK_100M_P	PCIE_REF_CLKP	PCIE 100MHz reference clock as output to PLL		
27	PCIE_RCLK_100M_N	PCIE_REF_CLKN	PCIE 100MHz reference clock as output to PLL		
28	PWM3A_IR/GPIO0_A6_d	GPIO0_A6	BT module power enable		
29	TCPD_VBUS_BDIS/GPIO0_B4_d	GPIO0_B4	PCIE reset output,active low		
30	GND	GND	GND		
31	NC	NC	NC		
32	NC	NC	NC		
33	GND	GND	GND		
34	NC	NC	NC		
35	NC	NC	NC		
36	GND	GND	GND		
37	NC	NC	NC		
38	NC	NC	NC		
39	GND	GND	GND		
40	NC	NC	NC		
41	NC	NC	NC		
42	GND	GND	GND		
43	NC	NC	NC		
44	NC	NC	NC		
45	NC	NC	NC		
46	ADC_IN4	ADC4	ADC input		
47	GND	GND	GND		
48	ADC_IN2	ADC2_KEY_IN	RECOVERY and user KEY		
49	NC	NC	NC		
50	GND	GND	GND		
51	GND	GND	GND		
52	NC	NC	NC		
53	NC	NC	NC		
54	GND	GND	GND		
55	NC	NC	NC		
56	NC	NC	NC		
57	GND	GND	GND		
58	NC	NC	NC		
59	NC	NC	NC		
60	GND	GND	GND		
61	NC	NC	NC		
62	NC	NC	NC		
63	GND	GND	GND		
64	NC	NC	NC		
65	NC	NC	NC		
66	GND	GND	GND		
67	NC	NC	NC		
68	NC	NC	NC		
69	USB20_HOST0_DP	HOST0_DP	USB2.0 HOST0 DP		
70	USB20_HOST0_DN	HOST0_DM	USB2.0 HOST0 DM		
71	GND	GND	GND		
72	PCIE_TX1_P	PCIE_TX1P	PCIE differential lane 1 positive output		
73	PCIE_TX1_N	PCIE_TX1N	PCIE differential lane 1 negative output		
74	GND	GND	GND		
75	PCIE_RX1_P	PCIE_RX1P	PCIE differential lane 1 positive input		
76	PCIE_RX1_N	PCIE_RX1N	PCIE differential lane 1 nositive input		
77	GND	GND	GND		
78	SDMMC0_WRPT/TEST_CLKOUT2/GPIO0_B0_u	GPIO0_B0	AP wake up PCIE,active low		I/O UP
79	GND	GND	GND		
80	SPKN_OUT	SPKN_OUT	Negative speaker driver output		
81	SPKP_OUT	SPKP_OUT	Positive speaker driver output		
82	GND	GND	GND		
83	MIC1P	MIC1_IN	input of the Microphone		
84	ADC3	ADC3_HP_HOOK	microphone to detect		
85	GND	GND	GND		
86	HPL_OUT	HPL	Left channel output of the headphone		
87	HP_SNS	HP_SNS	Reference ground for the headphone		
88	HPR_OUT	HPR	Right channel output of the headphone		
89	GND	GND	GND		
90	NC	NC	NC		
91	NC	NC	NC		
92	NPU_USB2_OTG_DP	NPU_USB1_DP	NPU USB2.0 DP		
93	NPU_USB2_OTG_DM	NPU_USB1_DM	NPU USB2.0 DM		
94	NC	NC	NC		
95	NPU_PCIE_TX0P/USB3_SSTXP	NPU_USB3_SSTXP	NPU USB3.0 positive SuperSpeedTX differential pair		
96	NPU_PCIE_TX0N/USB3_SSTXN	NPU_USB3_SSTXN	NPU USB3.0 negative SuperSpeedTX differential pair		
97	GND	GND	GND		
98	NPU_PCIE_RX0P/USB3_SSRXP	NPU_USB3_SSRXP	NPU USB3.0 positive SuperSpeedRX differential pair		
99	NPU_PCIE_RX0N/USB3_SSRXN	NPU_USB3_SSRXN	NPU USB3.0 negative SuperSpeedRX differential pair		
100	GND	GND	GND		

X3 Connector					
PIN	Core board pin definition	Default function	Defual function description	IO Power domain	Pad type IO Pull
1	GND	GND	GND		
2	MIPI_RX0_D2P	MIPI_RX0_D2P	MIPI-CSI0 differential lane 2 positive		
3	MIPI_RX0_D2N	MIPI_RX0_D2N	MIPI-CSI0 differential lane 2 negative		
4	GND	GND	GND		
5	MIPI_RX0_D3P	MIPI_RX0_D3P	MIPI-CSI0 differential lane 3 positive		
6	MIPI_RX0_D3N	MIPI_RX0_D3N	MIPI-CSI0 differential lane 3 negative		
7	GND	GND	GND		
8	MIPI_TX1/RX1_D3P	MIPI_TX1/RX1_D3P	MIPI-DSI1/CSI1 differential lane 3 positive		
9	MIPI_TX1/RX1_D3N	MIPI_TX1/RX1_D3N	MIPI-DSI1/CSI1 differential lane 3 negative		
10	GND	GND	GND		
11	MIPI_TX1/RX1_D2P	MIPI_TX1/RX1_D2P	MIPI-DSI1/CSI1 differential lane 2 positive		
12	MIPI_TX1/RX1_D2N	MIPI_TX1/RX1_D2N	MIPI-DSI1/CSI1 differential lane 2 negative		
13	GND	GND	GND		
14	MIPI_TX1/RX1_CLKP	MIPI_TX1/RX1_CLKP	MIPI-DSI1/CSI1 differential clock lane positive		
15	MIPI_TX1/RX1_CLKN	MIPI_TX1/RX1_CLKN	MIPI-DSI1/CSI1 differential clock lane negative		
16	GND	GND	GND		
17	MIPI_TX1/RX1_D1P	MIPI_TX1/RX1_D1P	MIPI-DSI1/CSI1 differential lane 1 positive		
18	MIPI_TX1/RX1_D1N	MIPI_TX1/RX1_D1N	MIPI-DSI1/CSI1 differential lane 1 negative		
19	GND	GND	GND		
20	MIPI_TX1/RX1_D0P	MIPI_TX1/RX1_D0P	MIPI-DSI1/CSI1 differential lane 0 positive		
21	MIPI_TX1/RX1_D0N	MIPI_TX1/RX1_D0N	MIPI-DSI1/CSI1 differential lane 0 negative		
22	GND	GND	GND		
23	MIPI_TX0_D0P	MIPI_TX0_D0P	MIPI-DSI0 differential lane 0 positive		
24	MIPI_TX0_D0N	MIPI_TX0_D0N	MIPI-DSI0 differential lane 0 negativ		
25	GND	GND	GND		
26	MIPI_TX0_D1P	MIPI_TX0_D1P	MIPI-DSI0 differential lane 1 positive		
27	MIPI_TX0_D1N	MIPI_TX0_D1N	MIPI-DSI0 differential lane 1 negativ		
28	GND	GND	GND		
29	MIPI_TX0_CLKP	MIPI_TX0_CLKP	MIPI-DSI0 differential clock lane positive		
30	MIPI_TX0_CLKN	MIPI_TX0_CLKN	MIPI-DSI0 differential clock lane negative		
31	GND	GND	GND		
32	MIPI_TX0_D2P	MIPI_TX0_D2P	MIPI-DSI0 differential lane 2 positive		
33	MIPI_TX0_D2N	MIPI_TX0_D2N	MIPI-DSI0 differential lane 2 negative		
34	GND	GND	GND		
35	MIPI_TX0_D3P	MIPI_TX0_D3P	MIPI-DSI0 differential lane 3 positive		
36	MIPI_TX0_D3N	MIPI_TX0_D3N	MIPI-DSI0 differential lane 3 negative		
37	GND	GND	GND		
38	NC	NC	NC		
39	NC	NC	NC		
40	GND	GND	GND		
41	SDIO0_PWREN/GPIO2_D3_d	GPIO2_D3	reserved GPIO		I/O DOWN
42	NC	NC	NC		
43	NC	NC	NC		
44	NC	NC	NC		
45	I2C1_SDA/GPIO4_A1_u	I2C1_SDA_1V8	Camera I2C interface (MIPI_RX0)	1.8V	I/O UP
46	I2C1_SCL/GPIO4_A2_u	I2C1_SCL_1V8	Camera I2C interface (MIPI_RX0)	1.8V	I/O UP
47	SPI2_CLK/VOP_DEN/CIF_CLKOUTA/GPIO2_B3_u	MIPI_RX0_MCLK	MIPI_RX0_MCLK		I/O UP
48	DP_HOTPLUG/GPIO4_D1_d	GPIO4_D1	Camera0 reset		I/O DOWN
49	GPIO4_D5_d	GPIO4_D5	Camera0 power enable,active high		
50	GND	GND	GND		
51	GND	GND	GND		
52	MIPI_RX0_CLKP	MIPI_RX0_CLKP	MIPI-CSI0 differential clock lane positive		
53	MIPI_RX0_CLKN	MIPI_RX0_CLKN	MIPI-CSI0 differential clock lane negative		
54	GND	GND	GND		
55	MIPI_RX0_D1P	MIPI_RX0_D1P	MIPI-CSI0 differential lane 1 positive		
56	MIPI_RX0_D1N	MIPI_RX0_D1N	MIPI-CSI0 differential lane 1 negative		
57	GND	GND	GND		
58	MIPI_RX0_D0P	MIPI_RX0_D0P	MIPI-CSI0 differential lane 0 positive		
59	MIPI_RX0_D0N	MIPI_RX0_D0N	MIPI-CSI0 differential lane 0 negative		
60	GND	GND	GND		
61	HDMI_TX2P	HDMI_TX2P	HDMI channel 2 differential serial data positive		
62	HDMI_TX2N	HDMI_TX2N	HDMI channel 2 differential serial data negative		
63	GND	GND	GND		
64	HDMI_TX1P	HDMI_TX1P	HDMI channel 1 differential serial data positive		
65	HDMI_TX1N	HDMI_TX1N	HDMI channel 1 differential serial data negative		
66	GND	GND	GND		
67	HDMI_TXCP	HDMI_TXCP	HDMI differential pixel clock positive		
68	HDMI_TXCN	HDMI_TXCN	HDMI differential pixel clock negative		
69	GND	GND	GND		
70	HDMI_TX0P	HDMI_TX0P	HDMI channel 0 differential serial data positive		
71	HDMI_TX0N	HDMI_TX0N	HDMI channel 0 differential serial data negative		
72	GND	GND	GND		
73	I2C3_SCL/UART2B_TX/GPIO4_C1_u	I2C3_SCL_HDMI	HDMI i2c interface	3.0V	I/O UP
74	I2C3_SDA/UART2B_RX/GPIO4_C0_u	I2C3_SDA_HDMI	HDMI i2c interface	3.0V	I/O UP
75	HDMI_CECINOUT/EDP_HOTPLUG/GPIO4_C7_u	HDMI_CEC	HDMI CEC communication		I/O UP
76	HDMI_HPD	HDMI_PORT_HPD	HDMI Hot Plug Detection interrupt with 5V tolerance		
77	VCC_LAN	VCC_LAN	LAN power output for lan led		
78	LED1_AD1	LED1_AD1	LAN Work GREEN LED		
79	LED0_AD0	LED0_AD0	LAN Work YELLOW LED		
80	NC	NC	NC		
81	GND	GND	GND		
82	LAN_MDI0+	LAN_MDI0+	LAN_MDI0+		
83	LAN_MDI0-	LAN_MDI0-	LAN_MDI0-		
84	GND	GND	GND		
85	LAN_MDI1+	LAN_MDI1+	LAN_MDI1+		
86	LAN_MDI1-	LAN_MDI1-	LAN_MDI1-		
87	GND	GND	GND		
88	LAN_MDI2+	LAN_MDI2+	LAN_MDI2+		
89	LAN_MDI2-	LAN_MDI2-	LAN_MDI2-		
90	GND	GND	GND		
91	LAN_MDI3+	LAN_MDI3+	LAN_MDI3+		
92	LAN_MDI3-	LAN_MDI3-	LAN_MDI3-		
93	GND	GND	GND		
94	VOP_D1/CIF_D1/I2C2_SCL/GPIO2_A1_u	I2C2_SCL_1V8	Camera I2C interface (MIPI_RX1)	1.8V	I/O UP
95	VOP_D0/CIF_D0/I2C2_SDA/GPIO2_A0_u	I2C2_SDA_1V8	Camera I2C interface (MIPI_RX1)	1.8V	I/O UP
96	SPI2_CLK/VOP_DEN/CIF_CLKOUTA/GPIO2_B3_u	MIPI_RX1_MCLK	MIPI RX MCLK		
97	GPIO4_D2	GPIO4_D2	Camera1 reset		
98	GPIO4_D0	GPIO4_D0	Camera1 power enable,active high		
99	PWM1/GPIO4_C6_d	GPIO4_C6	AP wake up BT module		I/O DOWN
100	GND	GND	GND		

X4 Connector					
PIN	Core board pin definition	Default function	Defual function description	IO Power domain	Pad type IO Pull
1	GND	GND	GND		
2	USB20_OTG1_DP	TYPEC1_DP	TYPEC1 USB2.0 DP		
3	USB20_OTG1_DN	TYPEC1_DM	TYPEC1 USB2.0 DM		
4	NC	NC	NC		
5	USB30_TX1P	TYPEC1_TX1P	TYPEC1 positive half of second SuperSpeedTX differential pair		
6	USB30_TX1M	TYPEC1_TX1N	TYPEC1 nositive half of second SuperSpeedTX differential pair		
7	GND	GND	GND		
8	USB30_RX1P	TYPEC1_RX1P	TYPEC1 pegative half of second SuperSpeedRX differential pair.		
9	USB30_RX1M	TYPEC1_RX1N	TYPEC1 negative half of second SuperSpeedRX differential pair.		
10	VOP_D5/CIF_D5/GPIO2_A5_d	SYSTEM_WORK_LED3	System work LED	1.8V	I/O DOWN
11	VOP_D4/CIF_D4/GPIO2_A4_d	SYSTEM_WORK_LED2	System work LED	1.8V	I/O DOWN
12	GND	GND	GND		
13	I2S0_SCLK/GPIO3_D0_d	I2S0_SCLK	I2S 0 port, for audio codec	1.8V	I/O DOWN
14	I2S0_SDI0/GPIO3_D3_d	I2S0_SDI0	I2S 0 port, for audio codec	1.8V	I/O DOWN
15	I2S0_SDO0/GPIO3_D7_d	I2S0_SDO0	I2S 0 port, for audio codec	1.8V	I/O DOWN
16	I2S0_LRCK_RX/GPIO3_D1_d/I2S0_LRCK_TX/GPIO3_D2_d	I2S0_LRCK	I2S 0 port, for audio codec	1.8V	I/O DOWN
17	I2S_CLK/GPIO4_A0_d	I2S_CLK	I2S MCLK, for both I2S0 and I2S1	1.8V	I/O DOWN
18	GND	GND	GND		
19	VOP_D3/CIF_D3/GPIO2_A3_d	SYSTEM_WORK_LED1	System work LED	1.8V	I/O DOWN
20	TCPD_VBUS_FDIS/TCPD_VBUS_SOURCE3/GPIO0_B5_d	GPIO0_B5	Headphone insert detect input		I/O DOWN
21	PMUIO2_VOLSEL/GPIO0_B1_d	GPIO0_B1	BT module wake up AP		I/O DOWN
22	VOP_D2/CIF_D2/GPIO2_A2_d	U3_VCC5V0_HOST_EN	USB3.0 HOST power enable	1.8V	I/O DOWN
23	SPI2_CSN0/GPIO2_B4_u	SYSTEM_WORK_LED0	System work LED	1.8V	I/O UP
24	VOP_D6/CIF_D6/GPIO2_A6_d	GPIO2_A6	CPU Wake up the LTE module, active low	1.8V	I/O DOWN
25	GPIO1_B5_d	GPIO1_B5	LTE flight mode control module,active high	1.8V	I/O DOWN
26	SDIO0_WRPT/GPIO0_A3_d	GPIO0_A3	LTE module Wake up the CPU, high level interrupts		I/O DOWN
27	UART2_TX/NPU_GPIO4_A2_u	NPU_UART2_TX	NPU DEBUG UART RX		I/O UP
28	UART2_RX/NPU_GPIO4_A3_u	NPU_UART2_RX	NPU DEBUG UART TX		I/O UP
29	GND	GND	GND		
30	NC	NC	NC		
31	NC	NC	NC		
32	GND	GND	GND		
33	NC	NC	NC		
34	NC	NC	NC		
35	GND	GND	GND		
36	NC	NC	NC		
37	NC	NC	NC		
38	GND	GND	GND		
39	NC	NC	NC		
40	NC	NC	NC		
41	GND	GND	GND		
42	NC	NC	NC		
43	NC	NC	NC		
44	NC	NC	NC		
45	NC	NC	NC		
46	GND	GND	GND		
47	UART0_TX/GPIO2_C1_u	UART0_TXD	UART0 serial port, for BT module	1.8V	I/O UP
48	UART0_RX/GPIO2_C0_u	UART0_RXD	UART0 serial port, for BT module	1.8V	I/O UP
49	UART0_RTSN/GPIO2_C3_u	UART0_RTS	UART0 serial port, for BT module	1.8V	I/O UP
50	GND	GND	GND		
51	GND	GND	GND		
52	NC	NC	NC		
53	NC	NC	NC		
54	GND	GND	GND		
55	NC	NC	NC		
56	NC	NC	NC		
57	GND	GND	GND		
58	NC	NC	NC		
59	NC	NC	NC		
60	GND	GND	GND		
61	NC	NC	NC		
62	NC	NC	NC		
63	GND	GND	GND		
64	NC	NC	NC		
65	NC	NC	NC		
66	GND	GND	GND		
67	NC	NC	NC		
68	NC	NC	NC		
69	GND	GND	GND		
70	NC	NC	NC		
71	NC	NC	NC		
72	GND	GND	GND		
73	NC	NC	NC		
74	NC	NC	NC		
75	GND	GND	GND		
76	NC	NC	NC		
77	NC	NC	NC		
78	NC	NC	NC		
79	NC	NC	NC		
80	NC	NC	NC		
81	GND	GND	GND		
82	USB20_HOST1_DP	HOST1_DP	USB2.0 HOST1 DP		
83	USB20_HOST1_DN	HOST1_DM	USB2.0 HOST1 DM		
84	GND	GND	GND		
85	SDMMC0_CMD/MCUJTAG_TMS/GPIO4_B5_u	SDMMC0_CMD	SDMMC0 command output	3.3V/1.8V	I/O UP
86	SDMMC0_D0/UART2A_RX/GPIO4_B0_u	SDMMC0_D0	SDMMC0 data port	3.3V/1.8V	I/O UP
87	SDMMC0_CLKOUT/MUCJTAG_TCK/GPIO4_B4_d	SDMMC0_CLK	SDMMC0 clock output	3.3V/1.8V	I/O DOWN
88	SDMMC0_D1/UART2A_TX/GPIO4_B1_u	SDMMC0_D1	SDMMC0 data port	3.3V/1.8V	I/O UP
89	SDMMC0_D2/APJTAG_TCK/GPIO4_B2_u	SDMMC0_D2	SDMMC0 data port	3.3V/1.8V	I/O UP
90	SDMMC0_D3/APJTAG_TMS/GPIO4_B3_u	SDMMC0_D3	SDMMC0 data port	3.3V/1.8V	I/O UP
91	SDMMC0_DET/GPIO0_A7_u	SDMMC0_DET_L	SDMMC0 detect input, active low	1.8V	I/O UP
92	NC	NC	NC		
93	NC	NC	NC		
94	SPI2_RXD/CIF_HREF/I2C6_SDA/GPIO2_B1_u	I2C6_SDA_1V8/GPIO2_B1	Control the PCIE PORT2 I2C	1.8V	I/O UP
95	SPI2_TXD/CIF_CLKIN/I2C6_SCL/GPIO2_B2_u	I2C6_SCL_1V8/GPIO2_B2	Control the PCIE PORT2 I2C	1.8V	I/O UP
96	NC	NC	NC		
97	NC	NC	NC		
98	VCC3V3_SD_S0	VCC3V3_SD_S0	VCC3V3_SD_S0		
99	UART0_CTSN/GPIO2_C2_u	UART0_CTS	UART0 serial port, for BT module	1.8V	I/O UP
100	GND	GND	GND		