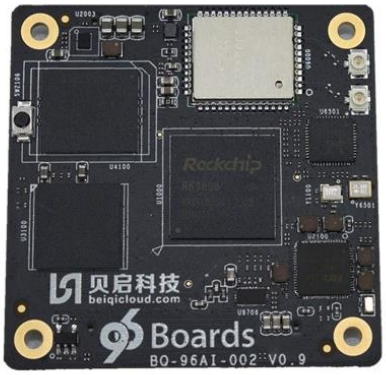
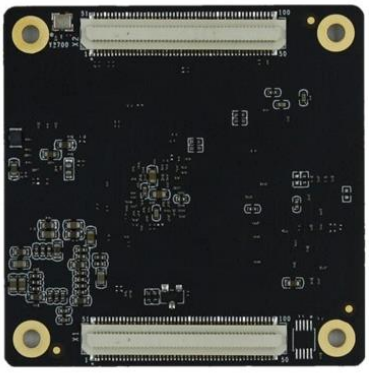
TB-96AIoT

(RK1808 Core Board)

Product Specification

V1.0





Version	Date of Revision	Content of Revision
V1.0	2019-05-08	The first version officially released

1、Product overview

1.1 Summary

On April 1st, 2019, Linaro officially released the 96Boards System-on-Moudle (SoM) specification V1.0 in Bangkok, Thailand. At the same time, it also launched two cores conforming to the 96Boards SoM specification developed by Xiamen Beiqi Technology Co., Ltd. Module TB-96AI and TB-96AIoT, TB-96AI uses RK3399Pro as the main control chip, TB-96AIoT uses RK1808 as the main control chip.

The TB-96AIoT is a low-power, high-powered core board for the AIoT field. It is equipped with a powerful neural network processing unit (NPU) and is compatible with a variety of mainstream inference models such as caffe and tensor flow. Together with the bottom board CarrierBoard developed by Xiamen Beiqi Technology Co., Ltd., it can form a complete development board or evaluation board; the base board that can be customized according to the actual needs of the customer can directly form the industrial application board, which can meet the sweeping robot, drone, smart speaker. , automotive products, smart wear, security monitoring, AI computing modules and other areas of demand.

1.2 Features

The following features are quoted from RockChip. If you have any questions, please contact BEIQICLOUD for more technical support.

1.2.1 CPU

- Dual-core ARM Cortex-A53 CPU for ultra-low power consumption.
- Includes vfp v4 hardware that supports single and double precision operations.
- ARM Neon Advanced SIMD (Single Instruction, Multiple Data) supports accelerated media and signal processing calculations.

1.2.2 Built-in neural network processor NPU, super high AI computing power

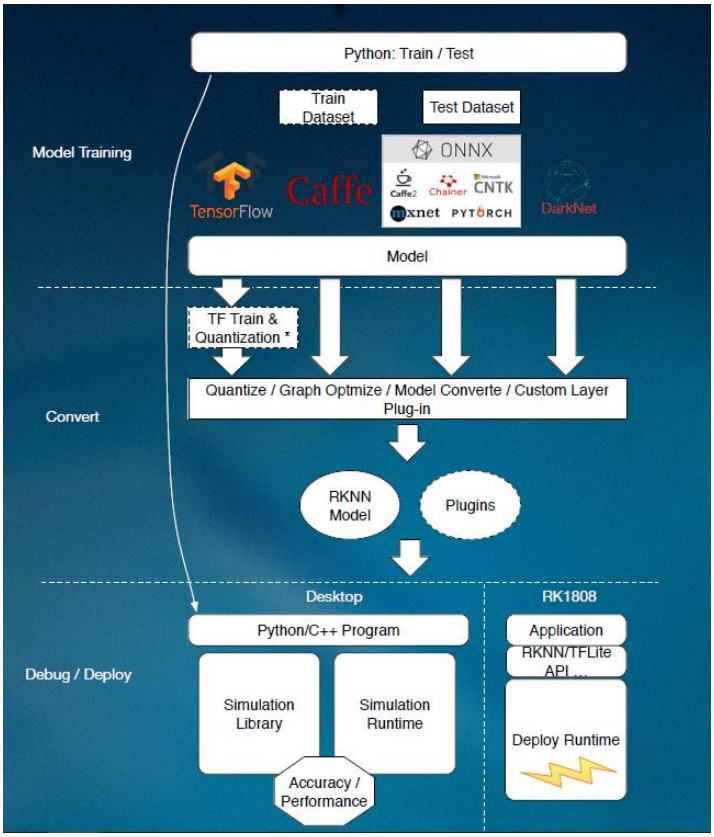
- Support 8bit/16bit computing, AI computing power up to 3.0TOPs（INT8 Inference）;

  (300 GOPs for INT16, 100 GFLOPs for FP16)

Model	Model name	FPS
Image recognition classification	VGG16	46.4
	ResNet50	81.2
	Inception_v4	21.7
Target Detection	YOLO_v2	43.4

Speech Recognition	DeepSpeech2**	Real-time rate	0.167
		Accuracy WER（LibriSpeech）	16.1

- Compatible with Caffe/Mxnet/TensorFlow model, support multi-class framework, support mainstream layer type, easy to add custom layer;
- Provide easy-to-use development tools, PC-side model conversion, performance estimation, and accuracy verification;
- AI APPlication Develop Flow



1.2.3 Video codec

- Video decoder
  - Support H.264/AVC BASE/MAIN/HIGH@LEVEL4.2;
  - Up to 1920×1080@60fps
- Video encoder
  - Support H.264 video encoder BP/MP/HP@4.2 level
  - Up to 1920×1080@60fps

1.2.4 Rich extension interface for AIoT applications

The TB-96AIoT has a rich peripheral interface for easy application expansion. Video supports MIPI input, supports MIPI display output; has a series of sensor input and output interfaces such as PWM/I2C/SPI/UART; has high-speed device interface such as Type-C/USB2.0/PCIE, built-in Gigabit Ethernet module and WiFi/ BT module; audio supports microphone array input and supports audio

output.

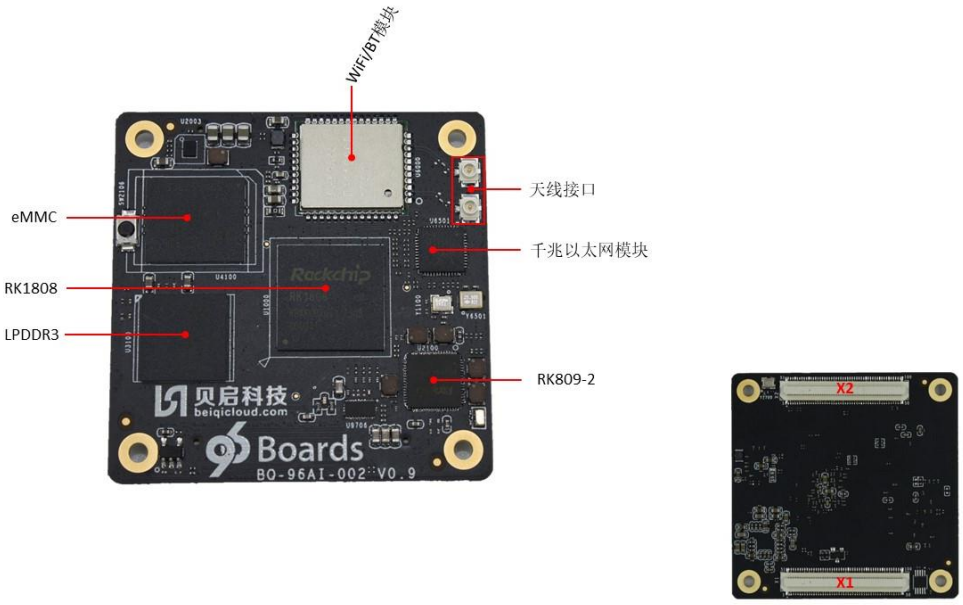
- Camera interface
  - MIPI-CSI×1, Built-in ISP image processor
  - Maximum support input resolution 1920×1080
- Display output interface
  - MIPI-DSI×1
  - Supports up to 1920×1080@60fps display output
- Audio port
  - Sperker×1
  - Headphone×1
  - Mic×1
  - I2S×1
- PCIE×1
- USB2.0 HOST×1；
- Type-C DRM×1；
- I2C×3
- LAN×1，1000M ETH
- UART Debug×1
- SPI×1
- SD Card ×1
- PWM×1
- ADC×1,One for key input and the other for headphone insertion detection

1.2.5 High-speed on-board connector for more stability and reliability

- 2 Panasonic high-speed onboard connectors for higher speed signal stability
- The core board can be fixed by 4 screw posts for various working environments.

1.2.6 Ultra-high integration, ultra-small size

- The core board integrates RK1808, LPDDR3, eMMC, power management module, Ethernet PHY chip, WiFi/BT chip, which has super high integration, which greatly reduces the design difficulty of the application backplane, and can help enterprises to quickly develop mass production specific applications. product.



- Designed to be 50mm x 50mm, it can be deployed more easily and flexibly to all types of application boards.

1.2.7 Easy to develop

Support for Linux operating system, AI application development SDK supports C / C + + and Python, convenient for customers to convert from floating point to fixed point network and debugging, development is very convenient.

1.2.8 Rich open materials, 96Boards community

The TB-96AI will be officially launched on Linaro's 96Boards, sharing 96Boards' rich software resources and easily communicating with developers around the world. For detailed reports, please visit Linaro's website: https://www.linaro.org/news/linaro-announces-launch-of-96boards-system-on-module-som-specification/

- Development board / evaluation board. Visit Beiqi Technology Official Outlet Store (Taobao Store): https://shop467163226.taobao.com/, you can directly purchase TB-96AIoT and the matching CarrierBoard to form a complete RK1808AIoT development board for algorithm development. Learning or product evaluation.
- TB-96AIoT_RK1808 core board_Product Specification.pdf
- Hardware related information.
  - Circuit schematic reference design
  - Connector PCB package
  - Core board size
  - Pin definition, interface package
- Software related materials.
  - Software development guide.pdf
  - Tools.
  - Firmware.
  - Source code

For more technical support, please contact us at service@beiqicloud.com

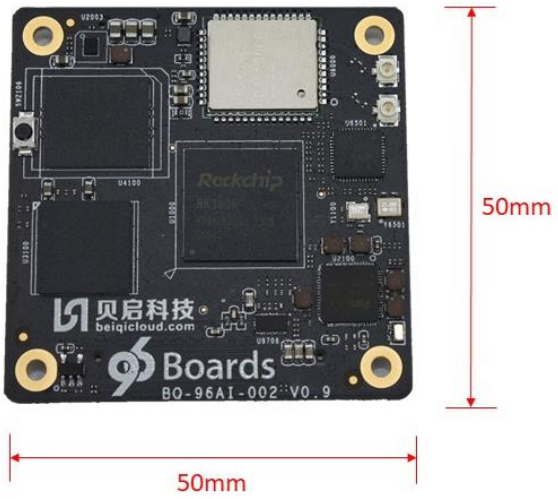
2、Specifications

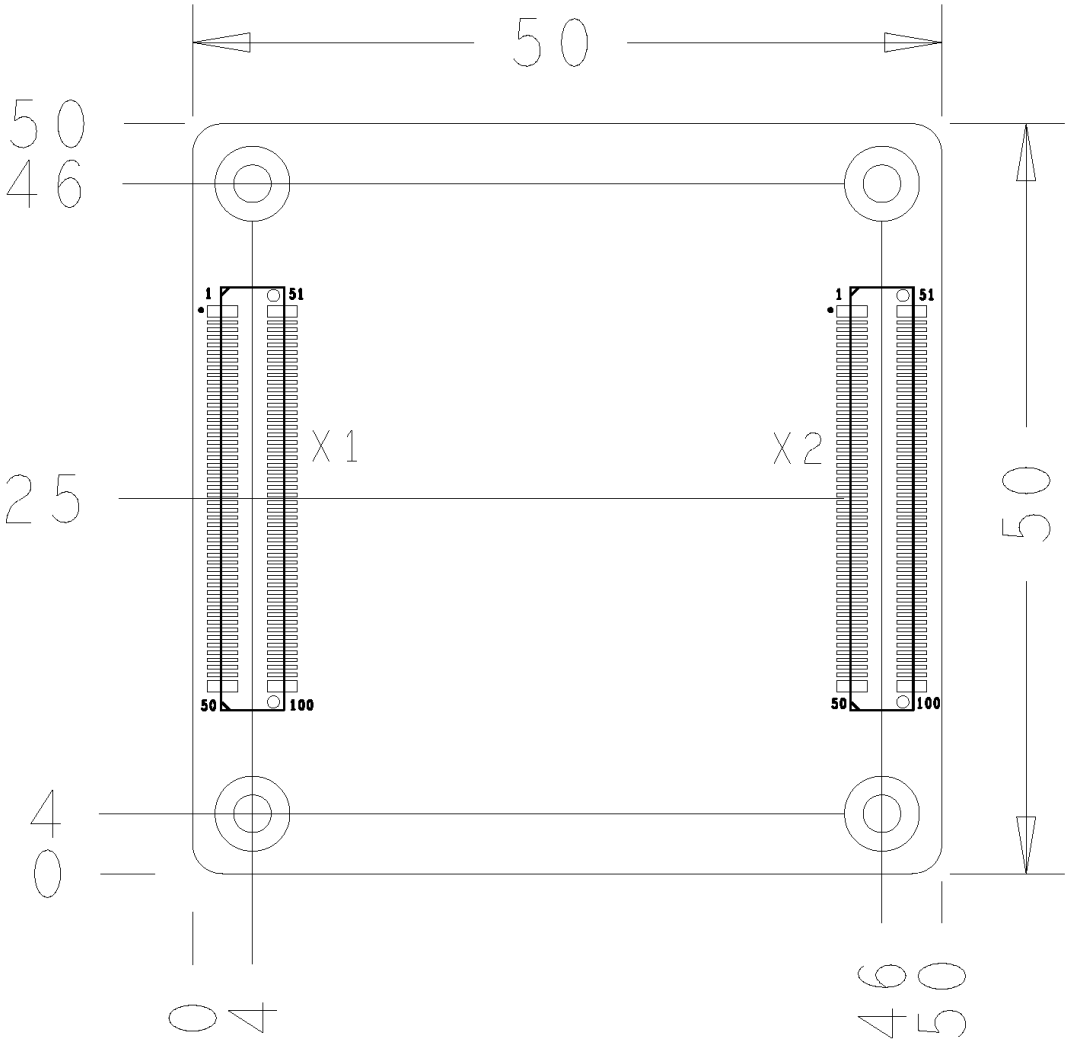
Basic Parameters	
SoC	Rockchip RK1808(22nm FD-SOI)
CPU	Dual Cortex-A35@1.6GHz
NPU	➢ Support 8bit/16bit operation, computing power up to 3.0TOPS ➢ Support TensorFlow, Caffe model
VPU	➢ 1080p@60P H.264 Decoder, ➢ 1080p@30P H.264 Encoder
RAM	Optional configuration with the following options: ➢ 1GB LPDDR3 ➢ 2GB LPDDR3 ➢ 4GB LPDDR3
Flash	Optional configuration with the following options: ➢ 16GB eMMC ➢ 32GB eMMC ➢ 64GB eMMC ➢ 128GB eMMC
Hardware Characteristics	
Ethernet	Built-in Gigabit Ethernet PHY chip, 10/100/1000Mbps adaptive
WiFi/BT	Built-in WiFi/BT module, reserved antenna holder, can be directly inserted into the antenna
Camera Interface	➢ MIPI-CSI，Maximum support 1920 × 1080 resolution

	➢ USB camera
Display Interface	One MIPI-DSI interface, up to 1920×1080@60fps display output
Audio Port	➢ Sperker×1 ➢ Headphone×1 ➢ Mic×1 ➢ I2S×1
Type-C	USB3.0 DRM ×1
USB	USB2.0 HOST ×1
Extension Port	➢ PCIE×1 ➢ I2C×3 ➢ UART Debug×1 ➢ SPI×2 ➢ SD Card ×1 ➢ PWM×1 ➢ ADC×2
Power input	DC 5V
System Software	
System Support	Linux ➢ The supported Linux distribution is buildroot-2018.02-rc3 ➢ The supported Linux kernel version is 4.4
Software Support	➢ Support 8bit/16bit operation, AI calculation power up to 3.0TOPs; ➢ Full load computing power, light load computing power

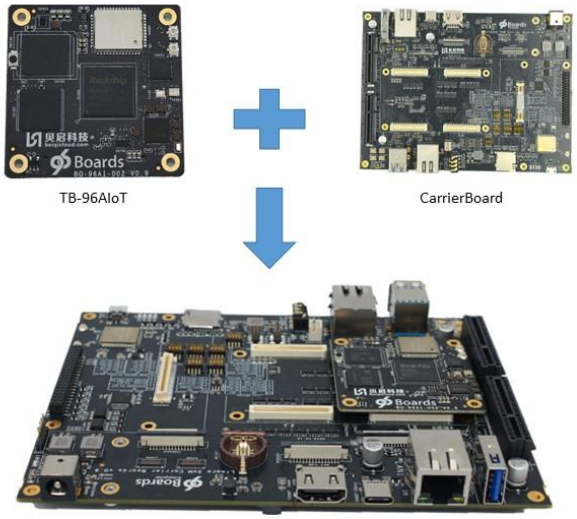
	consumption is low; ➢ The AI Application Development SDK supports C/C++ and Python, which facilitates the conversion and debugging of floating-point to fixed-point networks, and is extremely easy to develop.
Other Specifications	
Size	50mm×50mm×1.6mm
PCB Specification	8 laminate
Connector	2 Panasonic 100PIN high speed connectors, type AXK6S00437YG (PIN spacing 0.5mm)

3、Structure Size



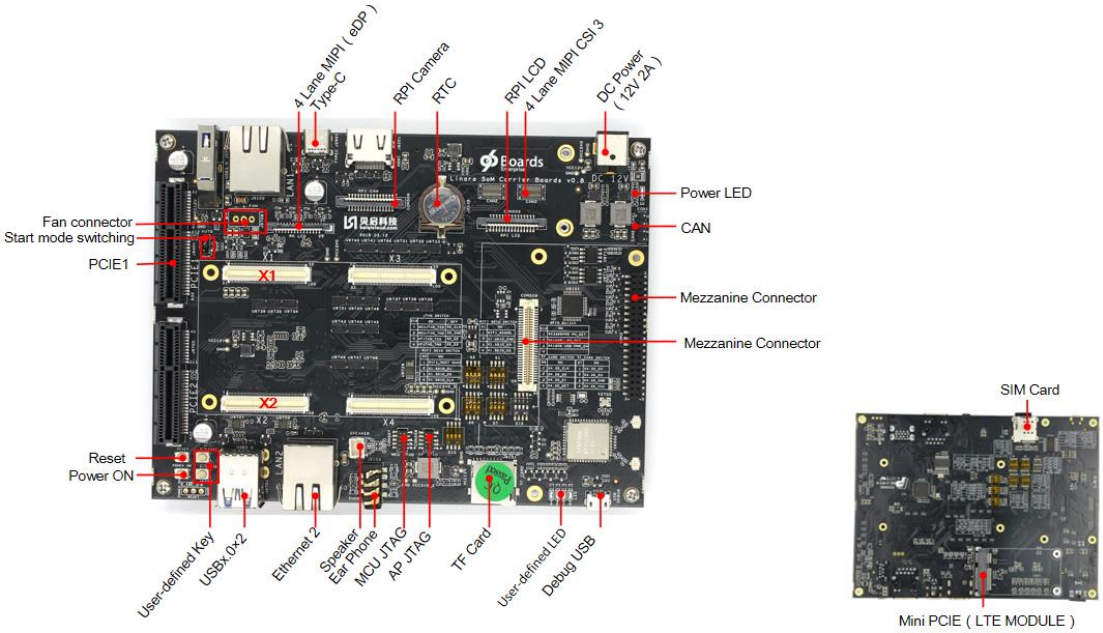


四、TB-96AIoT+Carrierboard Guide for use



The following figure shows the use of TB-96AIoT RK1808 SOM on the Carrier board.

The following figure shows the interfaces on the board that can be provided to TB-96AIoT RK1808 SOM



Download firmware

Connect the TYPEC to PC

Long press and hold the Maskrom button as shown in the following figure.

Insert power supply.

Interface use

Som connector: Use the X1 X2

LAN: Only can use the Ethernet2

Camera: Only can use CAM3 connector

Wifi: Only use the WIFI module on SOM

HDMI: No HDMI interface

PCIE: Only use the PCIE1(Different SOM hardware required)

USB: Only USB2.0 on the USBx.0 connector

The TF card,debug usb,power key,reset key,user key,user leds, DC Jacket,Audio Jacket are common connector.

Switch

The switches for TB-96AIoT are configured as follows

All switch on S1,S2,S6,S7 ,S10,S11,S12,S14,S15, config to disconnect.

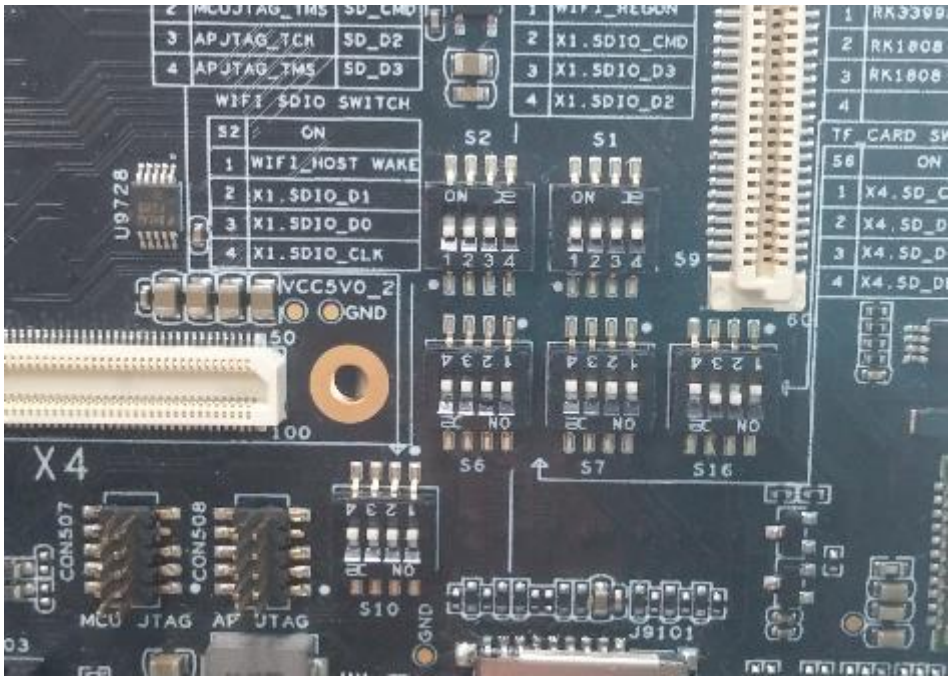
All switch on S8,S9 config to connect for TFcard

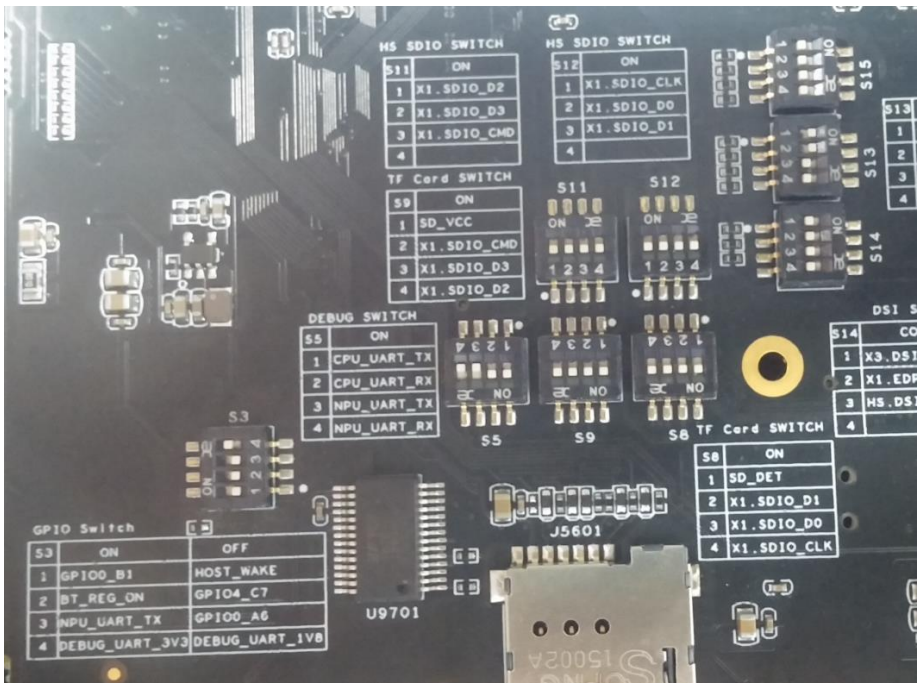
Bit2,bit3 on S16 config to connect.

Bit1,bit2 on S5 config to connect fot debug uart

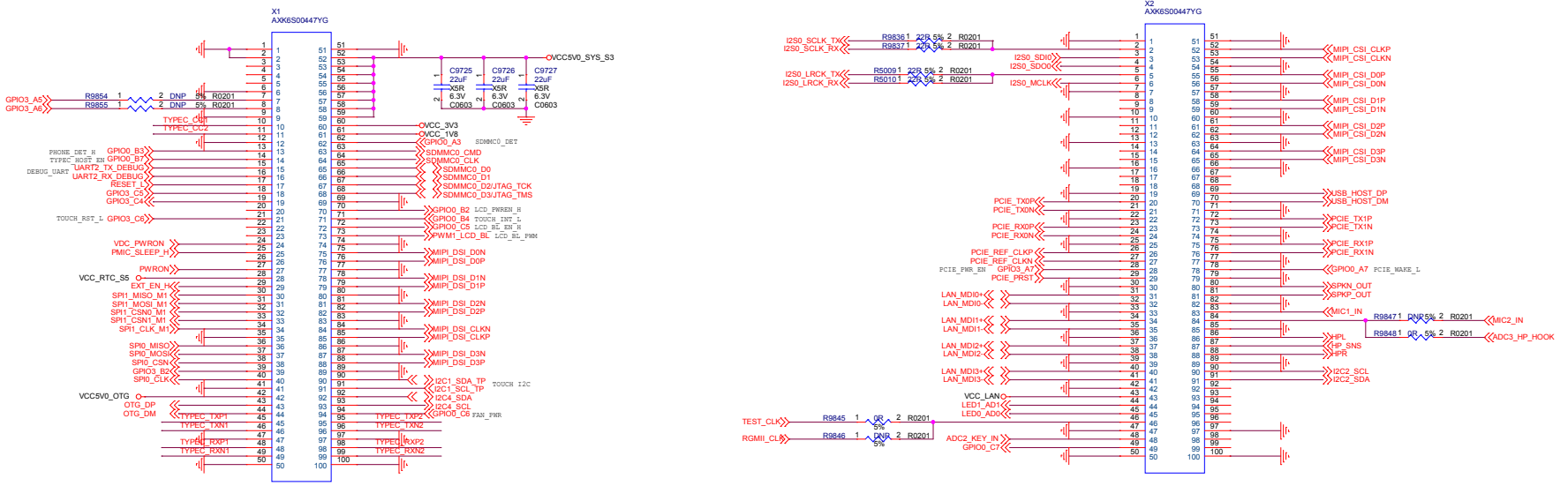
Bit4 on S3 config to connect for debug uart

Bit1,bit2 on S13 config to connect for USB





5、Interface definition


X1
AXK6S00447YG
X2
AXK6S00447YG
C9725
C9726
C9727
22uF
X5R
6.3V
C0603
R9854
R9855
R0201
DNP
5%
GPIO3_A5
GPIO3_A6
OVCC5V0_SYS_S3
OVCC_3V3
OVCC_1V8
TYPEC_CC1
TYPEC_CC2
PHONE_DET_H
TYPEC_HOST_EN
DEBUG_UART
UART2_TX_DEBUG
UART2_RX_DEBUG
RESET_L
TOUCH_RST_L
VDC_PWRON
PMIC_SLEEP_H
PWRON
VCC_RTC_S5
EXT_EN_H
SPI1_MISO_M1
SPI1_MOSI_M1
SPI1_CSN0_M1
SPI1_CSN1_M1
SPI1_CLK_M1
SPI0_MISO
SPI0_MOSI
SPI0_CSN
SPI0_CLK
VCC5V0_OTG
OTG_DP
OTG_DM
TYPEC_TXP1
TYPEC_TXN1
TYPEC_RXP1
TYPEC_RXN1
TYPEC_TXP2
TYPEC_TXN2
TYPEC_RXP2
TYPEC_RXN2
SDMMC0_DET
SDMMC0_CMD
SDMMC0_CLK
SDMMC0_D0
SDMMC0_D1
SDMMC0_D2/JTAG_TCK
SDMMC0_D3/JTAG_TMS
LCD_PWREN_H
TOUCH_INT_L
LCD_BL_EN_H
LCD_BL_PWM
MIPI_DSI_D0N
MIPI_DSI_D0P
MIPI_DSI_D1N
MIPI_DSI_D1P
MIPI_DSI_D2N
MIPI_DSI_D2P
MIPI_DSI_CLKN
MIPI_DSI_CLKP
MIPI_DSI_D3N
MIPI_DSI_D3P
I2C1_SDA_TP
I2C1_SCL_TP
I2C4_SDA
I2C4_SCL
TOUCH_I2C
FAN_PWR
I2S0_SCLK_TX
I2S0_SCLK_RX
I2S0_LRCK_TX
I2S0_LRCK_RX
R9836
R9837
R50091
R50101
22R
I2S0_SDI0
I2S0_SDO0
I2S0_MCLK
TEST_CLK
RGMII_CLK
R9845
R9846
0R
DNR
ADC2_KEY_IN
GPIO0_C7
MIPI_CSI_CLKP
MIPI_CSI_CLKN
MIPI_CSI_D0P
MIPI_CSI_D0N
MIPI_CSI_D1P
MIPI_CSI_D1N
MIPI_CSI_D2P
MIPI_CSI_D2N
MIPI_CSI_D3P
MIPI_CSI_D3N
USB_HOST_DP
USB_HOST_DM
PCIE_TX1P
PCIE_TX1N
PCIE_RX1P
PCIE_RX1N
PCIE_TX0P
PCIE_TX0N
PCIE_RX0P
PCIE_RX0N
PCIE_REF_CLKP
PCIE_REF_CLKN
PCIE_PRST
PCIE_PWR_EN
GPIO3_A7
GPIO0_A7
PCIE_WAKE_L
SPKN_OUT
SPKP_OUT
MIC1_IN
R98471
R98481
MIC2_IN
ADC3_HP_HOOK
LAN_MDI0+
LAN_MDI0-
LAN_MDI1+
LAN_MDI1-
LAN_MDI2+
LAN_MDI2-
LAN_MDI3+
LAN_MDI3-
VCC_LAN
LED1_AD1
LED0_AD0
HPL
HP_SNS
HPR
I2C2_SCL
I2C2_SDA

X1 Connector

PIN	Core board pin definition	Default function	Defual function description	IO Power domain	Pad type IO Pull
1	GND	GND	GND		
2	GND	GND	GND		
3	NC	NC	NC		
4	NC	NC	NC		
5	NC	NC	NC		
6	GND	GND	GND		
7	I2SO_SDI3/PDM_SDI3/GPIO3_A5_d	GPIO3_A5	TYPECO_AUX differential TX/RX serial data		I/O DOWN
8	I2SO_SDI2/PDM_SDI2/GPIO3_A6_d	GPIO3_A6	TYPECO_AUX differential TX/RX serial data		I/O DOWN
9	GND	GND	GND		
10	TYPEC_CC1	TYPEC_CC1	TYPEC_CC1		
11	TYPEC_CC2	TYPEC_CC2	TYPEC_CC2		
12	GND	GND	GND		
13	UART0_RX/GPIO0_B3_d	GPIO0_B3	Headphone insert detect input, active high	1.8V	I/O DOWN
14	PWM0/OTG_DRV/GPIO0_B7_d	GPIO0_B7	typec host power enable	1.8V	I/O DOWN
15	SDMMC0_DO/UART2_TX_M0/GPIO4_A2_u	UART2_TX_DEBUG	DEBUG_UART	3.3V	I/O UP
16	SDMMC0_D1/UART2_RX_M0/GPIO4_A3_u	UART2_RX_DEBUG	DEBUG_UART	3.3V	I/O UP
17	RESET	RESET_L	system reset signal Input, External connection Reset key, active low	1.8V	
18	LCDC_D11/UART6_RX/GPIO3_C5_d	GPIO3_C5	System work LED	1.8V	I/O DOWN
19	LCDC_D10/UART6_TX/GPIO3_C4_d	GPIO3_C4	System work LED	1.8V	I/O DOWN
20	NC	NC	NC		
21	LCDC_D12/UART7_TX/GPIO3_C6_d	GPIO3_C6	touch reset,active low	1.8V	I/O DOWN
22	NC	NC	NC		
23	NC	NC	NC		
24	VDC_PWRON	VDC_PWRON	Adapter voltage detect input		
25	PMIC_SLEEP_H	PMIC_SLEEP_H	pmic sleep control,active high		
26	NC	NC	NC		
27	PWRON	PWRON	Power on Signal Input, External connection Power key , active low		
28	VCC_RTC	VCC_RTC_S5	RTC Power supply		
29	EXT_EN	EXT_EN_H	VCC_RTC Power supply		
30	LCDC_D16/PWM10/SPI1_MISO_M1/GPIO3_D2_d	SPI1_MISO_M1	SPI bus port 1		I/O DOWN
31	LCDC_D14/PWM8/SPI1_MOSI_M1/GPIO3_D0_d	SPI1_MOSI_M1	SPI bus port 1		I/O DOWN
32	LCDC_D15/PWM9/SPI1_CSN0_M1/GPIO3_D1_d	SPI1_CSN0_M1	SPI bus port 1		I/O DOWN
33	LCDC_D17/PWM11/SPI1_CSN1_M1/GPIO3_D3_d	SPI1_CSN1_M1	SPI bus port 1		I/O DOWN
34	LCDC_D13/UART7_RX/SPI1_CLK_M1/GPIO3_C7_d	SPI1_CLK_M1	SPI bus port 1		I/O DOWN
35	GND	GND	GND		
36	SPI0_MISO/I2C2_SDA_M1/UART1_TX_M1/GPIO1_B5	SPI0_MISO	SPI bus port 0		I/O UP
37	SPI0_MOSI/I2C2_SCL_M1/UART1_RX_M1/GPIO1_B	SPI0_MOSI	SPI bus port 0		I/O UP
38	SPI0_CSN/PWM4/GPIO1_B6_u	SPI0_CSN	SPI bus port 0		I/O UP
39	I2SO_SDO3/ISP_FLASHTRIGIN/LCDC_HSYNC_M1/G	GPIO3_B2	SPI bus port 0		I/O DOWN
40	SPI0_CLK/PWM5/GPIO1_B7_d	SPI0_CLK	SPI bus port 0		I/O DOWN
41	GND	GND	GND		
42	VCC5V0_OTG	VCC5V0_OTG	5V_OTG_power_supply		
43	USB_OTG_DP	OTG_DP	OTG Data Plus port		
44	USB_OTG_DM	OTG_DM	OTG Data Plus port		
45	TYPEC_TXP1	TYPEC_TXP1	TYPECO positive half of second SuperSpeedTX differential pair		
46	TYPEC_TXN1	TYPEC_TXN1	TYPECO nositive half of second SuperSpeedTX differential pair		
47	GND	GND	GND		
48	TYPEC_RXP1	TYPEC_RXP1	TYPECO pegative half of second SuperSpeedRX differential pair.		
49	TYPEC_RXN1	TYPEC_RXN1	TYPECO negative half of second SuperSpeedRX differential pair.		
50	GND	GND	GND		
51	GND	GND	GND		
52	VCC5V0_SYS_S3	VCC5V0_SYS_S3	5V_System_power_supply		
53	VCC5V0_SYS_S3	VCC5V0_SYS_S3	5V_System_power_supply		
54	VCC5V0_SYS_S3	VCC5V0_SYS_S3	5V_System_power_supply		
55	VCC5V0_SYS_S3	VCC5V0_SYS_S3	5V_System_power_supply		
56	VCC5V0_SYS_S3	VCC5V0_SYS_S3	5V_System_power_supply		
57	VCC5V0_SYS_S3	VCC5V0_SYS_S3	5V_System_power_supply		
58	VCC5V0_SYS_S3	VCC5V0_SYS_S3	5V_System_power_supply		
59	VCC5V0_SYS_S3	VCC5V0_SYS_S3	5V_System_power_supply		
60	VCC_3V3	VCC_3V3	3.3V_power_supply		
61	VCC_1V8	VCC_1V8	1.8V_power_supply		
62	SDMMC0_DETN/PCIE_CLKREQN_M0/GPIO0_A3_u	GPIO0_A3	SDMMC0_detect_input	3.3V	I/O UP
63	SDMMC0_CMD/TEST_CLKO/GPIO4_A0_u	SDMMC0_CMD	SDMMC0_command_output	3.3V	I/O UP
64	SDMMC0_CLK/GPIO4_A1_d	SDMMC0_CLK	SDMMC0_clock_output	3.3V	I/O DOWN
65	SDMMC0_D0/UART2_TX_M0/GPIO4_A2_u	SDMMC0_D0	SDMMC0_data_port	3.3V	I/O UP
66	SDMMC0_D1/UART2_RX_M0/GPIO4_A3_u	SDMMC0_D1	SDMMC0_data_port	3.3V	I/O UP
67	SDMMC0_D2/JTAG_TCK/GPIO4_A4_u	SDMMC0_D2/JTAG_TCK	SDMMC0_data_port/_JTAG_TCK_for_AP	3.3V	I/O UP
68	SDMMC0_D3/JTAG_TMS/GPIO4_A5_u	SDMMC0_D3/JTAG_TMS	SDMMC0_data_port/_JTAG_TMS_for_MCU	3.3V	I/O UP
69	GND	GND	GND		
70	UART0_TX/GPIO0_B2_d	GPIO0_B2	LCD_power_enable_,active_high	1.8V	I/O DOWN
71	UART0_CTS/GPIO0_B4_u	GPIO0_B4	touch controler interrupt input_,active_low	1.8V	I/O UP
72	PCIE_WAKE_M1/PWM2/GPIO0_C5_d	GPIO0_C5	LCD backlight enable,active_high	1.8V	I/O DOWN
73	PWM1/UART3_TX/GPIO0_C3_d	PWM1_LCD_BL	Control the LCD backlight brightness	1.8V	I/O DOWN
74	GND	GND	GND		
75	DPHY_TX_D0N	MIPI_DSI_D0N	MIPI-DSI differential lane 0 nositive		
76	DPHY_TX_D0P	MIPI_DSI_D0P	MIPI-DSI differential lane 0 pegatiy		
77	GND	GND	GND		
78	DPHY_TX_D1N	MIPI_DSI_D1N	MIPI-DSI differential lane 1 nositive		
79	DPHY_TX_D1P	MIPI_DSI_D1P	MIPI-DSI differential lane 1 pegatiy		
80	GND	GND	GND		
81	DPHY_TX_D2N	MIPI_DSI_D2N	MIPI-DSI differential clock lane nositive		
82	DPHY_TX_D2P	MIPI_DSI_D2P	MIPI-DSI differential clock lane pegative		
83	GND	GND	GND		
84	DPHY_TX_CLKN	MIPI_DSI_CLKN	MIPI-DSI differential lane 2 nositive		
85	DPHY_TX_CLKP	MIPI_DSI_CLKP	MIPI-DSI differential lane 2 pegative		
86	GND	GND	GND		
87	DPHY_TX_D3N	MIPI_DSI_D3N	MIPI-DSI differential lane 3 nositive		
88	DPHY_TX_D3P	MIPI_DSI_D3P	MIPI-DSI differential lane 3 pegative		
89	GND	GND	GND		
90	I2C1_SDA/GPIO0_C1_d	I2C1_SDA_TP	Touch the i2c_interface	1.8V	I/O DOWN
91	I2C1_SCL/GPIO0_C0_d	I2C1_SCL_TP	Touch the i2c_interface	1.8V	I/O DOWN
92	LCDC_D9/UART5_RX/I2C4_SDA/GPIO3_C3_d	I2C4_SDA	I2C serial port 4	1.8V	I/O DOWN
93	LCDC_D8/UART5_TX/I2C4_SCL/GPIO3_C2_d	I2C4_SCL	I2C serial port 4	1.8V	I/O DOWN
94	PCIE_CLKREQN_M1/UART3_CTS/GPIO0_C6_d	GPIO0_C6	Fan_power_control		I/O DOWN
95	TYPEC_TXP2	TYPEC_TXP2	TYPECO positive half of second SuperSpeedTX differential pair		
96	TYPEC_TXN2	TYPEC_TXN2	TYPECO nositive half of second SuperSpeedTX differential pair		
97	GND	GND	GND		
98	TYPEC_RXP2	TYPEC_RXP2	TYPECO pegative half of second SuperSpeedRX differential pair.		
99	TYPEC_RXN2	TYPEC_RXN2	TYPECO negative half of second SuperSpeedRX differential pair.		
100	GND	GND	GND		

X2 Connector

PIN	Core board pin definition	Default function	Defual function description	IO Power domain	Pad type IO Pull
1	GND	GND			
2	I2SO_SCLK_TX/ISP_PRELIGHTTRIG/GPIO3_B7_d/I2SO_SCLK_RX/PDM_CLKO/GPIO3_B0_d	I2SO_SCLK_TX/RX	I2S 0 port, for audio codec	1.8V	I/O DOWN
3	I2SO_SDI0/PDM_SDI0/GPIO3_C1_d	I2SO_SDI0	I2S 0 port, for audio codec	1.8V	I/O DOWN
4	I2SO_SDO0/ISP_SHUTTERTRIG/GPIO3_C0_d	I2SO_SDO0	I2S 0 port, for audio codec	1.8V	I/O DOWN
5	I2SO_LRCK_TX/ISP_FLASHTRIGOUT/GPIO3_B6_d I2SO_SCLK_TX/ISP_PRELIGHTTRIG/GPIO3_B7_d	I2SO_LRCK_TX/RX	I2S 0 port, for audio codec	1.8V	I/O DOWN
6	I2SO_MCLK/ISP_SHUTTEREN/GPIO3_B5_d	I2SO_MCLK	I2S 0 port, for audio codec	1.8V	I/O DOWN
7	GND	GND	GND		I/O DOWN
8	NC	NC	NC		
9	NC	NC	NC		
10	GND	GND	GND		
11	NC	NC	NC		
12	NC	NC	NC		
13	GND	GND	GND		
14	NC	NC	NC		
15	NC	NC	NC		
16	GND	GND	GND		
17	NC	NC	NC		
18	NC	NC	NC		
19	GND	GND	GND		
20	PCIE_TX0P/USB3_SSTXP	PCIE_TX0P	PCIE differential lane 0 positive input		
21	PCIE_TX0N/USB3_SSTXN	PCIE_TX0N	PCIE differential lane 0 negative input		
22	GND	GND	GND		
23	PCIE_RX0P/USB3_SSRXP	PCIE_RX0P	PCIE differential lane 0 positive input		
24	PCIE_RX0N/USB3_SSRXN	PCIE_RX0N	PCIE differential lane 0 negative input		
25	GND	GND	GND		
26	PCIE_REFCLKP	PCIE_REF_CLKP	PCIE 100MHz reference clock as input to PLL		
27	PCIE_REFCLKN	PCIE_REF_CLKN	PCIE 100MHz reference clock as input to PLL		
28	I2SO_SDI1/PDM_SDI1/GPIO3_A7_d	GPIO3_A7	PCIE power enable	1.8V	I/O DOWN
29	PCIE_PERST_M1/GPIO0_B6_u	PCIE_PRST	PCIE reset output	1.8V	I/O UP
30	GND	GND	GND		
31	LAN_MDI0+	LAN_MDI0+	LAN_MDI0+		
32	LAN_MDI0-	LAN_MDI0-	LAN_MDI0-		
33	GND	GND	GND		
34	LAN_MDI1+	LAN_MDI1+	LAN_MDI1+		
35	LAN_MDI1-	LAN_MDI1-	LAN_MDI1-		
36	GND	GND	GND		
37	LAN_MDI2+	LAN_MDI2+	LAN_MDI2+		
38	LAN_MDI2-	LAN_MDI2-	LAN_MDI2-		
39	GND	GND	GND		
40	LAN_MDI3+	LAN_MDI3+	LAN_MDI3+		
41	LAN_MDI3-	LAN_MDI3-	LAN_MDI3-		
42	GND	GND	GND		
43	VCC_LAN	VCC_LAN	LAN_power_supply		
44	LED1_AD1	LED1_AD1	LAN_Work_LED		
45	LED0_AD0	LED0_AD0	LAN_Work_LED		
46	CIF_CLKOUT/ROM11_CLK/GPI02_B7_d	ROM11_CLK	camera_MCLK	1.8V	I/O UP
47	GND	GND	GND		
48	ADC_IN2	ADC2_KEY_IN	RECOVER		
49	UART3_RTS/GPIO0_C7_d	GPIO0_C7	camera_power_enable_,active_high	1.8V	I/O DOWN
50	GND	GND	GND		
51	GND	GND	GND		
52	DPHY_RX_CLKP	MIPI_CSI_CLKP	MIPI-CSI differential clock lane positive		
53	DPHY_RX_CLKN	MIPI_CSI_CLKN	MIPI-CSI differential clock lane negative		
54	GND	GND	GND		
55	DPHY_RX_D0P	MIPI_CSI_D0P	MIPI-CSI differential lane 0 positive		
56	DPHY_RX_D0N	MIPI_CSI_D0N	MIPI-CSI differential lane 0 negative		
57	GND	GND	GND		
58	DPHY_RX_D1P	MIPI_CSI_D1P	MIPI-CSI differential lane 1 positive		
59	DPHY_RX_D1N	MIPI_CSI_D1N	MIPI-CSI differential lane 1 negative		
60	GND	GND	GND		
61	DPHY_RX_D2P	MIPI_CSI_D2P	MIPI-CSI differential lane 2 positive		
62	DPHY_RX_D2N	MIPI_CSI_D2N	MIPI-CSI differential lane 2 negative		
63	GND	GND	GND		
64	DPHY_RX_D3P	MIPI_CSI_D3P	MIPI-CSI differential lane 3 positive		
65	DPHY_RX_D3N	MIPI_CSI_D3N	MIPI-CSI differential lane 3 negative		
66	GND	GND	GND		
67	NC	NC	NC		
68	NC	NC	NC		
69	USB_HOST_DP	USB_HOST_DP	USB_HOST_Data_Plus_port		
70	USB_HOST_DM	USB_HOST_DM	USB_HOST_Data_Minus_port		
71	GND	GND	GND		
72	PCIE_TX1P	PCIE_TX1P	PCIE differential lane 1 positive input		
73	PCIE_TX1N	PCIE_TX1N	PCIE differential lane 1 negative input		
74	GND	GND	GND		
75	PCIE_RX1P	PCIE_RX1P	PCIE differential lane 1 positive input		
76	PCIE_RX1N	PCIE_RX1N	PCIE differential lane 1 negative input		
77	GND	GND	GND		
78	PCIE_WAKE_M0/GPIO0_A7_u	GPIO0_A7	PCIE_power_enable		I/O UP
79	GND	GND	GND		
80	SPKN_OUT	SPKN_OUT	Negative speaker driver output		
81	SPKP_OUT	SPKP_OUT	Positive speaker driver output		
82	GND	GND	GND		
83	MIC1P	MIC1_IN	input_of_the_Microphone		
84	ADC_IN3	ADC3_HP_HOOK	microphone to detect		
85	GND	GND	GND		
86	HPL_OUT	HPL	Left channel output of the headphone		
87	HP_SNS	HP_SNS	Reference ground for the headphone		
88	HPR_OUT	HPR	Right channel output of the headphone		
89	GND	GND	GND		
90	I2SO_SDO2/I2C2_SCL_M0/LCDC_VSYNC_M1/GPIO3_B3	I2C2_SCL	Camera I2C interface	1.8V	I/O DOWN
91	I2SO_SDI1/I2C2_SDA_M0/GPIO3_B4_d	I2C2_SDA	Camera I2C interface	1.8V	I/O DOWN
92	NC	NC	NC		
93	NC	NC	NC		
94	NC	NC	NC		
95	NC	NC	NC		
96	NC	NC	NC		
97	GND	GND	GND		
98	NC	NC	NC		
99	NC	NC	NC		
100	GND	GND	GND		